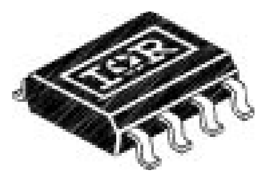
International
IOR Rectifier

PD – 91746B
PD – 91747B

IRF7805/IRF7807

HEXFET® Chip-Set for DC-DC Converters

- N Channel Application Specific MOSFETs
- Ideal for Mobile DC-DC Converters
- Low Conduction Losses
- Low Switching Losses



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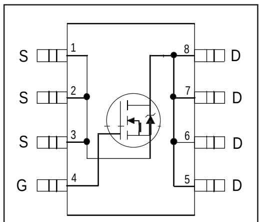

Top View

Description

These new devices employ advanced HEXFET Power MOSFET technology to achieve an unprecedented balance of on-resistance and gate charge. The reduced conduction and switching losses make them ideal for high efficiency DC-DC Converters that power the latest generation of mobile microprocessors.

The IRF7805/IRF7807 combination offers maximum efficiency for mobile CPU core DC-DC converters, while a pair of IRF7807 devices provides the best cost/performance solution for system voltages, such as 3.3V and 5V.

Device Features

	IRF7805	IRF7807
Vds	30V	30V
Rds(on)	11mΩ	25mΩ
Qg	31nC	17nC
Qsw	11.5nC	5.2nC
Qoss	36nC	16.8nC

Absolute Maximum Ratings

Parameter		Symbol	IRF7805	IRF7807	Units
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Drain or Source	25°C	I_D	13	8.3	A
Current ($V_{GS} \geq 4.5V$)	70°C		10	6.6	
Pulsed Drain Current①		I_{DM}	100	66	
Power Dissipation	25°C	P_D	2.5		W
	70°C		1.6		
Junction & Storage Temperature Range		T_J, T_{STG}	–55 to 150		°C
Continuous Source Current (Body Diode)①		I_S	2.5	2.5	A
Pulsed source Current		I_{SM}	106	66	

Thermal Resistance

Parameter		Max.	Units
Maximum Junction-to-Ambient③	$R_{\theta JA}$	50	°C/W

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Electrical Characteristics

Parameter		IRF7805			IRF7807				
Parameter		**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Drain-to-Source Breakdown Voltage*	$V_{(BR)DSS}$	30	–	–	30	–	–	V	V_{GS} = 0V, I_D = 250µA
Static Drain-Source on Resistance*	$R_{DS}(on)$		9.2	11		17	25	mΩ	V_{GS} = 4.5V, I_D = 7A②
Gate Threshold Voltage*	$V_{GS}(th)$	1.0			1.0			V	V_{DS} = V_{GS}, I_D = 250µA
Drain-Source Leakage Current*	I_{DSS}			30			30	µA	V_{DS} = 24V, V_{GS} = 0
				150			150		V_{DS} = 24V, V_{GS} = 0, Tj = 100°C
Gate-Source Leakage Current*	I_{GSS}			±100			±100	nA	V_{GS} = ±12V
Total Gate Charge*	Q_g		22④	31④		12	17		V_{GS} = 5V, I_D = 7A
Pre-Vth Gate-Source Charge	Q_{gs1}		3.7			2.1			V_{DS} = 16V, I_D = 7A
Post-Vth Gate-Source Charge	Q_{gs2}		1.4			0.76		nC	
Gate to Drain Charge	Q_{gd}		6.8			2.9			
Switch Charge* (Q_{gs2} + Q_{gd})	Q_{SW}		8.2	11.5		3.66	5.2		
Output Charge*	Q_{oss}		30	36		14	16.8		V_{DS} = 16V, V_{GS} = 0
Gate Resistance	R_g		1.7			1.2		Ω	
Turn-on Delay Time	$t_d(on)$		16			12			V_{DD} = 16V
Rise Time	t_r		20			17		ns	I_D = 7A
Turn-off Delay Time	t_d (off)		38			25			R_g = 2Ω
Fall Time	t_f		16			6			V_{GS} = 4.5V Resistive Load

Source-Drain Rating & Characteristics

Parameter		Min	Typ	Max	Min	Typ	Max	Units	Conditions
Diode Forward Voltage*	V_{SD}			1.2			1.2	V	I_S = 7A②, V_{GS} = 0V
Reverse Recovery Charge⑤	Q_{rr}		88			80		nC	di/dt = 700A/µs V_{DS} = 16V, V_{GS} = 0V, I_S = 7A
Reverse Recovery Charge (with Parallel Schottky)⑤	$Q_{rr(s)}$		55			50			di/dt = 700A/µs (with 10BQ040) V_{DS} = 16V, V_{GS} = 0V, I_S = 7A

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Pulse width ≤ 300 µs; duty cycle ≤ 2%.
③ When mounted on 1 inch square copper board, t < 10 sec.
④ Measured at V_{DS} < 100mV. This approximates actual operation of a synchronous rectifier.
⑤ Typ = measured - Q_{oss}
* Devices are 100% tested to these parameters.

Power MOSFET Selection for DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}{}^{2} \times R_{ds(on)}\right) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f\right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2}, can be seen from Fig 1.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached (t1) and the time the drain current rises to I_{dmax} (t2) at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure 2 shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

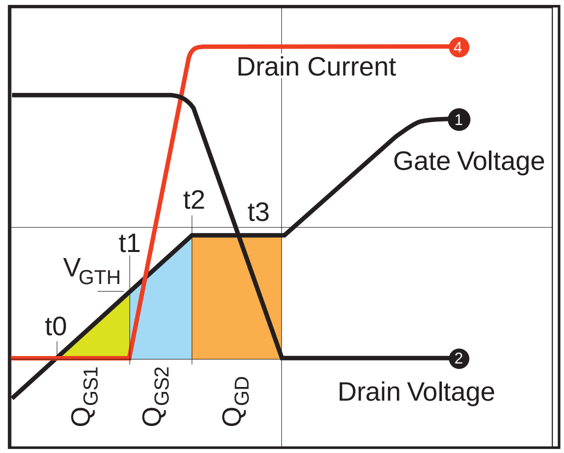


Figure 1: Typical MOSFET switching waveform

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P^{*}_{output}$$

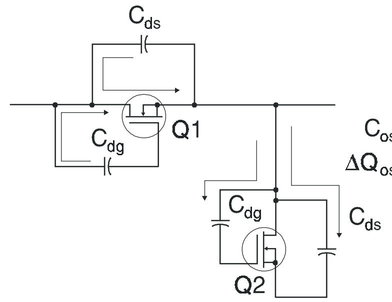
$$P_{loss} = \left(I_{rms}{}^{2} \times R_{ds(on)}\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right) + \left(Q_{rr} \times V_{in} \times f\right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in}. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.

Spice models for IRF7805 & IRF7807 can be downloaded in machine readable format at www.irf.com.



$$C_{oss} = C_{dg} + C_{ds}$$
$$\Delta Q_{oss} = C_{oss} \times \Delta V_{in}$$

Figure 2: Q_{oss} Characteristic

Typical Mobile PC Application

The performance of these new devices has been tested in circuit and correlates well with performance predictions generated by the system models. IRF7805 and IRF7807 were designed specifically for the mobile Pentium II CPU core supply. Fig 3 shows performance characteristics for this converter under low charge battery conditions, typical battery and worst case adapter input. An advantage of this new technology platform is that the MOSFETs it produces are suitable for both control FET and synchronous FET applications. This has been demonstrated with the 3.3V and 5V converters. (Fig 4 and Fig 5). In these applications the same MOSFET IRF7807 was used for both the control FET (Q1) and the synchronous FET (Q2). This provides a highly effective cost/performance solution.

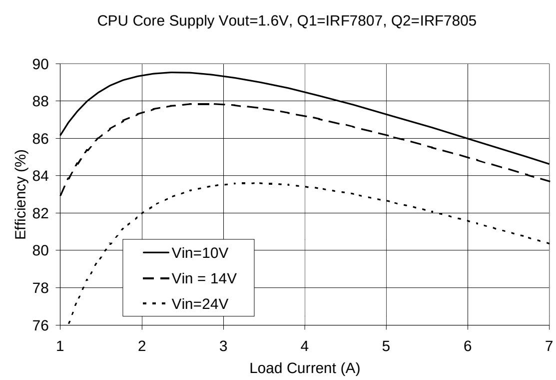


Figure 3

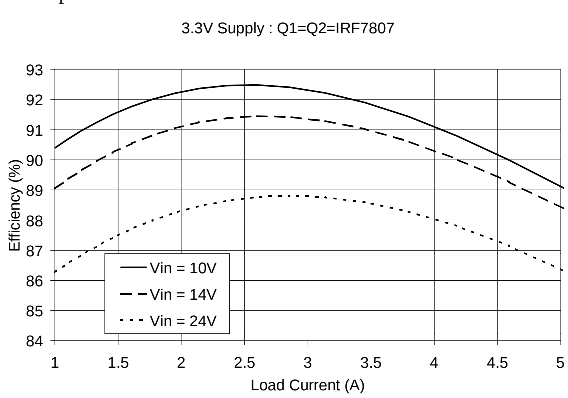


Figure 4

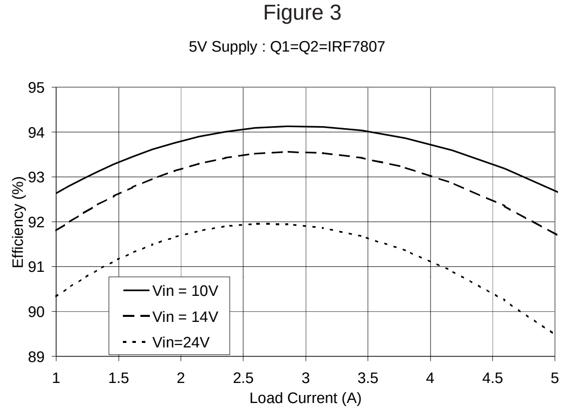


Figure 5

Typical Characteristics

IRF7805 **IRF7807**

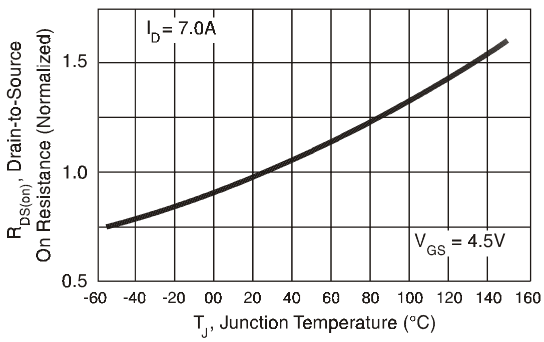


Figure 6. Normalized On-Resistance vs. Temperature

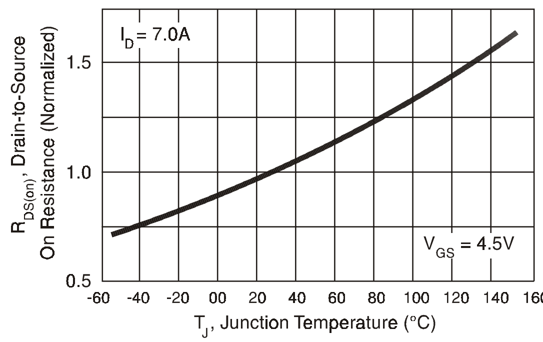


Figure 7. Normalized On-Resistance vs. Temperature

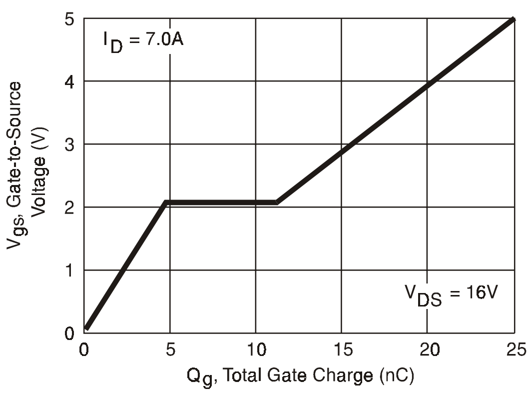


Figure 8. Typical Gate Charge vs. Gate-to-Source Voltage

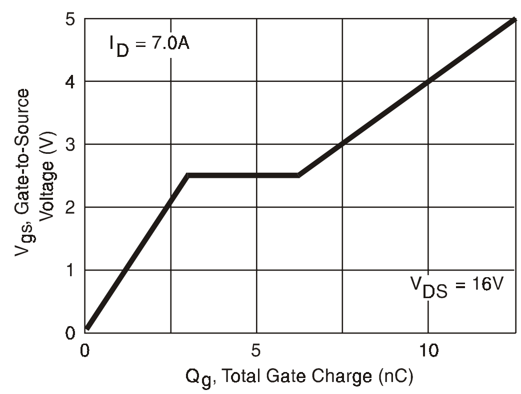


Figure 9. Typical Gate Charge vs. Gate-to-Source Voltage

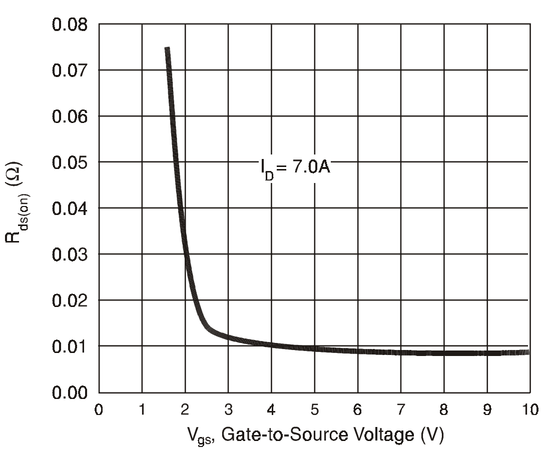


Figure 10. Typical Rds(on) vs. Gate-to-Source Voltage

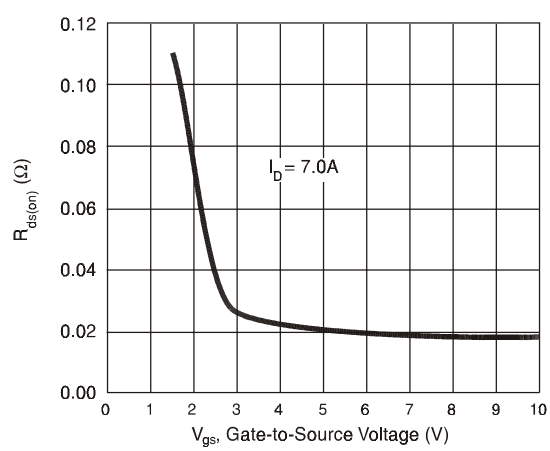


Figure 11. Typical Rds(on) vs. Gate-to-Source Voltage

IRF7805

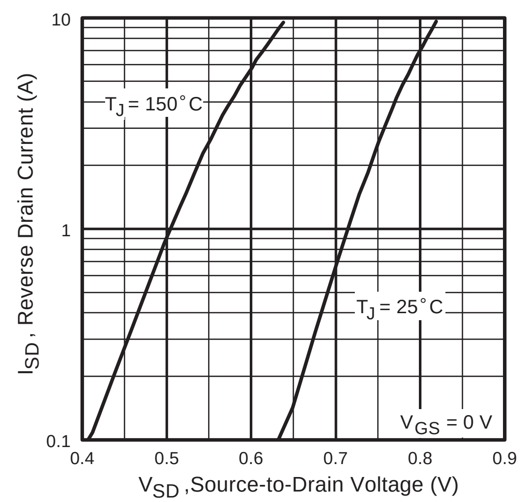


Figure 12. Typical Source-Drain Diode Forward Voltage

IRF7807

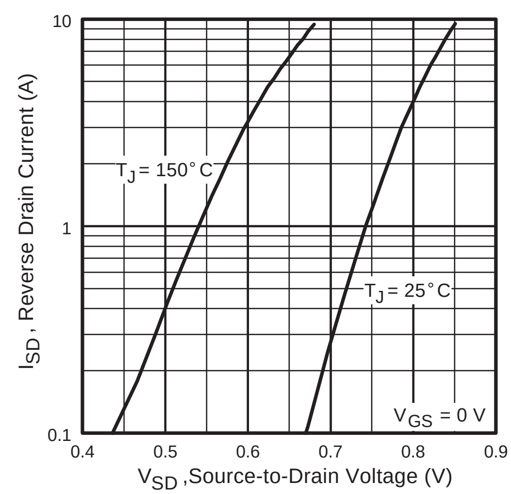


Figure 13. Typical Source-Drain Diode Forward Voltage

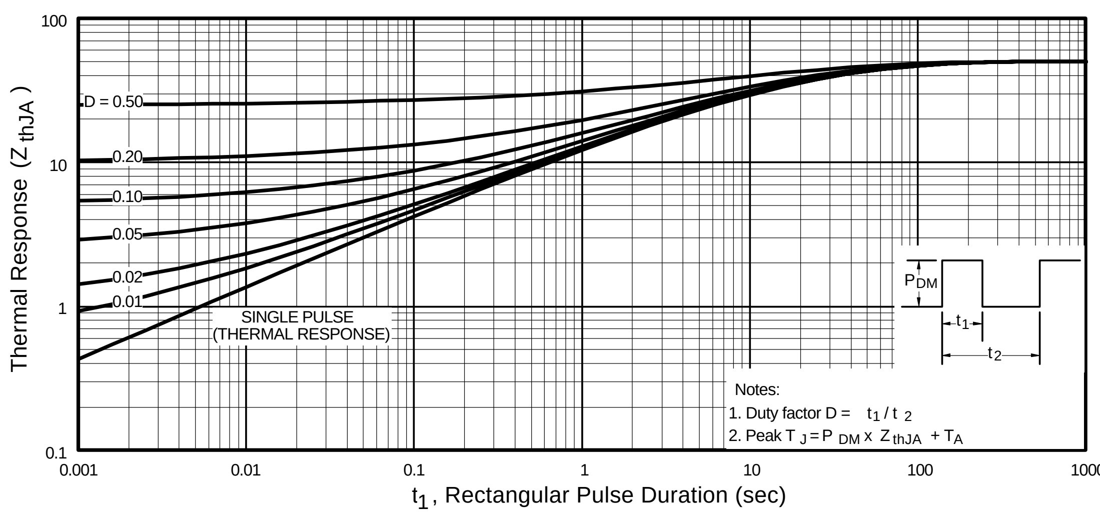
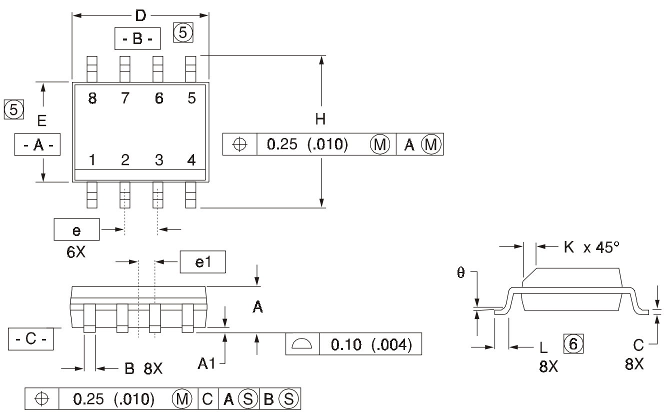


Figure 14. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

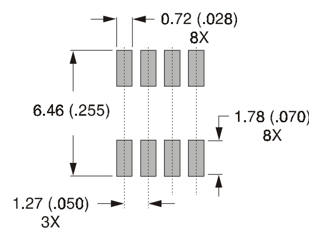
Package Outline

SO8 Outline



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.16	.050	0.41	1.27
θ	0°	8°	0°	8°

RECOMMENDED FOOTPRINT

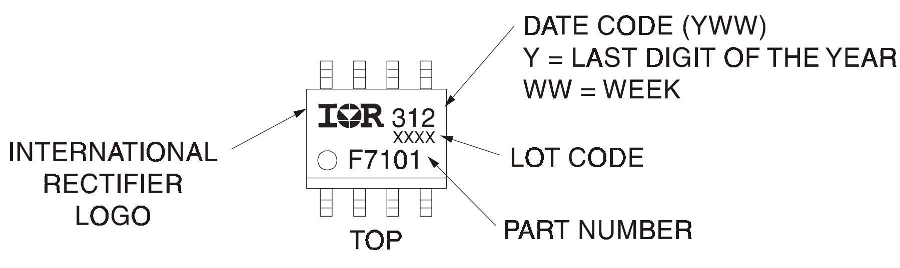


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS
   MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.006).
6. DIMENSIONS IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE..

Part Marking Information

SO8

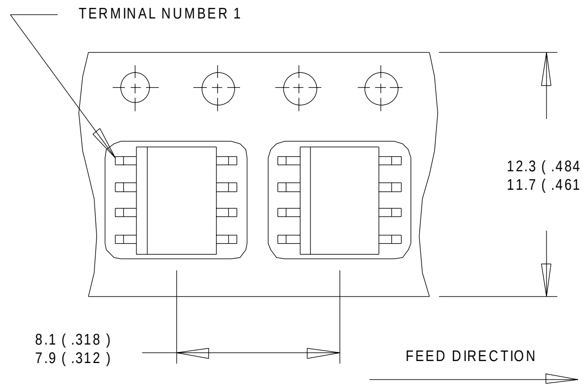
EXAMPLE: THIS IS AN IRF7101



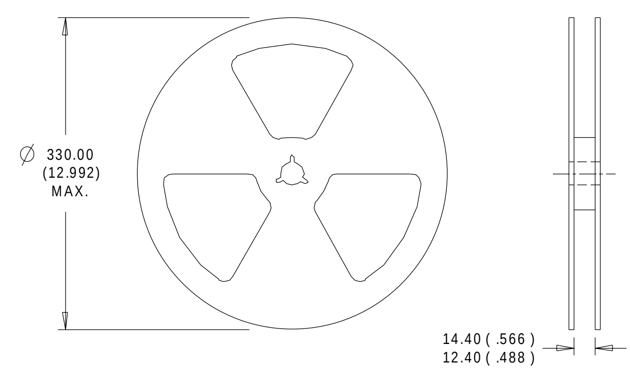
Tape & Reel Information

508

Dimensions are shown in millimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

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