PD - 94365

 $I_{D}$ 

16A

14A

# International

PROVISIONAL

V<sub>DSS</sub>

30V

# IRF6604

DirectFET<sup>TM</sup> Power MOSFET

R<sub>DS(on)</sub> max

 $11.5m\Omega@V_{GS} = 7.0V$ 

 $13m\Omega@V_{GS} = 4.5V$ 

- Application Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- Low Switching Losses
- Low Profile (<0.7 mm)
- Dual Sided Cooling Compatible
- Compatible with existing Surface Mount Techniques

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### Description

The IRF6604 combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET<sup>™</sup> packaging to achieve the lowest on-state resistance charge product in a package that has the footprint of an SO-8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, IMPROVING previous best thermal resistance by 80%.

The IRF6604 balances both low resistance and low charge along with ultra low package inductance to reduce both conduction and switching losses. The reduced total losses make this product ideal for high efficiency DC-DC converters that power the latest generation of processors operating at higher frequencies. The IRF6604 has been optimized for parameters that are critical in synchronous buck converters including Rds(on) and gate charge to minimize losses in the control FET socket.

### **Absolute Maximum Ratings**

	Parameter	Max.	Units
V <sub>DS</sub>	Drain- Source Voltage	30	V
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	59	
I <sub>D</sub> @ T <sub>A</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	15	
I <sub>D</sub> @ T <sub>A</sub> = 70°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	12.5	A
I <sub>DM</sub>	Pulsed Drain Current ①	130	
P <sub>D</sub> @T <sub>A</sub> = 25°C	Power Dissipation	5.0	w
P <sub>D</sub> @T <sub>A</sub> = 70°C	Power Dissipation	3.2	
	Linear Derating Factor	40	mW/°C
V <sub>GS</sub>	Gate-to-Source Voltage	±12	V
T <sub>J</sub> , T <sub>STG</sub>	Junction and Storage Temperature Range	-55 to + 150	°C

#### **Thermal Resistance**

Symbol	Parameter	Тур.	Max.	Units	
R <sub>θJA</sub>	Junction-to-Ambient3		25		
R <sub>0JA</sub>	Junction-to-Ambient		12.5		
R <sub>0JA</sub>	Junction-to-Ambient®		20	°C/W	
R <sub>θJC</sub>	Junction-to-Case6		3.0		
R <sub>0J-PCB</sub>	Junction-to-PCB mounted		1.0	1	

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# IRF6604

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# Static @ $T_J = 25^{\circ}C$ (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	30			V	$V_{GS} = 0V, I_D = 250 \mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	_	0.02		V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
D	Static Drain-to-Source On-Resistance		9.0	11.5	mΩ	V <sub>GS</sub> = 7.0V, I <sub>D</sub> = 16A ③
R <sub>DS(on)</sub>			10	13		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 14A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0		3.0	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
I <sub>DSS</sub>	Drain-to-Source Leakage Current			30	μA	$V_{DS} = 24V, V_{GS} = 0V$
USS	Drain to bource Leakage ourient			150	μΛ	$V_{DS} = 24V, V_{GS} = 0V, T_{J} = 100^{\circ}C$
I <sub>GSS</sub>	Gate-to-Source Forward Leakage			100	nA	V <sub>GS</sub> = 12 V
	Gate-to-Source Reverse Leakage			-100	ПА	V <sub>GS</sub> = -12 V

## Dynamic @ $T_J = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
9 <sub>fs</sub>	Forward Transconductance	TBA			S	V <sub>DS</sub> = 16V, I <sub>D</sub> = 15A
Qg	Total Gate Charge Cont FET		20	30		$V_{GS} = 5.0V, V_{DS} = 16V, I_{D} = 15A$
Qg	Total Gate Charge Sync FET		17			$V_{GS} = 5.0V, V_{DS} < 100mV$
Q <sub>gs1</sub>	Pre-Vth Gate-Source Charge		5.4			V <sub>DS</sub> = 16V, I <sub>D</sub> = 15A
Q <sub>gs2</sub>	Post-Vth Gate-Source Charge		1.4		nC	
Q <sub>gd</sub>	Gate to Drain Charge		7.0	10		
Q <sub>oss</sub>	Output Charge		12			$V_{DS} = 16V, V_{GS} = 0V$
R <sub>g</sub>	Gate Resistance		2.0		Ω	
t <sub>d(on)</sub>	Turn-On Delay Time		TBA			V <sub>DD</sub> = 16V
tr	Rise Time		TBA		ns	I <sub>D</sub> = 15A
t <sub>d(off)</sub>	Turn-Off Delay Time		TBA			$V_{GS} = 5.0 V$
t <sub>f</sub>	Fall Time		TBA			Clamped Inductive Load
Ciss	Input Capacitance		TBA			$V_{GS} = 0V$
Coss	Output Capacitance		TBA		pF	V <sub>DS</sub> = 16V ③
C <sub>rss</sub>	Reverse Transfer Capacitance		TBA			f = 1.0 MHz

## **Avalanche Characteristics**

Symbol	Parameter	Тур.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy@		164	mJ
I <sub>AR</sub>	Avalanche Current <sup>®</sup>		TBA	А

## **Diode Characteristics**

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
Is	Continuous Source Current			15		MOSFET symbol
	(Body Diode)			15		showing the
I <sub>SM</sub>	Pulsed Source Current			130	A	integral reverse 🔍 🗍
	(Body Diode) ①					p-n junction diode.
V <sub>SD</sub>	Diode Forward Voltage			1.2	V	$T_J = 25^{\circ}C, I_S = 15A, V_{GS} = 0V$ (3)
VSD	Didde Folward Voltage		TBA			$T_J = 125^{\circ}C, I_S = 15A, V_{GS} = 0V$ (3)
t <sub>rr</sub>	Reverse Recovery Time		TBA	TBA	ns	$T_J = 25^{\circ}C, I_F = 15A, V_R = 16V$
Q <sub>rr</sub>	Reverse Recovery Charge		41	50	nC	di/dt = 700A/µs ③
Q <sub>rr(s)</sub>	Reverse Recovery Charge		TBA	TBA	nC	di/dt = 100A/µs
	(with Parallel Schottky)					$V_{DS} = 16V, V_{GS} = 0V, I_{S} = 15A$

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DirectFET™ Pad Layout



PCB Pad Layout



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# IRF6604

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## DirectFET™ Outline Dimension



#### Notes:

- Repetitive rating; pulse width limited by max. junction temperature.
- ② Pulse width  $\leq$  400µs; duty cycle  $\leq$  2%.
- ③ Surface mounted on 1 in square Cu board
- ④ Used double sided cooling, mounting pad



- ⑤ Mounted on minimum footprint full size board with metalized back and with small clip heatsink
- © T<sub>C</sub> measured with thermal couple mounted to top (Drain) of part.

Data and specifications subject to change without notice. This product has been designed and qualified for the Consumer market. Qualification Standards can be found on IR's Web site.

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