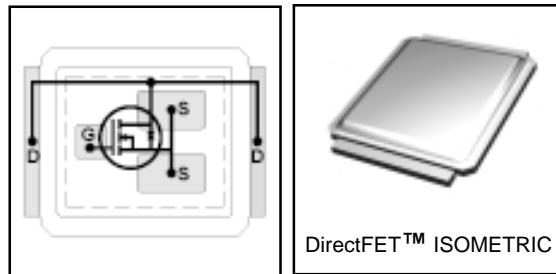


IRF6601

- Application Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- Low Switching Losses
- Low Profile (<0.7 mm)
- Dual Sided Cooling Compatible
- Compatible with existing Surface Mount Techniques

DirectFET™ Power MOSFET

V_{DSS}	R_{DS(on)} max	I_D
20V	3.8mΩ@V _{GS} = 10V	26A
	5.0mΩ@V _{GS} = 4.5V	21A



Description

The IRF6601 combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of an SO-8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, IMPROVING previous best thermal resistance by 80%.

The IRF6601 balances both low resistance and low charge along with ultra low package inductance to reduce both conduction and switching losses. The reduced total losses make this product ideal for high efficiency DC-DC converters that power the latest generation of processors operating at higher frequencies. The IRF6601 has been optimized for parameters that are critical in synchronous buck converters including R_{ds(on)}, gate charge and C_{dV/dt}-induced turn on immunity. The IRF6601 offers particularly low R_{ds(on)} and high C_{dV/dt} immunity for synchronous FET applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
V _{DS}	Drain- Source Voltage	20	V
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	85	A
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	26	
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V	20	
I _{DM}	Pulsed Drain Current ①	200	
P _D @ T _A = 25°C	Power Dissipation	3.6	W
P _D @ T _A = 70°C	Power Dissipation	2.3	
	Linear Derating Factor	28	mW/°C
V _{GS}	Gate-to-Source Voltage	±20	V
T _J , T _{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJA}	Junction-to-Ambient③	—	35	°C/W
R _{θJA}	Junction-to-Ambient④	—	12.5	
R _{θJA}	Junction-to-Ambient⑤	—	20	
R _{θJC}	Junction-to-Case⑥	—	3.0	
R _{θJ-PCB}	Junction-to-PCB mounted	—	1.0	

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{\text{GS}} = 0\text{V}, I_D = 100\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.019	—	$^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	—	3.8	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}, I_D = 26\text{A}$
		—	—	5.0		$V_{\text{GS}} = 4.5\text{V}, I_D = 21\text{A}$ ②
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	1.0	—	3.0	V	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{\text{DS}} = 16\text{V}, V_{\text{GS}} = 0\text{V}$
		—	—	100		$V_{\text{DS}} = 16\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 70^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{\text{GS}} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{\text{GS}} = -20\text{V}$

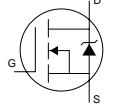
Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	50	—	—	S	$V_{\text{DS}} = 10\text{V}, I_D = 21\text{A}$
Q_g	Total Gate Charge Cont FET	—	36	54	nC	$I_D = 21\text{A}$
Q_{gs}	Gate-to-Source Charge	—	11	—		$V_{\text{DS}} = 16\text{V}$
Q_{gd}	Gate to Drain ("Miller")Charge	—	12	—		$V_{\text{GS}} = 4.5\text{V},$
Q_{oss}	Output Charge	—	48	—		$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = 16\text{V}$
$t_{d(\text{on})}$	Turn-On Delay Time	—	16	—		$V_{DD} = 15\text{V}$
t_r	Rise Time	—	140	—	ns	$I_D = 21\text{A}$
$t_{d(\text{off})}$	Turn-Off Delay Time	—	33	—		$R_G = 5.1\Omega$
t_f	Fall Time	—	110	—		$V_{\text{GS}} = 4.5\text{V}$ ②
C_{iss}	Input Capacitance	—	3440	—		$V_{\text{GS}} = 0\text{V}$
C_{oss}	Output Capacitance	—	2430	—	pF	$V_{\text{DS}} = 10\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	380	—		$f = 1.0\text{MHz}$

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	65	mJ
I_{AR}	Avalanche Current ①	—	21	A

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	28	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	200		
V_{SD}	Diode Forward Voltage	—	0.83	1.2	V	$T_J = 25^\circ\text{C}, I_S = 21\text{A}, V_{\text{GS}} = 0\text{V}$ ②
		—	0.68	—		$T_J = 125^\circ\text{C}, I_S = 21\text{A}, V_{\text{GS}} = 0\text{V}$ ②
t_{rr}	Reverse Recovery Time	—	60	90	ns	$T_J = 25^\circ\text{C}, I_F = 21\text{A}, V_R = 15\text{V}$
Q_{rr}	Reverse Recovery Charge	—	94	140	nC	$di/dt = 100\text{A}/\mu\text{s}$ ②
t_{rr}	Reverse Recovery Time	—	62	93	ns	$T_J = 125^\circ\text{C}, I_F = 21\text{A}, V_R = 15\text{V}$
Q_{rr}	Reverse Recovery Charge	—	88	130	nC	$di/dt = 100\text{A}/\mu\text{s}$ ②

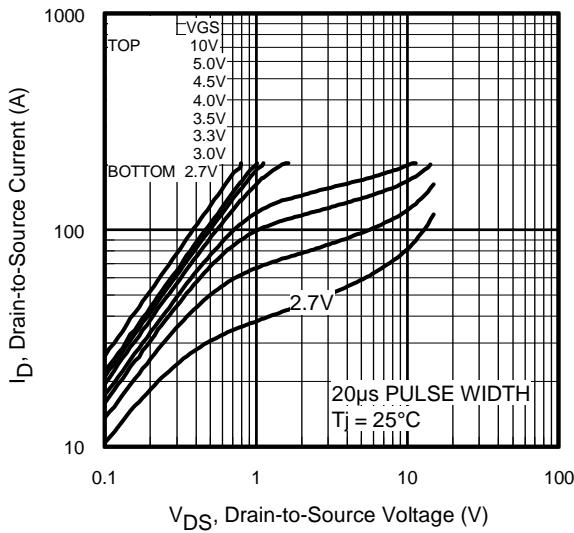


Fig 1. Typical Output Characteristics

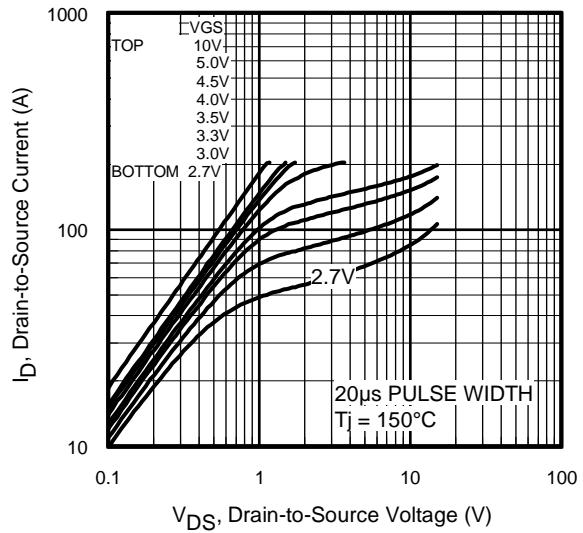


Fig 2. Typical Output Characteristics

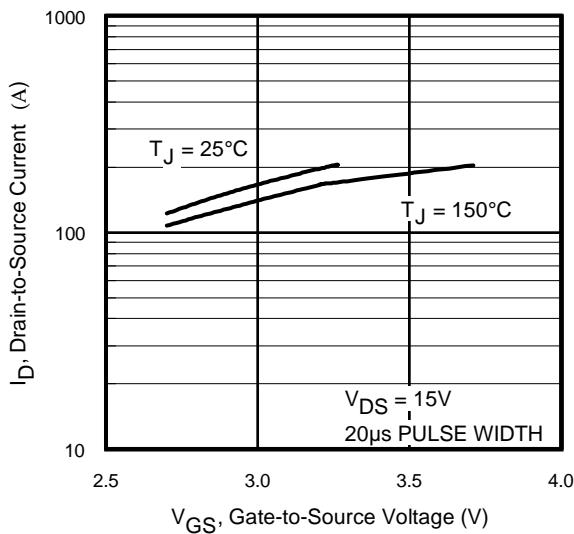


Fig 3. Typical Transfer Characteristics

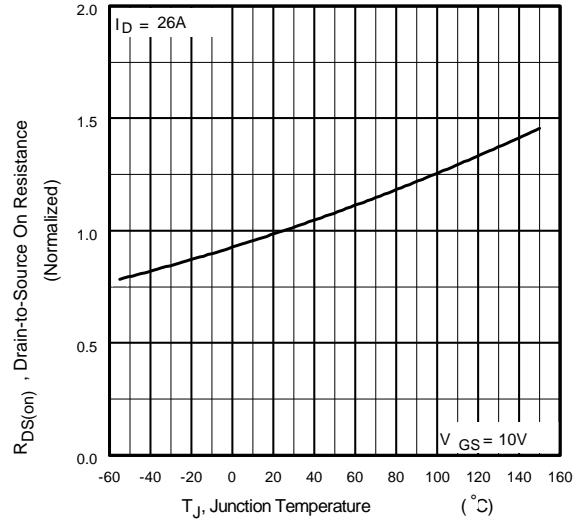


Fig 4. Normalized On-Resistance
Vs. Temperature

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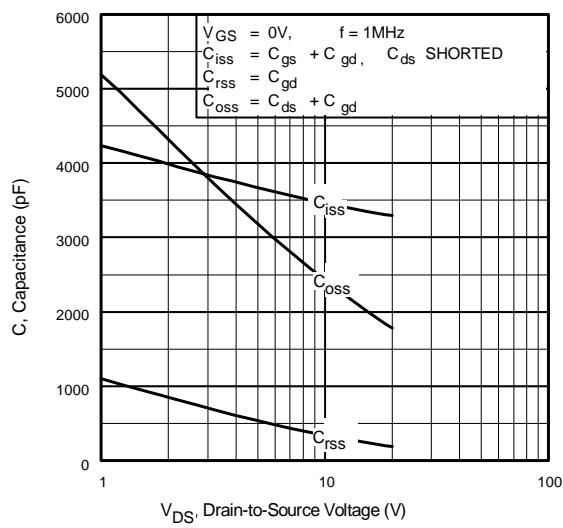


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

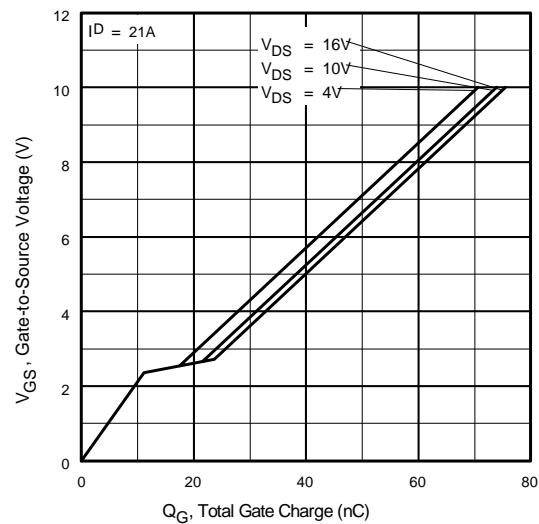


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

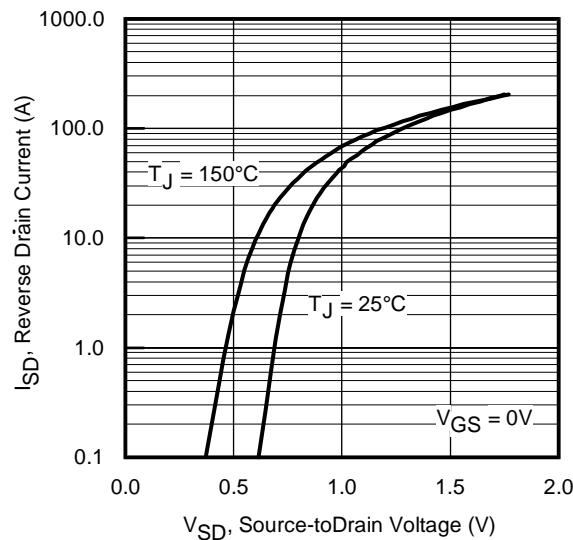


Fig 7. Typical Source-Drain Diode
Forward Voltage

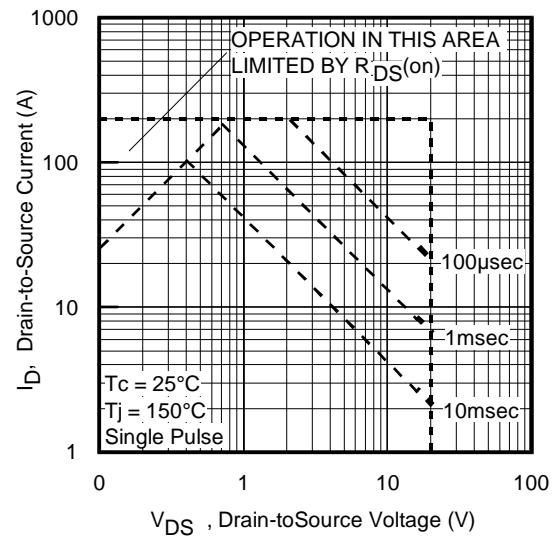


Fig 8. Maximum Safe Operating Area

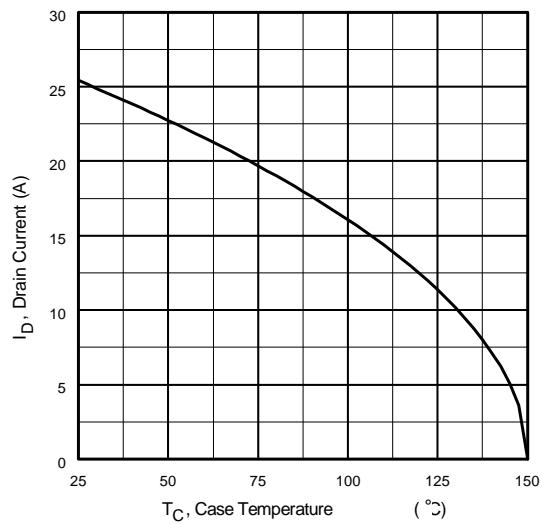


Fig 9. Maximum Drain Current Vs.
Ambient Temperature

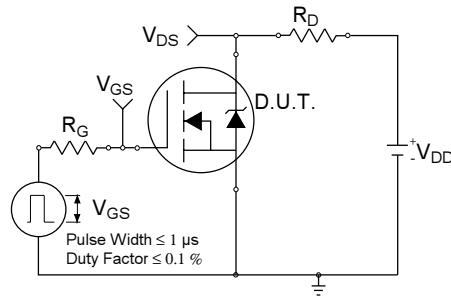


Fig 10a. Switching Time Test Circuit

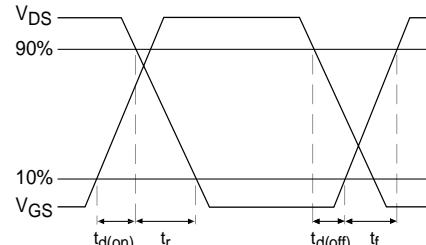


Fig 10b. Switching Time Waveforms

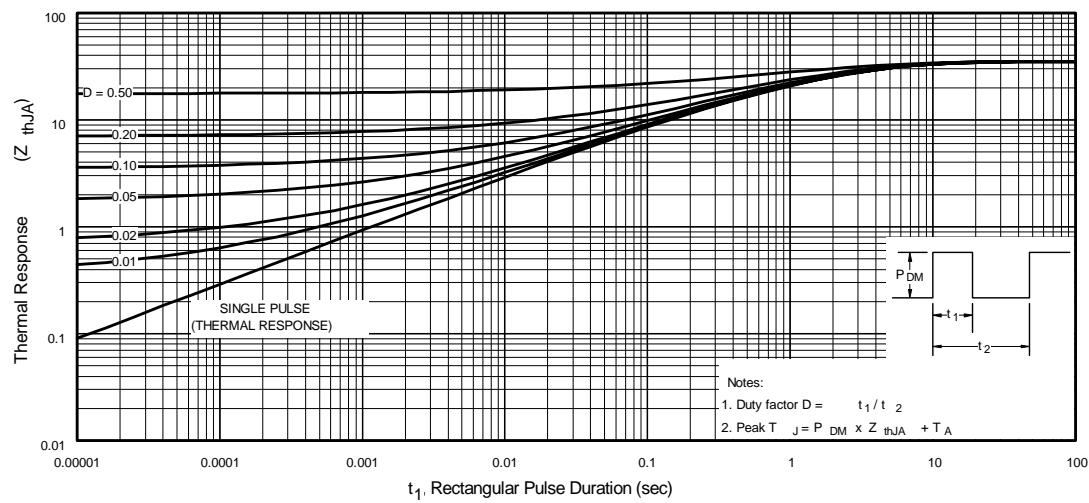


Fig 10. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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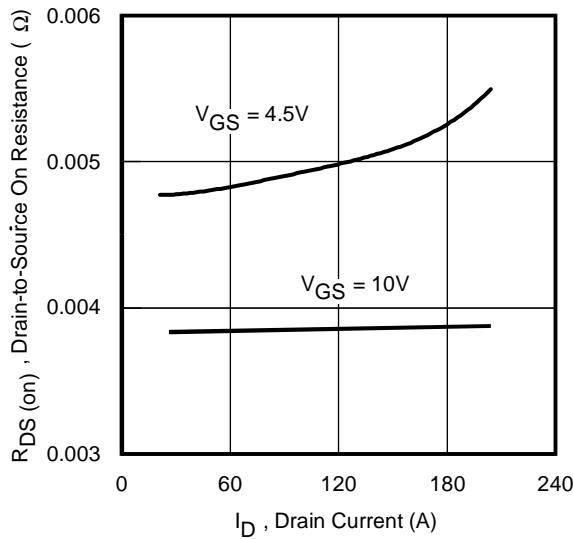


Fig 12. On-Resistance Vs. Drain Current

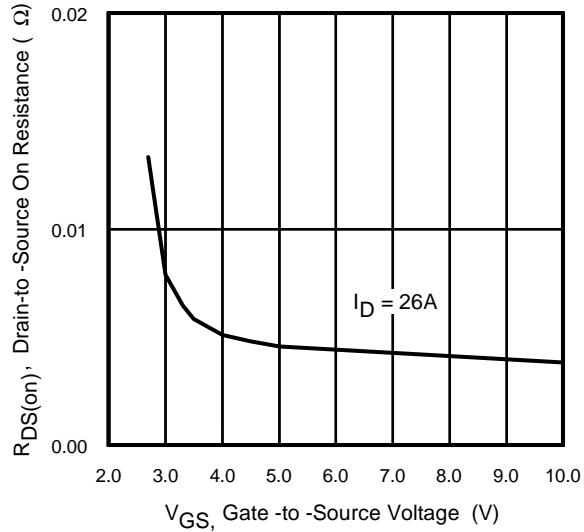


Fig 13. On-Resistance Vs. Gate Voltage

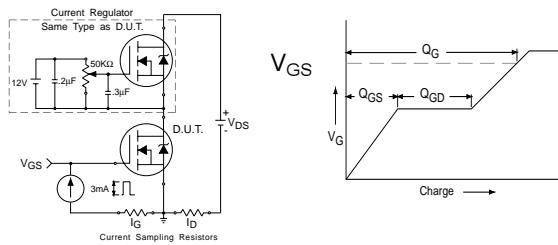


Fig 13a&b. Basic Gate Charge Test Circuit and Waveform

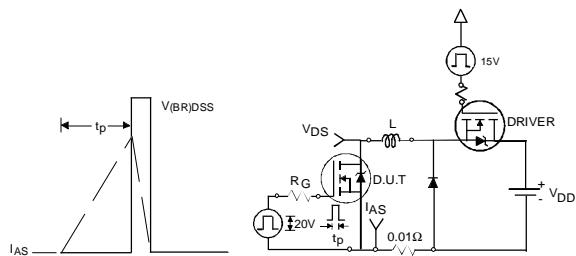


Fig 14a&b. Unclamped Inductive Test circuit and Waveforms

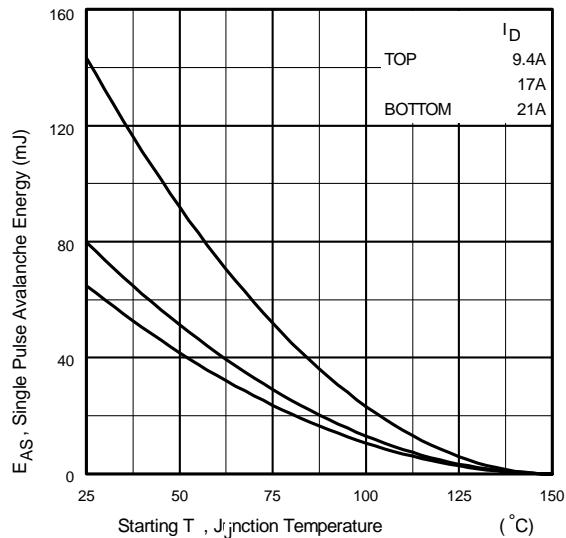
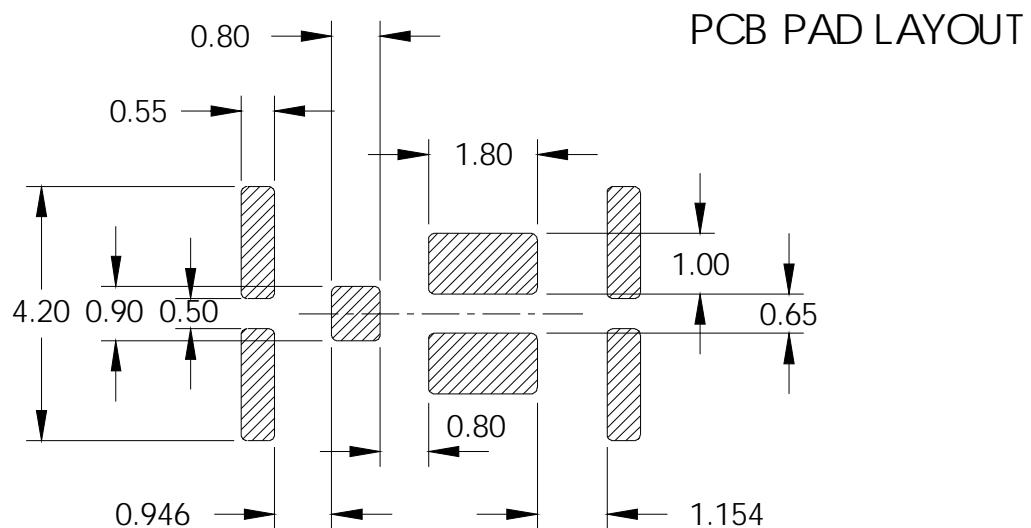
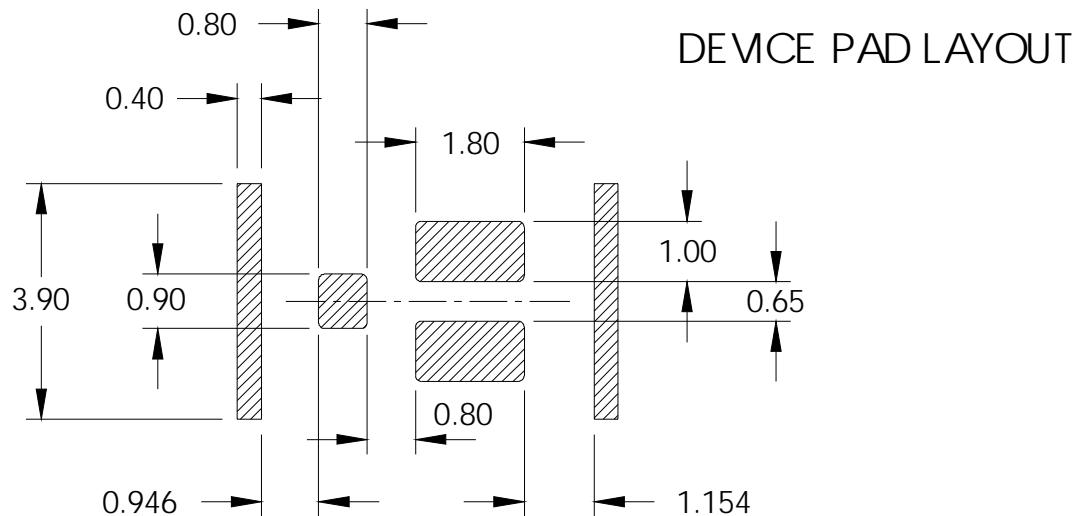


Fig 14c. Maximum Avalanche Energy Vs. Drain Current

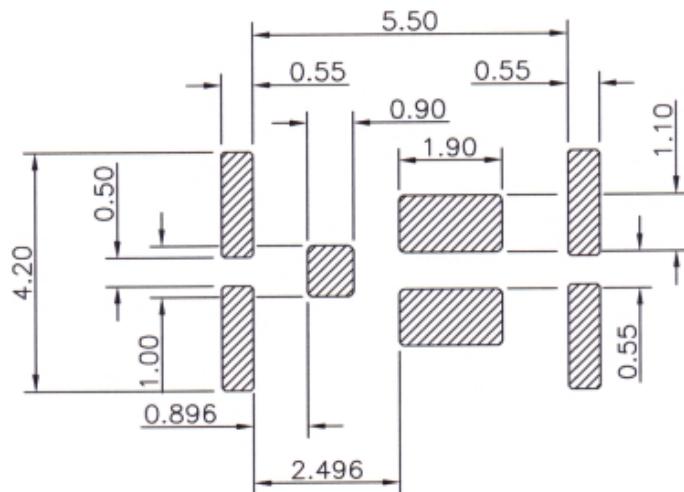
DirectFET™ Pad Layout



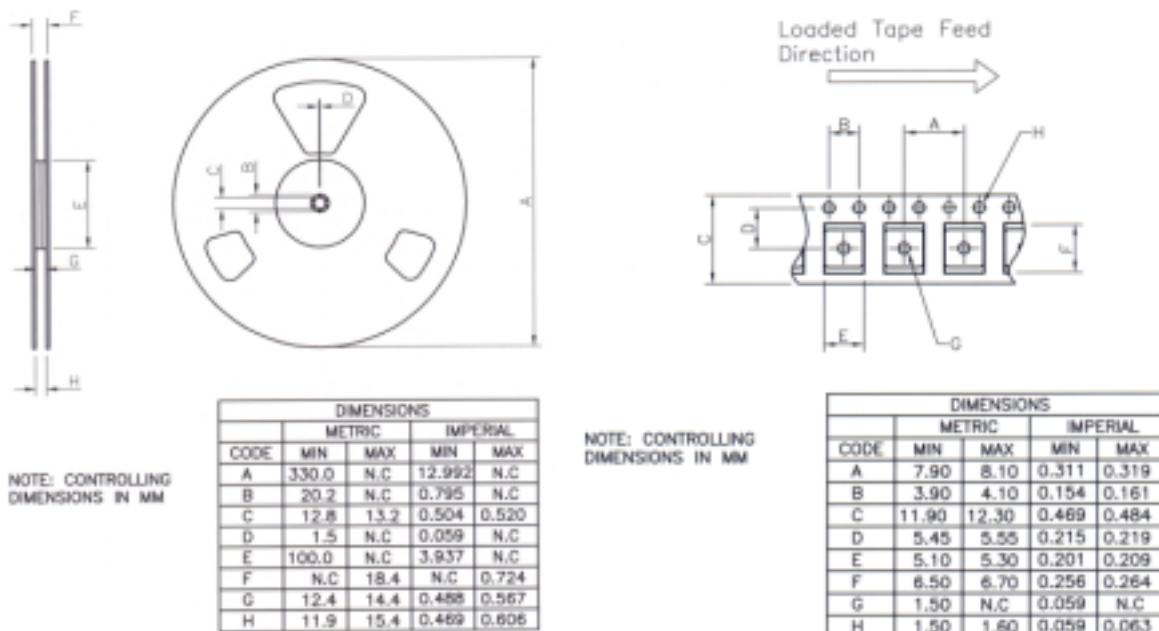
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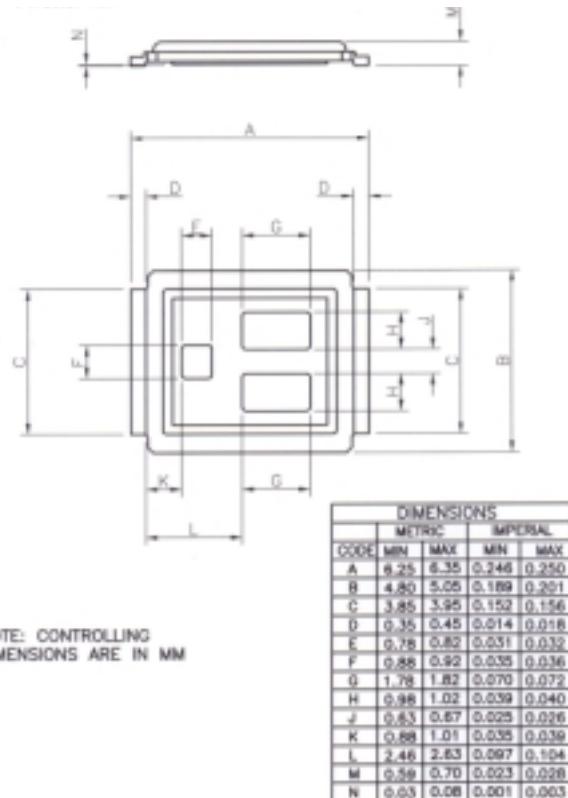
DirectFET™ Board Footprint



DirectFET™ Tape and Reel Dimension



DirectFET™ Outline Dimension



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ③ Surface mounted on 1 in square Cu board
- ④ Used double sided cooling, mounting pad
- ⑤ Mounted on minimum footprint full size board with metalized back and with small clip heatsink
- ⑥ T_C measured with thermal couple mounted to top (Drain) of part.
- ⑦ Starting $T_J = 25^\circ\text{C}$, $L = 0.30\text{mH}$, $R_G = 25\text{W}$, $I_{AS} = 21\text{A}$. (See Figure 14)

Data and specifications subject to change without notice.
 This product has been designed and qualified for the consumer market.
 Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
 TAC Fax: (310) 252-7903
 Visit us at www.irf.com for sales contact information.01/02
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