

Applications

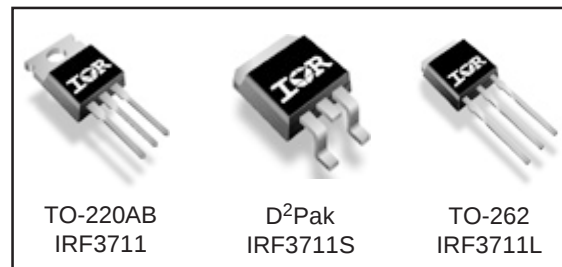
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- High Frequency Buck Converters for Server Processor Power Synchronous FET
- Optimized for Synchronous Buck Converters Including Capacitive Induced Turn-on Immunity

Benefits

- Ultra-Low Gate Impedance
- Very Low RDS(on) at 4.5V V_{GS}
- Fully Characterized Avalanche Voltage and Current

HEXFET® Power MOSFET

V _{DSS}	R _{DS(on)} max	I _D
20V	6.0mΩ	110A ^⑥



Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V _{DS}	Drain-Source Voltage	20	V
V _{GS}	Gate-to-Source Voltage	± 20	V
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	110 ^⑥	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	69	
I _{DM}	Pulsed Drain Current ^①	440	
P _D @ T _C = 25°C	Maximum Power Dissipation	120	W
P _D @ T _A = 25°C	Maximum Power Dissipation ^⑤	3.1	W
	Linear Derating Factor	0.96	W/°C
T _J , T _{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	1.04	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface ^④	0.50	—	
R _{θJA}	Junction-to-Ambient ^④	—	62	
R _{θJA}	Junction-to-Ambient (PCB mount) ^⑤	—	40	

Notes ① through ⑥ are on page 11

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IRF3711/3711S/3711L

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.022	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	4.7	6.0	m Ω	$V_{GS} = 10V, I_D = 15A$ ③
		—	6.2	8.5		$V_{GS} = 4.5V, I_D = 12A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 16V, V_{GS} = 0V$
		—	—	100		$V_{DS} = 16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -16V$

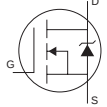
Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

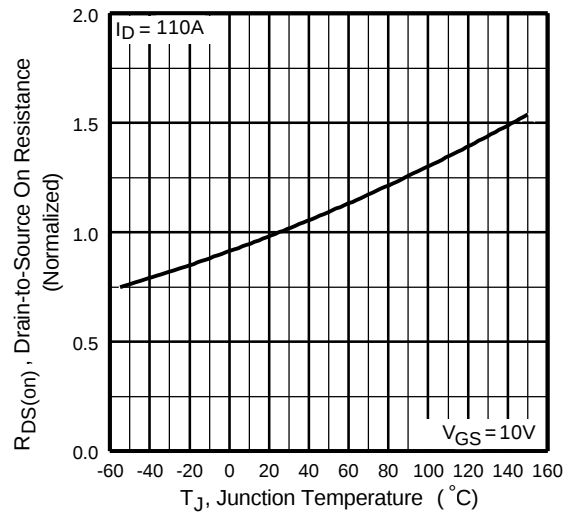
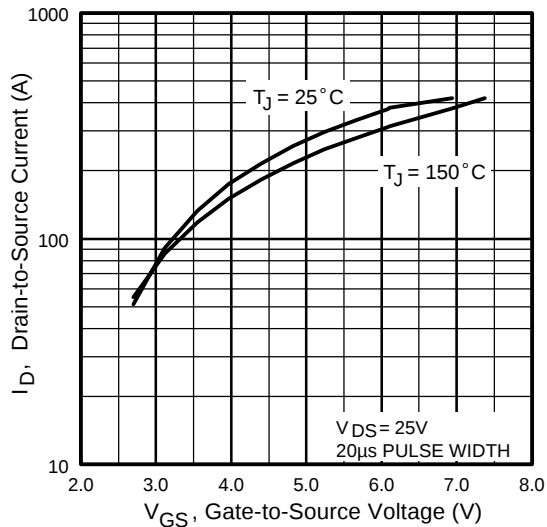
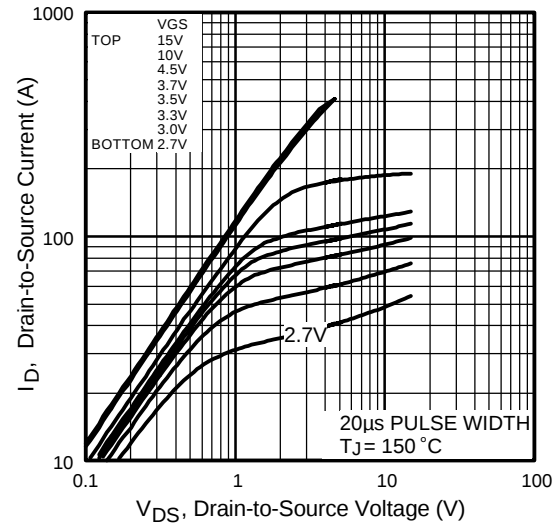
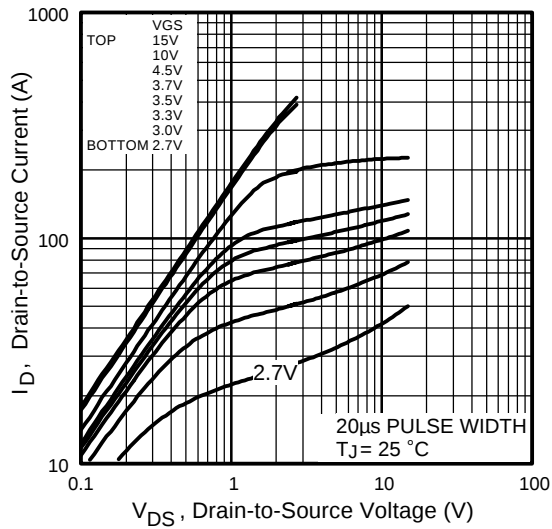
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	53	—	—	S	$V_{DS} = 16V, I_D = 30A$
Q_g	Total Gate Charge	—	29	44	nC	$I_D = 15A$
Q_{gs}	Gate-to-Source Charge	—	7.3	—		$V_{DS} = 10V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	8.9	—		$V_{GS} = 4.5V$
Q_{oss}	Output Gate Charge	—	33	—		$V_{GS} = 0V, V_{DS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	$V_{DD} = 10V$
t_r	Rise Time	—	220	—		$I_D = 30A$
$t_{d(off)}$	Turn-Off Delay Time	—	17	—		$R_G = 1.8\Omega$
t_f	Fall Time	—	12	—		$V_{GS} = 4.5V$ ③
C_{iss}	Input Capacitance	—	2980	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1770	—		$V_{DS} = 10V$
C_{rss}	Reverse Transfer Capacitance	—	280	—		$f = 1.0MHz$

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	460	mJ
I_{AR}	Avalanche Current①	—	30	A

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	110⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	440		
V_{SD}	Diode Forward Voltage	—	0.88	1.3	V	$T_J = 25^\circ\text{C}, I_S = 30A, V_{GS} = 0V$ ③
		—	0.82	—		$T_J = 125^\circ\text{C}, I_S = 30A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	50	75	ns	$T_J = 25^\circ\text{C}, I_F = 16A, V_R = 10V$
Q_{rr}	Reverse Recovery Charge	—	61	92	nC	$di/dt = 100A/\mu s$ ③
t_{rr}	Reverse Recovery Time	—	48	72	ns	$T_J = 125^\circ\text{C}, I_F = 16A, V_R = 10V$
Q_{rr}	Reverse Recovery Charge	—	65	98	nC	$di/dt = 100A/\mu s$ ③



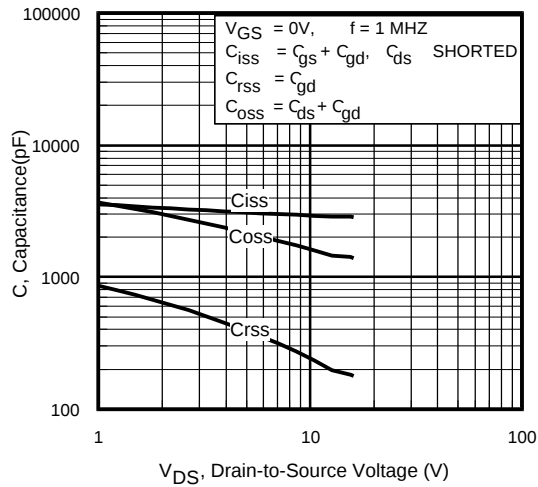


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

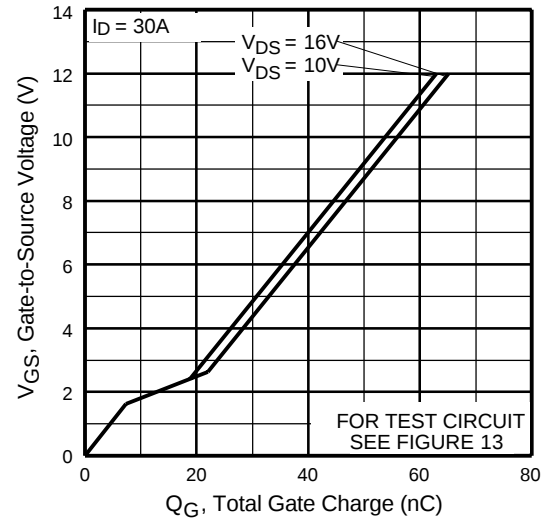


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

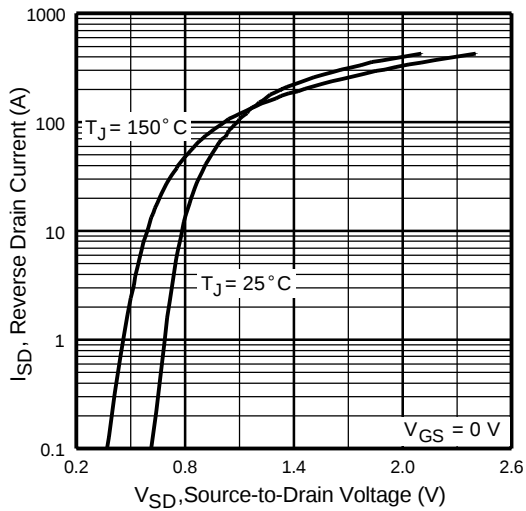


Fig 7. Typical Source-Drain Diode Forward Voltage

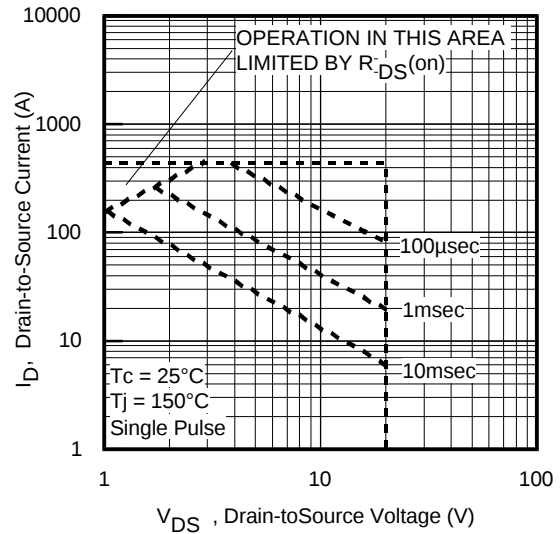


Fig 8. Maximum Safe Operating Area

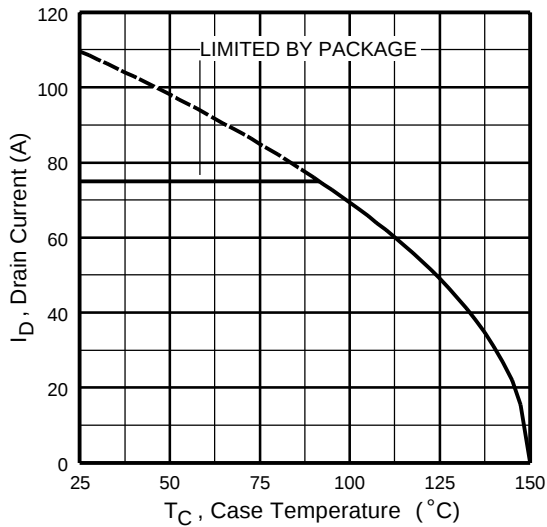


Fig 9. Maximum Drain Current Vs. Case Temperature



Fig 10a. Switching Time Test Circuit

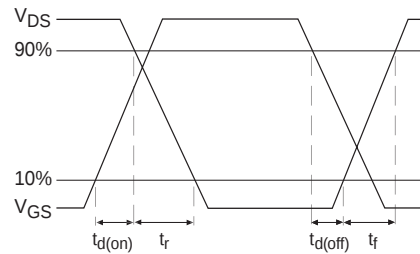


Fig 10b. Switching Time Waveforms

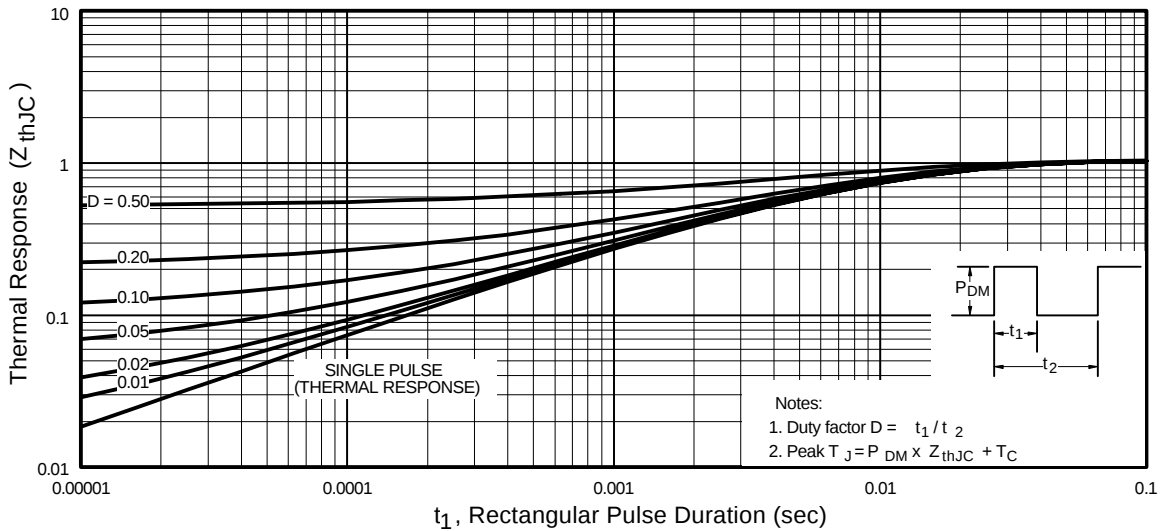


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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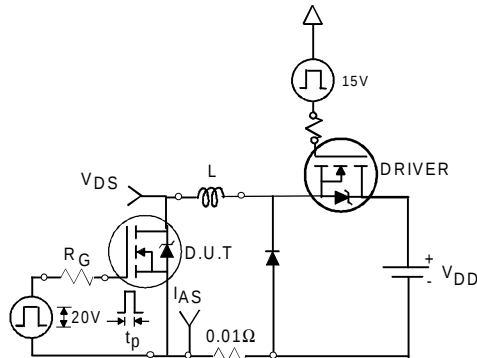


Fig 12a. Unclamped Inductive Test Circuit

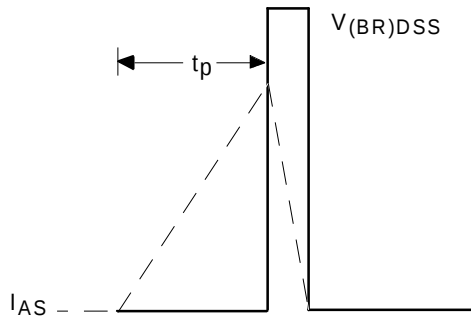


Fig 12b. Unclamped Inductive Waveforms

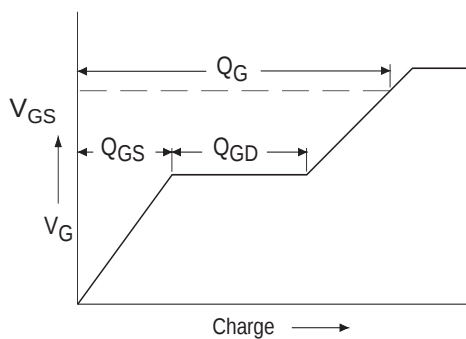


Fig 13a. Basic Gate Charge Waveform

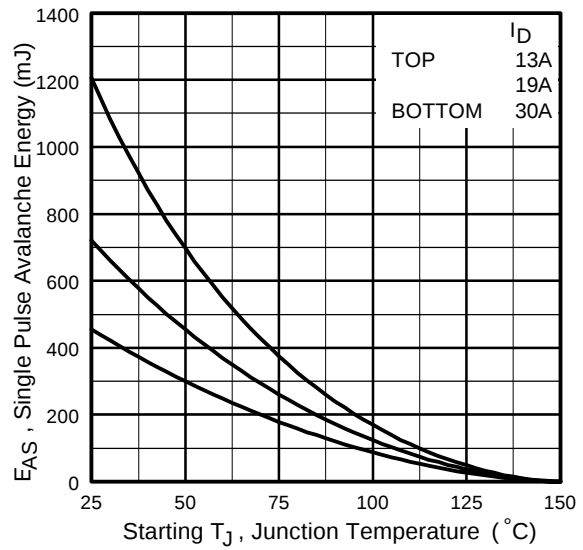


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

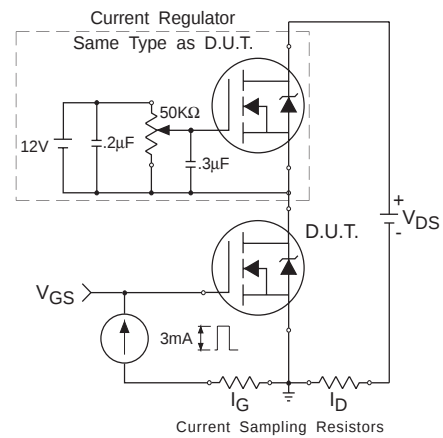
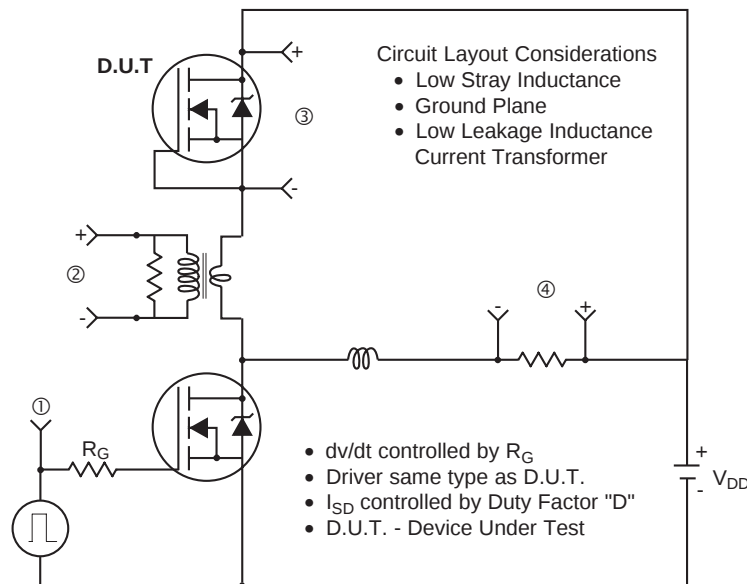


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

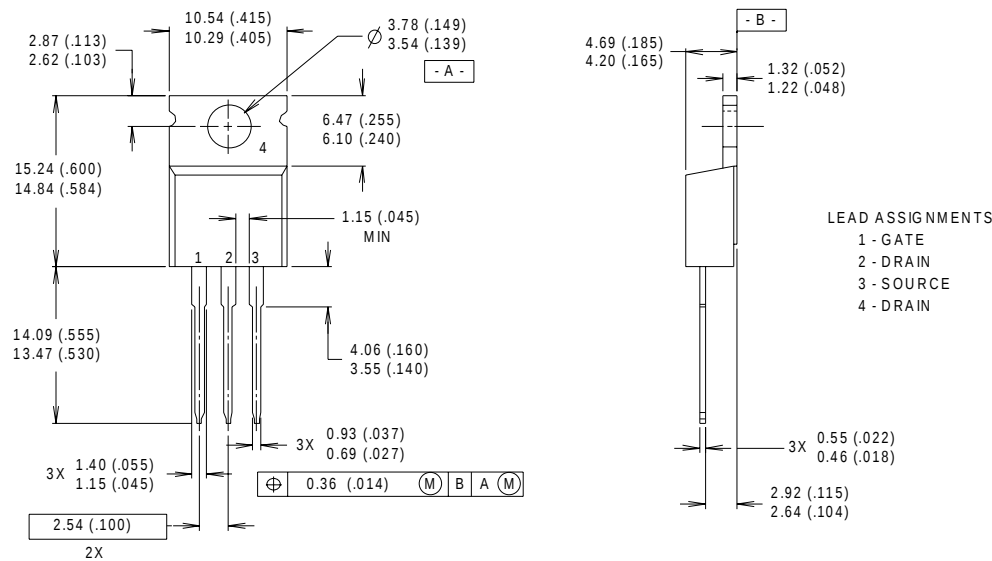
Fig 14. For N-Channel HEXFET® Power MOSFETs

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TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



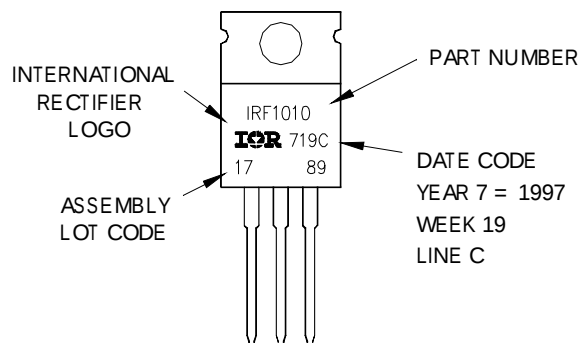
NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

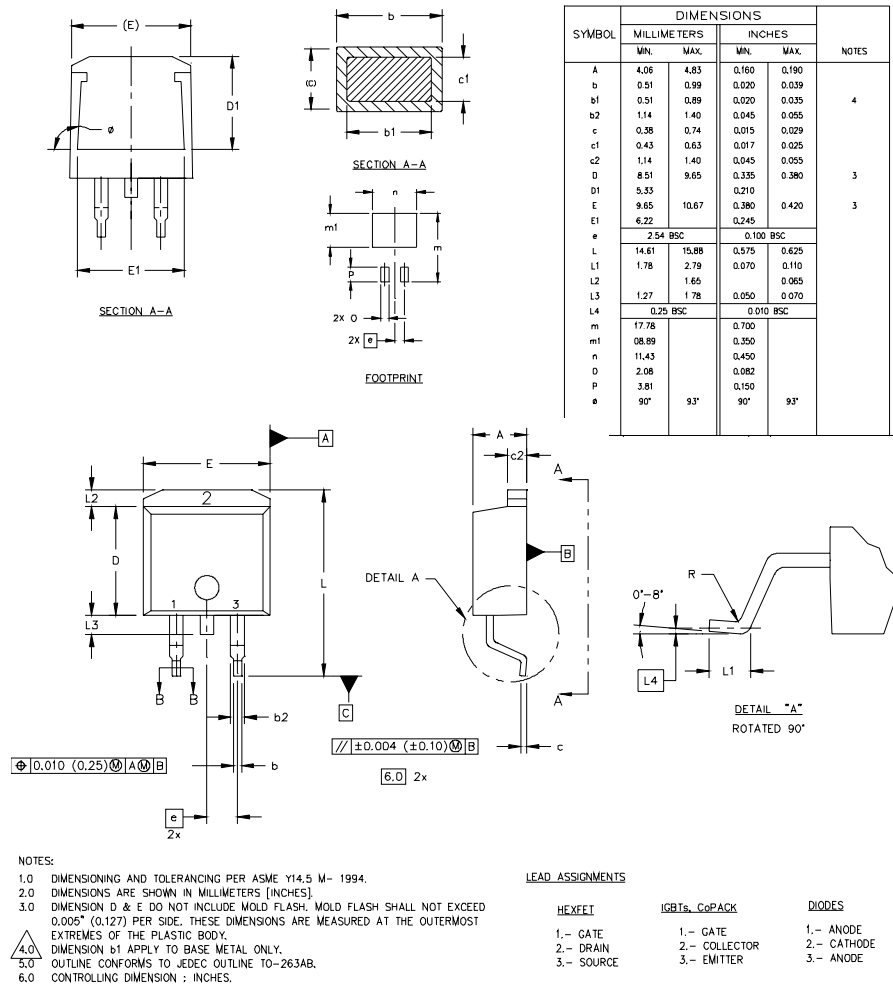
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

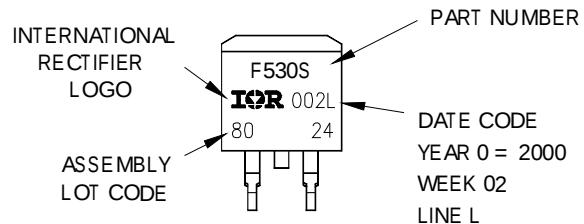


D²Pak Package Outline



D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW02, 2000
IN THE ASSEMBLY LINE "L"



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Technical drawing of a 3-pin connector. The drawing shows a top view and a side view. The top view is a rectangle with a central rectangular area labeled '4' and three vertical slots labeled '1', '2', and '3'. The side view shows the profile of the connector with dimensions for height and width. Dimensions are given in inches and millimeters in brackets. Lead assignments are shown in a table at the bottom.

Dimensions (inches [millimeters]):

- Top width: 10.54 [.415]
- Top width: 10.29 [.405]
- Top width: -A-
- Top width: 1.15 [.045] MIN.
- Top width: 10.54 [.415]
- Top width: 9.91 [.390]
- Top width: -C-
- Top width: 14.09 [.555]
- Top width: 13.47 [.530]
- Top width: 4.06 [.160]
- Top width: 3.55 [.140]
- Top width: 1.40 [.055]
- Top width: 1.15 [.045]
- Top width: 0.93 [.037]
- Top width: 0.69 [.027]
- Top width: 2.54 [.100]
- Top width: 2X
- Top width: 3X

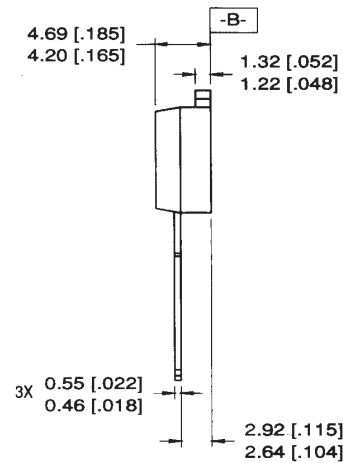
Lead Assignments:

⊕	0.36 [.014]	Ⓜ	B	A	Ⓜ
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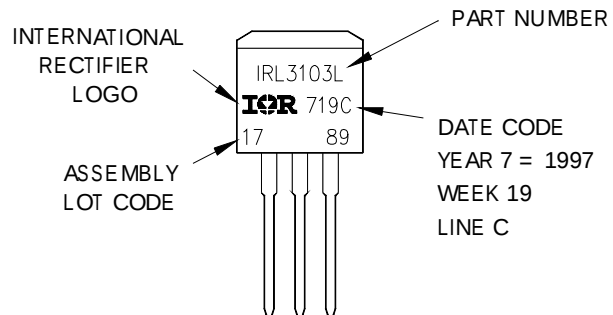
LEAD ASSIGNMENTS

1 = GATE 3 = SOURCE
2 = DRAIN 4 = DRAIN

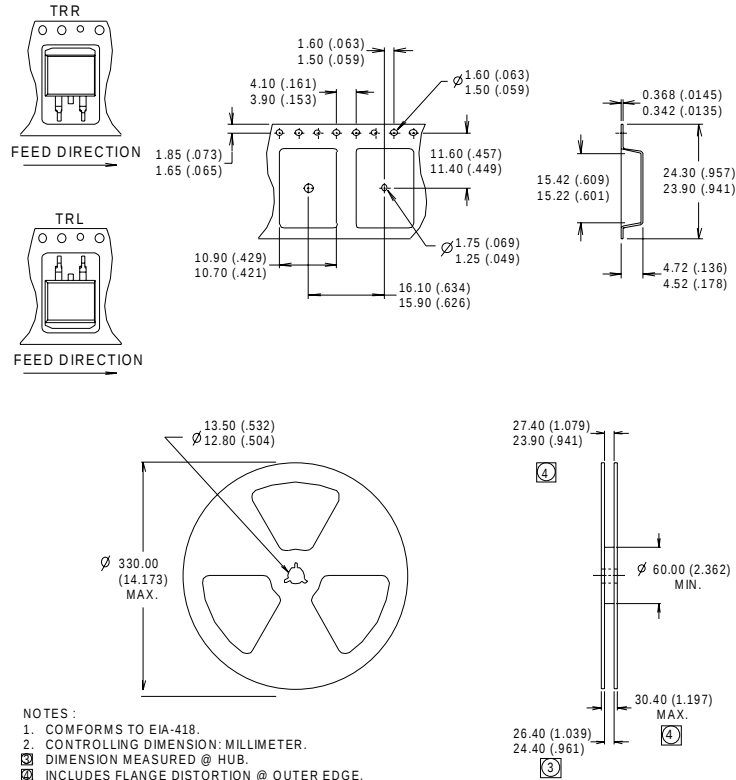
- NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.



EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON VW 19, 1997
IN THE ASSEMBLY LINE "C"



D²Pak Tape & Reel Information



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 1.0\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 30\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ This is only applied to TO-220AB package
- ⑤ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.