International
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REFERENCE DESIGN IRDCiP2001-A

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IRDCiP2001-A, 500kHz, 40A, 2-phase Synchronous Buck Converter using iP2001

Overview

In this document, table 1 and figure 1 are provided to enable engineers to easily evaluate the iP2001 in a 2-phase configuration that is capable of providing up to 40A in a lab environment without airflow. Figures 3, 4, 5 and 6 and the complete bill of materials in table 2 are provided as a reference design to enable engineers to very quickly and easily design a 2-phase converter. In order to optimize this design to your specific requirements refer to the data sheet for the controller listed in the bill of materials. A variety of other controllers may also be used, but the design will require layout and control circuit modifications.

iPOWIR™ TECHNOLOGY

Demoboard Quick Start Guide

Initial Settings:

- The output is set to 1.7V, but can be adjusted from 1.1 to 1.85V by setting S1 according to the VID codes provided in Table 1. Droop control is set to 100mV at 40A, but can be adjusted by following the instructions in the data sheet for the PWM controller.
- The switching frequency per phase is set to 500kHz with the frequency set resistor R4. This creates an effective output frequency of 1Mhz. The graph in figure 1 shows the relationship between R4 and the switching frequency per phase. This frequency may be adjusted by changing R4 according to this graph; however, extreme changes from the 500kHz set point may require redesigning the control loop and adjusting the values of input and output capacitors. Also, refer to the SOA graph in the iP2001 datasheet for maximum operating current at different frequencies.

Procedure for Connecting and Powering Up Demoboard:

1. Apply input voltage (5-12V) across V_{IN} (TP18) and PGND (TP15). Note that this input source must be applied first during the power-up sequence.
2. Apply +5V logic power across +5V (TP19) and PGND (TP20).
3. Apply load across VOUT pads (TP11 & TP12) and PGND pads (TP15 & TP16)
4. Set ENABLE high.
5. Monitor switch node signals (optional) via TP7 & TP8.
6. Adjust load accordingly.

iP2001 Recommended Operating Conditions

(refer to the iP2001 datasheet for maximum operating conditions)

Input voltage:	5 - 12V
Output voltage:	1.1 - 1.85V
Output current:	20A per phase, 40A total for 2-phase demo board.
Switching Freq:	500kHz per phase, 1MHz effective output frequency.

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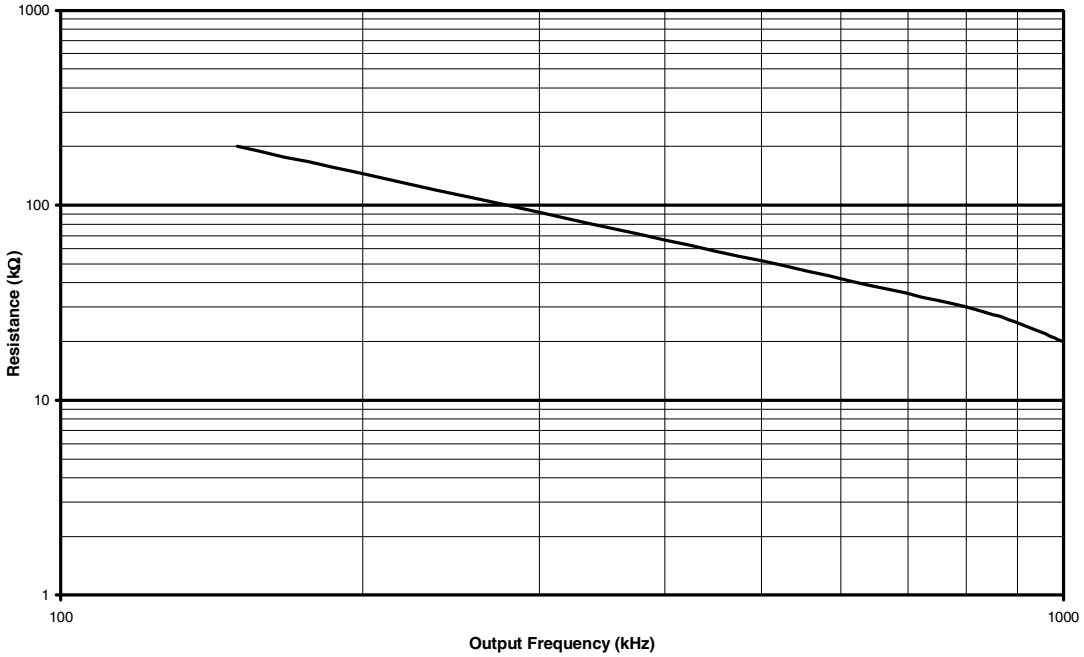

Figure 1 - R4 vs. Frequency (per Phase)

VID4	VID3	VID2	VID1	VID0	VDAC	VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	1	1	Off	0	1	1	1	1	1.475
1	1	1	1	0	1.100	0	1	1	1	0	1.500
1	1	1	0	1	1.250	0	1	1	0	1	1.525
1	1	1	0	0	1.150	0	1	1	0	0	1.550
1	1	0	1	1	1.175	0	1	0	1	1	1.575
1	1	0	1	0	1.200	0	1	0	1	0	1.600
1	1	0	0	1	1.225	0	1	0	0	1	1.625
1	1	0	0	0	1.250	0	1	0	0	0	1.650
1	0	1	1	1	1.275	0	0	1	1	1	1.675
1	0	1	1	0	1.300	0	0	1	1	0	1.700
1	0	1	0	1	1.325	0	0	1	0	1	1.725
1	0	1	0	0	1.350	0	0	1	0	0	1.750
1	0	0	1	1	1.375	0	0	0	1	1	1.775
1	0	0	1	0	1.400	0	0	0	1	0	1.800
1	0	0	0	1	1.425	0	0	0	0	1	1.825
1	0	0	0	0	1.450	0	0	0	0	0	1.850

Table 1 - PWM IC Voltage Identification Codes

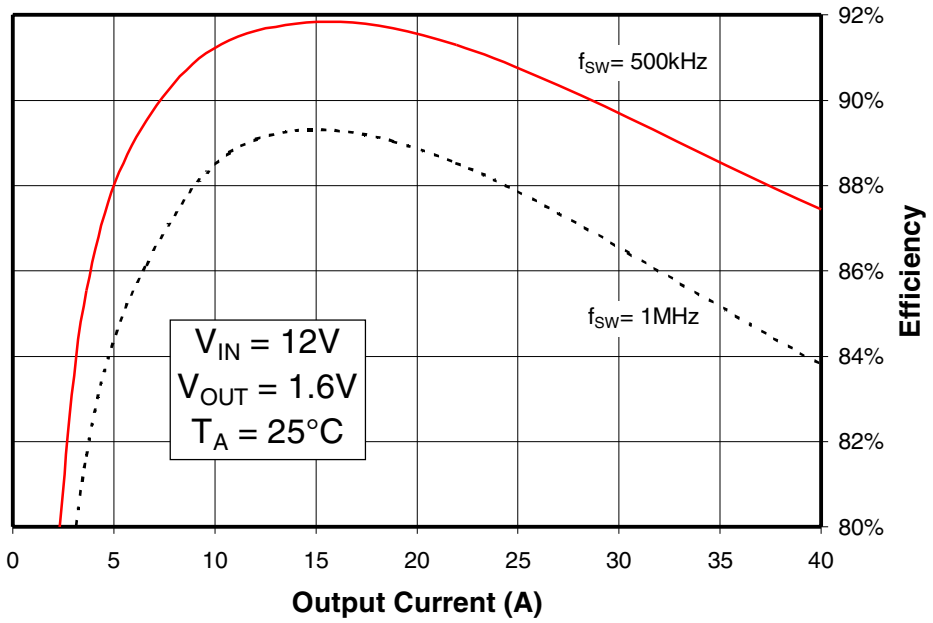

Figure 2 - Typical Efficiency vs. Current

Refer to the following application notes for detailed guidelines and suggestions when implementing iP0WIR Technology products:

AN-1028: Recommended Design, Integration and Rework Guidelines for International Rectifier's iPOWIR Technology BGA Packages
This paper discusses the assembly considerations that need to be taken when mounting iPOWIR BGA's on printed circuit boards. This includes soldering, pick and place, reflow, inspection, cleaning and reworking recommendations.

AN-1029: Optimizing a PCB Layout for an iPOWIR Technology Design
This paper describes how to optimize the PCB layout design for both thermal and electrical performance. This includes placement, routing, and via interconnect suggestions.

AN-1030: Applying iPOWIR Products in Your Thermal Environment
This paper explains how to use the Power Loss and SOA curves in the data sheet to validate if the operating conditions and thermal environment are within the Safe Operating Area of the iPOWIR product.

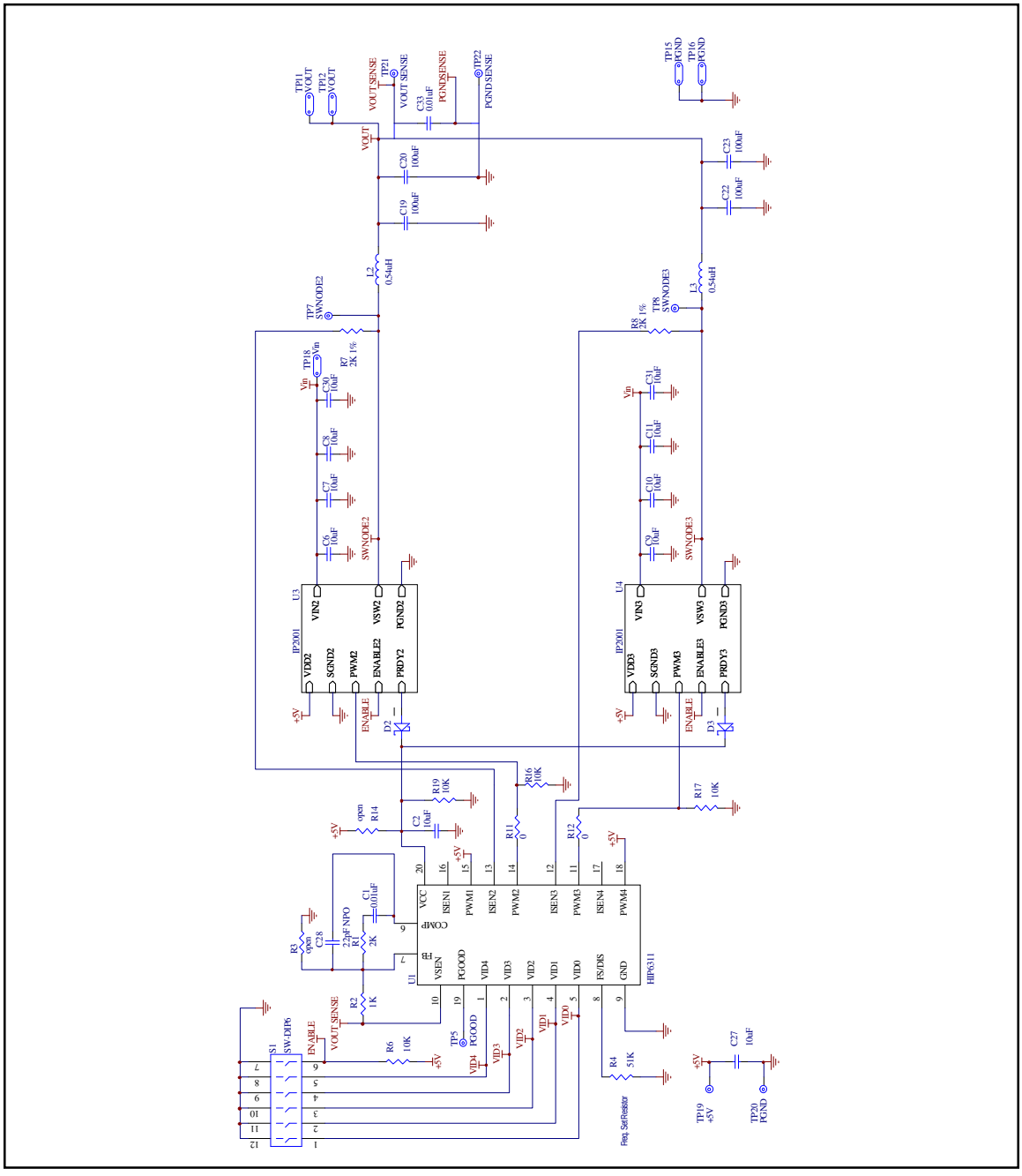

Fig. 3 - Reference Design Schematic

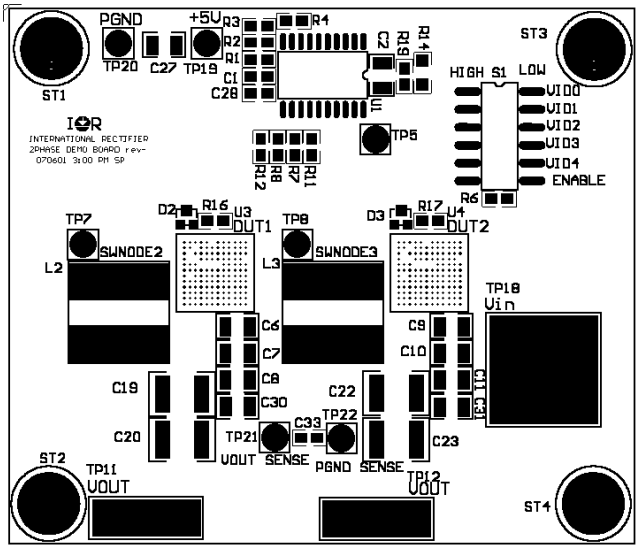

Fig. 4 - Component Placement Top Layer

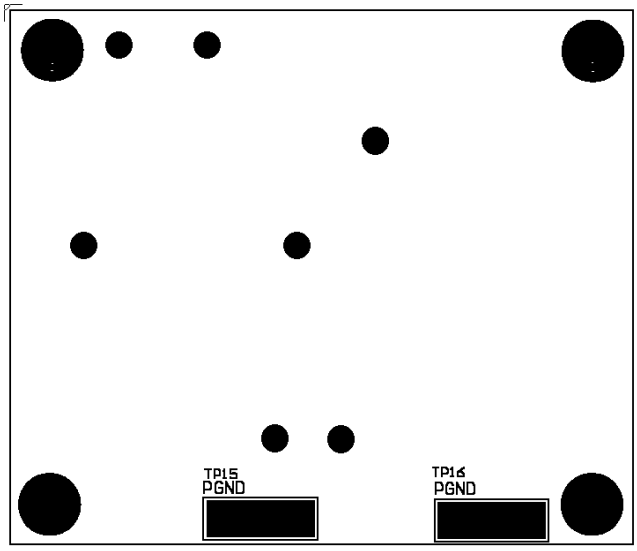

Fig. 5 - Component Placement Bottom Layer

Designator	Value 1	Value 2	Type	Tolerance	Package	Mfr. 1	Mfr. 1 Part No.	Mfr. 2	Mfr. 2 Part No.
C1 & C33	0.01uF	50V	X7R	10%	0805	TDK	C2012X7R1H103KT	SAMSUNG	CL21B103KBNC
C2, C6, C11, C27, C30, C31	10uF	16V	X5R	10%	1210	TDK	C3225X5R1C106KT	Murata	GRM42-2 X5R 106K16
C19, C20, C22, C23	100uF	6.3V	X5R	10%	2220	TDK	C5750X5R0J107KT	MuRata	GRM44-1-X5R 107K 6.3
C28	22pF	50V	NPO	5%	0805	TDK	C2012X7R1H220JT	ROHM	MCH215A220JK
D2 & D3	30V	100mA	Schottky	-	SOT23	Central	CMPSH-3	-	-
L2 & L3	0.54uH	27A	Ferrite	20%	SMT	Panasonic	ETQP6F0R6BFA	Bi Technologie	HM73-30R60
R1	2K	1/8W	Thick film	5%	0805	ROHM	MCR10EZHJ202	-	-
R2	1K	1/8W	Thick film	5%	0805	ROHM	MCR10EZHJ102	-	-
R3 & R14	-	-	-	-	-	-	-	-	-
R4	51K	1/8W	Thick film	5%	0805	ROHM	MCR10EZHJW513	-	-
R6, R16, R17, R19	10K	1/8W	Thick film	5%	0805	ROHM	MCR10EZHJ103	-	-
R7 & R8	2K	1/8W	Thick film	1%	0805	KOA	RK73H2A2001F	-	-
R11 & R12	0	1/8W	Thick film	<50mΩ	0805	ROHM	MCR10EZHJ000	-	-
S1	SPST	6 position	Dip switch	-	SMT	C&K Comp.	SD06H0SK	-	-
ST1 - ST4	Stand Off	-	-	-	4-40	Keystone	8412K	-	-
U1	4.6-6 V	0-1.850V	PWM IC	0 - 70°C	20 Ld SOIC	Intersil	HIP6311CB	-	-
U3 & U4	-	-	-	-	11x11mm	IR	iP2001	-	-

Table 2 - Reference Design Bill of Materials

Adjusting the Over-Current Limit

R7 and R9 are the resistors used to adjust the over-current trip point. The trip point is a function of the controller and corresponds to 165% of the output current indicated on the x-axis of Fig. 6. For example, selecting a resistance of 1.5K at each phase will set the trip point to 165% of 15A, or 24.75A. The trip point of each phase on the demoboard is currently set to 165% of 20A, or 33A.

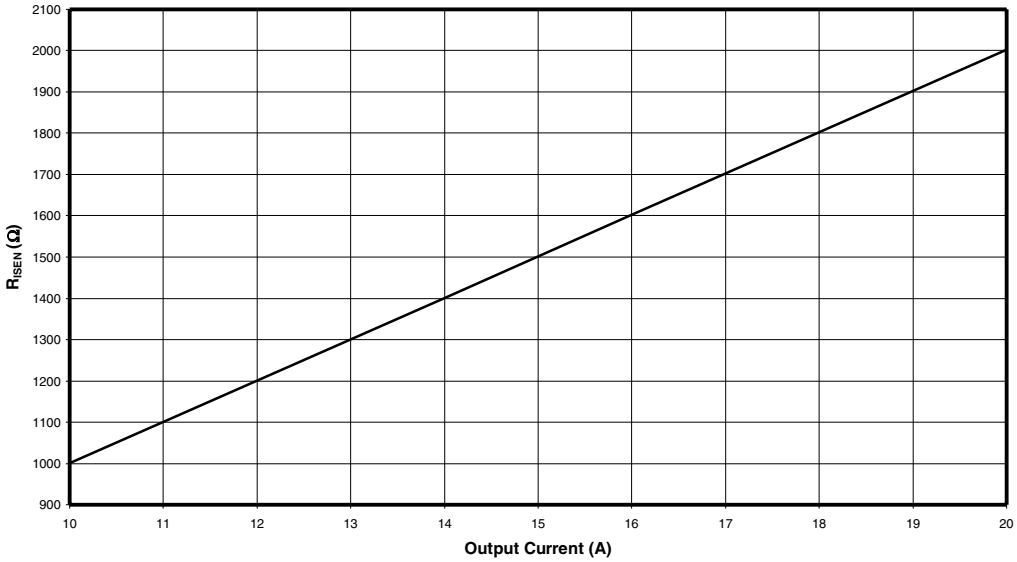

Fig. 6 - R_{ISEN} vs Current (per Phase)