

# IR2181/IR21814

## HIGH AND LOW SIDE DRIVER

### Features

- Floating channel designed for bootstrap operation  
Fully operational to +600V  
Tolerant to negative transient voltage  
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 5V Schmitt triggered input logic
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs (IR2181/IR21814)

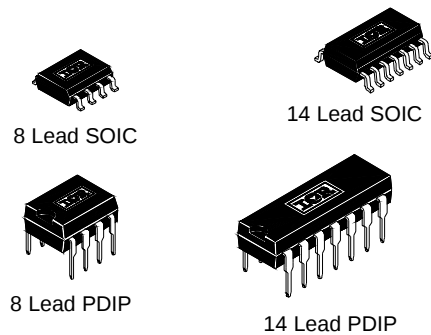
### Product Summary

|                            |               |
|----------------------------|---------------|
| $V_{\text{OFFSET}}$        | 600V max.     |
| $I_{\text{O}+/-}$          | 1.7 A / 1.7 A |
| $V_{\text{OUT}}$           | 10 - 20V      |
| $t_{\text{on/off}}$ (typ.) | 180 ns        |
| Delay matching             | 50 ns         |

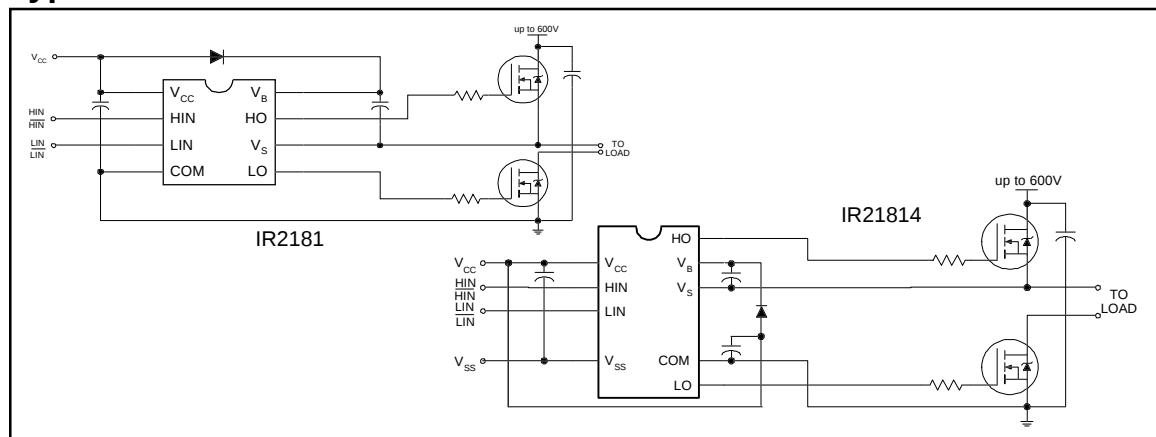
### Description

The IR2181/IR21814 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

### Packages



### Typical Connection



# IR2181/IR21814

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## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol              | Definition                                         | Min.                  | Max.                  | Units |      |
|---------------------|----------------------------------------------------|-----------------------|-----------------------|-------|------|
| V <sub>B</sub>      | High side floating absolute voltage                | -0.3                  | 625                   | V     |      |
| V <sub>S</sub>      | High side floating supply offset voltage           | V <sub>B</sub> - 25   | V <sub>B</sub> + 0.3  |       |      |
| V <sub>HO</sub>     | High side floating output voltage                  | V <sub>S</sub> - 0.3  | V <sub>B</sub> + 0.3  |       |      |
| V <sub>CC</sub>     | Low side and logic fixed supply voltage            | -0.3                  | 25                    |       |      |
| V <sub>LO</sub>     | Low side output voltage                            | -0.3                  | V <sub>CC</sub> + 0.3 |       |      |
| V <sub>IN</sub>     | Logic input voltage (HIN & LIN - IR2181/IR21814)   | V <sub>SS</sub> - 0.3 | V <sub>CC</sub> + 0.3 |       |      |
| V <sub>SS</sub>     | Logic ground (IR21814 only)                        | V <sub>CC</sub> - 25  | V <sub>CC</sub> + 0.3 |       |      |
| dV <sub>S</sub> /dt | Allowable offset supply voltage transient          | —                     | 50                    | V/ns  |      |
| P <sub>D</sub>      | Package power dissipation @ T <sub>A</sub> ≤ +25°C | (8 lead PDIP)         | —                     | 1.0   | W    |
|                     |                                                    | (8 lead SOIC)         | —                     | 0.625 |      |
|                     |                                                    | (14 lead PDIP)        | —                     | 1.6   |      |
|                     |                                                    | (14 lead SOIC)        | —                     | 1.0   |      |
| R <sub>thJA</sub>   | Thermal resistance, junction to ambient            | (8 lead PDIP)         | —                     | 125   | °C/W |
|                     |                                                    | (8 lead SOIC)         | —                     | 200   |      |
|                     |                                                    | (14 lead PDIP)        | —                     | 75    |      |
|                     |                                                    | (14 lead SOIC)        | —                     | 120   |      |
| T <sub>J</sub>      | Junction temperature                               | —                     | 150                   | °C    |      |
| T <sub>S</sub>      | Storage temperature                                | -50                   | 150                   |       |      |
| T <sub>L</sub>      | Lead temperature (soldering, 10 seconds)           | —                     | 300                   |       |      |

## Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The  $V_S$  and  $V_{SS}$  offset rating are tested with all supplies biased at 15V differential.

| Symbol   | Definition                                       | Min.       | Max.       | Units            |
|----------|--------------------------------------------------|------------|------------|------------------|
| $V_B$    | High side floating supply absolute voltage       | $V_S + 10$ | $V_S + 20$ | V                |
| $V_S$    | High side floating supply offset voltage         | Note 1     | 600        |                  |
| $V_{HO}$ | High side floating output voltage                | $V_S$      | $V_B$      |                  |
| $V_{CC}$ | Low side and logic fixed supply voltage          | 10         | 20         |                  |
| $V_{LO}$ | Low side output voltage                          | 0          | $V_{CC}$   |                  |
| $V_{IN}$ | Logic input voltage (HIN & LIN - IR2181/IR21814) | $V_{SS}$   | $V_{CC}$   |                  |
| $V_{SS}$ | Logic ground (IR21814/IR21824 only)              | -5         | 5          |                  |
| $T_A$    | Ambient temperature                              | -40        | 125        | $^\circ\text{C}$ |

Note 1: Logic operational for  $V_S$  of -5V to +600V. Logic state held for  $V_S$  of -5V to - $V_{BS}$ .

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $V_{SS}$  = COM,  $C_L$  = 1000 pF,  $T_A$  = 25°C.

| Symbol    | Definition                          | Min. | Typ. | Max. | Units | Test Conditions    |
|-----------|-------------------------------------|------|------|------|-------|--------------------|
| $t_{on}$  | Turn-on propagation delay           | —    | 180  | 270  | nsec  | $V_S = 0V$         |
| $t_{off}$ | Turn-off propagation delay          | —    | 170  | 250  |       | $V_S = 0V$ or 600V |
| MT        | Delay matching, HS & LS turn-on/off | —    | 0    | 50   |       |                    |
| $t_r$     | Turn-on rise time                   | —    | 40   | 60   |       | $V_S = 0V$         |
| $t_f$     | Turn-off fall time                  | —    | 20   | 30   |       | $V_S = 0V$         |

## Static Electrical Characteristics

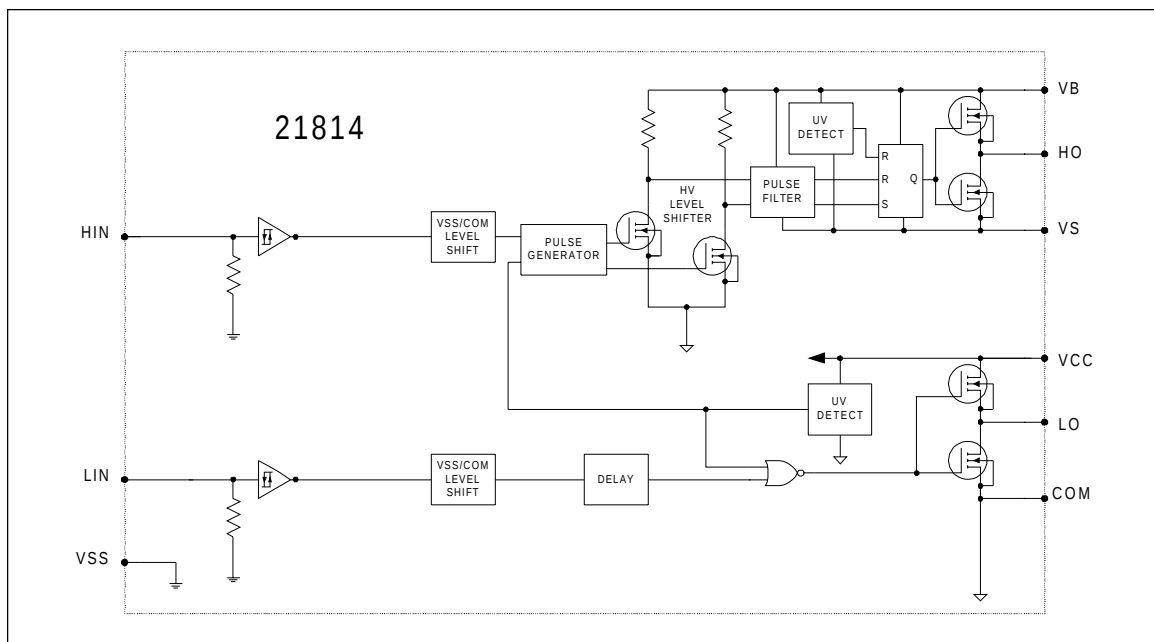
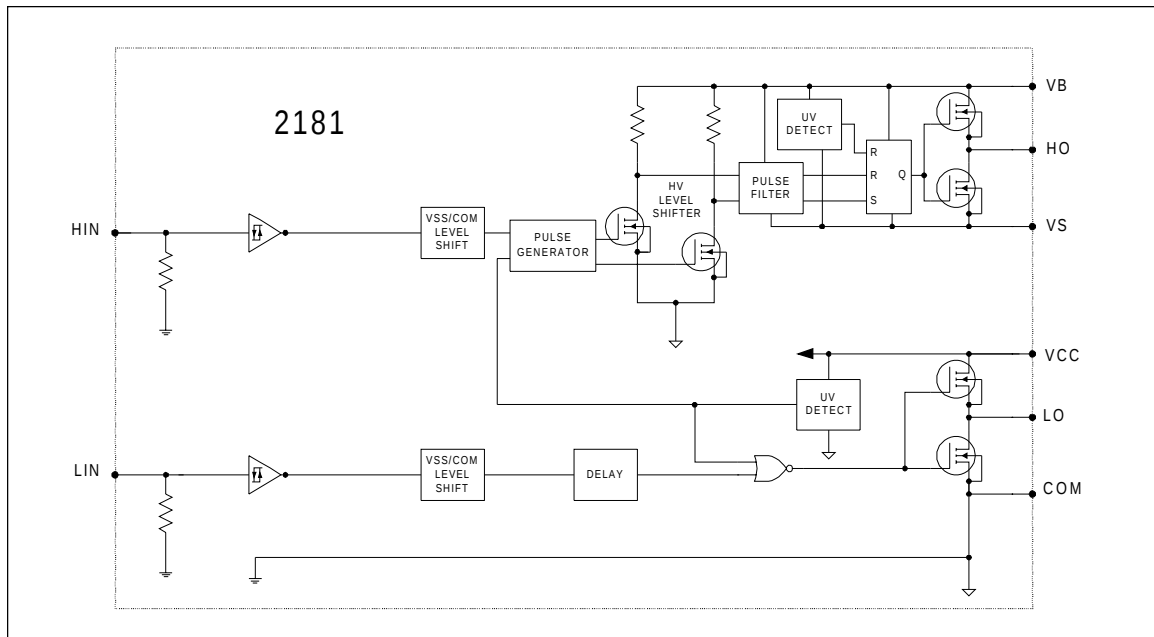
$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $V_{SS}$  = COM and  $T_A$  = 25°C unless otherwise specified. The  $V_{IL}$ ,  $V_{IH}$  and  $I_{IN}$  parameters are referenced to  $V_{SS}/COM$  and are applicable to the respective input leads: HIN and LIN (IR2181/IR21814) and HIN and LIN (IR2182/IR21824). The  $V_O$ ,  $I_O$  and  $R_{on}$  parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

| Symbol                     | Definition                                                         | Min. | Typ. | Max. | Units   | Test Conditions                     |
|----------------------------|--------------------------------------------------------------------|------|------|------|---------|-------------------------------------|
| $V_{IH}$                   | Logic "1" input voltage (IR2181/IR21814 )                          | 2.7  | —    | —    | V       | $V_{CC} = 10V$ to 20V               |
| $V_{IL}$                   | Logic "0" input voltage (IR2181/IR21814)                           | —    | —    | 0.8  |         | $V_{CC} = 10V$ to 20V               |
| $V_{OH}$                   | High level output voltage, $V_{BIAS} - V_O$                        | —    | —    | 1.2  |         | $I_O = 0A$                          |
| $V_{OL}$                   | Low level output voltage, $V_O$                                    | —    | —    | 0.1  |         | $I_O = 0A$                          |
| $I_{LK}$                   | Offset supply leakage current                                      | —    | —    | 50   | $\mu A$ | $V_B = V_S = 600V$                  |
| $I_{QBS}$                  | Quiescent $V_{BS}$ supply current                                  | 20   | 60   | 150  |         | $V_{IN} = 0V$ or 5V                 |
| $I_{QCC}$                  | Quiescent $V_{CC}$ supply current                                  | 50   | 120  | 240  |         | $V_{IN} = 0V$ or 5V                 |
| $I_{IN+}$                  | Logic "1" input bias current                                       | —    | 20   | 40   |         | $V_{IN} = 5V$ (IR2181(4))           |
| $I_{IN-}$                  | Logic "0" input bias current                                       | —    | —    | 1.0  | V       | $V_{IN} = 0V$ (IR2181(4))           |
| $V_{CCUV+}$<br>$V_{BSUV+}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold | 8.0  | 8.9  | 9.8  |         |                                     |
| $V_{CCUV-}$<br>$V_{BSUV-}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold | 7.4  | 8.2  | 9.0  |         |                                     |
| $V_{CCUVH}$<br>$V_{BSUVH}$ | Hysteresis                                                         | 0.3  | 0.7  | —    |         |                                     |
| $I_{O+}$                   | Output high short circuit pulsed current                           | 1.7  | 2    | —    | A       | $V_O = 0V$ ,<br>$PW \leq 10 \mu s$  |
| $I_{O-}$                   | Output low short circuit pulsed current                            | 1.7  | 2    | —    |         | $V_O = 15V$ ,<br>$PW \leq 10 \mu s$ |

# IR2181/IR21814

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## Functional Block Diagram



**Lead Definitions**

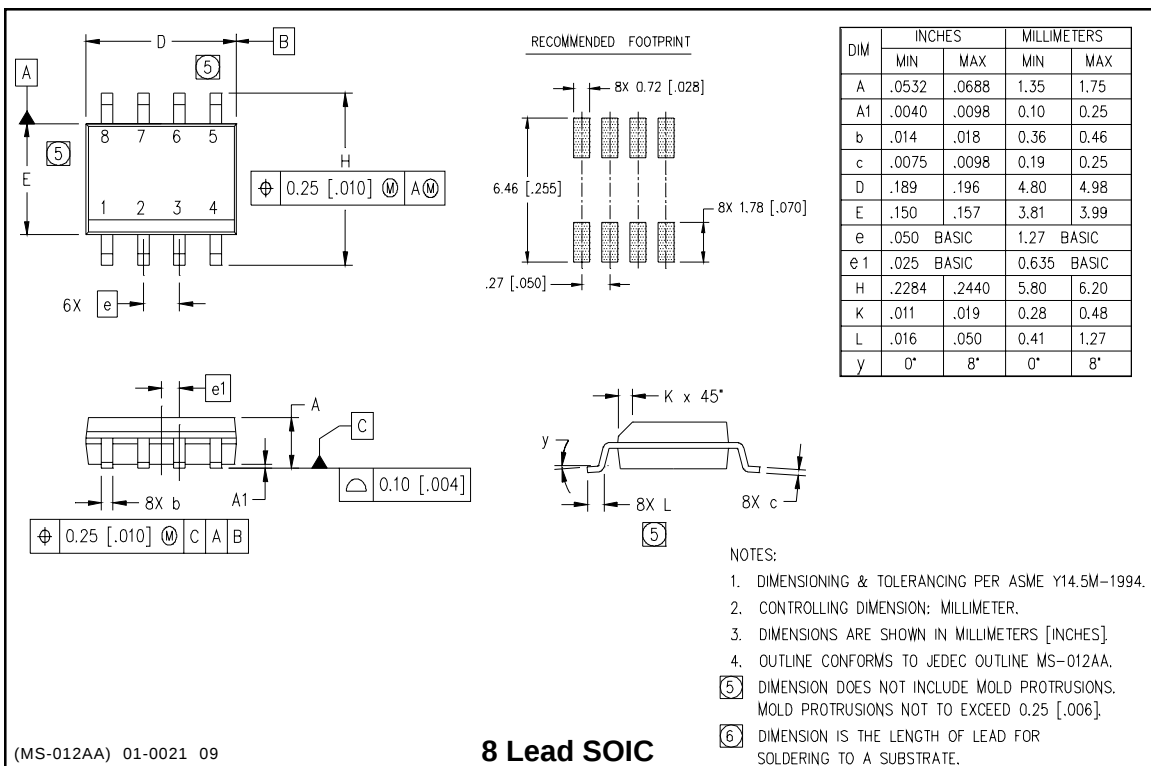
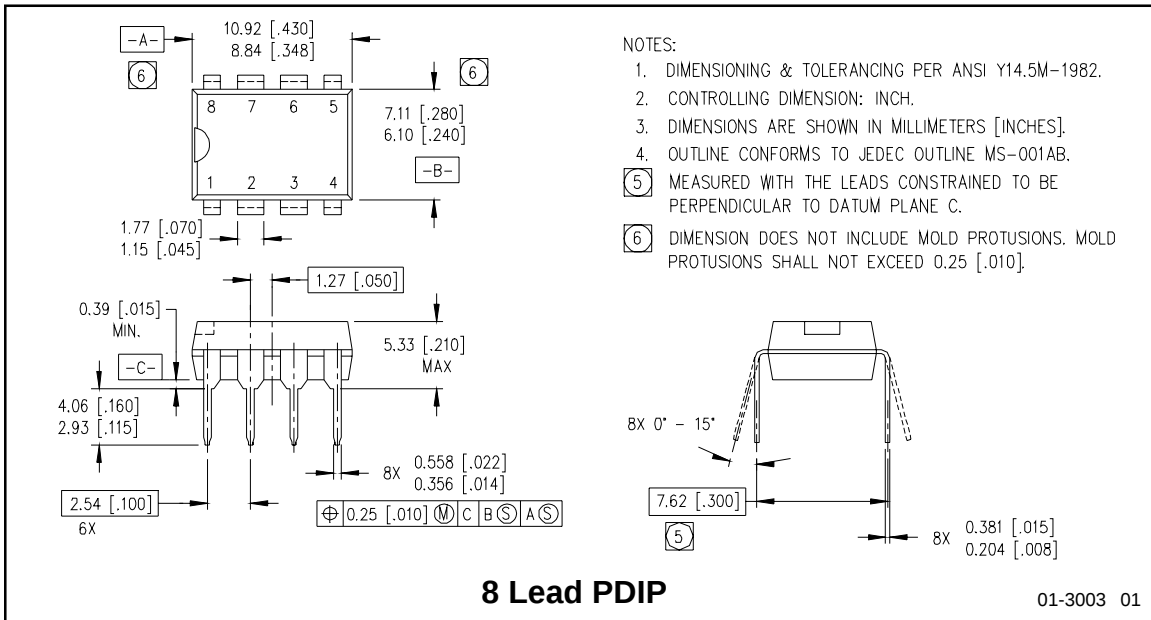
| Symbol          | Description                                                                  |
|-----------------|------------------------------------------------------------------------------|
| HIN             | Logic input for high side gate driver output (HO), in phase (IR2181/IR21814) |
| LIN             | Logic input for low side gate driver output (LO), in phase (IR2181/IR21814)  |
| VSS             | Logic Ground (IR21814 only)                                                  |
| V <sub>B</sub>  | High side floating supply                                                    |
| HO              | High side gate drive output                                                  |
| V <sub>S</sub>  | High side floating supply return                                             |
| V <sub>CC</sub> | Low side and logic fixed supply                                              |
| LO              | Low side gate drive output                                                   |
| COM             | Low side return                                                              |

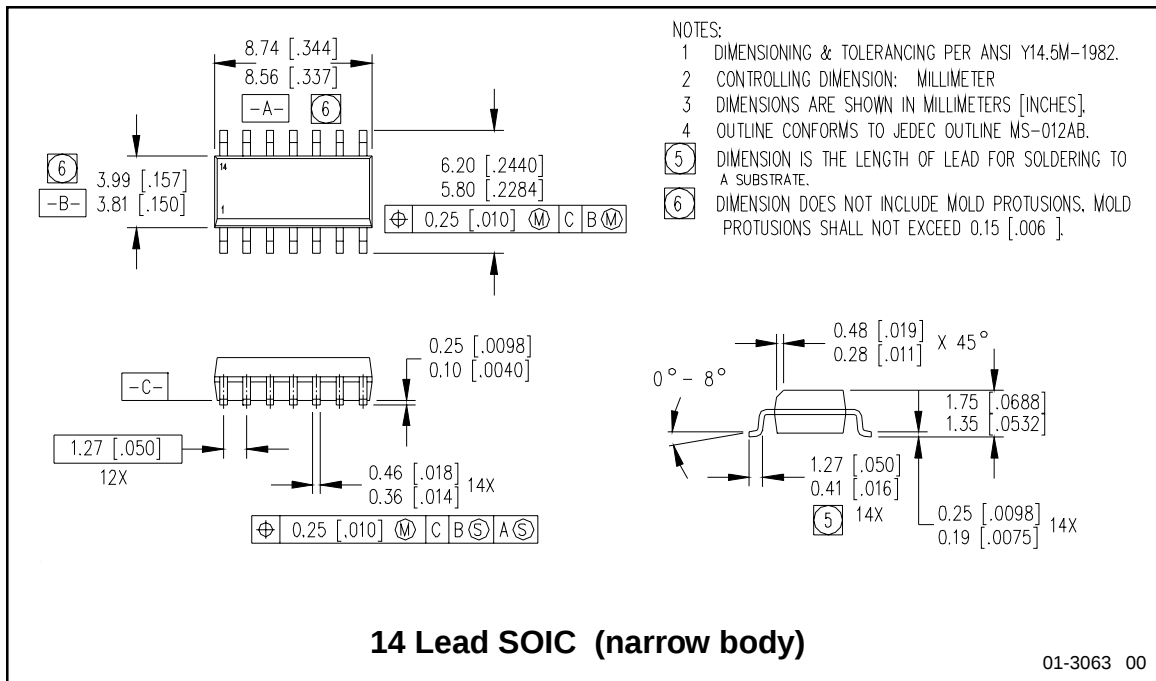
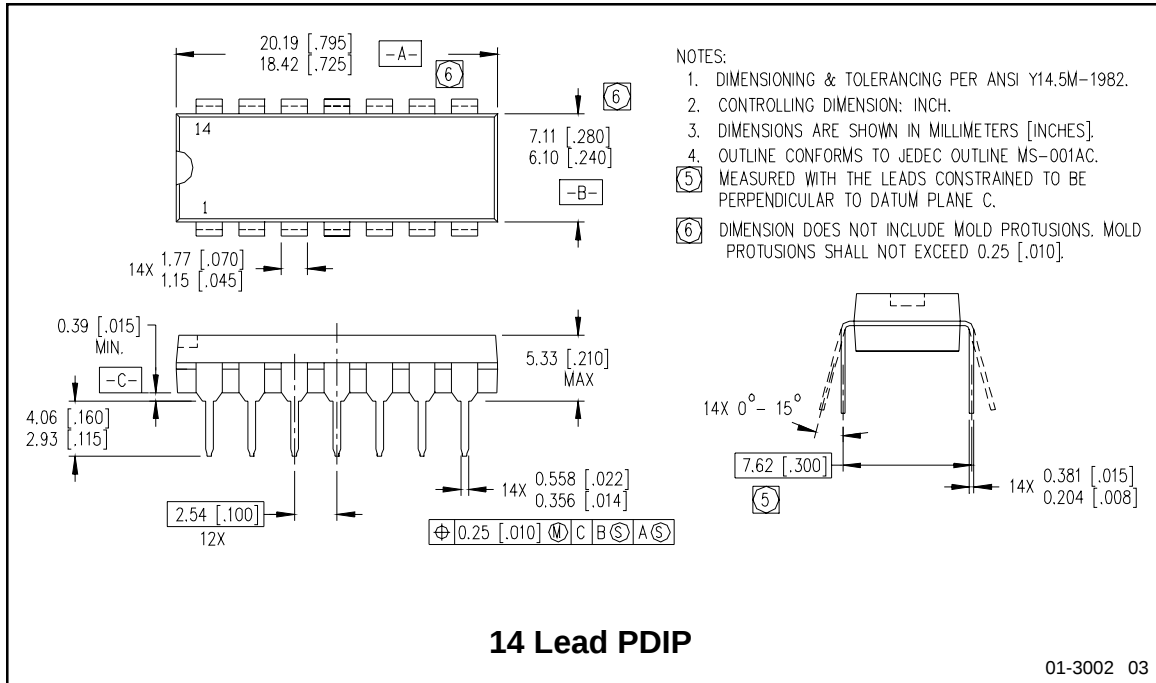
**Lead Assignments**

|                     |                     |
|---------------------|---------------------|
| <p>8 Lead PDIP</p>  | <p>8 Lead SOIC</p>  |
| <b>IR2181</b>       | <b>IR2181S</b>      |
| <p>14 Lead PDIP</p> | <p>14 Lead SOIC</p> |
| <b>IR21814</b>      | <b>IR21814S</b>     |

# IR2181/IR21814

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# IR2181/IR21814

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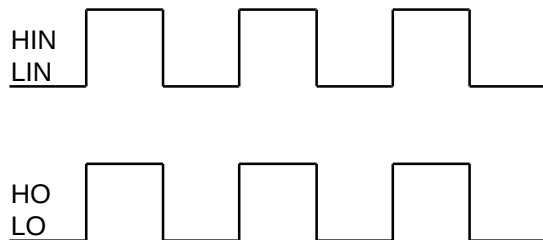


Figure 1. Input/Output Timing Diagram

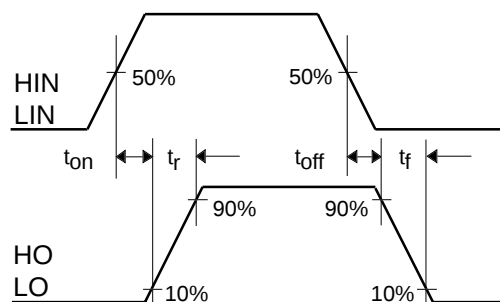


Figure 2. Switching Time Waveform Definitions

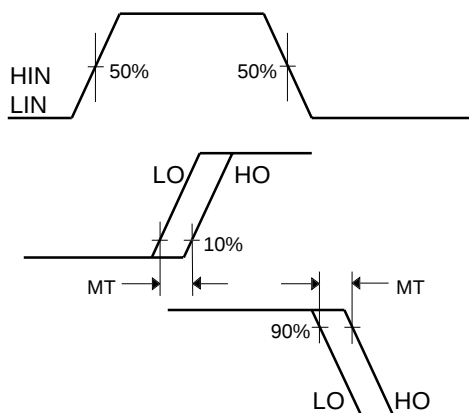


Figure 3. Delay Matching Waveform Definitions

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*Data and specifications subject to change without notice. 4/11/2000*

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