International
IOR Rectifier

IR2110E6

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- Separate logic supply range from 5 to 20V
  Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Product Summary

V_{OFFSET}	600V max.
I_O+/-	2A / 2A
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	120 & 94 ns
Delay Matching	10 ns

Description

The IR2110E6 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Parameter	Min.	Max.	Units
V_B	High Side Floating Supply Absolute Voltage	-0.5	V_S + 20	V
V_S	High Side Floating Supply Offset Voltage	—	600	
V_{HO}	High Side Output Voltage	V_S -0.5	V_B + 0.5	
V_{CC}	Low Side Fixed Supply Voltage	-0.5	20	
V_{LO}	Low Side Output Voltage	-0.5	V_{CC} + 0.5	
V_{DD}	Logic Supply Voltage	-0.5	V_{SS} + 20	
V_{SS}	Logic Supply Offset Voltage	V_{CC} - 20	V_{CC} + 0.5	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS} - 0.5	V_{DD} + 0.5	
dV_S/dt	Allowable Offset Supply Voltage Transient (Fig. 16)	—	50	V/ns
P_D	Package Power Dissipation @ T_A ≤ = 25°C (Fig. 19)	—	1.6	W
R_{thJA}	Thermal Resistance, Junction to Ambient	—	125	°C/W
T_j	Junction Temperature	-55	125	°C
T_S	Storage Temperature	-55	150	
T_L	Package Mounting Surface Temperature	300 (for 5 seconds)		
	Weight	0.45 (typical)		g

9/11/98

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figures 36 and 37.

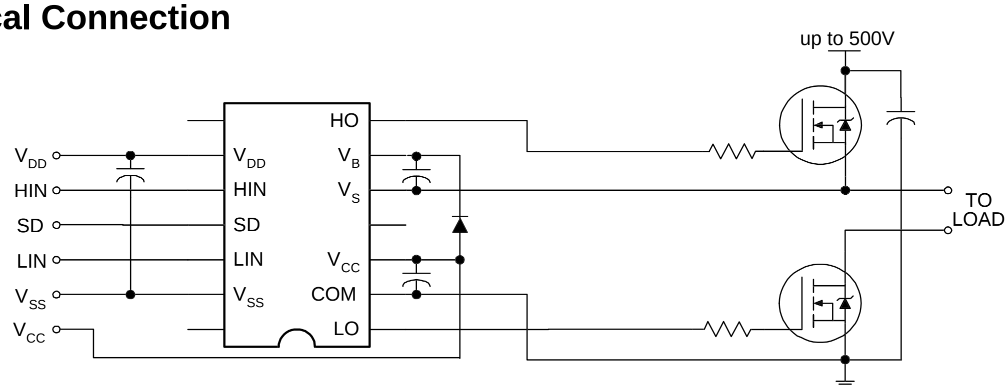
Symbol	Parameter	Min.	Max.	Units
V_B	High Side Floating Supply Absolute Voltage	V_S + 10	V_S + 20	V
V_S	High Side Floating Supply Offset Voltage	-4	600	
V_{HO}	High Side Output Voltage	V_S	V_B	
V_{CC}	Low Side Fixed Supply Voltage	10	20	
V_{LO}	Low Side Output Voltage	0	V_{CC}	
V_{DD}	Logic Supply Voltage	V_{SS} + 5	V_{SS} + 20	
V_{SS}	Logic Supply Offset Voltage	-5	5	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified.
The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

		Tj = 25°C			Tj = -55 to 125°C				
Symbol	Parameter	Min	Typ.	Max.	Min.	Max	Units	Test Conditions	Ref.
t_{on}	Turn-On Propagation Delay	—	120	150	—	260	ns	V_S = 0V	Fig. 12
t_{off}	Turn-Off Propagation Delay	—	94	125	—	220		V_S = 600V	
t_{sd}	Shutdown Propagation Delay	—	110	140	—	235		V_S = 600V	
t_r	Turn-On Rise Time	—	25	35	—	50		C_L = 1000pf	Fig. 13
t_f	Turn-Off Fall Time	—	17	25	—	40		C_L = 1000pf	
Mt_{on}	Delay Matching, HS & LS Turn-On	—	—	10	—	—		(Ht_{on}-Lt_{on})	Fig. 14
Mt_{off}	Delay Matching, HS & LS Turn-Off	—	—	10	—	—		(Ht_{off}-Lt_{off})	
DHt_{on}	Deadtime, LS Turn-Off to HS Turn-On	16	26	36	—	—		(Ht_{on}-Lt_{off})	Fig. 15
DLt_{on}	Deadtime, LS Turn-Off to LS Turn-On	16	26	36	—	—		(Lt_{on}-Ht_{off})	

Typical Connection

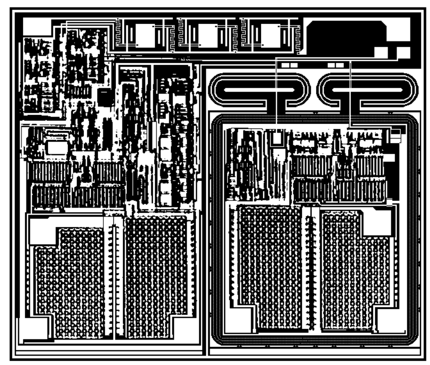


Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

		Tj = 25°C			Tj = -55 to 125°C				
Symbol	Parameter	Min	Typ.	Max.	Min.	Max	Units	Test Conditions	Ref.
V_{IH}	Logic "1" Input Voltage	3.1	—	—	3.3	—	V	V_{DD} = 5V	Fig. 4
		6.4	—	—	6.8	—		V_{DD} = 10V	
		9.5	—	—	10	—		V_{DD} = 15V	
		12.6	—	—	13.3	—		V_{DD} = 20V	
V_{IL}	Logic "0" Input Voltage	—	—	1.8	—	1.7		V_{DD} = 5V	
		—	—	3.8	—	3.6		V_{DD} = 10V	
		—	—	6	—	5.7	W	V_{DD} = 15V	
		—	—	8.3	—	7.9	V	V_{DD} = 20	
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	—	0.7	1.2	—	1.5	V	V_{IN} = V_{IH}, I_O = 0A	Fig. 10
V_{OL}	Low Level Output Voltage, VO	—	—	0.1	—	0.1		V_{IN} = V_{IL}, I_O = 0A	
I_{LK}	Offset Supply Leakage Current	—	—	50	—	250	µA	V_B = V_S = 600V	Fig. 5
I_{QBS}	Quiescent V_{BS} Supply Current	—	125	230	—	500		V_{IN} = V_{IH} or V_{IL}	Fig. 6
I_{QCC}	Quiescent V_{CC} Supply Current	—	180	340	—	600		V_{IN} = V_{IH} or V_{IL}	Fig. 7
I_{QDD}	Quiescent V_{DD} Supply Current	—	5	30	—	60		V_{IN} = V_{IH} or V_{IL}	
I_{IN+}	Logic "1" Input Bias Current	—	15	40	—	70		V_{IN} = 15V	Fig. 8
I_{IN-}	Logic "0" Input Bias Current	—	—	1	—	10		V_{IN} = 0V	
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	7.5	8.7	9.7	—	—	V		Fig. 9
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	7.0	8.3	9.4	—	—			
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	7.4	8.6	9.6	—	—			
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	7.0	8.2	9.4	—	—			
I_{O+}	Output High Short Circuit Pulsed Current	2	—	—	—	—	A	V_{OUT} = 0V, V_{IN} = 15V PW < = 10 µs	
I_{O-}	Output Low Short Circuit Pulsed Current	2	—	—	—	—		V_{OUT} = 15V, V_{IN} = 0V PW < = 10 µs	

Device Information

Process & Design Rule			HVDCMOS 4.0 µm
Transistor Count			220
Die Size			100 X 117 X 26 (mil)
Die Outline			
Thickness of Gate Oxide			800Å
Connections		Material	Poly Silicon
	First Layer	Width	4 µm
		Spacing	6 µm
		Thickness	5000Å
		Material	Al - Si (Si: 1.0% ±0.1%)
	Second Layer	Width	6 µm
		Spacing	9 µm
		Thickness	20,000Å
Contact Hole Dimension			8 µm X 8 µm
Insulation Layer		Material	PSG (SiO_2)
		Thickness	1.5 µm
Passivation (1)		Material	PSG (SiO_2)
		Thickness	1.5 µm
Passivation (2)		Material	Proprietary*
		Thickness	Proprietary*
Method of Saw			Full Cut
Method of Die Bond			Ablebond 84 - 1
Wire Bond		Method	Thermo Sonic
		Material	Au (1.0 mil / 1.3 mil)
Leadframe		Material	Cu
		Die Area	Ag
		Lead Plating	Pb : Sn (37 : 63)
Package		Types	14 & 16 Lead PDIP / 16 Lead SOIC
		Materials	EME6300 / MP150 / MP190
Remarks:	* Patent Pending		

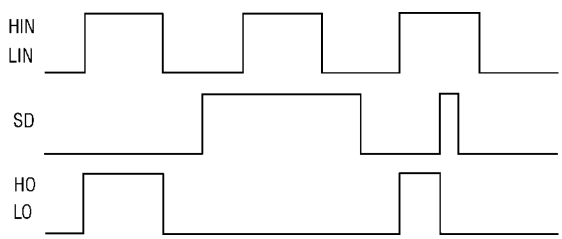


Figure 1. Input/Output Timing Diagram

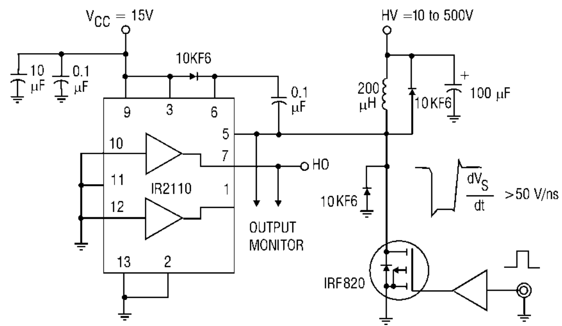


Figure 2. Floating Supply Voltage Transient Test Circuit

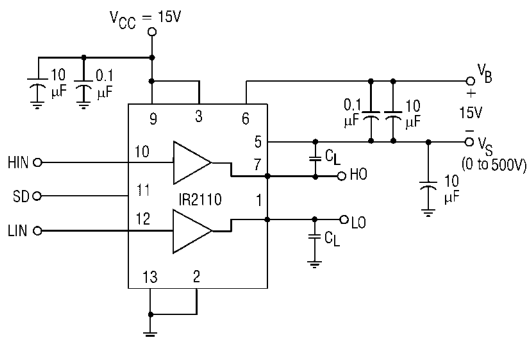


Figure 3. Switching Time Test Circuit

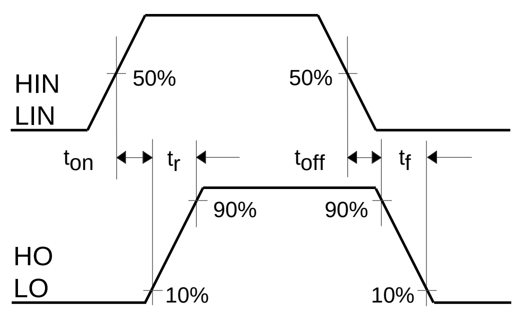


Figure 4. Switching Time Waveform Definition

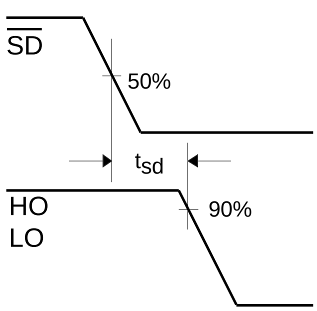


Figure 3. Shutdown Waveform Definitions

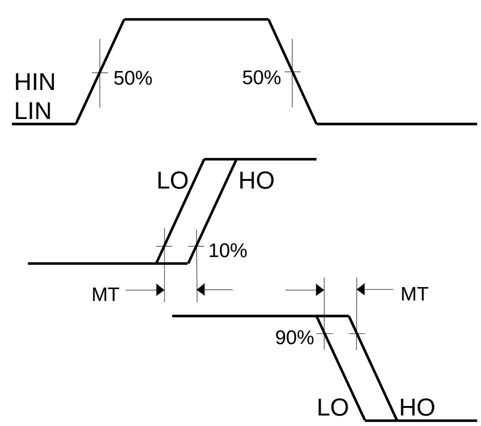


Figure 6. Delay Matching Waveform Definitions

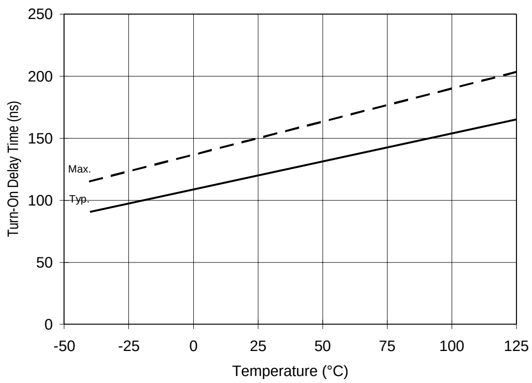


Figure 7A. Turn-On Time vs. Temperature

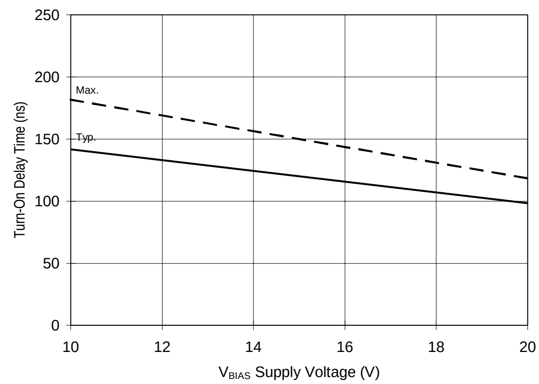


Figure 7B. Turn-On Time vs. Voltage

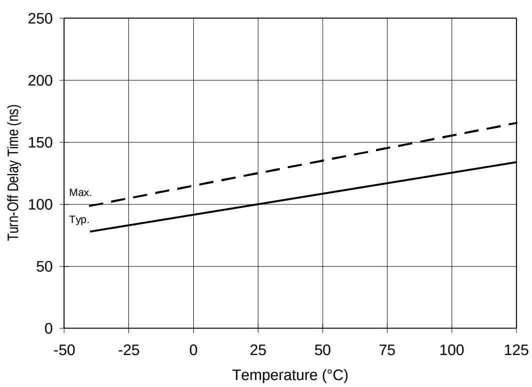


Figure 8A. Turn-Off Time vs. Temperature

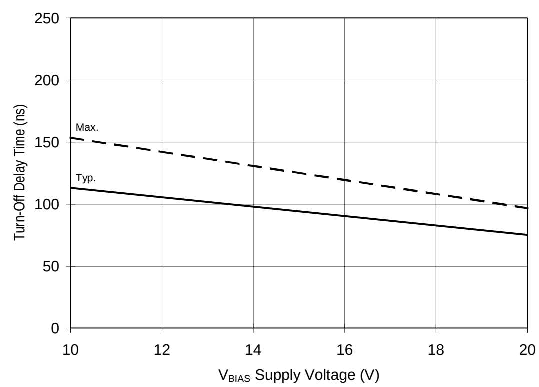


Figure 8B. Turn-Off Time vs. Voltage

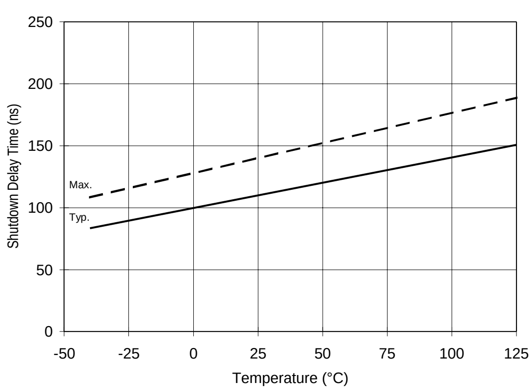


Figure 9A. Shutdown Time vs. Temperature

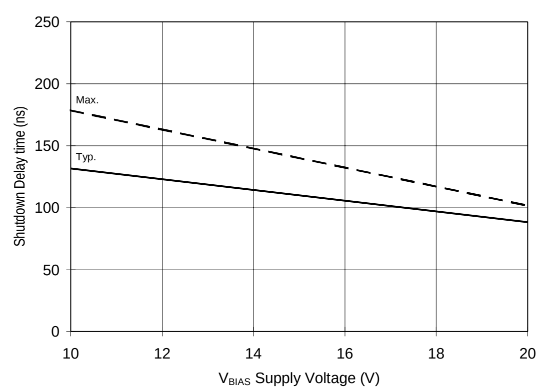


Figure 9B. Shutdown Time vs. Voltage

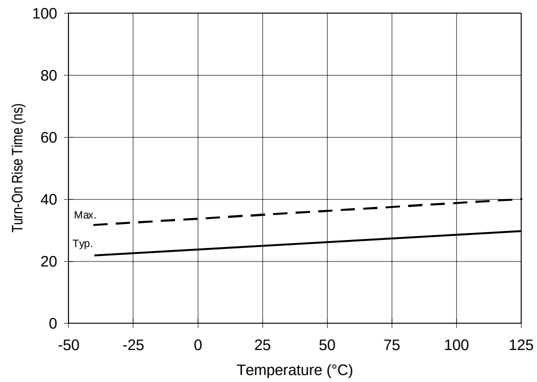


Figure 10A. Turn-On Rise Time vs. Temperature

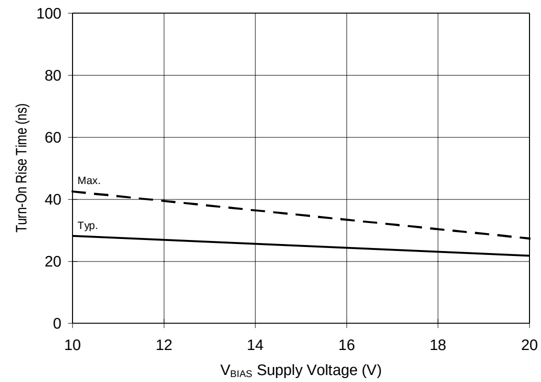


Figure 10B. Turn-On Rise Time vs. Voltage

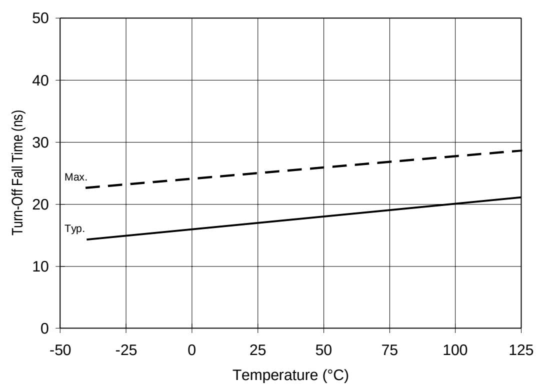


Figure 11A. Turn-Off Fall Time vs. Temperature

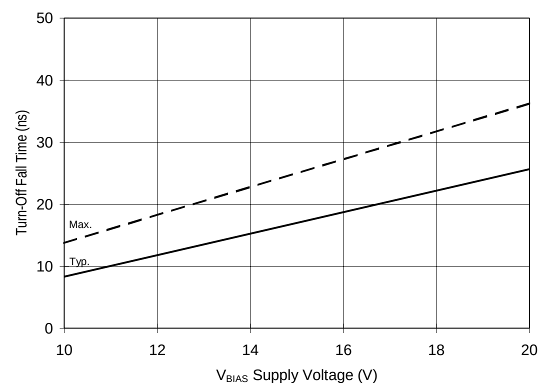


Figure 11B. Turn-Off Fall Time vs. Voltage

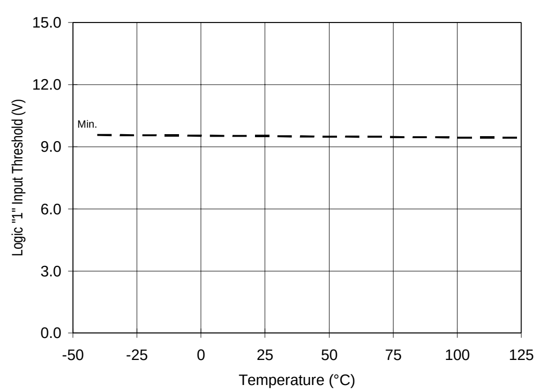


Figure 12A. Logic “1” Input Threshold vs. Temperature

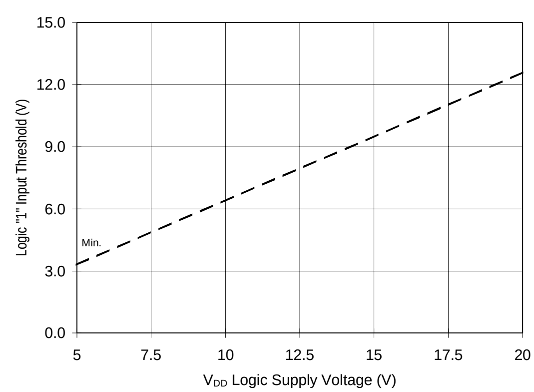


Figure 12B. Logic “1” Input Threshold vs. Voltage

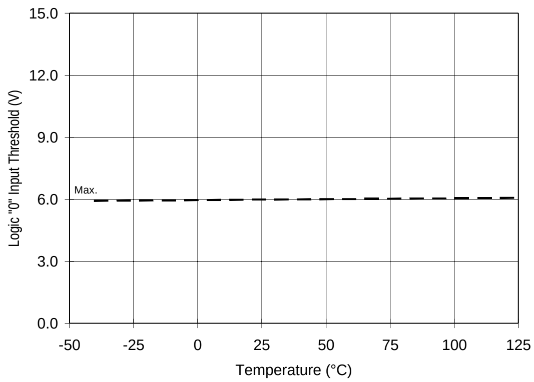


Figure 13A. Logic “0” Input Threshold vs. Temperature

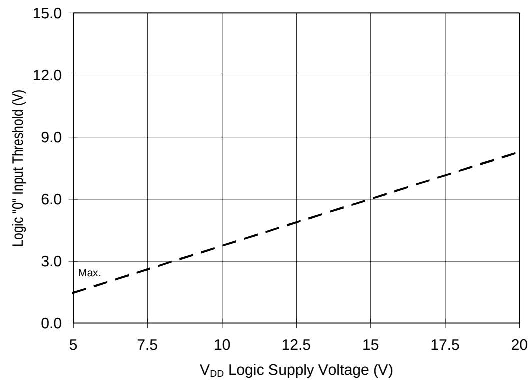


Figure 13B. Logic “0” Input Threshold vs. Voltage

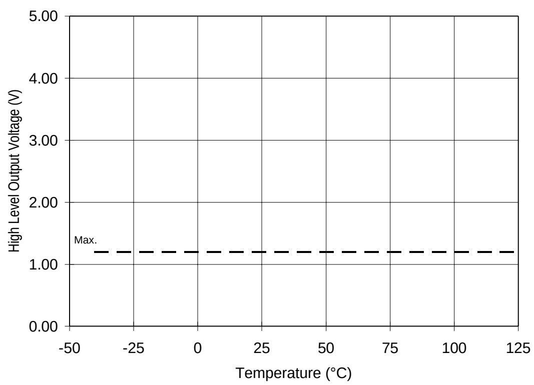


Figure 14A. High Level Output vs. Temperature

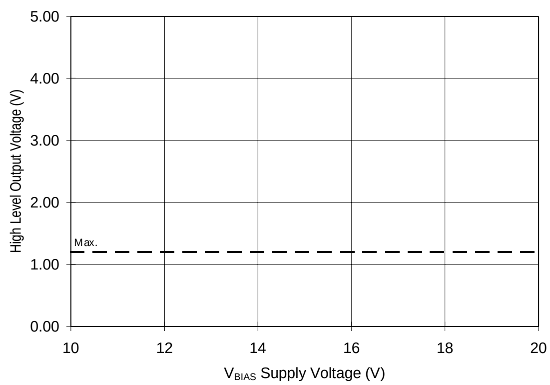


Figure 14B. High Level Output vs. Voltage

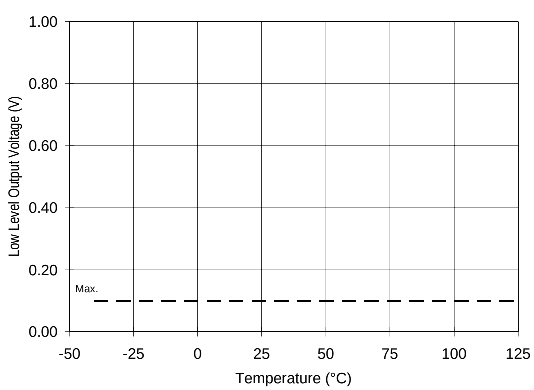


Figure 15A. Low Level Output vs. Temperature

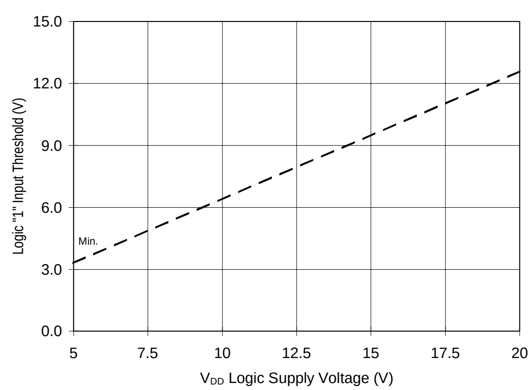


Figure 15B. Low Level Output vs. Voltage

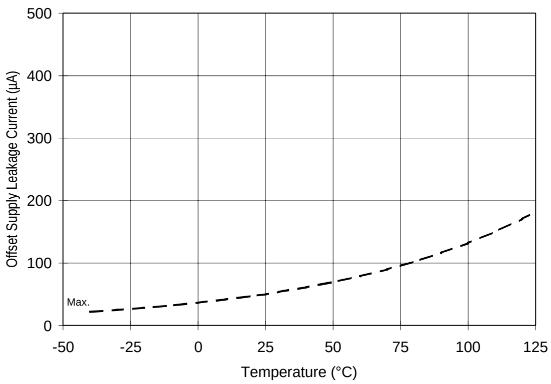


Figure 16A. Offset Supply Current vs. Temperature

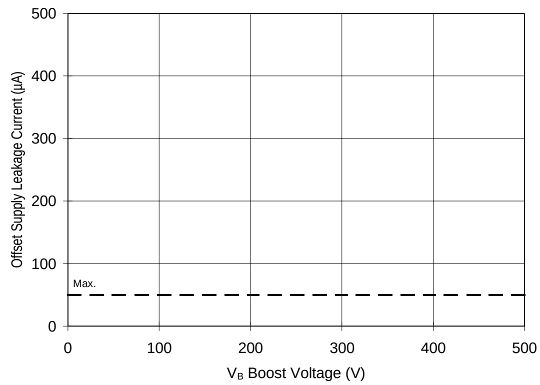


Figure 16B. Offset Supply Current vs. Voltage

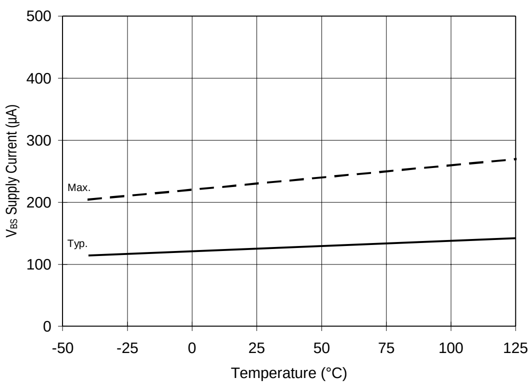


Figure 17A. V_{BS} Supply Current vs. Temperature

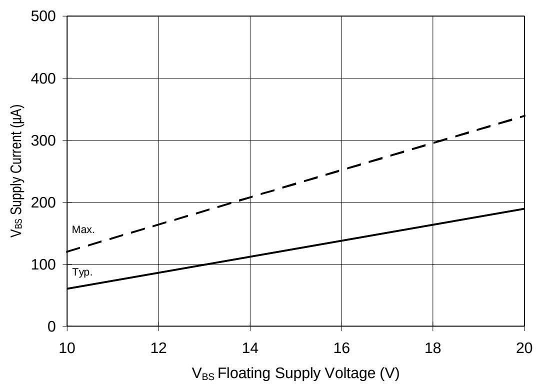


Figure 17B. V_{BS} Supply Current vs. Voltage

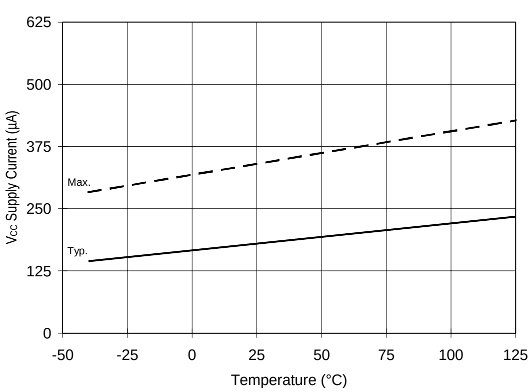


Figure 18A. V_{CC} Supply Current vs. Temperature

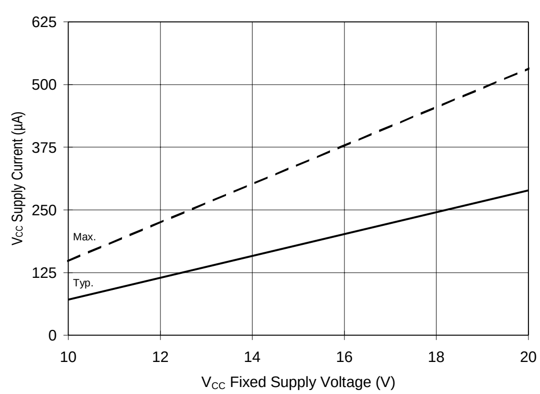


Figure 18B. V_{CC} Supply Current vs. Voltage

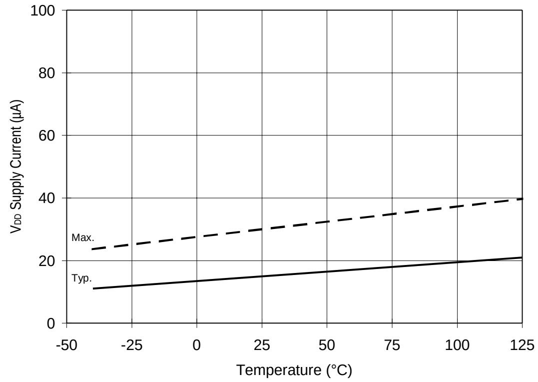


Figure 19A. V_{DD} Supply Current vs. Temperature

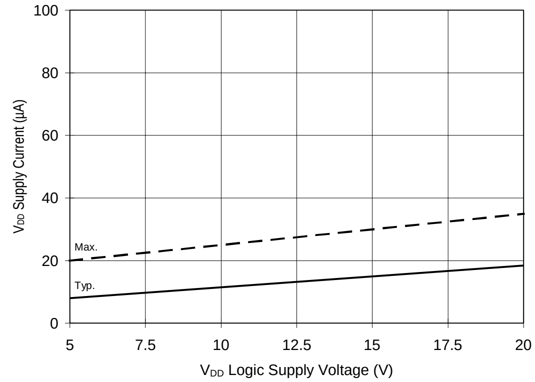


Figure 19B. V_{DD} Supply Current vs. Voltage

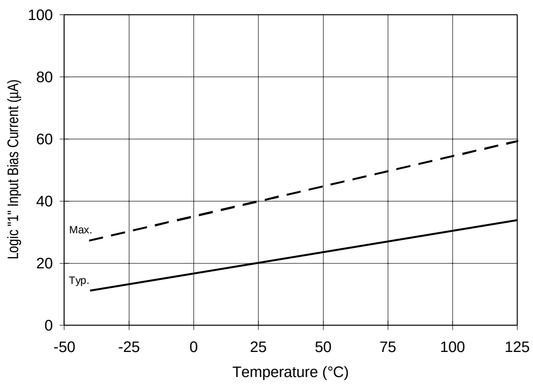


Figure 20A. Logic "1" Input Current vs. Temperature

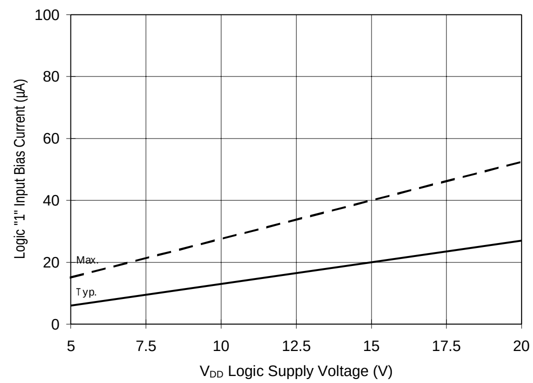


Figure 20B. Logic "1" Input Current vs. Voltage

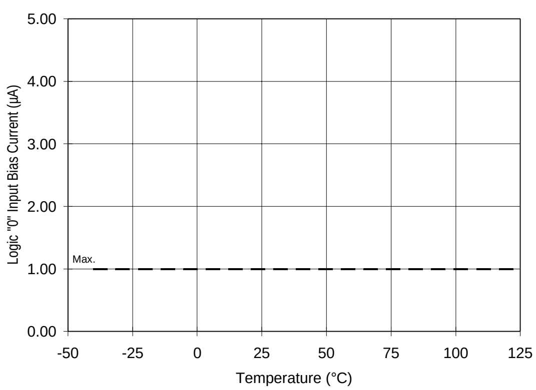


Figure 21A. Logic "0" Input Current vs. Temperature

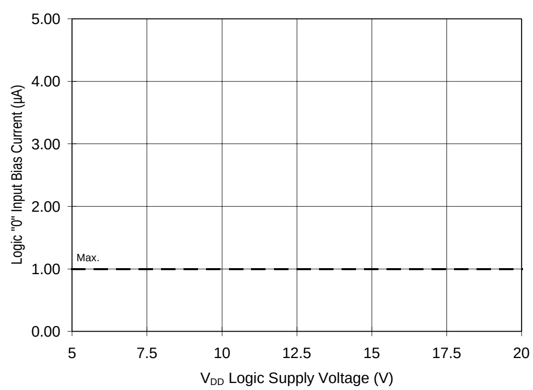


Figure 21B. Logic "0" Input Current vs. Voltage

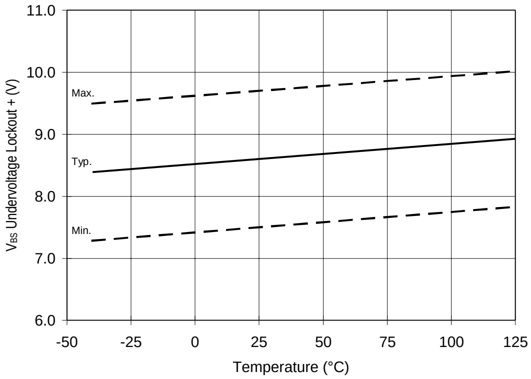


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

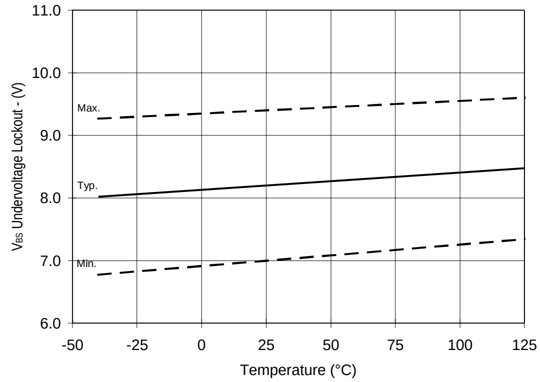


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

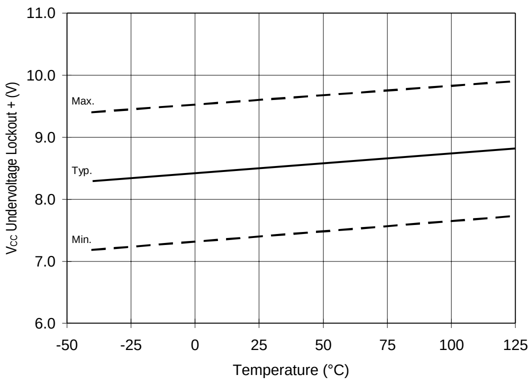


Figure 24. V_{CC} Undervoltage (+) vs. Temperature

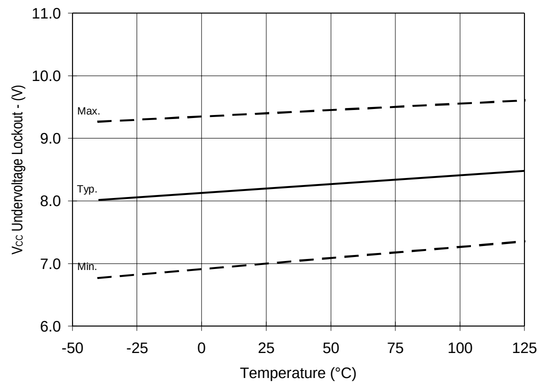


Figure 25. V_{CC} Undervoltage (-) vs. Temperature

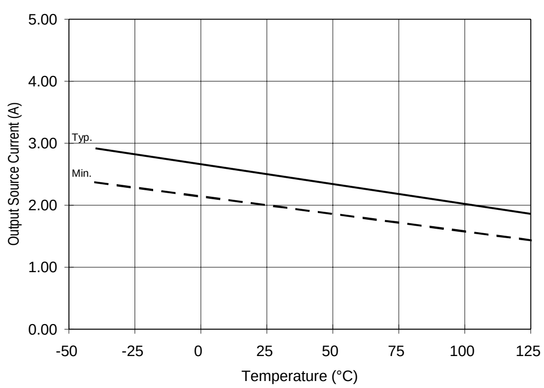


Figure 26A. Output Source Current vs. Temperature

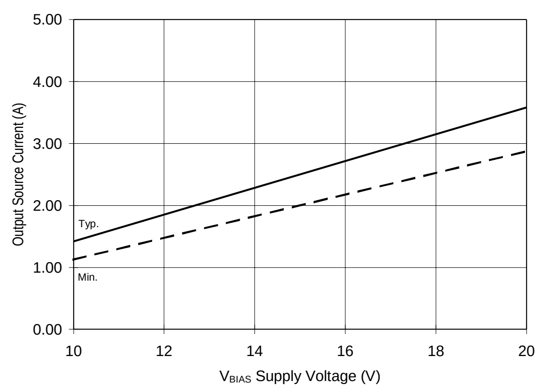


Figure 26B. Output Source Current vs. Voltage

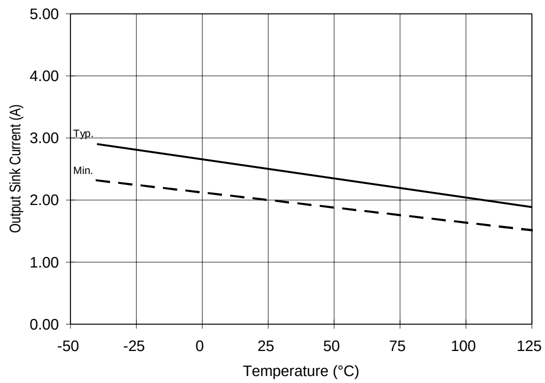


Figure 27A. Output Sink Current vs. Temperature

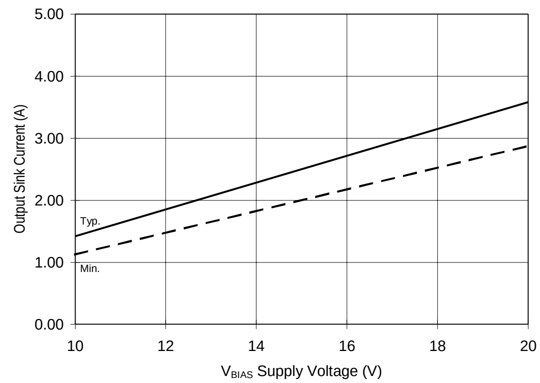


Figure 27B. Output Sink Current vs. Voltage

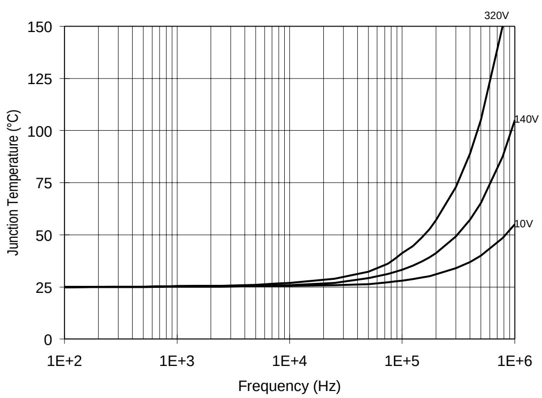


Figure 28. IR2110 T_J vs. Frequency (IRFBC20)
R_{GATE} = 33Ω, V_{CC} = 15V

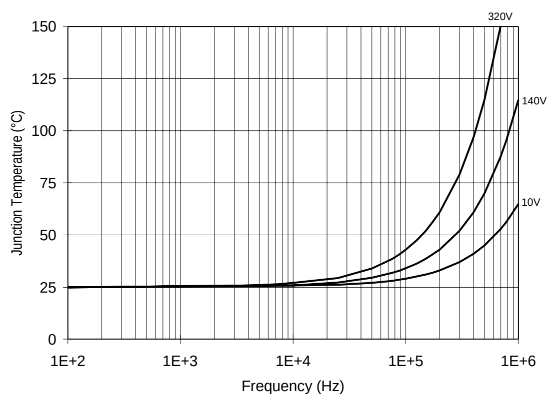


Figure 29. IR2110 T_J vs. Frequency (IRFBC30)
R_{GATE} = 22Ω, V_{CC} = 15V

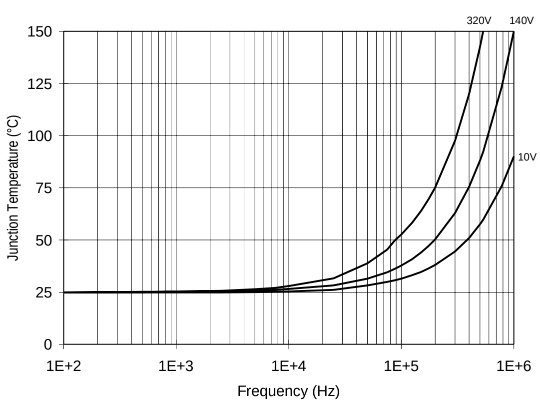


Figure 30. IR2110 T_J vs. Frequency (IRFBC40)
R_{GATE} = 15Ω, V_{CC} = 15V

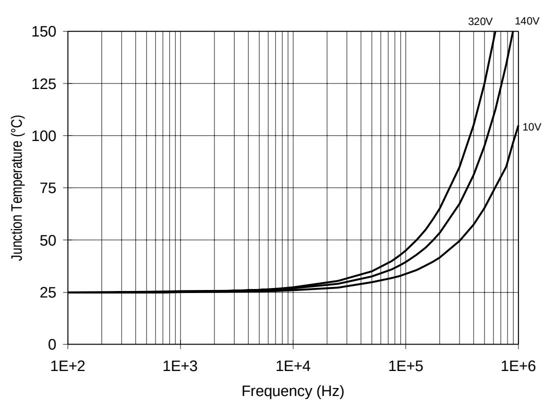


Figure 31. IR2110 T_J vs. Frequency (IRFPE50)
R_{GATE} = 10Ω, V_{CC} = 15V

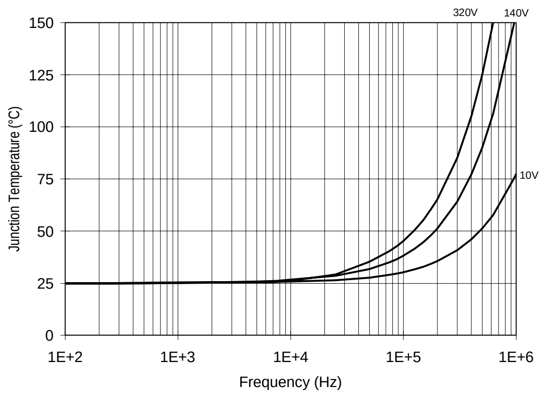


Figure 32. IR2110S T_J vs. Frequency (IRFBC20) R_{GATE} = 33Ω, V_{CC} = 15V

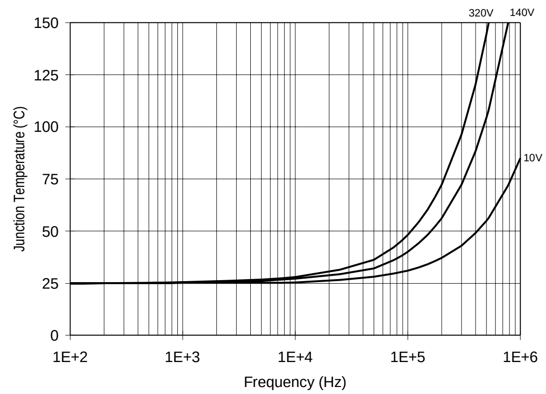


Figure 33. IR2110S T_J vs. Frequency (IRFBC30) R_{GATE} = 22Ω, V_{CC} = 15V

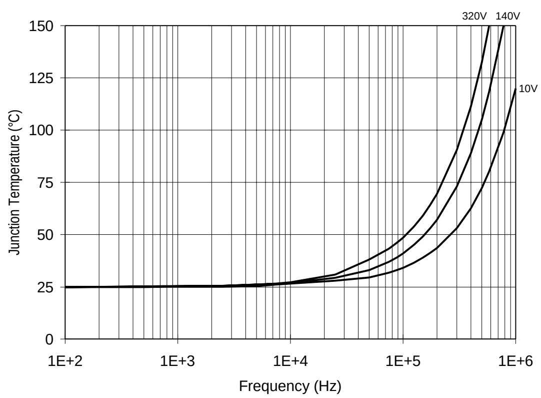


Figure 34. IR2110S T_J vs. Frequency (IRFBC40) R_{GATE} = 15Ω, V_{CC} = 15V

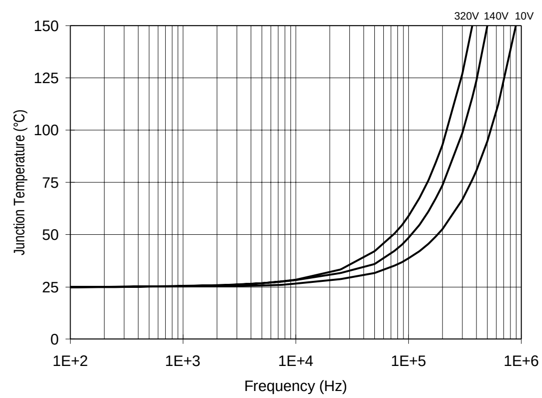


Figure 35. IR2110S T_J vs. Frequency (IRFPE50) R_{GATE} = 10Ω, V_{CC} = 15V

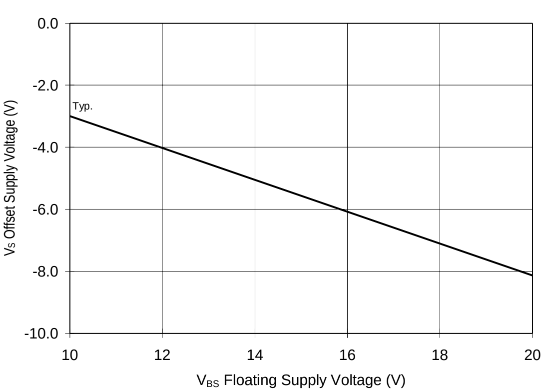


Figure 36. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

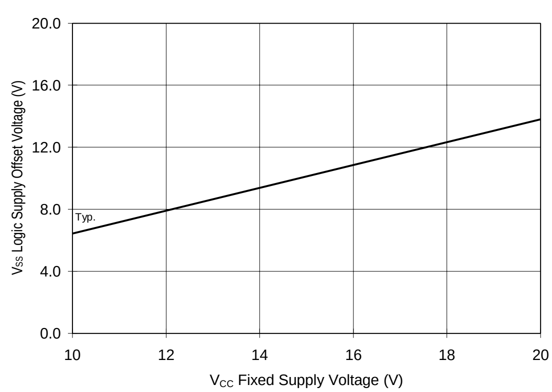
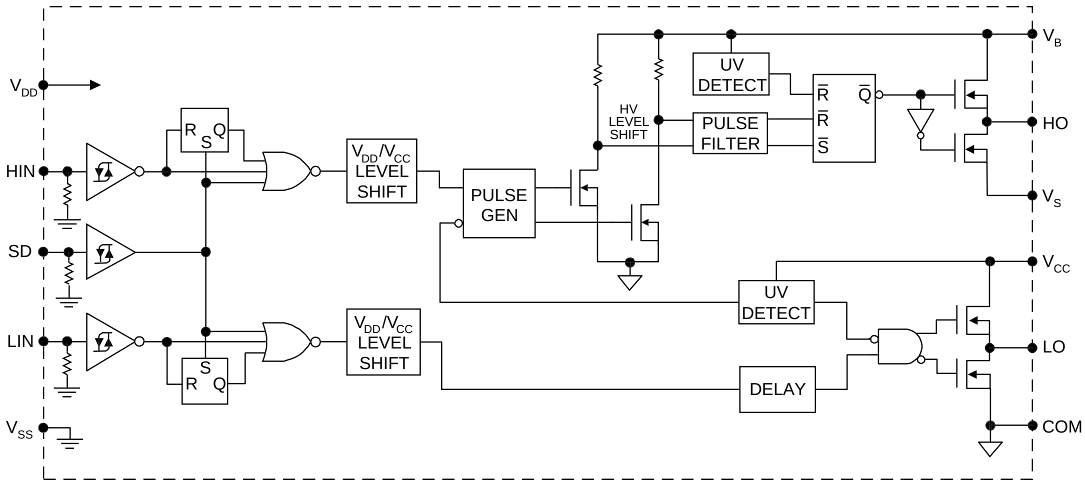


Figure 37. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage

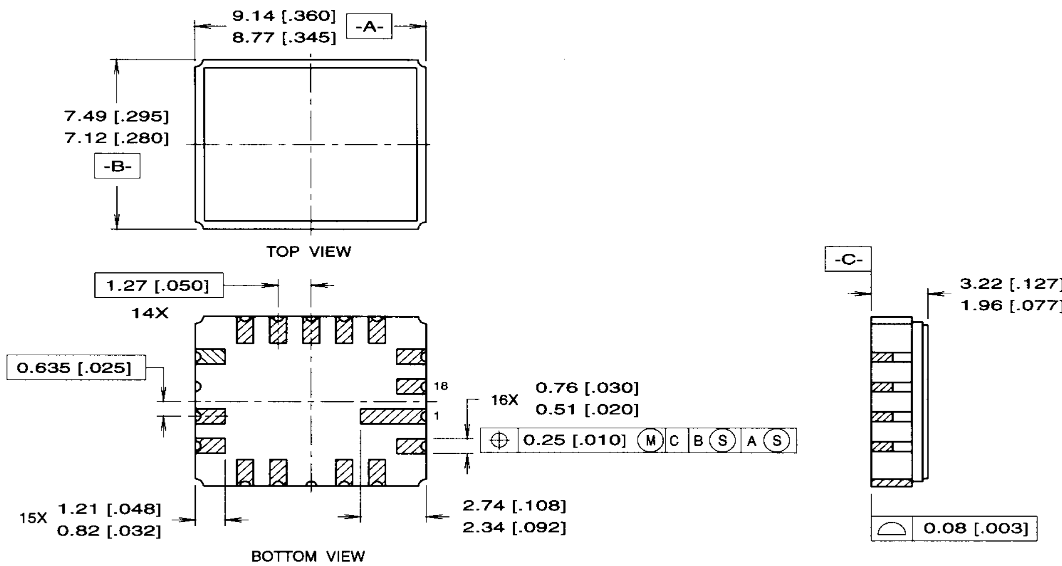
Functional Block Diagram

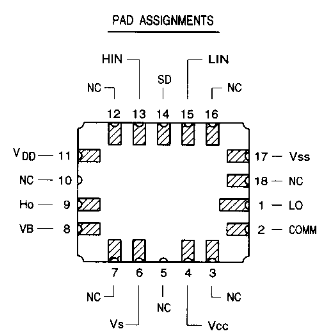


Lead Definitions

Lead Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Case Outline and Dimensions — Leadless Chip Carrier (LCC) Package





NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

International
IOR Rectifier

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IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
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