International
IOR Rectifier

ADVANCE INFORMATION **Data Sheet PD 60178A**

IR1175

Synchronous Rectifier Driver

Features

- Provides constant and proper gate drive to power MOSFETs regardless of transformer output
- Minimizes loss due to power MOSFET body drain diode conduction
- Stand alone operation - no ties to primary side
- Schmitt trigger input with double pulse suppression allows operation in noisy environments
- High current drive capability - 2A
- High speed operation - 2MHz
- Adaptable to multiple topologies (such as single-ended forward, double-ended forward)

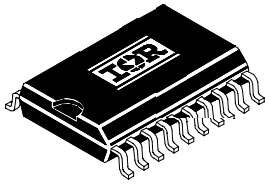
Product Summary

V_{dd}	5Vdc
$I_{O+/-}$	2A/2A
F_{max}	2MHz
Max lead time	500nsec

Description

The IR1175 is a high speed CMOS controller designed to drive N-channel power MOSFETs used as synchronous rectifiers in high current, high frequency forward converters with output voltages equal or below 5VDC. Schmitt trigger inputs with double pulse suppression allow the controller to operate in noisy environments. The circuit does not require any ties to the primary side and derives its operating power directly from the secondary. The circuit functions by anticipating transformer output transitions, then turns the power MOSFETs on or off before the transitions of the transformer to minimize body drain diode conduction and reduce associated losses. Turn on/off lead time can be adjusted to accommodate a variety of power MOSFET sizes and circuit conditions. The IR1175 also provides gate drive overlap/dead-time control via external components to further minimize diode conduction by nulling effects of secondary loop and device package inductance.

Package



20 Lead Surface Mount (SSOP-20)

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur.

Symbol	Definition	Min.	Max.	Units
V_{dd}	Supply voltage	—	7	V_{DC}
I_{in}	Input clamp current	—	+/- 10	mA_{DC}
P_D	Power dissipation (SSOP-20)	—	400	mW
Rth_{JC}	Thermal resistance (SSOP-20) junction-to-case	—	28.5	°C/W
Rth_{JA}	Thermal resistance (SSOP-20) junction-to-ambient	—	90.5	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	°C
T_L	Lead temperature (soldering, 10 seconds)	—	300	°C

Recommended Operating Conditions

Symbol	Definition	Min.	Typ.	Max.	Units
Vdd	Supply voltage operating range	—	5	—	V_{DC}
T_A	Ambient temperature	−40	—	85	°C
Freq	Operating frequency	250	—	500	KHz
Rbias	Required bias resistor (+/- 1%)	—	69.8	—	KW
UV	Voltage at UVSET pin	1.75	—	2.25	V_{DC}
Xin	Maximum voltage at X1 and X2 inputs	—	—	5.6	V_{DC}
Cd1/Cd2	Capacitance at pins DTIN1 and DTIN2	—	—	22	pF
Cf	Loop filter bypass capacitor	470	—	—	KW

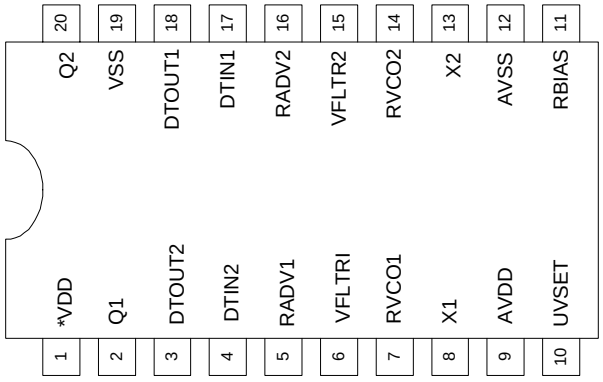
Dynamic Electrical Characteristics

Vdd=5V, T_A = 25°C, Rbias = 69.8K unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units
Vdd	Supply voltage operating range	4.0	—	5.5	V_{DC}
Iqdd	Vdd quiescent current (Vin=0 or 5V, Iout=0)	—	3	5	mA_{DC}
Freq	Operating frequency	100	—	2000	KHz
UVSET+	UVSET positive going threshold	1.10	—	1.4	V
UVSET-	UVSET negative going threshold	0.8	—	1.1	V
Vxth+	X1/X2 Input positive going threshold	—	1.4	—	V_{DC}
Vxth-	X1/X2 Input negative going threshold	—	1.0	—	V_{DC}
Tadv	Externally adjustable lead time (advance)	—	—	500	nsec
Td	Externally adjustable dead-time for Q1 and Q2	20	—	—	nsec
Isink	Q1,Q2 output sink current (Vdd=5.0V, pulsed, 10 usec)	—	—	2	A
Isource	Q1,Q2 output source current (Vdd=5.0V, pulsed, 10 usec)	—	—	2	A
tio	Input to output delay (PLL bypassed, cross coupled mode)	—	20	—	nsec
tr	Gate turn-on rise time (C1=1000pf, Vdd=5V)	—	20	—	nsec
tf	Gate turn-off fall time (C1=1000pf, Vdd=5V)	—	20	—	nsec
Vtr	Cross-over voltage (Vdd=5Vdc, DTIN shorted to DTOUT, C1=1000pf) Fig. 3	—	2.5	—	V_{DC}
Rbias	Required bias resistor	68	—	71	KW
Vbias	Voltage at Rbias pin	—	1.25	—	V_{DC}
Tjitter	Phase-lock loop output jitter	-20	—	20	nsec
Ichgpump	Charge pump output current (at VFLTR pin)	—	50	—	mA_{DC}
Vchgpump	Charge pump output voltage (at VFLTR pin)	1.3	1.5	1.7	V_{DC}
Kvco_dc	PLL Vco DC gain	—	62	—	KHz/

Lead Definitions and Assignments

Symbol	Description
AVDD	Power - + 5 V_{DC} to MOSFET drivers
Q1	Output - gate drive for Q1 power MOSFET
DTOUT1	Output - sets dead time for Q1 output - used with DTIN1
DTIN1	Input - sets dead time for Q1 - used with DTOUT1
RADV1	Output - sets lead time (advance) for Q1
VFLTR1	Output - PLL loop filter for Q1 output
RVCO1	Output - sets PLL center frequency for Q1 output
X1	Input - transformer input for Q1
VDD	Power - +5 Vdc for internal logic
UVSET	Input - sets UVLO+ If this pin is pulled below 1.25VDC externally, then both Q1 and Q2 outputs will be at Vss (disabled)
RBIAS	Output - connected to 249K +/- 1% resistor - sets operating current
AVSS	Ground for logic supply (AVDD)
X2	Input - transformer input for Q2
RVCO2	Output - sets PLL center frequency for Q2 output
VFLTR2	Output - PLL loop filter for Q2
RADV2	Output - sets lead time (advance) for Q2
DTIN2	Input - sets dead time for Q2 - used with DTOUT2
DTOUT2	Output - sets dead time for Q2 - used with DTIN2
VSS	Ground for MOSFET driver supply (VDD)
Q2	Output - gate drive for Q2 power MOSFET



20 Lead SSOP
IR1175

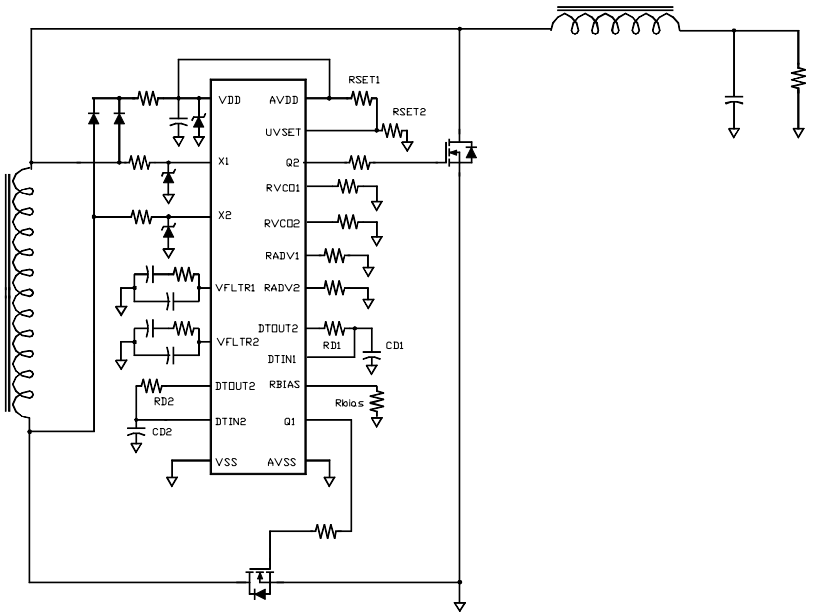


Fig. 1 Typical application circuit when supply Vout < 5.0 V_{DC}

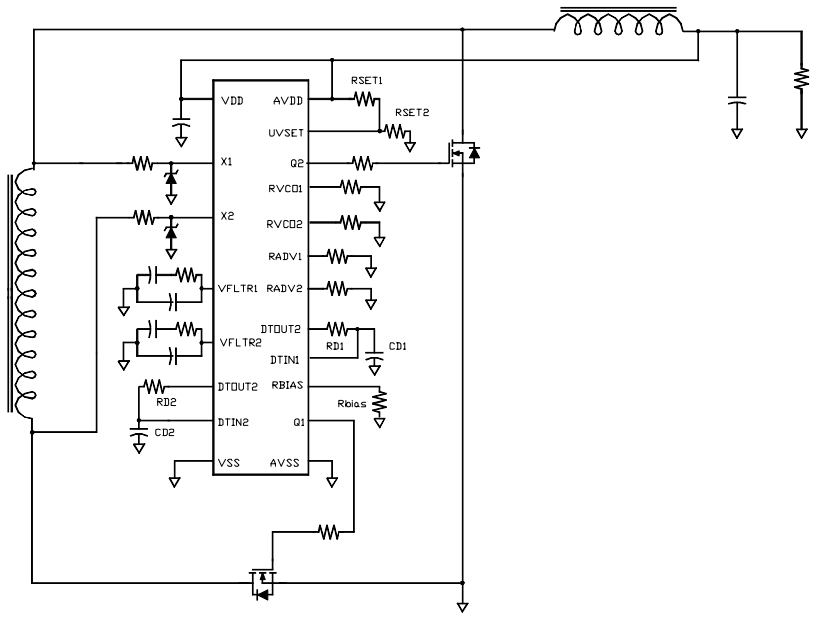


Fig. 2 Typical application circuit when supply Vout = 5.0 V_{DC}

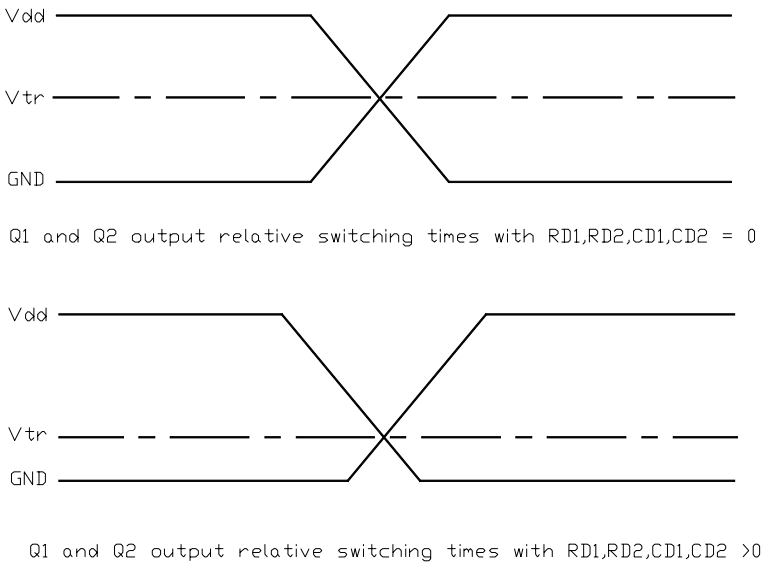


Fig. 3 Gate drive characteristics and definitions

Phase Lock Loop Design Equations:

1 - Resistor to set VCO Ceter Frequency:

Rvco (KW) = 143 x [Vchgpump(V_{DC}) / fvco(KHz)] x Kvco _ dc(KHz/mA)

Example (A): Choose Vchgpump = 1.5V, desired frequency (fvco) = 300KHz

Rvco = 143 x [1.5 /300] x 62 Hz/mA = 44.33 KW

2 - Small Signal gain for VCO:

Kvco_ac (KHz/Volt) = 1E3 x Kvco_dc (KHz/mA)/(7 x Rvco(KW)

Example (B): Choosing same conditions as in example A:

Kvco_ac = 1E3 x 62 / (7 x 44.33) = 199.9 KHz/volt

3 - PLL Natural frequency:

$$\omega n = 2\pi fn(KHz) = \sqrt{Ichpump(uA) \times Kvco\_ac(KHz/V) / C(nF)}$$

Choose Cf such that **Cf=C/16** (Minimum value for Cf=470pF)

4 - PLL Damping factor calculations:

$$P = \pi E\text{-}3 \times Rf\ (KOhms) \times C(nF) \times fn(KHz)$$

Typical value for P is 0.707. (Critically damped)

5 - Advance timing:

$$Tadv(nsec) = RADV\ (KOhms)*10 - 10$$

Where RADV is resistance from RADV1 or RADV2 to ground.
Example C: RADV=10Kohms will result in Tadv=10*10 - 10 =90 nsec .

6- Dead time calculations:

$$Td(nsec) = 0.69*Rdt(KOhms)*Cdt(pF) + 5 \quad (For\ Vdd=5\ V)$$

Where Rdt is resistance between pins DTIN1 and DTOUT1 or DTIN2 and DTOUT2. Cdt is capacitance from DTIN1 or DTIN2 to ground.
Example D: Rdt=10Kohms and Cdt=22pF will result in: Td=156.8 nsec

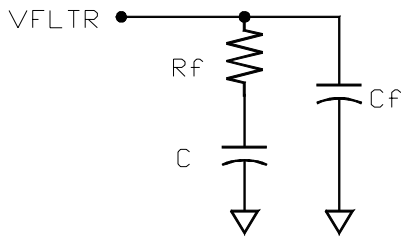


Fig. 4 PLL loop filter component definitions

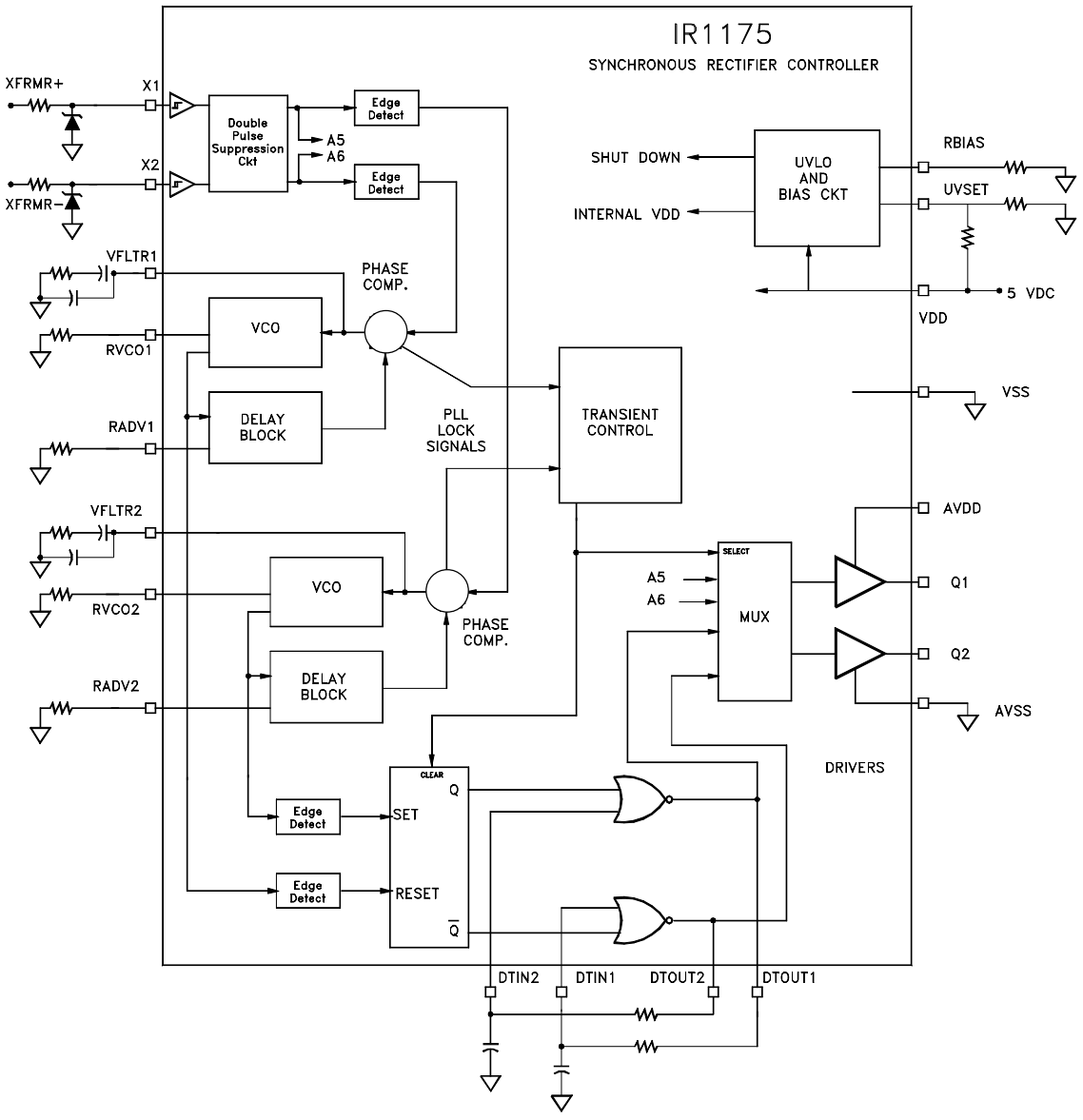
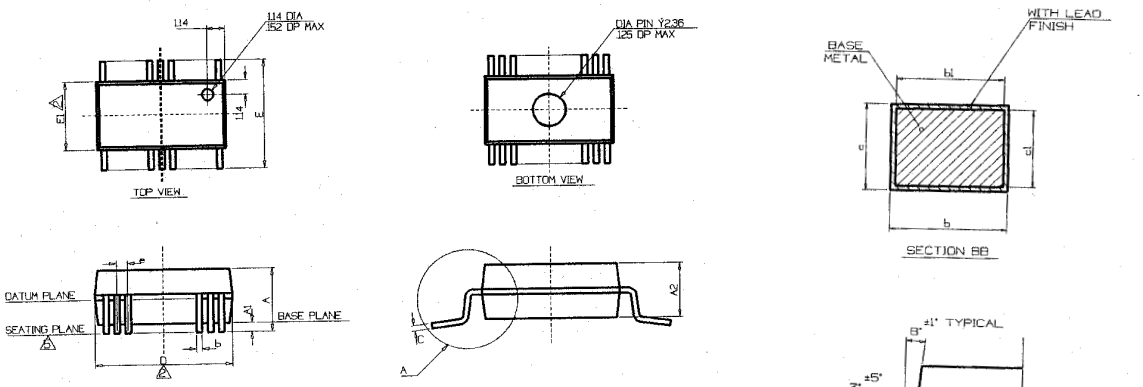


Fig. 5 IR1175 Block Diagram



SYMBOL	COMMON DIMENSION						NOTE
	MIN		NOM		MAX		
	INCH	MM	INCH	MM	INCH	MM	
A	.068	1.73	.073	1.86	.078	2.00	
A1	.002	0.05	.005	0.13	.008	0.20	
A2	.065	1.65	.069	1.75	.073	1.85	
b	.009	0.22	.012	0.30	.015	0.38	
b1	.009	0.22	.012	0.30	.013	0.33	
c	.004	0.09	.006	0.15	.010	0.25	
c1	.004	0.09	.006	0.15	.008	0.21	
D	SEE VARIATIONS						2
E	.291	7.40	.307	7.80	.323	8.20	
E1	.197	5.00	.209	5.30	.221	5.60	2
e	.026 INCH 0.65 MM BSC						
L	.022	0.55	.030	0.75	.037	0.95	3
N	SEE VARIATIONS						4
R	.004	0.09					
θ	0°		4°		8°		

NOTE	2						4
VARIATIONS	D						N
	MIN		NOM		MAX		
	INCH	MM	INCH	MM	INCH	MM	
AE	.271	6.90	.283	7.20	.295	7.50	20

NOTE:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. "D" & "E1" ARE REFERANCE DATUMS AND DO NOT INCLUDE MOLD DEFLASH OR PROTRUSIONS.BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE.MOLD DEFLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15(.006") PER SIDE. END FLASH FROM THE PACKAGE BODY SHALL NOT EXCEED 0.15(.006") PER SIDE (D).
3. DIMENSION L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
4. 'N' IS THE NUMBER OF THE TERMINAL POSITIONS.
5. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.10(.004") AT SEATING PLANE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. DAMBAR PROTRUSION TO BE 0.13mm(.005") MAX PER SIDE.

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