Data Sheet No.PD 60151-I

International
IOR Rectifier

IPS031G/IPS032G

SINGLE/DUAL FULLY PROTECTED POWER MOSFET SWITCH

Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Low current & logic level input
- E.S.D protection

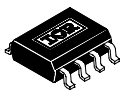
Description

The IPS031G/IPS032G are fully protected single/dual low side SMART POWER MOSFETs that feature over-current, over-temperature, ESD protection and drain to source active clamp.These devices combine a HEXFET® POWER MOSFET and a gate driver. They offer full protection and high reliability required in harsh environments. The driver allows short switching times and provides efficient protection by turning off the power MOSFET when the temperature exceeds 165°C or when the drain current reaches 12A. The device restarts once the input is cycled. The avalanche capability is significantly enhanced by the active clamp and covers most inductive load demagnetizations.

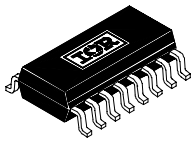
Product Summary

$R_{ds(on)}$	70mΩ (max)
V_{clamp}	50V
Ishutdown	12A
T_{on}/T_{off}	1.5µs

Packages

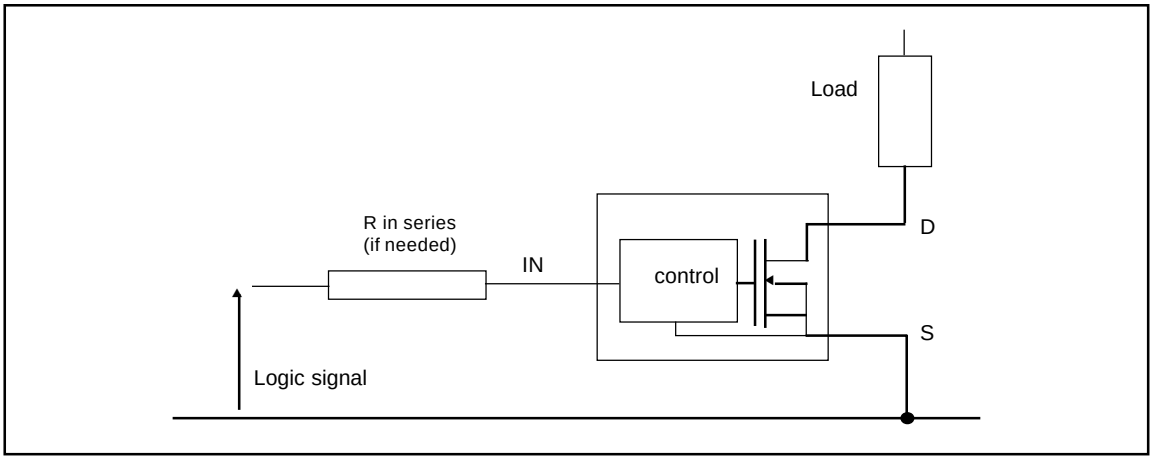


8 Lead SOIC
IPS031G



16 Lead SOIC
IPS032G
(Dual)

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to SOURCE lead. ($T_{Ambient}$ = 25°C unless otherwise specified). PCB mounting uses the standard footprint with 70 µm copper thickness. All Sources leads of each mosfet must be connected together to get full current capability

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{ds}	Maximum drain to source voltage	—	47	V	
V_{in}	Maximum input voltage	-0.3	7		
$I_{in, max}$	Maximum IN current	-10	+10	mA	
$I_{sd\ cont.}$	Diode max. continuous current (1)			A	
	(rth=125°C/W) IPS031G	—	1.4		
	(for all sd mosfets, rth=85°C/W) IPS032G	—	2		
$I_{sd\ pulsed}$	Diode max. pulsed current (1) (for ea. mosfet)	—	15		
Pd	Maximum power dissipation(1)			W	
	(rth=125°C/W) IPS031G	—	1		
	(for all Pd mosfets, rth=85°C/W) IPS032G	—	1.5		
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10µH
T_j max.	Max. storage & operating junction temp.	-40	+150	°C	

Thermal Chacteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th1}	Thermal resistance with standard footprint	—	100	—	°C/W	SOIC-8
R_{th2}	Thermal resistance with 1" square footprint	—	65	—		
R_{th1} (2 mos on)	Thermal resistance with standard footprint (2 mosfets on)	—	85	—		SOIC-16
R_{th2} (1 mos on)	Thermal resistance with standard footprint (1 mosfet on)	—	100	—		
R_{th3} (2 mos on)	Thermal resistance with 1" square footprint (2 mosfets on)	—	60	—		

(1) Limited by junction temperature (pulsed current limited also by internal wiring)

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
$V_{ds\ (max)}$	Continuous Drain to Source voltage	—	35	V
V_{IH}	High level input voltage	4	6	
V_{IL}	Low level input voltage	0	0.5	
I_{ds} $T_{amb}=85^oC$	Continuous drain current (TAmbient = 85°C, IN = 5V, rth = 100°C/W, Tj = 125°C) IPS031G	—	2.2	A
	(TAmbient = 85°C, IN = 5V, rth = 85°C/W, Tj = 125°C) IPS032G	—	1.65	
R_{in}	Recommended resistor in series with IN pin	0.2	5	kΩ
$T_{r\text{-}in(max)}$	Max recommended rise time for IN signal (see fig. 2)	—	1	µS
$F_{r\text{-}Isc}$ (2)	Max. frequency in short circuit condition (Vcc = 14V)	0	1	kHz

Static Electrical Characteristics

($T_j = 25^oC$ unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$	ON state resistance $T_j = 25^oC$	20	45	60	mΩ	V_{in} = 5V, I_{ds} = 1A
$R_{ds(on)}$	ON state resistance $T_j = 150^oC$	—	75	100		
I_{dss} @Tj=25°C	Drain to source leakage current	0	0.5	25	µA	V_{cc} = 14V, T_j = 25°C
I_{dss2} @Tj=25°C	Drain to source leakage current	0	5	50		V_{cc} = 40V, T_j = 25°C
V clamp 1	Drain to source clamp voltage 1	47	52	56	V	I_d = 20mA (see Fig.3 & 4)
V clamp 2	Drain to source clamp voltage 2	50	53	60		I_d=$I_{shutdown}$ (see Fig.3 & 4)
$V_{in\ clamp}$	IN to source clamp voltage	7	8.1	9.5		I_{in} = 1 mA
V_{th}	IN threshold voltage	1	1.6	2		I_d = 50mA, Vds = 14V
$I_{in,\ -on}$	ON state IN positive current	25	90	200	µA	V_{in} = 5V
$I_{in,\ -off}$	OFF state IN positive current	50	130	250		V_{in} = 5V over-current triggered

Switching Electrical Characteristics

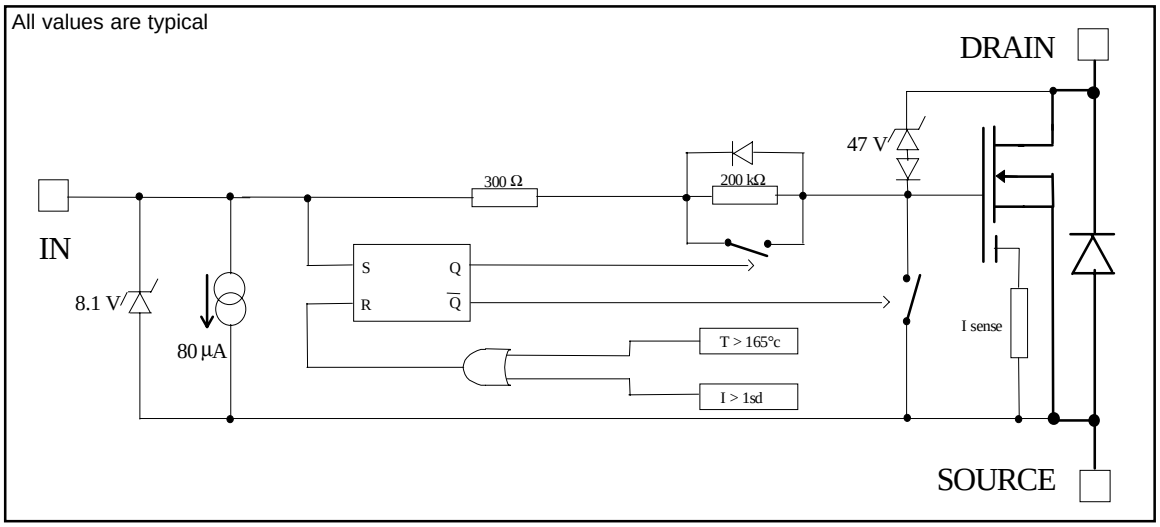
V_{cc} = 14V, Resistive Load = 5Ω (IPS031), Resistive Load = 3Ω (IPS031S), Rinput = 50Ω, 100µs pulse,T_j = 25°C, (unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{on}	Turn-on delay time	0.05	0.3	0.6	µs	See figure 2
T_r	Rise time	0.4	1	2		
T_{rf}	Time to 130% final $R_{ds(on)}$	—	8	—		
T_{off}	Turn-off delay time	0.8	2	3.5		See figure 2
T_f	Fall time	0.5	1.5	2.5		
Q_{in}	Total gate charge	—	1.1	—	nC	V_{in} = 5V

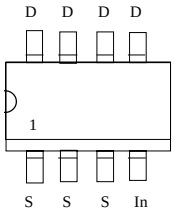
Protection Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{sd}	Over temperature threshold	—	165	—	°C	See fig. 1
I_{sd}	Over current threshold	10	14	18	A	See fig. 1
V_{reset}	IN protection reset threshold	1.5	2.3	3	V	
T_{reset}	Time to reset protection	2	10	40	µs	V_{in} = 0V, Tj = 25°C
EOI_OT	Short circuit energy (see application note)	—	400	—	µJ	V_{cc} = 14V

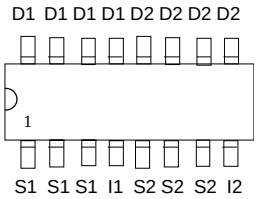
Functional Block Diagram



Lead Assignments



8 Lead SOIC



16 Lead SOIC
(Dual)

IPS031G	IPS032G
Part Number	

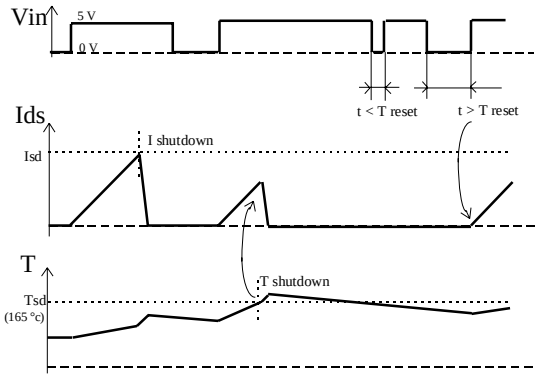


Figure 1 - Timing diagram

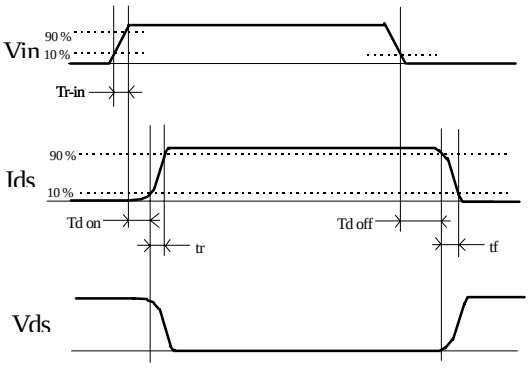


Figure 2 - IN rise time & switching time definitions

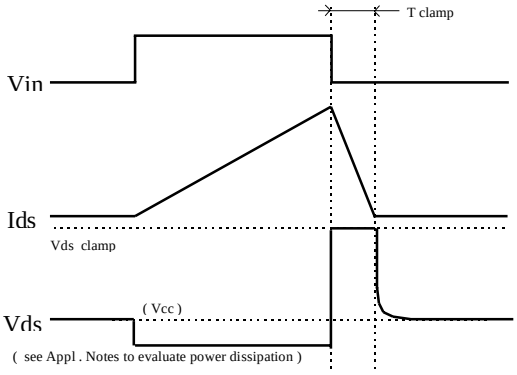


Figure 3 - Active clamp waveforms

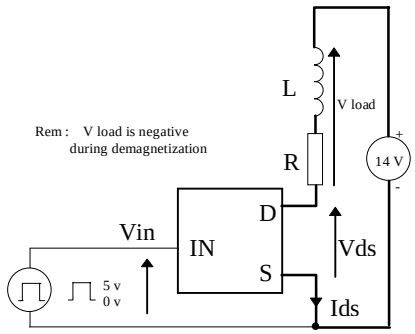


Figure 4 - Active clamp test circuit

All curves are typical values with standard footprints. Operating in the shaded area is not recommended.

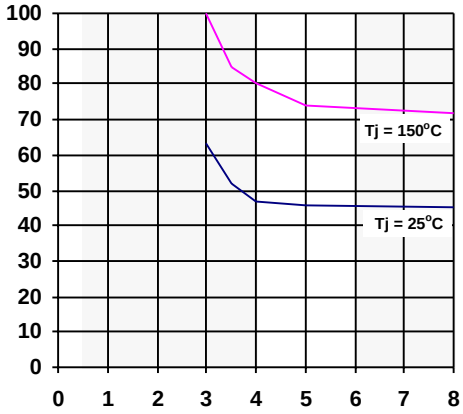


Figure 5 - Rds ON (mΩ) Vs Input Voltage (V)

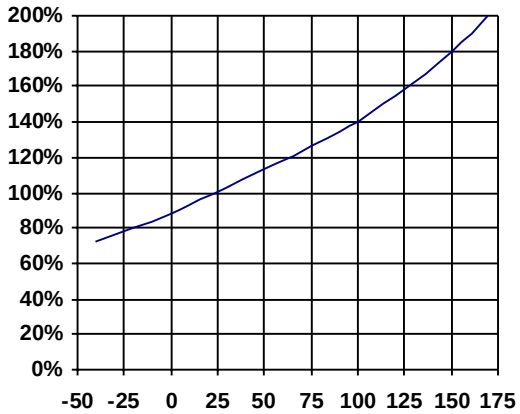


Figure 6 - Normalised Rds ON (%) Vs Tj (°C)

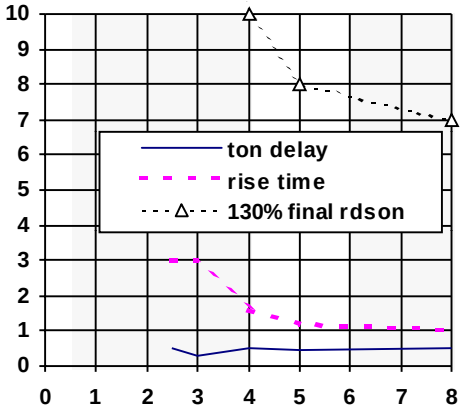


Figure 7 - Turn-ON Delay Time, Rise Time & Time to 130% final Rds(on) (us) Vs Input Voltage (V)

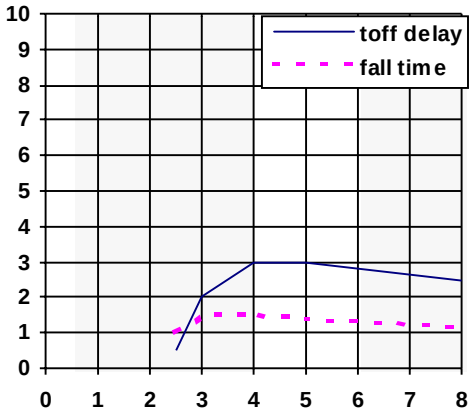


Figure 8 - Turn-OFF Delay Time & Fall Time (us) Vs Input Voltage (V)

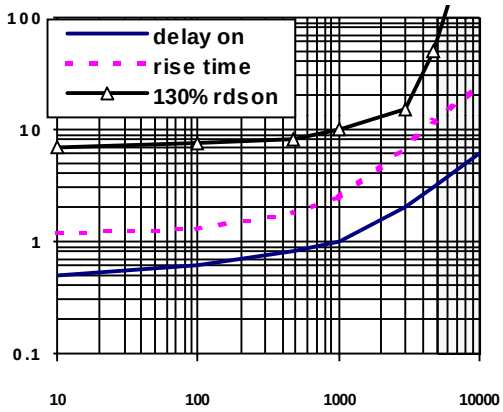


Figure 9 - Turn-ON Delay Time, Rise Time & Time to 130% final Rds(on) Vs IN Resistor (Ω)

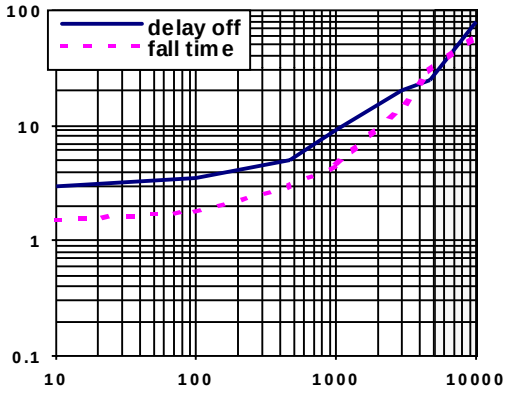


Figure 10 - Turn-OFF Delay Time & Fall Time (us) Vs IN Resistor (Ω)

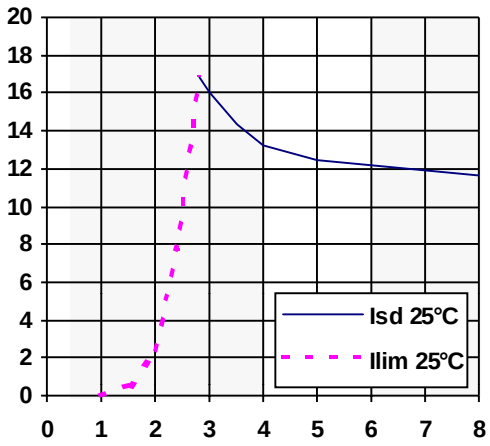


Figure 11 - Current limimitation & I shutdown (A) Vs Vin (V)

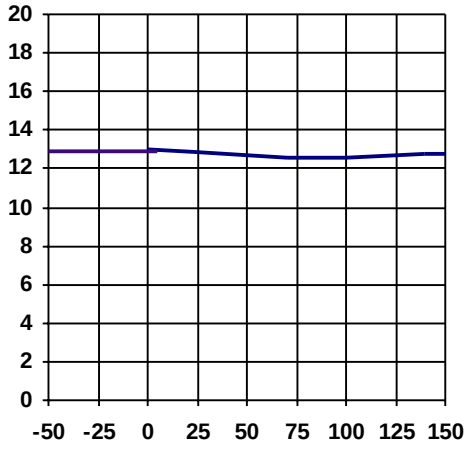


Figure 12 - I shutdown (A) Vs Temperature (^{O}C)

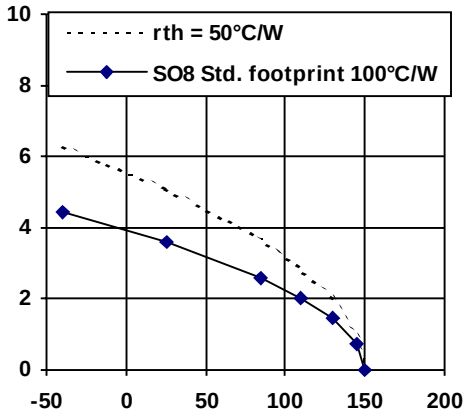


Figure 13a - Max.Cont. Ids (A)
Vs Amb. Temperature (°C) - IPS031G

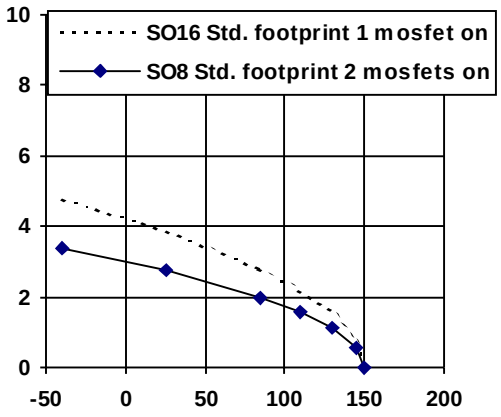


Figure 13b - Max.Cont. Ids (A)
Vs Amb. Temperature (°C) - IPS032G

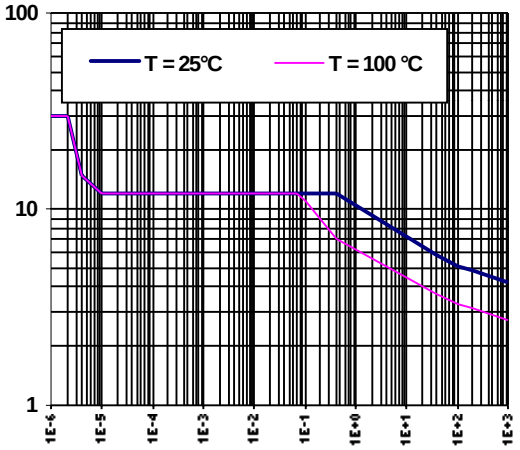


Figure 14 - Ids (A) Vs Protection Resp. Time (s)
IPS031G/IPS032G

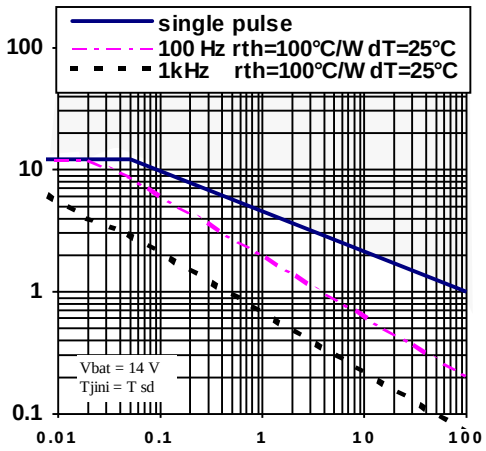


Figure 15 - Iclamp (A) Vs Inductive Load (mH)

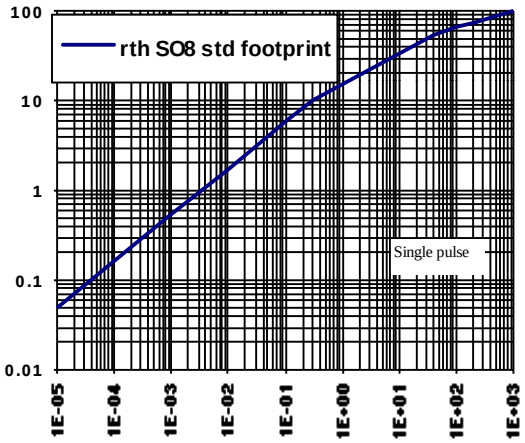


Figure 16a - Transient Thermal Imped. (ºC/W) Vs Time (s) - IPS031G

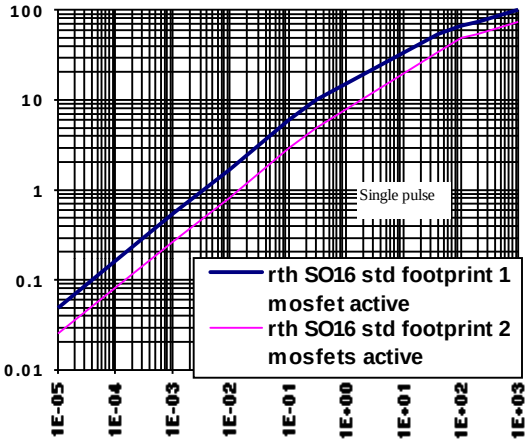


Figure 16b - Transient Thermal Imped. (ºC/W) Vs Time (s) - IPS032G

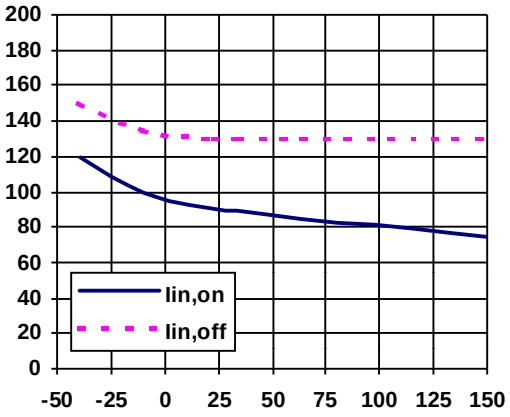


Figure 17 - Input current (µA) Vs Tj (ºC)

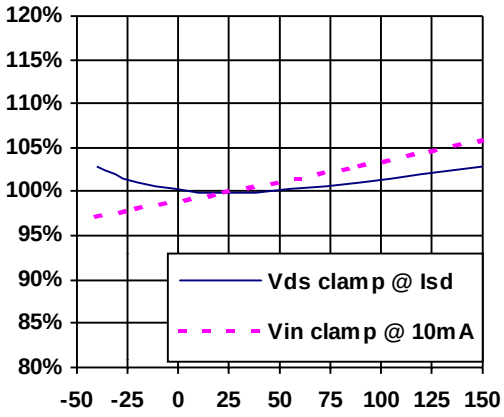


Figure 18 - Vin clamp and V clamp2 (%) Vs Tj (ºC)

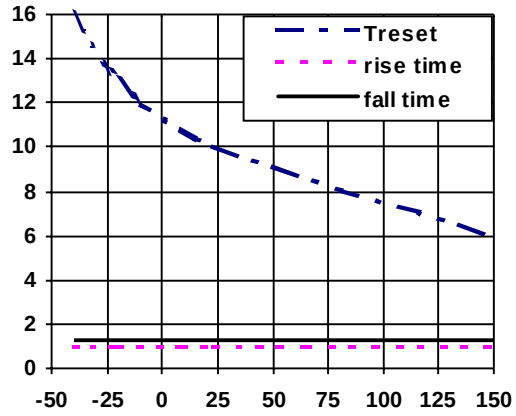
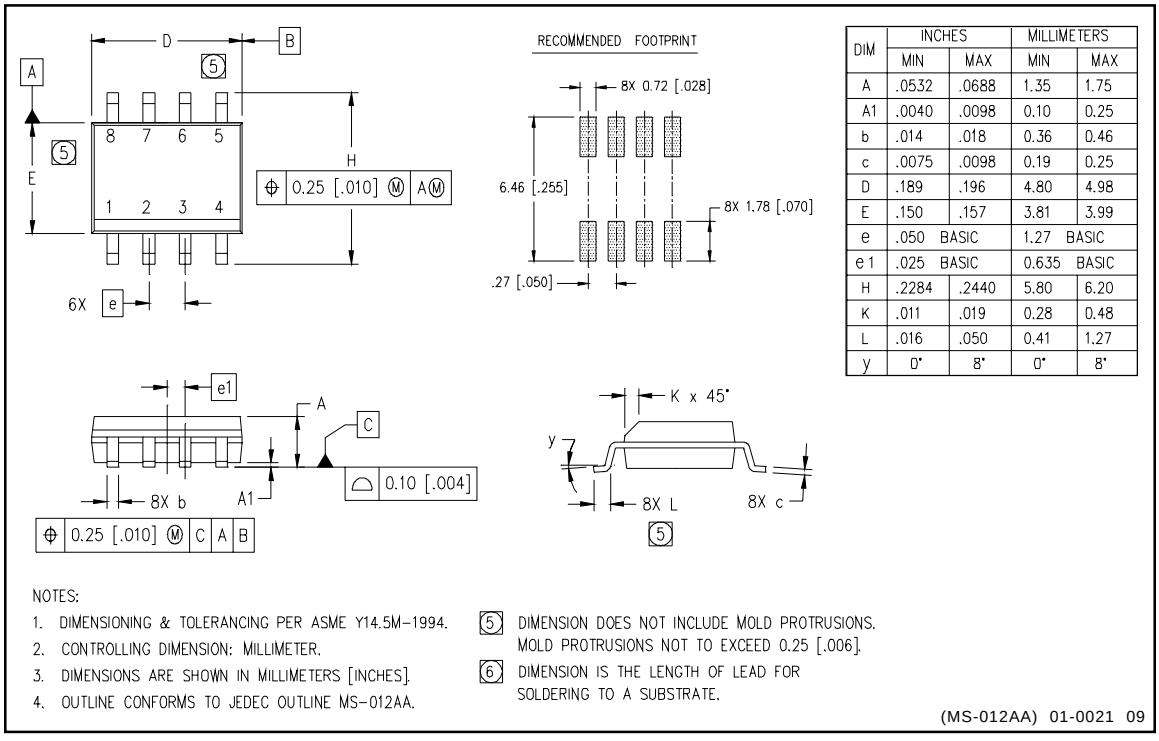


Figure 19 - Turn-on, Turn-off, and Treset (us)
Vs Tj (ºC)

Case Outline - 8 Lead SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

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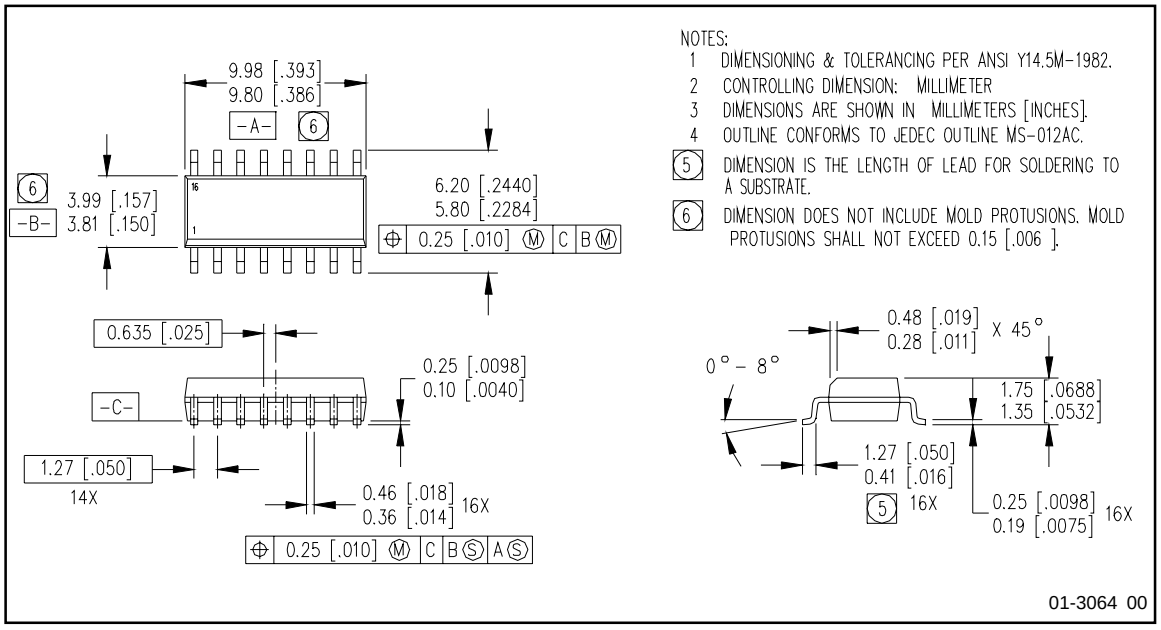
Case Outline - 16 Lead SOIC (narrow body)



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