iPOWIR™ TECHNOLOGY

Synchronous Buck Multiphase Optimized BGA Power Block

Integrated Power Semiconductors, Drivers & Passives

Features:

- 20A continuous output current with no derating up to T_{PCB} = 90°C
- Very small 11mm x 11mm x 3mm footprint
- Internal features minimize layout sensitivity *
- Optimized for very low power losses
- 5 to 12V input voltage

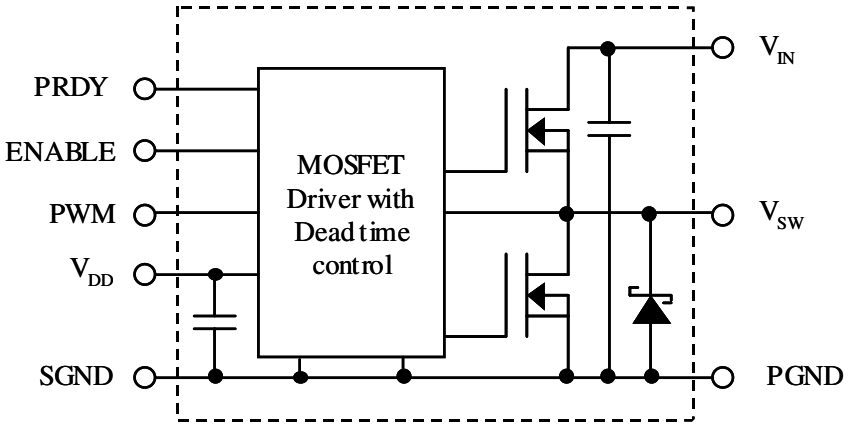
iP2001 Power Block

Description

The iP2001 is a fully optimized solution for high current synchronous buck multiphase applications. Board space and design time are greatly reduced because most of the components required for each phase of a typical discrete based multiphase circuit are integrated into a single 11mm x 11mm x 3mm BGA power block. The only additional components required for a complete multiphase converter are a PWM IC, the external inductors plus the input and output capacitors.

iPOWIR technology offers designers an innovative board space saving solution for applications requiring highest power density. iPOWIR technology eases design for applications where component integration offers benefits in performance and functionality. iPOWIR technology solutions are also optimized internally for layout, heat transfer and component selection.

iP2001 Internal Block Diagram



* All of the difficult PCB layout and bypassing issues have been addressed with the internal design of the iPOWIR Block. There are no concerns about double pulsing, unwanted shutdown, or other malfunctions which often occur in switching power supplies. The iPOWIR Block will function normally without any additional input power supply bypass capacitors. However, for reliable long term operation it is recommended that the adequate amount of input decoupling is provided on the V_{IN} pin. No additional bypassing is required on the V_{DD} pin.

Absolute Maximum Ratings :

Parameter	Min	Typ	Max	Units	Conditions
V_{IN} to PGND	-	-	16	V	
Sw Node to PGND	-0.3	-	17	V	
Output RMS Current	-	-	20	A	
V_{DD} to SGND	-	-	6.0	V	
DRV_IN to SGND	-0.3	-	6.0	V	
Enable to SGND	-0.3	-	6.0	V	
Storage Temperature	-40	-	125	°C	

Recommended Operating Conditions :

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
Input Voltage Range	V_{IN}	4.75	-	12.6	V	
Output Voltage Range	V_{OUT}	0.9	-	2.0	V	
Output Current Range	I_{OUT}	-	-	20	A	see Fig.2
Operating Frequency	fsw	150	-	1000	kHz	see Fig. 2

Electrical Specifications @ V_{DD} = 5V (Unless otherwise specified) :

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Block Power Loss ①	P_{BLK}	-	3.1	3.8	W	f_{SW}=500kHz, V_{IN}=12V, I_{OUT}=20A
Turn On Delay ②	$t_{d(on)}$	-	63	-	ns	I_{OUT}=20A, V_{OUT}=1.6V, f_{SW}=500kHz,
Turn Off Delay ②	$t_{d(off)}$	-	26	-		V_{IN}=12V
V_{IN} Quiescent Current	I_{Q-VIN}	-	-	1.0	mA	Enable=0V, V_{IN}=12V
V_{DD} Quiescent Current	I_{Q-VDD}	-	-	10	µA	Enable=0V, V_{DD}=5V
Under Voltage Lockout	UVLO					
Start Threshold	V_{START}	4.2	4.4	4.6	V	
Hysteresis	$V_{Hys-UVLO}$	-	.05	-		
Enable	Enable					
Input Voltage High	V_{IH}	2.0	-	-	V	
Input Voltage Low	V_{IL}	-	-	0.8		
Power Ready	PRDY					
Logic Level High	V_{OH}	4.5	4.6	-	V	V_{DD}=4.6V, I_{Load}=10mA
Logic Level Low	V_{OL}	-	0.1	0.2		V_{DD}=UVLO Threshold, I_{Load}=10µA
Drive Input	DRV_IN					
Logic Level High	V_{OH}	2.0	-	-	V	
Logic Level Low	V_{OL}	-	-	0.8		

① Measurement were made using four 10uF (TDK C3225X7R1C106M or equiv.) capacitors across the input. See Figs. 1 & 3.

② Not associated with the rise and fall times. Does not affect Power Loss (see Fig 4).

Pin Description Table

Pin Name	Ball Designator	Pin Function
V_{DD}	A1 – A3, B1 – B3	Supply voltage for the internal circuitry.
V_{IN}	A5 – A12, B5 – B12, C5 - C10	Input voltage for the DC-DC converter.
PGND	C11, C12, D11, D12, E11, E12, F6, F7, F12, G6, G7, G12, H6, H7, H12, J6, J7, J12, K5 – K7, K12, L5, L6, L12, M5 – M7, M12	Power ground - Connection to the ground of bulk and filter capacitors.
V_{SW}	D5 – D10, E5 – E10, F8 – F11, G8 – G11, H8 – H11, J8 – J11, K8 – K11, L8 – L11, M8 – M11	Switching node - Connection to the output inductor.
SGND	C1 – C3, D1 –D3, E1 –E3	Signal Ground.
ENABLE	F1	When set to logic level high, internal circuitry of the device is enabled. When set to logic level low, the PRDY pin is forced low, the internal circuitry is disabled and the supply current is less than 10µA.
PRDY	K1	Power Ready - This pin indicates the status of V_{DD}. When V_{DD} is less than 4.4V(typ.), this output is driven low. When V_{DD} is greater than 4.4V(typ.), this output is driven high. This output has a 10mA source and 10µA sink capability.
PWM	H1	TTL-level input signal to MOSFET drivers.
NC	B4, C4, D4, E4, F2 – F4, G2 – G4, H2 – H4, J1, J2 – J4, K3, L1, L2, M1 – M4	This pin is not for electrical connection. It should be attached only to dead copper for thermal conductive routing.

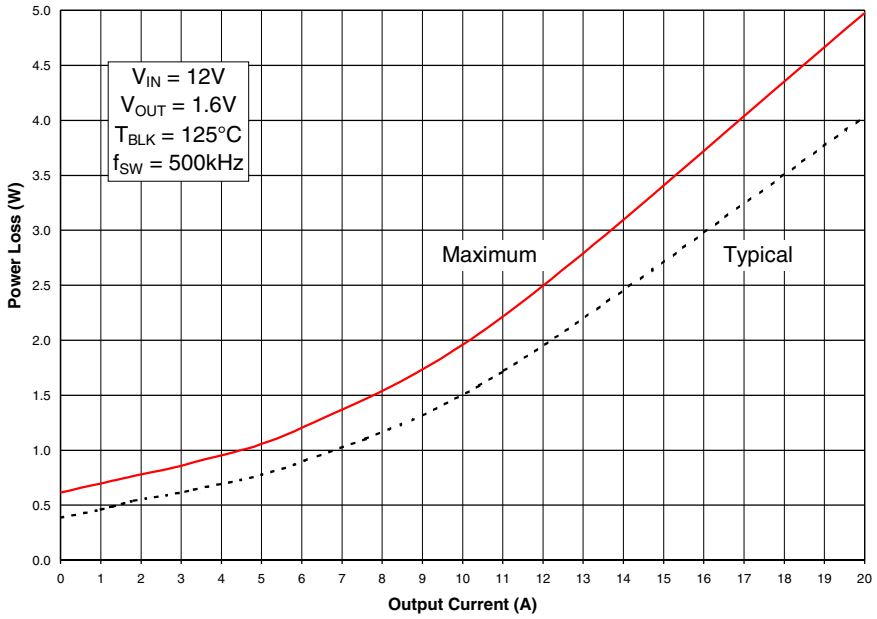


Fig 1. Power Loss vs. Current

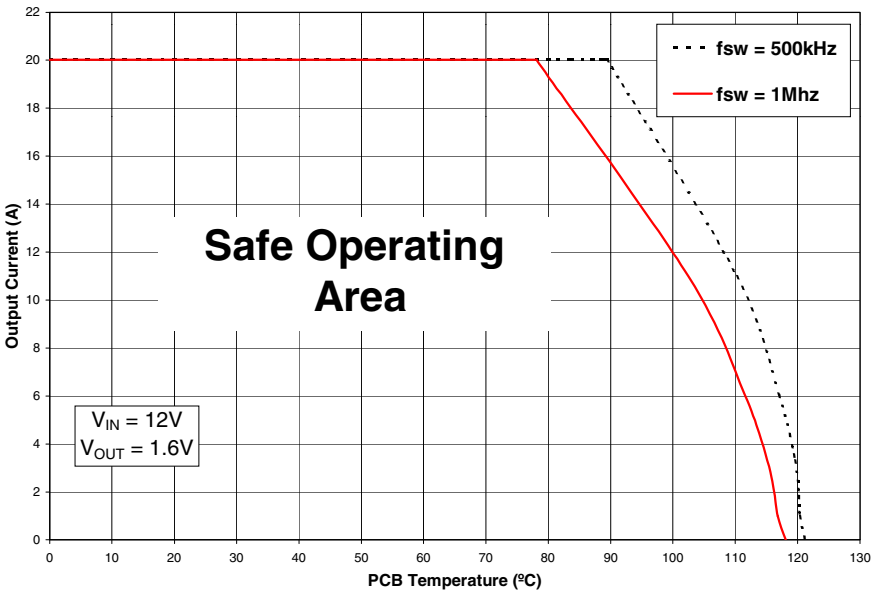


Fig 2. Safe Operating Area (SOA) vs. T_{PCB}

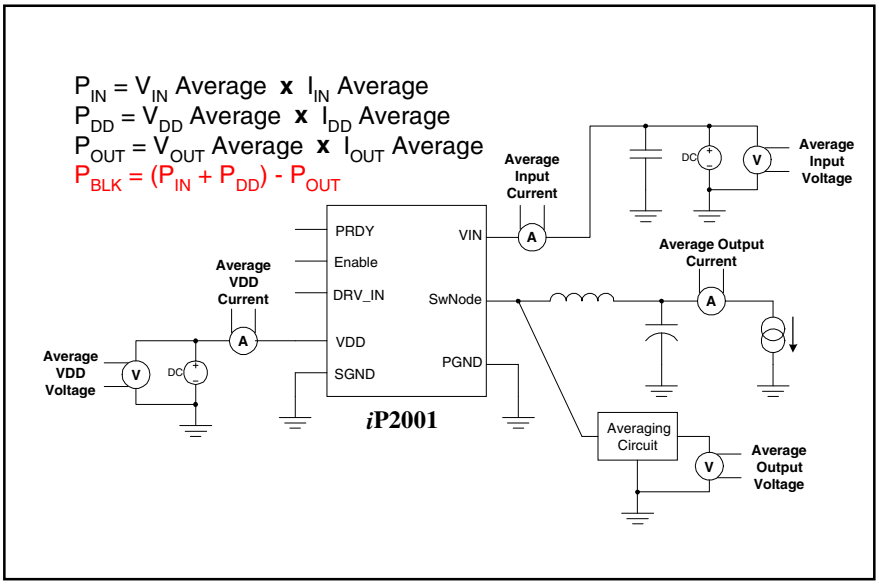


Fig 3. Power Loss Test Circuit

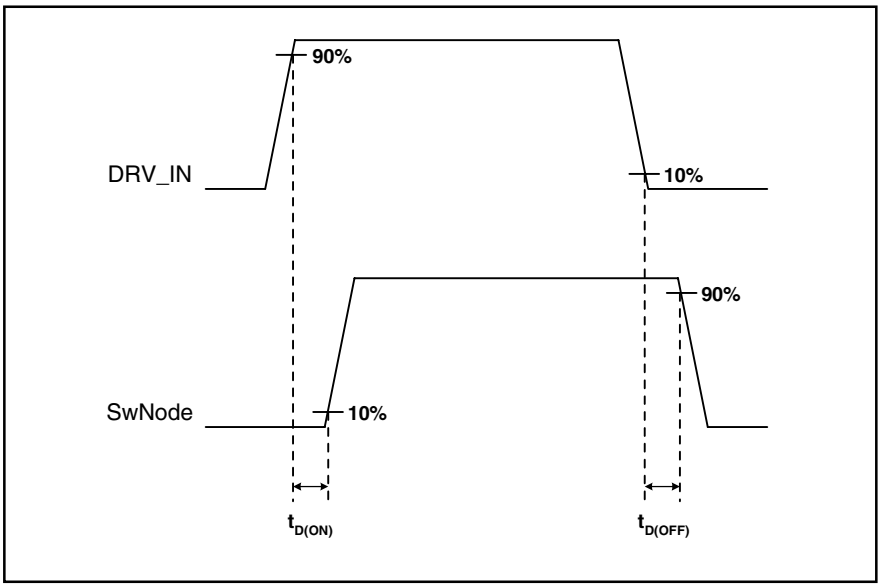
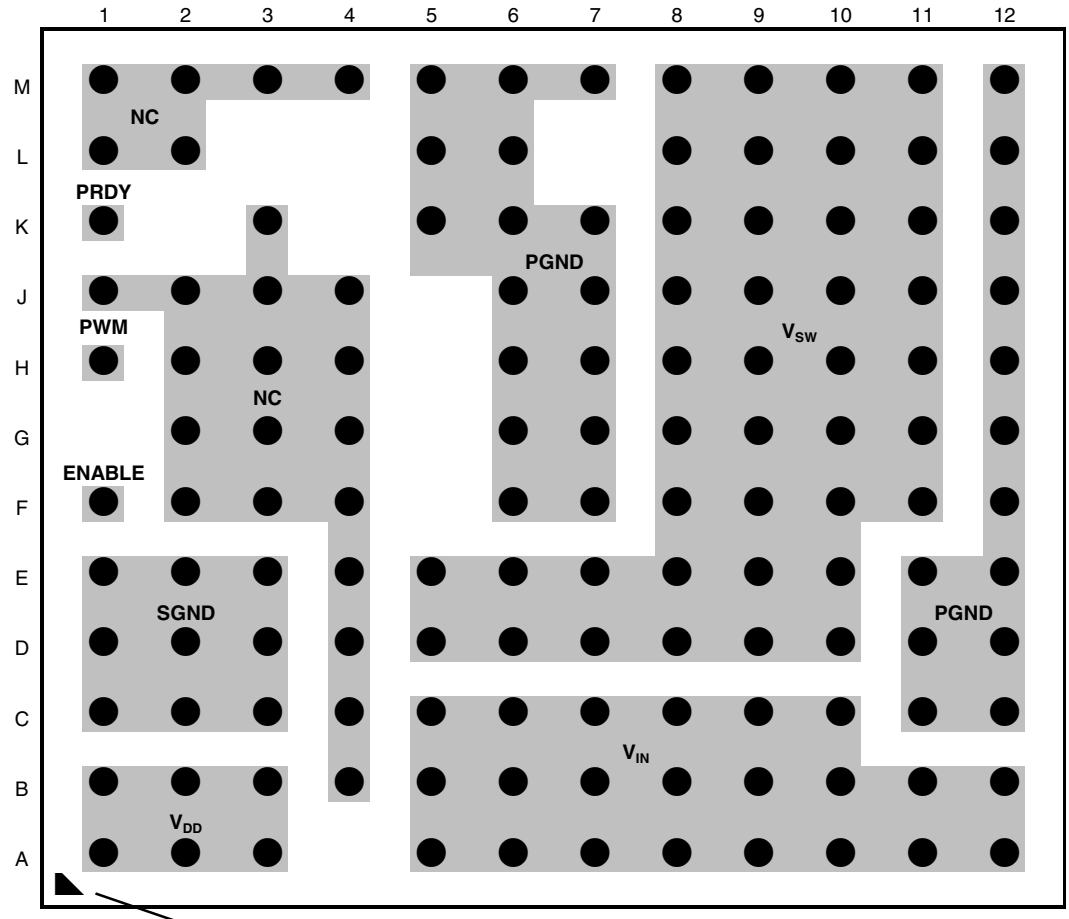
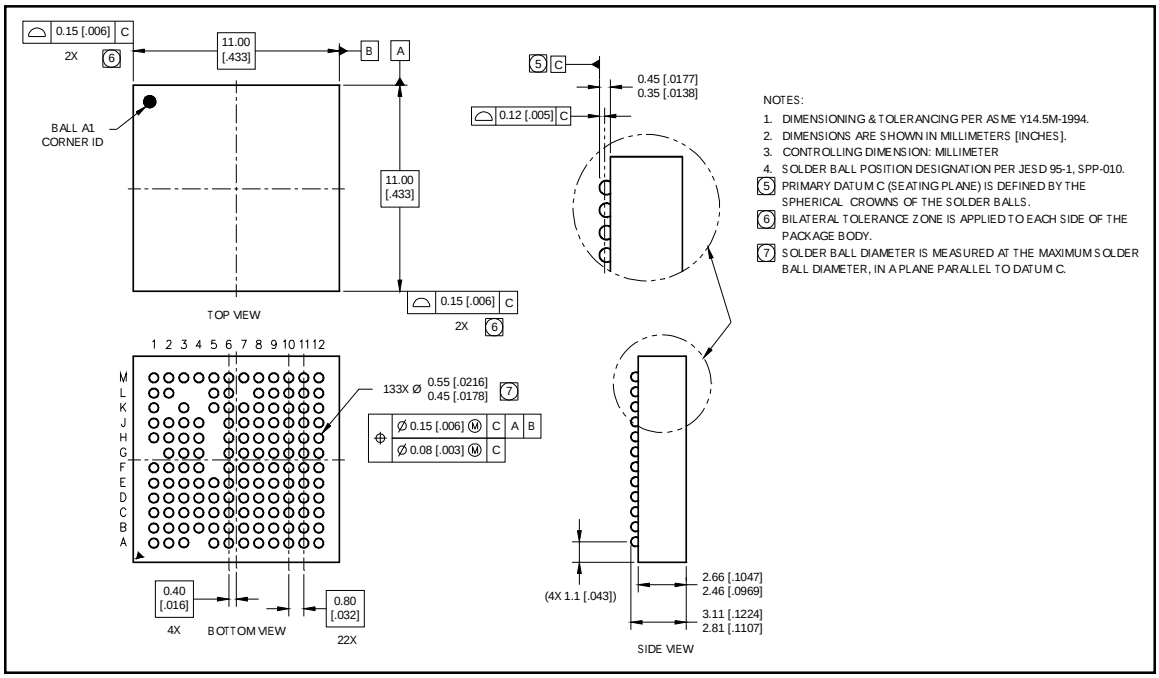


Fig 4. Timing Diagram


1
2
3
4
5
6
7
8
9
10
11
12
M
L
K
J
H
G
F
E
D
C
B
A
NC
PRDY
PWM
NC
ENABLE
SGND
PGND
V_{SW}
PGND
V_{IN}
V_{DD}
Ball A1 identifier as seen from bottom of package
Bottom View

Pin Diagram



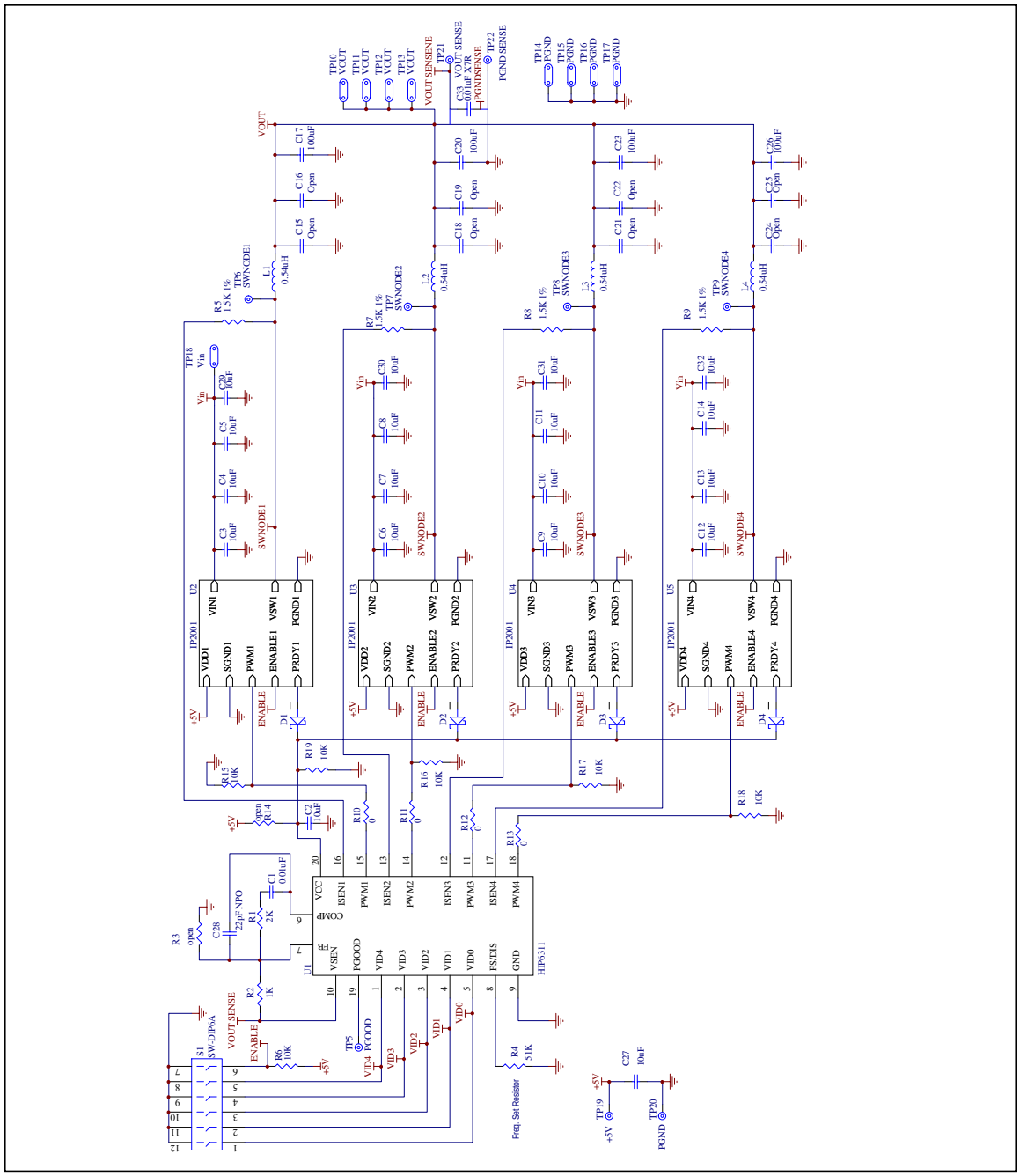
Mechanical Drawing

Refer to the following application notes for detailed guidelines and suggestions when implementing iP0WIR Technology products:

AN-1028: Recommended Design, Integration and Rework Guidelines for International Rectifier's iPOWIR Technology BGA Packages
This paper discusses the assembly considerations that need to be taken when mounting iPOWIR BGA's on printed circuit boards. This includes soldering, pick and place, reflow, inspection, cleaning and reworking recommendations.

AN-1029: Optimizing a PCB Layout for an iPOWIR Technology Design
This paper describes how to optimize the PCB layout design for both thermal and electrical performance. This includes placement, routing, and via interconnect suggestions.

AN-1030: Applying iPOWIR products in your thermal environment
This paper explains how to use the Power Loss and SOA curves in the data sheet to validate if the operating conditions and thermal environment are within the Safe Operating Area of the iPOWIR product.



4-Phase Reference Design Schematic

Designator	Value 1	Value 2	Type	Tolerance	Package	Mfr. 1	Mfr. 1 Part No.	Mfr. 2	Mfr. 2 Part No.
C1	0.01uF	50V	X7R	10%	0805	TDK	C2012X7R1H103KT	SAMSUNG	CL21B103KBNC
C2 - C14	10uF	16V	X5R	10%	1210	TDK	C3225X5R1C106KT	Murata	GRM42-2 X5R 106K16
C15	-	-	-	-	-	-	-	-	-
C16	-	-	-	-	-	-	-	-	-
C17	100uF	6.3V	X5R	10%	2220	TDK	C5750X5R0J107KT	MuRata	GRM44-1-X5R 107K 6.3
C18	-	-	-	-	-	-	-	-	-
C19	-	-	-	-	-	-	-	-	-
C20	100uF	6.3V	X5R	10%	2220	TDK	C5750X5R0J107KT	MuRata	GRM44-1-X5R 107K 6.3
C21	-	-	-	-	-	-	-	-	-
C22	-	-	-	-	-	-	-	-	-
C23	100uF	6.3V	X5R	10%	2220	TDK	C5750X5R0J107KT	MuRata	GRM44-1-X5R 107K 6.3
C24	-	-	-	-	-	-	-	-	-
C25	-	-	-	-	-	-	-	-	-
C26	100uF	6.3V	X5R	10%	2220	TDK	C5750X5R0J107KT	MuRata	GRM44-1-X5R 107K 6.3
C27	10uF	16V	X5R	10%	1210	TDK	C3225X5R1C106KT	Murata	GRM42-2 X5R 106K16
C28	22pF	50V	NPO	5%	0805	TDK	C2012X7R1H220JT	ROHM	MCH215A220JK
C29 - C32	10uF	16V	X5R	10%	1210	TDK	C3225X5R1C106KT	Murata	GRM42-2 X5R 106K16
C33	0.01uF	50V	X7R	10%	0805	TDK	C2012X7R1H103KT	SAMSUNG	CL21B103KBNC
D1 - D4	30V	100mA	schottky	-	SOT23	Central	CMPSH-3	-	-
L1 - L4	0.54uH	27A	ferrite	20%	SMT	Panasonic	ETQP6F0R6BFA	Bi Technologie	HM73-30R60
R1	2K	1/8W	thick film	5%	0805	ROHM	MCR10EZHJ202	-	-
R2	1K	1/8W	thick film	5%	0805	ROHM	MCR10EZHJ102	-	-
R3	-	-	-	-	-	-	-	-	-
R4	51K	1/8W	thick film	5%	0805	ROHM	MCR10EZHJW513	-	-
R5	1.5K	1/8W	thick film	1%	0805	ROHM	MCR10EZHF1501	KOA	RK73H2A1501F
R6	10K	1/8W	thick film	5%	0805	ROHM	MCR10EZHJ103	-	-
R7 - R9	1.5K	1/8W	thick film	1%	0805	ROHM	MCR10EZHF1501	KOA	RK73H2A1501F
R10 - R13	0	1/8W	thick film	<50mΩ	0805	ROHM	MCR10EZHJ000	-	-
R14	-	-	-	-	-	-	-	-	-
R15 - R19	10K	1/8W	thick film	5%	0805	ROHM	MCR10EZHJ103	-	-
U1	4.6-6 V	0-1.850V	PWM IC	0 - 70øC	20 Ld SOIC	Intersil	HIP6311CB	-	-
U2 - U5	-	-	-	-	11x11x3mm	IR	iP2001	-	-

4-Phase Reference Design Bill of Materials