International
IOR Rectifier

PD - 94336

iP1001

PRELIMINARY DATASHEET

iPOWIR™ TECHNOLOGY

Full Function Synchronous Buck Power Block

Integrated Power Semiconductors, Control IC & Passives

Features

- 5V to 12V input voltage①
- 20A maximum load capacity.
- 5 bit DAC settable, 0.925V to 2V output voltage range ②
- Configurable down to 2.5Vin & up to 3.3Vout with simple external circuit ③.
- +/-1% output voltage accuracy.
- 200kHz & 300kHz switching frequency selectable
- Remote output voltage and ground sense.
- Optimized for very low power losses & 100% production tested.
- Over & undervoltage protection.
- Adjustable lossless current limit ④.
- Internal features minimize layout sensitivity *
- Very small outline 14mm x 14mm x 3mm

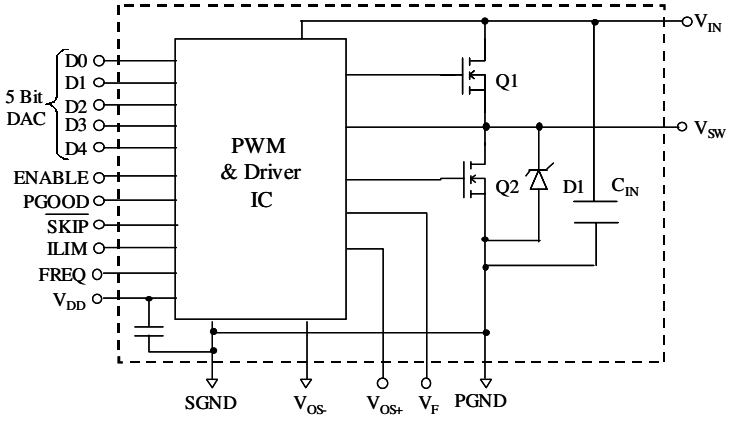
iP1001 Power Block

Description

The iP1001 is a fully optimized solution for high current synchronous buck applications, requiring up to 20A. The iP1001 is optimized for single-phase applications, and includes a full function fast transient response constant-on-time PWM control IC, with an optimized power semiconductor chip-set and associated passives, achieving benchmark power density. Very few external components are required, including output inductor, input & output capacitors. Further range of operation down to 2.5Vin can be achieved with the addition of a simple external boost circuit, and operation up to 3.3Vout can be achieved with a simple external voltage divider.

iPOWIR technology offers designers an innovative board space saving solution for applications requiring highest power density. iPOWIR technology eases design for applications where component integration offers benefits in performance and functionality. iPOWIR technology solutions are also optimized internally for layout, heat transfer and component selection.

iP1001 Internal Block Diagram



* All of the difficult PCB layout and bypassing issues have been addressed with the internal design of the iPOWIR block. There are no concerns about unwanted shutdown or other malfunctions which often occur in switching power supplies. The iPOWIR block will function normally without any additional input power supply bypass capacitors. However, for stable and reliable long term operation it is recommended that the adequate amount of input decoupling is provided on the V_{IN} pin. No additional bypassing is required on the V_{DD} pin.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units	Conditions
V_{IN} to PGND		-0.3	-	16.0	V	
V_{DD} to PGND		-0.3	-	6.0		
$\overline{SKIP}$ to PGND		-0.3	-	V_{DD}+0.3		
V_{OS+}		-0.3	-	V_{DD}+0.3		
V_F		-0.3	-	V_{DD}+0.3		
D0-D4		-0.3	-	V_{DD}+0.3		
PGOOD to PGND		-0.3	-	V_{DD}+0.3		
ENABLE to PGND		-0.3	-	V_{DD}+0.3		
ILIM		-0.3	-	V_{DD}+0.3		
FREQ		-0.3	-	V_{DD}+0.3		
V_{SW} output current		-	-	TBD	A	
Block Temperature	T_{BLK}	-	-	125	°C	Capable of -40°C start-up
Storage Temperature	T_{STG}	-40	-	125		

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{DD}	4.5	-	5.5	V	
Input Voltage Range①	V_{IN}	5.0	-	12.0		
Output Current from V_{SW}⑥	$Iout_{vsw}$	-	-	20	A	$5V_{IN}$-$12V_{IN}$ & ≤ $2V_{OUT}$
		-	-	12		$3.3V_{IN}$ / $2.5V_{OUT}$ / 200kHz
Output Voltage Range②	Vout	0.925	-	2.0	V	DAC Setting See VID table②
Operating Temperature	T_{PCB}	0	-	90	°C	No derating see SOA fig 2

Electrical Specifications @ V_{DD} = 5V (Unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Power Loss ④	P_{LOSS}	-	3.1	3.7	W	300kHz, $12V_{IN}$, 20A, $1.3V_{OUT}$
Overcurrent Shutdown		-	25	-	A	300kHz, $12V_{IN}$, $1.3V_{OUT}$
Soft-Start Time		-	1.7	-	ms	ON to I_{LIMIT}
On-Time	T_{ON}	-	350	-	ns	300kHz, $12V_{IN}$, 20A, $1.3V_{OUT}$
Current Limit Setting	ILIM	See ILIM curve⑤				
Output Voltage Accuracy		-1.0	-	1.0	%	$4.5V_{IN}$ to $12V_{IN}$
V_{DD} Undervoltage Lockout		4.1	-	4.4	V	

Electrical Specifications (continued) @ V_{DD} = 5V (Unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Output Undervoltage Shutdown Threshold		0.75	-	0.85	V	unloaded output @ V_F sense pin
Output Overvoltage Shutdown Threshold		2.2	-	2.3	V	unloaded output @ V_F sense pin
PGOOD Trip Threshold	PGOOD	V_{DAC}-8%	-	V_{DAC}-3%	V	V_{OS+} output unloaded
PGOOD Leakage Current		-	-	1	uA	@5V
PGOOD Output Low Voltage		-	-	0.4	V	I_{sink} = 1mA
Logic Input High Voltage		2.4	-	-	V	D0-D4, $\overline{SKIP}$, ENABLE
Logic Input Low Voltage		-	-	0.8	V	
V_{DD} Quiescent Current	I_{QVDD}	-	-	15	uA	Shutdown mode
V_{IN} Quiescent Current	I_{QVIN}	-	-	1	mA	ENABLE Low V_{IN} = 12V

Notes :

① Can be modified to operate down to 2.5V_{IN}. See reference design for details.

② Can be modified to operate up to 3.3V_{OUT}, outside of DAC settable range. See reference design for details.

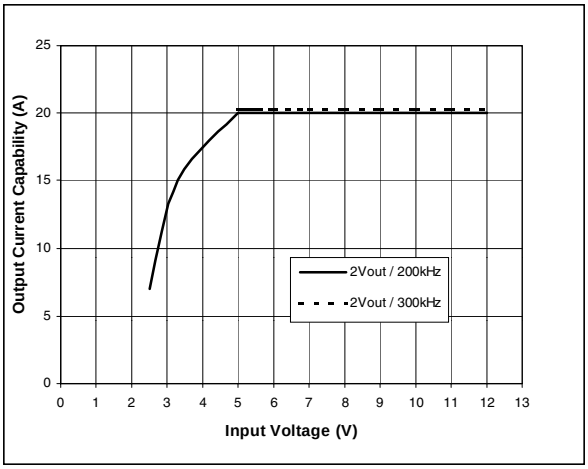
③ Only buck configurations allowed, ie $V_{IN} \geq 1.25V_{OUT}$.

④ See figures 1 & 3.

⑤ See reference design for ILIM R7 resistor setting details.

⑥ See curve for output current rating versus input voltage.

Output Current Capability versus Input Voltage



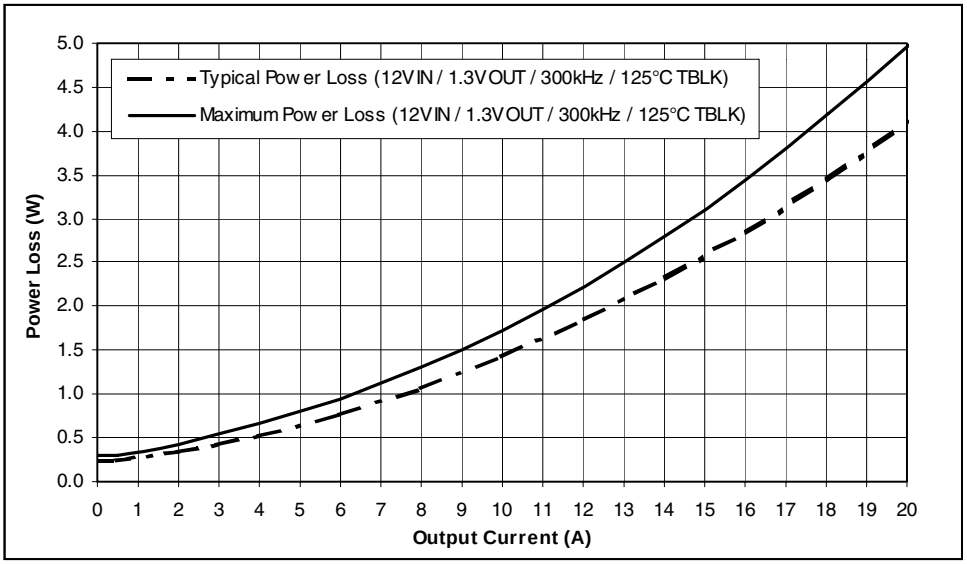


Fig 1. Maximum & Typical Power Loss vs. Output Current

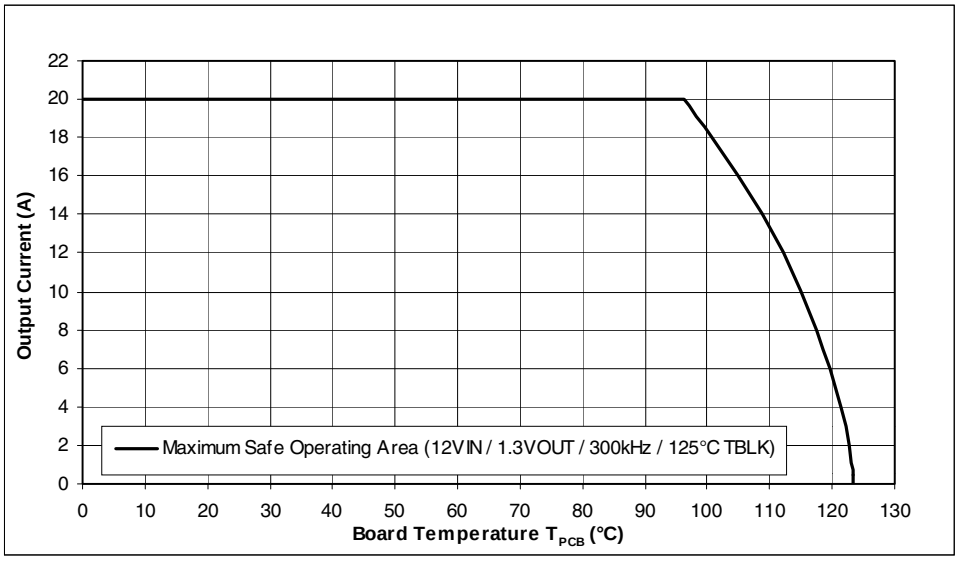


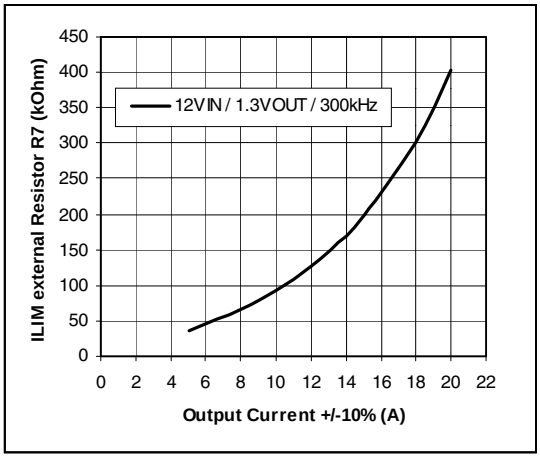
Fig 2. Maximum Safe Operating Area (Output Current vs T_{PCB})

VID Code Table②

D4	D3	D2	D1	D0	OUTPUT VOLTAGE(V)
0	0	0	0	0	2.00
0	0	0	0	1	1.95
0	0	0	1	0	1.90
0	0	0	1	1	1.85
0	0	1	0	0	1.80
0	0	1	0	1	1.75
0	0	1	1	0	1.70
0	0	1	1	1	1.65
0	1	0	0	0	1.60
0	1	0	0	1	1.55
0	1	0	1	0	1.50
0	1	0	1	1	1.45
0	1	1	0	0	1.40
0	1	1	0	1	1.35
0	1	1	1	0	1.30
0	1	1	1	1	Shutdown*
1	0	0	0	0	1.275
1	0	0	0	1	1.250
1	0	0	1	0	1.225
1	0	0	1	1	1.200
1	0	1	0	0	1.175
1	0	1	0	1	1.150
1	0	1	1	0	1.125
1	0	1	1	1	1.100
1	1	0	0	0	1.075
1	1	0	0	1	1.050
1	1	0	1	0	1.025
1	1	0	1	1	1.000
1	1	1	0	0	0.975
1	1	1	0	1	0.950
1	1	1	1	0	0.925
1	1	1	1	1	Shutdown*

* Shutdown : Upon receipt of the shutdown code (per VID code table above), both FETs are turned OFF and the output is discharged as it enters UVP fault mode.

ILIM setting vaules for R7 resistor④ (select nearest 1% value)



Pin Description

Pin Name	Ball Designator	Pin Description
V_{IN}	A9-A12, B9-B12, C9-C14, D9-D14, E9-E16, F9-F16, G9-G16	Input voltage (battery or AC adapter) connection node.
	A13-A15, B13-B16, C15-C16, D15-D16	Thermal connections only, but recommended that these balls be connected to V_{IN}.
V_{SW}	H9-H14, J11-J14, K11-K14, L11-L14, N11-N14, M11-M14, P11-P14, R11-R14, S11-S14	Output inductor connection node.
PGND	H15-H16, J15-J16, K9-K10, K15-K16, L9-L10, L15-L16, M9-M10, M15-M16, N9-N10, N15-N16, P9-P10, P15-P16, R9-R10, R15-R16, S9-S10, S15-S16	Power ground.
	J6-J8, K6-K8, L6-L8, M6-M8, N7-N8, P7-P8, R6-R8, S6-S8	Thermal connection only, but recommended that these balls be connected to PGND.
V_{DD}	R4-R5, S4-S5	Low side gate driver supply voltage.
SGND	A2-A3, B2-B3	Signal ground.
V_{OS-}	E1	Remote sense ground. To be connected to ground at the load.
ENABLE	R3, S3	Commands output ON or OFF. Active floating (internally pulled high). When logic low, the synchronous FET gate is forced high.
$\overline{SKIP}$	R2, S2	Enables pulse skipping when low. Forced PWM when floating (internally pulled high).
PGOOD	R1, S1	Output of PGOOD is an open drain output.
V_F	C1-C2	Output voltage feedback sense connected at the output bulk capacitors.
V_{OS+}	D1-D2	Output voltage remote sense feedback signal connected at the load.
D0	P1-P2	VID code setting D/A inputs. Internally pulled high.
D1	N1-N2	
D2	M1-M2	
D3	L1-L2	
D4	K1-K2	
ILIM	A5, B5, C5	Current limit threshold setting pin. See ILIM curve for R7 external resistor values.
FREQ	A4, B4	Switching frequency selector pin. Floating selects 300kHz, tied to V_{DD} selects 200kHz.
Heatsink	A1, A6-A7, B1, B6-B7, C3, C6-C7, D3-D4, D6, E3-E6, F1-F5, G1-G5, H1-H5, J1-J2, N4-N5, P4-P5	For heatsink purposes only.

Pin-out Diagram - Bottom View (Not to scale)

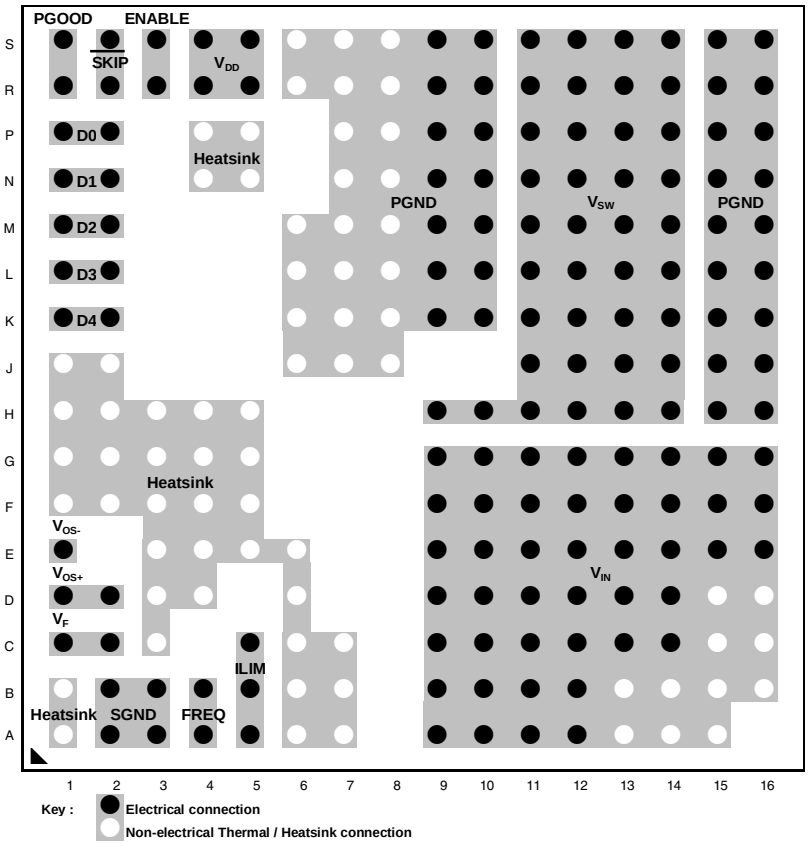
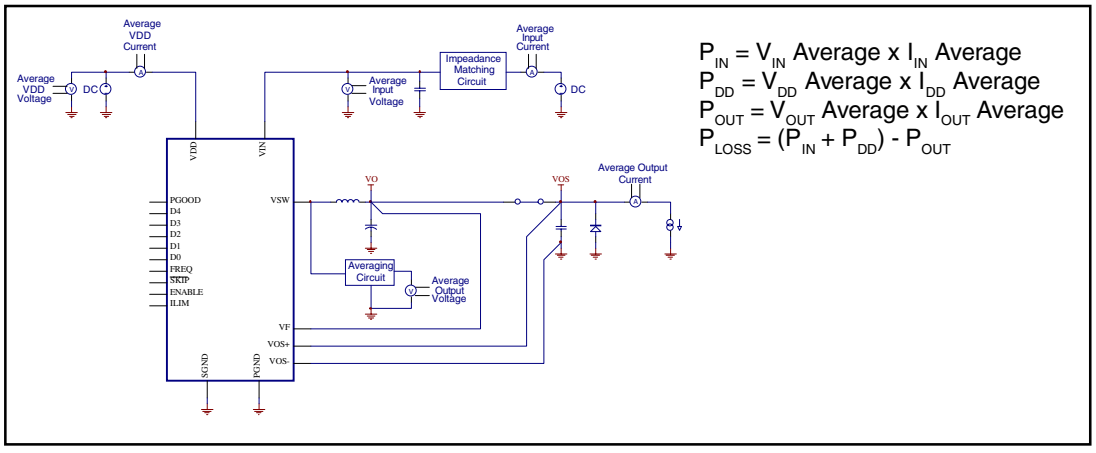


Fig. 3 - Power Loss Test Circuit



$P_{IN} = V_{IN}$ Average x I_{IN} Average
$P_{DD} = V_{DD}$ Average x I_{DD} Average
$P_{OUT} = V_{OUT}$ Average x I_{OUT} Average
$P_{LOSS} = (P_{IN} + P_{DD}) - P_{OUT}$

iP1001 Reference Design

The schematics in Fig.4a & 4b and complete Bill of Materials in Table 1 are provided as a reference design to enable a preliminary evaluation of iP1001. They represent a simple method of applying the iP1001 solution in a synchronous buck topology. Fig. 4a shows the implementation in $<5V_{IN}$ applications, and Fig. 4b shows the implementation in $5V_{IN}$ - $12V_{IN}$ applications. The connector pins are the solder balls on the bottom layer of the package. With the addition of L1 inductor and the output capacitors C11-C14, a total power supply solution is presented. Input capacitors C1-C10 are for bypassing in the $5V_{IN}$ - $12V_{IN}$ application, but only C1-C3 are required for $<5V_{IN}$ applications. SW1 is a dip switch that programs the output voltage (switches 1-5). Use the VID table provided in this datasheet to set the output voltage to the desired setting. Resistors R3 & R4 need to be removed for operation at standard VID levels. Switch 8 (ENABLE) enables the output when pulled high. 5 volt control power should be applied prior to applying V_{IN}, and ENABLE should start the sequence in a low state. Switch 7 ($\overline{SKIP}$) is enabled by pulling the pin low, and provides higher efficiency at light load conditions by forcing a skip mode of operation.

The 5Volt V_{DD} power terminal and input power terminals are provided as separate inputs. They can be connected if the application requires only 5V input operation.

The iP1001 employs a constant-on-time PWM control IC centered around a fixed frequency (200kHz or 300kHz). The actual switching frequency varies as a function of the output voltage, input voltage and inductor current. The inductor current ripple information is obtained from the ESR of the output capacitors and the output voltage ripple developed across the filter capacitors provides the PWM ramp signal. Adhere to the recommended reference design component selection to provide stable power supply operation.

The design offers a higher output voltage programmability feature for 2.5V & 3.3V outputs. For output voltages above 2Vout, the DAC setting must be set to 2Vout, and then by selecting resistors R3 & R4 as per the formula below in Equation 1, other output voltages can be derived. Tighter regulation can be achieved by using resistors with better than 1% tolerance. 3.3Vout (+/- 3%) is the maximum output voltage allowed, and for all output voltages higher than 2Vout, a 12A maximum load current is allowed. Note that as the Vout increases with respect to the input, the switching frequency increases, due to the constant on-time control method. For Vin < 5Vin and Vout > 2Vout, the frequency select pin (FREQ) needs to be set to 200kHz, or connected to V_{DD}. For applications with Vin < 5Vin and where there is no auxiliary $5V_{DD}$ available, connections JP2 and JP3 must be included to enable the boost circuit which will provide the $5V_{DD}$ necessary for the iP1001 internal logic to function. The boost circuit will convert 2.5Vin & 3.3Vin power to $5V_{DD}$, and will provide enough power to supply internal logic for up to 5 x iP1001 power blocks.

Equation 1 : $Vout = V_F \cdot \{1 + R3/R4\}$

where V_F is equal to the DAC setting

Fig. 4a - iP1001 reference design schematic for <5V$_{IN}$

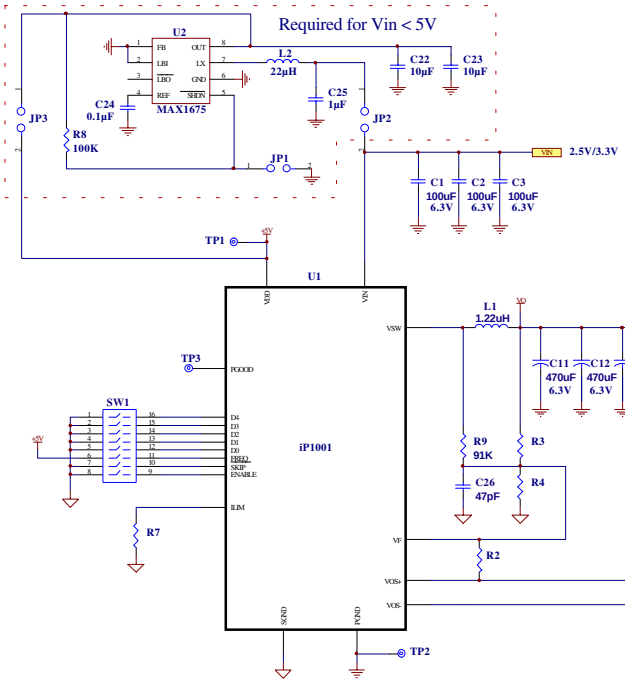


Fig. 4b - iP1001 reference design schematic for 5V$_{IN}$ - 12V$_{IN}$

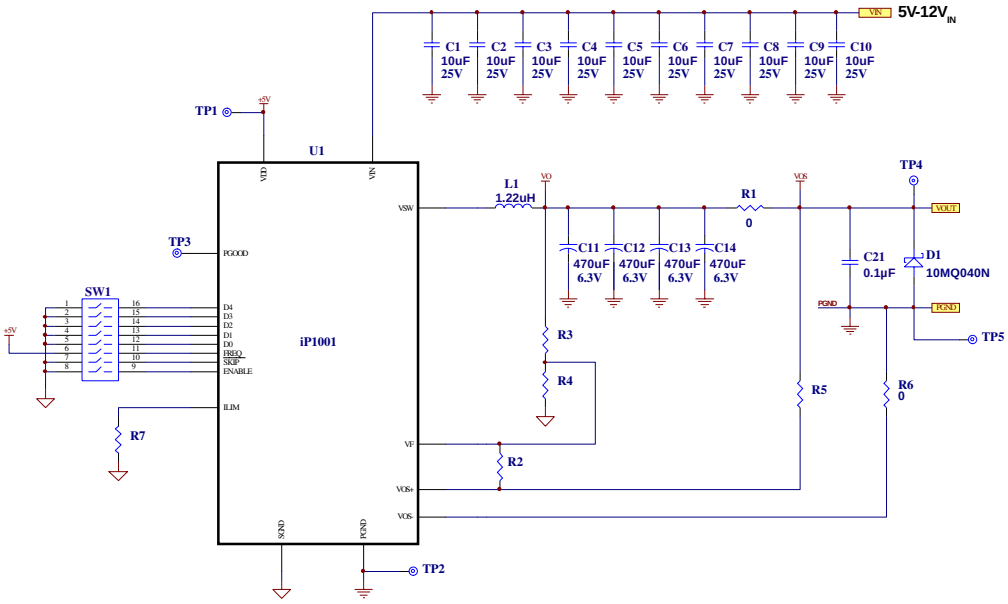


Table 1 - iP1001 reference design bill of materials

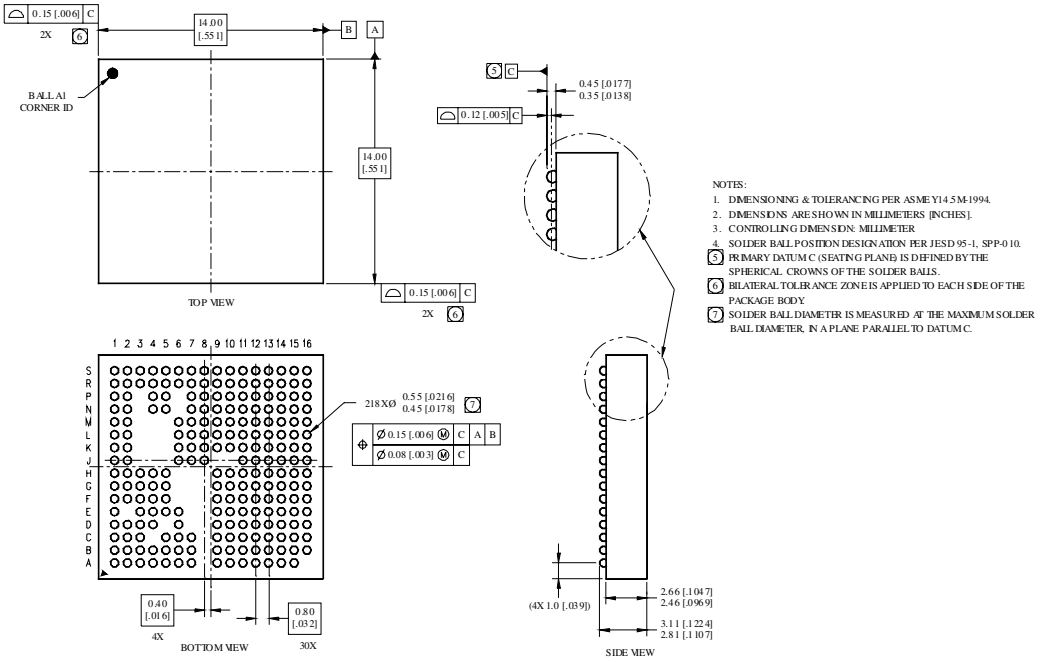
Required for high input voltages (Vin = 5-12V):

Designator	Value	Part Type	Footprint	Mfr.	Mfr. PN
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10	10uF	Capacitor, 25V, 20%	1812	TDK	C4532X7R1E106MT
C11, C12, C13, C14	470uF	Capacitor, 6.3V, 20%	7343	Sanyo	6TPB470M
C16	0.100uF	Capacitor, 50V, 10%	1206	Murata-Erie	GRM42-6X7R104K050A
C15, C22, C23, C24, C25, C26		Not installed			
D1		Diode, 75V, 200mA	SOD80C	Diodes Inc.	LL4148
L1	1.22uH	Inductor, 22A, 20%	SMT	Panasonic	ETQP2H1R2BFA
L2		Not installed			
R1	0	Resistor, 0ohm Jumper	SMT	Isotek Corp.	SMT-R000
R2		For <2Vout, Not installed For >2Vout, Resistor, 0ohm Jumper			
R3		Install for >2Vout, see formula for values			
R4		Install for >2Vout, see formula for values			
R5		For <2Vout, Resistor, 0ohm Jumper For >2Vout, Not installed			
R6	0	Resistor, 0ohm Jumper	1206	Rohm	MCR18EZHJ000
R7		See ILIM curves for values			
R8, R9		Not installed			
SW1		Switch, 8 positon, SPDT	SMT	C&K Components	SD08H0SK
U1		Power Block	SSBGA14x14mm	International Rectifier	iP1001
U2		Not installed			

Required for low input voltage (Vin < 5V):

Designator	Value	Part Type	Footprint	Mfr.	Mfr. PN
C1, C2, C3	100uF	Capacitor, 6.3V, 20%	1812	TDK	C4532X5R0J107MT
C4, C5, C6, C7, C8, C9, C10		Not installed			
C11, C12, C13	470uF	Capacitor, 6.3V, 20%	7343	Sanyo	6TPB470M
C22, C23	10uF	Capacitor, 16V, 20%	1210	Murata-Erie	GRM42-2X5R106K016A
C21, C24	0.100uF	Capacitor, 50V, 10%	1206	Murata-Erie	GRM42-6X7R104K050A
C25	1uF	Capacitor, 10V, 10%	805	Murata-Erie	GRM40X7R105K010A
C26	47pF	Capacitor, 50V, 10%	1206	Murata-Erie	GRM42-6C0G470J050A
D1		Diode, 75V, 200mA	SOD80C	Diodes Inc.	LL4148
L1	1.22uH	Inductor, 22A, 20%	SMT	Panasonic	ETQP2H1R2BFA
L2	22uH	Inductor, 0.68A, 20%	SMT	Sumida	CR43-220
R1	0	Resistor, 0ohm Jumper	SMT	Isotek Corp.	SMT-R000
R2		For <2Vout, Not installed For >2Vout, Resistor, 0ohm Jumper			
R3		Install for >2Vout, see formula for values			
R4		Install for >2Vout, see formula for values			
R5		For <2Vout, Resistor, 0ohm Jumper For >2Vout, Not installed			
R6	0	Resistor, 0ohm Jumper	1206	Rohm	MCR18EZHJ000
R7		See ILIM curve for values			
R8	100K	Resistor, 5%	1206	ROHM	MCR18J104
R9	91K	Resistor, 5%	1206	Rohm	MCR18J913
SW1		Switch, 8 positon, SPDT	SMT	C&K Components	SD08H0SK
U1		Power Block	SSBGA14x14mm	International Rectifier	iP1001
U2		IC, Step-Up DC to DC Converter, 0.5A	8uMAX	Maxim	MAX1675EUAT

iP1001 Mechanical Drawing



Refer to the following application notes for detailed guidelines and suggestions when implementing iP0WIR Technology products:

AN-1028: Recommended Design, Integration and Rework Guidelines for International Rectifier's iPOWIR Technology BGA Packages
This paper discusses the assembly considerations that need to be taken when mounting iPOWIR BGA's on printed circuit boards. This includes soldering, pick and place, reflow, inspection, cleaning and reworking recommendations.

AN-1029: Optimizing a PCB Layout for an iPOWIR Technology Design
This paper describes how to optimize the PCB layout design for both thermal and electrical performance. This includes placement, routing, and via interconnect suggestions.

AN-1030: Applying iPOWIR products in your thermal environment
This paper explains how to use the Power Loss and SOA curves in the data sheet to validate if the operating conditions and thermal environment are within the Safe Operating Area of the iPOWIR product.