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CDV/DT INDUCED TURN-ON IN SYNCHRONOUS BUCK REGULATORS

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Abstract

Cdv/dt induced turn-on of the synchronous MOSFET deteriorates performance in synchronous buck regulators. We will discuss this problem and provide several solutions that can reduce the effects.

SYNCHRONOUS BUCK REGULATOR

Synchronous buck topology is becoming popular in powering ultra-fast CPU cores. A standard buck circuit is shown in Figure 1(a) and a synchronous buck is shown in Figure 1(b). As shown in Figure 1(b), by replacing the freewheeling diode with a MOSFET, the standard buck regulator is converted into a synchronous buck topology. This topology will provide higher efficiency than the standard buck circuit. Typically a Schottky diode is paralleled with MOSFET Q2 but is omitted from this paper because it is not required to understand and solve the Cdv/dt induced turn-on problem.

Ideal synchronous buck regulator waveforms are illustrated in Figure 2(a). The control MOSFET Q1 is used to regulate the output voltage by adjusting its duty factor. When Q1 is turned off, the inductor current of Lout continues to flow through either the synchronous MOSFET Q2 or its body diode.

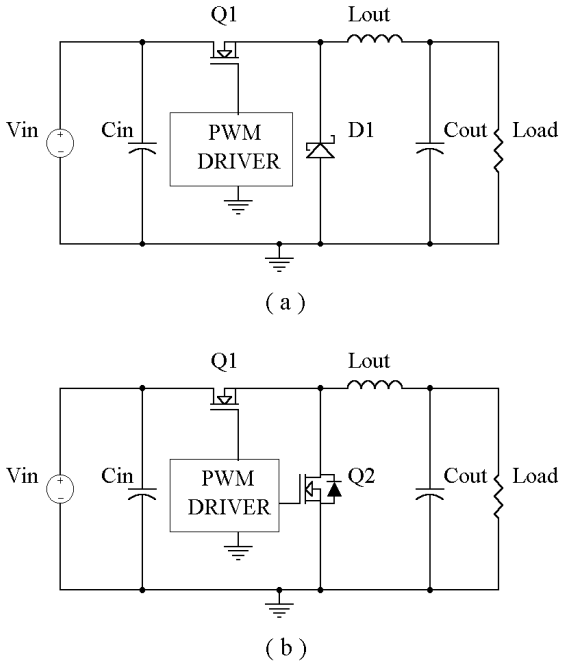

Figure 1. (a) Standard buck topology.
(b) Synchronous buck topology.

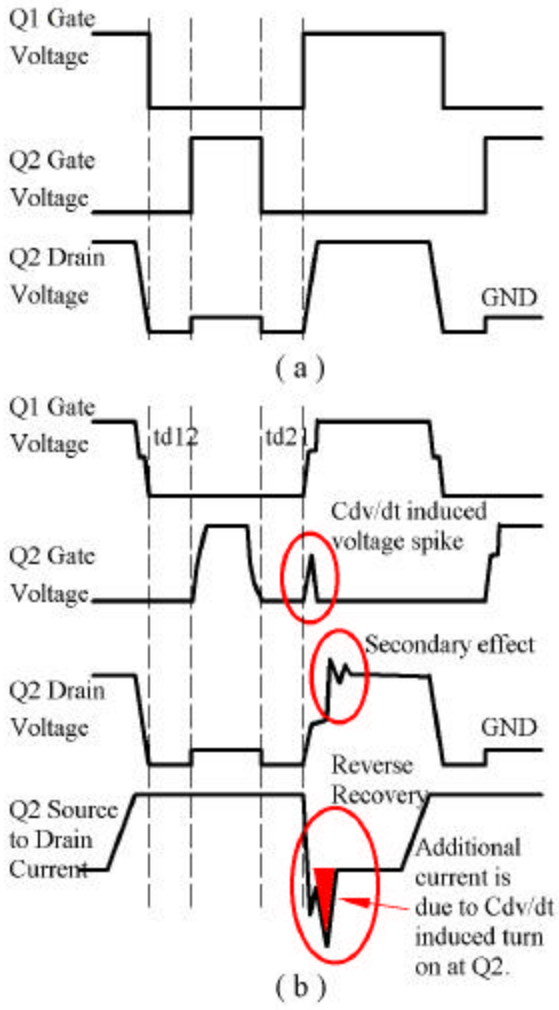

Figure 2. (a) Ideal waveforms in a synchronous buck voltage regulator; (b) waveforms due to Cdv/dt induced turn-on at Q2.

Dead-times, td12 and td21 as shown in Figure 2(a) are introduced to prevent the cross conduction that would occur if Q1 and Q2 gate drive signals were overlapped. During the dead time, only the body diode of Q2 conducts and the drain voltage of Q2 is clamped to minus one diode

drop. MOSFET Q2 is zero-voltage-switching on and off because of the conduction on its body diode. The synchronous MOSFET Q2 then takes over the inductor current, which results in less voltage drop compared to that of schottky diodes in a standard buck topology. Body diode of Q2 conducts during dead-time td21; thus creating stored charge that must be removed before Q2 can support voltage. This Qrr reverse recovery charge causes power loss in MOSFET Q1. Adding an external Schottky diode to Q2 or simply replacing Q2 with a FETKY™ will boost the efficiency even higher [1].

Unfortunately, Cdv/dt induced voltage in the synchronous buck circuit might cause undesired turn-on of Q2 and deteriorate overall system efficiency. The Cdv/dt induced turn-on problem is caused by a fast changing voltage on the drain side of MOSFET Q2, which results from turning on the control MOSFET Q1, as shown in Figure 2(b). We will discuss this problem and provide several solutions that can be used to resolve Cdv/dt induced turn-on in synchronous buck topologies.

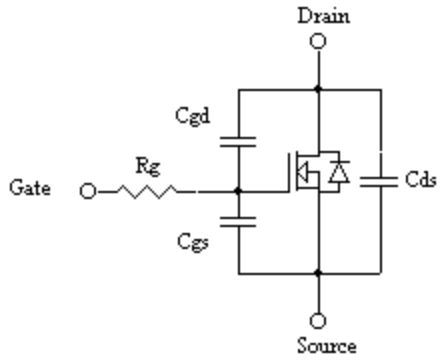

Figure 3. A simplified MOSFET model.

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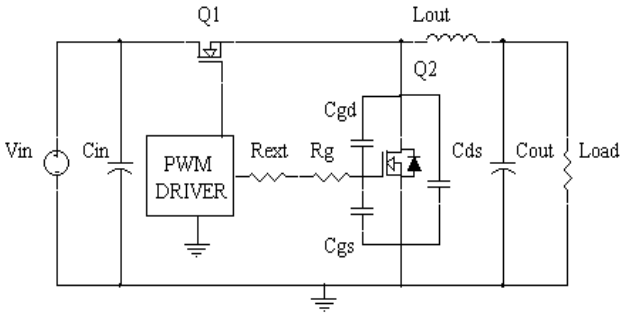

Figure 4. Detailed representation of Q2 in a synchronous buck regulator.

CDV/DT INDUCED TURN-ON

A simplified MOSFET model is introduced in Figure 3 to help describe the Cdv/dt induced turn-on problem. Rg is the internal gate resistance of the MOSFET while Cgs, Cgd, and Cds are the gate-to-source capacitance, the gate-to-drain miller capacitance, and the output capacitance, respectively. A detailed representation of Q2 in a synchronous buck regulator is illustrated in Figure 4.

During the turn on switching period of Q1, the full input voltage does not immediately appear at drain of Q2 because of the miller effect and turn-on delay at MOSFET Q1. The drain voltage imposed on Q2 induces a current that is coupled through its miller capacitance Cgd. This induced current generates a voltage drop across the internal gate resistance Rg of Q2 and the external gate resistance Rext, and charges the gate-to-source capacitance Cgs at Q2 gate. The amplitude of the induced gate voltage on Q2 is a function of dv/dt, Cgd, Cgs, and the total gate resistance. The gate drive circuit also plays an important role in Cdv/dt induced voltage, but this will be discussed in more detail later in this article.

If this induced gate voltage exceeds the threshold voltage of MOSFET Q2; it will be spuriously turned on while Q1 is on. As a result, a shoot-through current will flow from the input voltage bus to the circuit common through Q1 and Q2. MOSFET Q1 will then have to carry load and shoot-through currents while Q2 conducts excessive shoot-through current. Because of this, undesired power losses are then generated in both Q1 and Q2 leading to an increase in their junction temperature and overall decrease in power supply efficiency.

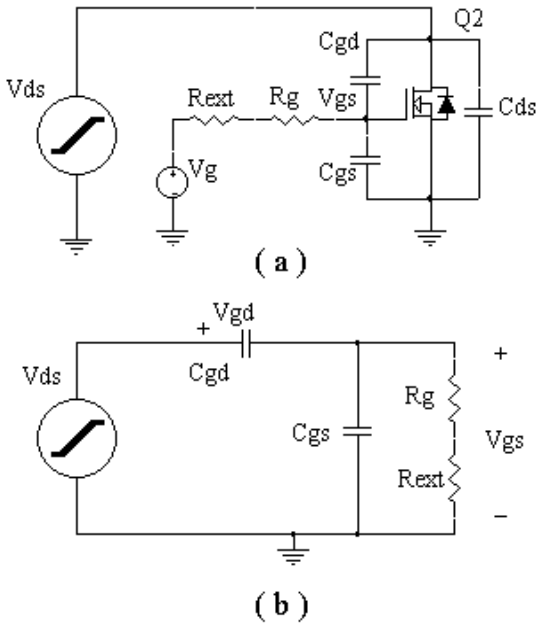

Figure 5. (a) Cdv/dt induced turn-on model circuit. (b) Equivalent circuit of (a).

Based on Figure 4, the Cdv/dt induced turn-on problem can be simulated as a periodic function of the trapezoidal voltage applied to the drain of Q2 when Q1 is turned on, as illustrated in Figure 5(a). The equivalent circuit of Figure 5(a) can also be depicted as in Figure 5(b). This equivalent circuit is valid only during the rising edge of the drain voltage in Q2. Another assumption for this equivalent circuit is that the gate drive circuit of Q2 can swing from zero to applied drive voltage, and that when Q2 is off the gate voltage will be zero.

Figure 5(b) is simply an R-C circuit. All of the node and loop equations in Figure 5(b) can be written as follows.

$$V_{ds} = V_{gd} + V_{gs}\,, \tag{1}$$

$$C_{gd}\frac{dV_{gd}}{dt} = C_{gs}\frac{dV_{gs}}{dt} + \frac{V_{gs}}{R_t}. \tag{2}$$

Resistance Rt is the sum of Rg and Rext. Also Vds, Vgd, and Vgs are drain voltage, drain-to-gate voltage, and gate-to-source voltage, respectively. Substituting Vgd from (1) into equation (2), we have

$$C_{gd}\frac{d(V_{ds} - V_{gs})}{dt} = C_{gs}\frac{dV_{gs}}{dt} + \frac{V_{gs}}{R_t}. \tag{3a}$$

$$C_{gd}\frac{dV_{ds}}{dt} = (C_{gs} + C_{gd})\frac{dV_{gs}}{dt} + \frac{V_{gs}}{R_t}. \tag{3b}$$

The drain voltage on Q2 is a periodic function and can be defined as

$$V_{ds} = \begin{cases} \dfrac{V_m}{T_m}\times t, \ if \ \ 0 \le t < T_m; \\ V_m, \ \ if \ \ T_m \le t < T_{on}; \\ 0, \quad if \ \ T_{on} \le t < T_s\,. \end{cases} \tag{4}$$

In (4), variable Tm is when Vds reaches its maximum value of Vm, Ton is the on time of Q1, and Ts is the switching period. During the rising period, the changing rate of applied drain voltage to Q2 is remained to be a constant,

$$\frac{dV_{ds}}{dt} = \frac{V_m}{T_m},\ 0 \le t < T_m\,. \tag{5}$$

Substitute (5) into (3b),

$$C_{gd}\times\frac{V_m}{T_m} = (C_{gs} + C_{gd})\frac{dV_{gs}}{dt} + \frac{V_{gs}}{R_t}. \tag{6}$$

Up to the point where Vgs=Vth the Cdv/dt induced voltage that appears at the gate terminal of Q2 can be solved from the linear differential equation (6). A closed form solution for the induced gate voltage is derived in equation (7).

$$V_{gs,ind} = R_t \times C_{gd} \times \frac{V_m}{T_m} \times \{1 - e^{\frac{-t}{R_t\times(C_{gd}+C_{gs})}}\}. \tag{7}$$

Equation (7) shows that the gate charges Cgd and Cgs, and the dv/dt slope on the drain of Q2, which is equivalent to Vm/Tm, determine the peak gate voltage induced at Q2. The faster the dv/dt is applied to the drain of Q2, the higher the induced gate voltage is. The maximum induced voltage happens at t = Tm.

$$V_{gs,max} = R_t \times C_{gd} \times \frac{V_m}{T_m} \times \{1 - e^{\frac{-T_m}{R_t\times(C_{gd}+C_{gs})}}\}. \tag{8}$$

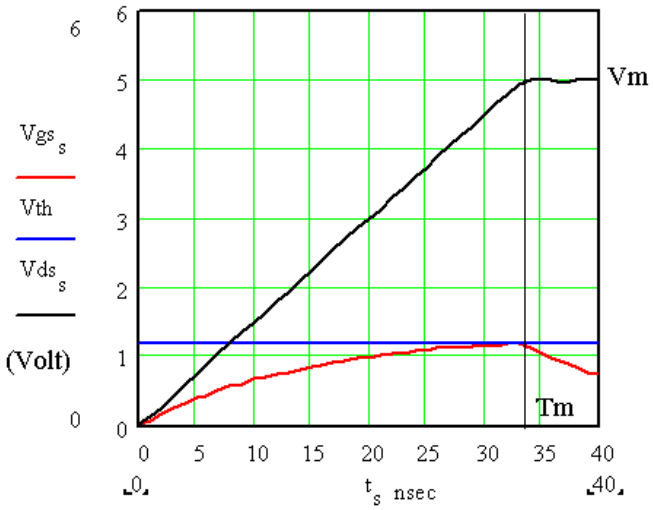

Figure 6. Minimum dv/dt to cause Vgs≥Vth.

If Tm<< Rt*(Cgd+Cgs), equation (8) can be further simplified.

$$\begin{aligned} V_{gs,max} &= R_t \times C_{gd} \times \frac{V_m}{T_m} \\ &\times \{1 - e^{\frac{-T_m}{R_t \times (C_{gd}+C_{gs})}}\} \\ &\cong R_t \times C_{gd} \times \frac{V_m}{T_m} \\ &\times \{1 - 1 + \frac{T_m}{R_t \times (C_{gd}+C_{gs})}\} \\ &\cong R_t \times C_{gd} \times \frac{V_m}{T_m} \times \frac{T_m}{R_t \times (C_{gd}+C_{gs})} \\ &\cong \frac{C_{gd}}{C_{gd}+C_{gs}} \times V_m . \end{aligned} \quad (9)$$

To prevent Cdv/dt induced turn-on, the gate voltage at MOSFET Q2 cannot be greater than its threshold voltage before its drain voltage reaches Vm. The corresponding waveforms are illustrated in Figure 6 and in this particular case, it shows the slowest dv/dt boundary where Vgs is equal to Vth at Tm. If the Vds slew rate applied on Q2 is greater than the one shown in Figure 6, then Vgs will exceed the threshold voltage Vth. As a result, MOSFET Q2 will be turned on spuriously due to the Cdv/dt induced voltage.

BIPOLAR OR CMOS GATE DRIVER?

An in-circuit waveform showing the Cdv/dt induced turn-on effect at Q2 gate is demonstrated in Figure 7. The gate drive circuit might further deteriorate this Cdv/dt induced turn-on problem. It is clear in Figure 7 that the gate driver can only pull the gate voltage of Q2 down to 0.7V, instead of zero, when Q2 is turned off. However, the Cdv/dt induced voltage is sitting on top of this turn-off gate voltage and makes Q2 more vulnerable to the Cdv/dt induced turn-on problem. The gate driver used in Figure 7 is created by a bipolar process.

Usually, a bipolar gate driver cannot pull the gate voltage down to zero because of the saturation voltage of output n-p-n transistors. Gate drivers with CMOS outputs are capable of rail-to-rail swing and will certainly be helpful in lowering the peak induced voltage.

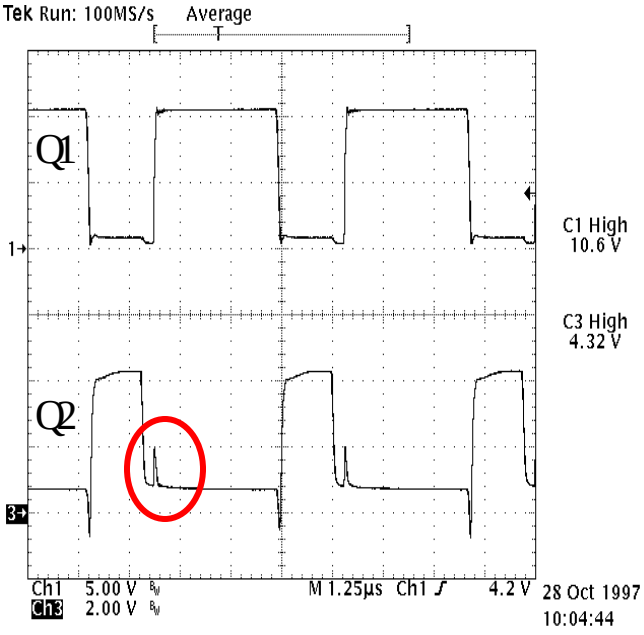

Figure 7. Cdv/dt effect on the gate voltages.

MOSFET SOLUTIONS

Several MOSFET design solutions can be applied to reduce the effect of the Cdv/dt induced turn-on problem in a synchronous buck topology. One solution would be to raise the threshold voltage on the MOSFETs, but this may lead to increase Rdson. Another solution would be to lower the miller capacitance Cgd. Thirdly, increasing the gate-to-source capacitance Cgs in order to prolong the charging time and reduce the peak induced voltage at the gate of Q2. Unfortunately, these methodologies involve design changes in the MOSFET devices that are probably not available to power system design engineers.

In order to prevent Cdv/dt induced turn-on, the criterion for selecting a Q2 device would be based on the Qgd/Qgs1 ratio. Qgs1 is the gate-to-source charge before the gate voltage reaches the threshold voltage. [2] As mentioned above, lowering Cds or enlarging Cgs will reduce Cdv/dt induced voltage. However, Cdv/dt induced turn-on at Q2 also depends on Vds and threshold voltage Vth. It then makes sense to use gate charges instead of gate capacitances to evaluate the Q2 device.

One intuitive way of interpreting the Cdv/dt induced turn-on problem is the accumulated miller charge. When Vds reaches the input voltage, it should be smaller than the total charge on Cgs at the Vth level so that Q2 will not be spuriously turned on.

$$C_{gd} \times V_{gd} \le C_{gs} \times V_{gs} \ . \quad (10)$$

In Figure 6, the maximum accumulated miller charge stored in Cgd is equal to the miller capacitance Cgd times the voltage difference between Vds and Vth when Vds reaches the input voltage. In this case, equation (10) is equivalent to

$$C_{gd} \times (V_{ds} - V_{th}) \leq C_{gs} \times V_{th} \quad . \qquad (11)$$

By dividing whole equation with the right-hand-side term, equation (11) can be further simplified to be a more meaningful expression.

$$\frac{Q_{gd}}{Q_{gs1}} = \frac{C_{gd} \times (V_{ds} - V_{th})}{C_{gs} \times V_{th}} \leq 1 \quad . \qquad (12)$$

Ideally, the charge ratio of Qgd/Qgs1 for Q2 should not be greater than 1 in order to prevent Cdv/dt induced turn-on voltages. In practical, to meet power transfer requirements, the Rdson and packaging of the device must also be considered when selecting Q2.

According to equation (12), higher input voltages will result in higher Qgd charge and, therefore, higher charge ratio of Q2. Thus the Cdv/dt induced turn-on problems tend to be much more severe in laptop dc-dc power supplies than in desktop supplies. Input voltages to the laptop switching voltage regulators range from 5V to 24V, while in the desktop VRM designs the inputs are mainly supplied from 5V.

ASYMMETRIC GATE DRIVE

Since the Cdv/dt induced turn-on at Q2 is caused by the fast turn-on of Q1, reducing the switching speed of Q1 is one possible solution. This can be implemented by adding an external gate resistance Rrise to MOSFET Q1. Optimization of this external gate resistance is extremely important in this case because the goal is to minimize switching losses while reducing dv/dt at turn-on of Q1. Adding an external gate resistance to Q1 would increase its switching losses as a by-product of slowing down the turn-on of Q1. Furthermore, adding gate resistance also causes slower turn-off for Q1, potentially causing loss of dead time with correspondingly conduction overlap of Q1 and Q2. Consequently this will create a huge shoot-through current when Q2 is turned on. An asymmetric gate drive on Q1, as shown in Figure 8, provides a practical solution if an external gate resistor is necessary to resolve Cdv/dt induced turn-on problems. By adding one small Schottky diode to bypass the gate resistor Rrise during the turn-off switching, the rise time of Q1 can be slowed down without a significant slowing at turn-off.

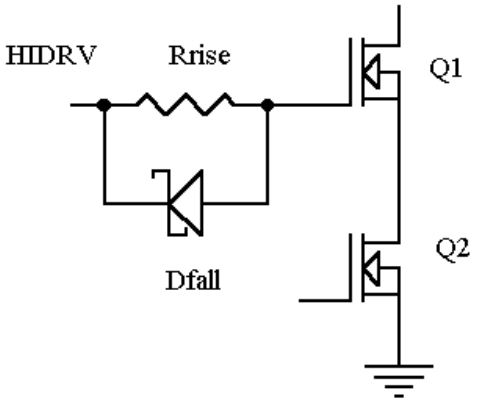

Figure 8. Asymmetric gate drive for MOSFET Q1.

When Q1is turned on, gate voltage is applied through the gate resistance to charge Q1. The total gate resistances including the driver resistance, external gate resistance, and the MOSFET's internal gate resistance controls the turn-on speed of Q1. During turn-off, the gate capacitance of Q1 is discharged to the gate driver through a schottky diode because it has the least resistive path. Still, the Cdv/dt induced voltage spike will appear at the gate of Q2 which might be high enough to turn Q2 on due to the variation of threshold voltages on devices.

The asymmetric gate drive technique is also constrained by PWM controllers due to the constant dead-time control scheme. Fixed dead time from 50ns to 250ns can be found in PWM controllers for powering Pentium™ II CPUs. It is important to make sure that there is no cross conduction between Q1 and Q2 after implementing asymmetric gate drive to MOSFET Q1.

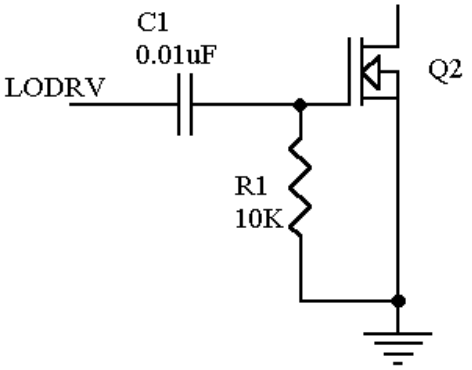

Figure 9. AC gate drive for MOSFET Q2.

AC GATE DRIVE

A more effective way of solving the Cdv/dt induced turn-on problem is to implement an AC gate drive for Q2. An example of implementing an AC gate drive can be found in the schematic of Figure 9. As shown in Figure 9, an AC coupling capacitor and a gate-to-source resistor are added to the gate of Q2. The purpose of using an AC gate drive is not to reduce the Cdv/dt induced voltage, but is instead intended to pull down the turn-off gate voltage at Q2 to below zero. This will shift the Cdv/dt induced voltage to below the threshold voltage. The corresponding waveforms after implementing the AC gate drive are demonstrated in Figure 10.

Implementation of an AC gate drive also depends on the gate drive voltage from PWM controllers. If the driver voltage is supplied from 5V, it will not be sufficient to enhance Q2. During the turn-on transient period, which is defined by C1 and R1, the peak gate voltage is very close to the peak-to-peak applied voltage; therefore, it is very important to ensure that the maximum gate voltage of the device will not be exceeded.

Measured efficiency based on AC and 5V DC drives are illustrated in Figure 11. The tested conditions are 5V input, 2.8V output, and 12.7A load current. MOSFET Q2 remained unchanged while various Q1's with different active areas were tested to search for the optimized device combination. As indicated in Figure 11, the AC drive is a 0.3% - 0.6% more efficient compared with the 5V DC drive circuitry. In terms of power losses, they are equivalent to 2% - 4% improvements.

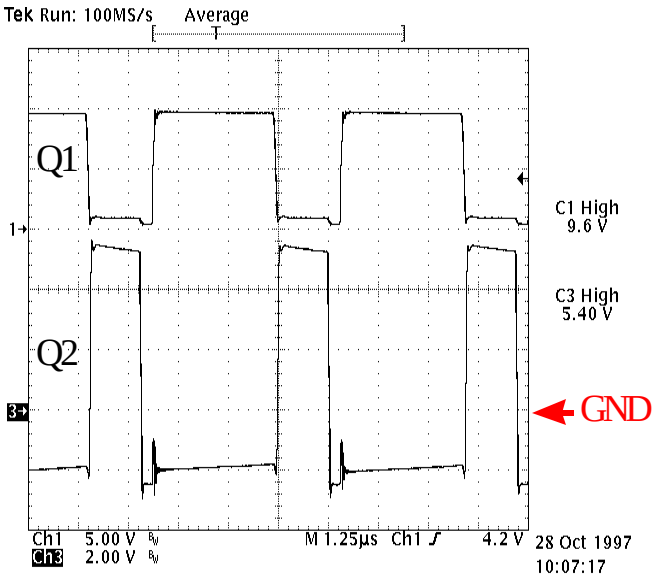

Figure 10. AC gate drive waveforms.

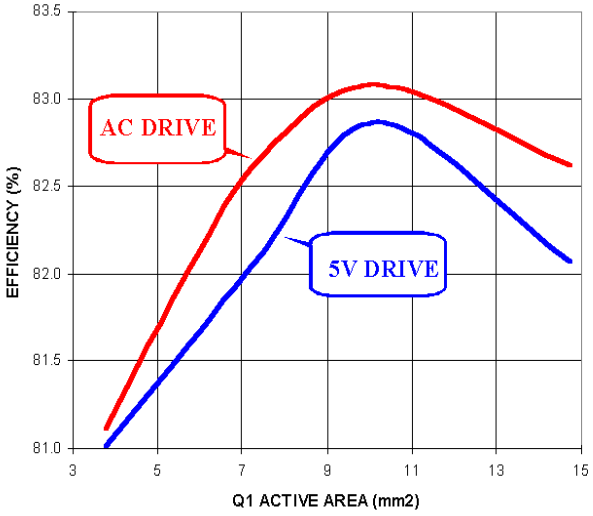

Figure 11. Measured efficiency on ac and 5V dc drives.

CONCLUSIONS

Cdv/dt induced turn-on in a synchronous buck regulator is caused by a rapidly rising drain voltage at the synchronous MOSFET Q2. As a result, the overall system efficiency deteriorates because of the undesired shoot-through currents flowing into both Q1 and Q2. Reduction in Qgd/Qgs1 ratio and increasing the threshold voltage of MOSFET devices can certainly decrease Cdv/dt induced current flow in MOSFET Q2. Several economical circuit solutions are also available to the power supply designers, these include: minimizing Q2 turn off gate drive resistance, ac gate drive at Q2, or asymmetric gate drive at Q1 can reduce or even prevent spurious Cdv/dt turn-on at Q2.

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