

Current Handling and Thermal Considerations in a High Current Semiconductor Switch Package

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Abstract - This paper presents a discussion of the way in which a combination of experimental work and computer modelling has been used to develop a high current discrete semiconductor switch package.

I. INTRODUCTION

In response to the need for a high current, low inductance, low resistance package, International Rectifier have designed the Supertab MOSFET. This new device is capable of carrying currents in excess of 200A and is suitable for applications such as automotive battery disconnection, synchronous rectification in high power alternators and power OR-ing which until now have been dominated by modules. The module approach tends to be expensive and suffers from thermal problems because of poorer heat dissipation due to the isolation layer which adds thermal impedance. The Supertab package is different from existing power MOSFET packages in that the source connection is made through a tab rather than a lead. This is shown in Fig 1.

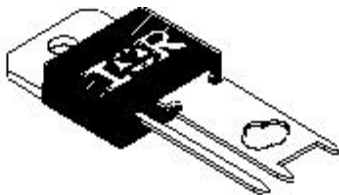


Fig. 1. The Supertab high current power semiconductor package.

The purpose of the source tab is to provide easy mounting to allow the flow of high currents without causing a significant rise in temperature. The drain connection can be made either directly through the header tab or indirectly through the screw which is used to mount the header to the heatsink. The gate connection is made through a gate leg.

Each Supertab MOSFET has a current rating in excess of 200A, and can be easily paralleled for higher current applications. This is best done using a bus bar configuration for which the Supertab package is specifically designed. The design of the step height between the source and the drain in the Supertab allows for the use of a laminated busbar which will further reduce the inductance. A suitable mounting configuration is shown in Fig. 2. In addition to the standard ratings this device has a current surge rating giving information on its performance when subject to high pulses of up to 500A.

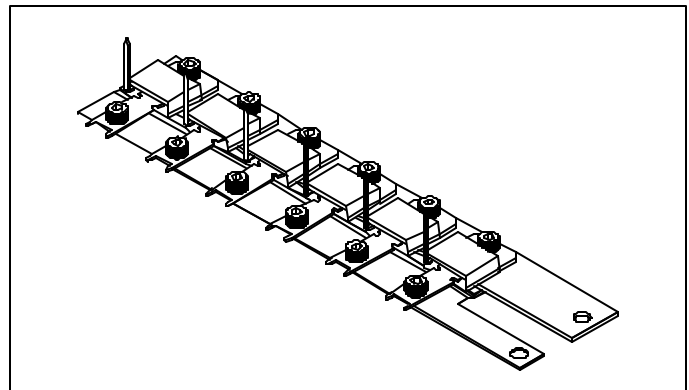


Fig. 2. Parallel mounting of Supertab MOSFETs in a low inductance configuration.

II. PACKAGE DESIGN

When designing a high current plastic package such as the Supertab there are many factors to be considered. In an ideal world the limitations of the silicon die and those of the package would converge to the same operating point. This means that as the current increases to the device limits the die temperature and the package temperature would be at their respective limits, less a safety margin. The operating

temperature of the silicon MOSFET depends on the $R_{DS(on)}$ and the thermal resistance. Recent advances in silicon MOSFET technology have dramatically reduced the on-state resistance of the silicon. Fig 3 shows how the contribution to the $R_{DS(on)}$ of a typical 40V silicon MOSFET die has decreased by a factor of seven since 1985.

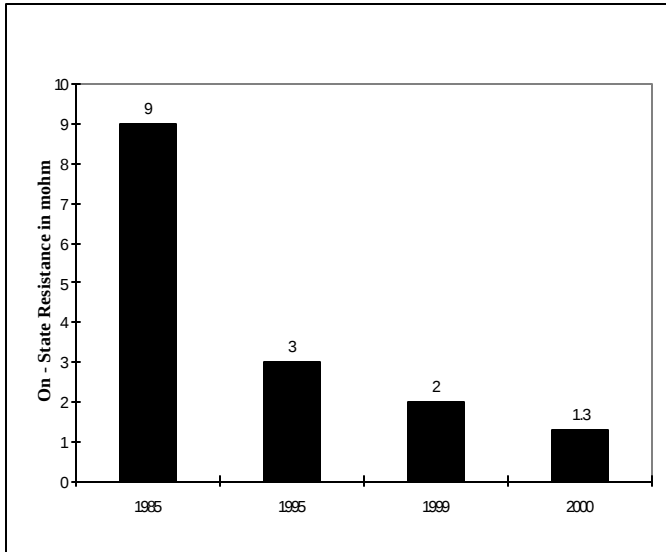


Fig. 3. The decrease in MOSFET on-state resistance over the last 15 years.

In many new devices the voltage drop across the MOSFET is now so low that the current handling capability of the silicon exceeds that of most of the popular packages. This is demonstrated in Fig. 4. It is therefore critically important that

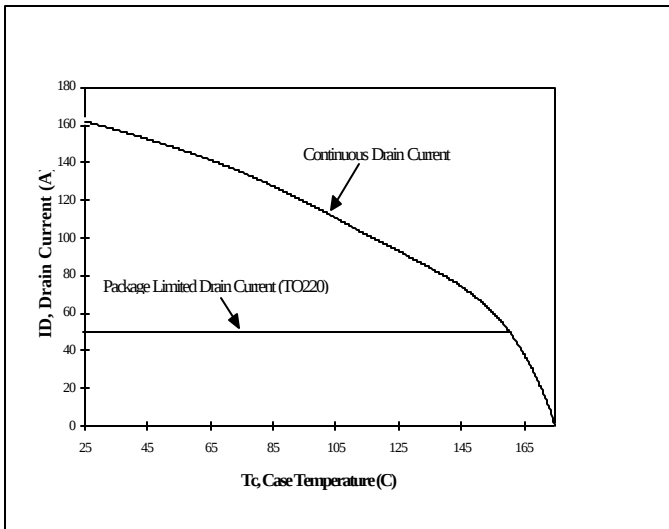


Fig. 4. Maximum drain current vs temperature for a typical TO220 MOSFET, showing the package limited drain current.

significant reductions are made to the die free package resistance if the full potential of the advances in silicon technology are to be exploited.

To calculate the effect of changes in the silicon and package resistances it is necessary to consider the operational temperature rise of the silicon and operational temperature rise of the package separately. Following the normal definitions for thermal resistance it can be shown that the increase in temperature of the silicon for current I , is given by

$$\Delta T = I^2 R_{DS(on)} (R_{\theta j-c} + R_{\theta c-s})$$

Where I is the current in amperes $R_{DS(on)}$ is the MOSFET drain - source resistance at the operating temperature in ohms $R_{\theta j-c}$ is the thermal resistance junction to case in $^{\circ}\text{C}/\text{W}$ $R_{\theta c-s}$ is the thermal resistance case to sink i.e. the contact thermal resistance in $^{\circ}\text{C}/\text{W}$.

For an ambient temperature of 25°C , ΔT must not exceed 150°C , such that the junction temperature does not exceed the maximum allowable limit of 175°C . Temperatures above this limit may cause permanent damage to the device structure.

The temperature rise of the package for the same current I is determined by the temperature rise of the bondwires and the temperature rise of the leg tab. In typical applications the leg tab will be mounted directly to a busbar as in Fig.2 which will provide thermal as well as electrical connections. Therefore the temperature rise of the bondwires is the most critical. This is given by:

$$\Delta T = I^2 R_w (R_{\theta w-c} + R_{\theta c-s}) / N^2$$

Where R_w is the resistance of a bondwire at the operating temperature in ohms $R_{\theta w-c}$ is the thermal resistance from the bondwire loop to the case in $^{\circ}\text{C}/\text{W}$ and N is the number of bondwires.

As with the silicon the ΔT of the bondwires should not normally exceed 150°C for a device operating in an ambient of 25°C . This is because the temperature of the bondwires during operation depends on the power dissipated in the wire and the thermal resistance of the plastic between the wire and the heatsink. If the temperature of the wires exceeds the glass transition temperature of the plastic then changes to the chemical nature of the moulding compound may occur increasing the thermal resistance. The effect of this is to cause further increase in the wire temperature. Furthermore, if the temperature of the wire exceeds T_j max the wire will act as a heat source for the die instead of a heatsink, an undesirable state of affairs.

It is apparent that if the performance of the device as a whole is to be optimised, then the ΔT for the silicon and the ΔT for the bondwires must be equal for a given current. This balance can be achieved by altering

- the on state resistance of the silicon
- the die free package resistance
- the thermal resistance of the package, junction to case and contact resistance.
- the thermal resistance between the bondwires and the package.

Taking each of these parameters in turn the best way forward can be determined.

A. On State Resistance: Silicon

The heating of the silicon for a known current I is given by $I^2 R_{DS(on)}$. Therefore a device with a high current rating will necessarily have a low $R_{DS(on)}$. The contribution to the on state resistance from the silicon depends on the area of the silicon and the wafer processing technology. The impressive reductions in $R_{DS(on)}$ shown in Fig 2 are a result of advances in silicon processing techniques which have enabled device designers to significantly increase the density of cells in the MOSFET structure. Recent developments such as Trench and P-Column technology have further reduced the on-resistance of a MOSFET of a given size. It should be remembered that this is a temperature dependent parameter which will be higher at operational temperatures than the databook value at 25°C. Graphs showing how the on-state resistance varies with temperature are usually available from the device manufacturer.

B. Die Free Package Resistance

The die free package resistance is the resistance of the package excluding the resistance of the silicon MOSFET. In the case of a Supertab device mounted directly onto low resistance busbars the DFPR is principally the resistance of the source bondwires. The more bondwires that there are in the package, the lower the resistance will be. In a similar way the DFPR may be reduced by using bondwires with a larger diameter. In most cases the diameter and number of bondwires used is restricted by the area of the bondpad on the silicon die and the processing technology available. In trying to design a high current package from a DFPR viewpoint the best solution is to use as many wires as possible with the largest diameter available. This is not always the case but it is a good starting point. Alternatives in this area include the development of clip connectors although these are not yet available on production parts for large size die. Whether

bondwires or clips are used, cost is always a consideration, so unnecessary use of additional connectors should be avoided.

C. Thermal Resistance

The thermal resistance of the package depends primarily on its size and the contact area with the heatsink. Whilst a large package will guarantee a lower thermal resistance, many applications are very restrictive in terms of the space available for the device and it is in such applications that a small discrete device has advantages over a module. A more detailed discussion of thermal resistance and contact thermal resistance for the Supertab package is given in [1].

The thermal resistance between the bondwire and the header is a parameter that isn't normally considered. However, to determine the temperature rise of the bondwires, and hence their current carrying capability, it is very important that this value is known. The method used to measure the thermal resistance is described in the next section.

III. EXPERIMENTAL

A. Thermal Resistance and Bondwire Heating.

To make an intelligent decision about the choice of wirebonds and their arrangement in the Supertab package more information was needed about the temperature of the wires for a given current. In view of the many variables it was decided that the temperature rise for a given current should be determined experimentally. Supertab samples were made up in which the wirebonds were connected directly to the header. Fine wire thermocouples were glued to the aluminium wire at the top of the wirebond loop. The samples were then molded and trimmed using standard processing routes.

Two sets of experiments were performed to fully characterise the thermal resistances in the package. In Experiment 1 a current of up to 100A was passed through one bondwire and the temperature of the adjacent bondwires was measured as shown on Fig 5. These wires were electrically disconnected so did not carry current. In Experiment 2 all of the wires were electrically conducting and the temperature rise of each wire was measured. For the purpose of these experiments the Supertab package was screw mounted using heat sink compound on large copper busbars which provided both the power connection and the heatsinking and the temperatures of the wires were recorded for a range of currents up to 300A. The voltage drop across the bondwires at the operating temperature was measured.

The results from the experimental work were used to create and verify computer models of the thermal performance of the package. The primary aim of this work was to develop modelling capabilities such that further experimentation would no longer be required when considering all of the different options for new package design.

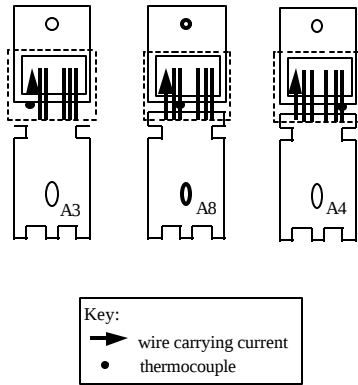


Fig. 5. Schematic of Experiment 1

One of the techniques used was Finite Element Analysis. The first stage of this work was to use the software to model the scenarios in Experiment 1 and Experiment 2. Once this was done the results of the modelling could be compared with the empirical data and an iterative process could be followed until agreement between modelled and experimental results was achieved. The work was then verified for a third independent situation. Examples of the modelling work are given in Figs. 6 and 7. These show the analysis for both types of experiment.

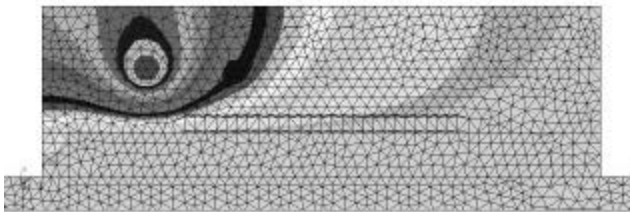


Fig. 6. The results of the Finite Element Analysis model for Experiment 1.

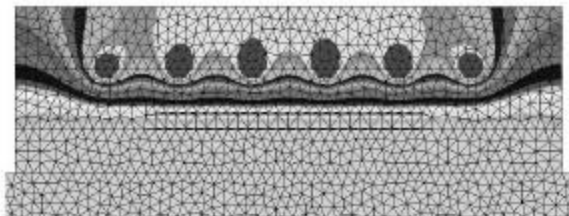


Fig. 7. The results of the Finite Element Analysis model for Experiment 2.

In addition to the FEA a thermal equivalent circuit was drawn up in PSPICE to allow the effect of changes such as the number of wires to be quickly and easily determined. Comparing the results of the approaches mentioned so far revealed that there was a further important factor namely the actual position of the wirebonds on the top contact of the silicon. This is discussed in the next section.

B. Modelling bond wire positioning

With large area die the effect of top metalization sheet resistance can add significant contributions to device on resistance. The voltage dropped across the top metalization between a MOSFET cell and wirebond for example, will reduce the drain to source voltage available to that cell. This leads to cells under wirebonds conducting more current than those located furthest from the bond position. One can reduce the contribution of top metal sheet resistance to on resistance by adopting more wirebonds. If positioned correctly the extra wirebonds will reduce the distance current has to flow through the top metalization to each MOSFET cell.

Experimental trials may be performed to help attain the lowest device on resistance by varying the positioning of wirebonds. However, this approach can be both time consuming and costly in terms of equipment time. To help attain the best wirebond positioning and cut design time we have developed a novel approach utilising computational modelling. Using the model we are able to map out the source potential across a die surface. By modifying wirebond positioning to reduce the source potential across the die, a lower on resistance is obtainable. Fig. 8 shows the source potential profile of a Supertab device containing 5 wirebonds. Note that the wirebond positions are easily identified as the troughs in the profile.

Work has been done to consider several arrangements of wirebonds. Fig. 9 shows an alternative non-uniform configuration. Samples wirebonded in this way tended to show failures when surge tested. Devices wirebonded as shown in Fig. 8 had a surge rating of 540A for a 6ms square pulse and 480A for a 10ms square pulse.

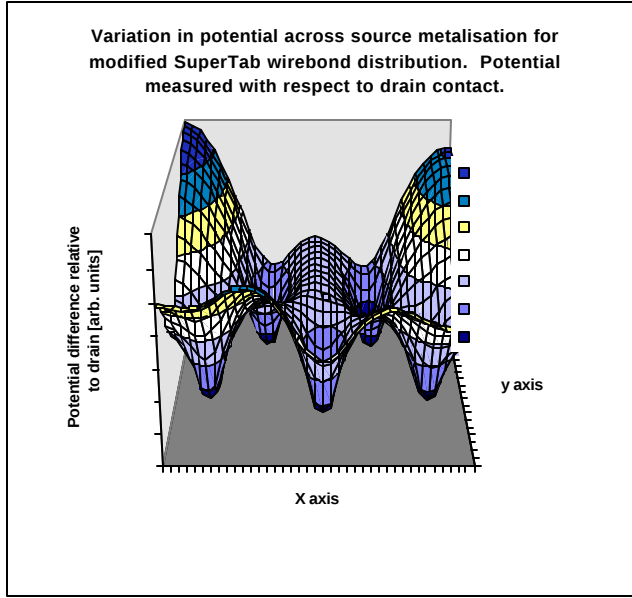


Fig. 8. Results of wirebond position modelling for a well designed package.

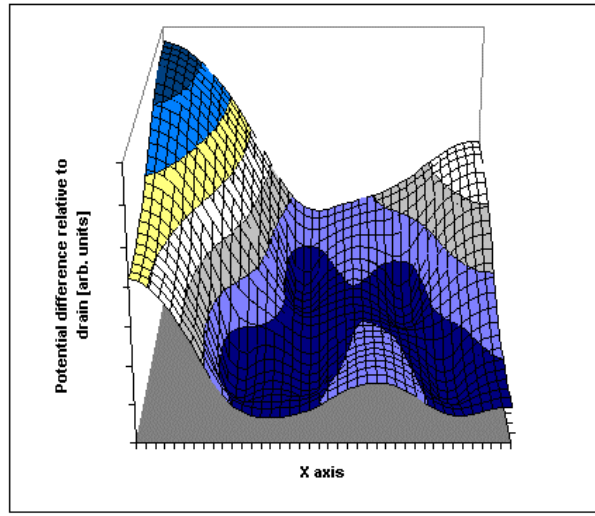


Fig. 9. Results of wirebond position modelling for a MOSFET with a lower surge current rating than in Fig. 8.

IV CONCLUSION

The work presented in this paper has enabled International Rectifier to design a well balanced SuperTab MOSFET. The electrical and thermal characteristics of this device are given in Table 1.

Table I. Summary of Electrical and Thermal Characteristics of A Supertab MOSFET

Maximum Current	> 200A
$R_{DS(on)}$ 30V	1.6 m Ω (typical), 2 m Ω (max)
$R_{DS(on)}$ 55V	2 m Ω (typical), 3 m Ω (max)
Thermal Resistance	0.4°C/W (junction to case), 0.25°C/W (contact)
I_{DSM}	540A (6ms square pulse)

In this device the maximum temperature rise of the package i.e. the bondwires, and the maximum temperature rise of the silicon junction will be the same. That is to say that the current carrying capability of even very low $R_{DS(on)}$ silicon is not restricted by the package. The temperature derating curve is shown in Fig. 10. This shows clearly that I_D is no longer package limited, even at lower temperatures.

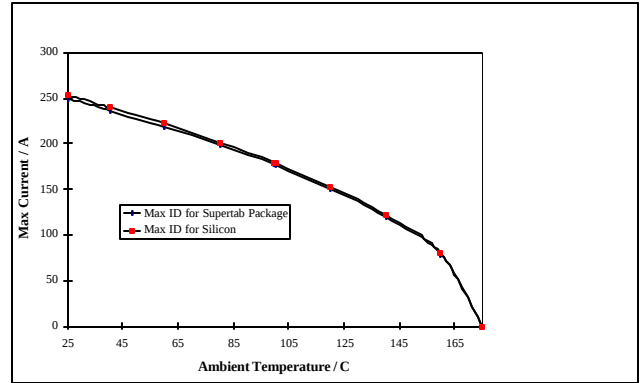


Fig. 10 Maximum drain current vs temperature for a the Supertab MOSFET.

ACKNOWLEDGMENT

The authors would like to thank Mark Pavier, Zoe Towells and Paul Westmarland from International Rectifier GB, and Vincent Thierry from IR France for their contributions to the work presented in this paper.

REFERENCES

- [1] P. J. Dugdale and A. Woodworth, "Supertab: A novel high current semiconductor switch package," Proceedings PCIM '99 / HFPC '99, to be published.