IMPROVED POWER DIP RIDE THROUGH, LOW SPEED PERFORMANCE, AND OTHER ADVANTAGES OF USING PHASE CONTROL SOFT START IC FOR VARIABLE FREQUENCY INVERTER AC MOTOR DRIVES

The use of SCR phase control to "soft-start" the DC bus capacitor for a PWM inverter AC drive has not previously been generally used, because the complexity of implementing the phase-control firing circuit with conventional components has not been justified. A new Soft Start IC now makes the approach attractive in it's own right. It also offers several important value-added functions, which are not possible with conventional bus capacitor charging methods. This paper explains the most important of these value-added functions, including improved power dip ride through and improved low speed performance of the inverter drive.

INTRODUCTION

Variable frequency PWM inverter drives for AC motors require a DC power source to feed the inverter. An uncontrolled diode bridge rectifier with DC bus capacitor commonly converts the incoming AC line to nominally fixed DC voltage for this purpose. Some means is needed to limit the bus capacitor charging current when the AC line is switched on. For low power drives, up to about 1kW, a temperature sensitive (NTC) resistor, connected in series with the rectifier output, is often used. See Figure 1(b). For higher power, a resistor, bypassed in normal operation by an electromechanical contactor, or by an SCR, is commonly used. See Figure 1(c). Another common approach is to connect SCRs in the input bridge itself. See Figure 1(a). The SCRs are used, in effect, as an on/off contactor. Firing current is withheld until the auxiliary diode/resistor circuit has charged the bus capacitor; firing current is then applied continuously, to turn the SCRs fully on for normal operation.

More sophisticated use of the half-controlled SCR bridge of Figure 1(a) could be made, by phase controlling the firing angle of the SCRs to limit the bus capacitor charging current. This would eliminate the auxiliary diodes and resistor. Phase-controlled SCR rectifiers have been widely used in other applications for many years. The use of SCR phase control, solely for the purpose of limiting the bus capacitor charging current in a PWM motor drive, has however generally not gained favor. The firing circuit, implemented with off-the-shelf components, would be too complex and occupy too much board space.

Complicating the design is the requirement that the phase controlled firing circuit must have high integrity: it must never deliver miss-timed firing pulses, even with severe distortion of the line, or during transient line dips and outages. Yet the speed of recovery in delivering correctly timed firing pulses after line outage is crucial, to optimize the power-dip-ride-through capability of the drive.

The recently introduced IR1110 Soft Start IC, capable of one or three-phase operation, shown in Figure 2, occupies minimal board space, and for the first time makes SCR phase control of the bus charging current of a PWM inverter drive practical. It offers a competitive solution in it's own merit, at power of about 10HP and upwards. In addition, it offers important value-added functions, which are simply not possible with conventional resistor charging. These functions are essentially independent on the basic soft charging function, yet come with little added complication.

The major purpose of this paper is to explain the most important value-added functions made possible by SCR phase control, as embodied in the new Soft Start IC. These are:

- Improved power dip ride through
- Protection against loss or reduction of one input phase
- Control of the DC bus voltage to provide:
- Protection against line voltage swells
- Increased inverter output current at low speed
- Improved motor voltage waveform at low speed
- Protection against DC bus short circuit

BASIC ARCHITECTURE

As shown in Figure 3, the soft start IC, with peripheral components, floats at the positive terminal of the half-controlled bridge, driving the SCR gates directly, without isolation. Optional opto-couplers deliver isolated fault feedback signals, and provide optional input control functions. Power supply voltage for the IC can be derived from the current that flows in dv/dt snubber circuits connected across the SCRs, or from an isolated power supply.

SOFT START FUNCTION

Before discussing the value-added functions, it will be instructive to compare the phase control soft start function versus the conventional resistive charging scheme. In the resistive scheme, as illustrated in Figure 4(a), when the bus voltage reaches a preset level during power up, a bypass switch is closed across the resistor. Resistive designs commonly take hundreds to thousands of milliseconds to charge the DC bus, partly because the rate of rise of voltage decreases exponentially during the charging process.

With SCR phase control, the phase of the SCR firing pulses is advanced step by step, increasing the bus voltage in a series of steps, as illustrated in Figure 4(b). At each step, a discrete pulse of current is drawn determined by the rate of advance of the SCR firing angle, and by inductance in the AC lines, as well as inductance (if any) at the output of the rectifier. A typical oscillogram of bus voltage during ramp-up is shown in Figure 5. The

rate of advance of the SCR firing angle can be programmed for essentially linear rise of bus voltage, at a significantly faster rate than is common with resistor charging. Total ramp-up time (after an initial delay of about 150msec) is typically programmed in the range of 150 to 350 milliseconds.

POWER DIP RIDE THROUGH

During short dips and outages of the input line voltage, the bus capacitor voltage may fall sufficiently that a bus under-voltage condition is reached, necessitating that power flow to the PWM inverter and motor be temporarily interrupted. It is desirable that load power is re-established as quickly as possible when the line voltage returns, to minimize the effect of the line interruption on the operation of the drive. The ability of SCR phase control to quickly re-establish load power after line interruption is fundamentally superior to that of the resistive charging method.

As illustrated in Figure 6(a), with resistive charging, the resistor is re-inserted during the line interruption so that it limits the capacitor recharging current when the line voltage returns. During the period after the line voltage has returned and the bus capacitor is being recharged via the resistor, it is generally not permissible simultaneously to deliver power to the motor, because the power dissipation and voltage drop across the resistor would be prohibitive. The result is that the total time for which the motor remains without power is approximately the sum of the line outage time plus the capacitor recharging time. The latter may be several times the former, thus the total period of load outage can be several times the period of the actual line outage.

With SCR phase control, by comparison, not only is the re-charging of the bus voltage usually faster than with resistive recharging, but power can be transmitted to the motor during the ramp back period, because there is no dissipating resistor to prevent this. See Figure 6(b). The result is that SCR phase control allows motor power to be re-established significantly faster, minimizing the impact of the line interruption.

PROTECTION AGAINST PHASE LOSS

The phase control firing circuit integrates the three phase line voltages, to produce noise-free timing waves, for synchronization of the SCR firing pulses to the line voltage. These timing waves are also used to provide noise free detection of the loss of one input phase during three phase operation.

As illustrated in Figure 7, when loss of one phase occurs, the SCR firing pulses are removed after a preset time, shutting down the rectifier. An optional phase loss feedback is provided. When the missing phase returns, the bus voltage automatically ramps back by phase control to set value. Automatic shut down of the rectifier when one phase is lost is generally desirable, to protect the bus capacitor. This is because the capacitor ripple

current becomes much greater when one phase is missing, and will generally exceed the capability of the capacitor.

CONTROL OF THE DC BUS VOLTAGE

The phase control function, already installed for soft starting, can be utilized to regulate the steady DC bus voltage during normal operation. A bus reference voltage is compared against the actual bus voltage, and the error is amplified and applied as input to the phase control circuit, to provide closed loop control of the bus voltage.

Bus voltage regulation should be done judiciously, as discussed later, to avoid excessive ripple current in the bus capacitor. Typical operating conditions under which the bus voltage regulation function can be used to advantage are discussed in the following sections.

PROTECTION AGAINST BUS OVER-VOLTAGE

The input line voltage may surge above the normal maximum continuous operating level for short periods - typically thirty seconds or less - due to external system disturbances. Under this condition, the bus voltage regulation function can be automatically engaged, to limit the bus voltage to a set maximum. It is necessary only to set a maximum value for the bus reference that corresponds to bus voltage slightly higher than maximum normal continuous operating voltage. For this purpose only, the bus reference can be generated locally via a resistive divider across the IC power supply; it is necessary to use an external PWM reference isolated from the IC.

Figure 8 illustrates operation of the voltage regulation function in limiting the bus voltage during line voltage swell. Utilizing the voltage control function in this way protects the bus capacitor, and the inverter, from temporary surges of input voltage. The bus capacitor is able to carry the increased ripple current caused by phase control, for the short period of the voltage swell.

BUS VOLTAGE REGULATION AT LOW SPEED

Increased inverter output current

As illustrated in Figure 9, at low output frequency, the instantaneous junction temperature of the IGBTs in the PWM inverter tends to follow the instantaneous value of motor current. There is little averaging of junction temperature over the duration of the low frequency output cycle, and the peak junction temperature is significantly higher than the average value. At higher output frequency, the thermal inertia of the IGBT junction temperature closer to the average value. The limiting operating temperature for the IGBT

is the peak - not the average - value, therefore the permissible output current of the inverter is significantly lower at low output frequency than it is at higher frequency.

If the DC bus voltage is regulated to a relatively low value at low speed, the IGBT switching losses, which are approximately proportional to the IGBTs will increase at reduced bus voltage, in order to maintain the desired motor voltage. This will increase the conduction component of desired motor voltage. This will increases the conduction component of IGBT power losses. The total IGBT losses - the sum of the switching losses and the conduction losses - will nonetheless generally decrease.

For given peak permissible inverter output current, as determined by the peak junction temperature of the IGBTs, without bus voltage inverter output frequency, according to the control characteristics shown in Figure 11(a) and (b). With bus voltage regulation, the permissible output current at 2Hz output frequency is equal or greater than the permissible current at 20Hz; is also significantly greater than the permissible low frequency output current with the bus voltage unregulated.

Improved voltage waveform

At low speed, the amplitude of the fundamental component of voltage applied to the motor is a small fraction of the full rated voltage, particularly when the motor is lightly loaded. The line to line output voltage of the PWM inverter consists of a train of narrow pulses with low duty cycle due to low modulation index at low speed. The amplitude of these pulses is equal to the DC bus voltage. The duration of each voltage pulse may typically vary from less than a microsecond, to a few microseconds, over the span of the fundamental output cycle. Pulse duration decreases as PWM frequency increases. Unbalances in the switching instants between phases of less than a microsecond, due to small differences of dead-time, and of the characteristics of the IGBTs themselves, can therefore cause significant pulse width errors, and corresponding significant distortion of the motor voltage and current waveforms.

With the DC bus voltage controlled to less than the maximum value at low speed, the amplitude of the line to line output voltage pulses decreases, thus their duration must be correspondingly increased, to maintain the desired fundamental component of motor voltage. The relative effect of switching errors therefore decreases in proportion to the reduction in the bus voltage.

Effect of bus voltage control on the line-related ripple current in the bus capacitor

As the SCR firing angle is phased back from the fully on condition, for a given average current in the DC link, the bus ripple voltage, and the line related capacitor ripple current increases. If excessive ripple current in the capacitor due to phase control is to be avoided, it is generally not permissible to operate at the full rated DC current when the bus voltage is under regulation. Fortunately, at low motor speed, even though the required *inverter* output current and motor torque may be high, the corresponding *rectifier* DC output

current, with appropriately reduced bus voltage, will be only a fraction of the full load value, because the power throughout is relatively low. This is illustrated by the design examples previously considered in Figure 11.

The average DC link current at reduced bus voltage is only a fraction of the full rated value. Therefore the corresponding maximum design value of line related capacitor ripple current at reduced voltage can turn out to be less than the mandatory design value that occurs with no phase delay and full rated power. Whether this will be so depends on the minimum design value of the input line inductance (assuming no DC output inductance). As line inductance increases, the width of the rectifier output current pulses also increase. With zero phase delay, the driving ripple voltage also increases, but only until continuous rectifier output current is attained. At this point, the driving ripple voltage stays approximately constant with further increase of line inductance; thus, once continuous conduction is reached, ripple current decreases in approximate proportion to the increase in inductance. At reduced (i.e., phase-controlled) bus voltage, the rectifier output current remains discontinuous at all practical values of line inductance, and the driving ripple voltage steadily increases as line inductance increases. The net result is that as line inductance increases, a crossover point is reached at which the ripple current at reduced bus voltage and reduced rectifier output current starts to exceed that at full rectifier output current and zero phase delay.

Considering the specific design example illustrated in Figure 11. The rms value of the line related ripple current in the bus capacitor will not exceed the full speed and full load value. The condition being that the minimum design value of line reactance is lower than about 1.1% for control curve (a) in Figure 11 and lower than about 2.2% for control curve (b). These values of line reactance are related to the full rated input line kVA for the drive.

For greater values of minimum design line reactance, the ripple current in the bus capacitor at reduced bus voltage will be greater than at full voltage. The ripple current rating of the capacitor would then have to be greater than that needed at full bus voltage, for continuous operation at the low speed reduced bus voltage condition. For control characteristic (c), the line-related capacitor ripple current at reduced bus voltage is approximately 2X the value at full rated power, full bus voltage, for minimum design line reactance of 1%, and approximately 2.7X, for minimum design line reactance of 2%.

PROTECTION AGAINST BUS SHORT CIRCUIT

If a short circuit occurs across the DC bus - caused for example by a faulty bus capacitor or a mis-wired external brake resistor - the ability to phase control the SCR firing pulses can be used advantageously to limit the fault current.

In Figure 12 (a), a DC bus short circuit already exists at power up. As normal ramp-up starts, the SCR firing angle advances. By the time the firing angle has advanced to about 40 degrees, the IC detects the short circuit. The firing angle is then reset to the fully

retarded value, again proceeds to re-advance, and is again reset. The cycle repeats indefinitely. The net results is that a continuous pulsating limitation of the fault current is provided, at a manageable level, allowing plenty of time for secondary protection to act.

In Figure 12 (b), a bus short circuit occurs during normal operation at full bus voltage. The amplitude of the first pulse of fault current output of the rectifier is high, because it occurs with the SCR already conducting at zero phase delay. Immediately after the first large current pulse, the firing angle is reset to full phase retard. The fault current is then contained by the pulsating action described above.

CONCLUSION

This paper has demonstrated how the IR1110 Soft Start IC, which provides SCR phase control of the bus capacitor charging current, also offers other significant value-added operating functions. These functions will enhance the overall performance and reliability of variable frequency PWM inverter AC drives.

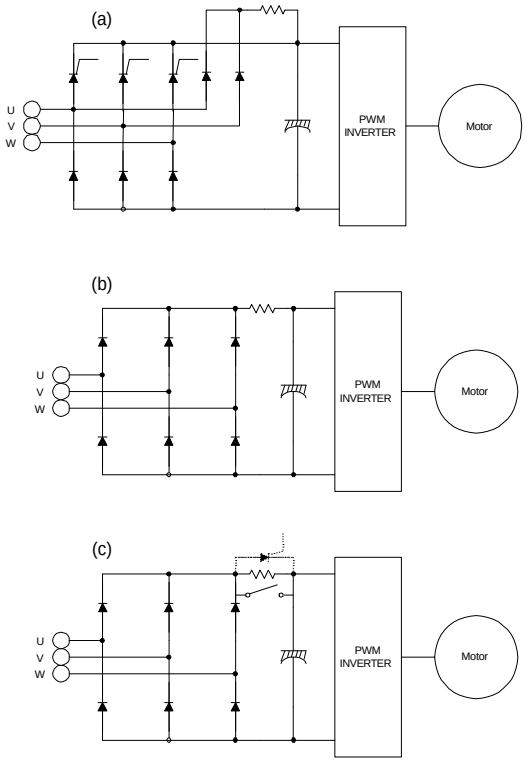

Figure 1: Conventional Methods of Charging the DC Bus Capacitor

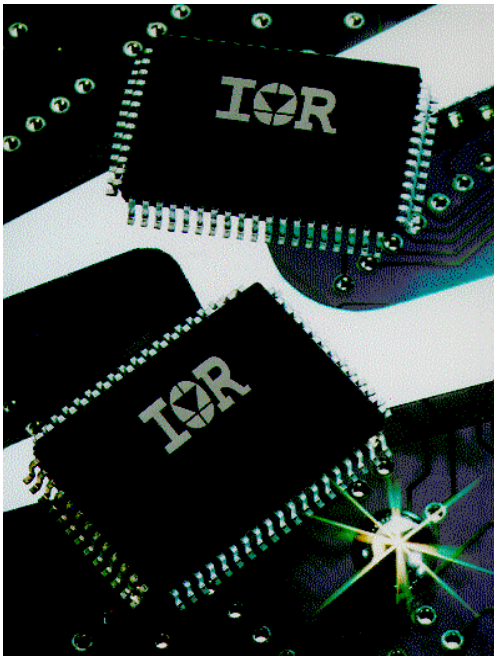

Figure 2: IR1110 Soft Start IC in MQFP64 Package

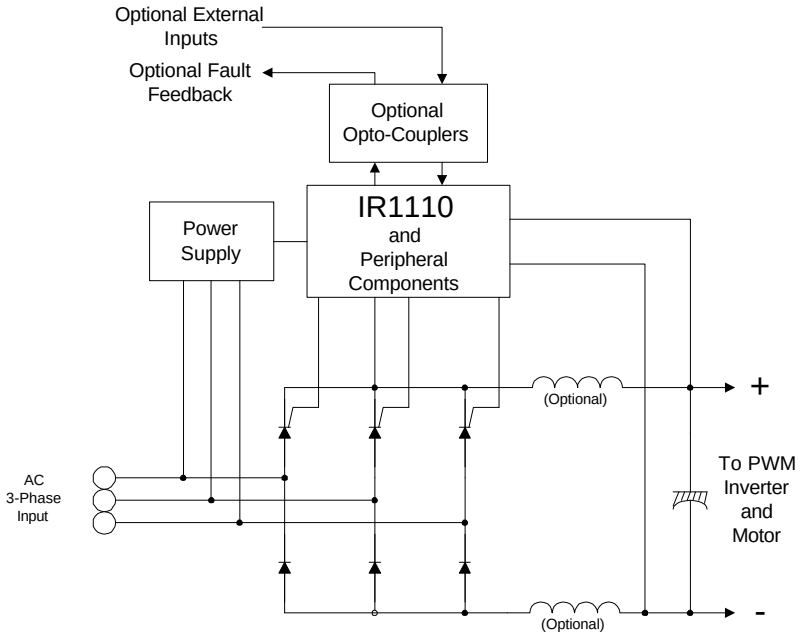

Figure 3: Basic System Architecture for Soft Start ASIC

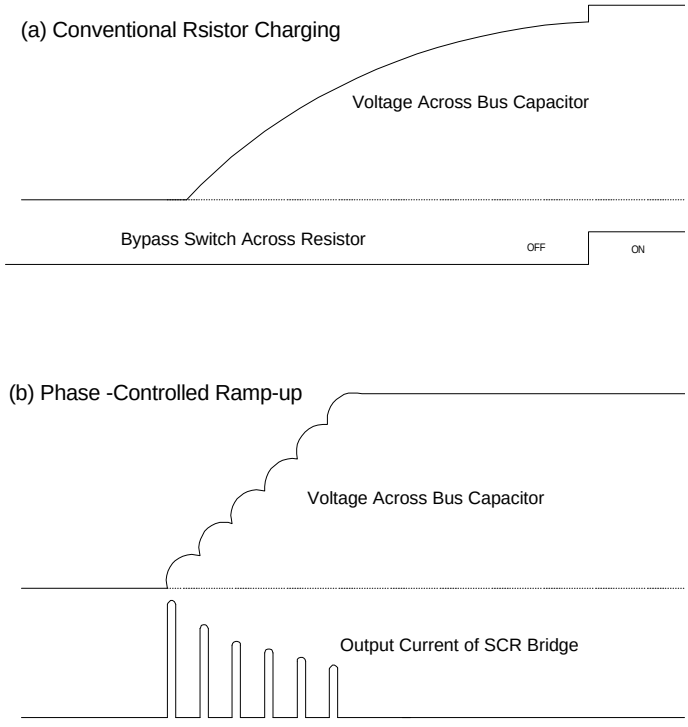

Figure 4: Conventional Method versus IR1110 Phase-Controlled Bus Charging

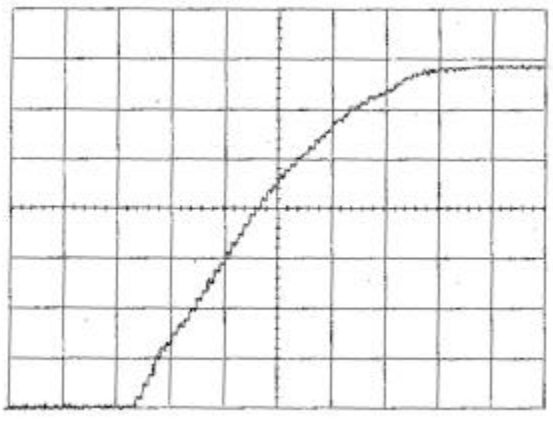

Figure 5: Typical Bus Voltage Ramp-up

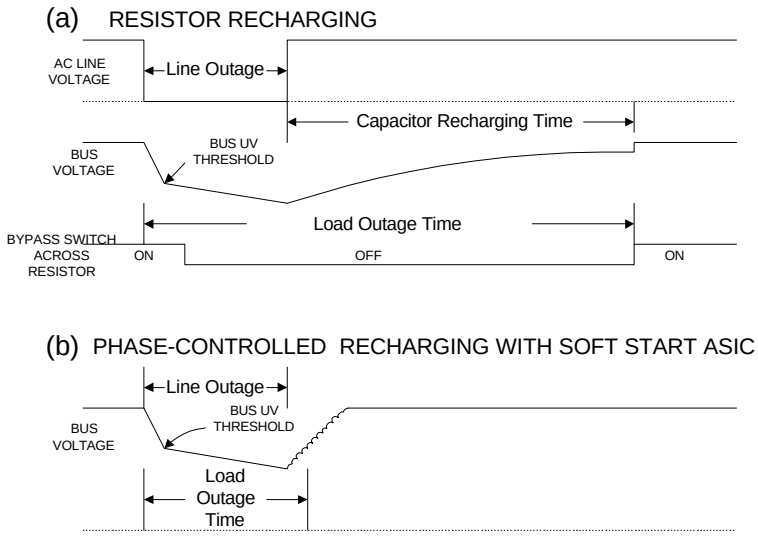

Figure 6: Power Dip Ride Through

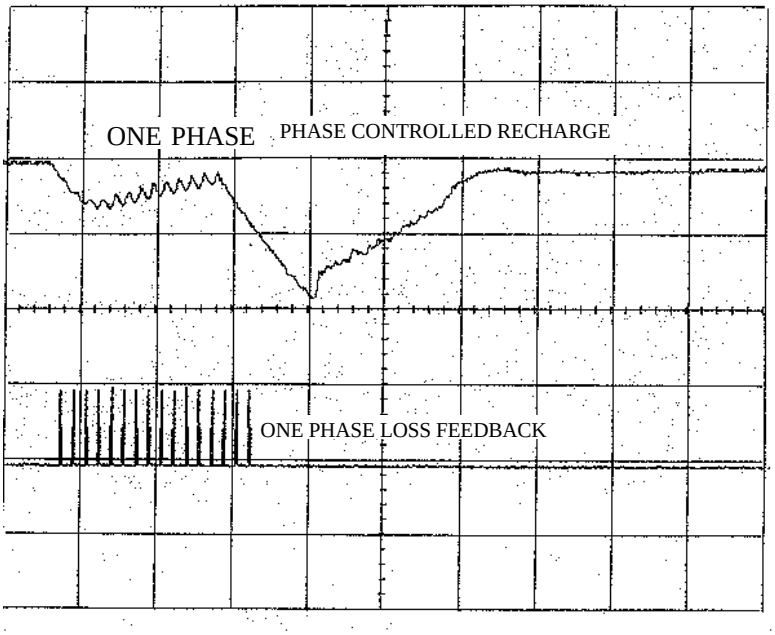

Figure 7: Operation During One Phase Loss

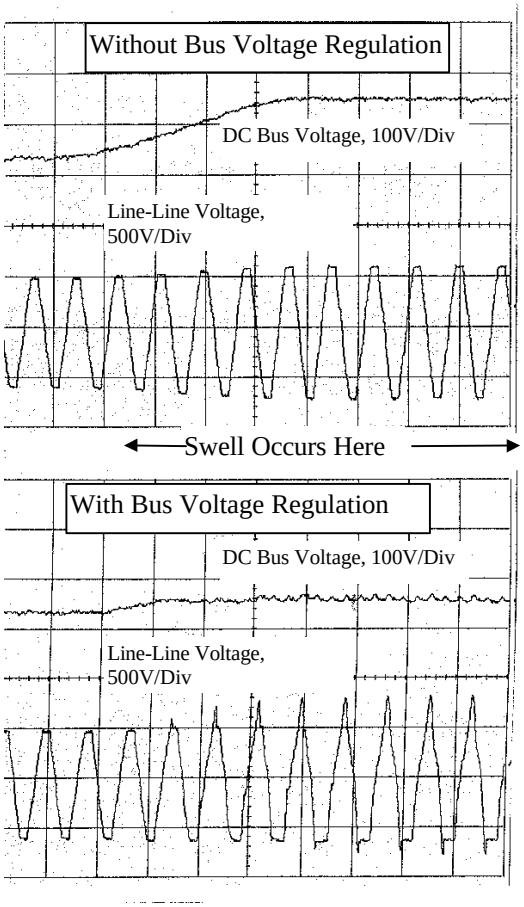

Figure 8: Regulating the Bus Voltage Against Transient Input Voltage Swell

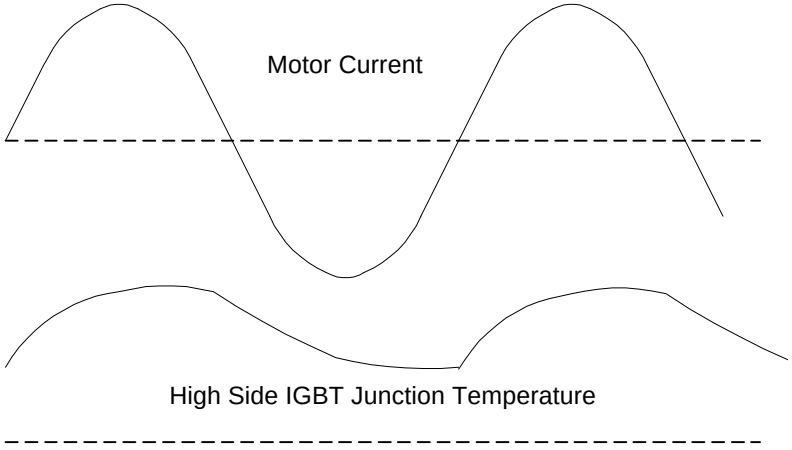

Figure 9: Instantaneous Junction Temperature of IGBT at Low Output Frequency

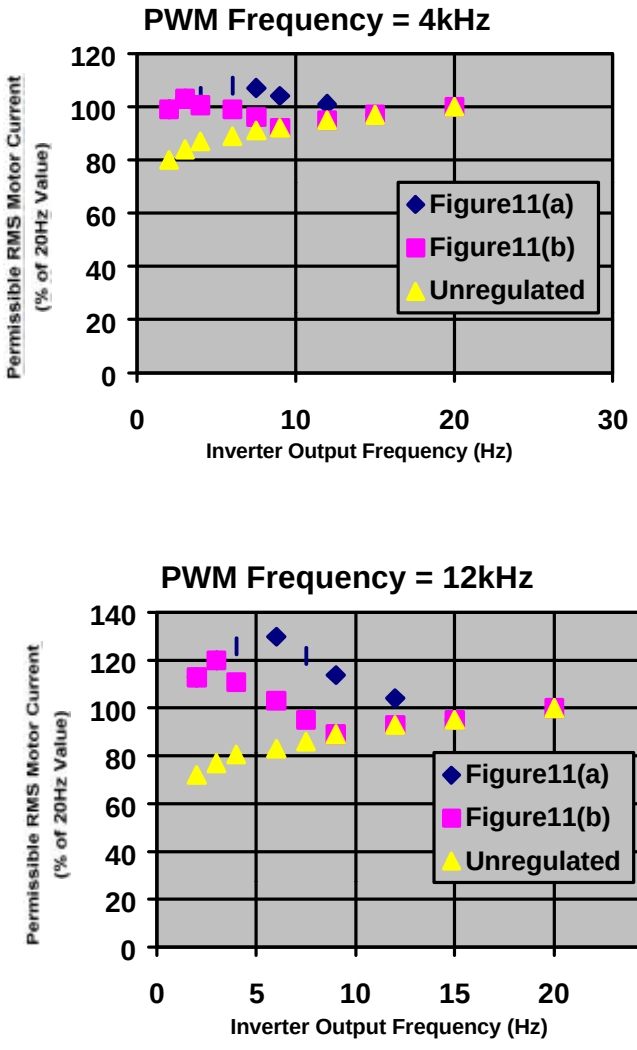

Figure 10: Permissible Output Current of PWM Inverter versus Output Frequency, with and without Bus Voltage Regulation

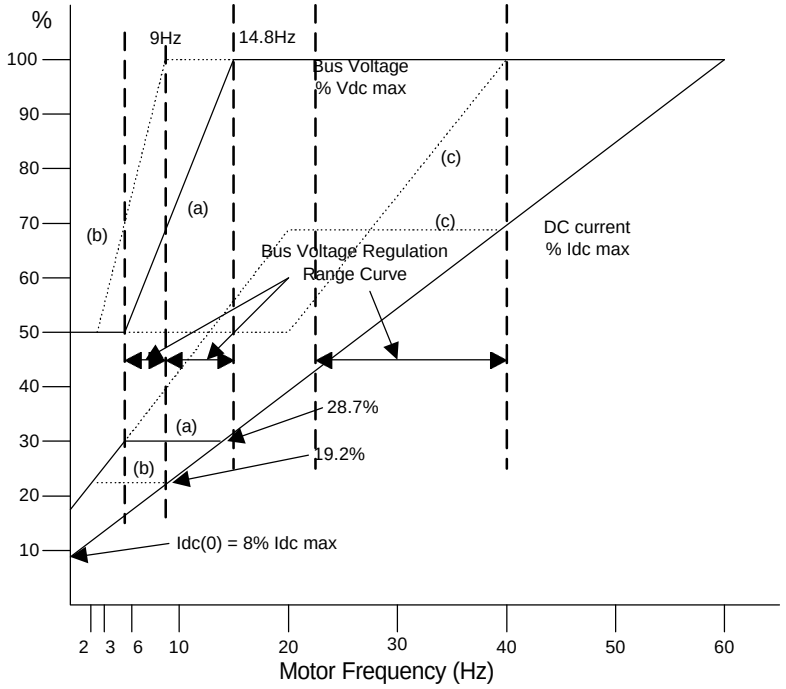

Figure 11: Bus Voltage & DC Current vs. Motor Freq for Constant Torque Drive

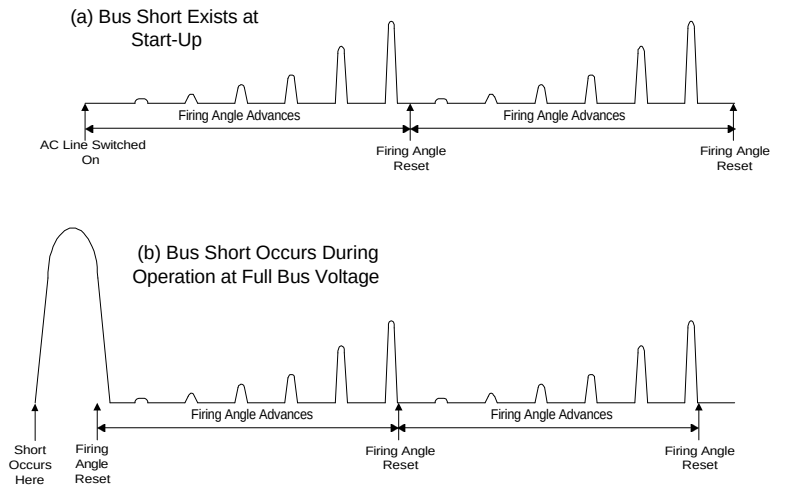

Figure 12: Operation with DC Bus Short Circuit