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New Power MOSFET Technology with Extreme Ruggedness and Ultra- Low $R_{DS(on)}$ Qualified to Q101 for Automotive Applications

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Abstract – An extremely rugged technology has been developed for ultra low $R_{DS(on)}$ applications. This paper compares the *R.A* product and ruggedness of this new technology with a previous generation technology. A factor of 2 improvement in *R.A* product and a factor of 5 improvement in avalanche energy have been demonstrated. The paper also presents a scheme to reliably rate devices under repetitive avalanche conditions.

1. INTRODUCTION

Today's automotive applications demand improved system efficiency at low cost. As system size shrinks and frequency increases, the performance demand on components rises rapidly. Trends have been towards lower $R_{DS(on)}$ parts, resulting in fewer components and improved efficiency and performance. However, as die size has decreased and switching frequency increased, the ruggedness requirements on today's power MOSFETs has significantly increased due to increased power density. Modern systems require parts to withstand repetitive high voltage transients generated by di/dt and parasitic inductance, sometimes forcing devices into a repetitive avalanching condition. A technology with extreme ruggedness has been developed, while maintaining ultra low $R_{DS(on)}$. This technology is ideal for electronic power steering, starter alternator and direct battery control automotive applications.

2. TECHNOLOGY

The technology described here is based on International Rectifier's advanced planar stripe topology. The stripe topology results in much higher ruggedness compared to a cell topology, since the P-body in each cell is continuously contacted along the entire strip length, rather than locally in the case of a cell design. This results in virtual immunity of the parasitic bipolar transistor from undesirable turn-on by minimizing the parasitic base resistance (R_b) under the N+ source and also ensuring the source is always shorted to the P- body. The stripe versus cell structure for the two technologies in question is shown in Figure 1, along with a cross-section of a power MOSFET illustrating the inherent parasitic bipolar transistor.

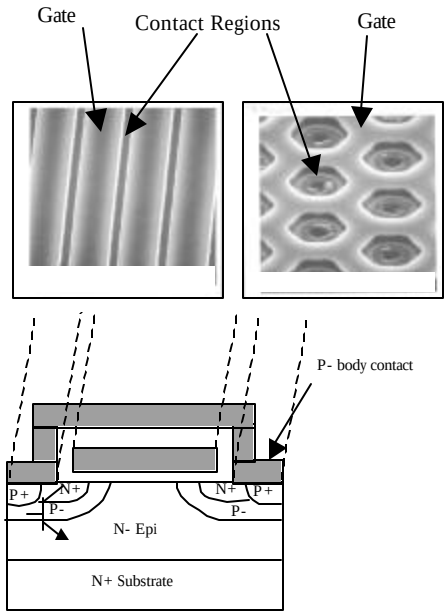

Figure 1. Photo of stripe versus cell topologies and cross-section of power MOSFET showing parasitic bipolar transistor.

3. ELECTRICAL RESULTS

3.1 *R.A* Product

The specific on resistance or *R.A* product for the new technology is plotted in Figure 2 versus rated breakdown voltage. All values are normalized to the old cell technology and measured at a gate drive voltage of Vgs=10V. Package resistance has been

subtracted from the measurements to give the true capability of the technology.
The new generation technology results in a significant decrease in *R.A* product, especially at lower voltages. The same improvements were observed at both 25°C and 175°C. The smaller cell geometry of the new planar stripe technology contributes to an increase in channel width per unit area (optimized W/L), resulting in a lower $R_{DS(on)}$. In general however, as voltage increases, this effect decreases due to the dominance of the N- drift region on $R_{DS(on)}$. At room temperature, the net result is a reduction in die size by about factor of two across the voltage ranges investigated.

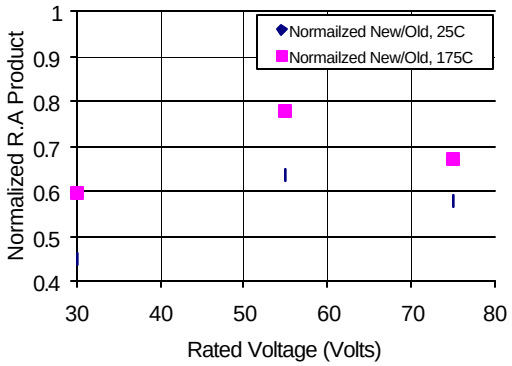

Figure 2. Normalized R.A product versus rated breakdown voltage. Measurements have been made at Vgs = 10V and package resistance has been subtracted.

3.3 Ruggedness.

Figure 3 shows single pulse avalanche energy versus $R_{DS(on)}$ for numerous technologies. All devices are 55V and approximately the same die size. We can see from the graph that the IRF1405, fabricated on the new stripe planar technology, shows almost a factor of 5 increase in single pulse avalanche energy over IR's previous technology, while still maintaining lowest $R_{DS(on)}$.

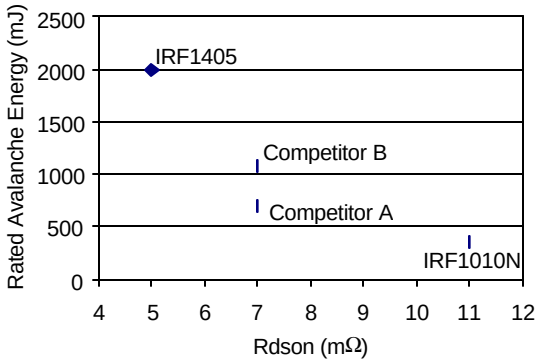

Figure 3. Rated avalanche energy versus $R_{DS(on)}$, illustrating high ruggedness and low $R_{DS(on)}$ for equivalent die sizes.

The next section expands on the above analysis and presents a scheme to reliably rate devices under repetitive avalanche conditions.

4. REPETITIVE AVALANCHE RATING

4.1 Avalanche Failure Mechanism

Two failure modes are normally prevalent during an avalanche condition. The first, and most destructive, is "bipolar latching". This failure occurs when the currents through the device result in sufficient voltage drop across the internal device resistance Rb' to cause transistor action and latching of the parasitic bipolar structure inherent in Power MOSFET's (see Figure 1). The second failure mode is purely thermal and occurs when the avalanche condition is allowed to raise the device temperature sufficiently high over the rated maximum to create a local mesoplasma [1].
As stated above, IR's new planar stripe technology is virtually immune to "bipolar latching" failure during avalanche. Figure 4 experimentally demonstrates this [2] showing actual destruct avalanche current for a 4mΩ, 40V, IRF1404 device plotted versus junction starting temperatures for various inductor values.

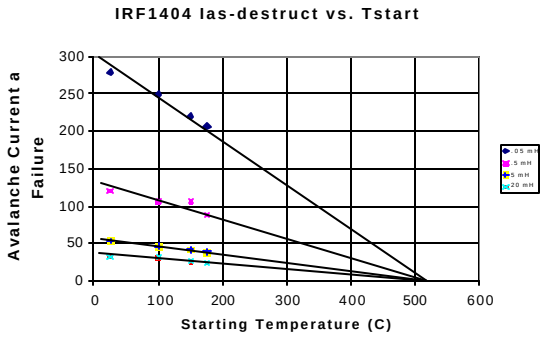

Figure 4. I_{as}-destruct versus Tstart for IRF1404.

Observe that the destruct lines behave linearly and extrapolate to zero device capability at a very high temperature (well in excess of rated T_{jmax}) consistent with mesoplasma formation.

4.2 Safe Repetitive Avalanche Specification

Traditionally, power MOSFETs are single pulse avalanche energy rated across a broad range of current and temperature, under varying circuit conditions. This often gives the designer little information on how the part will perform in a real circuit and very little information is provided on repetitive use in avalanche. The following section illustrates how single pulse or repetitive avalanche conditions are limited only by maximum drain current (I_{dmax}) and thermal considerations (ie: T_{jmax}). Additionally, a useful curve is provided from which maximum safe avalanche conditions can be determined under any set of operating conditions.

As an example, we use an IRF1404 to drive an inductive load such as a solenoid with high resistance ($R_{solenoid}$ = 2.5Ω) and inductance L = 2.0mH (see [3] for standard UIS circuit and schematic). Consider that T_{jmax} reaches no more than 150°C (inclusive of conduction state). When the solenoid fires at a frequency of 450Hz the inductive "kick" results in an avalanche current pulse. Hence, for Vdd = 13V and $R_{DS(on)}$.= 4mΩ,

$$R_{Total} = R_{solenoid} + R_{DS(on)} \qquad [1]$$

giving R_{Total} = 2.504Ω. Therefore,

$$I_{av} = \frac{V_{dd}}{R_{Total}} = 5.2\,\text{A}$$

The avalanche energy can be calculated from

$$E_{as} = \tfrac{1}{2} \times L \times I_{av}^2 \qquad [2]$$

and average power dissipated due to avalanche can be calculated from

$$P_d = E_{as} \times f \qquad [3]$$

where f is frequency.

Combining [2] and [3] and substituting for the above circuit conditions gives

P_d = 12.13 Watts. [4]

The average time in avalanche, t_{av}, is given by [3]

$$t_{av} = \frac{L}{R_{Total}} \cdot \ln\left[\frac{I_{as} \times R_{Total}}{(1.3BV_{Rated} - V_{dd})} + 1\right] \qquad [5]$$

Hence t_{av} = 0.22ms

The duty cycle is

$$D = t_{av} \times f = 10\% \qquad [6].$$

The average rise in junction temperature is given by

$$\Delta T_j = P_d \times Z_{th} \qquad [7]$$

where Z_{th} is the transient thermal resistance of the device. In this case, Z_{th} is read from the IRF1404 datasheet, using D = 10% and assuming the case of pulse-width equal to inductive fall time. Therefore, using Z_{th} = 0.11°C/W, we can calculate

$$\Delta T = 1.33°\text{C} \qquad [8].$$

Hence, the final junction temperature is given by

$$T_J = T_{j\max} + \Delta T = 151.3^\circ\text{C} \quad [9]$$

Since rated T_{jmax} of 175°C is not exceeded, safe operation results.

To provide for an easy, graphic solution inclusive of the thermal calculation, a convenient table is now included in the datasheet (see Figure 5).

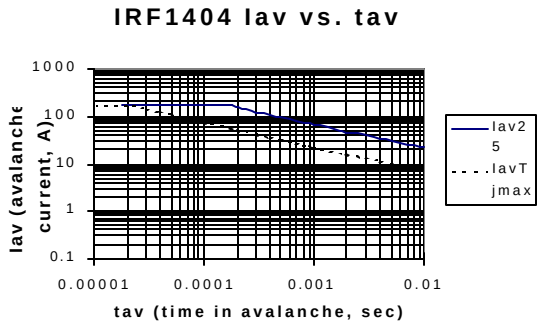

Figure 5. Curve of I_{av} vs. t_{av} for IRF1404

From this chart it is only necessary to know avalanche current I_{av}, time in avalanche t_{av}, and the temperature before avalanche pulses are imposed. In the example above it can be seen that the combination of .00022 sec and 5.2 A at 150C indicates a point well to the left of the "Iav 150" line, or in the region of safe operation.

5. SUMMARY AND CONCLUSIONS

This paper has presented an extremely rugged stripe planar MOSFET technology with ultra-low $R_{DS(on)}$ and extreme ruggedness. The technology demonstrates a factor of 2 improvement in $R_{DS(on)}$ and a factor of 5 improvement in single pulsed avalanche capability over the previous generation. Furthermore, the technology has been qualified to Q101 quality standard.

The paper also demonstrates ruggedness of the technology by presenting a technique to safely rate the devices under repetitive avalanche conditions. This technique is independent of test conditions and allows the designer to safely rate devices using only avalanche current I_{av}, time in avalanche t_{av}, and the temperature before avalanche pulses are imposed.

References

[1] A.C. English, "Physical Investigation of the Mesoplasma in Silicon," IEEE Transactions on Electron Devices, ED-13, No. 8/9, pp 662-667 (1966).

[2] Stoltenburg Rodney R., "Boundary of Power-MOSFET, unclamped inductive-switching (UIS, avalanche current capability)", APEC IEEE 1989 Conference proceedings, pp. 359-364.

[3] Application Note AN-1005, International Rectifier, http://www.irf.com.