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# MOSFET TECHNOLOGY ADVANCES DC-DC CONVERTER EFFICIENCY FOR PROCESSOR POWER

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**Abstract**
The trade-off between on-resistance ($R_{dson}$) and gate-drain charge ($Q_{gd}$) inherent in the unit cells of all commercially available MOSFET technologies has limited the performance of DC-DC converters for processor power. In this paper, a new trench MOSFET technology that effectively decouples the on-resistance and gate-drain charge of the MOSFET unit cell is presented. The result is an optimized chipset with the lowest $R_{dson}$ X gate charge product (132mΩ-nC) and the lowest $R_{dson}$ X $Q_{switch}$ product (34mΩ-nC), industry accepted figures of merit for MOSFET's used in DC-DC converters. The MOSFET's manufactured using this technology enable benchmark efficiency levels in a wide range of circuit topologies.

## Introduction

Power management efficiency, density and reliability requirements are being pushed to higher levels by the explosive growth of Internet. Wider bandwidth channels are now being used for data transmission along with power hungry CPUs for faster processing of that information. Newer GHz class processors need higher current and lower voltages than the previous generation. Even in telecom and networking industries, which use high current isolated converters, the output voltage of the converter may go down to as low as 1.5V to power the next generation of broadband equipment, where the ASIC is expected to operate at this low voltage. Under all these conditions, synchronous rectification is necessary to reduce power dissipation and maintain the required efficiency level. Further, these high current requirements in both industries need to be met without using additional real estate on the PCB. Consequently, the DC-DC converter not only needs to increase its power level and efficiency but also provide all that in the same or smaller form factor. To satisfy these stringent needs of the near future, a new trench MOSFET technology developed at International Rectifier using a proprietary manufacturing process is presented in this paper. MOSFET's manufactured using this technology achieve the lowest $R_{dson}$ x gate charge product (and $R_{dson}$ X $Q_{switch}$ product) <u>simultaneously</u> with a lower $R_{dson}$ x Active Area product, industry accepted figures of merit for MOSFET's used in DC-DC converter topologies.

## Current MOSFET Technology

In order to appreciate the advantages offered by the proposed trench MOSFET technology, the power losses associated with the FET's in a Synchronous Buck (sync buck) converter need to be examined. These losses can be estimated using the following set of equations [1],

$$Pon = I^2_{rms} \; x \; R_{dson} \qquad (1)$$

$$Psw \; @ \; V_{in} \; x \; (Q_{gd} + Q_{gs2}) \; x \; fs \; x \; I_{out}/I_g \qquad (2)$$

$$Pgd \; @ \; Q_g \; x \; V_g \; x \; fs \qquad (3)$$

$$P(Q_{oss}) \; @ \; 1/2 \; x \; (V_{in} \; x \; Q_{oss} \; x \; fs) \qquad (4)$$

$$P(Q_{rr}) = V_{in} \; x \; Q_{rr} \; x \; fs \qquad (5)$$

Note that Equation 2 does not apply to the sync FET as it undergoes zero voltage switching and Equation 5 does not apply to the control FET as its body diode never conducts in the continuous conduction mode of the sync buck converter. Pon is the conduction loss, Psw is the total switching loss, Pgd is the gate drive loss and $P(Q_{oss})$ is the power loss associated with the output charge ($Q_{oss}$) and $P(Q_{rr})$ is the diode reverse recovery losses. $Q_{gd}$ is the gate-drain charge, $Q_g$ is the total gate charge and $Q_{gs2}$ is the post threshold voltage gate-charge. The sum of $Q_{gs2}$ and $Q_{gd}$ is also referred to as $Q_{switch}$. $I_{rms}$ is the root mean square current through each FET, $V_{in}$ is the input voltage, $I_{out}$ is the output current, $I_g$ is the gate current during switching and fs is the converter switching frequency.

In a sync buck converter, the switching losses (sum of all frequency dependent losses) in the control fet are comparable to its conduction losses (Pon). However, for the sync FET, the conduction losses are the dominant component of the total loss as it undergoes almost zero voltage switching. Further, at switching frequencies of 250kHz-300kHz, the gate drive losses are small for both the control and the sync FET's. For the control FET, the planar DMOS technology is the popular choice (despite its higher $R_{dson}$ X Active Area product than trench technology) due to its low $R_{dson}$ X $Q_{switch}$ product while for the sync FET, the trench technology is popular due to its lower $R_{dson}$ X Active Area product. A low channel density conventional trench fet may also be used for the control FET, however, at the expense of a higher $R_{dson}$ X Active Area product. This is undesirable as it translates into a bigger chip to deliver the same performance as the chip manufactured using the planar DMOS technology. In the past two years, technologies targeted specifically for control and sync FET sockets were introduced by International Rectifier that have set the standard for DC-DC converters. The planar stripe DMOS technology optimized for the control FET socket has the industry lowest $R_{dson}$ x $Q_{switch}$ product of 50mΩ-nC while the trench FET technology optimized for the sync FET socket has the industry lowest $R_{dson}$ x Active Area product of 35 mΩ-mm$^2$. To reduce the power losses in the control FET, a technology with a $R_{dson}$ x $Q_{switch}$ product less than 50mΩ-nC is needed and to reduce the power losses in the sync FET, a technology with a $R_{dson}$ x Active Area product less than 35 mΩ-mm$^2$ is needed, while maintaining a low total gate charge.

It was realized that merely adopting the popular market trend of packing more MOSFET cells per unit area to maximize the channel density was not sufficient to reduce the sync FET power losses. The reason for this is explained below. In addition to the conduction losses, the sync FET also has the associated gate drive losses (Pgd) that are directly proportional to its gate charge as given by Equation 3. The gate charge ($Q_g$) of the MOSFET increases linearly with the number of cells per unit area while the $R_{dson}$ reduces sub-linearly with the number of cells per unit area. This is because, of the total $R_{dson}$, the channel component (which is inversely proportional to the number of cells per unit area) is only about 20%-40% depending on the channel length. Hence, more cells per unit area always increase the $R_{dson}$ X $Q_g$ product. In other words, for a part with the same $R_{dson}$ manufactured using a higher cell density technology, the $Q_g$ will be higher than the part manufactured using the lower cell density technology. This will increase the gate drive losses, which is undesirable. The gate drive losses, although low (but not insignificant) for the current switching frequencies of 250kHz-300kHz, would become significant as the operating frequencies are pushed into the 1-2 MHz range in the near future. Further, the maximum gate charge of the sync FET is also constrained by the limited drive currents of the IC which impose an upper limit on the channel density. Therefore, to avoid the situation where the existing control IC/drivers find it difficult to drive the future very high density trench designs, and to reduce the gate drive losses at high operating frequencies, the future sync FET trench technology needs to reduce the gate charge per unit cell.

Similar concerns are valid for the use of higher density designs in the control FET socket as well. The $Q_{switch}$ ($Q_{gd}$+$Q_{gs2}$) of the MOSFET increases linearly with the number of cells per unit area while the $R_{dson}$ reduces sub-linearly with the number of cells per unit area. Hence, more cells per unit area always increase the $R_{dson}$ x $Q_{switch}$ product. This is glaringly obvious in case of the trench technology, with its 3 X increase in channel density has 72% higher $R_{dson}$ X $Q_{switch}$ product compared to the planar DMOS technology. Therefore, to be able to use a high density trench technology for control FET's, their $R_{dson}$ X $Q_{switch}$ product needs to match or beat that product obtained from the planar DMOS technology.

Furthermore, in both the planar DMOS and trench technologies, there is a trade-off between $R_{dson}$ and $Q_{switch}$ that is fundamental to the unit cells of these technologies. This trade-off emerges because, in the unit cell, the thickness of the oxide in gate-drain overlap region is equal to the gate oxide thickness over the channel region as both these oxides are grown simultaneously during processing. To reduce the conduction losses (Pon), the gate oxide over the channel region is kept relatively thin so that the channel component of the $R_{dson}$ is reduced. Consequently, the oxide capacitance in the gate-drain overlap region is increased as it is inversely proportional to the oxide thickness. This increases the effective gate-drain capacitance, which is equal to the series combination of the oxide capacitance and the silicon depletion capacitance. Thus, the $Q_{switch}$ is unnecessarily increased, which in turn increases the switching losses (Psw) in the MOSFET, especially the control FET. Hence, the $R_{dson}$ and $Q_{switch}$ trade-off. Clearly, this coupling of $R_{dson}$ and $Q_{switch}$ through the gate oxide limits the $R_{dson}$ X $Q_{switch}$ product possible with the FET technology. With these ends in mind, focus of the research at International Rectifier shifted towards improving both $R_{dson}$ , $Q_g$ and $Q_{gd}$ per unit cell.

**New MOSFET Technology**

A unit cell cross-section of the conventional and the proposed trench MOSFET structures is shown in Figure 1. Significant structural changes were successfully incorporated into the unit cell of the proposed trench FET to break the $R_{dson}$ versus $Q_{switch}$ (and $Q_g$) trade-off that was described above. Using a proprietary fabrication process flow, the channel length is reduced and a thicker oxide is grown over the gate-drain overlap region along the bottom of the trench in comparison to the thickness of the gate oxide over the channel region along the vertical walls of the trench. Since, the trench bottom oxide (TBO) thickness is independent of the gate oxide thickness, a reduced effective gate-drain capacitance (and hence gate-drain charge) and a lower channel resistance are *simultaneously* achieved for the same cell density as the previous trench technology. An $R_{dson}$ X Active Area product of 26 mΩ-mm$^2$ now possible with this advanced trench technology is about 26% lower than the previous trench technology. In addition, the proposed technology also has a 27% lower $Q_g$ and 47% lower $Q_{switch}$ than the previous trench technology. Furthermore, the 34 mΩ-nC $R_{dson}$ x $Q_{switch}$ product possible with the proposed technology is about 31% lower than the $R_{dson}$ x $Q_{switch}$ product of the planar DMOS technology. It is worth pointing out that this improvement in the $R_{dson}$ x $Q_{switch}$ product also comes with a 60%

lower $R_{dson}$ x Active Area product implying that more efficient control FET's can be manufactured using this latest trench technology as demonstrated in the section on the in-circuit performance. This increase in efficiency along with die size reduction, when compared to the prior generation planar technology, leads to a smaller footprint thus saving the valuable onboard real estate.

In addition, due to the 27% reduction in $Q_g$ per unit cell, for the same total $Q_g$, higher density designs can now be used to further reduce the $R_{dson}$ and lower the conduction losses in the sync FET. Furthermore, high di/dt requirements of the next generation CPU's will necessitate the converters to operate with the switching frequency in the MHz range so that the size of the magnetics and other storage elements can be reduced to support the high di/dt. For these power supplies, FET's with low gate charge possible with the proposed technology will be needed to keep the gate drive losses low.

**Table 1.** Important parameters of the IRF7811W and IRF7822. Both the parts are rated for 30 V.

| **Parameter** | **IRF7811W (typical)** | **IRF7822 (typical)** |
|---|---|---|
| $R_{DS(on)}$ @Vgs=4.5 V | 9.0 mΩ | 5.0 mΩ |
| $Q_g$ | 18 nC | 44 nC |
| $Q_{SW}$ | 5.5 nC | 11.5 nC |
| $Q_{OSS}$ | 12 nC | 27 nC |

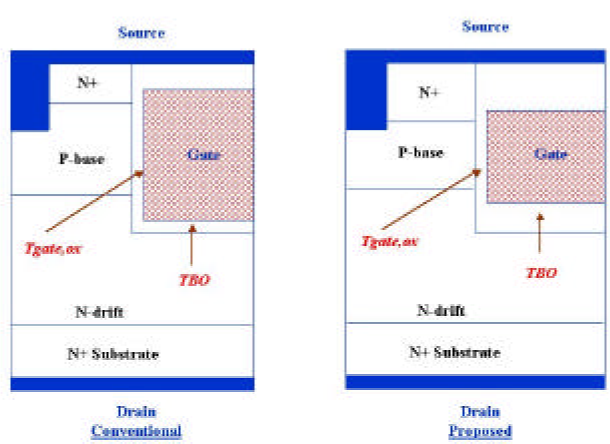


**Figure 1.** Unit cell cross-section of the conventional and the proposed MOSFET structure.

A chip set optimized for DC-DC converters was designed and manufactured using the proposed technology. The typical value of some of the more relevant parameters is shown in Table 1 below. The IRF7822 has been optimized for the sync FET socket while IRF7811W has been optimized for the control FET socket. It is worth pointing out that the IRF7811W can also be used as a sync FET in lower power applications depending on the target efficiency and power density required by the application. The in-circuit performance of this ultra efficient chip set is also discussed below.

**In-circuit Performance**

The in-circuit performance of the power MOSFET's was tested in a range of DC-DC converters using various circuit topologies under different operating conditions as described below.

***Topology 1. Single Phase Sync Buck DC-DC Converter***

Figure 2 illustrates an efficiency comparison between the new optimized wire bonded IRF7811W/IRF7822 chipset and the industry previous best *CopperStrap*™ IRF7811/IRF7809 chipset tested in a 2-device buck regulator with Synchronous Rectification operating at 300kHz, output voltage of 1.3V and input voltage of 14V. The circuit was configured with a single control FET and a single sync FET. At 15A output load conditions, the results show the new chipset has a distinct efficiency advantage of 2% over the *CopperStrap*™ MOSFET's. At peak efficiency the IRF7811W/IRF7822 chipset maintained its 2% advantage over the IRF7811/IRF7809 chipset.

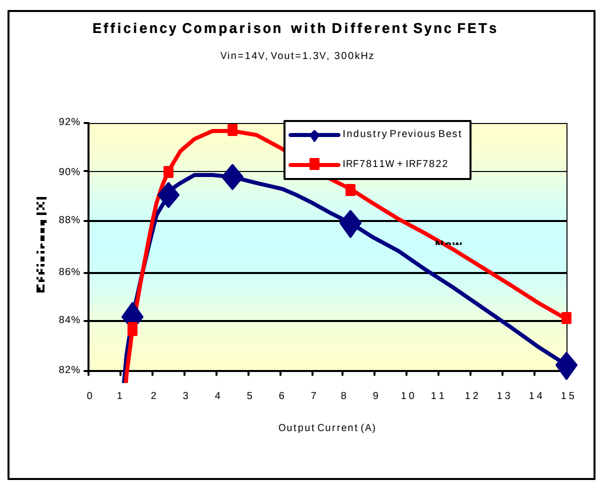


**Figure 2.** Efficiency comparison between the wire bonded IRF7811W/IRF7822 chipset and the *CopperStrap*™ IRF7811/IRF7809 chipset illustrating the better performance of the IRF7811W/IRF7822 chipset

***Topology 2. Multiphase Sync Buck DC-DC Converter***

In a multiphase sync buck converter, configured with 2-control FET's and 4-sync FET's per phase, the efficiency at full load of 6-IRF7811W's was 3.7% better than 6-IRF7811's as shown in Figure 3. This circuit was operating at 700kHz per phase, 12V input voltage and output voltage/current of 1.4V/35A per phase. Replacing the 4-IRF7811W sync FET's with 2-IRF7822 sync

FET's, the efficiency remained a very respectable 78.4% thus showing that the part count could be significantly reduced with minimal impact on the overall efficiency.

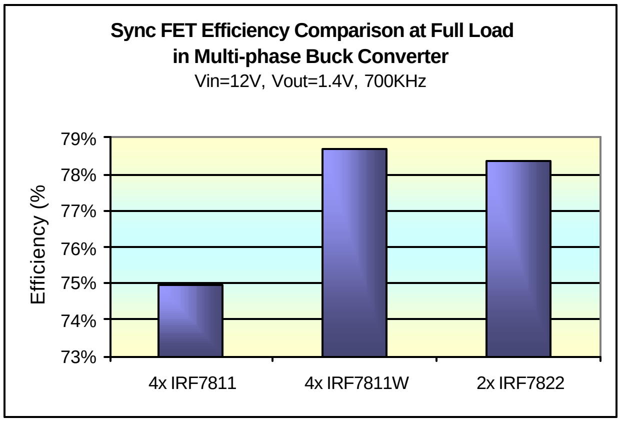


**Figure 3.** Efficiency Comparison in a multiphase buck converter, operating at Full Load, between 4-IRF7811s, 4-IRF7811Ws or 2-IRF7822s.

With the circuit operating at full load, the case temperature of the *CopperStrap™* IRF7811 was nearly 6°C hotter (at 90.4°C) than the wire bonded IRF7811W (see Figure 4). Since the junction to lead thermal resistance is higher for the wire bonded IRF7811W, a lower junction temperature demonstrates the reduction in the power losses in the sync FET brought about by the lower $R_{dson}$ X Active Area product of the proposed trench FET structure.

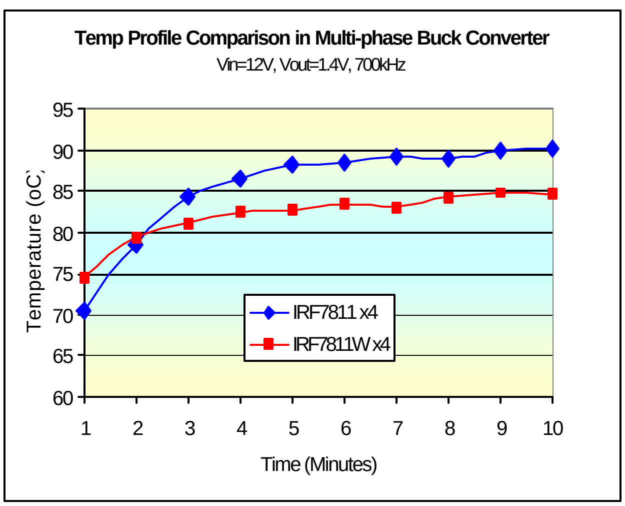


**Figure 4.** Temperature Profile Comparison in Multi-phase buck converter

A similar four-phase sync buck converter configured with 1-control FET and 2-sync FET's per phase was used to evaluate the performance benefits from the use of the proposed technology for control FET's. Comparative efficiency measurements were performed under identical operating conditions with Vin=12V and Vout=1.61V and with the <u>same set of sync FET's</u>. In one case, the control FET was the *CopperStrap™* IRF7811 manufactured using the planar DMOS technology and in the second case, the control FET was the IRF7811W manufactured with the proposed trench technology. The resulting efficiency curve, plotted below in Figure 5, shows about 0.5% higher peak efficiency and about 2% higher full load (60A) efficiency for the IRF7811W. In addition, the four IRF7811W control FET's were also running 6°C cooler, with the average junction temperature of 99.8 °C vs 105.7 °C , the average junction temperature of the four *CopperStrap™* IRF7811's. This demonstrates the reduction in the power losses in the control FET brought about by the lower $R_{dson}$ X $Q_{switch}$ product of the proposed trench technology.

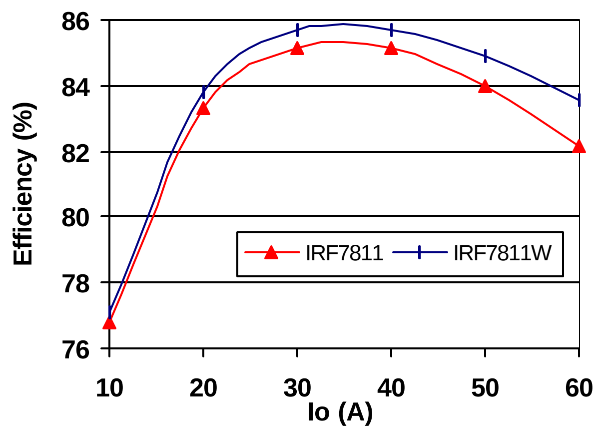


**Figure 5** Efficiency curves for a 4-phase sync buck converter comparing the control FET's manufactured using the Planar DMOS Vs the proposed trench FET technology

***<u>Topology 3. Isolated DC-DC Converter with Synchronous Rectification</u>***

6-IRF7822 MOSFET's were paralleled and used as synchronous rectifiers in an isolated single ended DC/DC converter. The measured efficiency was between 86% to 88% (see Figure 6) with output current in the range of 20A and 40A, output voltage of 1.5V and an operating frequency of 200kHz.

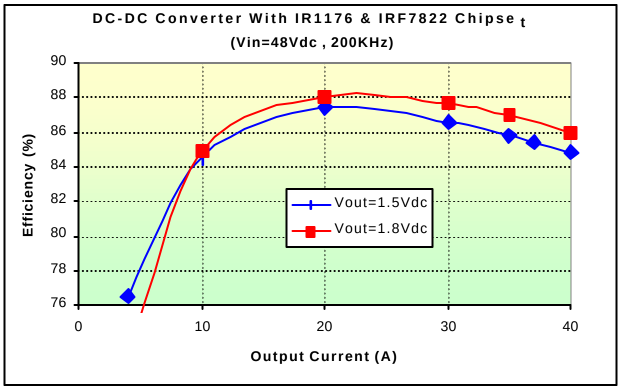


**Figure 6** Efficiency curves for an isolated DC/DC converter, where 6-IRF7822 MOSFET's per leg are used as Synchronous Rectifiers

## Conclusions

Up until now, the high density trench FET technology had not gained acceptance in the control FET socket due to its high $R_{dson}$ X $Q_{switch}$ product. This was shown to be due to the disproportional scaling of these parameters with channel density and the trade-off that exists between these parameters within the MOSFET unit cell. The new trench technology proposed and demonstrated in this paper effectively decouples the $R_{dson}$ and $Q_{switch}$ thereby breaking the trade-off. Consequently, more efficient and smaller footprint control FET's can now be manufactured using the proposed technology thus saving the valuable onboard real estate. In addition, the proposed technology simultaneously offers a lower $R_{dson}$ X gate charge product and a lower $R_{dson}$ X Active Area product than the best commercially available FET technologies for the sync FET. Consequently, higher cell density trench FET designs with a lower $R_{dson}$ can also be accommodate in the sync FET socket to reduce the conduction losses and keep in check the gate drive losses. The new IRF7811W/IRF7822 chipset manufactured using the proposed technology have set benchmark efficiencies, 3.5% higher in some applications and lower case temperature (about 6$^{o}$C in some applications) thus outperforming the previous best *CopperStrap™* IRF7811/IRF7809 chipset in several power supply applications.

## Acknowledgements

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[1] Ritu Sodhi *et. al* "Integrated Design Environment for DC/DC Converter FET Optimization", *Proc. International Symposium on Power Semicoonductor Devices and IC's*, pp. 241-244, *May 1999*