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Extremely Rugged MOSFET Technology with Ultra-low $R_{DS(on)}$ Specified for A Broad Range of E_{AR} Conditions

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ABSTRACT

An extremely rugged technology has been developed for ultra low $R_{DS(on)}$ applications. This paper describes a methodology of guaranteeing repetitive avalanche performance as long as maximum operating junction temperature, $T_{J(Max)}$, is not exceeded. The low $R_{DS(on)}$·A product and the inherent ruggedness of the technology, qualified to the Q101 quality standard, make it particularly suitable for automotive 42V bus applications. This paper specifically looks at the 42V integrated starter-alternator design and the impact of it's architecture on the performance of 75V power MOSFETs.

1. INTRODUCTION

The increase in power requirements in today's automobiles has forced auto manufacturers to consider higher supply voltages. The general trend is to move from the 14V bus towards a combined 42/14V bus. It is thought that high power loads (Electric Power Steering (EPS), Integrated Starter-Alternator (ISA) and Anti-lock Brakes (ABS), etc.) will run from the 42V bus, while some of the lower voltage systems (windshield wipers, power windows, etc.) will still run from the regular 14V rail. These new developments will place increased ruggedness requirements on today's power MOSFETs.

In tandem with the improvements in automobile design, power semiconductors have also been improved, trending towards lower $R_{DS(on)}$ and improved power handling. These technology advances have resulted in power semiconductor manufacturers making smaller die sizes for a given $R_{DS(on)}$, giving rise to lower cost and reduced size and weight, but also the undesirable effects of increased power densities and thermal resistances. Hence today's devices have achieved improved performance, but need to be even more rugged than before, and are sometimes required to withstand repetitive high voltage transients generated by *di/dt* and parasitic inductance. In fact, in the case of the integrated starter-alternator (ISA), 75V devices may even experience repetitive avalanche conditions during normal operation.

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International Rectifier has followed the above semiconductor trends and has developed an extremely rugged technology suitable for automotive applications of the future. The technology maintains ultra low $R_{DS(on)}$ and is qualified to the Q101 quality standard. The extreme ruggedness is demonstrated by guaranteeing the devices survive repetitive avalanche conditions under most circuit conditions, provided $T_{J(max)}$ is not exceeded.

This paper first introduces the technology and failure mechanisms. It then gives a brief summary of the device requirements for a 42V ISA design. The ruggedness requirements and the methodology behind a repetitive avalanche rating are then described.

2. DEVICE TECHNOLOGY AND FAILURE MECHANISMS

The technology has already been briefly introduced in a previous paper [1]. The devices are fabricated on an advanced planar stripe design, as opposed to a cell design (see Figure 1).

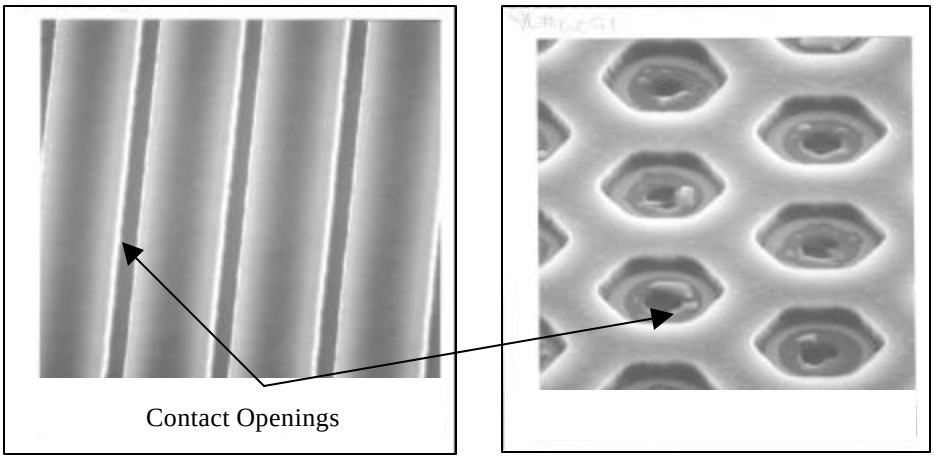

Figure 1. Planar stripe versus planar cell design. Note that both photos are to scale.

The planar stripe design significantly reduces, in fact almost eliminates, the likelihood of parasitic bipolar turn-on in the MOSFET. In Figure 2 we can see that parasitic bipolar turn-on can occur if a lateral current flow under the N+ source causes a voltage drop sufficient to forward bias the N+ source/P- base emitter junction (~0.7V). This can usually be avoided by shorting the N+ source to the P- base and minimizing the sheet resistance of the latter. However, in a cell design, if even one N+ source contact is poorly contacted, the resulting floating source is likely to cause the N+/P- junction to become forward biased, resulting in turn-on of the parasitic bipolar. In the case of a stripe design, the contact is opened along the entire length of the stripe (equal to the width of the die), so the N+/P- short is always present along some point of the stripe. Hence the N+ source is never floating in this case, virtually eliminating the likelihood of parasitic bipolar turn-on.

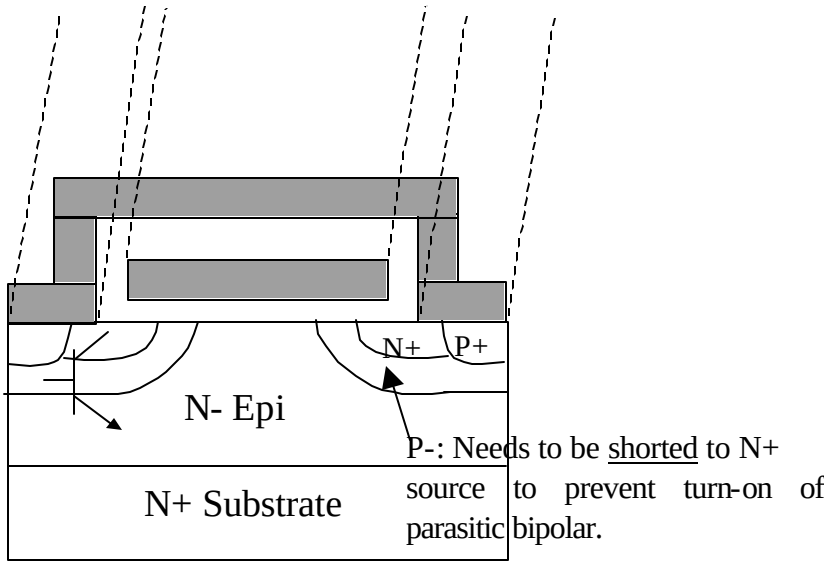

Figure 2. Power MOSFET cell cross-section, illustrating parasitic bipolar.

The new generation planar stripe FETs are therefore virtually immune to failure by turn-on of the parasitic bipolar. Therefore, it can be assumed that failure of the FETs is purely a thermal phenomenon, limited by the maximum junction operating temperature, $T_{J(Max)}$. This is verified and expanded in detail in the latter part of the paper.

3. THE 42V INTEGRATED STARTER-ALTERNATOR

As power requirements have increased in the automobile, it has become clear that the standard 14V bus is inadequate. Therefore, in order to meet the new power requirements, there has been a trend towards a 42V bus. A 42V integrated starter-alternator (ISA) has been one of the results of this trend, where the existing starter-motor and alternator are replaced by a single machine, integrated into the drive-train. Configurations vary depending on power requirements, from 6-12kW in Europe to 20-25kW in the USA, but the basic circuit topology is the same in all cases, that of a three-phase inverter. In the case of a 12kW load, the required current is approximately 300A. Hence, each inverter phase will most likely require paralleled MOSFETs. Furthermore, the inverter topology requires anti-parallel diodes to re-circulate the current during the off phase, requiring a robust, soft diode recovery. The preferred solution is to use the body diode of the MOSFETs.

During diode recovery, the voltage overshoot experienced across the device is given by

$$V_{RR} = L_S \frac{dI_R}{dt}, \tag{1}$$

where L_S is the lumped stray inductance and dI_R/dt is the reverse di/dt of the body diode. Hence, if L_S = 50nH and dI_R/dt = 800A/µs, we get V_{RR} = 40V. Therefore, the use of 75V devices in this 42V application could result in repetitive avalanche of the devices. Two ways to avoid avalanche overshoot is to use a softer body diode (lower dI_R/dt) or minimize the stray inductance L_S (L_S would need to be in the order of 20nH in the example above). Alternatively, 100V MOSFETs could be used to provide more overshoot headroom, however the higher $R_{DS(on)}$ associated with these parts (up to a factor of two) would mean larger die or more devices in parallel in order to meet the current requirements. This may be undesirable from a cost and system size point of view.

4. REPETITIVE AVALANCHE RATING

In today's harsh automotive environment, the performance demands on power MOSFETs have risen dramatically with increased power requirements. As seen above, the use of 75V FETs in a 42V system can result in repetitive avalanche of the devices. This is due primarily to high voltage transients generated by high di/dt and parasitic inductance.

Historically, IR datasheets specify single pulse avalanche energy (E_{AS}) versus junction start temperature at three different currents (see Figure 3). This allows the customer to predict the performance of the device under 'single shot' avalanche conditions. Repetitive avalanche (E_{AR}) has typically been specified as a single number, only under one set of circuit and temperature conditions. With the advent of the 42V automotive system, a need has clearly arisen to provide more information and rate parts under repetitive avalanche conditions. This issue has been addressed by guaranteeing the parts performance under repetitive avalanche conditions provided maximum junction operating temperature, $T_{J(Max)}$, is not exceeded.

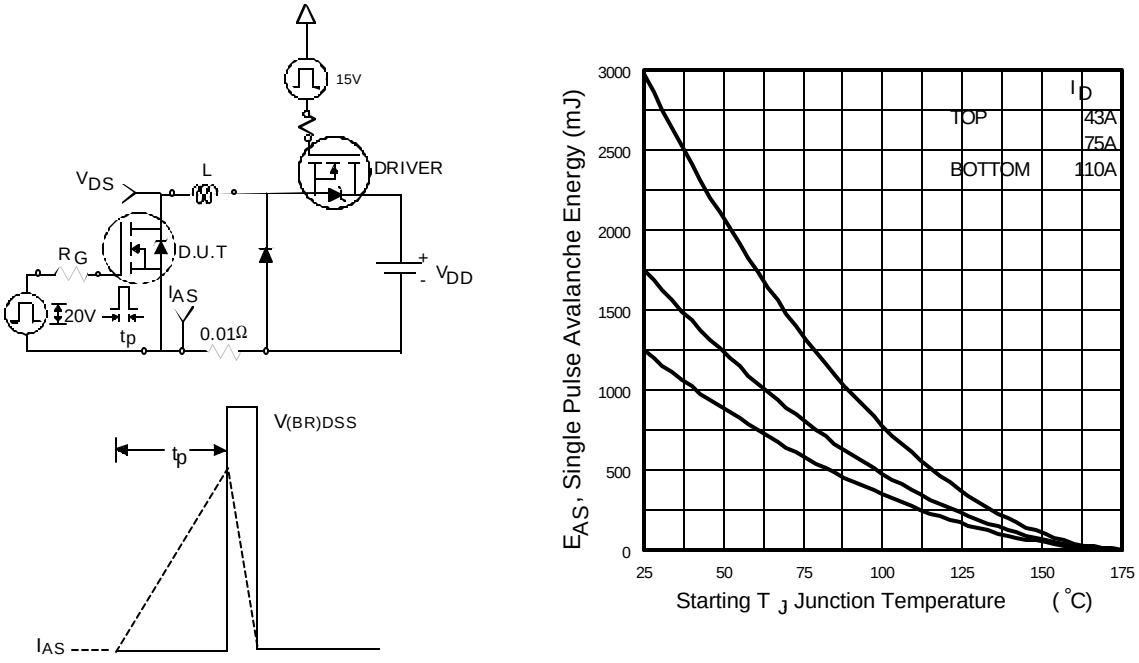

Figure 3. Test circuit diagram and single pulse E_{AS} rating curve (4.5mΩ, 75V, IRFP2907).

4.1 Repetitive Avalanche Rating Assumptions

The over-riding assumptions are that the failure mechanism is purely thermal and that $T_{J(Max)}$ is not exceeded during repetitive avalanche conditions. As will be seen below, for a purely thermal failure, actual failure will occur at a junction temperature far in excess of $T_{J(Max)}$.

The assumption of a purely thermal failure is reinforced by the ruggedness of the stripe technology design. As mentioned previously, turn-on of the parasitic bipolar is assumed highly unlikely and therefore, under most circuit conditions, failure will be purely thermal. This is verified for every part by generating a set of curves similar to those shown in Figure 4. Figure 4 plots single pulse avalanche fail current (I_{fail}) versus starting junction temperature for various values of inductor. As inductance increases, time in avalanche increases and therefore I_{fail} decreases. Note that a straight line fit to each curve for a given inductor results in convergence at a common temperature point[2]. This common temperature is thought to be close to the temperature at which silicon goes intrinsic, and far exceeds the maximum operating junction temperature, $T_{J(Max)}$. This straight line behavior of the avalanche fail current versus temperature indicates that the failure mechanism is thermal [2], and not dependent overly on any other mechanisms such as parasitic bipolar turn-on.

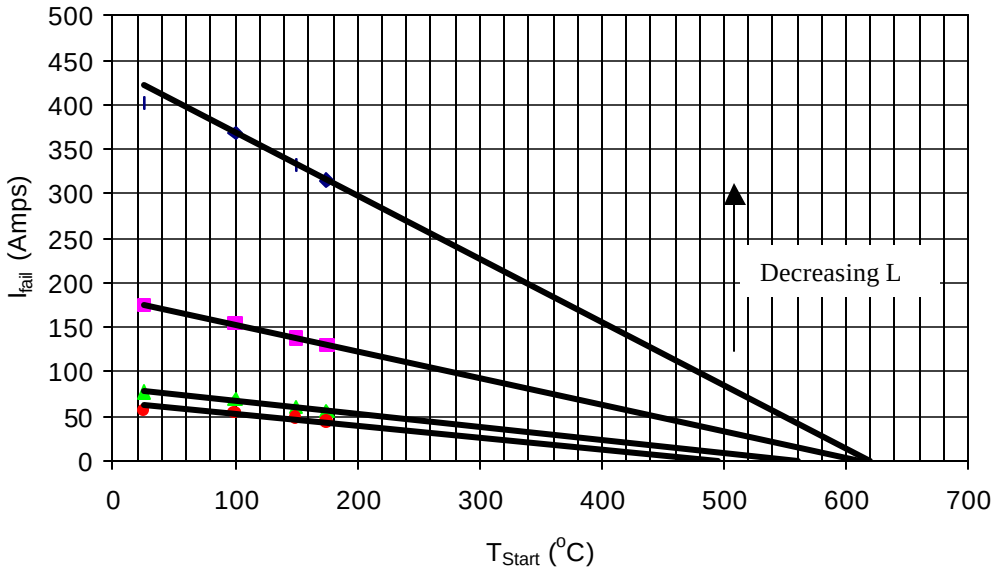

Figure 4. Single pulse avalanche fail current versus starting junction temperature for various values of inductor (4.5mΩ, 75V, IRFP2907).

[2] Note that the point of intersection varies significantly with the accuracy of the straight line fit. A first order approximation puts the convergence point somewhere between 500-600^{o}C. This is close to the silicon intrinsic temperature and far in excess of $T_{J(Max)}$.

5. REPETITIVE AVALANCHE SOA CURVE

A repetitive avalanche SOA curve can be generated knowing the transient thermal resistance $Z_{q\,jc}$, an allowable rise in junction temperature ΔT (not to exceed $T_{J(Max)}$), the time in avalanche t_{av} and the avalanche duty cycle D. The average power dissipation, $P_{D(ave)}$, during an avalanche event is given by

$$P_{D(ave)} = \frac{1}{2}\left(1.3BV \cdot I_{av}\right) = \frac{\Delta T}{Z_{q\,jc}}, \tag{2}$$

where BV is the rated breakdown voltage and I_{av} is the allowed (safe) avalanche current for a given rise in temperature ΔT. The factor '1.3' accounts for the rise in breakdown voltage during the avalanche event. Hence,

$$I_{av} = \frac{2\Delta T}{1.3BV \cdot Z_{q\,jc}}. \tag{3}$$

Note that the transient thermal resistance $Z_{q\,jc}$ is a function of avalanche duty cycle D and time in avalanche t_{av} and can be read directly from curves on the datasheet. An avalanche energy can therefore be calculated using

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}. \tag{4}$$

Note that equation (4) may be used for both single pulse or repetitive conditions, depending on the specified value of $Z_{q\,jc}$.

Equation (3) can therefore be used to generate a repetitive avalanche SOA curve. Note that this curve accounts for an allowed rise in temperature ΔT due to avalanche losses only. The system designer should estimate the junction operating temperature and account for any additional rise in temperature due to other losses. This value should be used as a starting temperature T_{Start} in the specific system and equation (5) can then be used to calculate the additional rise in temperature due to repetitive avalanche conditions.

$$\Delta T = T_{Final} - T_{Start}. \tag{5}$$

Note that the worst case rise in temperature allowed is given when $T_{Final} = T_{J(Max)}$. Figure 5 shows a repetitive avalanche SOA curve (safe avalanche current versus time in avalanche for a given duty cycle) for a rise in junction temperature of 25°C. A more detailed mathematical analysis is presented in [3].

Note that the single pulse curve given in Figure 3 is fully consistent with the single pulse duty cycle curve of Figure 5. Looking at Figure 5, we can see that for a current of 110A, t_{av} = 6*E*-6sec. Using equation (2),

$$P_{D(ave)} = \frac{1}{2}(1.3 \times 75 \times 110) = 5362.5\,\text{W}.$$

Hence, using equation (4),

$$E_{AS(AR)} = 5362.5 \times 6E-6 = 32\,\text{mJ}.$$

This value corresponds to the E_{AS} value read from Figure 3 assuming a starting temperature of T_{Start} = 150°C and an avalanche current of 110A. Furthermore, the curve in Figure 3 can be reproduced for the repetitive case using the same methodology. This is illustrated in Figure 6. Note that in the case of Figure 3 and Figure 6, the starting junction temperature corresponds to a value which will allow a rise up to $T_{J(Max)}$ = 175°C, whereas Figure 5 allows an arbitrary 25°C rise.

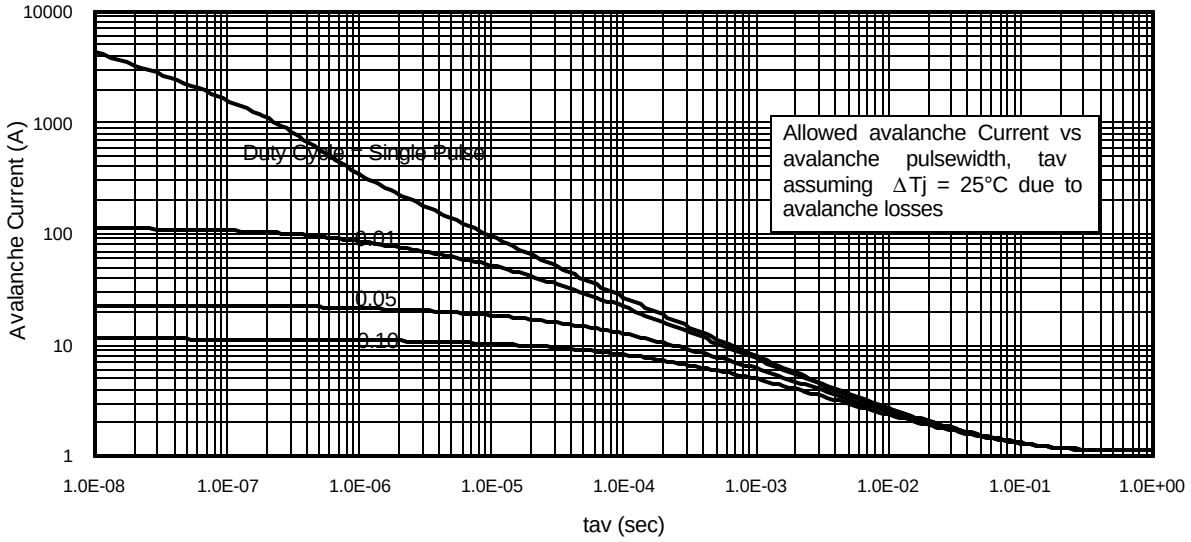

Figure 5. Repetitive avalanche SOA curve, showing safe avalanche current versus time in avalanche for a given duty cycle.

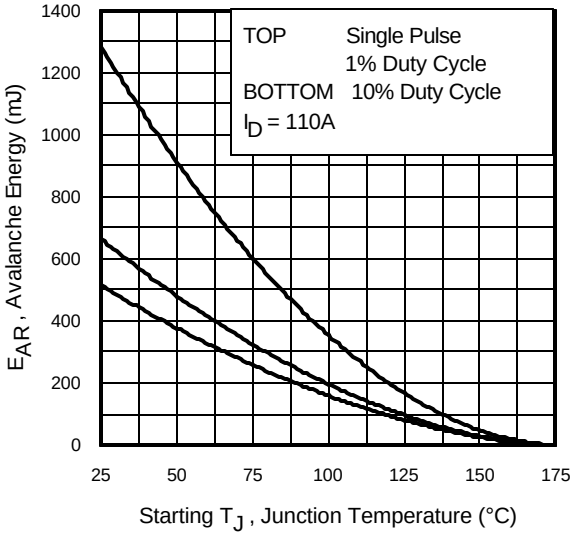

Figure 6. Repetitive avalanche energy versus starting junction temperature for varying duty cycle *D*.

Note also that the 'top' single pulse curve in Figure 6 is the same as the 'bottom' 110A curve in Figure 3. Figure 6 thus illustrates the de-rating of avalanche energy due to the repetitive duty cycle.

6. CONCLUSIONS

This paper has presented an extremely rugged, Q101 qualified technology suitable for 42V bus automotive applications. The technology is virtually immune to parasitic bipolar turn-on, and it has been demonstrated that the avalanche failure is a purely thermal phenomenon, occurring at a temperature far in excess of $T_{J(Max)}$. As repetitive avalanche is a possibility when 75V devices are used in a 42V automotive system, for example integrated starter-alternator (ISA), a technique for guaranteeing and rating parts under repetitive avalanche conditions has been presented. This gives the user a technique for estimating the safe avalanche current for an allowable rise in junction temperature. It is assumed that $T_{J(Max)}$ is not exceeded during the avalanche event.

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[2] R. R. Stoltenburg, "Boundary of Power-MOSFET, Unclamped Inductive-Switching (UIS), Avalanche Current Capability", in *IEEE Proceedings of APEC 1989*, pp. 359-364, 1989.
[3] Application Note AN-1005, International Rectifier