

New Materials and Technologies Solve Hermetic SMD Integration

Tiva Bussarakons, International Rectifier, Inc., El Segundo, California

Hermetic semiconductor SMDs (surface-mount devices) can now be successfully and economically integrated in most system designs because of the:

- Availability of low temperature coefficient of expansion (TCE) board materials
- Advances in materials
- Innovative SMD carrier designs
- Maturity of power module technology

Prior to these advancements, popularity of hermetic SMD semiconductor was hindered by the TCE incompatibility between the package and board materials and significantly wider operating temperature demands. The soldered interface of the assembly could crack when subjected to temperature extremes, i.e., after a soldering operation or after temperature cycling screens. *Figure 1* shows the packages that will be covered, the ceramic leadless chip carrier (CLCC), the SMD and the leaded TO-25X.

Generally, SMDs offer smaller size, lighter weight, and excellent thermal performance. In particular, they are widely used in high frequency applications because of their inherently low inductance and resistance. Even before the availability of low TCE board materials for hermetic SMDs, successful assembly integration of plastic SMDs was well established. This was possible because the plastic package's TCE was comparable to the industry's standard board materials, and the operating environments for most plastic SMDs was usually benign.

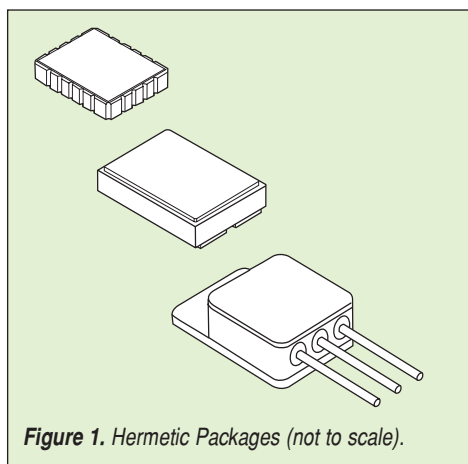


Figure 1. Hermetic Packages (not to scale).

Package Construction

The SMD package (*Figure 1*) differs considerably from its predecessor, the CLCC (ceramic leadless chip carrier) surface-mount package. One major difference is in the package base design. Whereas the CLCC uses tungsten feedthroughs, the SMD uses a thin piece of copper-tungsten (CuW) to minimize package thermal resistance. The SMD is typically a three-terminal device. While CLCC packages offer up to 40 terminals in larger sizes,

they are smaller and generally used in lower-current and lower-power applications. In contrast, SMD packages are larger and can accommodate larger die sizes. Combining this with their excellent thermal performance, SMDs find most of their use in higher-power applications.

A hermetic SMD semiconductor package consists of three terminal pads, ceramic housing, seal ring, and lid brazed together to form a hermetic, semiconductor die carrier. This SMD package is used in military and space applications, in which product reliability is imperative. As

illustrated in *Figure 2*, a semiconductor die is soldered to a large terminal pad. This is typically a drain terminal for a MOSFET or a cathode terminal for a rectifier. It also serves as a thermal path to an external heat sink. The other two, smaller pads are gate and source terminals for a MOSFET or anode terminal(s) for a rectifier. To optimize the package's integrity, its materials are carefully chosen to closely match the silicon die's

Hermetic SMDs are the choice for designs requiring smaller size, lighter weight, excellent thermal performance, cleaner switching waveforms, and higher circuit efficiency.

TCE, which is 4.2 ppm/°C. Table 1 lists the TCEs of these materials.

Package Comparison

Each SMD package is designed to accommodate a specific die size. Package piece parts are shaped to eliminate excess material without compromising mechanical integrity. This results in the smallest, lightest package possible. Terminal pads are solid CuW. The thin structure of the drain pad (in case of a FET) represents a very short thermal path from the heat source (die) to an external heat sink. Combined with the outstanding thermal conductivity property of CuW, the package produces a very low thermal resistance path, thus a very low package junction-to-case thermal resistance (θ_{JC}). Performance of various SMD and leaded (TO-254, TO-257 and TO-258) devices are tabulated in Table 2.

The following analyses are based on the same die size for each of the package comparisons. The die sizes are noted in Table 2. SMD 0.5 is the smallest SMD package in production today and is normally used in place of the TO-257. SMD 1 is about twice the size of the SMD 0.5 and is comparable to the TO-254. SMD 2 and SMD 3 are the largest packages of the series and are usually used in place of the TO-258. In all instances, the SMD devices are superior to their leaded counterparts with respect to weight reduction and footprint requirements. The packages' thermal resistances are comparable in all cases.

When integrating SMD devices to an assembly, TCE of the board/substrate material must be closely matched to SMD's TCE, typically within 2-3 ppm/°C to minimize mechanical stress and insure mechanical integrity. In addition, proper cooling must be provided to insure that the devices' operating junction temperatures are maintained below the desired level under the worst case condition. A device's thermal characteristics, θ_{JC} and θ_{JA} (junction-to-

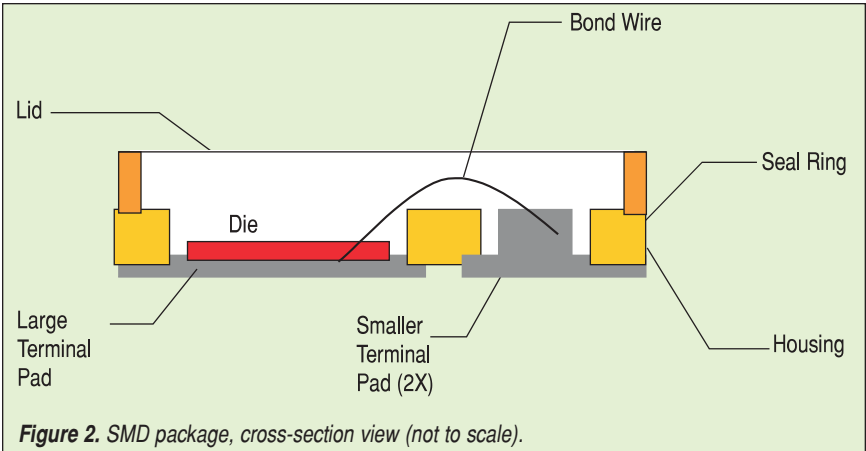


Figure 2. SMD package, cross-section view (not to scale).

SMD Elements	Material	TCE ppm/°C
Die	Silicon	4.2
Terminal Pads	CuW	6.0
Housing	Al ₂ O ₃	6.4
Seal Ring	Kovar	5.1
Lid	Kovar	5.1

Table 1. TCE property of SMD elements.

ambient thermal resistance) are essential and must be considered in the design process.

Low Power Designs

SMD and CLCC devices can be attached directly to the traditional FR-4 or polyimide p.c. boards. However, due to considerable TCE mismatch, this assembly integration is limited to smaller packages. To circumvent solder joint fatigue, many designers empirically limit the package size to a maximum of 0.5 in. in any one dimension.

For designs with larger SMD packages and/or with wide temperature extremes, low TCE board materials are the solution because of the availability of materials with a TCE of 7-9 ppm/°C. Other TCE control techniques for p.c. boards include the use of molybdenum, copper-invar-copper, or para-aramid fiber reinforcement as the board stiffener.

SMDs can be bonded to a board with a silver-filled epoxy or a soldering process. For an attachment using solder, eutectic alloys should be used. Preheating of the assembly prior to

Package	Typical Weight (gms)	Footprint Required (in. ²)	θ_{JC} (°C/W)
SMD .5	1.1	0.118	1.67 (1)
TO-257	7.0	0.340 (4)	1.67 (1)
SMD 1	2.6	0.281	0.83 (2)
TO-254	9.3	0.521 (4)	0.83 (2)
SMD 2	3.3	0.362	0.42 (3)
SMD 3	3.4	0.387	0.42 (3)
TO-258	10.9	0.693 (4)	0.42 (3)

Notes:

- 1) With size 3 die (0.116W x 0.181-in.L)
- 2) With size 5 die (0.257W x 0.257-in.L)
- 3) With size 6 die (0.260W x 0.360-in.L)
- 4) Including lead length of 0.150-in.

Table 2. Mechanical and thermal performance data of SMD and leaded packages.

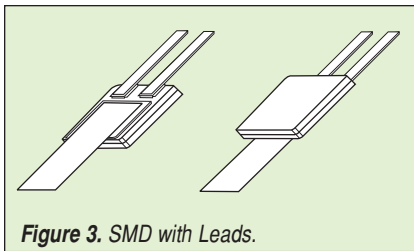


Figure 3. SMD with Leads.

soldering and allowing the assembly to cool naturally after a soldering process are highly recommended. Exposing SMD components to higher than 300°C may cause permanent damage.

Because FR-4 and polyimide board materials are poor thermal conductors, the p.c. board should not be considered as a thermal medium or heat spreader unless its copper traces are sufficiently large. Otherwise, cooling the semiconductor relies almost entirely on the package's ability to dissipate thermal losses in the free convection environment. The package's θ_{JA} then becomes the key design parameter.

For the aerospace environment where convection is nonexistent and radiation cooling is minimal, conduction is the only meaningful cooling method. For cooling, it may be necessary to attach an SMD to an on-board heat spreader or an enlarged copper trace.

For a device dissipating 1W with θ_{JA} of 25°C/W, the junction temperature equals 100°C for an 75°C ambient. This is based on:

$$P_D = \frac{(T_J - T_A)}{\theta_{JA}} \quad (1)$$

Where:

P_D = Device power dissipation

T_J = Operating junction temperature

T_A = Ambient temperature

θ_{JA} = Package junction-to-ambient thermal resistance

High Power Designs

For high-power applications where SMD devices dissipate more than a few watts and must be cooled with a heat sink, there are three basic assembly integration techniques. One

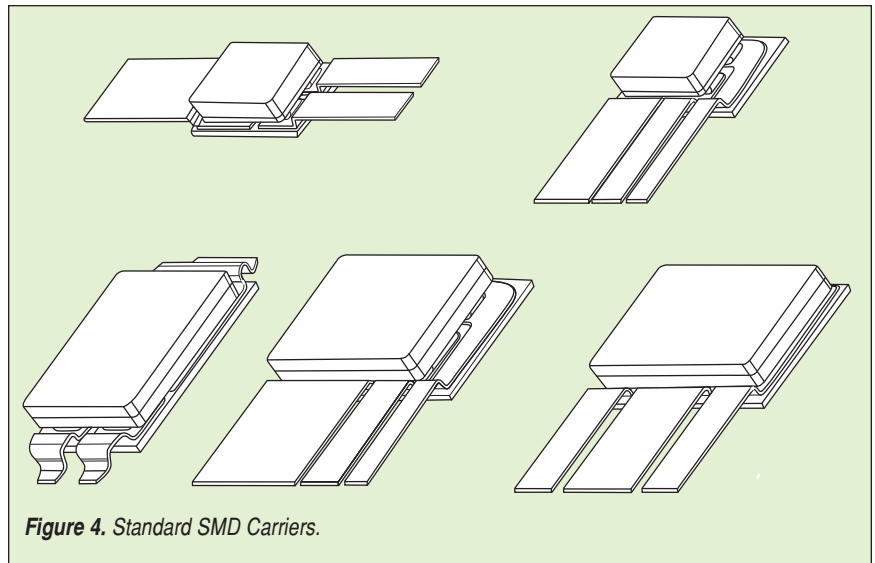


Figure 4. Standard SMD Carriers.

approach is the SMD with leads assembly technique, where the SMD is attached with flat copper leads for electrical connections. The SMD semiconductor is bonded to a heat sink or a heat spreader via its lid, using a thermally conductive epoxy or a thermal pad for cooling. The SMD semiconductor is electrically isolated from the heat sink because the lid is isolated from the die. The junction-to-lid thermal resistance for SMD 2 is about 6°C/W. Thermal resistance of the epoxy must be included when determining the total thermal resistance of the assembly. Figure 3 depicts a typical SMD with leads.

Another common assembly technique is to bond the leaded surfaces of the SMD semiconductor directly to a heat sink with a thermally conductive epoxy or thermal pad. Unless the bonding medium contains an insulating material, placing a thin layer of ceramic at the bonding interface will provide the required electrical isolation.

For assembly designs with one or two SMD devices, the SMD carrier is the solution to a cost-effective design. An SMD carrier is a leaded DBC (direct bond copper) substrate with three extended flat copper leads (one each for gate, drain, and source terminal as in the case of a MOSFET). The SMD semiconductor is soldered

to the carrier, providing an isolated ready-to-use SMD assembly. With its good thermal conductivity and excellent dielectric properties, the ceramic layer within the DBC provides the essential electrically isolated thermal path with negligible impact on the overall thermal performance of the assembly. Standard SMD carriers are shown in Figure 4.

Figure 5 illustrates a design implementation using SMD carrier assemblies. Here, all small-signal and low-power components are populated on a FR-4 or polyimide board and each SMD is attached to a carrier. The SMD carrier assemblies may be bonded to a common base with a thermally conductive epoxy or soldered directly to a low TCE base. The base or chassis is usually a thermally conductive metal such as aluminum serving as a cold plate or heat sink for the entire assembly. The low TCE base can be Al/SiC (aluminum/silicon carbide) or any material with a TCE in the range of 5-9 ppm/°C. Electrical connections from the carrier assembly to the board are made through the copper leads of the carrier. The overall assembly's junction-to-base thermal resistance (θ_{JB}) depends on the die size, substrate material, base material, and the substrate bonding method. For a carrier assembly with SMD 2 device using size 6 die, alumina (Al_2O_3) sub-

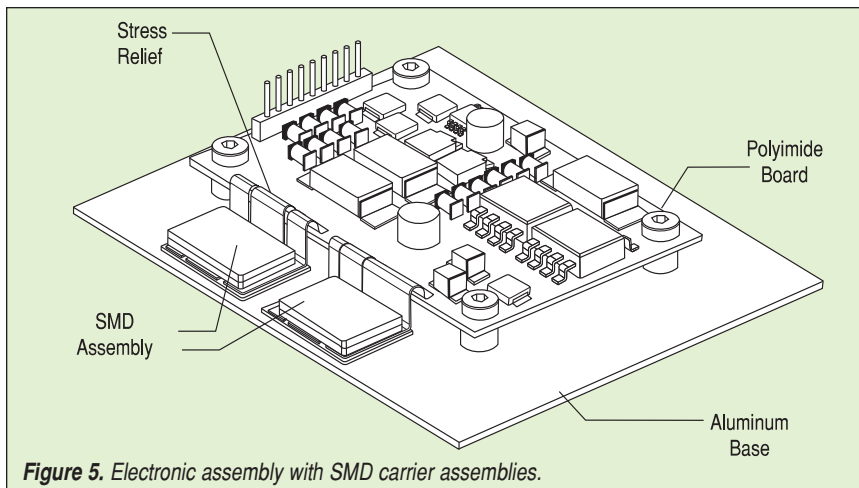


Figure 5. Electronic assembly with SMD carrier assemblies.

strate, Al/SiC base, and soldering process for the attachment, the θ_{JB} is about 0.7-0.8°C/W.

Power Module Assembly

A power module assembly is basically a large SMD carrier populated with any number of surface mount components. The assembly may include any surface mount semiconductor and passive components, i.e., capacitors, resistors, magnetic parts, etc. Unlike the previous assembly integration, however, all SMDs and associated components are populated on one or more DBC substrates. Similar to the traditional p.c. board, copper traces of the DBC substrate provide electrical connections for the components and its ceramic (alumina) interlayer provides the electrical isolation. More than 2000V isolation can be expected for 0.025-in. thick alumina. To complete the assembly, the DBC substrate is soldered to a base with a comparable TCE and a high thermal conductivity material that promotes the assembly's thermal conduction.

For most design applications, DBC Al_2O_3 is the substrate material of choice due to its reasonable thermal conductivity and its relatively low cost. Other substrate materials that have been used successfully include DBC AlN (aluminum nitride), and DBC BeO (beryllium oxide). These materials have excellent thermal conductivity and will provide a better

thermal performance than DBC Al_2O_3 . However, the cost of these materials is about three to five times that of the DBC Al_2O_3 for the same design. Though BeO is a hazardous material and its use is limited by a government agency, its low dielectric constant may be the solution for designs that require low assembly coupling capacitance.

Closely matched substrate, base, and the SMD semiconductor TCEs produce a complete assembly with sound mechanical integrity. This design/manufacturing approach is often referred to as 'Power Module' technology. The technology is now matured, but the cost of manufacturing a small quantity is high due to substantial capital investment in manufacturing equipment, nonrecurring assembly tooling costs and minimum buy of specialty materials. To reduce design time and system costs, designers generally subcontract the assembly design and manufacturing as the solution to the design integration. Other essential benefits of this design approach include design flexibility, excellent electrical performance, greater reliability, and ease of assembly integration.

Figure 6 shows a power module assembly with four SMD 1 devices. The assembly uses copper leads for electrical connections to other assemblies. The substrate is an AlN substrate and the base uses Al/SiC mate-

rial. Power module assembly offers a variety of assembly interface designs. Pins, terminals, standoffs, flex circuit, bus bars, and any custom interface terminals can be easily incorporated to facilitate the system design integration.

The conventional visual inspection method cannot be used for an assembly populated with SMD devices because the soldered connections are not visible. The approved inspection methods are x-ray, sonascan, and thermal response. If the inspection cannot be performed in-house, several independent laboratories have the proper equipment and will perform the required inspection for a fee.

Electrical Performance

The SMD's low package resistance and low lead inductance provide the best possible electrical performance, especially in switching applications. Table 3 shows the typical lead induc-

Lead Inductance TO-258	TO-257 TO-254 SMD 3	SMD 1 SMD 2
Drain (nH)	5 – 8.7	0.8 – 2
Source (nH)	8.7 – 15	2.8 – 4.1

Table 3. Device lead inductance data, SMD's vs. leaded packages.

tance of these devices as a result of internal bond wires and 0.25 in. of lead for a TO-25X package. SMD series resistance is extremely low, 1m Ω , compared with 5 m Ω or greater for the leaded TO-25X packages, resulting in lower $R_{DS(on)}$ for the SMD.

In switching applications, skin effect can cause ac losses in the package leads that are greater than the dc losses. Leads of a TO-25X package contain ferromagnetic materials and a magnetic field is generated as current passes through the leads. Eddy currents induced in a lead by the magnetic field cause skin effect. Skin effect causes current in a lead to flow only on the outer periphery of the leads. The depth of this annular conducting area is inversely proportional to the square root of the frequency^[1].

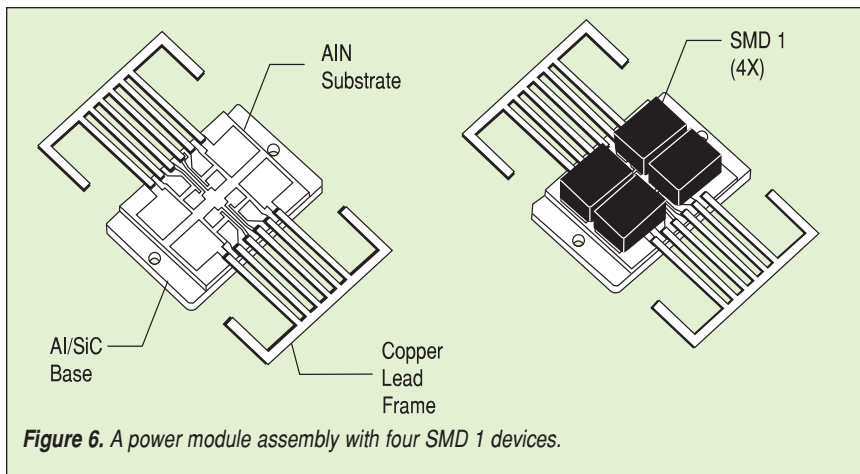


Figure 6. A power module assembly with four SMD 1 devices.

For a 40-mil diameter lead (wire size of TO-254), the ratio of ac to dc resistance at 50kHz is about 1.35. The ratio increases to 1.75 (~29%) as the frequency rises from 50kHz to 100kHz. The resistance ratio is also a function of the lead's diameter. The resistance ratio increases as the lead's diameter increases. Increasing the lead's diameter from 40 mils to 60 mils (TO-258), the ac resistance to dc resistance ratio increases by about

50% at the frequency of 100kHz^[1]. The ac losses will further reduce circuit efficiency.

In most assembly configurations, the SMD package lends itself to layouts where components are in close proximity, which allows short interconnections between circuits. This results in low-circuit resistance, low-circuit inductance and negligible ac losses that improve circuit efficiency and produce the best possible switch-

ing waveforms, which in some cases can eliminate the need for snubber circuits.

SMD Rework

Should replacement or realignment of an SMD be required, rework personnel may need a hot-air system with appropriate orifice masking to protect surrounding components. Pre-heating the assembly to within 50°C of the solder's melting temperature will facilitate the rework process. To avoid permanent damage to the SMD, the temperature must be carefully controlled and monitored when applying heat to the device.

Reference

1. A. I. Pressman, "Switching Power Supply Design," McGraw-Hill, Inc., New York, 1991.

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