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The Hermetic Surface Mount Device (SMD), Its Advantages and Solutions to Assembly Integration

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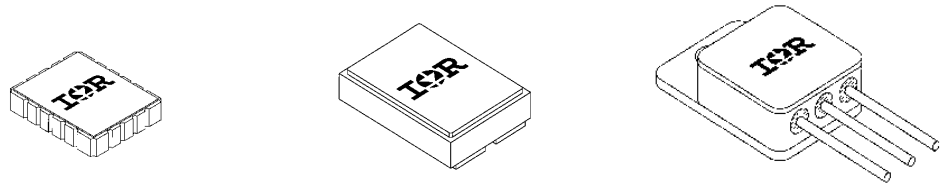
Introduction

Hermetic surface mount packages have been in existence for more than 15 years. While the leaded packages (TO-257, TO-254, etc.) continue to find their use in many current designs, a vast majority of new electronic equipment designs have been integrating the SMD packages due to smaller size, lighter weight, and the excellent thermal performance that the surface mount devices offer. Design engineers for high frequency applications particularly enjoy the inherently low inductance and low resistance these packages provide. In many instances, the SMD's are the absolute requirement.

Successful assembly integration of plastic SMD devices is well established because of the temperature coefficient of expansion (TCE) of the package is comparable to the industry's standard board materials, FR-4 and polyimide to which the devices are mounted. Additionally, the environments where most plastic SMD's are used are generally benign.

Unlike the plastic SMD, the popularity of the hermetic SMD devices has been somewhat hindered by the TCE incompatibility of the SMD package and the board materials, and significantly wider operating temperature demands. The soldered interface of the assembly can crack when it is subjected to temperature extremes, i.e., after a soldering operation or after temperature cycling screens. Solutions to the hermetic SMD assembly integration will be presented in this article. With the availability of low TCE (temperature coefficient of expansion) board materials, advances in materials, innovative SMD carrier designs, and maturity of the Power Module technology, the hermetic SMD devices can be now successfully and economically integrated in most of system designs. This article will focus on the new generation and more thermally efficient hermetic surface mount packages hereafter referred to as 'SMD'.

Figure 1 shows the packages that are discussed in the article, the ceramic leadless chip carrier (CLCC), the SMD and the leaded TO-25X.



CLCC SMD TO-25X

Figure 1. Hermetic Packages (drawing is not to scale)

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SMD Package Construction

The SMD package differs notably from its predecessor, the CLCC (Ceramic Leadless Chip Carrier) surface mount package. One major difference is in the package base design where the CLCC uses tungsten feed-throughs and the SMD uses a thin piece of copper-tungsten (CuW) to minimize the package thermal resistance. The SMD is typically a three-terminal device. The CLCC packages do offer up to 40 terminals in larger sizes. The CLCC packages are smaller and are generally used in lower current and lower power applications. The SMD packages are larger and can accommodate larger die sizes. Combining this with their excellent thermal performance, the SMD's find most of their use in higher power applications.

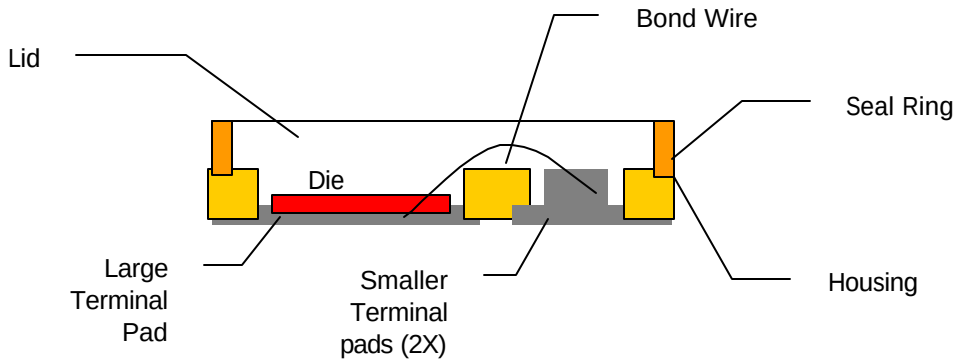

Figure 2. SMD Package, Cross-Sectional View (drawing is not to scale)

The hermetic SMD package consists of three terminal pads, a ceramic housing, a seal ring, and a lid. These parts are brazed together to form a hermetic, semiconductor die carrier. This SMD package is used in military and space applications where product reliability is imperative. As illustrated in Figure 2, a semiconductor die is soldered to a large terminal pad. This is typically a drain terminal for a MOSFET device or a cathode terminal for a rectifier. It also serves as a thermal path to an external heat sink. The other two smaller pads are gate and source terminals for a MOSFET device or anode terminal(s) for a rectifier. To optimize the package's integrity, the package materials are carefully chosen to closely match the TCE of the silicon die, which has a TCE of 4.2 ppm/°C. Table 1 shows the TCE property of these materials.

SMD Elements	Material	TCE (ppm/°C)
Die	Silicon	4.2
Terminal Pads	CuW	6
Housing	Al_2O_3	6.4
Seal Ring	Kovar	5.1
Lid	Kovar	5.1

Table 1. TCE Property of SMD Elements

Package Performance Comparison

Each SMD package is designed to accommodate a specific die size. The package piece parts are shaped to eliminate excess material without compromising the mechanical integrity. This results in the smallest and lightest possible package. The terminal pads are solid CuW. The thin structure of the drain pad (in case of a FET) represents a very short thermal path from the heat source (die) to an external heat sink. Combined with the outstanding thermal conductivity property of CuW, the package produces a very low thermal resistance path, thus a very low package junction-to-case thermal resistance (θJC). Performances of various SMD and leaded (TO-254, TO-257 and TO-258) devices are shown in Table 2.

PACKAGE	WEIGHT typical (grams)	FOOTPRINT REQ'D (sq. inch)	RθJC (°C/W)
SMD .5	1.1	0.118	1.67 (1)
TO-257	7	0.340 (4)	1.67 (1)
SMD 1	2.6	0.281	0.83 (2)
TO-254	9.3	0.521 (4)	0.83 (2)
SMD 2	3.3	0.362	0.42 (3)
SMD 3	3.4	0.387	0.42 (3)
TO-258	10.9	0.693 (4)	0.42 (3)

Notes:
1) With size 3 die (0.116"W x 0.181"L)
2) With size 5 die (0.257"W x 0.257"L)
3) With size 6 die (0.260"W x 0.360"L)
4) Including lead length of 0.150"

Table 2. Mechanical and Thermal Performance Data of SMD and Leaded Packages

The following analyses are based on the same die size for each of the package comparisons. The die sizes are as noted in Table 2 above. SMD .5 is the smallest SMD package in production today and is normally used in place of the TO-257. SMD 1 is about twice the size of the SMD .5 and is comparable to the TO-254. SMD 2 and SMD 3 are the largest packages of the series and are usually used in place of the TO-258. In all instances, the SMD devices are superior to their leaded counterparts with respect to weight reduction and footprint requirements. The packages' thermal resistances are comparable in all cases.

SMD Assembly Design Integration Guidelines

When integrating SMD devices to an assembly design, TCE of the board/substrate material must be closely matched to TCE of the SMD's, typically within 2-3 ppm/°C to minimize mechanical stress and to insure the mechanical integrity. Additionally, proper cooling must be provided to insure that the devices' operating junction temperatures are maintained below the desired level under the worst case condition. A device's thermal characteristics, θJC and θJA (junction-to-ambient thermal resistance) are essential and must be considered in the design process.

Low Power Designs

The SMD and CLCC devices can be attached directly to the traditional FR-4 or polyimide printed wiring board (PWB). However, due to considerable TCE mismatch, this assembly integration is limited to smaller packages. Many designers empirically limit the package size to a maximum of 0.5" in any one dimension to circumvent solder joint fatigue.

For designs with larger SMD packages and/or with wide temperature extremes, low TCE board materials are the solution as board materials with TCE of 7-9 ppm/°C are now available. Other TCE control techniques for printed wiring boards include the use of molybdenum, copper-invar-copper, or para-aramid fiber reinforcement as the board stiffener.

SMD can be bonded to a board with a silver filled epoxy or with a soldering process. For an attachment using solder, eutectic alloys should be used. Preheating of assembly prior to soldering and allowing the assembly to cool naturally after a soldering process, are highly recommended. Exposing the SMD components to temperatures in excess of 300°C is prohibited. Permanent damage to the SMD components may result.

Since FR-4 and polyimide board materials are poor thermal conductors, the PWB should not be considered as a thermal medium or heat spreader for the SMD unless the copper traces are sufficiently large. Otherwise, it is clear that the cooling of this device relies almost entirely on the package's ability to dissipate thermal losses in the free convection environment. The package's θJA then becomes the key design parameter.

For space environment where convection is nonexistence and radiation cooling is minimal, conduction is the only meaningful method of cooling. It may be necessary to attach an SMD to an on-board heat spreader or an enlarged copper trace for cooling.

Design Example:

For a device dissipating 1 watt and θJA of 25 °C/W, the junction temperature shall equal 100 °C for an ambient temperature of 75°C. This is based on the formula $PD = [TJ - TA]/\theta JA$, where PD is the device's power dissipation, TJ is the operating junction temperature, TA is the ambient temperature, and θJA is the package's junction-to-ambient thermal resistance.

High Power Designs

For high power applications where SMD devices dissipate more than a few watts and must be cooled with a heat sink, there are three basic assembly integration techniques, which are described as follows:

1) SMD with Leads

For this assembly technique, the SMD is attached with flat copper leads for electrical connections. The SMD device is bonded to a heat sink or a heat spreader via its lid with a thermally conductive epoxy or a thermal pad for cooling purposes. The SMD is electrically isolated from the heat sink as the lid is isolated from the die. The **junction-to-lid** thermal resistance for SMD 2 is about **6°C/W**. Thermal resistance of the epoxy must be included when determining the total thermal resistance of the assembly. Figure 3 depicts a typical SMD with leads.

Another common assembly technique is to bond the leaded surfaces of the SMD directly to a heat sink with a thermally conductive epoxy or a thermal pad. Unless the bonding medium contains an insulating material, placing a thin layer of ceramic at the bonding interface will provide the required electrical isolation.

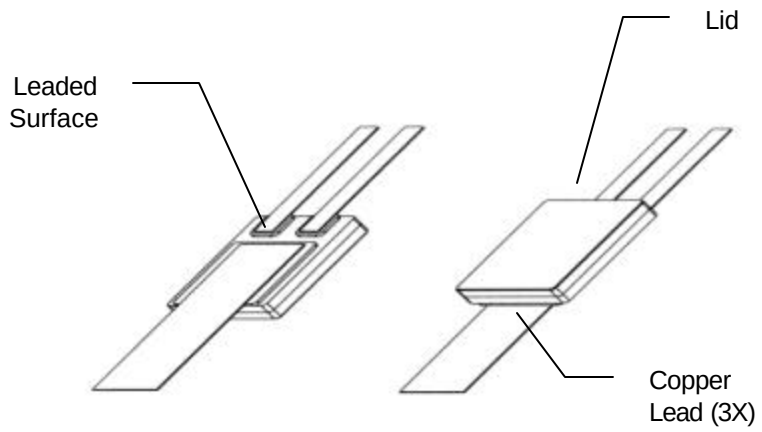

Figure 3. An SMD with Leads

2) SMD Carrier Assembly

For assembly designs with one or two SMD devices, the SMD carrier is the solution to a cost-effective design. SMD carrier is a leaded DBC substrate with three extended flat copper leads (one each for gate, drain and source terminal as in the case of a MOSFET device). An SMD device is soldered to the carrier resulting in an isolated ready-to-use SMD assembly. With its good thermal conductivity and excellent dielectric properties, the ceramic layer within the DBC provides the SMD device the essential electrically isolated thermal path with negligible impact on the overall thermal performance of the assembly. Standard SMD carriers are shown in Figure 4.

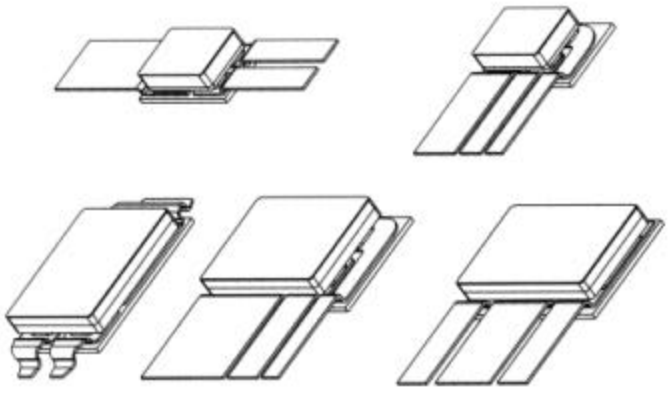

Figure 4. Standard SMD Carriers

Figure 5 illustrates a design implementation using the SMD carrier assemblies. In this design approach, all small signal and low power components are populated on a FR-4 or polyimide board and each SMD is

attached to a carrier. The SMD carrier assemblies may be bonded to a common base with a thermally conductive epoxy or soldered directly to a low TCE base. The base or chassis is usually a thermally conductive metal such as aluminum serving as a cold plate or heat sink for the entire assembly. The low TCE base can be Al/SiC (aluminum/silicon carbide) or any material with a TCE in the range of 5-9 ppm/°C. Electrical connections from the carrier assembly to the board are made through the copper leads of the carrier. The overall assembly's junction-to-base thermal resistance (θJB) depends on the die size, substrate material, base material, and the substrate bonding method. For a carrier assembly with SMD 2 device using size 6 die, alumina (Al_2O_3) substrate, Al/SiC base, and soldering process for the attachment, the θJB is about 0.7-0.8°C/W.

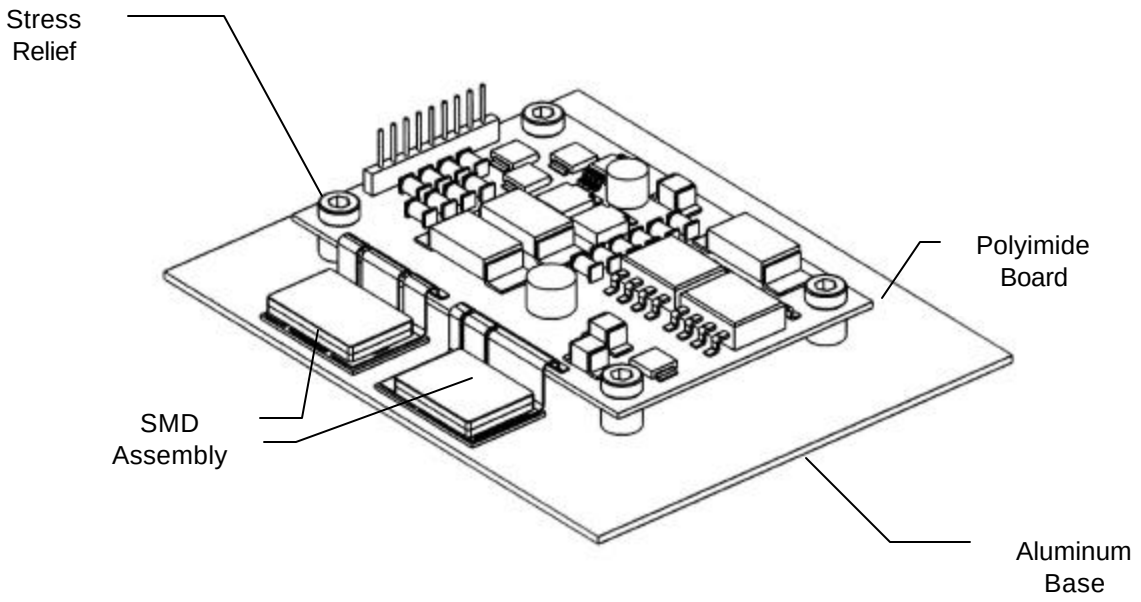

Figure 5. An Electronic Assembly with SMD Carrier Assemblies

3) Power Module Assembly

A power module assembly is basically a large SMD carrier populated with any number of surface mount components. The assembly may include any surface mount semiconductor and passive components, i.e., capacitors, resistors, magnetic parts, etc. However, unlike the previous assembly integration, all SMD's and associated components are populated on one or more direct bonded copper (DBC) substrates. Similar to the traditional PWB, copper traces of the DBC substrate provide electrical connections for the components and its ceramic (alumina) interlayer provides the electrical isolation. For .025" thick alumina, voltage isolation of greater than 2000 volts can be expected. To complete the assembly, the DBC substrate is soldered to a base with a comparable TCE and high thermal conductivity material to promote the assembly's thermal conduction.

For most design applications, DBC Al_2O_3 is the substrate material of choice due to its reasonable thermal conductivity and its relatively low cost. Other substrate materials which have been used successfully, include DBC AlN (aluminum nitride), and DBC BeO (beryllium oxide). These materials have excellent thermal conductivity and will provide a better thermal performance than DBC Al_2O_3. However, the cost of these materials is about three to five times that of the DBC Al_2O_3 for the same design. BeO is a hazardous material and its use is limited by the government agency. However, its low dielectric constant property may be the solution for designs that require low assembly coupling capacitance.

With closely matched TCE's of the substrate, base and the SMD device, this design produces a complete assembly with sound mechanical integrity. This design/manufacturing approach is often referred to as 'Power Module' technology. The technology is now matured. However, the cost of manufacturing a small quantity is high due to substantial capital investment in manufacturing equipment, nonrecurring assembly tooling costs and minimum buy of specialty materials. To reduce design time and system costs, designers generally subcontract the assembly design and manufacturing as the solution to the design integration. Other essential benefits of this design approach include design flexibility, excellent electrical performance, greater reliability, and ease of assembly integration.

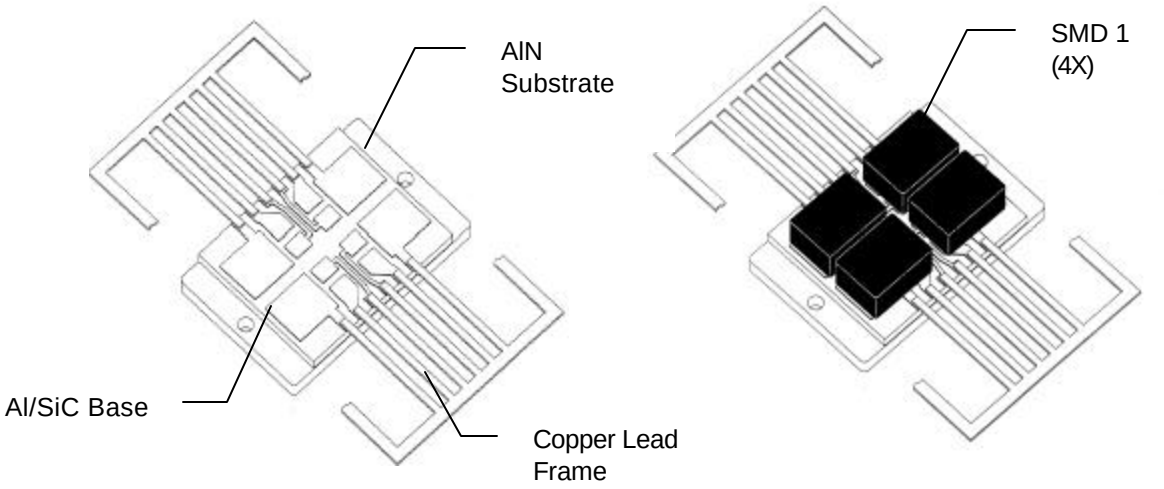

Figure 6. A Power Module Assembly with Four SMD 1 Devices

Figure 6 depicts a power module assembly with four SMD 1 devices. The assembly uses copper leads for electrical connections to other assemblies. The substrate is an AlN substrate and the base uses Al/SiC material. Power module assembly offers a variety of assembly interface designs. Pins, terminals, standoffs, flex circuit, bus bars, and any custom interface terminals can be easily incorporated to facilitate the system design integration.

Verification Methods for Attachment Integrity

The conventional visual inspection method cannot be used for an assembly populated with SMD devices as the soldered connections are not visible. The approved inspection methods are x-ray, sonascan, and thermal response. If the inspection cannot be performed in-house, there are several independent laboratories that have the proper equipment and will perform the required inspection for a fee.

SMD Provides Desirable Electrical Performance

SMD, due to its low package resistance and low lead inductance, provides the best possible electrical performance especially in switching applications. Table 4 shows the typical lead inductance of these devices as a result of internal bond wires and 0.25 inch of lead for a TO-25X package. Unlike the leaded TO-25X packages, series resistance of the SMD is extremely low, 1 mΩ as compared to 5 mΩ or greater, resulting in lower Rds(on).

In switching applications, skin effect can cause AC losses in the leads of the package to be greater than the DC losses. Lead of a TO-25X package contains ferromagnetic materials. Magnetic field is generated as current passes through the leads. Eddy currents induced in a lead by the magnetic field cause skin effect. Skin effect causes current in a lead to flow only on the outer periphery of the leads. The depth of this annular conducting area is inversely proportional to the square root of the frequency(1).

For a 40 mils diameter lead (wire size of TO-254), the ratio of AC resistance to DC resistance at 50 KHz is about 1.35. The ratio increases to 1.75 (~29%) as the frequency rises from 50 KHz to 100 KHz. The resistance ratio is also a function of the lead's diameter. The resistance ratio increases as the lead's diameter increases. Increasing the lead's diameter from 40 mils to 60 mils (TO-258), the AC resistance to DC resistance ratio increases by about 50% at the frequency of 100kHz(1). The AC losses will further reduce the circuit efficiency.

In most assembly configurations, the SMD package lends itself to layouts where components are in close proximity yielding short circuitry interconnections. This results in low circuit resistance, low circuit inductance and negligible AC losses which improve the circuit efficiency and produce the best possible switching waveforms, which in some cases forgo the need for snubber circuits.

Lead Inductance	TO-254 TO-257 TO-258	SMD 1 SMD 2 SMD 3
Drain (nH)	5 - 8.7	0.8 -2
Source (nH)	8.7 - 15	2.8 - 4.1

Table 3. Device Lead Inductance Data, SMD's vs. Leaded Packages

SMD Rework Procedure

Should replacement or re-alignment of an SMD be required, a hot air system with appropriate orifice masking to protect surrounding components may be needed. Preheating of the assembly to within 50°C of the solder's melting temperature will facilitate the rework process. Temperature must be carefully controlled and monitored when applying heat to the device to avoid permanent damage to the SMD.

Conclusions

The Hermetic SMD is the choice for designs that require smaller size and lighter weight assembly with excellent thermal performance. Additional benefits include cleaner switching waveforms and higher circuit efficiency. Populating an SMD on a printed wiring board is limited to low power applications. For a larger SMD, board materials with a low TCE are now available to simplify the assembly designs.

For high power applications, there are three basic assembly integration methods. The techniques include the use of an SMD with leads, the SMD carrier assembly and the SMD power module assembly. For an SMD with leads, the device is conduction cooled via the lid or leaded surfaces of the package. For the carrier and power module assemblies, the SMD's are populated onto the DBC substrate that serves as the thermal path to a cold plate. It also provides the essential electrical isolation and electrical connections. These assembly integration techniques will facilitate the assembly design process and will promote the use of the surface mount devices.

Reference:

1) A. I. Pressman, "Switching Power Supply Design," McGraw-Hill, Inc., New York, 1991.