FlipFET^{TM} MOSFET Design for High Volume SMT Assembly

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Introduction & Summary

International Rectifier has used a proprietary technique to position all the terminals of a HEXFET® device on the same face of the die. This has enabled the development of wafer scale packaged MOSFETs. We're calling the technology platform the FlipFET MOSFET, and we are using it to offer surface mount products with the lowest $R_{DS(on)}$ per footprint area in the industry.
This paper introduces the form factor and outlines design considerations. Specific guidelines for use and initial product performance are then discussed.

Package Design Considerations

Design for high volume assembly in commercial electronic equipment dictated the following constraints:

a) Must be suitable for use with clean and no-clean flux processes
b) Pitch of interconnects must suit existing track design rules
c) Interconnect material must suit standard eutectic solder reflow
d) No underfill (or other tertiary) process required to achieve device reliability

The form factor resulting from these constraints is illustrated in Figure 1.

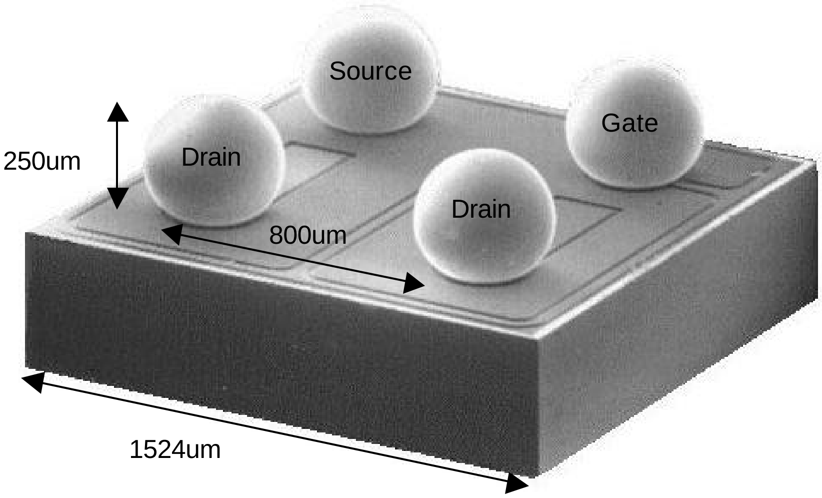

Figure 1: The FlipFET^{TM} MOSFET Form Factor

Constraints ‘a’, ’b’, and ‘c’ have been addressed by feature geometry. The pitch of the solder bump interconnects is 0.8mm to fit standard JEDEC defined CSP footprint designs and hence avoid any requirements for fine pitch substrate conductor definition. The size of the solder bumps has been designed to be similar to existing CSP products allowing clean or no clean fluxing processes to be used at board mount.

Constraint ‘d’ required consideration of the likely failure modes of a naked assembly. These have been identified as moisture ingression leading to corrosion of the device interconnects and solder joint fatigue leading to contact degradation (both electrical and mechanical) [1].

Moisture Ingression

Passivation of the active areas of the device is achieved by depositing a passivation layer as the last masking process in fabrication. Vulnerability is thus localised to the areas of exposed metal used for interconnect via the solder bumps. This has been addressed by the mechanical structure of an under- bump metal (UBM) layer which is also required to prevent diffusion of the wafer metallurgy into the solder bump to and provide a solderable surface for the solder bumps to adhere to.

This layer is a Nickel Phosphorus alloy. A zincate process is used to selectively catalyse the areas of top metal exposed by the passivation. Plating then takes place directly on the wafer metalization with no masking process required. The nature of the electroless nickel process gives a very even, flat deposit, mirroring the surface of the top metal. The plating also grows equally in the horizontal and vertical directions, giving an overlap of the passivation layer hence providing a mechanical seal that prevents ingress of moisture into the device. This structure is illustrated in Figure 2. A thin layer (~0.1um) of immersion gold over the nickel finishes the UBM, preventing oxidation and providing a solderable surface finish. Gold embrittlement of the solder joint due to intermetallic formation is not a concern with this structure as this will give <0.03% Au in the bump.

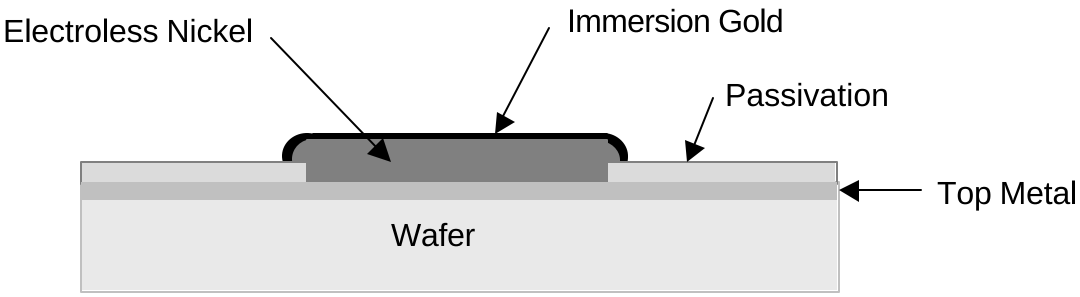

Figure 2: The FlipFET^{TM} MOSFET Under Bump Metal Structure

Solder Joint Fatigue

Degradation of the solder joints is primarily caused by cracks propagating through the joint caused by thermally induced mechanical stress. The distribution of this stress is illustrated in Figure 3.

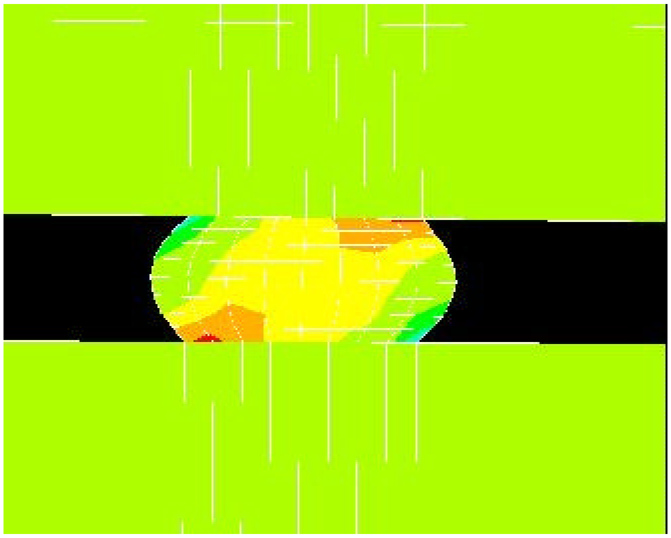

Figure 3: Thermally Induced Mechanical Stress in Solder Bumps

Initial investigation of the interaction between package design and this phenomenon was completed using a FEA model developed by Scott Popelar at IC Interconnect [2]. The model has previously been validated on flip chip, BGA, and CSP packages. An experiment was designed to look at the following parameters at two levels:

- Board Thickness
- Die Standoff
- Passivation Opening
- Conductor thickness

All of the above were considered for two thermal profiles (-55 to +150°C and –40 to +125°C). The device used was 1.524x1.524mm and had an array of 4 bumps at 0.8 mm pitch. The substrate was FR-4.

Results, shown in Table 1, predicted that even with the worst combination of factors, the FlipFET MOSFET would pass 1000 cycles of temperature cycling.

Predicted Fatigue life (MTTF, Cycles)		
Profile	Worst Combination	Best Combination
-40/125°C	1736	2819
-55/150°C	1538	2417

Table 1: FEA Modelled Weibul Life for a 1.524x1.524mm The FlipFET™ MOSFET

Of the factors studied, only die standoff and passivation opening were found to be significant. Standoff is an important factor with all flip chip devices, as it increases, the effect of thermal co-efficient of expansion mismatch between silicon and substrate is reduced. In most flip chip devices, at considerably smaller pitches and standoffs, the influence of the TCE mismatch between solder and silicon is far outweighed by that of the substrate to silicon. However, in this case, it was found that the stresses caused were of the same order of magnitude.

For this reason initial devices have been designed with passivation openings at the lower end and bump height (hence standoff) was designed at the higher end of the windows we considered in our experiment.
Temperature cycling on real devices to validate these modelled results is underway.

Solder joints can also be degraded by electromigration [3]. This is the movement of metal in the direction of electron flow due to a mass transfer effect, and is dependent on current density and temperature. In the case where the die forms the cathode, movement of the solder components away from the UBM occurs leaving micro voids. The increase in resistance and current density exacerbates the situation and will eventually lead to complete failure of the interconnect. Work is currently ongoing to determine the impact of electromigration to current ratings for FlipFET MOSFET devices.

Board Design

The FlipFET MOSFET is suitable for assembly onto ceramic and organic boards. Both solder masked and non-solder mask defined pads can be used and should be 250 micron diameter.

The surface finish can be almost any that is generally used for SMT. Much of the evaluation testing has been successfully carried out on electroless Ni/Au boards. Finishes such as immersion silver or tin and the various organic surface preservatives will also be suitable.

Hot air levelled solder is not recommended, as it will give variable solder volumes on the pads. This will lead to tilted die and reduced reliability.

The heat path from a FlipFET™ MOSFET to the PCB is extremely short, making this the primary direction of heat loss from the device. It is imperative therefore that the thermal requirements of the assembly are considered when designing the printed circuit board.

Connection to a large ground plane for example will provide a much improved heat path over narrow tracks.

Assembly Process and Materials

It is anticipated that FlipFET MOSFET^{TM} will most commonly be used with printed solder in a standard SMT process. It is recommended that a low residue no clean solder paste should be used with type 3, 63/37 Sn/Pb powder.

It is important that the volume of solder on each pad is consistent, as this will prevent tilting of the die. As with all fine pitch components great care should be taken to avoid formation of extraneous solder balls which could cause a short between adjacent interconnects or tracks.

The placement accuracy required is +/- the radius of the pads on the substrate. This will ensure that the centre of the ball is always placed over the pad. Due to the surface tension of the solder, devices that have all balls placed in solder on the pads will self align to give symmetrical joints.

Die Technology

FlipFET MOSFET design is based on International Rectifier's low voltage, extremely low $R_{DS(on)}$ cellular trench technology. This very high channel density design packs over $110x10^6$ cells/in^2 and has been successfully used in numerous p-channel and n-channel ultra low $R_{DS(on)}$ benchmark products targeted for portables, laptops and automotive applications. The process description has been reported in [4]. The main difference in the FlipFET MOSFET design from conventional trench structure is that the drain is brought up from the back to the front of the die using a proprietary process.

Device Performance

The initial FlipFET MOSFET offering is 2 devices in p-channel configuration. The IRF6100 is a 20V p-channel device and the IRF6150 is a dual 20V p-channel device. Some of the key device characteristics are listed in Table 2.

		IRF6100 (P-Channel)	**IRF6150 (dual P-Channel)**
Parameters	**Conditions**	Typical Values	Typical Values
BV_{DSS}	I_{DS}=250 uA	-23.2 V	-23.7 V
I_{DSS}	V_{DS}=-20 V	48 nA	158nA
$R_{DS(on)1}$	V_{GS}=4.5 V	42 mOhm	23 mOhm
$R_{DS(on)2}$	V_{GS}=2.5 V	60 mOhm	39 mOhm
$V_{GS\ (Th)}$	I_{DS}=250 uA	-625 mV	-840 mV

I_{GSS}	V_{GS}=+12 V	0.9 nA	2.2 nA
I_{GSS}	V_{GS}=-12 V	1.9 nA	68.7 nA
$R_{\theta jA}$	1sq inch Cu on FR4	50°C/W	27°C/W

Table 2. Basic Characteristics of the first two The FlipFET MOSFET^{TM} Devices

The performance of this new platform is the result of several distinctive features of the design. The first feature is the elimination of packaging and therefore package related resistance and inductance losses allowing for much smaller device footprints for a given $R_{DS(on)}$. Secondly, the improved thermal dissipation: footprint area performance allows designers to plan for higher power densities than have been possible using standard small outline packages devices.

The typical applications for these parts include battery charging and load switching in cell phones and laptops; therefore these devices are required to have extremely low $R_{DS(on)}$ for longer battery life. However, the FlipFET MOSFET architecture can be applied to other HEXFET® silicon generation platforms and hence produce products optimised for applications with different critical parameters such as avalanche capability or switching speed.

Conclusion

The FlipFET^{TM} MOSFET is compatible with existing high volume assembly techniques without the need for underfill or other tertiary processes. The lead products, optimised for use in portable and ultra-compact applications, are benchmark in terms of $R_{DS(on)}$ per device footprint area.

References

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