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Chip Scale Packaging Technology Increases Cell Phone Talk Time

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Two main objectives in the design of a cell phone are minimizing size and maximizing talk/standby time. To achieve this the lithium-ion battery, with it's high energy density and cubic shape, is today's technology of choice. However, due to the inherent damaging consequences of overcharging or discharging a li-ion battery, battery protection must be used and is usually incorporated in the battery pack.

Figure 1 shows a typical battery pack assembly showing the battery and battery protection circuit assembly using SOIC packaged devices. This circuitry requires 17.6% of the total volume of the battery pack. The battery measures 1.38 x 1.86 x 0.34 in. for a volume of 0.873 in.^{3}. The flex circuit board measures 1.38 x 1.86 x 0.073 in. for a volume of 0.187 in.^{3}. The SO-8 controller and MOSFETs are the tallest components on the board. This equals a total volume of 1.06 in.^{3}.

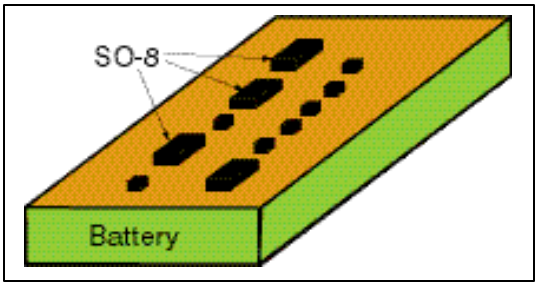

Figure 1. Battery pack controller using SOIC packaged devices.

To reduce the volume of the circuit board assembly, alternate packaging technology must be used. For the semiconductor devices, the most efficient type of packaging is a Chip-Scale-Package (CSP). CSPs have no external package or leads, the plastic over-mold, wire bonds, and lateral leads are eliminated. The silicon is the package, achieving 100% utilization of the footprint area for the chip as well as reducing the height. All electrical connections needed for operation are brought to the top surface of the chip. Electrical connection and mount down is achieved with an array of solder bumps on the top surface of the chip. The CSP is mounted by flipping the chip over and reflowing the solder bumps to attach to pads on the PC board. Standard surface mount equipment and techniques can be used for this process. No special equipment is required.

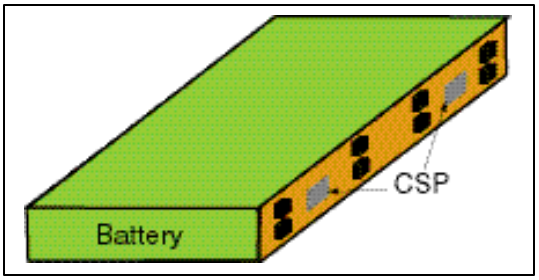

Figure 2. Battery pack controller using CSP devices.

Figure 2 is an illustration of a battery pack showing the battery and a battery protection circuit assembled using a bi-directional MOSFET switch, an IRF6150 FlipFET™ and a DS2760 battery monitor/controller Flip-

Chip. Both are CSP devices, minimizing the volume of the assembly. This assembly will fit on the edge of the battery, measuring 1.38 x 0.34 x 0.05 in. for a volume of 0.0235 $in.^3$. The tallest component on this assembly is a capacitor. The new total volume is 0.8965 $inches^3$. This is only 2.6% of the total battery pack volume, freeing up 15% of the volume. This space could be used to increase the battery volume, thus increasing talk time 15% or it could be used to shrink the battery size to reduce the size of the cell phone.

The CSP battery protection solution is a full feature solution providing the ability to identify the particular characteristics of the pack, monitor parameters such as temperature, voltage, and current consumption. From this information the user can determine the remaining capacity of the battery, an estimate of the run time of the product and the viability of the pack. Coupled with the switch resistance of less than 26 milliohms, with a gate drive of 2.5V, this battery protection solution will equal any circuit assembled from SO-8 packaged devices in less than 13% of the volume.