

Alleviating High Side Latch on Problem at Power Up

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I - INTRODUCTION

In a typical IR2xxx high voltage IC application with bootstrap power supply, the bootstrap capacitors are charged before the system becomes operational. In the process of charging up the bootstrap capacitor prior to establishing the high side supply voltage, if the high side output inadvertently turns on and stays on, it may cause a shoot through and may damage the IGBT devices. Even though the data sheet does not specify this power up transient case, the startup behavior is crucial for motor drive applications.

In general, the high side outputs of most of our control IC products rely on the high side Under Voltage Lock out circuit (UVBS) during power up to stay low during the power up. Under a combination of certain overstress and startup conditions, however, the high side output can inadvertently turn on and such an operating condition must be avoided.

II - TYPICAL APPLICATION PROBLEM

The high side output could latch on during a power up sequence in the system if a combination of the following conditions takes place:

1. No load condition (no motor lead connection to each VS nodes): The voltage at Vs node could be anywhere between the positive and the negative DC bus prior to charging the bootstrap capacitor.
2. High dV_{bs}/dt : Fast charging of the bootstrap capacitor.
3. V_{bs} is biased at a negative voltage prior to power up.

An AC motor drive system which uses a high voltage IC with bootstrap power supply initially goes through a power up sequence in which the bootstrap capacitors are charged up. Figure 1 shows a typical power up sequence. The following description assumes the three conditions listed above:

At start up, the units go through several stages before the drive is ready for normal operation. One of these stages involves charging up the bootstrap capacitor by turning on the low side IGBT devices. When the VS node is pulled down to the ground from high voltage floating node, the bootstrap capacitor charges through the bootstrap diode as shown in Figure 2. At this moment, if the conditions mentioned above are all met, the following events could occur:

- V_{bs} is charged at a very fast rate when the low side outputs are turned on.
- The whole high side circuit is biased to the negative DC bus at a very fast rate of dV_s/dt due to high impedance floating condition (no motor connection).
- If a negative voltage is applied to V_{BS}, when the high side circuit is powered up, the output can be latched on due to unwanted current flow into all of the high side circuit through its internal ESD diode structure.

(d) As a result, the high side output can be latched on while the associated low side output has already been turned on.

This is a mode of potential shoot through during a power up. The key to avoiding the shoot through is to properly initialize the high side circuit during a power up.

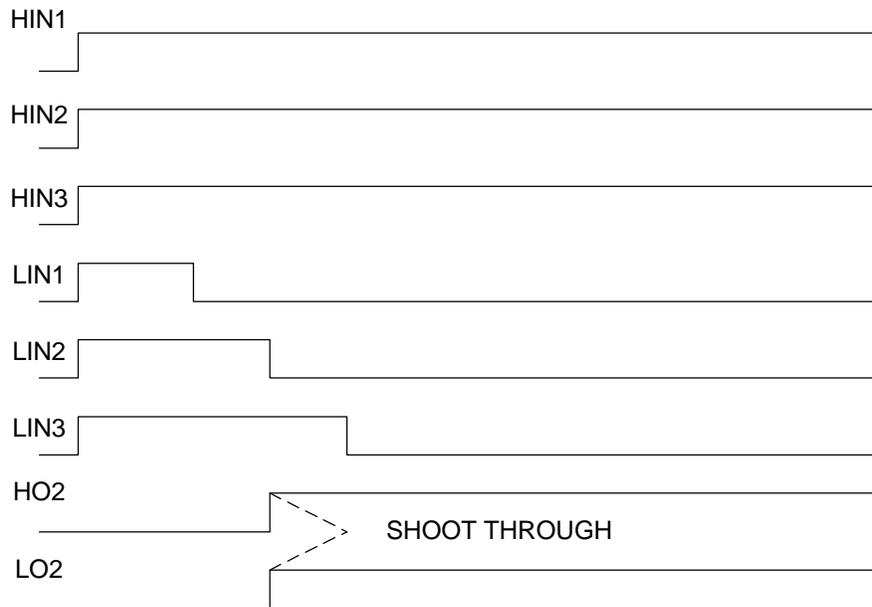


Figure 1: Power up sequence of Bootstrap Capacitor Charging

III - RECOMMENDED SOLUTION

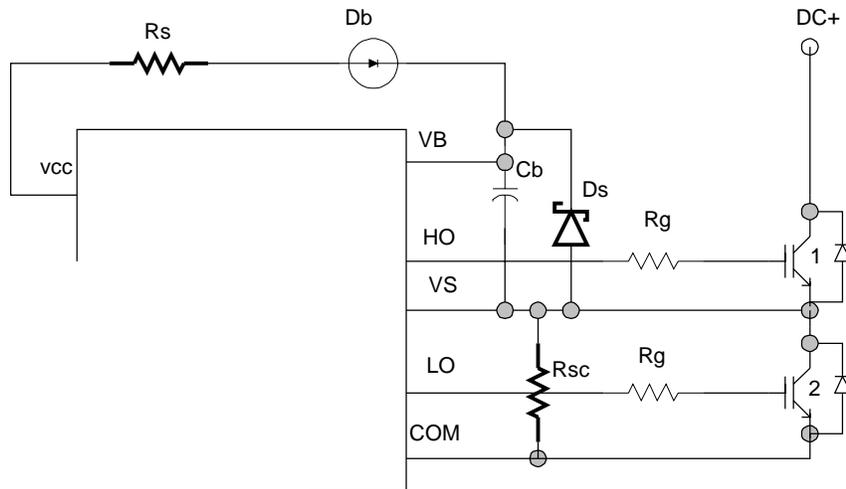


Figure 2: Typical bootstrap scheme with preventative elements

The most effective way of eliminating a potential shoot through is to eliminate the overstress condition of a negative voltage on VBS. Prior to a power up, if Vbs is biased to negative voltage which exceeds more than -0.3V as specified in the Absolute Maximum Rating specification - i.e. the condition #3 mentioned above -, then a forward diode current would flow through the ESD diode for the internal circuit in the high side as well as all P/N junctions in the high side well. One of the cause for such an overstress condition could be that, under a no load condition – i.e. condition #1 mentioned above -, the VS node is floating and the VS voltage could be high anywhere between DC+ and COM prior to charging up the bootstrap capacitor. To avoid both negative bias on VBS and a high dv/dt on the Vs node when the low side turns on, one can connect a bleeding resistor (Rsc) between VS and COM (Figure 2) so that the high side voltage can stay roughly at the negative DC bus potential prior to normal operation mode. Note that the Rsc value should both satisfy normal operation condition and minimize the power dissipation across Rsc – e.g. when M1 switches on, the Rsc should be able to dissipate $P_d = DC+ \times DC+ / R_{sc}$.

If a Schottky diode (Ds) must be connected between VB and VS – see Figure 4 – to avoid a negative bias on VBS, the Schottky diode should have the following specification:

- low forward voltage drop, e.g. $V_f = 0.2V$
- minimum 35V reverse breakdown voltage
- low reverse leakage current
- fast reverse recovery time

One effective method of slowing down the dV_{bs}/dt is to add a resistor in series with the bootstrap diode (figure 2). The value of series resistor relative to the bootstrap capacitor value should be chosen such that the RC time constant is equal or greater than 10usec. Note that if the rising dV_{bs}/dt is slowed down too much, it could result in a few missing pulses temporarily during the start-up phase due to insufficient VBS voltage. This possibility is more likely in a higher frequency application, and detailed guidelines are given in the Appendix. For bootstrap capacitor selection, refer to the design tip DT 98-2.

IV - CONCLUSION

To eliminate the possibility of a latch-on at power up under a no load condition, the IC must be operated as follows:

- dV_{bs}/dt higher than 10usec.
- Do not allow the VS node to float prior to normal operation mode.
- Do not allow VB to go below VS by more than one diode forward voltage drop prior to the power up of the high side circuit.

APPENDIX

In order to choose the optimum value for R_s, the following two conditions must be satisfied:

1. R_s X C_b time constant (figure 4) must be greater than 10usec.
2. The bootstrap capacitor (C_b) would charge through not only the bootstrap diode (D_b) but also through the series resistor (R_s) from the V_{cc} supply. Thus, the minimum charge which the bootstrap capacitor needs to supply would be:

$$C_b \times (V_{cc} - V_{rs} - V_f - V_{BSmin}) > 2Q_g + (I_{qbs}/f_c) \quad (1)$$

Where:

V_{rs}: Voltage drop across series resistor.

V_f: Forward voltage drop across the bootstrap diode.

V_{BSmin}: Minimum voltage across the bootstrap capacitor required for full enhancement.

Q_g: Gate charge of high side IGBT.

I_{qbs}: high side channel quiescent current.

f_c: switching frequency.

Examples:

The following two examples demonstrate the cycle-by-cycle fluctuation in the bootstrap voltage during the start-up phase over one PWM fundamental frequency.

Condition:

For both Case 1 and Case 2

$$V_{cc} = 15v, V_f = 1.5v, V_{BSmin} = 12.5v, Q_g = 200nC, I_{qbs} = 200\mu A, f_c = 2kHz, C_b = 2\mu F$$

For Case 1, R_s = 9Ω and for Case 2, R_s = 10Ω

Each parameters in the table are derived by the following equations.

$$T_c = 1 / f_c$$

$$m = (\sin 2\pi f T_c + 1) / 2$$

where f = 60Hz (fundamental frequency)

$$\Delta V_{dis} = (2Q_g + (I_{qbs} \times T_{on})) / C_b$$

$$V_{bsdis} = V_{bschrg}(prev) - \Delta V_{dis}$$

$$\Delta V_{ch} = (V_{cc} - V_f - V_{bsdis}) \times (1 - \exp(-t/RC)) \text{ Assume } V_f \text{ is constant over charging current}$$

$$V_{bschrg} = V_{bsdis} + \Delta V_{ch}$$

$$I_{rs} = (C_b \times \Delta V_{ch}) / T_{off}$$

$$V_{rs} = I_{rs} \times R_s$$

Where:

Tc: carrier period

m: modulation index [0 - 1]

ΔV_{dis} : voltage difference for discharging period of Cb

V_{bsdis}: voltage across Cb after discharge

ΔV_{ch} : voltage difference for charging period of Cb

V_{bscharg}: voltage across Cb after charge

V_{bscharg(prev)}: voltage across Cb after charge of previous state

Case 1: Cb = 2uF, Rs = 9 Ohms

seq #	Tc (ms)	m	T(on) (us)	T(off) (us)	ΔV_{dis} (v)	V _{bsdis} (v)	ΔV_{ch} (v)	V _{bscharg} (v)	I _{rs} (mA)	V _{rs} (v)	V _{bsdis} > V _{bsmin} ?
1	0	.5	250	250	0.225	13.275	0.225	13.5	1.8	0.016	Yes
2	0.5	0.593	297	203	0.23	13.27	0.214	13.484	2.1	0.019	Yes
3	1	0.684	342	158	0.235	13.249	0.232	13.481	2.9	0.026	Yes
4	1.5	0.768	384	116	0.239	13.242	0.232	13.474	4	0.036	Yes
5	2	0.842	421	79	0.242	13.232	0.23	13.462	5.8	0.052	Yes
6	2.5	0.904	452	48	0.245	13.217	0.215	13.432	8.9	0.08	Yes
7	3	0.952	476	24	0.248	13.184	0.175	13.359	14.5	0.131	Yes
8	3.5	0.984	492	8	0.249	13.11	0.093	13.203	23.3	0.21	Yes
9	4	0.999	499.5	0.5	0.25	12.953	0.009	12.962	36.4	0.328	Yes
10	4.5	0.991	498	2	0.25	12.712	0.051	12.763	50.6	0.455	Yes
11	5	0.975	488	12	0.249	12.514	0.26	12.774	43.3	0.39	Yes
12	5.5	0.938	469	31	0.247	12.527	0.478	13.005	30.8	0.278	Yes
13	6	0.885	443	57	0.244	12.761	0.443	13.204	15.5	0.14	Yes
14	6.5	0.819	410	90	0.241	12.963	0.397	13.36	8.8	0.079	Yes
15	7	0.741	370	130	0.237	13.123	0.298	13.421	4.6	0.041	Yes
16	7.5	0.654	327	173	0.233	13.188	0.271	13.459	3.1	0.028	Yes
17	8	0.563	282	218	0.228	13.231	0.241	13.472	2.2	0.02	Yes
18	8.5	0.469	235	265	0.224	13.248	0.232	13.48	1.75	0.016	Yes
19	9	0.376	188	312	0.219	13.261	0.223	13.484	1.4	0.013	Yes
20	9.5	0.287	144	356	0.214	13.27	0.217	13.487	1.2	0.011	Yes
21	10	0.206	103	397	0.21	13.28	0.212	13.492	1.1	0.01	Yes
22	10.5	0.136	68	432	0.207	13.285	0.205	13.49	0.95	0.009	Yes
23	11	0.078	39	461	0.204	13.286	0.205	13.491	0.9	0.008	Yes
24	11.5	0.035	18	482	0.202	13.289	0.203	13.492	0.84	0.0076	Yes
25	12	0.009	5	495	0.201	13.291	0.201	13.492	0.81	0.0073	Yes
26	12.5	0	0.1	499.9	0.2	13.292	0.2	13.492	0.8	0.0072	Yes
27	13	0.009	5	495	0.201	13.291	0.202	13.493	0.81	0.0073	Yes
28	13.5	0.035	18	482	0.202	13.291	0.202	13.493	0.84	0.0075	Yes
29	14	0.077	39	461	0.204	13.289	0.204	13.492	0.9	0.0079	Yes

Case 1: Cb = 2uF, Rs = 9 Ohms

seq #	Tc (ms)	m	T(on) (us)	T(off) (us)	ΔV_{dis} (v)	Vbsdis (v)	ΔV_{ch} (v)	Vbschar _g (v)	Irs (mA)	Vrs (v)	Vbsdis > Vbsmin ?
30	14.5	0.135	68	432	0.207	13.286	0.206	13.493	0.95	0.0086	Yes
31	15	0.205	103	397	0.21	13.282	0.209	13.491	1	0.009	Yes
32	15.5	0.286	144	356	0.214	13.277	0.214	13.491	1.2	0.011	Yes
33	16	0.375	188	312	0.219	13.272	0.217	13.489	1.4	0.013	Yes
34	16.5	0.468	235	265	0.224	13.265	0.222	13.487	1.7	0.015	Yes

Table 1

Case 2: Cb = 2uF, Rs = 10 Ohms

seq #	Tc (ms)	m	T(on) (us)	T(off) (us)	ΔV_{dis} (v)	Vbsdis (v)	ΔV_{ch} (v)	Vbschar _g (v)	Irs (mA)	Vrs (v)	Vbsdis > Vbsmin ?
1	0	.5	250	250	0.225	13.275	0.225	13.5	1.8	0.018	Yes
2	0.5	0.593	297	203	0.23	13.27	0.212	13.482	2	0.02	Yes
3	1	0.684	342	158	0.235	13.247	0.233	13.48	2.9	0.029	Yes
4	1.5	0.768	384	116	0.239	13.241	0.23	13.471	3.9	0.039	Yes
5	2	0.842	421	79	0.242	13.229	0.227	13.456	5.8	0.058	Yes
6	2.5	0.904	452	48	0.245	13.211	0.21	13.421	8.8	0.088	Yes
7	3	0.952	476	24	0.248	13.173	0.167	13.34	13.9	0.139	Yes
8	3.5	0.984	492	8	0.249	13.091	0.089	13.18	22.3	0.223	Yes
9	4	0.999	499.5	0.5	0.25	12.93	0.009	12.939	34.7	0.347	Yes
10	4.5	0.991	498	2	0.25	12.689	0.044	12.733	44.1	0.441	Yes
11	5	0.975	488	12	0.249	12.484	0.259	12.743	43.1	0.431	No
12	5.5	0.938	469	31	0.247	12.496	0.453	12.949	29.2	0.292	No
13	6	0.885	443	57	0.244	12.705	0.472	13.177	16.6	0.166	Yes
14	6.5	0.819	410	90	0.241	12.936	0.394	13.33	8.8	0.088	Yes
15	7	0.741	370	130	0.237	13.093	0.319	13.412	4.9	0.049	Yes
16	7.5	0.654	327	173	0.233	13.179	0.272	13.451	3.2	0.032	Yes
17	8	0.563	282	218	0.228	13.223	0.245	13.468	2.2	0.022	Yes
18	8.5	0.469	235	265	0.224	13.244	0.234	13.478	1.8	0.018	Yes
19	9	0.376	188	312	0.219	13.259	0.223	13.482	1.4	0.014	Yes
20	9.5	0.287	144	356	0.214	13.268	0.218	13.486	1.2	0.012	Yes
21	10	0.206	103	397	0.21	13.276	0.212	13.488	1.06	0.0106	Yes
22	10.5	0.136	68	432	0.207	13.281	0.208	13.489	0.96	0.0096	Yes
23	11	0.078	39	461	0.204	13.285	0.205	13.49	0.89	0.0089	Yes
24	11.5	0.035	18	482	0.202	13.288	0.203	13.491	0.84	0.0084	Yes
25	12	0.009	5	495	0.201	13.29	0.202	13.492	0.81	0.0081	Yes
26	12.5	0	0.1	499.9	0.2	13.292	0.2	13.492	0.80	0.008	Yes
27	13	0.009	5	495	0.201	13.291	0.202	13.493	0.81	0.0081	Yes

Case 2: Cb = 2uF, Rs = 10 Ohms

seq #	Tc (ms)	m	T(on) (us)	T(off) (us)	ΔV_{dis} (v)	Vbsdis (v)	ΔV_{ch} (v)	Vbschar _g (v)	Irs (mA)	Vrs (v)	Vbsdis > Vbsmin ?
28	13.5	0.035	18	482	0.202	13.291	0.201	13.492	0.83	0.0083	Yes
29	14	0.077	39	461	0.204	13.288	0.204	13.492	0.88	0.0088	Yes
30	14.5	0.135	68	432	0.207	13.285	0.206	13.491	0.95	0.0095	Yes
31	15	0.205	103	397	0.21	13.281	0.21	13.491	1.1	0.011	Yes
32	15.5	0.286	144	356	0.214	13.277	0.212	13.489	1.2	0.012	Yes
33	16	0.375	188	312	0.219	13.27	0.218	13.488	1.4	0.014	Yes
34	16.5	0.468	235	265	0.224	13.264	0.222	13.486	1.7	0.017	Yes

Table 2

In case #1 with Rs= 9 Ohms, the high side supply voltage at the end of Ton (Vbsdis) is greater than the required minimum voltage (Vbsmin= 12.5v) at all times, while in case #2 with Rs= 10 Ohms, Vbsdis is smaller than Vbsmin in two of the sequences 11 & 12. Therefore, to satisfy the two conditions mentioned the optimum value of the Rs would be:

$$5 \Omega < R_s < 10 \Omega$$

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