

Intelligent Power Switches (IPS): Operation in an Automotive Environment

By X. de Frutos and A. Mathur

TOPICS COVERED

Ground loss

Ground offset

Voltage peaks

Reverse battery conditions

Battery disconnection

Load dump capability

Intelligent Power Switches (IPSs) are particularly appreciated in the automotive environment, where they have to deal with some of the worst electrical conditions - including ground loss or offset, voltage peaks, reverse or disconnected battery, and load dump. IPSs protect against all these conditions, while driving loads ranging from power relays and electrovalves to motors and lamps. Low side, high side and groundless high side switches use different internal structures to do so, and their behaviour varies for various electrical stresses. (Automotive electrical stresses refer to the ISO 7637 definitions).

1. GROUND LOSS

1-1 Low Side IPSs

When the ground is disconnected on a low side switch, the load is no longer activated. Figure 1 shows the parasitic structure that is activated in this case. A resistor in series, R_{in} , limits the current that would flow into the microcontroller. The resistor has to be a low enough value (about $1\text{ k}\Omega$) such that the voltage drop across it is negligible, thus assuring proper operation under normal conditions.

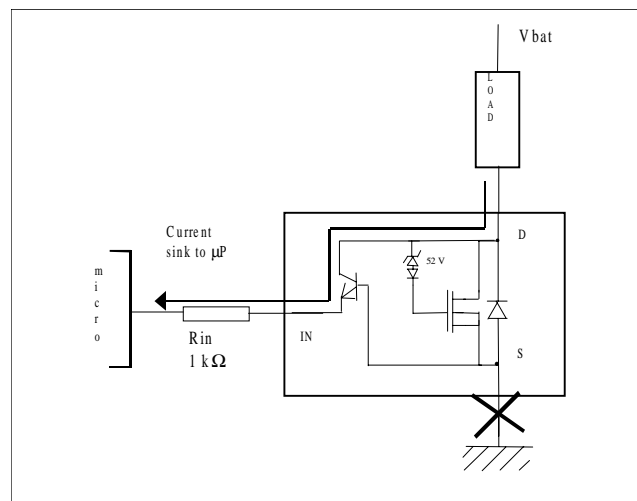


Figure 1 - LSS current path during ground loss

1-2 High Side IPSs

High side switch logic control is referenced to V_{cc} . When the ground is disconnected, the IN pin is pulled-up to V_{cc} . The Power MOSFET turns-off and the load is no longer activated. Resistors in series (about $15k\Omega$ each) limit current re-injection through DG and IN to about 1 mA. Figure 2 shows the current path during ground loss.

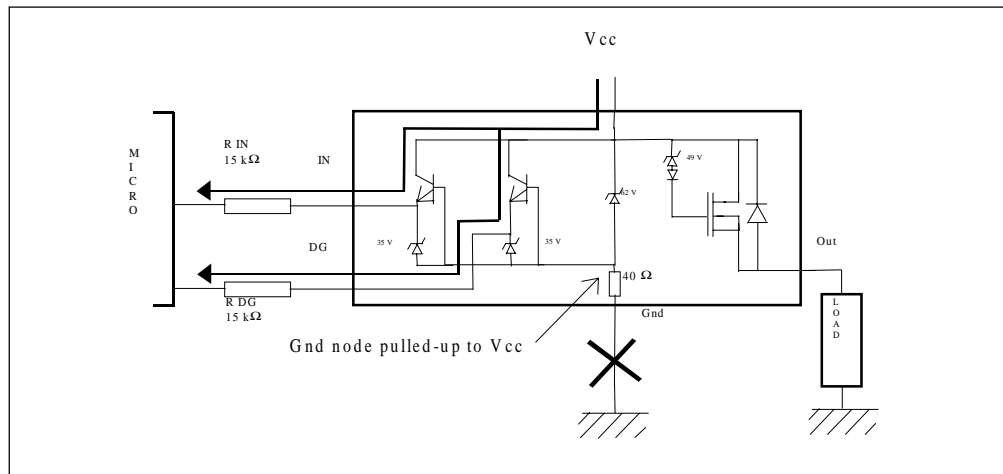


Figure 2 - HSS current path during ground loss

1-3 V_{cc} referenced Input High Side IPSs

A V_{cc} referenced Input high side switch is not connected to a ground in normal use. Therefore, a loss of ground connection is irrelevant.

2. GROUND OFFSET

The floating gate drive of the high side switches allows positive and negative voltages between load ground and logic ground. The ground offset is defined as the common mode of the output voltage referenced to the logic ground (see Figure 3). The IPS remains under active control as long as the load ground is (a) less than V_{cc} , and (b) greater than $(V_{cc}-V_{cl})$.

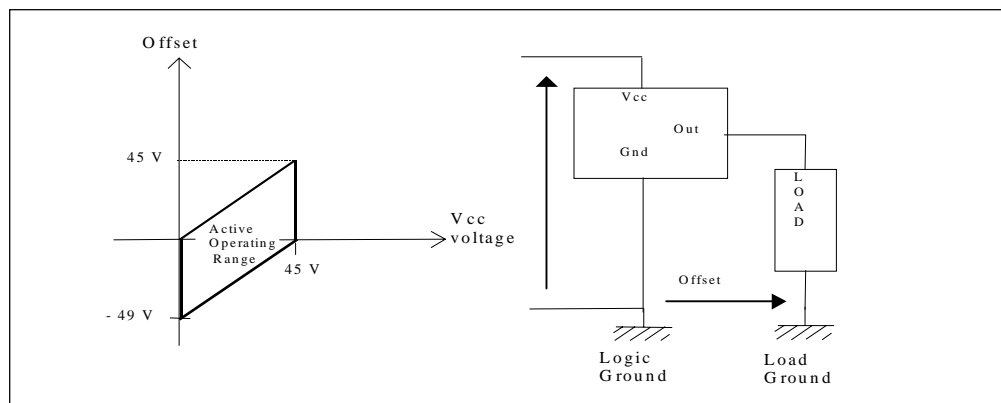


Figure 3 - HSS ground offset definition

3. VOLTAGE PEAKS

The profile of a voltage pulse on Vcc or Vbat is typically defined by the rise time, duration and source resistance. For example, in a typical case of the IR European version, positive pulses have the following characteristics: $V_p = 100\text{ V}$, $t_r = 1\text{ ms}$, $T_d = 50\text{ ms}$, $R_i = 10\Omega$; while negative pulses have a shorter duration: $V_p = 100\text{ V}$, $t_r = 1\text{ ms}$, $T_d = 2\text{ ms}$, $R_i = 10\Omega$.

Both types of pulses represent inductive effects: the positive pulse is generated when the current through an inductance in series with the device is turned-off; the negative one is generated when the current through an inductive load in parallel with the device is switched-off.

3-1 Low Side IPS

Positive Pulse

For low side switches, when the Vcc voltage exceeds Vclamp, the difference between Vpulse and Vclamp activates the load, and therefore prevents current re-injection into the microprocessor.

Negative Pulse

Negative pulses also activate the load by turning on the body-diode. A reverse bias protection scheme helps to avoid current re-injection to the microprocessor (Fig 4b).

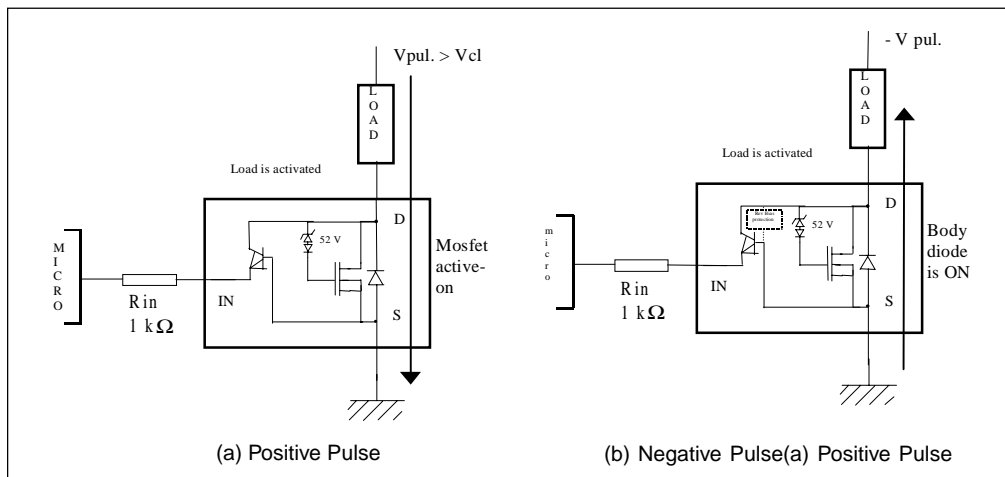


Figure 4 - LSS current paths during pulses

3-2 High Side IPS

Under either a positive or negative pulse on Vcc, one may need to add the zener diodes (shown in Fig 5) to supplement the limited power dissipation capability of the internal structure of a high side IPS device.

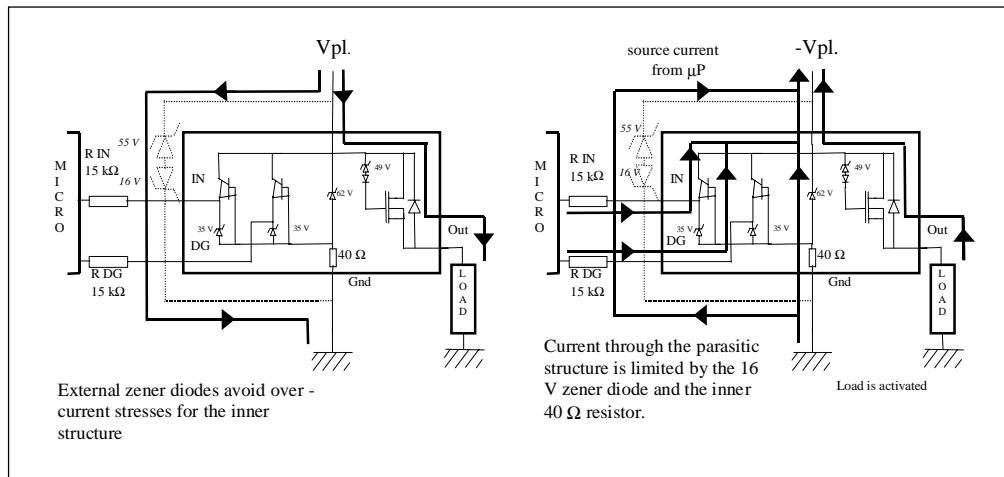


Figure 5 - High Side IPS current paths during pulses

3-3 Vcc referenced Input High Side IPS

For Vcc referenced Input high side switches, such as the IPS 5551T, an additional zener diode must be added between Vcc and IN, as shown in Figure 6, to limit the current to and from the microprocessor. In either a positive or negative pulse, the load is activated.

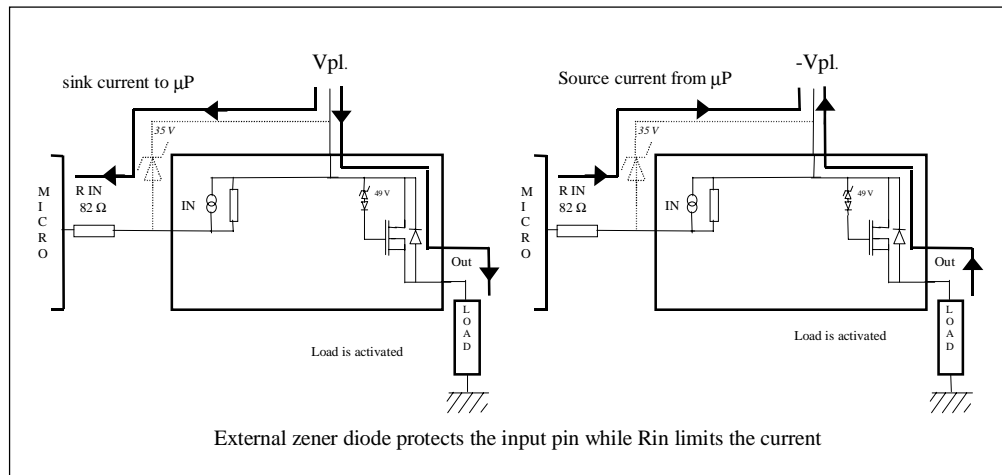


Figure 6 - External zener diode protects the input pin while R_{in} limits the current

4. REVERSE BATTERY CONDITION

4-1 Low Side IPSs

When a reverse battery condition occurs, current flows through the forward biased body diode (as shown in Figure 7), and activates the load. In this case the junction temperature should be evaluated, since this condition can, in several seconds, heat the junction to a high temperature due to diode dissipation.

An inbuilt reverse bias protection prevents this current from being re-injected into the microcontroller.

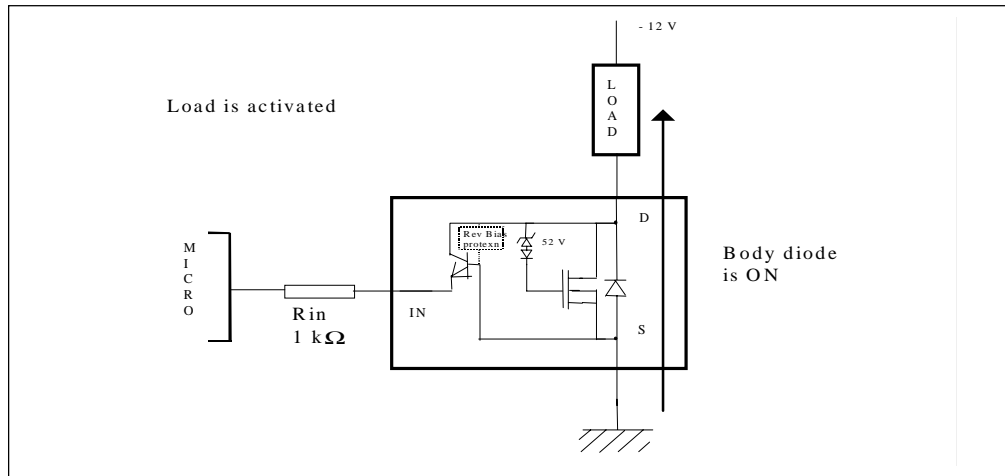


Figure 7 - LSS current path during reverse battery

4-2 High Side IPSs

A schottky diode in series with the ground return is used to prevent negative bias (Figure 8). The load is activated through the body diode, and therefore, the junction temperature rise (due to diode dissipation) has to be evaluated. If the load cannot be activated, a power schottky diode should be inserted in the positive Vcc line. (An IPS with a low Rds(on) can be used instead of the schottky to reduce the voltage drop.)

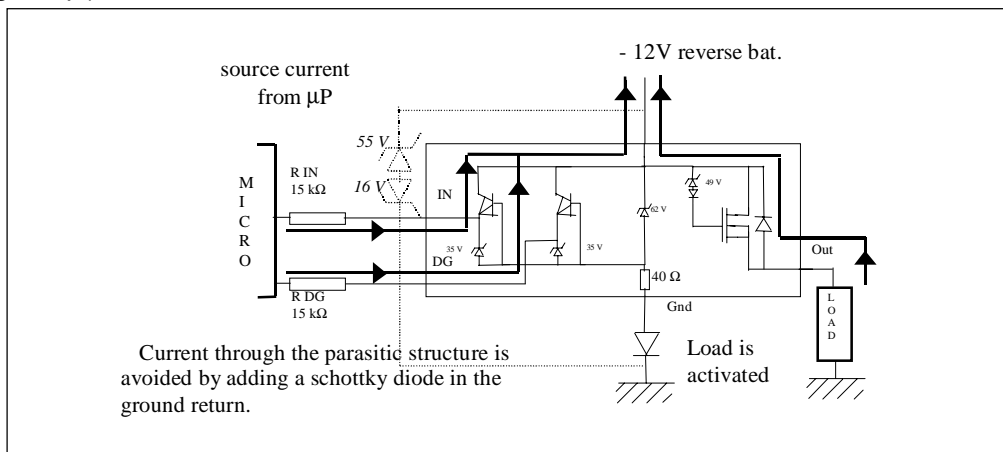


Figure 8 - HSS current path for -14V reverse battery

4-3 Vcc referenced Input High Side IPSs

A schottky diode in series with the input is used to prevent negative bias (Figure 9). (A low current schottky diode is suitable). Again, the load is activated through the body diode.

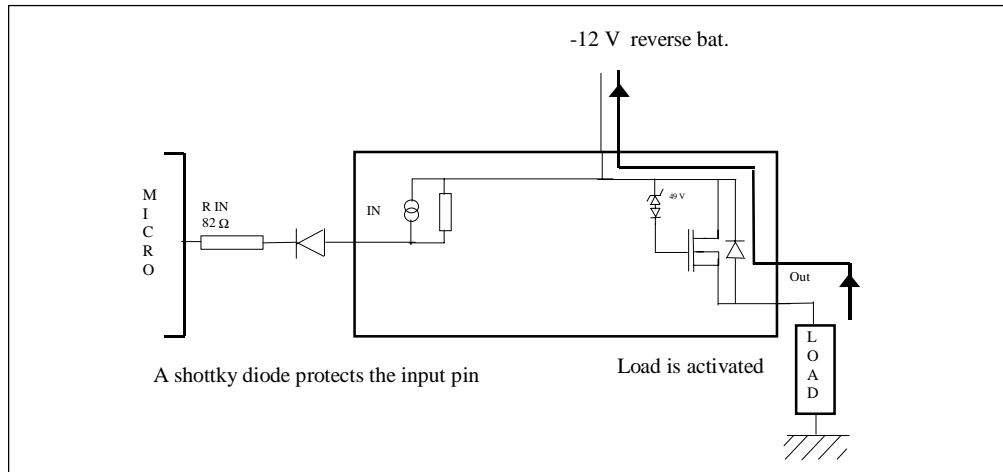


Figure 9 - Groundless HSS current path for -14V reverse battery

5. BATTERY DISCONNECTION

If the supply is disconnected while an inductive load is energised, the current must find an alternate path. However, since the low side and Vcc referenced Input high side switches cannot offer any demagnetisation path, a disconnected battery condition leads to a situation similar to the 'reverse battery condition'.

For a high side IPS, however, the load current will attempt to flow through the internal diode and the 40 Ω resistor. To protect this resistor (which can only withstand 0.4 A), it is necessary to add an alternate current path that uses a zener (DZ1) and a diode (D2) in series as shown in Figure 10.

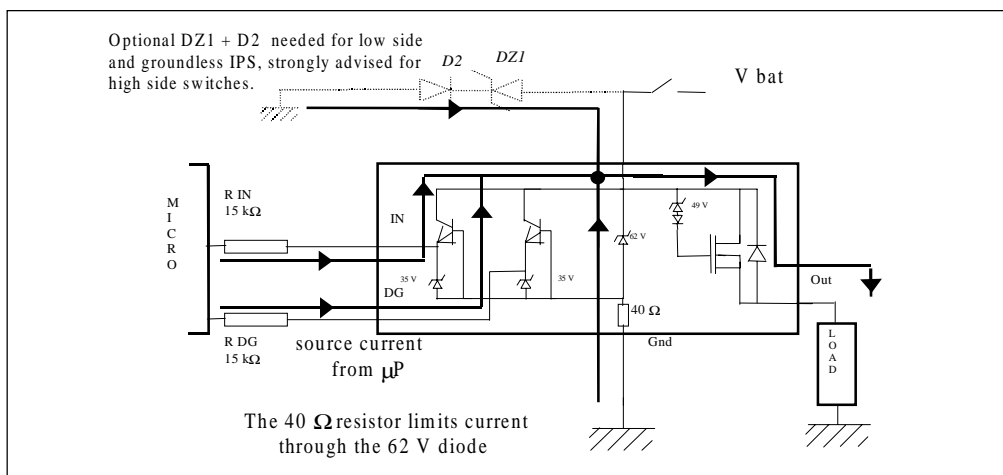


Figure 10 - HSS current path with battery disconnection

6. LOAD DUMP CAPABILITY

A load dump occurs when the battery is disconnected while the alternator is at full flux. Its profile on Vcc is defined by its maximum peak voltage, its rise time, its duration and its source resistance. For example, for our European versions, typical load dump values are: $V_p = 37\text{ V}$, $T_r = 10\text{ ms}$, $T_{on} = 200\text{ ms}$ and $R_i = 2\Omega$.

As a general rule, IPSs should have a V_{cl} rating above the load dump voltage (to prevent current re-injection to the micro). The load dump overvoltage remains below V_{cl} so nothing happens when the switch is OFF. When ON, however, power dissipation increases ($R_{ds(on)} \times I^2$ load dump) and the rise in junction temperature, ΔT_j , has to be evaluated.

If the system requires the load to operate during load dump, the drain current has to remain below I_{sd} .

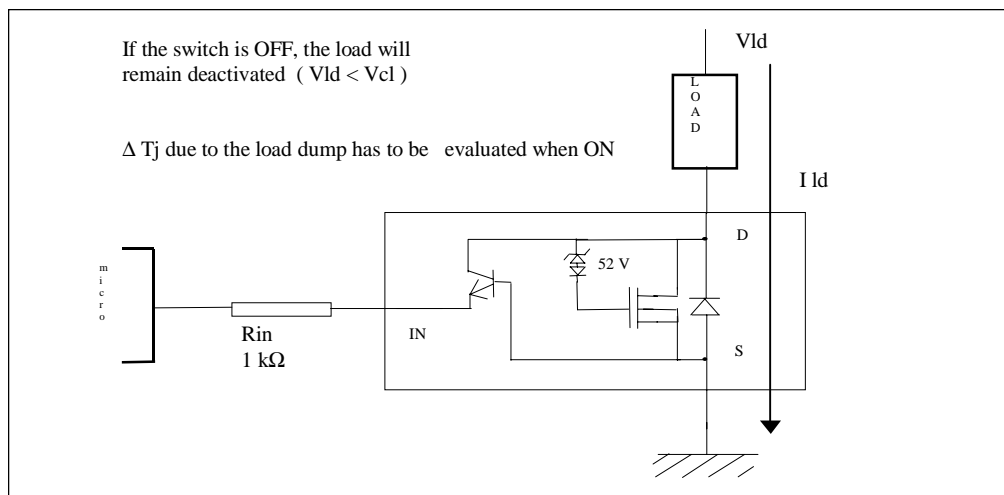


Figure 11 - LSS current path during load dump

7. CONCLUSION

This Design Tip offers an in-depth understanding of IPS operations in an automotive environment. For information on the basic protective features offered by these devices, refer to Design Tip 99-4. Design Tip 99-5 describes the Switching and Diagnostic capabilities of the IPS devices.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 0BL, United Kingdom

Tel: ++44 (0) 20 8645 8000

IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 81 (0) 33 983 0086

IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon,

Hong Kong Tel: (852) 2803-7380

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