International
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DESIGNTIP

DT 99-1

International Rectifier 233 Kansas Street El Segundo CA 90245 USA

Overshoot Voltage Reduction Using IGBT Modules With Special Drivers.

By David Heath & Peter Wood

TOPICS COVERED

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1. DESIGN CONSIDERATIONS

A critical problem common to all power switching circuits is inductive energy storage in stray inductances within the circuit. At low power levels of a few Watts a fast turn-off transition results in ringing with an overshoot voltage proportional to the stored energy and the switching speed. At high power levels these overshoots pose a major problem in terms of adequate voltage margins to handle them and the additional cost of such devices. Higher switch voltage ratings also result in higher conduction losses and lower overall efficiency. We are thus faced with a dilemma, how to maintain high efficiency with fast switching speeds without creating huge overshoots with all their attendant problems.

2. TURN-OFF PARASITICS

It is not possible to eliminate all stray inductances so there will always be overshoots at turn-off. Obviously circuit inductance must be reduced to the absolute minimum and there are many ways to do this, but the internal package inductance of the switching device is a measure of how well its manufacturer understands the inductance problem and has designed his switch accordingly.

Circuit inductance can be reduced by decreasing the effective loop size of the circuit and the most effective way to do this is by the use of laminated bus structures. The energy storage is thus greatly reduced and with it the overshoot voltage for a given switch speed. Strategically placed decoupling capacitors further reduce inductance values. Note, low internal ESR-ESL of these capacitors is also critical.(See DT 99-2 for further details)

There are a variety of methods used to combat these overvoltage spikes, all with the tradeoff of increased power dissipation in the switching device or external devices such as snubbers. One method of reducing the overvoltage spike is by limiting di/dt by increasing Rg. This can be done individually for turn-off as well as turn-on, but still has a substantial increase of the switching loss in order to obtain an appreciable reduction in the voltage spike.

Figure 1 shows a typical voltage spike at turn-off across a 600V, 200A Ultra-fast IGBT module operating at a bus voltage of 360V and 200A, where Rg(on) is 4.7Ω and Rg(off) is 0, and the effect of increasing Rg(off) to 30Ω in the indicated increments. Table 1 shows the increase in switching loss.

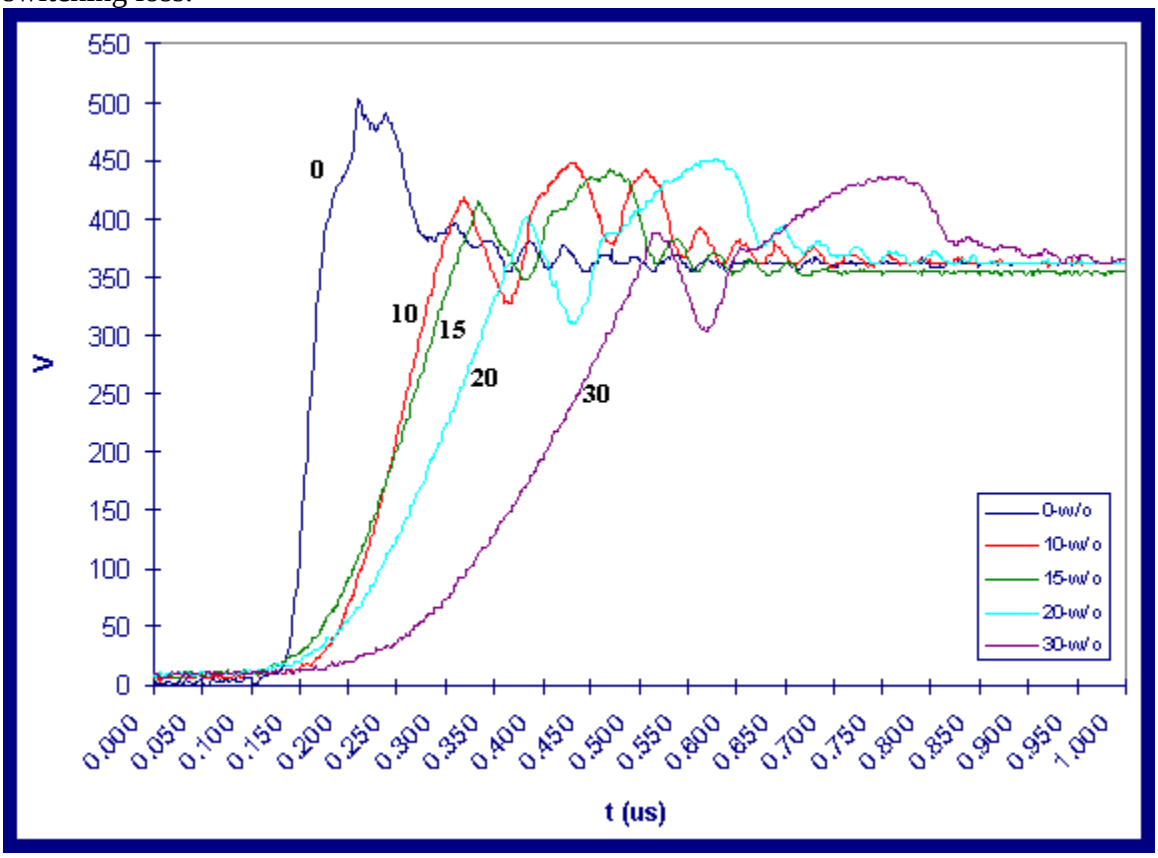


Figure 1

TABLE 1	
Rg(off)	Eoff
0	6.0mJ
10	11.1mJ
15	13.2mJ
20	15.4mJ
30	19.8mJ

As can be seen, increasing Rg to 10 ohms doubles the turn-off switch loss while only reducing the peak voltage by 13%. This would allow the use of a 600V device with a reasonable safety margin, but at the expense of a decrease in overall efficiency.

3. NEW METHOD FOR VOLTAGE OVERSHOOT REDUCTION

The ideal scenario would be to use dv/dt control such that the device turns off as fast as possible (within the dV/dt limits of the commutation diode) until Vce reaches the bus voltage, then decrease dv/dt to reduce the overvoltage spike. This will minimize switch loss while also reducing the overshoot.

The basic approach to this would be to discharge the gate at turn-off through a 0Ω gate resistor, or through a small value if dV/dt is too high, until Vce reaches the bus voltage, then switch the discharge path to a higher value resistance. Figure 2 shows one approach to accomplishing this.

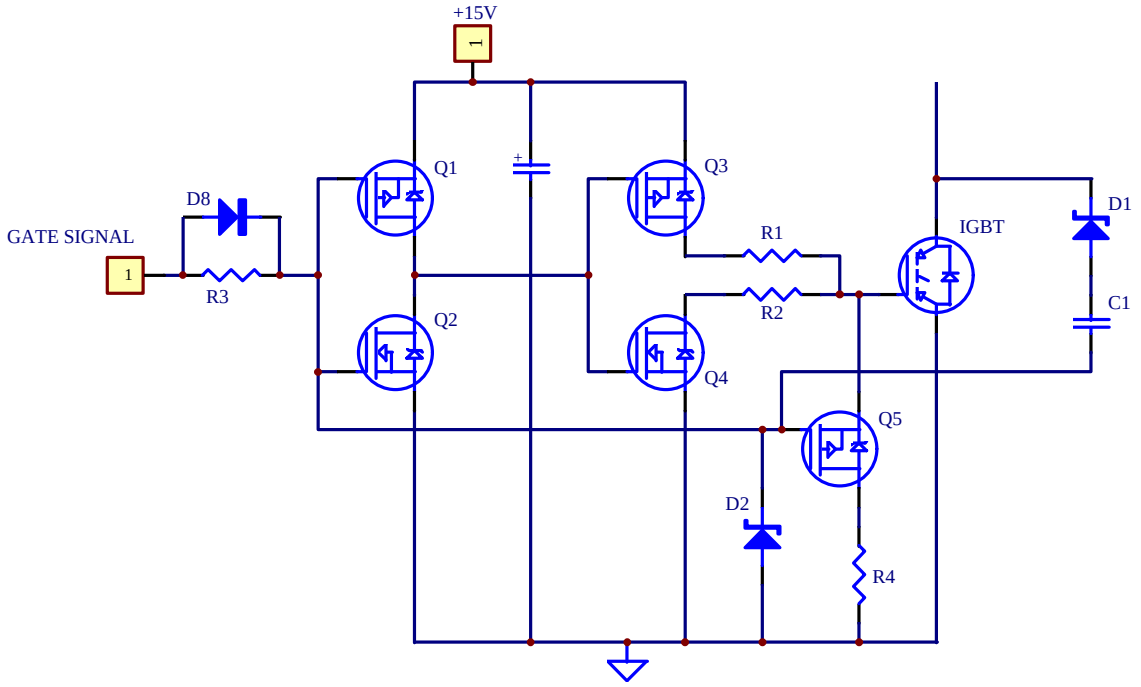


Figure 2: Overvoltage reduction method

With this approach, the input drive signal is fed into D8, bypassing R3, for a fast rise time. This turns Q1 off and Q2 on, bringing the gates of Q3 and Q4 to ground, which turns Q3 on and Q4 off. The drain current of Q3 flows through R1 and charges the gate of the IGBT. The gate of Q5 is connected to the gate signal, which is turned off during the IGBT turn-on. To turn off the IGBT, Q1 turns on and Q2 turns off. The gates of Q3 and Q4 are biased high, which turns Q3 off and Q4 on. At the same time, the gate of Q5 is pulled low, turning it on. This will discharge the gate immediately through R4, which could be a short or set to some value depending on the dV/dt parameters of the IGBT in use. Vce will begin to rise.

When the collector voltage reaches the breakdown voltage of zener D1, it will conduct and current will flow through C1to charge the gate of Q5, turning it off. This pulse will be very short, but long enough to turn Q5 off. With Q5 no longer discharging the gate, the remainder of the gate charge now flows through R2, slowing the rate of turn-off and reducing the overshoot voltage. D2 is a 12-15V zener to protect the IGBT gate from excessive forward voltage.

Figure 2 shows the effect of different resistor values for Rg(off) with this circuit. Table 2 shows the corresponding effect of Eoff.

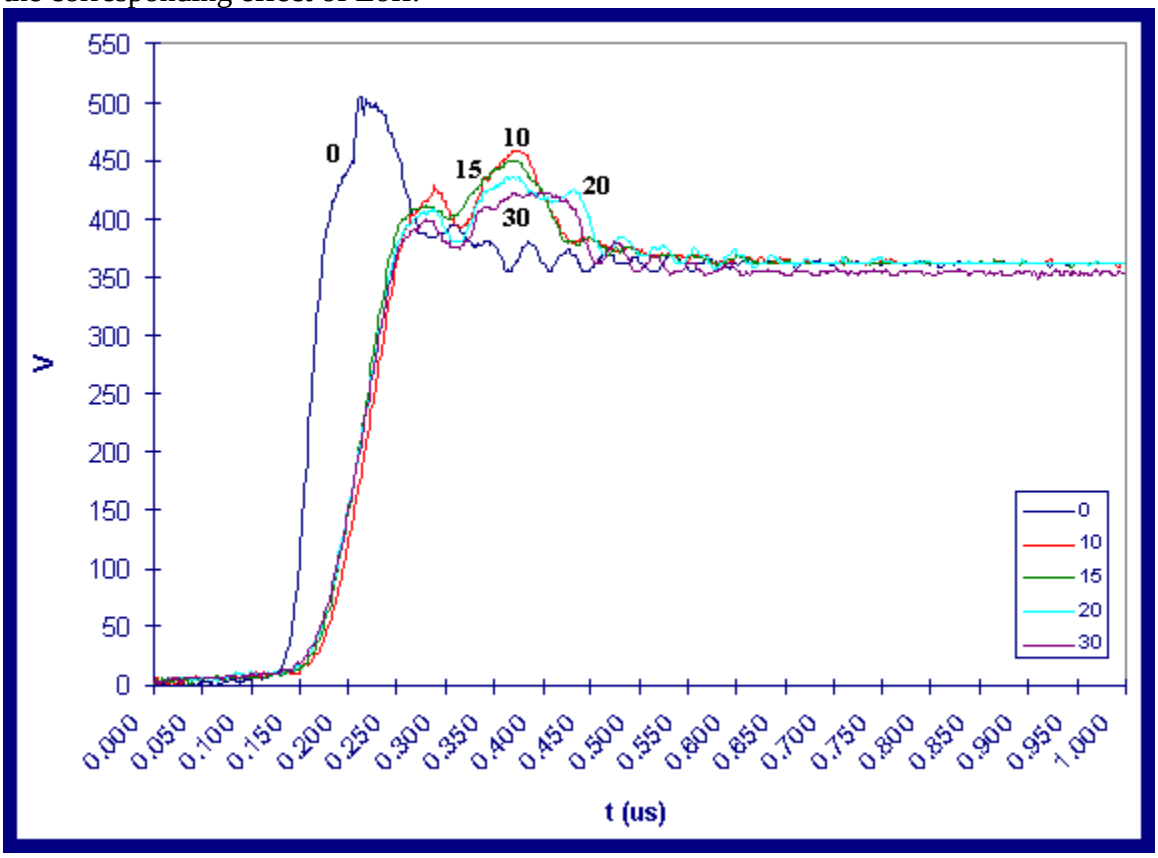


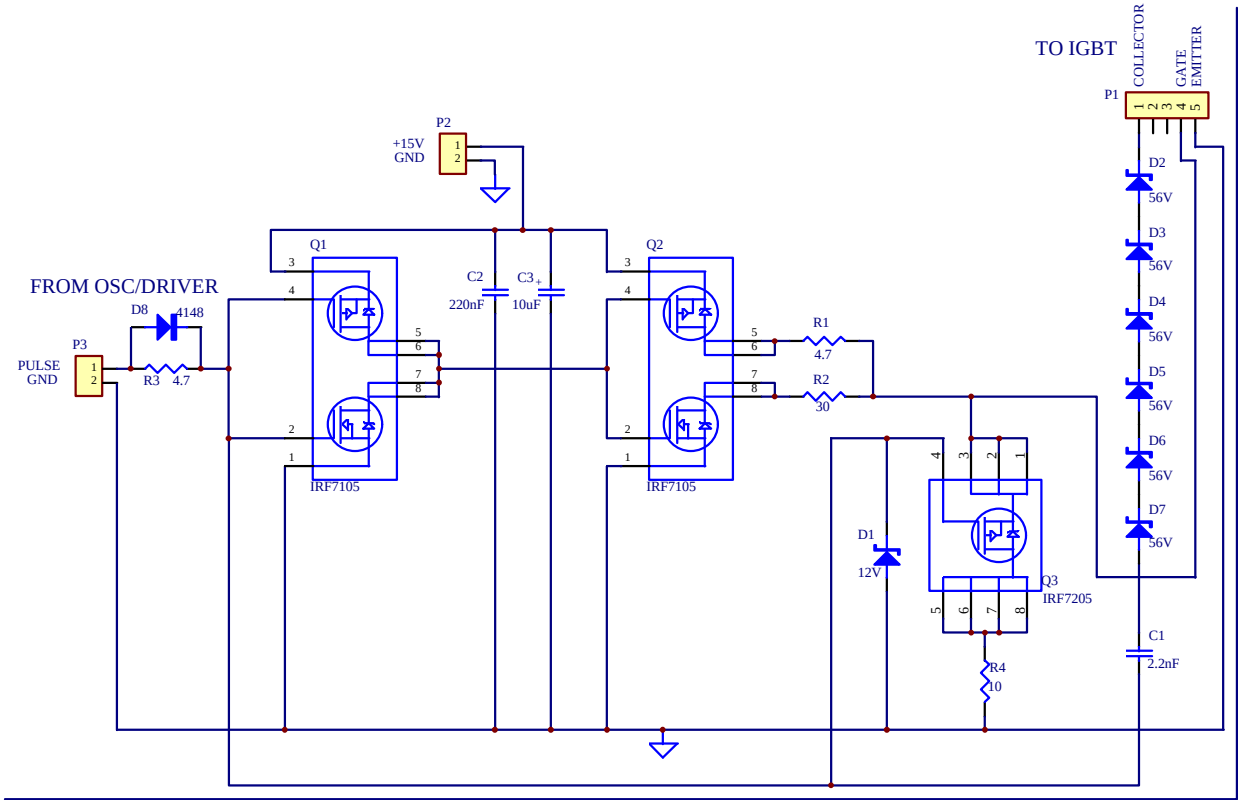
Figure 3

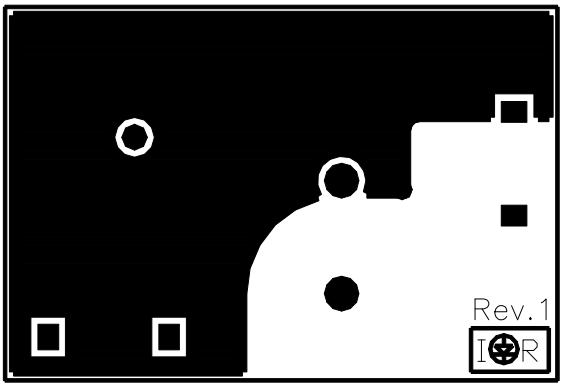
TABLE 2	
Rg(off)	Eoff
0	6.0mJ
10	9.4mJ
15	9.9mJ
20	10.3mJ
30	10.6mJ

So, in conclusion, a lower peak turn-off voltage can be achieved with half the switching loss of an IGBT without dv/dt control.

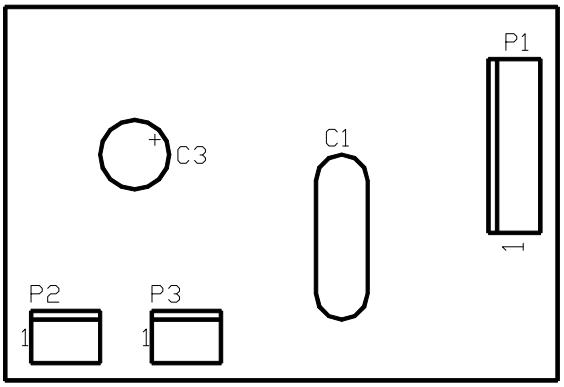
4. DESIGN EXAMPLE

A driver circuit was optimized for circuit inductance/impedance by using SMT components to keep the loop size of the gate discharge path to a minimum.

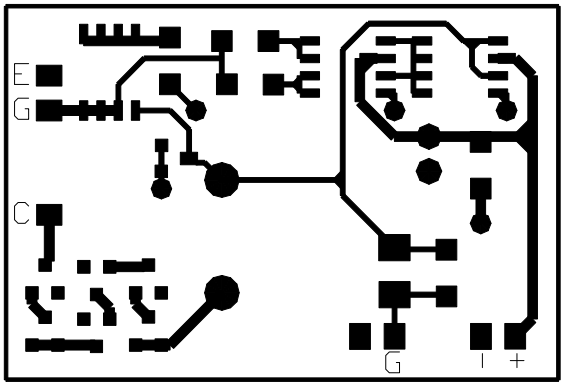




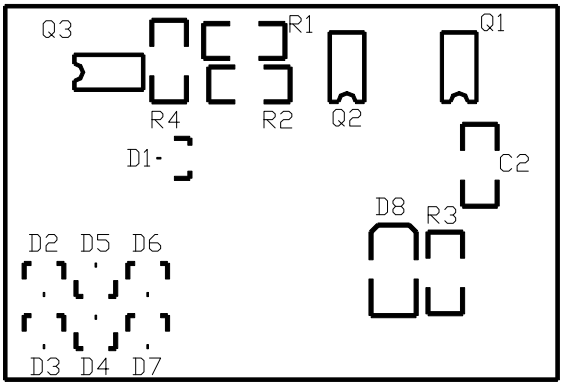
COMPONENT SIDE



TOP SILK



SOLDER SIDE



BOTTOM SILK