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DESIGN TIP

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Designing with IR2137

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TOPICS COVERED

1. Brief description of the application circuitry

IR2137 is a three-phase gate driver with enhanced protection features such as desaturation for the high-side devices.

The usual application circuitry is presented in Fig.1. It shows the communication link with the microcontroller stages through the *PWM* signal as well as the *Fault* and *Clear_Fault* signals. This stage needs a 5V power supply.

The operation mode of the *Desat* function or over-current protection (*ITRIP*) are not detailed in this design tip as they are presented in a separate technical paper.

This design tip is trying to address the questions regarding the applicability of the IR2137, the particular design of the bootstrap stage when applied within different PWM converters, to the design of the gate resistors as well as to the grounding issues.

2. Considerations regarding the bootstrap stage

IR2137 is delivering the control pulses for three-phase inverters that are working under a PWM algorithm. There are different types of PWM algorithms that are currently used by industry. Any particular PWM algorithm defines different values of the minimum and maximum pulse-widths. Since the bootstrap capacitor only charges when the low-side device is on, the duration of this interval should be high enough to ensure the rise of capacitor voltage to VCC.

Denoting by R the resistor on the charging path of the bootstrap capacitor (diode plus additional current-limiting resistor), the voltage across the capacitor is given by:

$$v_C(t) = [V_{CC} - V_f - V_{LS}] \cdot \left[1 - \exp\left(-\frac{t}{R \cdot C}\right)\right] \quad (1)$$

and the on-time of the lower IGBT (considered as charging time) should be enough for charging-up the capacitor above the minimum allowed voltage for proper operation of the high-side circuitry within the IR2137, that is 11.3V when VCC=15V.

Taking account of the possible discharge of the capacitor during the high-side IGBT conduction, one can restrict the level of the desirable voltage at the end of the charging interval at 90%. It yields:

$$[V_{CC} - V_f - V_{LS}] \cdot 0.90 = [V_{CC} - V_f - V_{LS}] \cdot \left[1 - \exp\left(-\frac{(t_{on}^L)_{\min}}{R \cdot C}\right)\right] \quad (2)$$

OR

$$(t_{on}^L) \geq -R \cdot C \cdot \ln[0.1] = 2.3 \cdot R \cdot C \quad (3)$$

By contrast, the bootstrap capacitor should sustain the gate current during turn-on and during the “on” state of the high-side IGBT. The value of the capacitor should correspond to the duration of this interval. In other words, the charge acquired during the on-state of the low-side IGBT should be enough to compensate for the charge needed by the high-side device. The usual equation for designing C is [1]:

$$C \geq \frac{2 \cdot \left|2 \cdot Q_G + [I_{qbs(\max)} \cdot t^H{}_{on}] + Q_{ls} + [I_{Cbs(leak)} \cdot t^H{}_{on}]\right|}{[V_{CC} - V_f - V_{Ls}] - V_{\min}} \quad (4)$$

where V_{min} should stay above 11.3V. Moreover it is suggested to choose a much larger value for a safer design.

It is recommended to use a resistor in series with the bootstrap diode. This resistor brings benefits in:
- correcting the time constant (both with C);
- limiting the charging current at start-up;
- limiting the current through the bootstrap circuit during possible negative V_s spikes. Both capacitor terminals are trying to follow the V_s negative spikes. Both capacitor terminals are trying to follow the V_s negative spike and this can turn-on the bootstrap diode allowing a current through R.

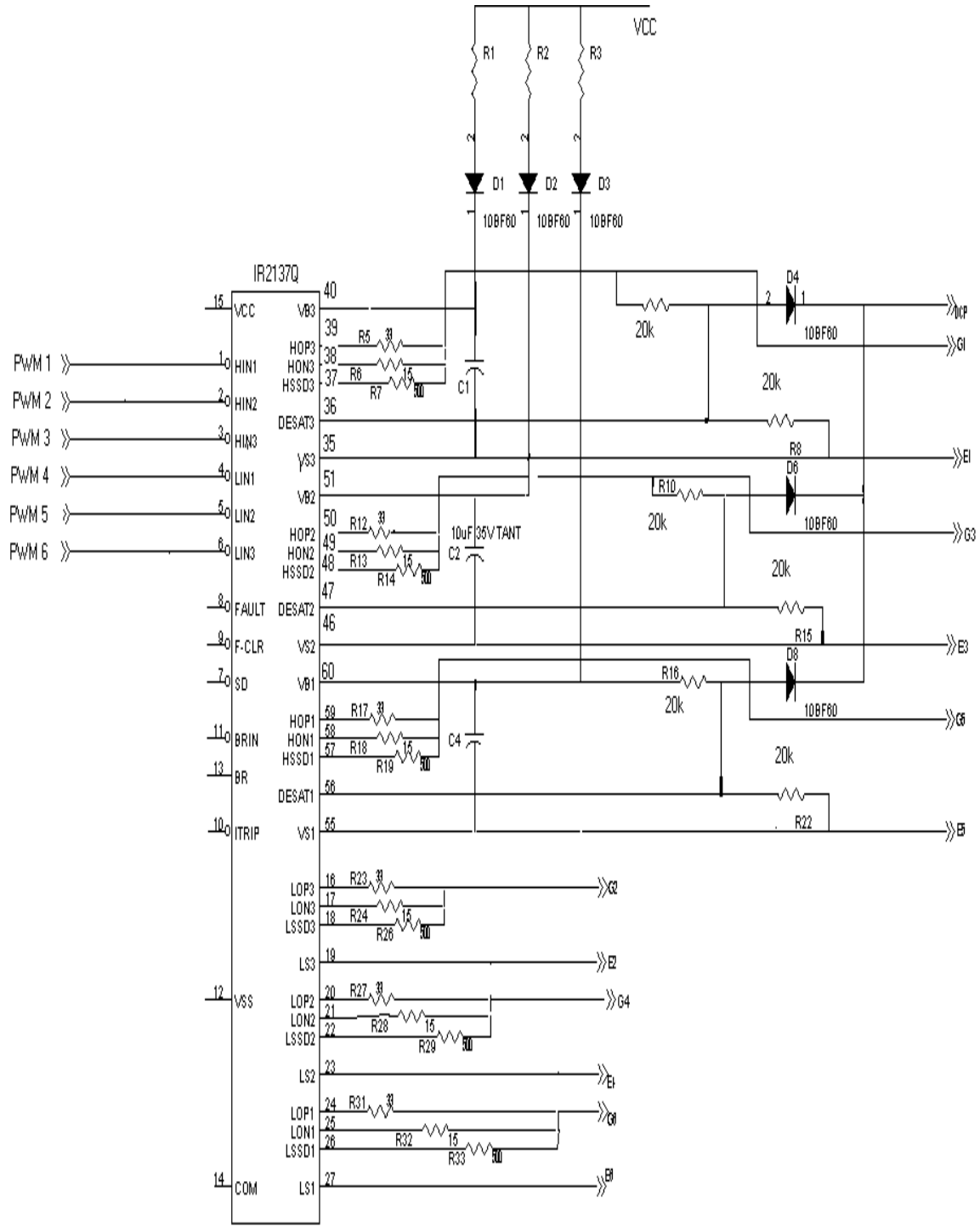

Figure 1: Basic application circuitry of the IR2137

Some measured values of the negative VB-COM spike for different situations are:

	malfunction (still working)	latched (destructive)
Low-side = ON, High side = OFF		
Pulse-Width = 500ns	7V	40V
Pulse-Width = 1us	6V	25V
Low-side = OFF, High side = ON		
Pulse-Width = 500ns	8V	52V
Pulse-Width = 1us	7V	19V

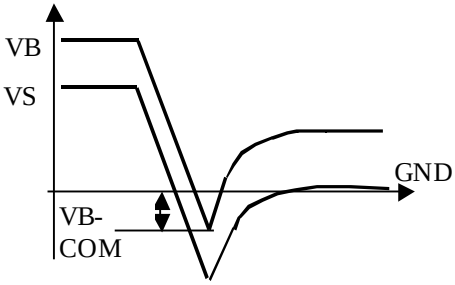

Figure 2: Vs spike definition

Since the three-phase inverters are using PWM algorithms that produce different time variations of the pulse width (t^H_{on} or t^L_{on}), designing a bootstrap capacitor should consider in eq.(3) and (4), the maximum value of the t^H_{on} and the minimum value of the t^L_{on} depending on the PWM method and output fundamental frequency.

Figure 3 presents an example of some possible evolutions of the t_{on} for PWM methods most used by industry.

It can be seen that the bootstrap method can successfully be used within sinusoidal PWM and Space Vector PWM and that there are some problems when used within 2-phase PWM (discontinuous PWM algorithms). Within these methods, the upper or lower IGBT is not switched for long time intervals (120 or 60 degrees) and this makes almost impossible the use of bootstrap capacitor method at low frequencies. Using the traditional inverter switching notations, a possible

Figure 3: Evolution of the pulse-width for different PWM algorithms

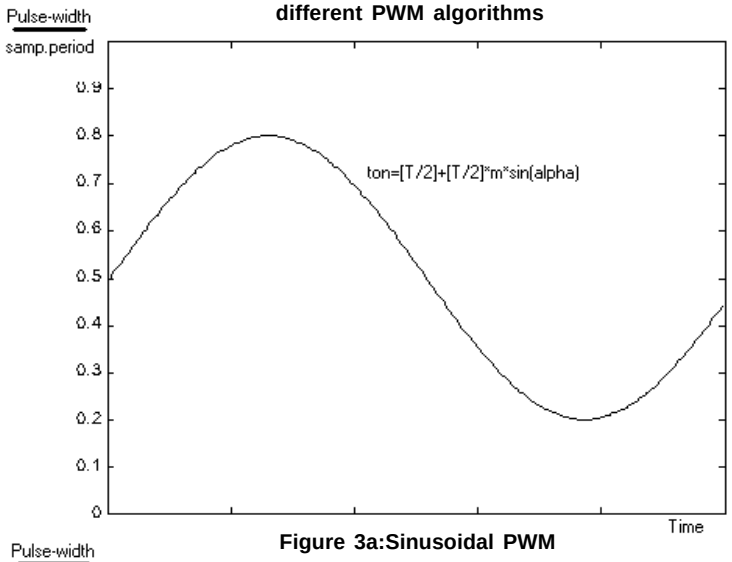

Figure 3a:Sinusoidal PWM

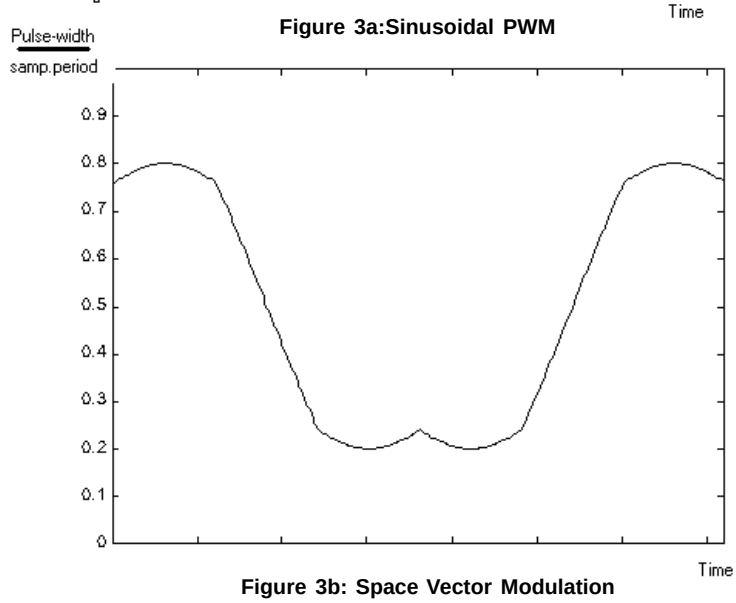

Figure 3b: Space Vector Modulation

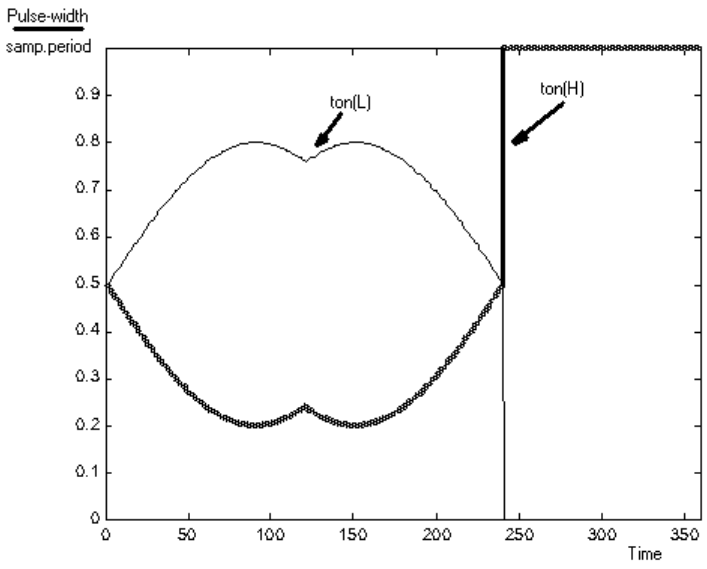

Figure 3c: 2-ph Modulation-A (t^{H}_{on} and t^{L}_{on})

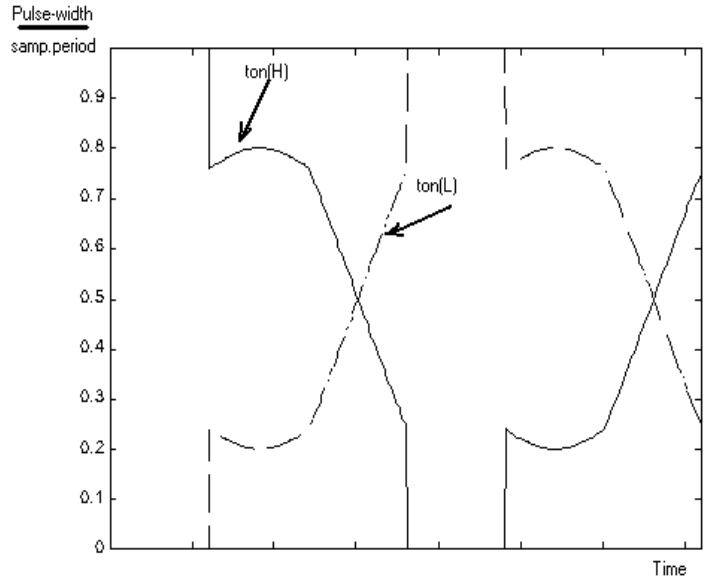

Figure 3d: 2-ph Modulation-B (t^{H}_{on} and t^{L}_{on})

sequence could be: … - 111 - 110 - 010 - 110 – 111 - ... with no switchings of the upper IGBT for 60 or 120 degrees (as shown in Figs.3c and 3d).

However, the discontinuous PWM algorithms demonstrate the advantage of lower inverter losses and many industrial applications take advantage of them. In order to be able to use these methods along with bootstrap capacitor method, the IGBTs should be switched periodically during the no-switching intervals. This means use of 000 state from time to time in low frequency range.

The bootstrap diode is designed based on V_{RRM} and I_F [1]. We recommend choosing diodes with τ_{RR}=50ns.

3. Establishing if IR2137 can be used directly to control an inverter

The first major requirement consists of the gate drive power level. During switching, the IGBT takes power from the gate drive power supply. The amount of the used power is a function of the operating frequency, on and off bias voltages and total gate charge. If we assume that IR2137 is infinitely fast and that its output impedance and inductances are negligible, the average current that must be supplied by the gate drive is:

$$I_G(peak) = \frac{V_{GG}}{R_{G\min}} \qquad (5)$$

The maximum gate currents should be provided under gate output short-circuit conditions and can be 220mA (R_{inIC}=30ohm) at turn-on and 460mA (R_{inIC}=16ohm) at turn-off.

Furthermore, the IR2137 is able to furnish a positive gate voltage only. Performance requirements as (dv/dt) induced shoot-through current, maximum allowable peak current, the desired (dv/dt) of the output phase voltage or power losses within diode and IGBT are considered to designing with IR2137.

The biggest concern when using IR2137 to control IGBT's gate with only positive voltage is related to the shoot-through current that can appear due to (dv/dt) of the turning-on device.

The values of the R_{GON} and R_{GOFF} gate resistors as well as the gate voltage represents degrees of freedom to obtaining desired performance.

Large R_{GON}	decreased EMI by increasing the turn-on time and decreasing the di/dt; decrease I peak and Vpeak during diode recovery
Small R_{GON}	decrease the turn-on losses
Large R_{GOFF}	improve the voltage rise time
Small R_{GOFF}	decrease the dv/dt sensitivity

In order to understand the effects of the Rg resistor, some sample experimental results are next included for an inverter leg equipped with IRG4PH40KD IGBT+D working at 9A (Rgon=Rgoff).

Rg (on/off)	5	30	100	200
dv/dt(off) [V/ns]	6.5	7.2	4.7	3
dv/dt(on) [V/ns]	14	10	6	3.8

4. Criteria for design of the gate resistors

Design of the gate resistors values can be done based on two criteria:

A. efficiency optimization snubberless design

B. low-cost snubberless design with good dynamic performance.

A. Efficiency optimization criteria

Since the gate resistors values are influencing the turn-on, turn-off and conduction losses of IGBT and diode, efficiency optimization can be a design criterium. Equations for power losses are presented in [3]. The main optimal problem consists in choosing between a large value of the gate resistor that would reduce the diode losses and a small value of the gate resistor would reduce the IGBT switching losses. Since there is a difference in the thermal conductivity of the diode and IGBT the optimal problem can be analyzed based on a weighted optimization function:

$$E = \frac{R_{thT} \cdot P_T + R_{thD} \cdot P_D}{P} \qquad (6)$$

B. Good dynamic performance

A low-cost design can be carried out based on simplified constraints as:

- gate driver providing positive voltage only;
- limited available gate peak current;
- minimum ensured (dv/dt)on
- minimum ensured (dv/dt)off
- maximum allowable peak voltage
- avoiding cross—conduction.

The details and equations for each condition can be found on [2].

R_{GON} can be chosen to respect both the design constraints corresponding to the minimum turn-on time (dv/dt) and maximum allowable peak voltage during recovery. However, one can choose within the available surface $R_{GON}(I_L,V_{GE})$, the highest available value of the resistance in order to limit the value of the necessary peak gate current.

R_{GOFF} results from an optimal design involving the condition for avoiding cross-conduction and minimization of turn-off (dv/dt). Once again, a larger value reduces the peak current requirements for the gate driver.

5. Conclusion

This paper presents some design hints for the three-phase gate driver IR2137. This power IC requires bootstrap supplies of the high-side gate drivers and can allow different gate resistors for turn-on and turn-off. Basic design considerations for these functions are detailed herein.

Notations

Q_G - *Gate charge of the high-side IGBT*
$I_{Cbs(leak)}$ - *Bootstrap capacitor leakage current*
Q_{Ls} - *level-shifter(IC) charge required per cycle*
V_{Ls} - *Voltage drop across the low-side IGBT*
t^H_{on} - *Duration of the high-side IGBT on-state*
t^L_{on} - *Duration of the low-side IGBT on-state*
P_T - *Loss power in IGBT*
P_D - *Loss power in diode*
P – *Total output power*
R_{thT} – *Thermal resistance of the IGBT*
R_{thD} – *Thermal resistance of the diode*

REFERENCES

[1] IR IC Designer Manual, DT 98-2
[2] IR IGBT Designer Manual, AN988, AN990
[3] IR IGBT Designer Manual, TPAP-1

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