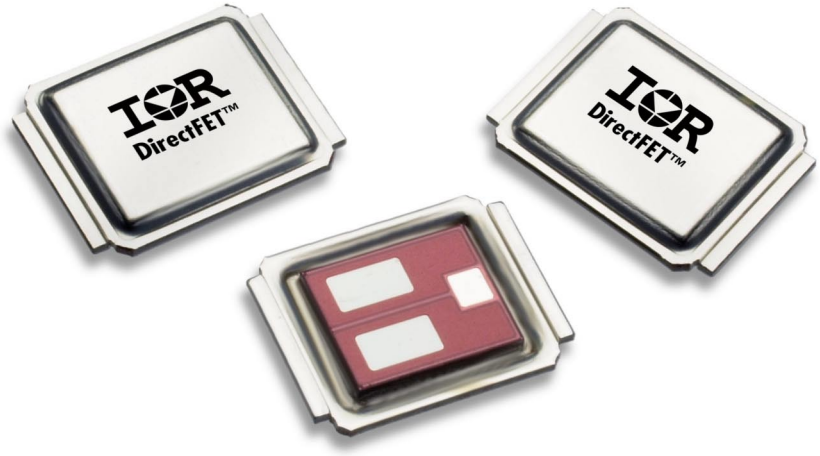
International
IOR Rectifier

AN-1035



DirectFET™ Technology

Board Mounting Application Note

Introduction

DirectFET™ is a new surface mount power semiconductor technology designed primarily for board-mounted power applications. It eliminates unnecessary elements of packaging that contribute to higher inductance and resistance, both thermal and electrical.

There are currently four devices in the DirectFET range: IRF6601, IRF6602, IRF6603 and IRF6604. Similar in size to an SO8, the power capabilities of IRF6601 and IRF6603 far exceed those of comparably sized packages.

Device construction

DirectFET devices use an innovative construction technique to make source and gate connections directly to the die surface (Figure 1). The remainder of the surface is coated with passivation to protect it and to control the position, shape and size of the solder contacts between device and substrate.

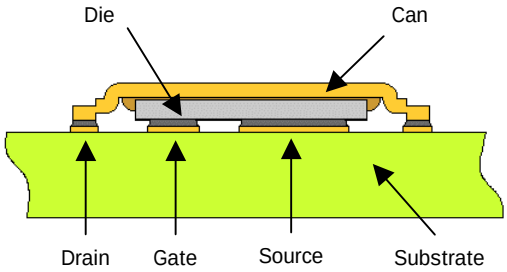


Figure 1 Sectional view

The drain connection is formed by a silver-plated copper can, which is bonded to the drain side of the silicon die. The can has two contact areas, both of which must be soldered to the substrate although one can be used solely as a mechanical anchor.

The shape and size of the can has a significant impact on the device's susceptibility to degradation in thermal cycle testing. It is the result of an extensive program of modeling and testing.

To optimize ease of board mounting and reliability in use, International Rectifier manufactures DirectFET devices to exacting standards. These high standards have evolved through evaluating many different materials and designs. Although such evaluations have yielded good results, the recommendations in this application note may need to be adjusted to suit specific production environments.

Device outline

Figures 2 and 3 show the pad layouts for DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. Source and gate contacts are recessed from the drain contacts, nominally set at 0.050–0.065mm sub-flush (Figure 4). For full dimensions and tolerances of each device, refer to the relevant product data sheet.

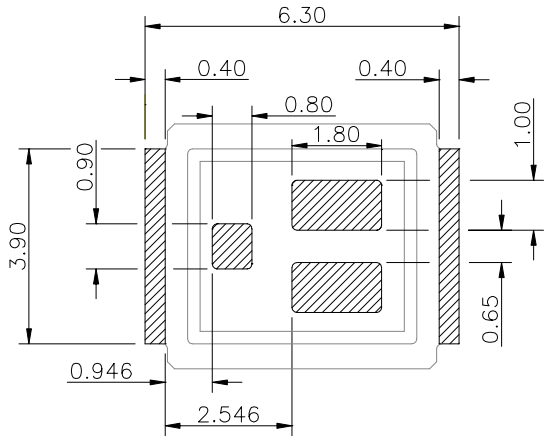


Figure 2 IRF6601 and IRF6603 pad layouts

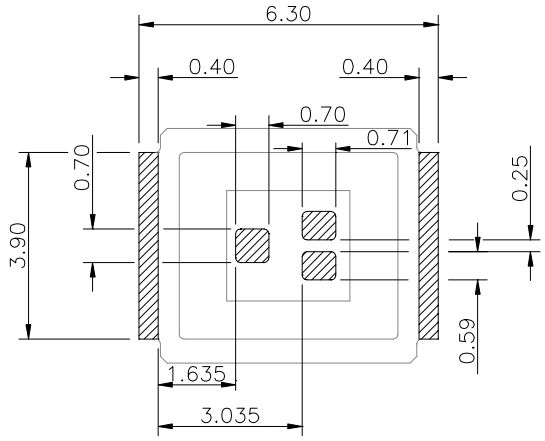


Figure 3 IRF6602 and IRF6604 pad layouts

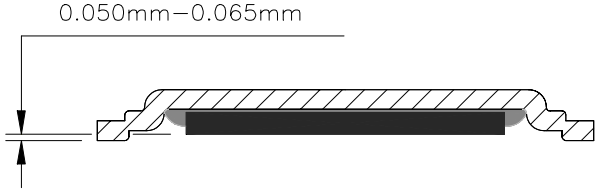
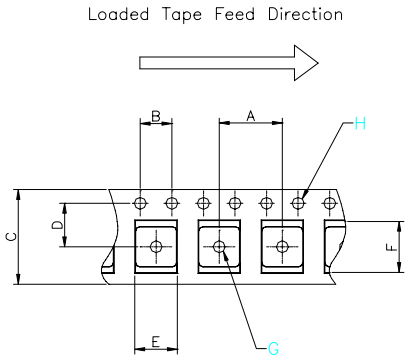


Figure 4 Contact planarity of DirectFET devices

Packaging

DirectFET devices are supplied in tape and reel format (Figure 5).



Note: Controlling dimensions in mm.

DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Figure 5 Tape and reel packaging

The gate contact, marked by a small dot (Figure 6), is furthest from the tape index holes. Pre-production devices have no gate marking or logo but the orientation is the same.

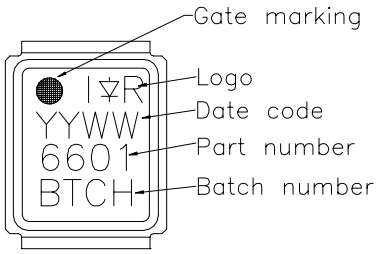


Figure 6 Device markings

Design considerations

Substrates

DirectFET technology was developed for use with epoxy and polyimide glass woven substrates. Evaluations to date have been based on such substrates, finished in electroless nickel immersion gold. However, many other surface finishes are available and DirectFET devices can be used with all of them.

Board Designs

To achieve low-loss track layouts, DirectFET devices were designed for use with solder-mask-defined layouts. Although the devices can be used with pad-defined layouts, these have not been evaluated.

The pad layout of DirectFET devices and the use of solder-mask-defined pads contribute to efficient board design. Large, well-spaced contact areas optimize electrical and thermal performance.

Evaluations have shown that the best overall performance is achieved using the substrate layouts shown in Figures 7 and 8. The gate and source pads on the substrate are oversized by 0.050mm (0.002”) on each side and the drain pads are enlarged in all external directions by 0.150mm (0.006”). Each drain contact pad is divided into two separate pads, which has been shown to improve solder joint quality.

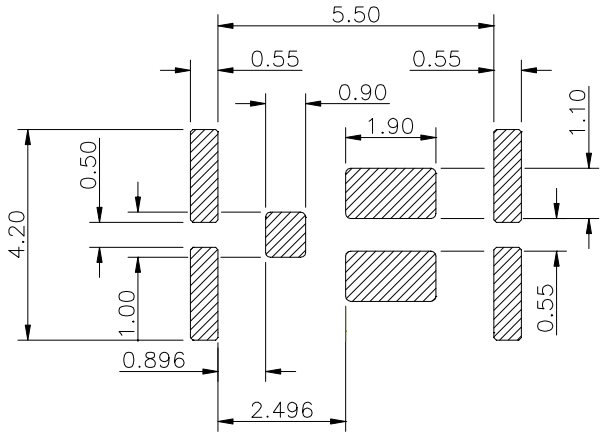


Figure 7 IRF6601 and IRF6603 substrate layouts

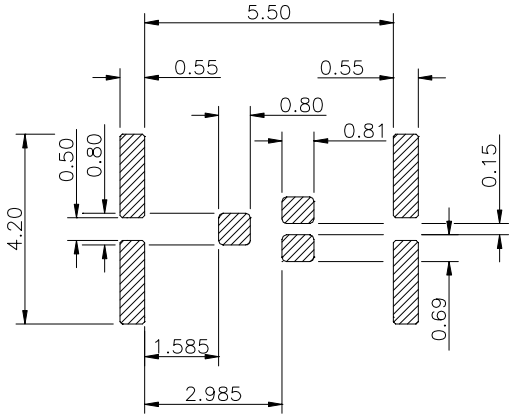


Figure 8 IRF6602 and IRF6604 substrate layouts

DirectFET devices can be placed in parallel using simple layouts (Figure 9). International Rectifier recommends a minimum separation of 0.5mm (0.020”), although this can be adjusted to reflect local process capabilities.

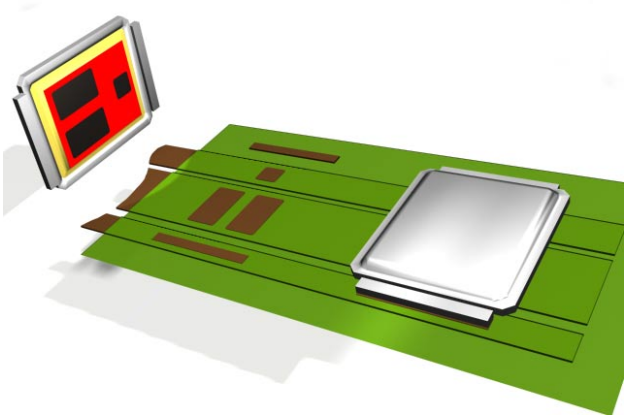


Figure 9 Placing DirectFET devices in parallel

Assembly considerations

International Rectifier designed DirectFET devices to be as easy as possible to assemble. Recessing the gate and source contacts (as shown in Figure 4) helps to overcome the solder balling problems that are often associated with large area array leadless packages. However, procedures and conditions can have a profound influence on assembly quality. This section outlines practices that have given good results during evaluations.

Reflow equipment

DirectFET devices are suitable for assembly using surface mount technology reflowing equipment and are recommended for use with convection, vapor phase and infrared equipment. They have a good resistance to short-term exposure to high temperatures, making them suitable for reflow profiles of up to 270°C (measured on the device). There are no special requirements for successful assembly but all reflow processes used in evaluation and qualification complied with the recommendations of solder paste suppliers.

Solder pastes

International Rectifier evaluated different types of solder paste from various manufacturers. The properties of pastes vary, meaning that some perform better than others with DirectFET devices, but all gave acceptable results.

The rheology of a paste often dictates its suitability for an application and, in general, pastes exhibiting higher viscosity and thixotropy are better with leadless packages because they are less prone to slump and solderballing. DirectFET technology has been evaluated using tin lead alloys Sn62 Pb36 Ag2 and Sn63 Pb37.

Screen design

The device standoff from the substrate (solder thickness) influences resistance to both temperature and power cycling. DirectFET technology is suited to screen thicknesses of 0.100–0.250mm (0.004–0.010”); thinner screens are unsuitable because they deposit insufficient solder to make the recessed gate and source joints.

The screen should be designed to print 1:1 with the board outline since International Rectifier found during evaluations that this did not promote issues with solder balling. However, since screen design is one of the more significant areas for controlling assembly problems such as solder balling and slump, it may be necessary to consider slight reduction or dissimilar stencil designs. Care is needed when reducing print areas as this can lead to insufficient solder volume to complete joints fully.

Device placement

When combined with solder thicknesses of 0.150mm (0.006”) or more, excessive placement pressure may increase the tendency to solder balling. Placement machines have different capabilities and so this is an area for experimentation. The tolerance of DirectFET devices for excessive placement pressure is enhanced by the sub-flush position of the gate and source contacts relative to the drain contacts. If solder balling problems should occur, it may be necessary to review the screen design, solder paste type or both.

Conversely, insufficient placement control or pressure may cause devices to tilt or bonds to be omitted or elongated. This often results from the device not being in intimate contact with the solder paste across all contacts. Devices should ideally be placed to an accuracy of 0.050mm on both X and Y axes. However, during evaluations, devices centered themselves from placement inaccuracies of more than 0.20mm.

Rework guidelines

Modern rework stations for ball grid array and leadless packages often use two heating stages. The first heats the substrate, either with a conventional hot-plate or a hot-air system. The second stage uses a hot-air system for localized heating, often with the option of unheated air for faster cooling of the solder interconnections on the replaced device; this improves the solder grain structure.

The device placement mechanism or arm usually has a hot air de-soldering gun as part of the pick head, equipped with a vacuum cup and thermocouple. Once the solder reflow temperature has been reached, the vacuum is automatically engaged to allow the device to be removed from the substrate. This reduces the risk of causing damage by premature removal.

To replace a DirectFET device:

1. Heat the site to approximately 100°C using the substrate heating stage. This reduces the amount of heating required from the hot air de-soldering tool, which in turn reduces the risk of damaging either the substrate or surrounding components.
2. Lower the placement arm to bring the de-soldering tool into contact with the device. When the device and the solder interconnects reach reflow temperature, lift the placement arm to remove the device from the substrate.
3. Clear residual solder and flux from the site with a blade-type de-soldering tool and de-soldering braid. Take care in cleaning the site: damage to the solder-resist may produce undesirable results. When the site is ready, apply new solder paste with a micro-screen and squeegee.
4. Heat the site to approximately 100°C using the substrate heating stage. Position the new device with the placement arm and then use the de-soldering tool to heat both device and solder interconnects to reflow temperature. Retract the arm, leaving the device in place. Cool as quickly as possible to achieve good grain structure in the new joint.

Mechanical test results

International Rectifier has subjected board-mounted DirectFET devices to extensive mechanical tests, conducted in accordance with industry standards and practices. This section contains summarized results for bend testing, compression testing, drop testing and vibration testing. Full reports are available on request.

Bend tests

Method

These tests were carried out in accordance with BS EN 60068-2-21:1999 Test U: Robustness of terminations and integral mounting devices.

- To gauge relative performance, DirectFET devices were tested against ceramic capacitors of a similar size.
- Substrates were initially tested over knife edges set at 90mm pitch but, as few devices failed, the pitch was changed to 70mm. This meant that the same deflection formed a more acute radius, increasing the strain and reducing the deflection needed to cause failure (13-14mm deflection over 70mm pitch causes approximately the same strain as 25mm deflection over 90mm pitch).
- The speed of deflection was $1mms^{-1}$ for all tests.
- The test board measured 100x40mm and was manufactured from FR4 2oz copper, finished in nickel gold. The solder used was Sn63 Pb37.
- Devices were mounted both longitudinally and transversely, and were tested with the devices mounted on both front and back of the board.

Results

Figures 10 and 11 show the deflection required to cause failure in IRF6601 and IRF6602 devices.

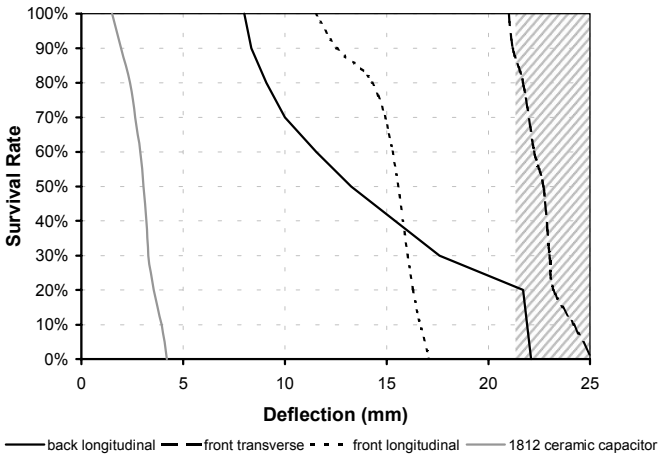


Figure 10 IRF6601 deflection test results

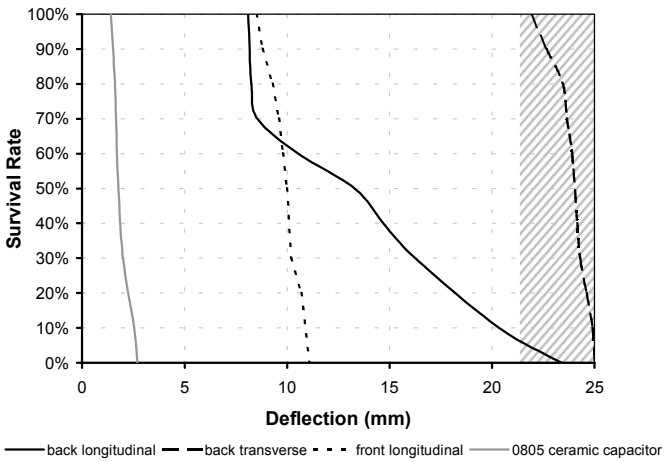


Figure 11 IRF6602 deflection test results

Note: The shaded areas indicate the point at which the substrates failed. No components survived beyond this.

Compression tests

Method

- Tests were carried out at ambient room temperature (22°C).
- Test speed was $0.5mmmin^{-1}$ (return speed of $20mmmin^{-1}$ where applicable).

- Test duration was measured from the point at which 0.05N of force registered on the tester.
- A maximum force of 1750N was used as a termination point for the test.

Continuous pressure:

Pressure was applied to the top of the device until the gate threshold voltage ($V_{g\text{-}th}$) shifted by ±20%.

Stepped pressure:

IRF6601: Pressure was raised to 600N, relieved and the device allowed to return to neutral. The pressure was then raised to 700N and relieved; this process was repeated in steps of 100N until the device failed. The gate threshold was monitored throughout.

IRF6602: The IRF6601 test was replicated but with an initial pressure of 400N and increments of 50N.

Note: Initial pressures were set close to the expected failure point to minimize the number of cycles and, therefore, the fatigue induced by them.

Results

The table below shows the average compression required to cause failure in DirectFET devices.

	IRF6601	**IRF6602**
Continuous	1407N	1204N
Stepped	1106N	663N

Note: Gravity (1g) was assumed to be 9.81ms^{-2}.

Figures 12 shows mortality curves for the survival rate of board-mounted DirectFET devices when increasing pressure is applied to the top surface.

Survival rates are calculated as follows:

$$\text{Survival rate} = \frac{n_{dt} - n_{df}}{n_{dt}} \times 100$$

n_{dt} Number of devices tested
n_{dt} Number of devices failed

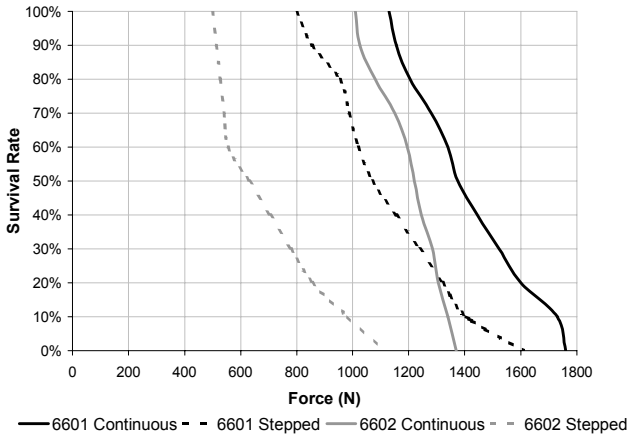


Figure 12 DirectFET survival rates

Drop tests

Methods

These tests were carried out in accordance with BS 2011: Part 2.1 Ed:1992 Test Ed: free fall.

DirectFET devices were dropped onto a steel block from different heights and in five attitudes:

1. On the short edge of the device
2. On the long edge of the device
3. On the corner of the device
4. With device flat, on top of the substrate
5. With the device flat, underneath the substrate

BS 2011 specifies drop heights of 25mm, 50mm, 100mm, 250mm, 500mm and 1000mm. When no devices failed, International Rectifier increased the drop height to 1500mm.

Results

	IRF6601		**IRF6602**	
Drop height (mm)	1000	1500	1000	1500
Attitude 1	0/10	0/10	0/10	0/10
Attitude 2	0/10	0/10	0/10	0/10
Attitude 3	0/10	0/10	0/10	0/10
Attitude 4	0/10	0/10	0/10	0/10
Attitude 5	0/10	0/10	0/10	0/10

Note: 10 devices were tested for each combination of height and attitude. Each device was dropped 20 times.

Vibration tests

Methods

These tests were carried out in accordance with BS 2011: Part 2.1 Fd:1973 Test Fd: random vibration – wide band general requirements.

DirectFET devices were subjected for three hours to random vibrations from 20Hz to 2kHz, experiencing 3.2g_{rms} (31.4ms$^{-2}{}_{rms}$) with an acceleration spectral density value of 0.005g^2Hz^{-1} ([0.48ms^{-2}] $^2Hz^{-1}$). Figure 13 shows the bandpass filter frequency chart.

The devices were tested in three attitudes:

1. On the short edge of the device
2. On the long edge of the device
3. With device flat, on top of the substrate

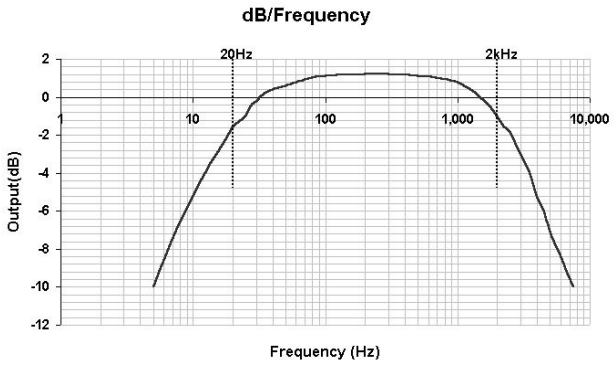


Figure 13 Bandpass filter frequency chart

Results

	6601
Attitude 1	0/16
Attitude 2	0/16
Attitude 3	0/16

Note: 16 devices were tested in each attitude.

Acknowledgements

International Rectifier would like to thank:

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Further reading

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Manko, Howard H (4th edn) *Solders and Soldering*. McGraw-Hill. ISBN 0-07-134417-9.

Prasad, Ray P (2nd edn) *Surface Mount Technology*. Kluwer Academic Publishers. ISBN 0-412-12-12921-3.

Frear, D R; Vianco, P T (1994) 'Intermetallic Growth and Mechanical Behavior of Low and High Melting Temperature Solder Alloys', *Metallurgical and Materials Transactions A*. Vol 25A pp1509-1523 July 1994.

Standards

BS EN 60068-2-21:1999 / IEC 60068-2-21:1999
Environmental testing – Part 2-21 Test U:
Robustness of terminations and integral mounting devices.
ICS 19.040

BS 2011: Part 2.1 Fd:1973
Basic environmental testing procedures – Part 2.1 Test Fd:
random vibration – wide band general requirements.

BS 2011: Part 2.1 Ed:1992 / IEC 68-2-32:1975
Environmental testing – Part 2.1 Test Ed: free fall.