This document should be printed in color to best view delineations on graphs.

Optimizing a PCB Layout for an *i*POWIR™ Technology Design

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Introduction

Though *i*POWIR™ technology based designs represent a unique class of power solutions, the design of a proper printed circuit board (PCB) can be a simple but effective means of optimizing the performance of an *i*POWIR solution. In general, there are a number of issues that need considering when designing a layout for a power supply design. These issues are applicable to both discrete and *i*POWIR solutions. This application note will describe how to optimize the layout design for both thermal and electrical properties.

Method

Recommended Footprint

An *i*POWIR solution must be mated to a proper PCB footprint. This will insure good electrical, thermal, and mechanical connections and will assure a reliable product.

Land pads on the PCB should be solder mask defined. The solder mask openings for the land pads are typically 80% of the solder ball diameter. This will provide the optimum standoff height[1].

Placement

Electrical

It is a fundamental design practice to keep the input and output filters close to the power switches in a synchronous buck design. This general rule also applies to designs using *i*POWIR technology (see Figure 1). The advantage of an *i*POWIR solution is that it's not as sensitive to layout conflicts as a discrete solution because it integrates capacitance for the input voltage lines.

*i*POWIR technology integrates high-speed power MOSFETs capable of switching voltages at rates of 2kV/µs. Therefore, input capacitors should have first priority during placement after the *i*POWIR block. Minimizing the distance between the bulk input caps and the *i*POWIR module reduces any ringing due to stray inductance during switching.

Output inductor and filter caps placement have a second order of importance. Placement should be relatively close to the *i*POWIR block, but it is not critical.

Thermal

Maintaining adequate distances between heat generating sources is an essential design practice. Knowing exactly how much distance is needed requires characterizing and understanding of your thermal environment[2].

Even though *i*POWIR technology has higher power density than a discrete solution, it does not allow for higher dissipation density on your PCB design. For example, if an *i*POWIR solution dissipating 5W will replace a discrete solution dissipating 5W, then the same amount of thermal mass and dissipation density is required in the PCB design. This assumes the PCB could only dissipate 5W and has no design margin.

Routing

*i*POWIR technology dissipates most of its heat generated by power loss through the PCB connection. Very little will dissipate off the top of the device. Therefore, it is critical that the PCB design be optimized to conduct heat.

Copper Pour

Use the following steps when designing the copper layers in your PCB design. Refer to Figure 1 for details:

1. Use large copper planes as interconnects between common-node solder balls instead of tracks.
2. Do not use thermal relieves.
3. Expand the copper on the high current nodes[3] wherever possible and mirror the layout to other layers. This will help increase the surface area for convective cooling and reduce the I^2R losses.
4. Use multiple vias as interconnect between layers for high current nodes.
5. Fill unused areas/layers with copper. This will help increase the board's total thermal mass.
6. Use thickest allowable copper (1oz to 2oz), especially on outer layers.

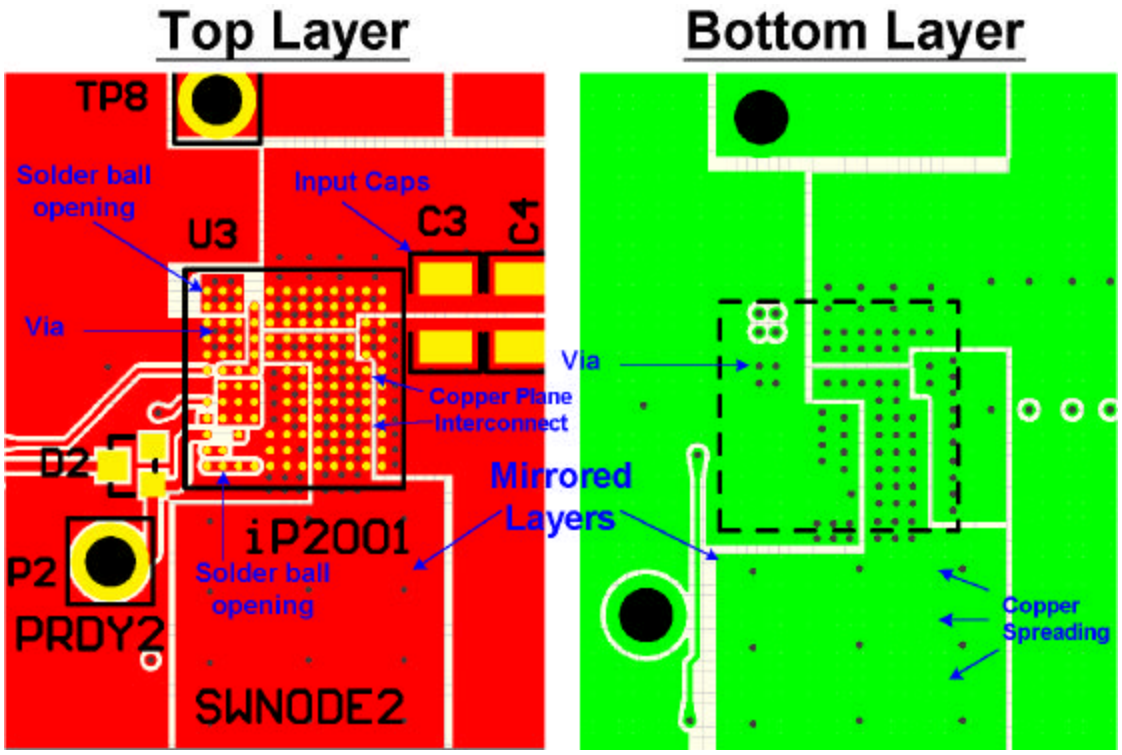

Figure 1

Via Interconnects

Use vias wherever possible for both electrical and thermal purposes. Standard vias can be used throughout the PCB design, but via type and placement around and underneath the *i*POWIR block requires special attention. The following will describe how to optimize the use of vias for an *i*POWIR block during a PCB design.

Via Types

Two types of vias used in PCB design are discussed in this application note (see Figure 2).

A. Example **A** shows a standard via with an exposed capture land. Do not use this type of via underneath the *i*POWIR block. The exposed metal opening will allow solder to wick down the via barrel from the solder ball, causing the solder ball to loose its structure. Furthermore when placing this type of via around the perimeter of the *i*POWIR block, there needs to be a minimum of 12 mils of solder mask from the via opening to the nearest solder ball opening.

B. Example **B** shows a standard via with a tented capture land. Solder mask is used to cover both the via hole and land capture. This type of via is allowed underneath and around the *i*POWIR block. Placement is the only critical issue, which is discussed later in this application note.

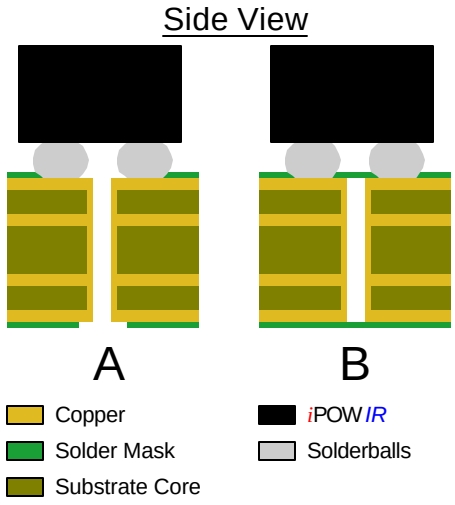

Figure 2

Via Placement

Use only example **B** style vias during the placement. Center the via between the footprint pad of four solder balls with the same node (see Figure 3). Repeat this throughout the footprint area of the common-node solder balls. Vias

should also be placed around the perimeter of the *i*POWIR block.

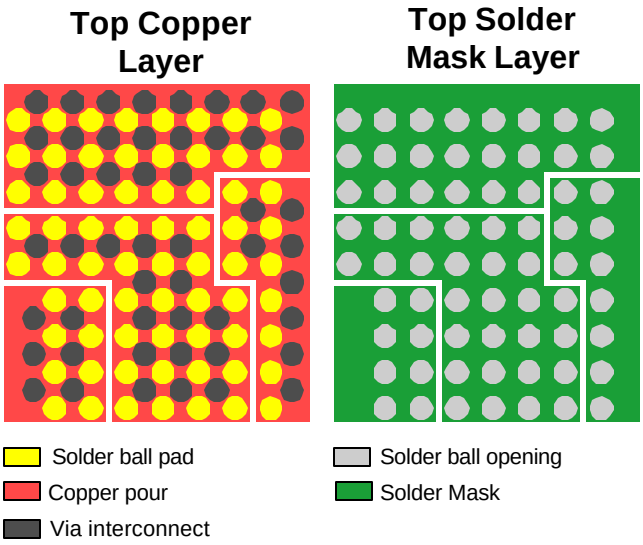

Figure 3

A via with a 25mil capture land is the maximum size allowed between the solder ball pads. The via drill hole size for 25mil capture land is typically 13mils or smaller.

Preview the top solder mask layer with a Gerber or Cad viewer. Verify the solder mask layer area underneath the *i*POWIR™ block shows only the solder ball openings and not the via capture opening (see Figure 3).

Final PCB

Applying all the design tips described earlier creates a heat sink for the *i*POWIR block through the PCB design (see Figure 4). Heat generated by the *i*POWIR block will conduct through the solder balls and down onto the top layer of the system board. A proper PCB design will then spread the heat throughout the top layer, down through the via, spread to inner & bottom layers, and finally spread throughout the substrate core.

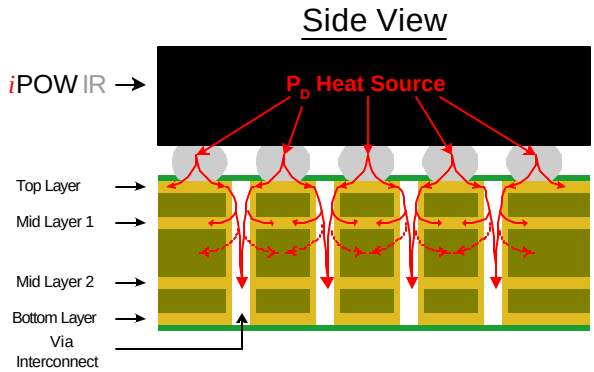

Figure 4

Summary

*i*POWIR technology dissipates most of its heat generated by power loss through the PCB connection. Very little is dissipated off the top of the device. A properly designed PCB will minimize the I^2R losses and act as a heat sink for the *i*POWIR block to provide optimal thermal performance.

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[1] Refer to AN-1028 "Recommended Design, Integration, and Rework Guidelines for International Rectifier's *i*POWIR™ technology BGA Packages" application note for further detailed information on footprint and mounting instructions.

[2] Refer to AN-1030 "Appling *i*POWIR™ products in your thermal environment" application note for further detailed information on thermal characterizing your PCB.

[3] High current nodes: 1) Voltage input node (V_{IN}); 2) Switching node (V_{SW}); 3) Power ground node (P_{GND})