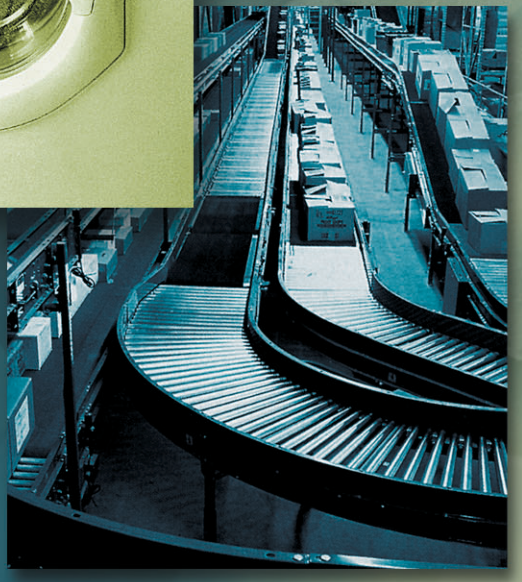
International
IOR Rectifier
THE POWER MANAGEMENT EXPERTS

Motor Drive and Inverter Designer's Manual

INCLUDING IGBTs, FETs, RECTIFIERS & GATE DRIVER ICs





2002

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High & Low Side Driver ICs
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IGBTs (Discrete & Co-Pack) 1kW - 6.5kW
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Single High Side Driver ICs
Three-Phase Bridge Driver ICs
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FAST DIODE DIE DATA SHEETS

IR060LM06CS02CB
IR060PM12CS02CB
IR135LM06CS02CB
IR180LMCS02CB Series
IR180LMCS05CB Series
IR207LM..CSO2CB
IR230LM06CS2CB
IR340LM..CS05CB
IR390LM..CS05CB

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FRED DIE DATA SHEETS

FD087U02A5B
FD100H06A5B
FD120H06A5B
FD160H06A5B
FD200H02A5B
FD200H06A5B

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HEXFET® POWER MOSFET DIE DATA SHEETS





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IRFC044
IRFC1404
IRFC240
IRFC2907
IRFC2907B
IRFC43N50KB

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HEXFRED® RECTIFIER DIE DATA SHEETS





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HF06A060ACE
HF10A060ACB
HF10A060ACE
HF20A060ACE
HF20C120ACE
HF30A060ACE
HF30C120ACB
HF30C120ACE
HF30D120ACE
HF40A060ACB
HF40A060ACE
HF4C120ACB
HF40C120ACE
HF40D120ACE
HF42A040SCE
HF42A060SCE
HF50A060ACB
HF50A060ACE
HF50C120ACE
HF50D120ACE
HF51A060ACE
HF51C120ACE
HF70D120ACE
HF72D120ACE

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IC DATA SHEETS





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IR2101/IR2102 (S)
IR2103 (S)
IR2104 (S)
IR2106(4) (S)
IR2108(4) (S)
IR2109(4) (S)
IR2110/IR2113 (S)
IR2111
IR2112 (S)
IR2117/IR2118 (S)
IR2121
IR2122 (S)
IR2125 (S)
IR2127(1)/IR2128 (S)
IR2130/IR2132 (J) (S)
IR2131 (J) (S)
IR2133/IR2135/IR2233/IR2235 (J) (S)
IR2136/IR21362 (J) (S)
IR2137/IR2237 (J) (Q)
IR2170
IR2171/IR2172
IR2181(4) (S)
IR2183(4) (S)
IR2184(4) (S)
IR2213 (S)
IR4426/IR4427/IR4428

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IGBT DIE DATA SHEETS

IRG4CC10KB
IRG4CC10SB
IRG4CC10UB
IRG4CC20FB
IRG4CC20KB
IRG4CC20MB
IRG4CC20RB
IRG4CC20UB
IRG4CC30FB
IRG4CC30KB
IRG4CC30SB
IRG4CC30UB
IRG4CC40FB
IRG4CC40KB
IRG4CC40RB
IRG4CC40SB
IRG4CC40UB
IRG4CC40WB
IRG4CC50FB
IRG4CC50KB
IRG4CC50SB
IRG4CC50UB
IRG4CC50WB
IRG4CC58KB
IRG4CC70UB
IRG4CC71KB
IRG4CC72KB
IRG4CC77KB
IRG4CC81KB
IRG4CC81UB
IRG4CC88KB
IRG4CH20KB
IRG4CH30KB
IRG4CH40KB
IRG4CH40SB
IRG4CH40UB
IRG4CH50KB
IRG4CH50SB
IRG4CH50UB
IRGC5B120KB
IRGC5B120UB
IRGC8B120KB
IRGC8B120UB
IRGC15B120KB
IRGC15B120UB
IRGC25B120KB
IRGC25B120UB
IRGC50B120KB
IRGC50B120UB
IRGC75B120KB
IRGC75B120UB
IRGC100B120KB
IRGC100B120UB

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IGBT MODULES FOR MOTOR DRIVES & UPS





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GA75TS60U
GA100TS60U
GA150KS61U
GA150TS60U
GA200NS61U
GA200TS60U
GA200SA60S
GA200SA60U
GA250TS60U
GA300TD60U
GA400TD60U
GA500TD60U
GA50TS120U
GA75TS120U
GA100TS120U
GA125TS120U
GA150TD120U
GA200TD120U
GA250TD120U

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IGBT MODULES FOR MOTOR DRIVES IN INDUSTRIAL ELECTRIC VEHICLES





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GA600GD255

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IGBTs - DISCRETE & CO-PACK FOR MOTOR DRIVES & UPS up to 10kW





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IRG4PC50S
IRG4PC50F
IRG4PC50FD
IRG4PSC71K
IRG4PSC71KD
IRG4PSC71U
IRG4PSC71UD
IRGP20B120U-E
IRGP20B120UD-E
IRG4PH50K
IRG4PH50KD
IRG4PH50U
IRG4PH50UD
IRG4PH50S
IRGP30B120KD-E
IRG4PSH71K
IRG4PSH71KD
IRGPS40B120U
IRGPS40B120UD
IRGPS60B120KB

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IGBTs - DISCRETE & CO-PACK FOR MOTOR DRIVES & UPS 1kW - 6.5kW





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IRG41BC30FD
IRG4RC20F
IRG4BC30U
IRG4BC30UD
IRG4PC30U
IRG4PC30UD
IRG4BC30U-S
IRG4BC30K-S
IRG4BC30KD-S
IRG4BC30K
IRG4BC30KD
IRG4PC30K
IRG4PC30KD
IRG4BC30F
IRG4BC30FD
IRG4PC30F
IRG4PC30FD
IRG4BC30S-S
IRG4BC30S
IRG4PC30S
IRG4BC40U
IRG4PC40U
IRG4PC40UD
IRG4BC40K
IRG4PC40K
IRG4PC40KD
IRG4BC40F
IRG4PC40F
IRG4PC40FD
IRG4PC50K
IRG4PC50KD
IRG4PC50U
IRG4PC50UD
IRG4BC40S
IRG4PC40S
IRG4BH20K-S
IRG4PH20K
IRG4PH20KD
IRG4BH20K-L
IRG4PH30K
IRG4PH30KD
IRG4PH40K
IRG4PH40KD
IRG4PH40U
IRG4PH40UD

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IGBTs - DISCRETE & CO-PACK FOR MOTOR DRIVES & UPS < 2kW





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IRG41BC10UD
IRG4RC10U
IRG4BC10UD
IRG4RC10K
IRG4BC10K
IRG4BC10KD
IRG4BC15UD-S
IRG4BC15UD
IRG41BC20UD
IRG41BC20KD
IRG4BC20UD-S
IRG4BC20U
IRG4BC20UD
IRG4RC10S
IRG4BC10S
IRG4BC10SD

IRG41BC20FD
IRG4BC20FD-S
IRG4BC20K-S
IRG4BC20KD-S
IRG4BC15MD
IRG4BC20FD
IRG4BC20F
IRG4BC20K
IRG4BC20KD
IRG41BC30KD
IRG41BC30UD
IRG4BC20MD-S
IRG4BC20MD
IRG4BC20SD-S
IRG4BC20S
IRG4BC20SD

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INPUT DIODE DIE DATA SHEETS

IR135DM16CCB
IR135DM12CCB
IR150DG12HCB
IR180DGH..HCB
IR180DM16CCB
IR180DM..CCB Series
IR207DM16CCB
IR210DG..HCB
IR230DGH
IR230DM12CCB
IR230DM16CCB
IR280DGH
IR350DG..HCB
IR350DM..CCB
IR480DGH

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THYRISTOR DIE DATA SHEETS

IR180SG...HCB
IR185BG08DCB
IR185BG12DCB
IR210SGH...HCB
IR230SGH..HCB
IR250BG ..DCB
IR250SG12HCB
IRG255SGH...HCB
IRG343SG12H
IR350SG12HCB
IR370SG..HCB
IR480BG...DCB
IRG480SG..HCB Series
IR590SG12HCB

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MOSFETS FOR MOTOR DRIVES IN INDUSTRIAL ELECTRIC VEHICLES





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IRFBA1404P
IRF1404
IRF1404S/L
IRF1405S/L
IRFP2907
IRF3415
IRF3415S/L
IRFP3415
IRF3710
IRF3710S/L
IRFPS3810

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SCHOTTKY DIE DATA SHEETS

SC021_5
SC036_5
SC050_5
SC060_5
SC070_5
SC095_5
SC100_5
SC105_5
SC170_5
SC180_5
SC200_5
SC275S030

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WARP Speed™ IGBTS FOR PFC IN MOTOR DRIVES & UPS





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IRG41BC20W
IRG4BC20W
IRG41BC30W
IRG4BC30W
IRG4BC30W-S
IRG4BC40W
IRG4PC40W
IRG4PC50W
IRG4PF50W

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AN-804	Determination of Available Fault Current for Semiconductor Fusing
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DT92-2A High Current Buffer for Control ICs

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REFERENCE DESIGNS

IRMDAC2 3-Phase 230VAC IR2133
IRMDAC3 3-Phase 460VAC IR2233
IRMDAC4 3-Phase 230VAC IR2137/IR2171

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TECHNICAL PAPERS

Power Conversion Processor Architecture

Solving IGBT protection in the AC or BLDC Motor Drive

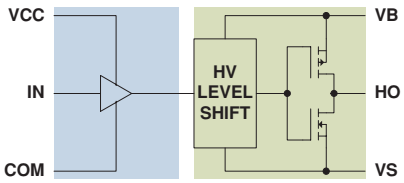
New Monolithic High Voltage Current Sensing IC Simplifies AC Drive Integration

Half-Bridge Drivers

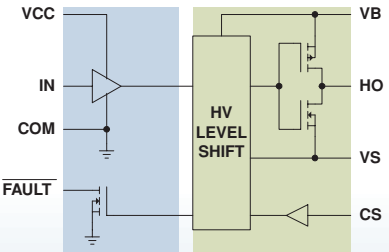
ALL FEATURE SOFT TURN ON

Output Source/ Sink Current	V_{CC} Range	V_{BS} Range	V_O Swing	Deadtime	Features	Part #	Package
UP TO 600V — IR2108							
+120 / -250 mA	10 - 25V with Under-Voltage Lockout	10 - 25V with Under-Voltage Lockout	Output Swing = Supply Voltage	Fixed 500 ns	Separate High and Low Side Inputs 3.3V, 5V, and 15V Logic Compatible Min. Deadtime Fixed at 500 ns	IR2108 IR2108S	8-Lead PDIP 8-Lead SOIC
				Set by External R 0.5 - 5 µs	Same As 2108 Plus All High Voltage Pins on One Side Separate Logic and Power Ground	IR21084 IR21084S	14-Lead PDIP 14-Lead SOIC
UP TO 600V — IR2109							
+120 / -250 mA	10 - 25V with Under-Voltage Lockout	10 - 25V with Under-Voltage Lockout	Output Swing = Supply Voltage	Fixed 500 ns	Single Input Plus Shutdown 3.3V, 5V, and 15V Logic Compatible Min. Deadtime Fixed at 500 ns	IR2109 IR2109S	8-Lead PDIP 8-Lead SOIC
				Set by External R 0.5 - 5 µs	Same As 2109 Plus All High Voltage Pins on One Side Separate Logic and Power Ground	IR21094 IR21094S	14-Lead PDIP 14-Lead SOIC
UP TO 600V — IR2183							
+1.7 / -1.7A	10 - 25V with Under-Voltage Lockout	10 - 25V with Under-Voltage Lockout	Supply Voltage -1.2V	Fixed 500 ns	Separate High and Low Side Inputs 3.3V, 5V, and 15V Logic Compatible Min. Deadtime Fixed at 500 ns	IR2183 IR2183S	8-Lead PDIP 8-Lead SOIC
				Set by External R 0.5 - 5 µs	Same As 2183 Plus All High Voltage Pins on One Side Separate Logic and Power Ground	IR21834 IR21834S	14-Lead PDIP 14-Lead SOIC
UP TO 600V — IR2184							
+1.7 / -1.7 A	10 - 25V with Under-Voltage Lockout	10 - 25V with Under-Voltage Lockout	Supply Voltage -1.2V	Fixed 500 ns	Single Input Plus Shutdown 3.3V, 5V, and 15V Logic Compatible Min. Deadtime Fixed at 500 ns	IR2184 IR2184S	8-Lead PDIP 8-Lead SOIC
				Set by External R 0.5 - 5 µs	Same As 2184 Plus All High Voltage Pins on One Side Separate Logic and Power Ground	IR21844 IR21844S	14-Lead PDIP 14-Lead SOIC

SINGLE HIGH SIDE DRIVERS



IR2117

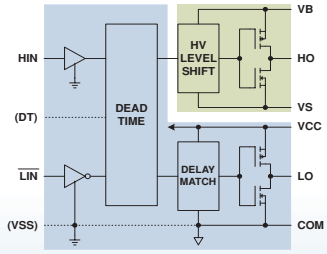


IR2127

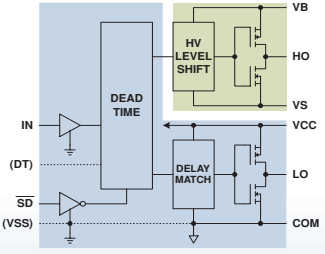
High and Low Side Drivers

Output Source/ Sink Current	V_{CC} Range	V_{BS} Range	V_O Swing	Delay Matching	Features	Part #	Package
UP TO 600V — IR2106							
+120 / -250 mA	10 - 25V with Under-Voltage Lockout	10 - 25V with Under-Voltage Lockout	Output Swing = VBS Supply Voltage	50 ns max	Soft Turn-On High and Low Side Driver Noninverting Inputs Compatible with 3.3V, 5V, and 15V Logic	IR2106 IR2106S	8-Lead PDIP 8-Lead SOIC
					Same As 2106, Plus All High Voltage Pins on One Side, Separate Logic and Power Ground	IR21064 IR21064S	14-Lead PDIP 14-Lead SOIC
UP TO 600V — IR2110 (500V) / IR2113 (600V)							
+2.0 / -2.0A	10 - 25V with Under-Voltage Lockout	10 - 25V with Under-Voltage Lockout	Supply Voltage -1.2V	10 ns max	Fast, High Output Current Noninverting Inputs 5 - 20V Separate Logic Supply Shutdown Input	IR211X IR211XS	14-Lead PDIP 16-Lead SOIC
UP TO 600V — IR2112							
+200 / -420 mA	10 - 25V with Under-Voltage Lockout	10 - 25V with Under-Voltage Lockout	Output Swing = Supply Voltage	30 ns max	Noninverting Inputs 5 - 20V Separate Logic Supply Shutdown Input	IR2112 IR2112S	14-Lead PDIP 16-Lead SOIC
UP TO 600V — IR2181							
+1.7 / -1.7A	10 - 25V with Under-Voltage Lockout	10 - 25V with Under-Voltage Lockout	Supply Voltage -1.2V	50 ns max	Soft Turn-On High and Low Side Driver Noninverting Inputs Compatible with 3.3V, 5V, and 15V Logic	IR2181 IR2181S	8-Lead PDIP 8-Lead SOIC
					Same As 2181 Plus All High Voltage Pins on One Side Separate Logic and Power Ground	IR21814 IR21814S	14-Lead PDIP 14-Lead SOIC
UP TO 1200V — IR2213							
+1.7 / -2.0A	12 - 25V with Under-Voltage Lockout	12 - 25V with Under-Voltage Lockout	Supply Voltage -1.2V	30 ns max	Fast, High Output Current Noninverting Inputs 5 - 20V Separate Logic Supply Shutdown Input	IR2213 IR2213S	14-Lead PDIP 16-Lead SOIC (Wide Body)

HALF BRIDGE DRIVERS

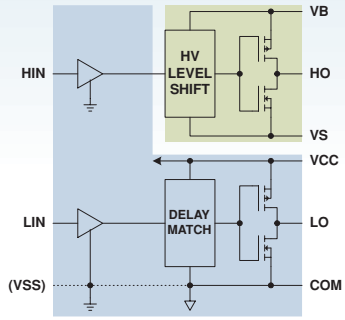


IR2108

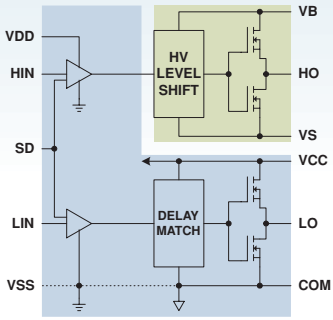


IR2109

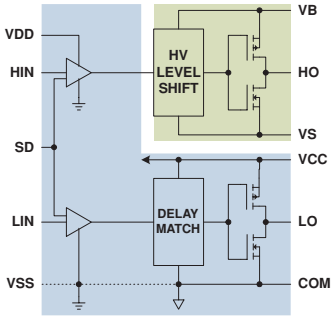
HIGH AND LOW SIDE DRIVERS



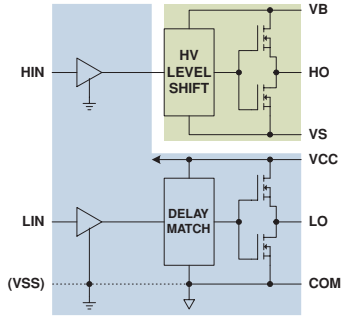
IR2106



IR2110/13/2213

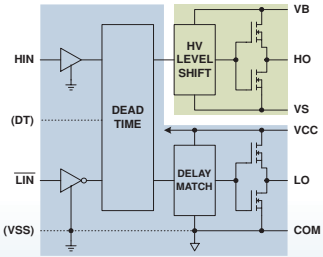


IR2112

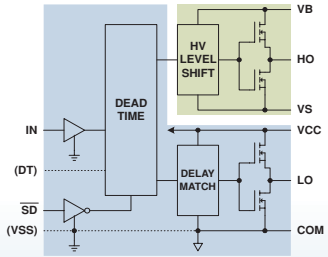


IR2181

HALF BRIDGE DRIVERS



IR2183



IR2184

IGBT Modules for Motor Drive and UPS

Part #	Package	Circuit Type	Speed	BV_{CES} (V)	$V_{CE(ON)}$ (V)	I_C @ 25°C (A)	Power Level (max) (kW)	APPLICATION: INDUSTRIAL	APPLICATION: UPS
GA75TS60U	INT-A-PAK	Half Bridge	Ultrafast	600	2.2	75	6.5 to 8.5		•
GA100TS60U	INT-A-PAK	Half Bridge	Ultrafast	600	2.1	100	7.5 to 10.0		•
GA150KS61U	INT-A-PAK	Chopper	Ultrafast	600	1.7	150	10.0 to 12.0	•	•
GA150TS60U	INT-A-PAK	Half Bridge	Ultrafast	600	2.3	150	10.0 to 12.0	•	•
GA200NS61U	INT-A-PAK	Chopper	Ultrafast	600	1.8	200	12.0 to 15.0		•
GA200TS60U	INT-A-PAK	Half Bridge	Ultrafast	600	2.2	200	12.0 to 15.0	•	•
GA200SA60S	SOT-227	Single	Standard	600	1.3	200	12.0 to 15.0	•	•
GA200SA60U	SOT-227	Single	Ultrafast	600	1.9	200	12.0 to 15.0		•
GA250TS60U	INT-A-PAK	Half Bridge	Ultrafast	600	2.3	250	15.0 to 18.0	•	•
GA300TD60U	Dual INT-A-PAK	Half Bridge	Ultrafast	600	2.3	300	18.0 to 30.0		•
GA400TD60U	Dual INT-A-PAK	Half Bridge	Ultrafast	600	2.4	400	30.0 to 40.0		•
GA500TD60U	Dual INT-A-PAK	Half Bridge	Ultrafast	600	2.4	500	40.0 to 50.0		•
GA50TS120U	INT-A-PAK	Half Bridge	Ultrafast	1200	3	50	8.0 to 10.0	•	•
GA75TS120U	INT-A-PAK	Half Bridge	Ultrafast	1200	3.1	75	10.0 to 15.0	•	•
GA100TS120U	INT-A-PAK	Half Bridge	Ultrafast	1200	2.9	100	15.0 to 20.0	•	•
GA125TS120U	INT-A-PAK	Half Bridge	Ultrafast	1200	3	125	20.0 to 25.0	•	•
GA150TD120U	Dual INT-A-PAK	Half Bridge	Ultrafast	1200	2.9	150	25.0 to 30.0	•	•
GA200TD120U	Dual INT-A-PAK	Half Bridge	Ultrafast	1200	2.8	200	30.0 to 40.0	•	•
GA250TD120U	Dual INT-A-PAK	Half Bridge	Ultrafast	1200	2.9	250	40.0 to 50.0	•	•

Discrete and Co-Pack IGBTs for Motor Drives and UPS up to 10kW

Part #	Package	Circuit Type	Speed	BV_{CES} (V)	$V_{CE(ON)}$ (V)	I_C @ 25°C (A)	Power Level (max) (kW)	APPLICATION: INDUSTRIAL	APPLICATION: UPS
IRG4PC50S	TO-247AC	Discrete	Standard	600	1.36	70	4.0 to 8.0	•	
IRG4PC50F	TO-247AC	Discrete	Fast	600	1.6	70	4.0 to 8.0		•
IRG4PC50FD	TO-247AC	CoPack	Fast	600	1.6	70	4.0 to 8.0		•
IRG4PSC71K	Super-247™	Discrete	Ultrafast*	600	2.3	85	5.0 to 10.0	•	
IRG4PSC71KD	Super-247™	CoPack	Ultrafast*	600	2.3	85	5.0 to 10.0	•	
IRG4PSC71U	Super-247™	Discrete	Ultrafast	600	2	85	5.0 to 10.0		•
IRG4PSC71UD	Super-247™	CoPack	Ultrafast	600	2	85	5.0 to 10.0		•
IRGP20B120U-E	TO-247AC	Discrete	Ultrafast*	1200	3.45	40	5.0 to 10.0	•	•
IRGP20B120UD-E	TO-247AC	CoPack	Ultrafast*	1200	3.05	40	5.0 to 10.0	•	•
IRG4PH50K	TO-247AC	Discrete	Ultrafast*	1200	3.5	45	4.0 to 8.0	•	
IRG4PH50KD	TO-247AC	CoPack	Ultrafast*	1200	3.5	45	4.0 to 8.0	•	
IRG4PH50U	TO-247AC	Discrete	Ultrafast	1200	3.7	45	4.0 to 8.0		•
IRG4PH50UD	TO-247AC	CoPack	Ultrafast	1200	3.7	45	4.0 to 8.0		•
IRG4PH50S	TO-247AC	Discrete	Standard	1200	1.7	57	4.0 to 8.0		•
IRGP30B120KD-E	TO-247AC	CoPack	Ultrafast*	1200	2.28	60	8.0 to 12.0	•	
IRG4PSH71K	Super-247™	Discrete	Ultrafast*	1200	3.9	78	5.0 to 10.0	•	
IRG4PSH71KD	Super-247™	CoPack	Ultrafast*	1200	3.9	78	5.0 to 10.0	•	

** 10µs short circuit capability*

Standard: DC – 1kHz; Fast: 2 -10 kHz; Ultrafast: 8 - 20 kHz

Discrete and Co-Pack IGBTs for Motor Drives and UPS 1kW – 6.5kW

Part #	Package	Circuit Type	Speed	BV_{CES} (V)	$V_{CE(ON)}$ (V)	I_C @ 25°C (A)	Power Level (max) (kW)	APPLICATION: APPLIANCE	INDUSTRIAL	UPS
IRG4IBC30FD	TO-220 FullPak	CoPack	Fast	600	1.8	20.3	1.0 to 2.5			•
IRG4RC20F	D-Pak	Discrete	Fast	600	2.1	22	1.0 to 2.5			•
IRG4BC30U-S	D²Pak	Discrete	Ultrafast	600	1.95	23	1.0 to 2.5	•	•	
IRG4BC30U	TO-220AB	Discrete	Ultrafast	600	2.1	23	1.0 to 2.5		•	
IRG4BC30UD	TO-220AB	CoPack	Ultrafast	600	2.1	23	1.0 to 2.5		•	•
IRG4PC30U	TO-247AC	Discrete	Ultrafast	600	2.1	23	1.0 to 2.5		•	•
IRG4PC30UD	TO-247AC	CoPack	Ultrafast	600	2.1	23	1.0 to 2.5		•	•
IRG4BC30K-S	D²Pak	Discrete	Ultrafast*	600	2.7	28	1.0 to 2.5		•	
IRG4BC30KD-S	D²Pak	CoPack	Ultrafast*	600	2.7	28	1.0 to 2.5		•	
IRG4BC30K	TO-220AB	Discrete	Ultrafast*	600	2.7	28	1.0 to 2.5		•	
IRG4BC30KD	TO-220AB	CoPack	Ultrafast*	600	2.7	28	1.0 to 2.5		•	
IRG4PC30K	TO-247AC	Discrete	Ultrafast*	600	2.7	28	1.0 to 2.5		•	
IRG4PC30KD	TO-247AC	CoPack	Ultrafast*	600	2.7	28	1.0 to 2.5		•	
IRG4BC30F	TO-220AB	Discrete	Fast	600	1.8	31	1.0 to 2.5			•
IRG4BC30FD	TO-220AB	CoPack	Fast	600	1.8	31	1.0 to 2.5			•
IRG4PC30F	TO-247AC	Discrete	Fast	600	1.8	31	1.0 to 2.5			•
IRG4PC30FD	TO-247AC	CoPack	Fast	600	1.8	31	1.0 to 2.5			•
IRG4BC30S-S	D²Pak	Discrete	Standard	600	1.6	34	1.0 to 2.5	•		
IRG4BC30S	TO-220AB	Discrete	Standard	600	1.6	34	1.0 to 2.5		•	
IRG4PC30S	TO-247AC	Discrete	Standard	600	1.6	34	1.0 to 2.5		•	•
IRG4BC40U	TO-220AB	Discrete	Ultrafast	600	2.1	40	1.5 to 4.5			•
IRG4PC40U	TO-247AC	Discrete	Ultrafast	600	2.1	40	1.5 to 4.5			•
IRG4PC40UD	TO-247AC	CoPack	Ultrafast	600	2.1	40	1.5 to 4.5			•
IRG4BC40K	TO-220AB	Discrete	Ultrafast*	600	2.6	42	1.5 to 4.5		•	
IRG4PC40K	TO-247AC	Discrete	Ultrafast*	600	2.6	42	1.5 to 4.5		•	
IRG4PC40KD	TO-247AC	CoPack	Ultrafast*	600	2.6	42	1.5 to 4.5		•	
IRG4BC40F	TO-220AB	Discrete	Fast	600	1.7	49	1.5 to 4.5			•
IRG4PC40F	TO-247AC	Discrete	Fast	600	1.7	49	1.5 to 4.5			•
IRG4PC40FD	TO-247AC	CoPack	Fast	600	1.7	49	1.5 to 4.5			•
IRG4PC50K	TO-247AC	Discrete	Ultrafast*	600	2.2	52	3.0 to 6.0		•	
IRG4PC50KD	TO-247AC	CoPack	Ultrafast*	600	2.2	52	3.0 to 6.0		•	
IRG4PC50U	TO-247AC	Discrete	Ultrafast	600	2	55	3.0 to 6.0			•
IRG4PC50UD	TO-247AC	CoPack	Ultrafast	600	2	55	3.0 to 6.0			•
IRG4BC40S	TO-220AB	Discrete	Standard	600	1.5	60	1.5 to 4.5		•	
IRG4PC40S	TO-247AC	Discrete	Standard	600	1.5	60	1.5 to 4.5		•	
IRG4BH20K-S	D²Pak	Discrete	Ultrafast*	1200	3.17	11	1.5 to 2.5		•	
IRG4PH20K	TO-247AC	Discrete	Ultrafast*	1200	4.3	11	1.5 to 2.5		•	
IRG4PH20KD	TO-247AC	CoPack	Ultrafast*	1200	4.3	11	1.5 to 2.5		•	
IRG4BH20K-L	TO-262	Discrete	Ultrafast*	1200	3.17	11	1.5 to 2.5		•	
IRG4PH30K	TO-247AC	Discrete	Ultrafast*	1200	4.2	20	2.5 to 4.5		•	

** 10µs short circuit capable*

Standard: DC – 1kHz; Fast: 2 -10 kHz; Ultrafast: 8 - 20 kHz

Discrete and Co-Pack IGBTs 1kW – 6.5kW, continued

Part #	Package	Circuit Type	Speed	BV_{CES} (V)	$V_{CE(ON)}$ (V)	I_C @ 25°C (A)	Power Level (max) (kW)	APPLICATION: APPLIANCE	INDUSTRIAL	UPS
IRG4PH30KD	TO-247AC	CoPack	Ultrafast*	1200	4.2	20	2.5 to 4.5		•	
IRG4PH40K	TO-247AC	Discrete	Ultrafast*	1200	3.4	30	3.5 to 6.5		•	
IRG4PH40KD	TO-247AC	CoPack	Ultrafast*	1200	3.4	30	3.5 to 6.5		•	
IRG4PH40U	TO-247AC	Discrete	Ultrafast	1200	3.5	30	3.5 to 6.5			•
IRG4PH40UD	TO-247AC	CoPack	Ultrafast	1200	3.5	30	3.5 to 6.5			•

** 10µs short circuit capable*

Standard: DC – 1kHz; Fast: 2 -10 kHz; Ultrafast: 8 - 20 kHz

Discrete and Co-Pack IGBTs for Motor Drives and UPS < 2kW

Part #	Package	Circuit Type	Speed	BV_{CES} (V)	$V_{CE(ON)}$ (V)	I_C @ 25°C (A)	Power Level (max) (kW)	APPLICATION: APPLIANCE	INDUSTRIAL	UPS
IRG4IBC10UD	TO-220 FullPak	CoPack	Ultrafast	600	2.15	6.8	up to 1.0	•		•
IRG4RC10U	D-Pak	Discrete	Ultrafast	600	2.6	8.5	up to 1.0	•		•
IRG4BC10UD	TO-220AB	CoPack	Ultrafast	600	2.6	8.5	up to 1.0	•		•
IRG4RC10K	D-Pak	Discrete	Ultrafast*	600	2.62	9	up to 1.0	•		
IRG4BC10K	TO-220AB	Discrete	Ultrafast*	600	2.62	9	up to 1.0	•		
IRG4BC10KD	TO-220AB	CoPack	Ultrafast*	600	2.62	9	up to 1.0	•		
IRG4BC15UD-S	D^2Pak	CoPack	Ultrafast	600	1.95	11	0.5 to 1.5	•		•
IRG4BC15UD	TO-220AB	CoPack	Ultrafast	600	1.95	11	0.5 to 1.5	•		•
IRG4IBC20UD	TO-220 FullPak	CoPack	Ultrafast	600	2.1	11.4	0.75 to 2.0	•	•	•
IRG4IBC20KD	TO-220 FullPak	CoPack	Ultrafast*	600	2.8	11.5	0.75 to 2.0	•		
IRG4BC20UD-S	D^2Pak	CoPack	Ultrafast	600	2.1	13	0.75 to 2.0	•		•
IRG4BC20U	TO-220AB	Discrete	Ultrafast	600	2.1	13	0.75 to 2.0	•	•	•
IRG4BC20UD	TO-220AB	CoPack	Ultrafast	600	2.1	13	0.75 to 2.0	•	•	•
IRG4RC10S	D-Pak	Discrete	Standard	600	1.7	14	up to 1.0	•		
IRG4BC10S	TO-220AB	Discrete	Standard	600	1.7	14	up to 1.0	•		
IRG4BC10SD	TO-220AB	CoPack	Standard	600	1.7	14	up to 1.0	•		
IRG4IBC20FD	TO-220 FullPak	CoPack	Fast	600	2	14.3	0.75 to 1.8	•		•
IRG4BC20FD-S	D^2Pak	Discrete	Fast	600	1.66	16	0.75 to 1.8	•		•
IRG4BC20K-S	D^2Pak	Discrete	Ultrafast*	600	2.8	16	0.75 to 1.8	•	•	
IRG4BC20KD-S	D^2Pak	CoPack	Ultrafast*	600	2.8	16	0.75 to 1.8	•	•	
IRG4BC15MD	TO-220AB	CoPack	Fast*	600	1.85	16	0.5 to 1.5	•	•	
IRG4BC20FD	TO-220AB	CoPack	Fast	600	2	16	0.5 to 1.5			•
IRG4BC20F	TO-220AB	Discrete	Fast	600	2	16	0.5 to 1.5			•
IRG4BC20K	TO-220AB	Discrete	Ultrafast*	600	2.8	16	0.5 to 1.5	•	•	
IRG4BC20KD	TO-220AB	CoPack	Ultrafast*	600	2.8	16	0.5 to 1.5	•	•	
IRG4IBC30KD	TO-220 FullPak	CoPack	Ultrafast*	600	2.7	17	1.0 to 2.5	•		
IRG4IBC30UD	TO-220 FullPak	CoPack	Ultrafast	600	2.1	17	1.0 to 2.5	•		
IRG4BC20MD-S	D^2Pak	CoPack	Fast*	600	2.1	18	0.75 to 2.0	•	•	
IRG4BC20MD	TO-220AB	CoPack	Fast*	600	2.1	18	0.75 to 2.0	•	•	
IRG4BC20SD-S	D^2Pak	CoPack	Standard	600	1.4	19	0.75 to 2.0	•		
IRG4BC20S	TO-220AB	Discrete	Standard	600	1.6	19	0.75 to 2.0	•		
IRG4BC20SD	TO-220AB	CoPack	Standard	600	1.6	19	0.75 to 2.0	•		

** 10µs short circuit capable*

Standard: DC – 1kHz; Fast: 2 -10 kHz; Ultrafast: 8 - 20 kHz

Three-Phase Bridge Drivers

Output Source/ Sink Current	V_{CC} Range	V_{BS} Range	V_O Swing	Deadtime	Features	Part #	Package
UP TO 600V — IR2133 / 2135							
+200 / -420 mA	10 - 25V with UVLO	10 - 25V with UVLO	Output Swing = Supply Voltage	≥ 200 ns	All Inputs Inverting, Separate High and Low Inputs,Undervoltage Lockout on All Drivers, Overcurrent Comparator	IR2133 IR2133J IR2133S	28-Lead PDIP 44-Lead PLCC 28-Lead SOIC
	12 - 25V with UVLO	12 - 25V with UVLO			Built In, Latching Fault Logic Fault Clear Input, Synchronized Shutdown Input, Uncommited Op-Amp	IR2135 IR2135J IR2135S	28-Lead PDIP 44-Lead PLCC 28-Lead SOIC
UP TO 600V — IR2136							
+120 / -250 mA	10 - 25V with UVLO	10 - 25V with UVLO	Output Swing = Supply Voltage	≥ 200 ns	Lower Output Current Version of 2133 5V Inverting Input Logic, Programmable Fault Clear Delay, Soft Turn-On Driver	IR2136 IR2136J IR2136S	28-Lead PDIP 44-Lead PLCC 28-Lead SOIC
	12 - 25V with UVLO	12 - 25V with UVLO			Same as 2136, Except High Side Noninverting Higher UV Lockout Threshold	IR21362 IR21362J IR21362S	28-Lead PDIP 44-Lead PLCC 28-Lead SOIC
UP TO 600V — IR2137							
+200 / -460 mA	12.5 - 25V with Under-Voltage Lockout	12.5 - 25V with Under-Voltage Lockout	Output Swing = Supply Voltage	≥ 200 ns	Separate Output Source / Sink Pins High-Side Desaturation Detection Shutdown and ITRIP Logic Inputs Synchronized Soft Fault Shutdown All Drivers Soft Turn-On Built-In Brake Driver	IR2137Q IR2137J	64-Lead MQFP 68-Lead PLCC
UP TO 1200V — IR2233 / 2235							
+200 / -420 mA	10 - 25V with UVLO	10 - 25V with UVLO	Output Swing = Supply Voltage	≥ 200 ns	All Inputs Inverting, Separate High and Low Inputs, Undervoltage Lockout on All Drivers, Overcurrent Comparator	IR2233 IR2233J IR2233S	28-Lead PDIP 44-Lead PLCC 28-Lead SOIC
	12 - 25V with UVLO	12 - 25V with UVLO			Built In, Latching Fault Logic Fault Clear Input, Synchronized Shutdown Input, Uncommited Op-Amp	IR2235 IR2235J IR2235S	28-Lead PDIP 44-Lead PLCC 28-Lead SOIC

Single High-side Drivers

Output Source/ Sink Current	V_{CC} Range	V_{BS} Range	V_O Swing	Typ. Prop Delay	Features	Part #	Package
UP TO 600V — IR2117 / 2118							
+200 / -420 mA	10 - 25V with Under-Voltage Lockout	10 - 25V with Under-Voltage Lockout	Output Swing = VBS Supply Voltage	125/105 ns On/Off	Single High Side Driver Non-inverting input Internal Pullup/down, 15V Logic	IR2117 IR2117S	8-Lead PDIP 8-Lead SOIC
					Same As 2117, Except Inverting Input	IR2118 IR2118S	8-Lead PDIP 8-Lead SOIC
UP TO 600V — IR2127 / 2128 *WITH OVERCURRENT DETECTION & SHUTDOWN*							
+200 / -420 mA	10 - 25V	12 - 25V	Output Swing = VBS Supply Voltage	200/150 ns On/Off	Single High Side Driver Non-inverting input, Inverting Fault Output Same As 2127, Except Inverting Input	IR2127 IR2127S IR2128 IR2128S	8-Lead PDIP 8-Lead SOIC 8-Lead PDIP 8-Lead SOIC
		9 - 25V			Same As 2127, Except Lower Undervoltage Threshold	IR21271 IR21271S	8-Lead PDIP 8-Lead SOIC

WARPSpeed™ IGBTs for PFC in Motor Drive and UPS

Part #	Package	Circuit Type	Speed	BV_{CES} (V)	$V_{CE(ON)}$ (V)	I_C @25°C (A)	Power Level HP	Power Level kW
IRG4IBC20W	TO-220 FullPak	Discrete	WarpSpeed *(50kHz)*	600	2.6	11.8	1.2	0.9
IRG4BC20W	TO-220AB	Discrete	WarpSpeed *(50kHz)*	600	2.6	13	1.3	1.0
IRG4IBC30W	TO-220 FullPak	Discrete	WarpSpeed *(50kHz)*	600	2.7	17	1.7	1.25
IRG4BC30W	TO-220AB	Discrete	WarpSpeed *(50kHz)*	600	2.7	23	2.3	1.75
IRG4BC30W-S	D²PAK	Discrete	WarpSpeed *(50kHz)*	600	2.1	23	2.3	1.75
IRG4PC30W	TO-247AC	Discrete	WarpSpeed *(50kHz)*	600	2.7	23	2.3	1.75
IRG4BC40W	TO-220AB	Discrete	WarpSpeed *(50kHz)*	600	2.5	40	4.0	3.0
IRG4PC40W	TO-247AC	Discrete	WarpSpeed *(50kHz)*	600	2.5	40	4.0	3.0
IRG4PC50W	TO-247AC	Discrete	WarpSpeed *(50kHz)*	600	2.3	55	5.5	4.0
IRG4PF50W	TO-247AC	Discrete	WarpSpeed *(50kHz)*	900	2.7	51	5.2	3.75

MOSFETs for Motor Drives in Industrial Electric Vehicles

Part #	Package	BV_{DSS} (V)	$R_{DS(on)}$ @ 10V (mΩ)	I_D* @ 25°C
IRFBA1404P	Super-220™	40	3.7	212
IRF1404S	D²Pak	40	4	162
IRF1404	TO-220	40	4	162
IRF1404L	TO-262	40	4	162
IRF1405S	D2Pak	55	5.3	133
IRF1405	TO-220	55	5.3	133
IRF1405L	TO-262	55	5.3	133
IRFP2907	TO-247	75	3.3	174
IRFPS3810	Super-247™	100	9	141
IRF3710S	D²Pak	100	25	58
IRF3710	TO-220	100	25	58
IRF3710L	TO-262	100	25	58
IRFPS3815	Super-247™	150	14	105
IRF3415S	D²Pak	150	42	43
IRF3415	TO-220	150	42	43
IRFP3415	TO-247	150	42	43

* Represents die capability

IGBT Modules for Motor Drives in Industrial Electric Vehicles

Part #	Package	Circuit Type	Speed	BV_{CES} (V)
GA400GD25S	Dual INT-A-PAK	Single	Standard	250
GA600GD25S	Dual INT-A-PAK	Single	Standard	250

Bulletin I0129J rev. C 02/00

International
IOR Rectifier

IR060LM06CS02CB

FAST RECOVERY DIODE

- **Junction Size:** **Square 60 x 60 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **600 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	1.3V	T_J=25°C, I_F=2A
V_{RRM} Reverse Breakdown Voltage	600V	T_J=25°C, I_{RRM}=10µA **(1)**
t_{rr} Typical Reverse Recovery Time	55ns	T_J=25°C, I_F=1A, -di/dt=100A/µs

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr-Ni-Ag (1 KA-4 KA-6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (5µm)
Chip Dimensions	60 x 60 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	260µm, ± 10µm
Maximum Width of Sawing Line	45µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in essicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	060	L	M	06	C	S02	CB
1	2	3	4	5	6	7	8

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: L = Wire Bondable Fast Recovery Diode

4 - Passivation Process: M = Glassivated MOAT

5 - Voltage code: Code x 100 = V_{RRM}

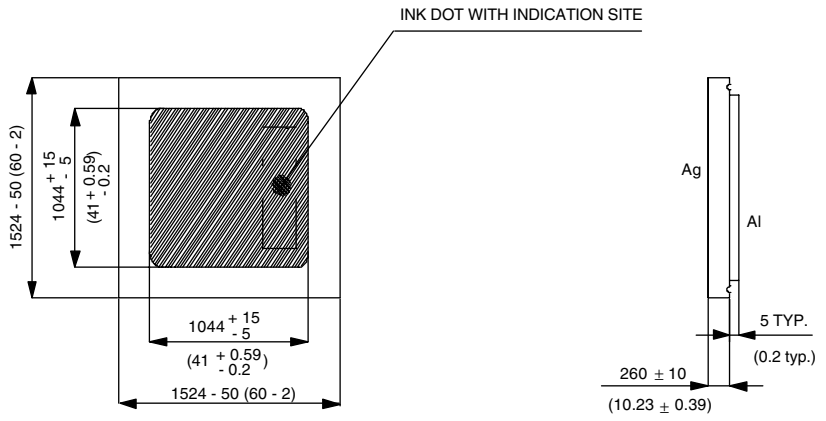
6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - t_{rr} code

8 - CB = Probed Uncut Die (wafer in box)

CF = Inked Probed Sawn wafer on film (blue tape)

Outline Table

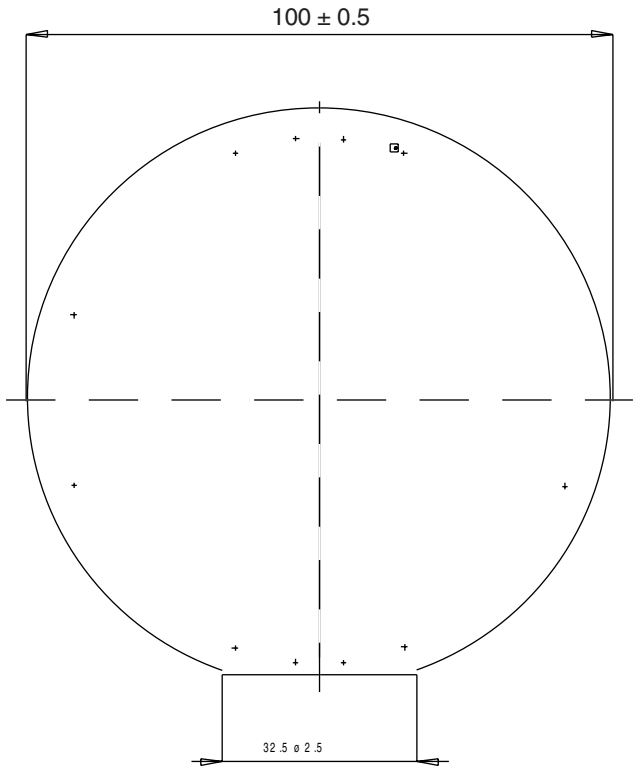


All dimensions are in microns (mils)

Wafer Layout

TOP VIEW

N° 3000 Basic Cells



All dimensions are in millimeters

Bulletin I0129J rev. C 02/00

International
IOR Rectifier

IR060LM06CS02CB

FAST RECOVERY DIODE

- **Junction Size:** **Square 60 x 60 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **600 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	1.3V	T_J=25°C, I_F=2A
V_{RRM} Reverse Breakdown Voltage	600V	T_J=25°C, I_{RRM}=10µA **(1)**
t_{rr} Typical Reverse Recovery Time	55ns	T_J=25°C, I_F=1A, -di/dt=100A/µs

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr-Ni-Ag (1 KA-4 KA-6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (5µm)
Chip Dimensions	60 x 60 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	260µm, ± 10µm
Maximum Width of Sawing Line	45µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in essicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	060	L	M	06	C	S02	CB
1	2	3	4	5	6	7	8

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: L = Wire Bondable Fast Recovery Diode

4 - Passivation Process: M = Glassivated MOAT

5 - Voltage code: Code x 100 = V_{RRM}

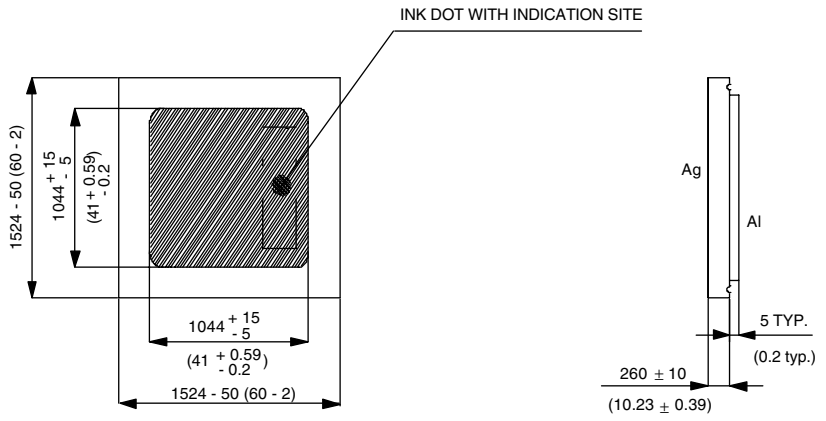
6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - t_{rr} code

8 - CB = Probed Uncut Die (wafer in box)

CF = Inked Probed Sawn wafer on film (blue tape)

Outline Table

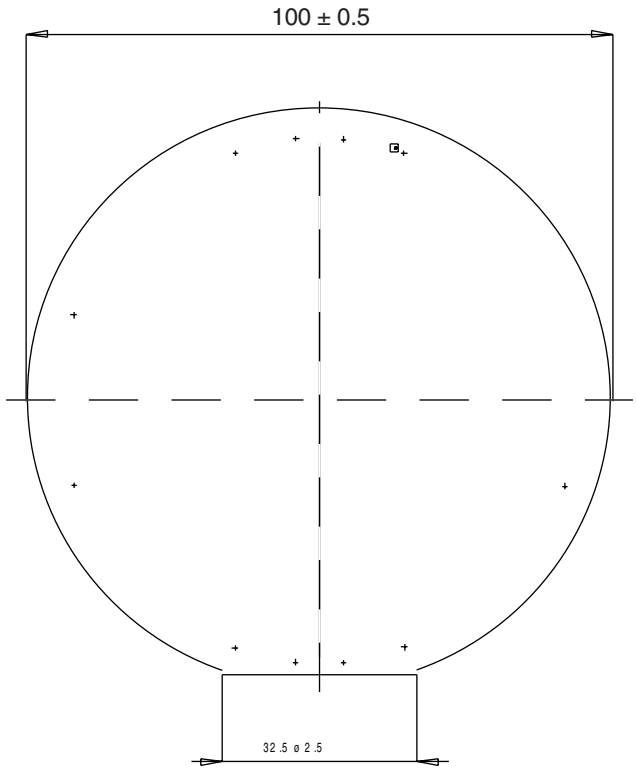


All dimensions are in microns (mils)

Wafer Layout

TOP VIEW

N° 3000 Basic Cells



All dimensions are in millimeters

International
IOR Rectifier

IR060PM12CS02CB

FAST RECOVERY DIODE

- **Junction Size:** **Square 60 x 60 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **1200 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:**

Major Ratings and Characteristics

Parameters		Units	Test Conditions	
V_{FM}	Maximum Forward Voltage	1.3 V	T_J = 25°C, I_F = 2 A	
V_{RRM}	Reverse Breakdown Voltage	1200 V	T_J = 25°C, I_{RRM} = 10 µA	**(1)**
t_{rr}	Typical Reverse Recovery Time	55 ns	T_J = 25°C, I_F = 1A, -di/dt = 100A/µs	

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al (5 µm)
Chip Dimensions	60 x 60 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	260 µm, ± 10 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in essicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	060	P	M	12	C	S02	CB
1	2	3	4	5	6	7	8

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device : P = Wire Bondable Fast Recovery Diode (Platinum)

4 - Passivation Process : M = Glassivated MOAT

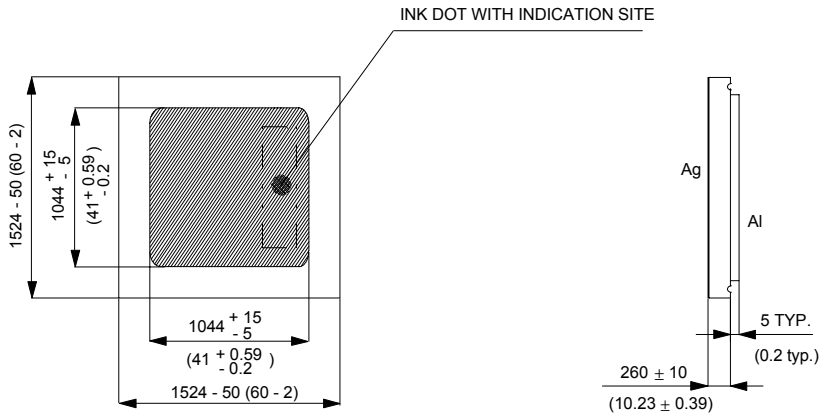
5 - Voltage code : Code x 100 = V_{RRM}

6 - Metallization : C = Aluminium (Anode) - Silver (Cathode)

7 - t_{rr} code

8 - CB : Probed Uncut Die (wafer in box)
CF : Inked Probed Sawn wafer on film (blue tape)

Outline Table

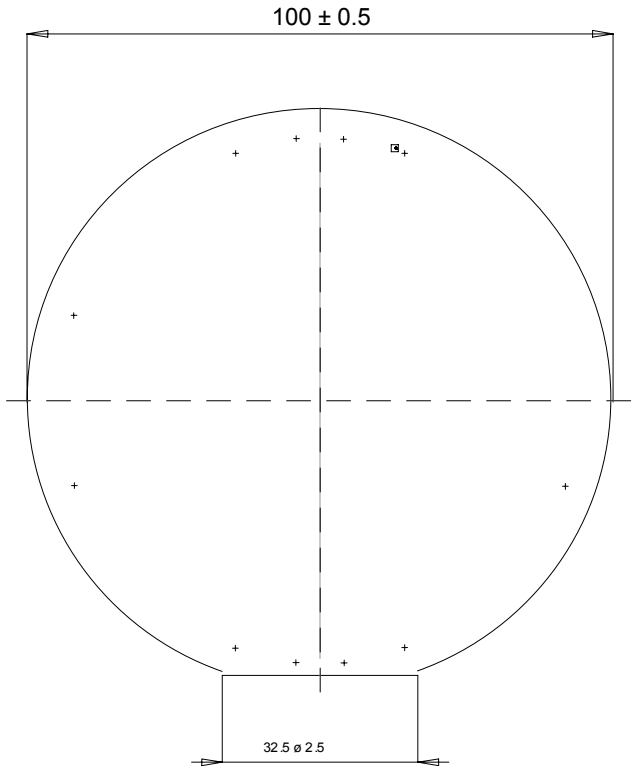


All dimensions are in microns (mils)

Wafer Layout

TOP VIEW

N° 3000 Basic Cells



All dimensions are in millimeters

International
IOR Rectifier

IR135LM06CS02CB

FAST RECOVERY DIODE

- **Junction Size:** **Rectangular 135 x 100 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **600 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:** **8EWF..S Series**

Major Ratings and Characteristics

Parameters		Units	Test Conditions
V_{FM}	Maximum Forward Voltage	1.2 V	T_J = 25°C, I_F = 8 A
V_{RRM}	Reverse Breakdown Voltage	600 V	T_J = 25°C, I_{RRM} = 100 µA **(1)**
t_{rr}	Reverse Recovery Time	55ns	T_J = 25°C, I_F = 1A, -di/dt = 100A/µs

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20 µm)
Chip Dimensions	135 x 100 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	300 µm, ± 10 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	135	L	M	06	C	S02	CB
1	2	3	4	5	6	7	8

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: L = Wire Bondable Fast Recovery Diode

4 - Passivation Process: M = Glassivated MOAT

5 - Voltage code: Code x 100 = V_{RRM}

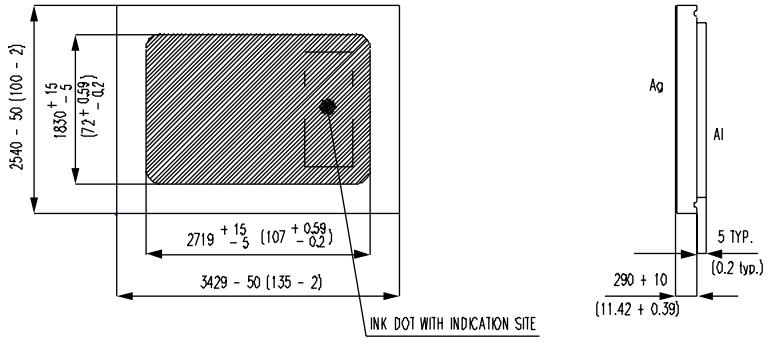
6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - t_{rr} code: S02 = 55 nsec

8 - CB = Probed Uncut Die (wafer in box)

None = Probed Die in chip carrier

Outline Table

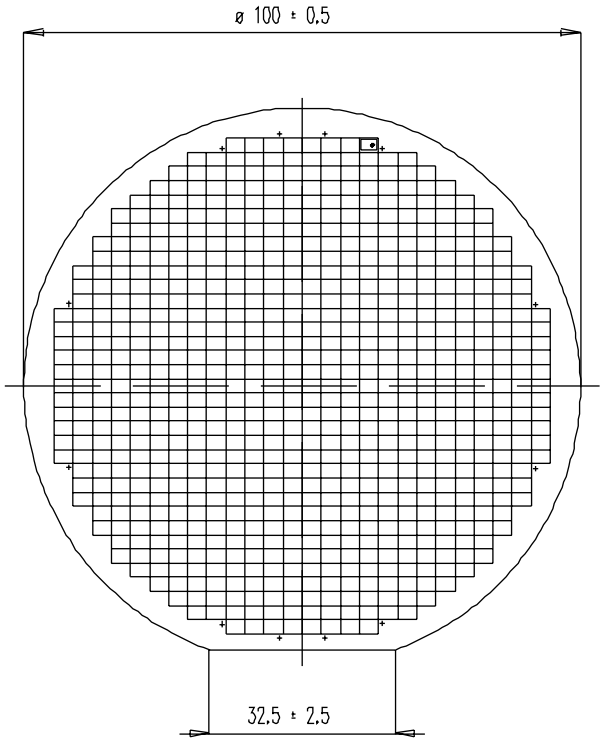


All dimensions are in microns (mils)

Wafer Layout

TOP VIEW

N° 735 Basic Cells



All dimensions are in millimeters

International
IOR Rectifier

IR180LM..CS02CB SERIES

FAST RECOVERY DIODES

- **Junction Size:** **Square 180 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **200 to 600 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:** **20ETF Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	1300 mV	T_J = 25°C, I_F = 20 A
V_{RRM} Reverse Breakdown Voltage Range	200 to 600 V	T_J = 25°C, I_{RRM} = 100 µA **(1)**

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20 µm)
Chip Dimensions	180 x 180 mils (4.57x4.57 mm) - see drawing
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	260 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	180	L	M	06	C	S02	CB
1	2	3	4	5	6	7	8

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: L = Wire Bondable Fast Recovery Diode

4 - Passivation Process: M = Glassivated MOAT

5 - Voltage code: Code x 100 = V_{RRM}

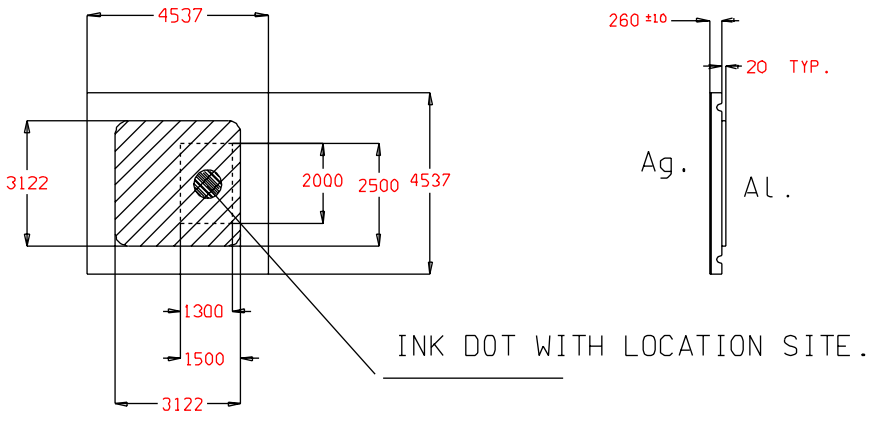
Available Class
02 = 200 V
04 = 400 V
06 = 600 V

6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - T_{rr} code: S02 = 200 nsec

8 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

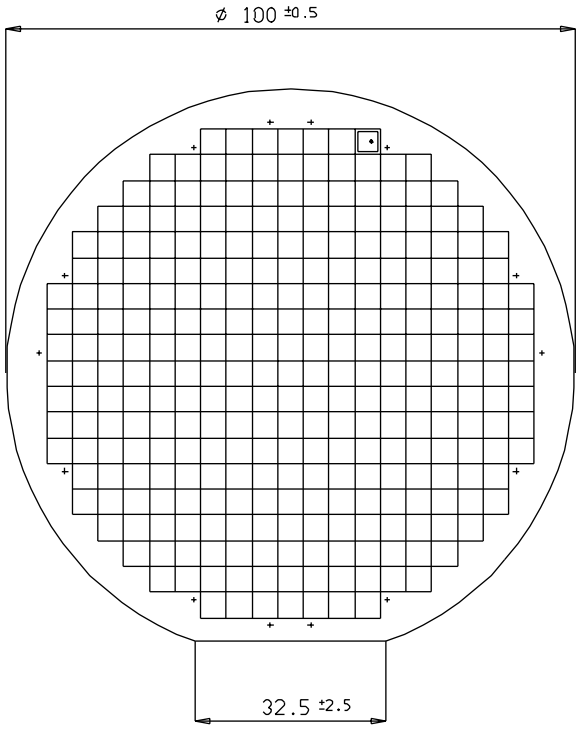


All dimensions are in microns

Wafer Layout

TOP VIEW

N° 293 Basic Cells



All dimensions are in millimeters

Bulletin I0125J 07/97

International
IOR Rectifier

IR180LM..CS05CB SERIES

FAST RECOVERY DIODES

- **Junction Size:** **Square 180 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **1000 and 1200 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:** **20ETF Series**

Major Ratings and Characteristics

Parameters		Units	Test Conditions	
V_{FM}	Maximum Forward Voltage	1350 mV	T_J = 25°C, I_F = 20 A	
V_{RRM}	Reverse Breakdown Voltage Range	1000 and 1200 V	T_J = 25°C, I_{RRM} = 100 µA	**(1)**

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20 µm)
Chip Dimensions	180 x 180 mils (4.57x4.57 mm) - see drawing
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	260 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	180	L	M	12	C	S05	CB
1	2	3	4	5	6	7	8

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: L = Wire Bondable Fast Recovery Diode

4 - Passivation Process: M = Glassivated MOAT

5 - Voltage code: Code x 100 = V_{RRM}

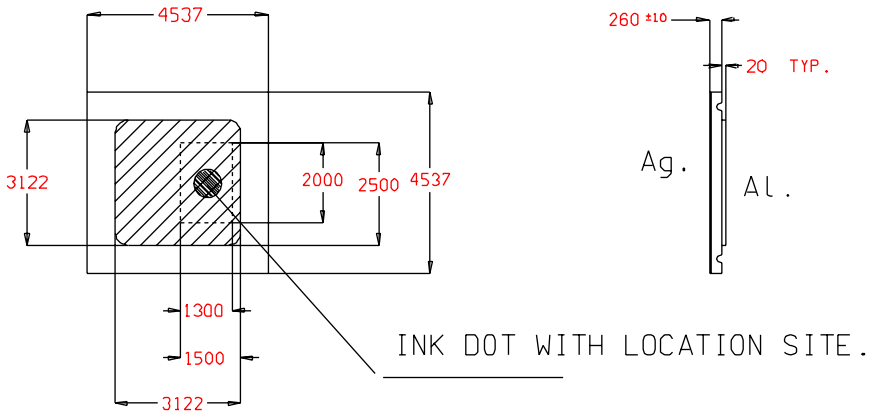
Available Class
10 = 1000 V
12 = 1200 V

6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - Fast Recovery Type: S05 = 500 nsec

8 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

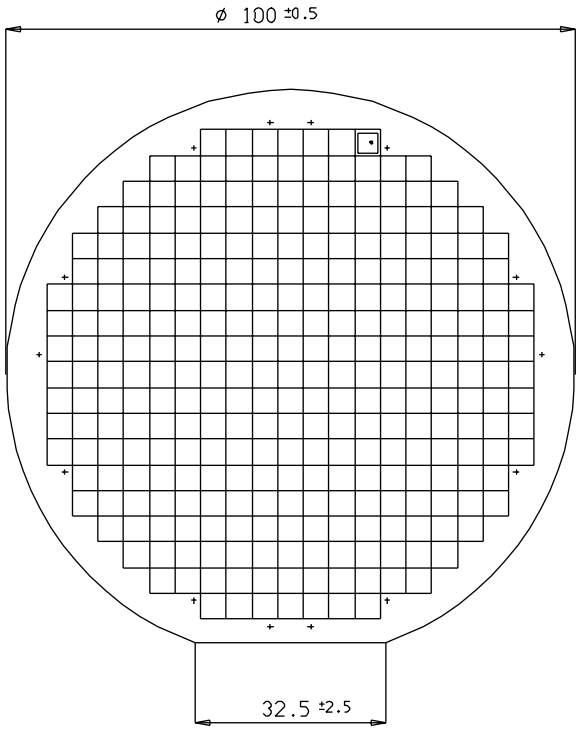


All dimensions are in microns

Wafer Layout

TOP VIEW

N° 293 Basic Cells



All dimensions are in millimeters

Bulletin I0138J rev. A 05/00

International
IOR Rectifier

IR207LM..CS02CB SERIES

FAST RECOVERY DIODES

- **Junction Size:** **Rectangular 207 x 157 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **200 to 600 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:** **20ETF Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	1300 mV	$T_J = 25°C$, $I_F = 20$ A
V_{RRM} Reverse Breakdown Voltage Range	200 to 600 V	$T_J = 25°C$, $I_{RRM} = 100$ µA **(1)**

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20 µm)
Chip Dimensions	207 x 157 mils (5.26x3.99 mm) - see drawing
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	260 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	207	L	M	06	C	S02	CB
1	2	3	4	5	6	7	8

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: L = Wire Bondable Fast Recovery Diode

4 - Passivation Process: M = Glassivated MOAT

5 - Voltage code: Code x 100 = V_{RRM}

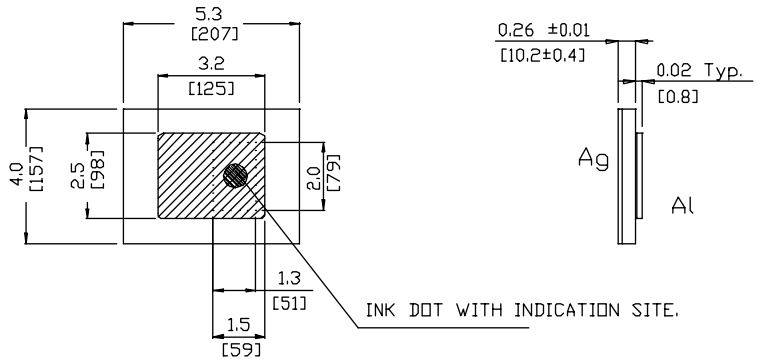
Available Class
02 = 200 V
04 = 400 V
06 = 600 V

6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - T_{rr} code: S02 = 200 nsec

8 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

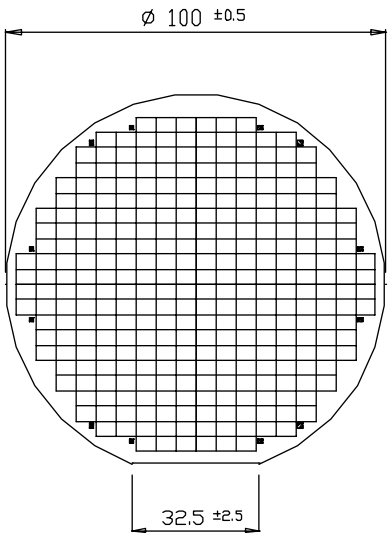


All dimensions are in millimeters (mils)

Wafer Layout

TOP VIEW

N° 304 Basic Cells



All dimensions are in millimeters

International
IOR Rectifier

IR230LM06CS02CB

FAST RECOVERY DIODE

- **Junction Size:** **Square 230 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **600 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:** **40EPF Series**

Major Ratings and Characteristics

Parameters		Units	Test Conditions
V_{FM}	Maximum Forward Voltage	1080 mV	T_J = 25°C, I_F = 20 A
V_{RRM}	Reverse Breakdown Voltage	600 V	T_J = 25°C, I_{RRM} = 100 µA **(1)**
t_{rr}	Reverse Recovery Time	60ns	T_J = 25°C, I_F = 1A, -di/dt = 100A/µs

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20 µm)
Chip Dimensions	230 x 230 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	300 µm, ± 10 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	230	L	M	06	C	S02	CB
1	2	3	4	5	6	7	8

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: L = Wire Bondable Fast Recovery Diode

4 - Passivation Process: M = Glassivated MOAT

5 - Voltage code: Code x 100 = V_{RRM}

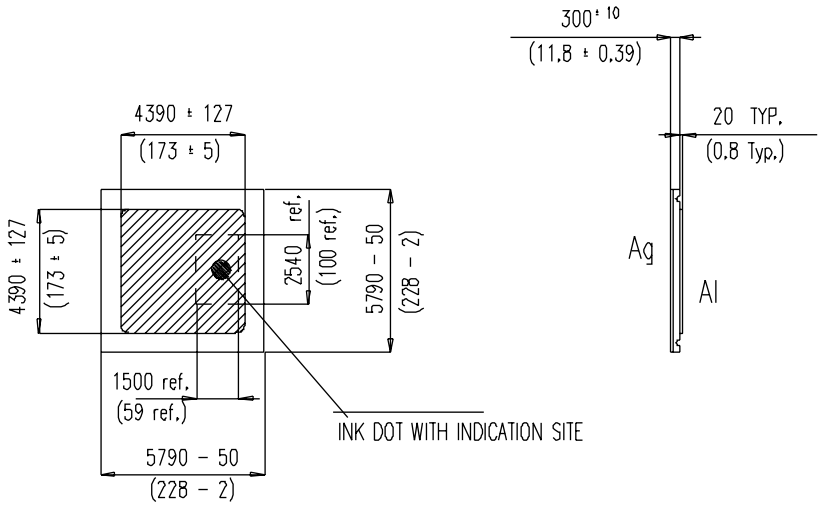
6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - t_{rr} code: S02 = 60 nsec

8 - CB = Probed Uncut Die (wafer in box)

None = Probed Die in chip carrier

Outline Table

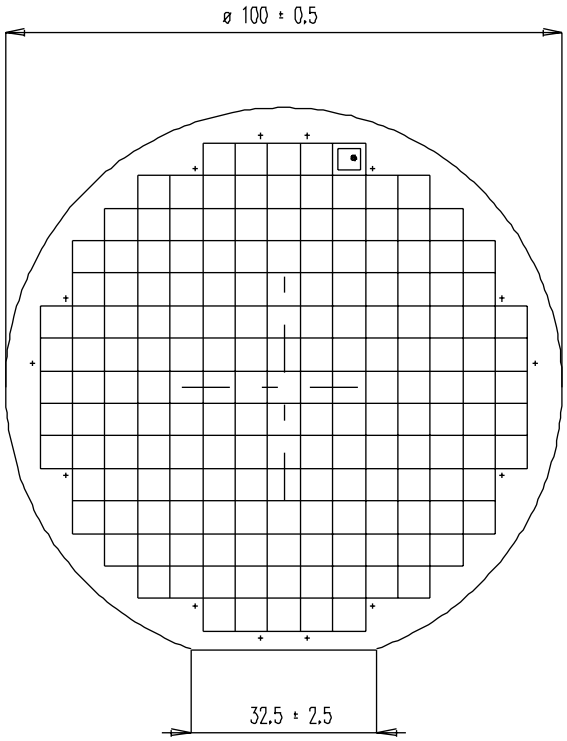


All dimensions are in microns (mils)

Wafer Layout

TOP VIEW

N° 177 Basic Cells



All dimensions are in millimeters

Bulletin I0114J 05/00

International
IOR Rectifier

IR340LM..CS05CB SERIES

FAST RECOVERY DIODES

- **Junction Size:** **Rectangular 350 x 230 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **1000 to 1200 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:** **60EPF Series**

Major Ratings and Characteristics

Parameters		Units	Test Conditions	
V_{FM}	Maximum Forward Voltage	1300 mV	$T_J = 25°C$, $I_F = 60$ A	
V_{RRM}	Reverse Breakdown Voltage Range	1000 to 1200 V	$T_J = 25°C$, $I_{RRM} = 100$ µA	**(1)**

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20 µm)
Chip Dimensions	350 x 230 mils (8.89x5.84 mm) - see drawing
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	260 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	340	L	M	12	C	S05	CB
1	2	3	4	5	6	7	8

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: L = Wire Bondable Fast Recovery Diode

4 - Passivation Process: M = Glassivated MOAT

5 - Voltage code: Code x 100 = V_{RRM}

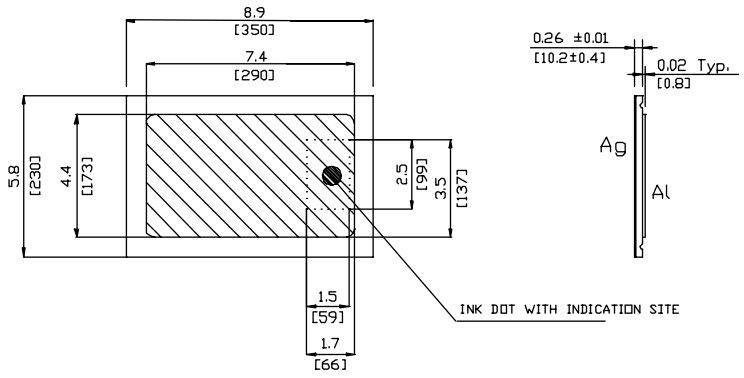
Available Class
10 = 1000 V
12 = 1200 V

6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - T_{rr} code: S05 = 500 nsec

8 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

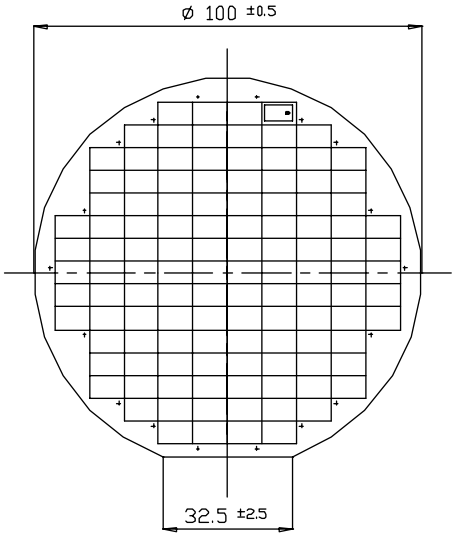


All dimensions are in millimeters (mils)

Wafer Layout

TOP VIEW

N° 118 Basic Cells



All dimensions are in millimeters

Bulletin I0113J 05/00

International
IOR Rectifier

IR390LM..CS05CB SERIES

FAST RECOVERY DIODES

- **Junction Size:** **Rectangular 390 x 270 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **1000 to 1200 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:** **80EPF Series**

Major Ratings and Characteristics

Parameters		Units	Test Conditions	
V_{FM}	Maximum Forward Voltage	1300 mV	$T_J = 25°C$, $I_F = 80$ A	
V_{RRM}	Reverse Breakdown Voltage Range	1000 to 1200 V	$T_J = 25°C$, $I_{RRM} = 100$ µA	**(1)**

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20 µm)
Chip Dimensions	390 x 270 mils (9.91x6.86 mm) - see drawing
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	260 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	390	L	M	12	C	S05	CB
1	2	3	4	5	6	7	8

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: L = Wire Bondable Fast Recovery Diode

4 - Passivation Process: M = Glassivated MOAT

5 - Voltage code: Code x 100 = V_{RRM}

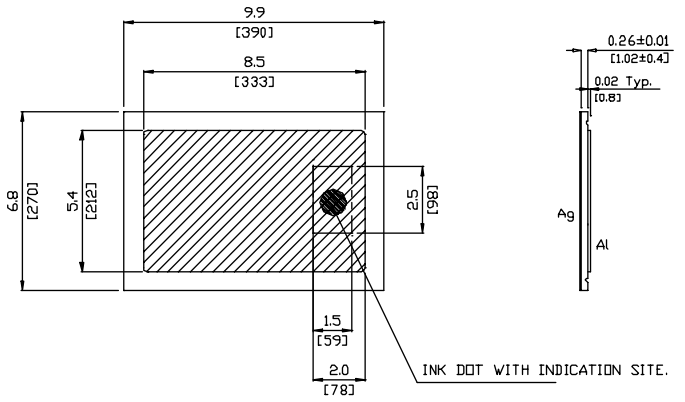
Available Class
10 = 1000 V
12 = 1200 V

6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - T_{rr} code: S05 = 500 nsec

8 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

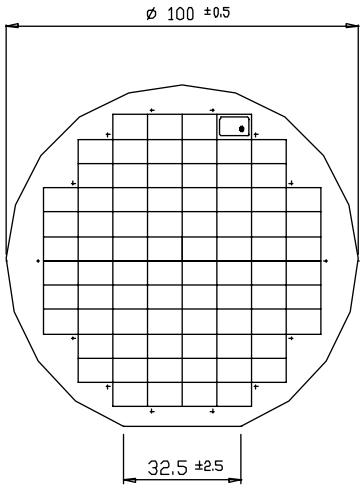


All dimensions are in millimeters (mils)

Wafer Layout

TOP VIEW

N° 80 Basic Cells

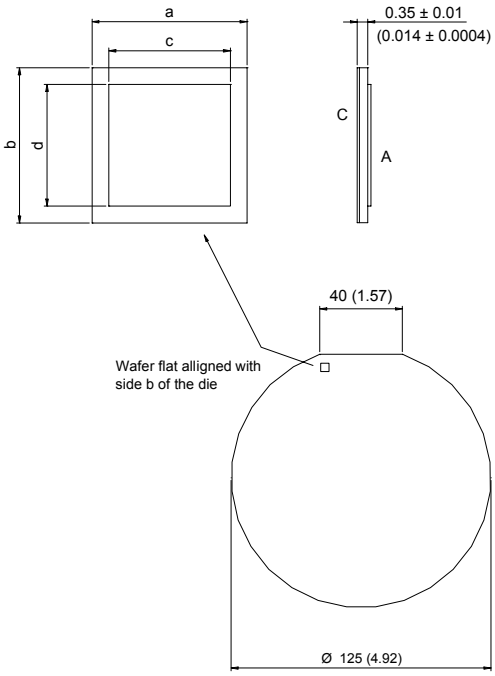


All dimensions are in millimeters

International
IOR Rectifier

FD087U02A5B

Fred Die in Wafer Form



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

2. CONTROLLING DIMENSION (INCH):

3. DIMENSIONS AND TOLERANCES:
   a = 2.210 ± 0.05
   (0.087 ± 0.002)
   b = 2.210 ± 0.05
   (0.087 ± 0.002)
   c = 1.996 ± 0.003
   (0.078 ± 0.0001)
   d = 1.996 ± 0.003
   (0.078 ± 0.0001)

4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)

5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade

6. MINIMUM ORDER QUANTITY:
   1300 die

NOT TO SCALE

Reference IR Packaged Part: MUR820 Series

Electrical Characteristics (Wafer Form)

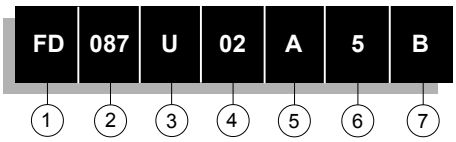
	Parameters	Units	Test Conditions
V_{FM}	Maximum Forward Voltage	0.975 V	$T_J = 25°C$, $I_F = 8$ A
V_{RRM}	Mimunum Reverse Breakdown Voltage	200 V	$T_J = 25°C$, $I_{RRM} = 100$ µA
I_{RM}	Max. Reverse Leakage Current	5µA	$T_J = 25°C$, $V_{RRM} = 200$ V
t_{rr}	Typ. Reverse Recovery Time	35ns	$I_F = 1A$, $di_F/dt = 50A/µs$, $V_R = 30$ V

Mechanical Data

	Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 2 KA - 3 KA)
	Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
	Chip Dimensions	0.087" x 0.087" (see drawing)
	Reject Ink Dot Size	0.25 mm diameter minimum
	Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code



1 - Fred Die

2 - Chip Dimension in Mils: 087 = 087x087 square

3 - Process U = UltraFast

4 - Voltage code Vrrm (*100) eg: 02 = 200V

5 - Chip surface metallization: A = Aluminium (anode), Silver (cathode)

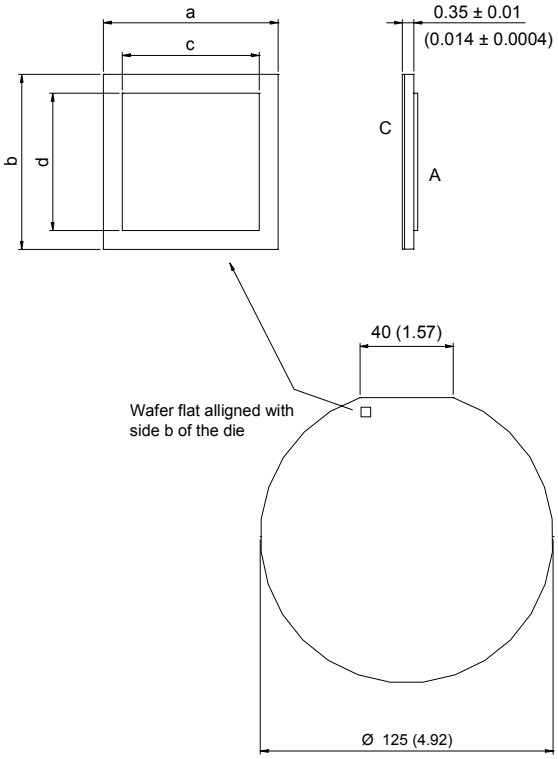
6 - Wafer diameter in inches

7 - Packaging: B = Inked Probed Unsawn Wafer (Wafer in box)

International
IOR Rectifier

FD100H06A5B

Fred Die in Wafer Form



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

2. CONTROLLING DIMENSION (INCH):

3. DIMENSIONS AND TOLERANCES:
   a = 2.540 ± 0.05
   (0.100 ± 0.002)
   b = 2.540 ± 0.05
   (0.100 ± 0.002)
   c = 1.880 ± 0.003
   (0.074 ± 0.0001)
   d = 1.880 ± 0.003
   (0.074 ± 0.0001)

4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)

5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade

6. MINIMUM ORDER QUANTITY:
   1300 die

NOT TO SCALE

Reference IR Packaged Part: 8ETH06 Series

Electrical Characteristics (Wafer Form)

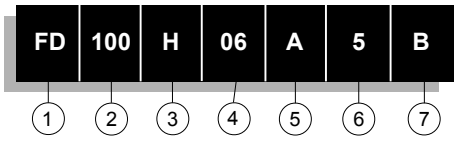
	Parameters	Units	Test Conditions
V_{FM}	Maximum Forward Voltage	2.3 V	T_J = 25°C, I_F = 8 A
V_{RRM}	Mimunum Reverse Breakdown Voltage	600 V	T_J = 25°C, I_{RRM} = 200 µA
I_{RM}	Max. Reverse Leakage Current	100µA	T_J = 25°C, V_{RRM} = 600 V
t_{rr}	Typ. Reverse Recovery Time	20ns	I_F = 1A, di/ dt = 100A/µs, V_R = 30 V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 2 KA - 3 KA)
Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
Chip Dimensions	0.100" x 0.100" (see drawing)
Reject Ink Dot Size	0.25 mm diameter minimum
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code



1 - Fred Die

2 - Chip Dimension in Mils: 100 = 100x100 square

3 - Process H = HyperFast

4 - Voltage code Vrrm (*100) eg: 06 = 600V

5 - Chip surface metallization: A = Aluminium (anode), Silver (cathode)

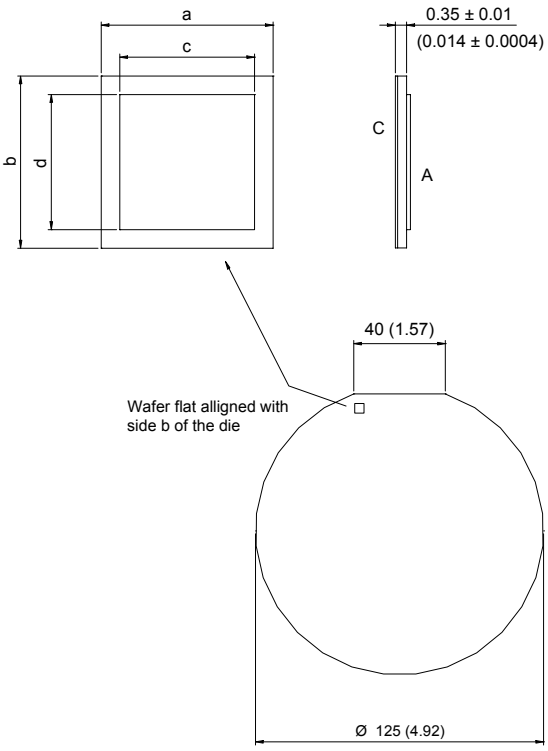
6 - Wafer diameter in inches

7 - Packaging: B = Inked Probed Unsawn Wafer (Wafer in box)

International
IOR Rectifier

FD120H06A5B

Fred Die in Wafer Form



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

2. CONTROLLING DIMENSION (INCH):

3. DIMENSIONS AND TOLERANCES:
   a = 3.048 ± 0.05
   (0.120 ± 0.002)
   b = 3.048 ± 0.05
   (0.120 ± 0.002)
   c = 2.388 ± 0.003
   (0.094 ± 0.0001)
   d = 2.388 ± 0.003
   (0.094 ± 0.0001)

4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)

5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade

6. MINIMUM ORDER QUANTITY:
   900 die

NOT TO SCALE

Reference IR Packaged Part: 15ETH06 Series

Electrical Characteristics (Wafer Form)

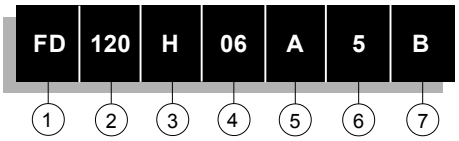
	Parameters	Units	Test Conditions
V_{FM}	Maximum Forward Voltage	2.3 V	T_J = 25°C, I_F = 15 A
V_{RRM}	Mimunum Reverse Breakdown Voltage	600 V	T_J = 25°C, I_{RRM} = 200 µA
I_{RM}	Max. Reverse Leakage Current	100µA	T_J = 25°C, V_{RRM} = 600 V
t_{rr}	Typ. Reverse Recovery Time	20 ns	I_F = 1A, di/ dt = 100A/µs, V_R = 30 V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 2 KA - 3 KA)
Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
Chip Dimensions	0.120" x 0.120" (see drawing)
Reject Ink Dot Size	0.25 mm diameter minimum
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code



1 - Fred Die

2 - Chip Dimension in Mils: 120 = 120x120 square

3 - Process H = HyperFast

4 - Voltage code Vrrm (*100) eg: 06 = 600V

5 - Chip surface metallization: A = Aluminium (anode), Silver (cathode)

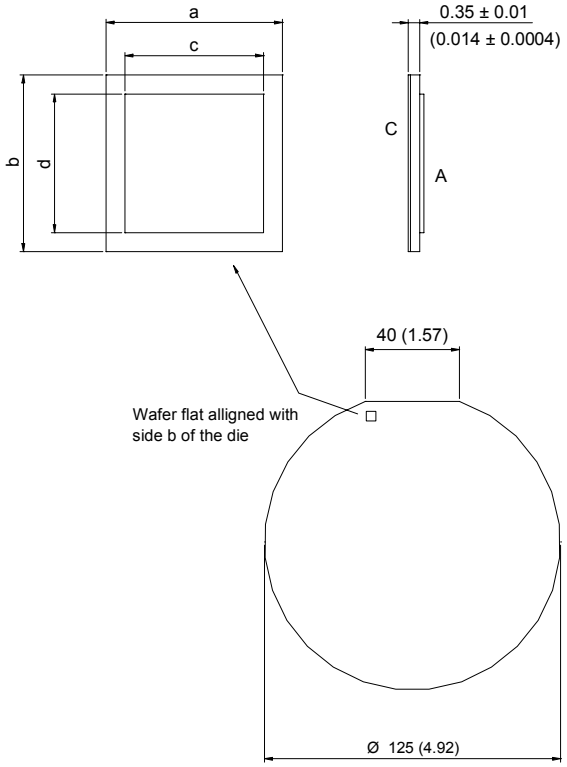
6 - Wafer diameter in inches

7 - Packaging: B = Inked Probed Unsawn Wafer (Wafer in box)

International
IOR Rectifier

FD160H06A5B

Fred Die in Wafer Form



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

2. CONTROLLING DIMENSION (INCH):

3. DIMENSIONS AND TOLERANCES:
   a = 4.064 ± 0.05
   (0.160 ± 0.002)
   b = 4.064 ± 0.05
   (0.160 ± 0.002)
   c = 3.404 ± 0.003
   (0.134 ± 0.0001)
   d = 3.404 ± 0.003
   (0.134 ± 0.0001)

4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)

5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade

6. MINIMUM ORDER QUANTITY:
   500 die

NOT TO SCALE

Reference IR Packaged Part: 30ETH06/ 30EPH06 Series

Electrical Characteristics (Wafer Form)

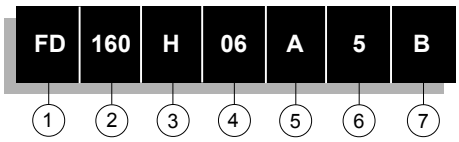
	Parameters	Units	Test Conditions
V_{FM}	Maximum Forward Voltage	2.3 V	T_J = 25°C, I_F = 30 A
V_{RRM}	Mimunum Reverse Breakdown Voltage	600 V	T_J = 25°C, I_{RRM} = 200 µA
I_{RM}	Max. Reverse Leakage Current	100µA	T_J = 25°C, V_{RRM} = 600 V
t_{rr}	Typ. Reverse Recovery Time	20 ns	I_F = 1A, di/ dt = 100A/µs, V_R = 30 V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 2 KA - 3 KA)
Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
Chip Dimensions	0.160" x 0.160" (see drawing)
Reject Ink Dot Size	0.25 mm diameter minimum
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code



1 - Fred Die

2 - Chip Dimension in Mils: 160 = 160x160 square

3 - Process: H = HyperFast

4 - Voltage code Vrrm (*100) eg: 06 = 600V

5 - Chip surface metallization: A = Aluminium (anode), Silver (cathode)

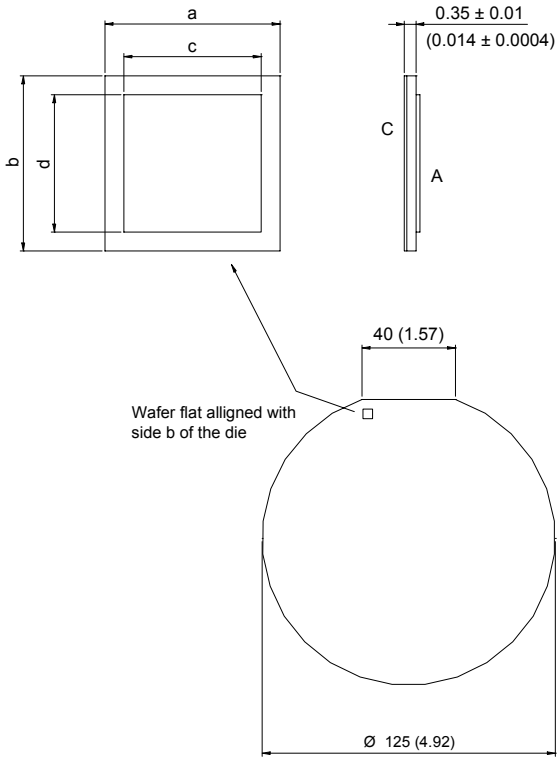
6 - Wafer diameter in inches

7 - Packaging: B = Inked Probed Unsawn Wafer (Wafer in box)

International
IOR Rectifier

FD200H02A5B

Fred Die in Wafer Form



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

2. CONTROLLING DIMENSION (INCH):

3. DIMENSIONS AND TOLERANCES:
   a = 5.080 ± 0.05
   (0.200 ± 0.002)
   b = 5.08 ± 0.05
   (0.200 ± 0.002)
   c = 4.420 ± 0.003
   (0.174 ± 0.0001)
   d = 4.420 ± 0.003
   (0.174 ± 0.0001)

4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)

5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade

6. MINIMUM ORDER QUANTITY:
   300 die

NOT TO SCALE

Electrical Characteristics (Wafer Form)

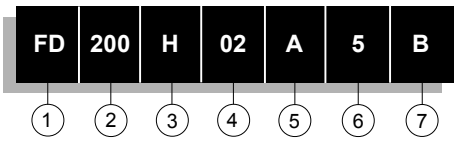
	Parameters	Units	Test Conditions
V_{FM}	Maximum Forward Voltage	1.13 V	T_J = 25°C, I_F = 150 A (Pow*IR*tab)
V_{FM}	Maximum Forward Voltage	1.08 V	T_J = 25°C, I_F = 60 A (TO-247)
V_{RRM}	Mimunum Reverse Breakdown Voltage	200 V	T_J = 25°C, I_{RRM} = 100 µA
I_{RM}	Max. Reverse Leakage Current	50 µA	T_J = 25°C, V_{RRM} = 200 V
t_{rr}	Typ. Reverse Recovery Time	35 ns	I_F = 1A, di/ dt = 100A/µs, V_R = 30 V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 2 KA - 3 KA)
Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
Chip Dimensions	0.200" x 0.200" (see drawing)
Reject Ink Dot Size	0.25 mm diameter minimum
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code



1 - Fred Die

2 - Chip Dimension in Mils: 200 = 200x200 square

3 - Process H = HyperFast

4 - Voltage code Vrrm (*100) eg: 02 = 200V

5 - Chip surface metallization: A = Aluminium (anode), Silver (cathode)

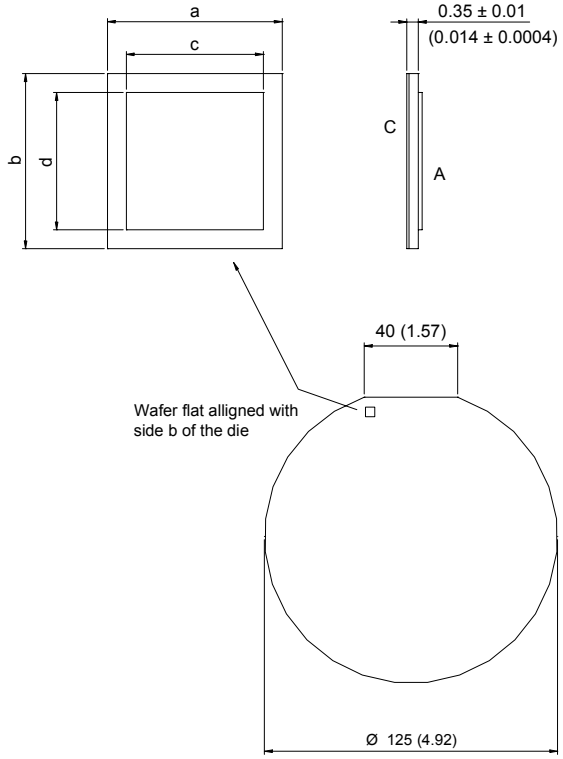
6 - Wafer diameter in inches

7 - Packaging: B = Inked Probed Unsawn Wafer (Wafer in box)

International
IOR Rectifier

FD200H06A5B

Fred Die in Wafer Form



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

2. CONTROLLING DIMENSION (INCH):

3. DIMENSIONS AND TOLERANCES:
   a = 5.080 ± 0.05
   (0.200 ± 0.002)
   b = 5.08 ± 0.05
   (0.200 ± 0.002)
   c = 4.420 ± 0.003
   (0.174 ± 0.0001)
   d = 4.420 ± 0.003
   (0.174 ± 0.0001)

4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)

5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade

6. MINIMUM ORDER QUANTITY:
   300 die

NOT TO SCALE

Electrical Characteristics (Wafer Form)

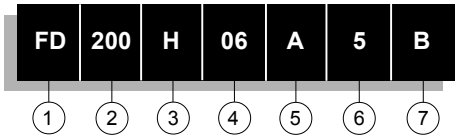
	Parameters	Units	Test Conditions
V_{FM}	Maximum Forward Voltage	2.3 V	T_J = 25°C, I_F = 30 A
V_{RRM}	Mimunum Reverse Breakdown Voltage	600 V	T_J = 25°C, I_{RRM} = 200 µA
I_{RM}	Max. Reverse Leakage Current	100µA	T_J = 25°C, V_{RRM} = 600 V
t_{rr}	Typ. Reverse Recovery Time	20 ns	I_F = 1A, di/ dt = 100A/µs, V_R = 30 V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 2 KA - 3 KA)
Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
Chip Dimensions	0.200" x 0.200" (see drawing)
Reject Ink Dot Size	0.25 mm diameter minimum
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code



1 - Fred Die

2 - Chip Dimension in Mils: 200 = 200x200 square

3 - Process H = HyperFast

4 - Voltage code Vrrm (*100) eg: 06 = 600V

5 - Chip surface metallization: A = Aluminium (anode), Silver (cathode)

6 - Wafer diameter in inches

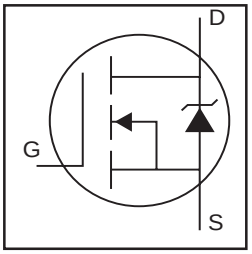
7 - Packaging: B = Inked Probed Unsawn Wafer (Wafer in box)

PD- 91874

International
IOR Rectifier

IRFC044

HEXFET® Power MOSFET Die in Wafer Form



60 V
Size 4.0
Rds(on)=0.034Ω
5" Wafer

Electrical Characteristics (Wafer Form)

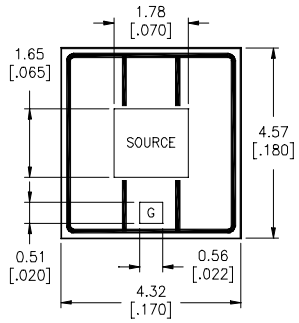
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60V Min.	V_{GS} = 0V, I_D = 100µA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	0.034Ω Max.	V_{GS} = 10V, I_D = 5.0A
$V_{GS(th)}$	Gate Threshold Voltage	2.1V Min.	V_{DS} = 5.0V, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	100µA Max.	V_{DS} = 60V, V_{GS} = 0V, T_J = 25°C
I_{GSS}	Gate-to-Source Leakage	± 10µA Max.	V_{GS} = ±20V
T_J T_{STG}	Operating Junction and Storage Temperature Range	125°C Max.	

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1kA°-2kA°-2.5kA°)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (0.004mm)
Dimensions:	0.170" x 0.180" (4.32mm x 4.57 mm)
Wafer Diameter:	125mm with 100 flat
Wafer thickness:	0.375mm + / -0.020mm
Relevant Die Mechanical Dwg. Number	01-5018
Minimum Street Width	0.084 mm
Reject Ink Dot Size	0.51mm Diameter Minimum
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRFZ44

Die Outline



NOTES:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE =	+/- 0.013
WIDTH	< [.0250] TOLERANCE =	+/- [.0005]
&	> 0.635 TOLERANCE =	+/- 0.025
LENGTH	> [.0250] TOLERANCE =	+/- [.0010]
OVERALL DIE:	< 1.270 TOLERANCE =	+/- 0.102
WIDTH	< [.050] TOLERANCE =	+/- [.004]
&	> 1.270 TOLERANCE =	+/- 0.203
LENGTH	> [.050] TOLERANCE =	+/- [.008]

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

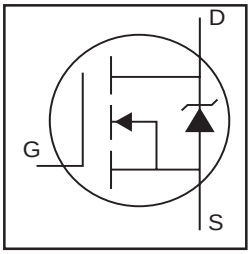
3/23/99

PD - 93776

International
IOR Rectifier

IRFC1404

HEXFET® Power MOSFET Die in Wafer Form



40V
Size 4.0
$R_{DS(on)}$=0.0029Ω
6" Wafer

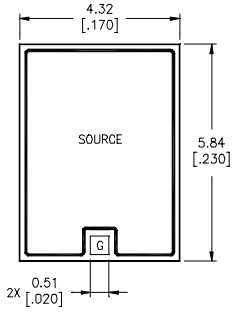
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40V Min.	V_{GS} = 0V, I_D = 250µA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	2.9mΩ Max.	V_{GS} = 10V, I_D = 45A
$V_{GS(th)}$	Gate Threshold Voltage	2.0V Min., 4.0V Max.	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	25µA Max.	V_{DS} = 40V, V_{GS} = 0V, T_J = 25°C
I_{GSS}	Gate-to-Source Leakage Current	± 200nA Max.	V_{GS} = ±20V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55°C to 175°C Max.	

Mechanical Data

Nominal Back Metal Composition, Thickness:	Cr-NiV-Ag (1kA°-2kA°-2.5kA°)
Nominal Front Metal Composition, Thickness:	100% Al (0.008 mm)
Dimensions:	.170" x .230" [4.32 mm x 5.84 mm]
Wafer Diameter:	150 mm, with 100 flat
Wafer Thickness:	0.356 mm ± 0.025 mm
Relevant Die Mechanical Drawing Number	01-5384
Minimum Street Width	0.109 mm
Reject Ink Dot Size	0.51 mm Diameter Minimum
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions:	For optimum electrical results, die attach temperature should not exceed 300 °C

Die Outline



NOTES:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:
   BONDING PADS: < 0.635 TOLERANCE = +/- 0.013
   WIDTH < [.0250] TOLERANCE = +/- [.0005]
   & > 0.635 TOLERANCE = +/- 0.025
   LENGTH > [.0250] TOLERANCE = +/- [.0010]
   OVERALL DIE: < 1.270 TOLERANCE = +/- 0.102
   WIDTH < [.050] TOLERANCE = +/- [.004]
   & > 1.270 TOLERANCE = +/- 0.203
   LENGTH > [.050] TOLERANCE = +/- [.008]
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

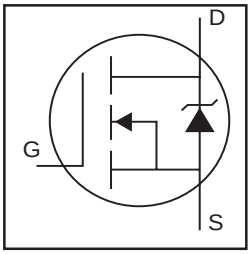
10/12/99

PD- 91873

International
IOR Rectifier

IRFC240

HEXFET® Power MOSFET Die in Wafer Form



200 V
Size 4.0
Rds(on)=0.18Ω
5" Wafer

Electrical Characteristics (Wafer Form)

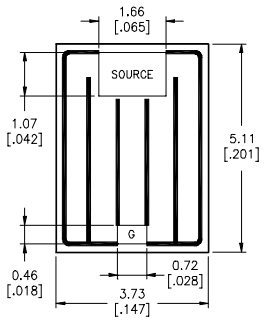
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200V Min.	V_{GS} = 0V, I_D = 100µA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	0.180Ω Max.	V_{GS} = 10V, I_D = 10A
$V_{GS(th)}$	Gate Threshold Voltage	2.3V Min., 4.0V Max.	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	25µA Max.	V_{DS} = 200V, V_{GS} = 0V, T_J = 25°C
I_{GSS}	Gate-to-Source Leakage	± 10µA Max.	V_{GS} = ±20V
T_J T_{STG}	Operating Junction and Storage Temperature Range	125°C Max.	

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1kA°-2kA°-2.5kA°)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (0.004 mm)
Dimensions:	0.147" x 0.201" (3.73mm x 5.11 mm)
Wafer Diameter:	125mm with 100 flat
Wafer thickness:	0.375mm + / -0.020mm
Relevant Die Mechanical Dwg. Number	01-5331
Minimum Street Width	0.084 mm
Reject Ink Dot Size	0.51mm Diameter Minimum
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRF640

Die Outline



NOTES:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE =	+/- 0.013
WIDTH	< [.0250] TOLERANCE =	+/- [.0005]
&	> 0.635 TOLERANCE =	+/- 0.025
LENGTH	> [.0250] TOLERANCE =	+/- [.0010]
OVERALL DIE:	< 1.270 TOLERANCE =	+/- 0.102
WIDTH	< [.050] TOLERANCE =	+/- [.004]
&	> 1.270 TOLERANCE =	+/- 0.203
LENGTH	> [.050] TOLERANCE =	+/- [.008]

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

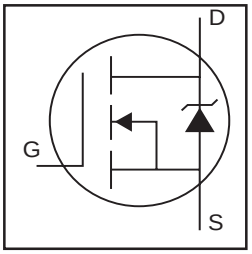
3/23/99

PD - 93777B

International
IOR Rectifier

IRFC2907

HEXFET® Power MOSFET Die in Wafer Form



75V
$R_{DS(on)}$=0.0033Ω
6" Wafer

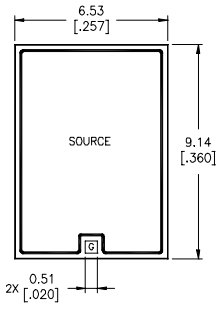
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75V Min.	V_{GS} = 0V, I_D = 250µA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	3.3mΩ Max.	V_{GS} = 10V, I_D = 45A
$V_{GS(th)}$	Gate Threshold Voltage	2.0V Min., 4.0V Max.	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	20µA Max.	V_{DS} = 75V, V_{GS} = 0V, T_J = 25°C
I_{GSS}	Gate-to-Source Leakage Current	± 200nA Max.	V_{GS} = ±20V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55°C to 175°C Max.	

Mechanical Data

Nominal Back Metal Composition, Thickness:	Cr-NiV-Ag (1kA°-2kA°-2.5kA°)
Nominal Front Metal Composition, Thickness:	100% Al (0.008 mm)
Dimensions:	.257" x .360" [6.53 mm x 9.14 mm]
Wafer Diameter:	150 mm, with 100 flat
Wafer Thickness:	0.375 mm ± 0.015 mm
Relevant Die Mechanical Drawing Number	01-5383
Minimum Street Width	0.107 mm
Reject Ink Dot Size	0.51 mm Diameter Minimum
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions:	For optimum electrical results, die attach temperature should not exceed 300 °C

Die Outline



NOTES:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:
   BONDING PADS: < 0.635 TOLERANCE = +/- 0.013
   WIDTH < [.0250] TOLERANCE = +/- [.0005]
   & > 0.635 TOLERANCE = +/- 0.025
   LENGTH > [.0250] TOLERANCE = +/- [.0010]
   OVERALL DIE: < 1.270 TOLERANCE = +/- 0.102
   WIDTH < [.050] TOLERANCE = +/- [.004]
   & > 1.270 TOLERANCE = +/- 0.203
   LENGTH > [.050] TOLERANCE = +/- [.008]
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

11/18/99

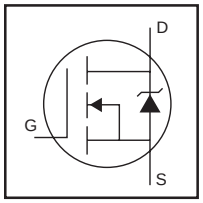
PD - 93777

International
IOR Rectifier

IRFC2907B

HEXFET® Power MOSFET Die in Wafer Form

- 100% Tested at Probe
- Available in Tape and Reel, Chip Pack, Sawn on Film and Gel Pack**
- Ultra Low On-Resistance



75V
$R_{DS(on)}$ = 2.5mΩ
(typ.)***
6" Wafer

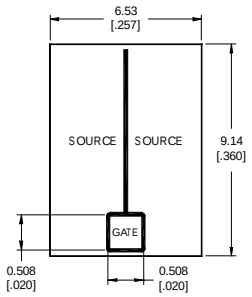
Electrical Characteristics *

Parameter	Description	Min	Typ.	Max	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75V	——	——	V_{GS} = 0V, I_D = 250µA
$R_{DS(on)}$***	Static Drain-to-Source On-Resistance	——	2.5mΩ	4.5mΩ	V_{GS} = 10V, I_D = 110A
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	——	——	20µA	V_{DS} = 75V, V_{GS} = 0V, T_J = 25°C
I_{GSS}	Gate-to-Source Leakage Current	——	——	± 200nA	V_{GS} = ±20V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55°C to 175°C Max.			

Mechanical Data

Nominal Back Metal Composition, Thickness:	Cr-NiV-Ag (1kA°-2kA°-5kA°)
Nominal Front Metal Composition, Thickness:	100% Al (0.008 mm)
Dimensions:	.257" x .360" [6.53 mm x 9.14 mm]
Wafer Diameter:	150 mm, with 100 flat
Wafer Thickness:	0.254 mm ± 0.025 mm
Relevant Die Mechanical Drawing Number	01-5403
Minimum Street Width	0.107 mm
Reject Ink Dot Size	0.51 mm Diameter Minimum
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions:	For optimum electrical results, die attach temperature should not exceed 300 °C
Reference Packaged Part	IRFP2907

Die Outline



NOTES:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

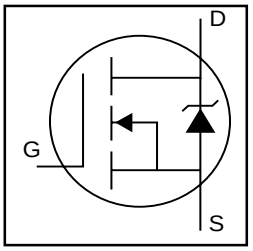
* Electrical characteristics are reported for the reference packaged part (see above) and can not be guaranteed in die sales form. Variations in customer packaging materials, dimensions and processes may affect parametric performance.
** Contact factory for these product forms.
***The typical $R_{DS(on)}$ is an estimated value for the bare die, actual results will depend on customer packaging materials and dimensions.

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IOR Rectifier

PD - 94242

IRFC43N50KB

HEXFET® Power MOSFET Die
in Wafer Form



500V
$R_{DS(on)}$=0.090Ω
6" Wafer

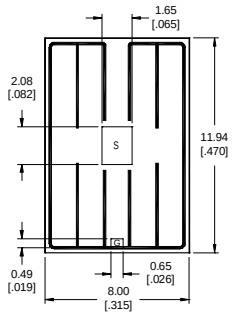
Electrical Characteristics

Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500V Min.	V_{GS} = 0V, I_D = 250µA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	0.090Ω Max.	V_{GS} = 10V, I_D = 28A
$V_{GS(th)}$	Gate Threshold Voltage	3.0V Min., 5.0V Max.	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	50µA Max.	V_{DS} = 500V, V_{GS} = 0V, T_J = 25°C
I_{GSS}	Gate-to-Source Leakage Current	± 100nA Max.	V_{GS} = ±30V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55°C to 150°C Max.	

Mechanical Data

Nominal Back Metal Composition, Thickness:	Cr-NiV-Ag (0.1µm-0.2µm-0.5µm)
Nominal Front Metal Composition, Thickness:	Al with 1% Si (0.004 mm)
Dimensions:	0.315" x 0.470" [8.00 mm x 11.94 mm]
Wafer Diameter:	150 mm
Wafer Thickness:	0.375 mm ± 0.025 mm
Relevant Die Mechanical Drawing Number	01-5444
Minimum Street Width	0.004"
Reject Ink Dot Size	0.005" Diameter Minimum
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions:	For optimum electrical results, die attach temperature should not exceed 300 °C
Referenced Package Part:	IRFPS43N50K

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

5. DIE THICKNESS = 0.254 [.010]

* Notes: Electrical characteristics are reported for the reference packaged part (see above) and cannot guaranteed in die sales form due to variations in packaging materials, dimension.

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IOR Rectifier

Preliminary Data Sheet PD-20596 rev. A 11/98

HF06A060ACE

Hexfred Die in Wafer Form

600 V
Size 06
5" Wafer

Electrical Characteristics (Wafer Form)

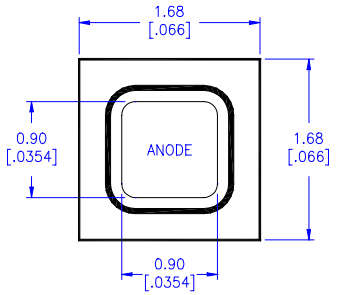
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	1.8V Max.	T_J = 25°C, I_F = 4.0A
BV_R	Reverse Breakdown Voltage	600V Min.	T_J = 25°C, I_R = 200µA
I_{RM}	Reverse Leakage Current	3µA Max.	T_J = 25°C, V_R = 600V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr-Ni-Ag (1kA-4kA-6kA)
Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
Chip Dimensions	0.066" x 0.066"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness	.015" ± .003"
Relevant Die Mechanical Dwg. Number	01-5158
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : HFA04TB60

Die Outline



NOTES :
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. DIMENSIONAL TOLERANCES :

BONDING PADS :	< 0.635 TOLERANCE = ± 0.013
WIDTH	< (.0250) TOLERANCE = ± (.0005)
&	> 0.635 TOLERANCE = ± 0.025
LENGTH	> (.0250) TOLERANCE = ± (.0010)
OVERALLDIE	< 1.270 TOLRANCE = ± 0.102
WIDTH	< (.050) TOLERANCE = ± (.004)
&	> 1.270 TOLERANCE = ± 0.203
LENGTH	> (.050) TOLERANCE = ± (.008)

International
IOR Rectifier

TARGET

HF10A060ACB

HF10A060ACB Hexfred Die in Wafer Form

600 V
Size 10
4" Wafer

Electrical Characteristics (Wafer Form)

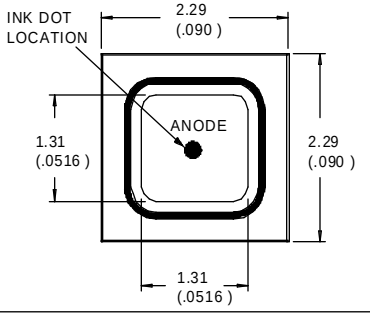
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	1.8V Max.	T_J = 25°C, I_F = 4A
BV_R	Reverse Breakdown Voltage	600V Min.	T_J = 25°C, I_R = 250µA
I_{RM}	Reverse Leakage Current	5µA Max.	T_J = 25°C, V_R =600V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni-Ag (1 kA-4kA-6kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (3 microns)
Dimensions:	0.09" x 0.09"
Wafer Diameter:	100mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5159
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	See Die Outline drawing below
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : HFA08TB60

Die Outline



NOTES :
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. LETTER DESIGNATION :
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES
   BONDING PADS : < 0.635 TOLERANCE = +/- 0.013
   WIDTH < (.0250) TOLERANCE =+/- (.0005)
   & > 0.635 TOLERANCE = +/- 0.025
   LENGTH > (.0250) TOLERANCE = +/- (.0010)
   OVERALL DIE < 1.270 TOLERANCE = +/- 0.102
   WIDTH < (.050) TOLERANCE = +/- (.004)
   & > 0.635 TOLERANCE = +/- 0.203
   LENGTH > (.050) TOLERANCE = +/- (.008)
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

Preliminary Data Sheet PD-20597 rev. A 11/98

HF10A060ACE

Hexfred Die in Wafer Form

600 V
Size 10
5" Wafer

Electrical Characteristics (Wafer Form)

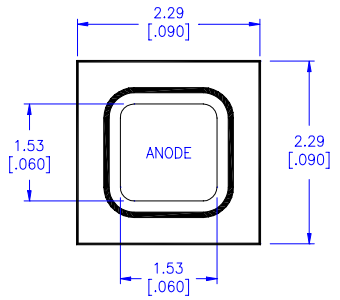
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	1.7V Max.	T_J = 25°C, I_F = 8.0A
BV_R	Reverse Breakdown Voltage	600V Min.	T_J = 25°C, I_R = 200µA
I_{RM}	Reverse Leakage Current	5µA Max.	T_J = 25°C, V_R = 600V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr-Ni-Ag (1kA-4kA-6kA)
Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
Chip Dimensions	0.090" x 0.090"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness	.015" ± .003"
Relevant Die Mechanical Dwg. Number	01-5159
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : HFA08TB60

Die Outline



NOTES :
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. DIMENSIONAL TOLERANCES :
   - BONDING PADS : < 0.635 TOLERANCE = ± 0.013
   - WIDTH < (.0250) TOLERANCE = ± (.0005)
   - & > 0.635 TOLERANCE = ± 0.025
   - LENGTH > (.0250) TOLERANCE = ± (.0010)
   - OVERALLDIE < 1.270 TOLRANCE = ± 0.102
   - WIDTH < (.050) TOLERANCE = ± (.004)
   - & > 1.270 TOLERANCE = ± 0.203
   - LENGTH > (.050) TOLERANCE = ± (.008)

International
IOR Rectifier

PD - 2.596

Preliminary # HF20A060ACE

HF20A060ACE Hexfred Die in Wafer Form

600 V
Size 20
5" Wafer

Electrical Characteristics (Wafer Form)

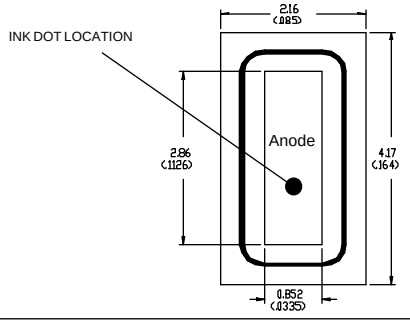
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	1.4V Max.	T_J = 25°C, I_F = 12.0A
BV_R	Reverse Breakdown Voltage	600V Min.	T_J = 25°C, I_R = 250µA
I_{RM}	Reverse Leakage Current	10µA Max.	T_J = 25°C, V_R = 600V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni-Ag (1kA-4kA-6kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (3 microns)
Dimensions:	0.107" x 0.130"
Wafer Diameter:	125mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5163
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	See Die Outline drawing below
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) :IRGBC30MD2

Die Outline



NOTES :
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. LETTER DESIGNATION :
   A : Anode
   K : Cathode
4. DIMENSIONAL TOLERANCES
   BONDING PADS : < 0.635 TOLERANCE = +/- 0.013
   WIDTH < (.0250) TOLERANCE =+/- (.0005)
   & > 0.635 TOLERANCE = +/- 0.025
   LENGTH > (.0250) TOLERANCE = +/- (.0010)
   OVERALL DIE < 1.270 TOLERANCE = +/- 0.102
   WIDTH < (.050) TOLERANCE = +/- (.004)
   & > 0.635 TOLERANCE = +/- 0.203
   LENGTH > (.050) TOLERANCE = +/- (.008)

International
IOR Rectifier

Preliminary Data Sheet PD-20613 11/98

HF20C120ACE

Hexfred Die in Wafer Form

1200 V
Size 20
5" Wafer

Electrical Characteristics (Wafer Form)

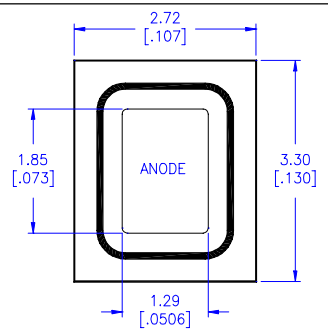
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	3.0V Max.	T_J = 25°C, I_F = 6.0A
BV_R	Reverse Breakdown Voltage	1200V Min.	T_J = 25°C, I_R = 200µA
I_{RM}	Reverse Leakage Current	5µA Max.	T_J = 25°C, V_R = 1200V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr-Ni-Ag (1kA-4kA-6kA)
Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
Chip Dimensions	0.130" x 0.107"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness	.015" ± .003"
Relevant Die Mechanical Dwg. Number	01-5165
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : HFA06TB120

Die Outline



NOTES :

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. DIMENSIONAL TOLERANCES :

BONDING PADS :	< 0.635 TOLERANCE = ± 0.013
WIDTH	< (.0250) TOLERANCE = ± (.0005)
&	> 0.635 TOLERANCE = ± 0.025
LENGTH	> (.0250) TOLERANCE = ± (.0010)
OVERALLDIE	< 1.270 TOLRANCE = ± 0.102
WIDTH	< (.050) TOLERANCE = ± (.004)
&	> 1.270 TOLERANCE = ± 0.203
LENGTH	> (.050) TOLERANCE = ± (.008)

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Preliminary Data Sheet PD-20608 rev.A 11/98

HF30A060ACE

Hexfred Die in Wafer Form

600 V
Size 30
5" Wafer

Electrical Characteristics (Wafer Form)

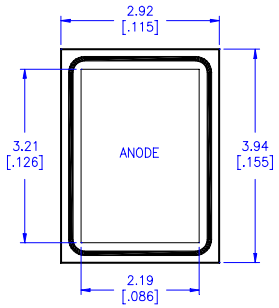
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	1.7V Max.	T_J = 25°C, I_F = 15.0A
BV_R	Reverse Breakdown Voltage	600V Min.	T_J = 25°C, I_R = 200µA
I_{RM}	Reverse Leakage Current	10µA Max.	T_J = 25°C, V_R = 600V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr-Ni-Ag (1kA-4kA-6kA)
Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
Chip Dimensions	0.115" x 0.155"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness	.015" ± .003"
Relevant Die Mechanical Dwg. Number	01-5161
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : HFA15TB60

Die Outline



NOTES :
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. DIMENSIONAL TOLERANCES :

BONDING PADS :	< 0.635 TOLERANCE = ± 0.013
WIDTH	< (.0250) TOLERANCE = ± (.0005)
&	> 0.635 TOLERANCE = ± 0.025
LENGTH	> (.0250) TOLERANCE = ± (.0010)
OVERALL DIE	< 1.270 TOLRANCE = ± 0.102
WIDTH	< (.050) TOLERANCE = ± (.004)
&	> 1.270 TOLERANCE = ± 0.203
LENGTH	> (.050) TOLERANCE = ± (.008)

International
IOR Rectifier

TARGET

HF30C120ACB

HF30C120ACB Hexfred Die in Wafer Form

1200 V
Size 30
4" Wafer

Electrical Characteristics (Wafer Form)

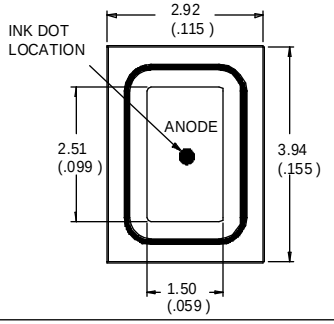
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	2.8V Max.	T_J = 25°C, I_F = 4.0A
BV_R	Reverse Breakdown Voltage	1200V Min.	T_J = 25°C, I_R = 250µA
I_{RM}	Reverse Leakage Current	10µA Max.	T_J = 25°C, V_R = 1200V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Al-Ti-Ni-Ag (1kA-1kA-4kA-6kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (3 microns)
Dimensions:	0.115" x 0.155"
Wafer Diameter:	100mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5156
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	See Die Outline drawing below
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : HFA08PB120

Die Outline



NOTES :
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. LETTER DESIGNATION :
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES
   BONDING PADS : < 0.635 TOLERANCE = +/- 0.013
   WIDTH < (.0250) TOLERANCE =+/- (.0005)
   & > 0.635 TOLERANCE = +/- 0.025
   LENGTH > (.0250) TOLERANCE = +/- (.0010)
   OVERALL DIE < 1.270 TOLERANCE = +/- 0.102
   WIDTH < (.050) TOLERANCE = +/- (.004)
   & > 0.635 TOLERANCE = +/- 0.203
   LENGTH > (.050) TOLERANCE = +/- (.008)
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

Preliminary Data Sheet PD-20502 rev. A 11/98

HF30C120ACE

Hexfred Die in Wafer Form

1200 V
Size 30
5" Wafer

Electrical Characteristics (Wafer Form)

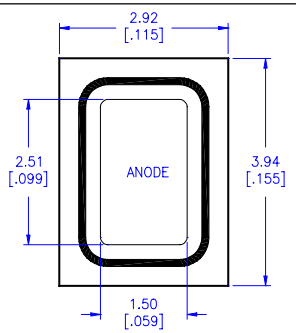
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	2.8V Max.	T_J = 25°C, I_F = 4.0A
BV_R	Reverse Breakdown Voltage	1200V Min.	T_J = 25°C, I_R = 200µA
I_{RM}	Reverse Leakage Current	10µA Max.	T_J = 25°C, V_R = 1200V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr-Ni-Ag (1kA-4kA-6kA)
Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
Chip Dimensions	0.115" x 0.155"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness	.015" ± .003"
Relevant Die Mechanical Dwg. Number	01-5167
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : HFA08PB120

Die Outline



NOTES :

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. DIMENSIONAL TOLERANCES :

BONDING PADS :	< 0.635 TOLERANCE = ± 0.013
WIDTH	< (.0250) TOLERANCE = ± (.0005)
&	> 0.635 TOLERANCE = ± 0.025
LENGTH	> (.0250) TOLERANCE = ± (.0010)
OVERALLDIE	< 1.270 TOLRANCE = ± 0.102
WIDTH	< (.050) TOLERANCE = ± (.004)
&	> 1.270 TOLERANCE = ± 0.203
LENGTH	> (.050) TOLERANCE = ± (.008)

International
IOR Rectifier

HF30D120ACE

Hexfred Die in Wafer Form

Features

- GEN3 Hexfred Technology
- Low V_F
- Low I_{RR}
- Low t_{RR}
- Soft Reverse Recovery

Benefits

- Benchmark Efficiency for Motor Control Applications
- Rugged Transient Performance
- Low EMI
- Excellent Current Sharing in Parallel Operation

1200V
$I_{F(nom)}$=15A
$V_{F(typ)}$= 2.05V @ $I_{F(nom)}$ @ 25°C
Motor Control Antiparallel Diode
125mm Wafer

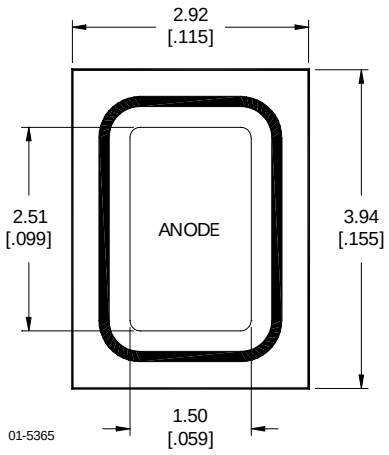
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (min, max)	Test Conditions
V_F	Forward Voltage Drop	1.50V min, 2.05V max	I_F = 7.5A, T_J = 25°C
BV_R	Reverse Breakdown Voltage	1200V min	T_J = 25°C, I_R = 150µA
I_{RM}	Reverse Leakage Current	5µA max	T_J = 25°C, V_R = 1200V

Mechanical Data

Nominal Backmetal Composition, (Thickness)	Cr- Ni - Ag, (1kA - 4kA - 6kA)
Nominal Front Metal Composition, (Thickness)	99% Al/1% Si, (3µm)
Dimensions	0.115" x 0.155"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness, Tolerance	310µm, +/-15µm
Relevant Die Mechanical Dwg. Number	01 - 5365
Minimum Street Width	100µm
Reject Ink Dot Size	0.25mm diameter minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300°C

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

Fig.1 - Typical Diode Recovery
V_{CC}=600V; Rg=10Ω; T_J=125°C;
L=200µH; Driver=IRGC15B120KB

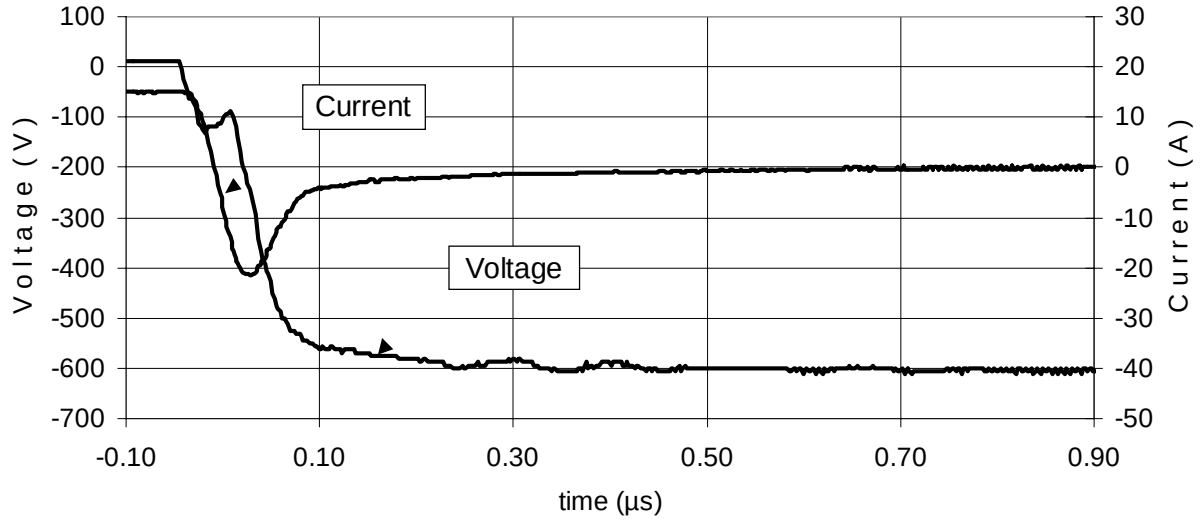


Fig.2 - Typical Diode Forward Characteristic
tp=300µs

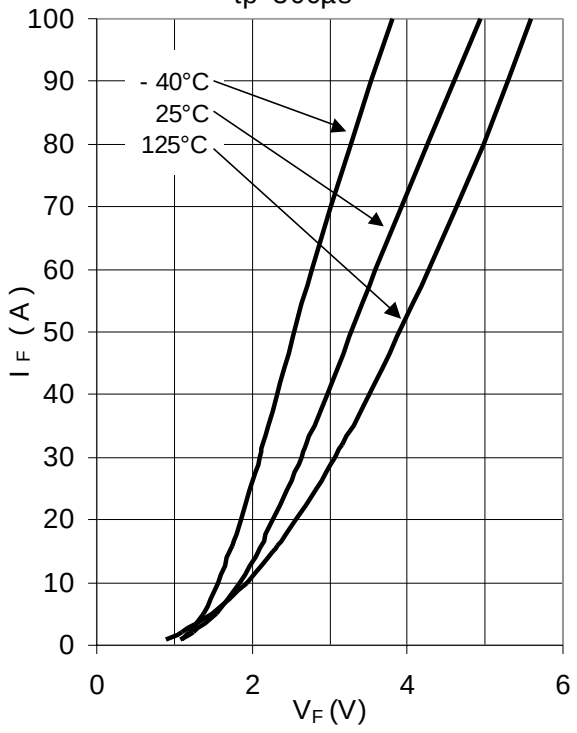
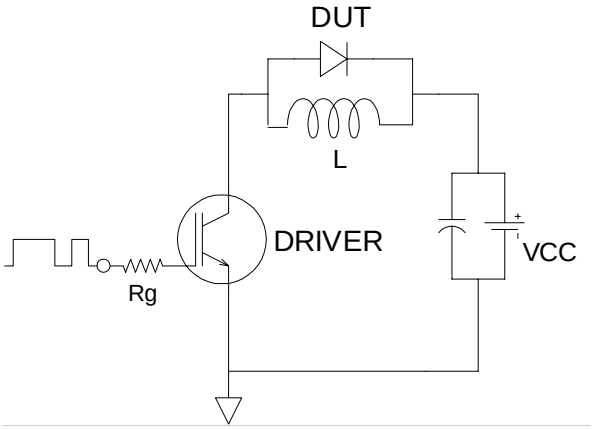


Fig. 3 - Diode Recovery Circuit



International
IOR Rectifier

TARGET

HF40A060ACB

HF40A060ACB Hexfred Die in Wafer Form

600 V
Size 40
4" Wafer

Electrical Characteristics (Wafer Form)

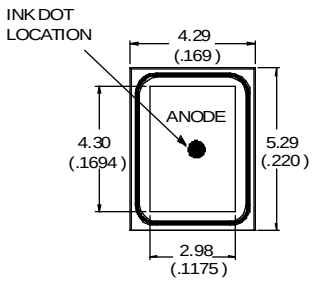
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	1.6V Max.	T_J = 25°C, I_F = 10A
BV_R	Reverse Breakdown Voltage	600V Min.	T_J = 25°C, I_R = 250µA
I_{RM}	Reverse Leakage Current	20µA Max.	T_J = 25°C, V_R =600V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni-Ag (1 kA-4kA-6kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (3 microns)
Dimensions:	0.169" x 0.220"
Wafer Diameter:	100mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5162
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	See Die Outline drawing below
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : HFA25TB60

Die Outline



NOTES :
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. LETTER DESIGNATION :
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES
   BONDING PADS : < 0.635 TOLERANCE = +/- 0.013
   WIDTH < (.0250) TOLERANCE =+/- (.0005)
   & > 0.635 TOLERANCE = +/- 0.025
   LENGTH > (.0250) TOLERANCE = +/- (.0010)
   OVERALL DIE < 1.270 TOLERANCE = +/- 0.102
   WIDTH < (.050) TOLERANCE = +/- (.004)
   & > 0.635 TOLERANCE = +/- 0.203
   LENGTH > (.050) TOLERANCE = +/- (.008)
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

Preliminary Data Sheet PD-20498 rev.A 11/98

HF40A060ACE

Hexfred Die in Wafer Form

600 V
Size 40
5" Wafer

Electrical Characteristics (Wafer Form)

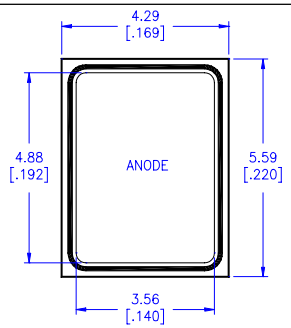
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	1.6V Max.	T_J = 25°C, I_F = 10A
BV_R	Reverse Breakdown Voltage	600V Min.	T_J = 25°C, I_R = 200µA
I_{RM}	Reverse Leakage Current	20µA Max.	T_J = 25°C, V_R = 600V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr-Ni-Ag (1kA-4kA-6kA)
Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
Chip Dimensions	0.169" x 0.220"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness	.015" ± .003"
Relevant Die Mechanical Dwg. Number	01-5169
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : HFA25TB60

Die Outline



NOTES:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. DIMENSIONAL TOLERANCES:

BONDING PADS :	< 0.635 TOLERANCE = ± 0.013
WIDTH	< (.0250) TOLERANCE = ± (.0005)
&	> 0.635 TOLERANCE = ± 0.025
LENGTH	> (.0250) TOLERANCE = ± (.0010)
OVERALLDIE	< 1.270 TOLRANCE = ± 0.102
WIDTH	< (.050) TOLERANCE = ± (.004)
&	> 1.270 TOLERANCE = ± 0.203
LENGTH	> (.050) TOLERANCE = ± (.008)

International
IOR Rectifier

TARGET

HF40C120ACB

HF40C120ACB Hexfred Die in Wafer Form

1200 V
Size 40
4" Wafer

Electrical Characteristics (Wafer Form)

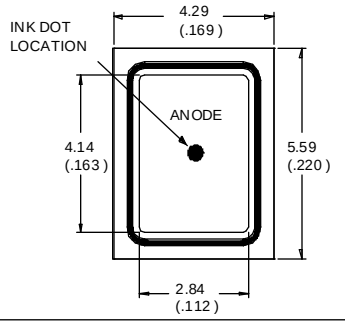
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	2.6V Max.	T_J = 25°C, I_F = 8.0A
BV_R	Reverse Breakdown Voltage	1200V Min.	T_J = 25°C, I_R = 250µA
I_{RM}	Reverse Leakage Current	20µA Max.	T_J = 25°C, V_R = 1200V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Al-Ti-Ni-Ag (1kA-1kA-4kA-6kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (3 microns)
Dimensions:	0.169" x 0.220"
Wafer Diameter:	100mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5157
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	See Die Outline drawing below
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : HFA16PB120

Die Outline



NOTES :
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. LETTER DESIGNATION :
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES
   BONDING PADS : < 0.635 TOLERANCE = +/- 0.013
   WIDTH < (.0250) TOLERANCE =+/- (.0005)
   & > 0.635 TOLERANCE = +/- 0.025
   LENGTH > (.0250) TOLERANCE = +/- (.0010)
   OVERALL DIE < 1.270 TOLERANCE = +/- 0.102
   WIDTH < (.050) TOLERANCE = +/- (.004)
   & > 0.635 TOLERANCE = +/- 0.203
   LENGTH > (.050) TOLERANCE = +/- (.008)
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

Preliminary Data Sheet PD-20497 rev. A 11/98

HF40C120ACE

Hexfred Die in Wafer Form

1200 V
Size 40
5" Wafer

Electrical Characteristics (Wafer Form)

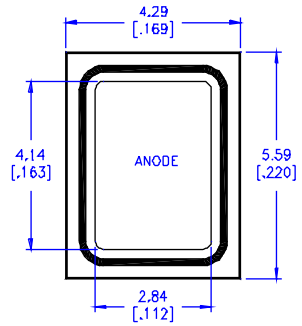
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	2.6V Max.	T_J = 25°C, I_F = 8.0A
BV_R	Reverse Breakdown Voltage	1200V Min.	T_J = 25°C, I_R = 200µA
I_{RM}	Reverse Leakage Current	20µA Max.	T_J = 25°C, V_R = 1200V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr-Ni-Ag (1kA-4kA-6kA)
Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
Chip Dimensions	0.169" x 0.220"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness	.015" ± .003"
Relevant Die Mechanical Dwg. Number	01-5170
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	See Die Outline drawing below
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : HFA16PB120

Die Outline



NOTES :
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. DIMENSIONAL TOLERANCES :

BONDING PADS :	< 0.635 TOLERANCE = ± 0.013
WIDTH	< (.0250) TOLERANCE = ± (.0005)
&	> 0.635 TOLERANCE = ± 0.025
LENGTH	> (.0250) TOLERANCE = ± (.0010)
OVERALL DIE	< 1.270 TOLRANCE = ± 0.102
WIDTH	< (.050) TOLERANCE = ± (.004)
&	> 1.270 TOLERANCE = ± 0.203
LENGTH	> (.050) TOLERANCE = ± (.008)

International
IOR Rectifier

HF40D120ACE

Hexfred Die in Wafer Form

Features
- GEN3 Hexfred Technology
- Low V_F
- Low I_{RR}
- Low t_{RR}
- Soft Reverse Recovery

Benefits
- Benchmark Efficiency for Motor Control Applications
- Rugged Transient Performance
- Low EMI
- Excellent Current Sharing in Parallel Operation

1200V
$I_{F(nom)}$=25A
$V_{F(typ)}$= 1.78V @ $I_{F(nom)}$ @ 25°C
Motor Control Antiparallel Diode
125mm Wafer

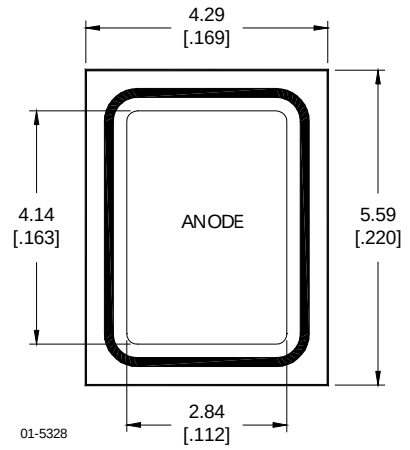
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (min, max)	Test Conditions
V_F	Forward Voltage Drop	1.30V min, 1.7V max	I_F = 10A, T_J = 25°C
BV_R	Reverse Breakdown Voltage	1200V min	T_J = 25°C, I_R = 150µA
I_{RM}	Reverse Leakage Current	10µA max	T_J = 25°C, V_R = 1200V

Mechanical Data

Nominal Backmetal Composition, (Thickness)	Cr- Ni - Ag, (1kA - 4kA - 6kA)
Nominal Front Metal Composition, (Thickness)	99% Al/1% Si, (3µm)
Dimensions	0.169" x 0.220"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness, Tolerance	310µm, +/-15µm
Relevant Die Mechanical Dwg. Number	01 - 5328
Minimum Street Width	100µm
Reject Ink Dot Size	0.25mm diameter minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300°C

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

Fig.1 - Typical Diode Recovery
V_{CC}=600V; Rg=5Ω; T_J=125°C;
L=200µH; Driver=IRGC25B120KB

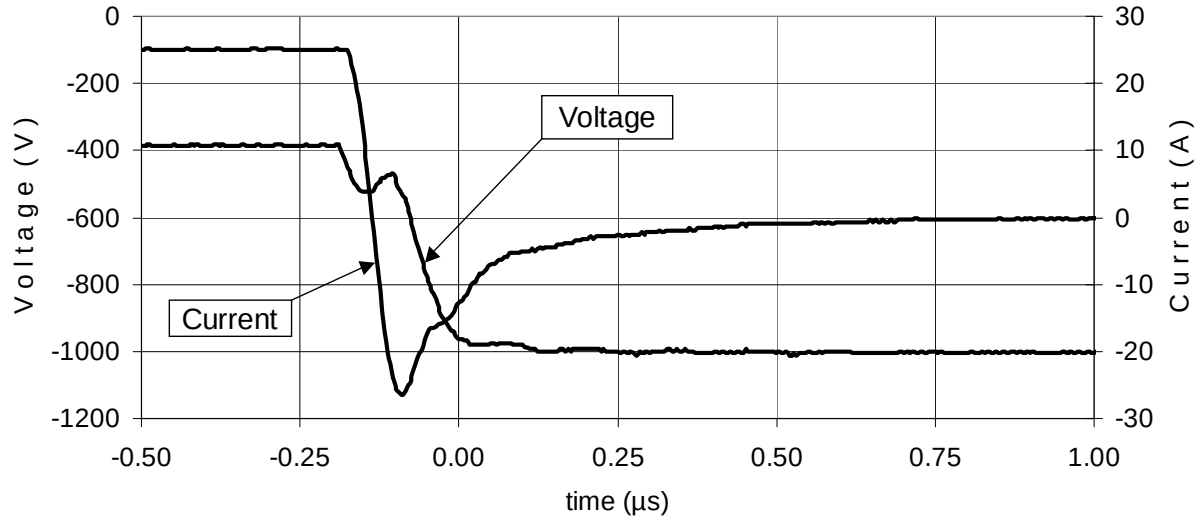


Fig.2 - Typical Diode Forward Characteristic
tp=300µs

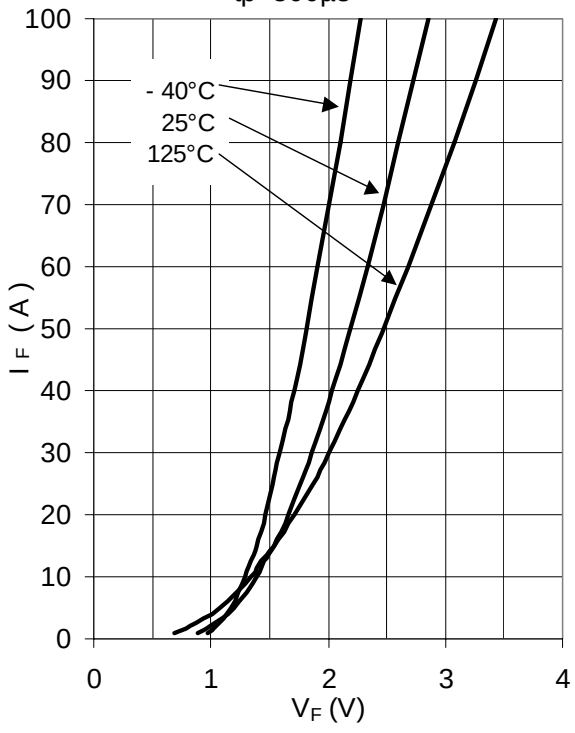
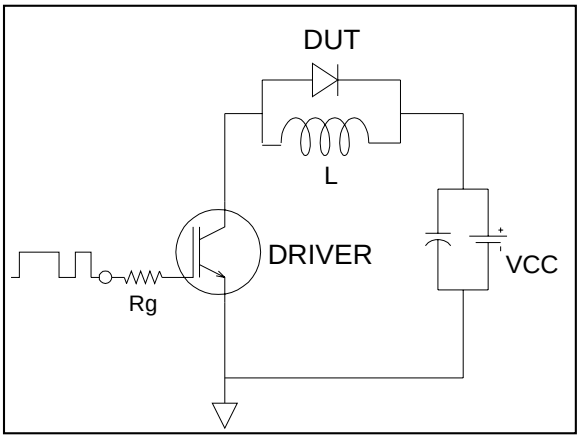


Fig. 3 - Diode Recovery Circuit



International
IOR Rectifier

HF42A040SCE

Hexfred Die in Wafer Form

400 V
Size 42
5" Wafer

Electrical Characteristics (Wafer Form)

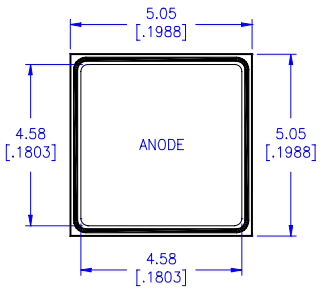
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	1.2V Max.	T_J = 25°C, I_F = 60A
BV_R	Reverse Breakdown Voltage	400V Min.	T_J = 25°C, I_R = 200µA
I_{RM}	Reverse Leakage Current	6µA Max.	T_J = 25°C, V_R = 400V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr-Ni-Ag (1kA-4kA-6kA)
Nominal Front Metal Composition, Thickness	Ti-Ni-Ag (2kA-1kA-35kA)
Chip Dimensions	0.1988" x 0.1988"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness	.015" ± .003"
Relevant Die Mechanical Dwg. Number	01-5313
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : HFA120MD40C

Die Outline



NOTES:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. DIMENSIONAL TOLERANCES:

BONDING PADS :	< 0.635 TOLERANCE = ± 0.013
WIDTH	< (.0250) TOLERANCE = ± (.0005)
&	> 0.635 TOLERANCE = ± 0.025
LENGTH	> (.0250) TOLERANCE = ± (.0010)
OVERALLDIE	< 1.270 TOLRANCE = ± 0.102
WIDTH	< (.050) TOLERANCE = ± (.004)
&	> 1.270 TOLERANCE = ± 0.203
LENGTH	> (.050) TOLERANCE = ± (.008)

International
IOR Rectifier

HF42A060SCE

Hexfred Die in Wafer Form

600 V
Size 42
5" Wafer

Electrical Characteristics (Wafer Form)

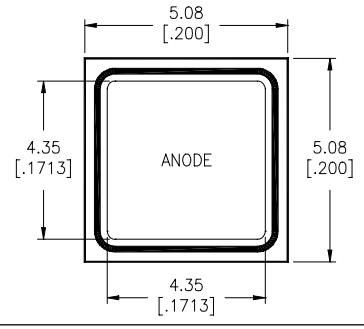
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	1.4V Max.	T_J = 25°C, I_F = 50A
BV_R	Reverse Breakdown Voltage	600V Min.	T_J = 25°C, I_R = 200µA
I_{RM}	Reverse Leakage Current	20µA Max.	T_J = 25°C, V_R = 600V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr-Ni-Ag (1kA-4kA-6kA)
Nominal Front Metal Composition, Thickness	Ti-Ni-Ag (2kA-1kA-35kA)
Chip Dimensions	0.200" x 0.200"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness	.015" ± .003"
Relevant Die Mechanical Dwg. Number	01-5314
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : HFA100MD60C

Die Outline



NOTES :
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. DIMENSIONAL TOLERANCES :

BONDING PADS :	< 0.635 TOLERANCE = ± 0.013
WIDTH	< (.0250) TOLERANCE = ± (.0005)
&	> 0.635 TOLERANCE = ± 0.025
LENGTH	> (.0250) TOLERANCE = ± (.0010)
OVERALLDIE	< 1.270 TOLRANCE = ± 0.102
WIDTH	< (.050) TOLERANCE = ± (.004)
&	> 1.270 TOLERANCE = ± 0.203
LENGTH	> (.050) TOLERANCE = ± (.008)

International
IOR Rectifier

Preliminary

HF50A060ACB

HF50A060ACB Hexfred Die in Wafer Form

600 V
Size 50
5" Wafer

Electrical Characteristics (Wafer Form)

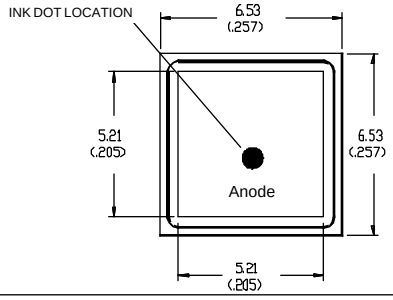
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	1.0V Max.	T_J = 25°C, I_F = 10.0A
BV_R	Reverse Breakdown Voltage	600V Min.	T_J = 25°C, I_R = 250µA
I_{RM}	Reverse Leakage Current	25µA Max.	T_J = 25°C, V_R = 600V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni-Ag (1kA-4kA-6kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (3 microns)
Dimensions:	0.257" x 0.205"
Wafer Diameter:	125mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5163
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	See Die Outline drawing below
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : GA75TS60U

Die Outline



NOTES :
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. LETTER DESIGNATION :
   A : Anode
   K : Cathode
4. DIMENSIONAL TOLERANCES
   BONDING PADS : < 0.635 TOLERANCE = +/- 0.013
   WIDTH & LENGTH: < (.0250) TOLERANCE =+/- (.0005)
   > 0.635 TOLERANCE = +/- 0.025
   > (.0250) TOLERANCE = +/- (.0010)
   OVERALL DIE WIDTH & LENGTH: < 1.270 TOLERANCE = +/- 0.102
   < (.050) TOLERANCE = +/- (.004)
   > 0.635 TOLERANCE = +/- 0.203
   > (.050) TOLERANCE = +/- (.008)

International
IOR Rectifier

Preliminary Data Sheet PD-20599 rev. B 11/98

HF50A060ACE

Hexfred Die in Wafer Form

600 V
Size 50
5" Wafer

Electrical Characteristics (Wafer Form)

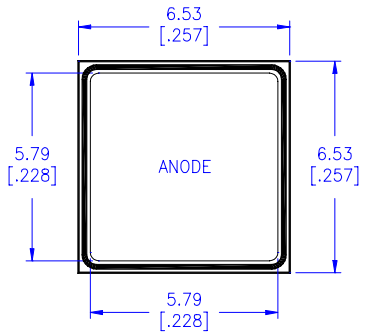
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	1.2V Max.	T_J = 25°C, I_F = 10.0A
BV_R	Reverse Breakdown Voltage	600V Min.	T_J = 25°C, I_R = 200µA
I_{RM}	Reverse Leakage Current	25µA Max.	T_J = 25°C, V_R = 600V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr-Ni-Ag (1kA-4kA-6kA)
Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
Chip Dimensions	0.257" x 0.257"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness	.015" ± .003"
Relevant Die Mechanical Dwg. Number	01-5171
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : IRG4PSC71KD

Die Outline



NOTES :

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. DIMENSIONAL TOLERANCES :

BONDING PADS :	< 0.635 TOLERANCE = ± 0.013
WIDTH	< (.0250) TOLERANCE = ± (.0005)
&	> 0.635 TOLERANCE = ± 0.025
LENGTH	> (.0250) TOLERANCE = ± (.0010)
OVERALLDIE	< 1.270 TOLRANCE = ± 0.102
WIDTH	< (.050) TOLERANCE = ± (.004)
&	> 1.270 TOLERANCE = ± 0.203
LENGTH	> (.050) TOLERANCE = ± (.008)

International
IOR Rectifier

Preliminary Data Sheet PD-20598 rev. B 11/98

HF50C120ACE

Hexfred Die in Wafer Form

1200 V
Size 50
5" Wafer

Electrical Characteristics (Wafer Form)

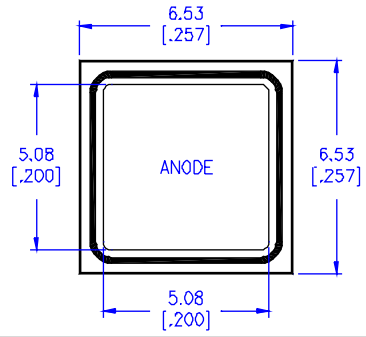
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	3.0V Max.	T_J = 25°C, I_F = 16A
BV_R	Reverse Breakdown Voltage	1200V Min.	T_J = 25°C, I_R = 200µA
I_{RM}	Reverse Leakage Current	20µA Max.	T_J = 25°C, V_R = 1200V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr-Ni-Ag (1kA-4kA-6kA)
Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
Chip Dimensions	0.257" x 0.257"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness	.015" ± .003"
Relevant Die Mechanical Dwg. Number	01-5168
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) :HFA30PB120

Die Outline



NOTES :
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. DIMENSIONAL TOLERANCES :

BONDING PADS :	< 0.635	TOLERANCE = ±0.013
WIDTH	< (.0250)	TOLERANCE = ± (.0005)
&	> 0.635	TOLERANCE = ±0.025
LENGTH	> (.0250)	TOLERANCE = ± (.0010)
OVERALLDIE	< 1.270	TOLRANCE = ±0.102
WIDTH	< (.050)	TOLERANCE = ± (.004)
&	> 1.270	TOLERANCE = ±0.203
LENGTH	> (.050)	TOLERANCE = ± (.008)

International
IOR Rectifier

HF50D120ACE

Hexfred Die in Wafer Form

Features
- GEN3 Hexfred Technology
- Low V_F
- Low I_{RR}
- Low t_{RR}
- Soft Reverse Recovery

Benefits
- Benchmark Efficiency for Motor Control Applications
- Rugged Transient Performance
- Low EMI
- Excellent Current Sharing in Parallel Operation

1200V
$I_{F(nom)}$=50A
$V_{F(typ)}$= 1.78V @ $I_{F(nom)}$ @ 25°C
Motor Control Antiparallel Diode
125mm Wafer

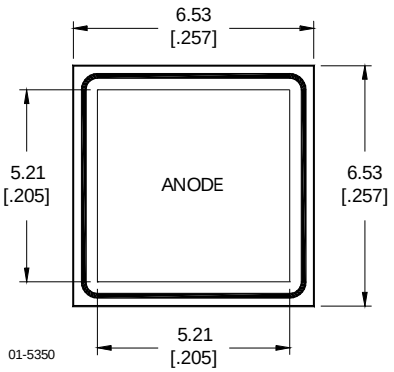
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (min, max)	Test Conditions
V_F	Forward Voltage Drop	1.15V min, 1.47V max	I_C = 10A, T_J = 25°C
BV_R	Reverse Breakdown Voltage	1200V min	T_J = 25°C, I_R = 150µA
I_{RM}	Reverse Leakage Current	20µA max	T_J = 25°C, V_R = 1200V

Mechanical Data

Nominal Backmetal Composition, (Thickness)	Cr- Ni - Ag, (1kA - 4kA - 6kA)
Nominal Front Metal Composition, (Thickness)	99% Al/1% Si, (3µm)
Dimensions	0.257' x 0.257"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness, Tolerance	310µm, +/-15µm
Relevant Die Mechanical Dwg. Number	01 - 5350
Minimum Street Width	100µm
Reject Ink Dot Size	0.25mm diameter minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300°C

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

Fig.1 - Typical Diode Recovery
V_{CC}=600V; Rg=5Ω; T_J=125°C;
L=200µH; Driver=IRGC50B120KB

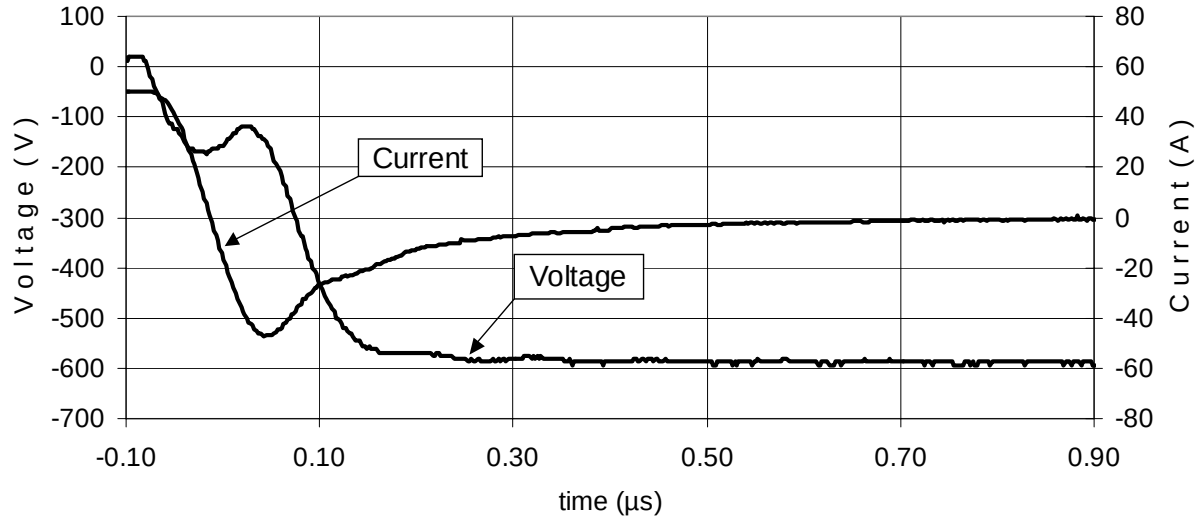


Fig.2 - Typical Diode Forward Characteristic
tp=300µs

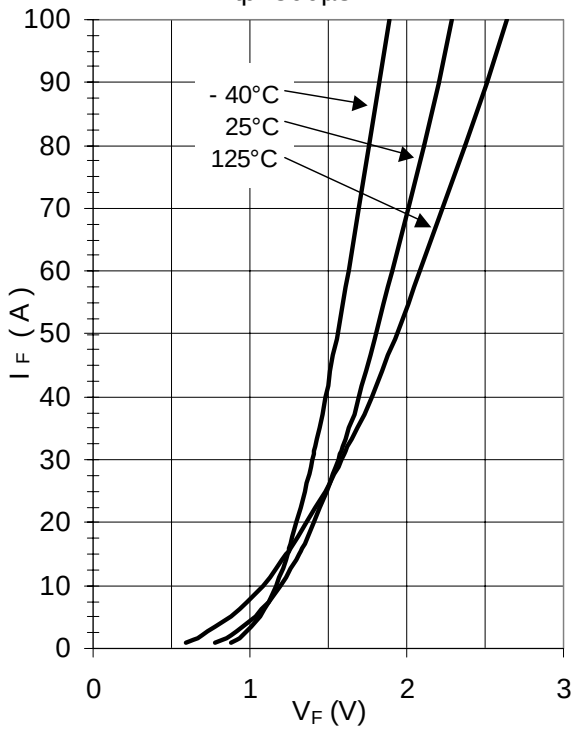
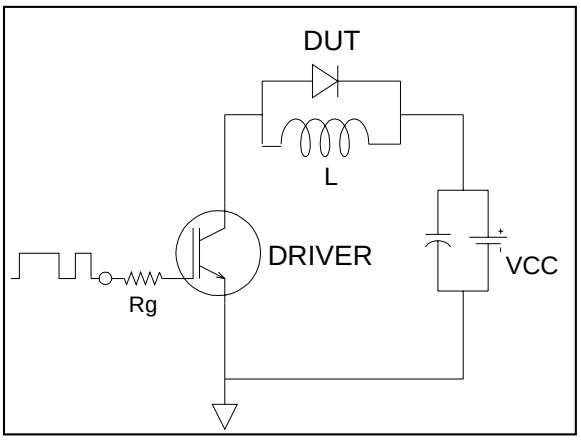


Fig. 3 - Diode Recovery Circuit



International
IOR Rectifier

Preliminary Data Sheet PD-20610 11/98

HF51A060ACE

Hexfred Die in Wafer Form

600 V
Size 51
5" Wafer

Electrical Characteristics (Wafer Form)

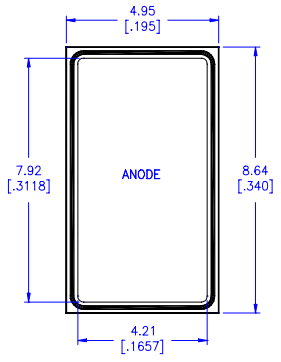
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	1.2V Max.	T_J = 25°C, I_F = 10.0A
BV_R	Reverse Breakdown Voltage	600V Min.	T_J = 25°C, I_R = 200µA
I_{RM}	Reverse Leakage Current	25µA Max.	T_J = 25°C, V_R = 600V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr-Ni-Ag (1kA-4kA-6kA)
Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
Chip Dimensions	0.340" x 0.195"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness	.015" ± .003"
Relevant Die Mechanical Dwg. Number	01-5312
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : IRG4PSC71KD

Die Outline



NOTES :
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. DIMENSIONAL TOLERANCES :

BONDING PADS :	< 0.635 TOLERANCE = ± 0.013
WIDTH	< (.0250) TOLERANCE = ± (.0005)
&	> 0.635 TOLERANCE = ± 0.025
LENGTH	> (.0250) TOLERANCE = ± (.0010)
OVERALLDIE	< 1.270 TOLRANCE = ± 0.102
WIDTH	< (.050) TOLERANCE = ± (.004)
&	> 1.270 TOLERANCE = ± 0.203
LENGTH	> (.050) TOLERANCE = ± (.008)

International
IOR Rectifier

Preliminary Data Sheet PD-20609 11/98

HF51C120ACE

Hexfred Die in Wafer Form

1200 V
Size 51
5" Wafer

Electrical Characteristics (Wafer Form)

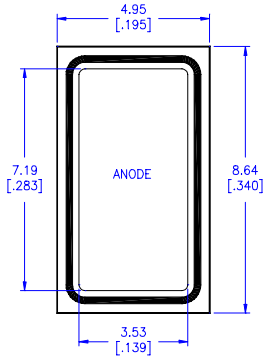
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
V_{FM}	Forward Voltage	3V Max.	T_J = 25°C, I_F = 16A
BV_R	Reverse Breakdown Voltage	1200V Min.	T_J = 25°C, I_R = 200µA
I_{RM}	Reverse Leakage Current	20µA Max.	T_J = 25°C, V_R = 1200V

Mechanical Data

Nominal Back Metal Composition, Thickness	Cr-Ni-Ag (1kA-4kA-6kA)
Nominal Front Metal Composition, Thickness	99% Al, 1% Si (3 microns)
Chip Dimensions	0.340" x 0.195"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness	.015" ± .003"
Relevant Die Mechanical Dwg. Number	01-5172
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : HFA30PB120

Die Outline



NOTES :
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. DIMENSIONAL TOLERANCES :

BONDING PADS :	< 0.635 TOLERANCE = ± 0.013
WIDTH	< (.0250) TOLERANCE = ± (.0005)
&	> 0.635 TOLERANCE = ± 0.025
LENGTH	> (.0250) TOLERANCE = ± (.0010)
OVERALLDIE	< 1.270 TOLRANCE = ± 0.102
WIDTH	< (.050) TOLERANCE = ± (.004)
&	> 1.270 TOLERANCE = ± 0.203
LENGTH	> (.050) TOLERANCE = ± (.008)

International
IOR Rectifier

HF70D120ACE

Hexfred Die in Wafer Form

Features

- GEN3 Hexfred Technology
- Low V_F
- Low I_{RR}
- Low t_{RR}
- Soft Reverse Recovery

Benefits

- Benchmark Efficiency for Motor Control Applications
- Rugged Transient Performance
- Low EMI
- Excellent Current Sharing in Parallel Operation

1200V
$I_{F(nom)}$=75A
$V_{F(typ)}$= 1.75V @ $I_{F(nom)}$ @ 25°C
Motor Control Antiparallel Diode
125mm Wafer

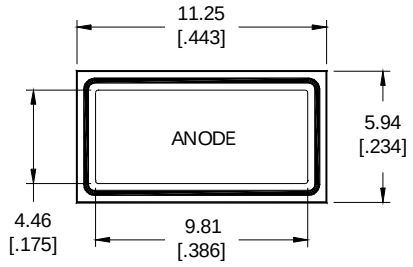
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (min, max)	Test Conditions
V_F	Forward Voltage Drop	0.99V min,1.31V max	I_F = 10A, T_J = 25°C
BV_R	Reverse Breakdown Voltage	1200V min	T_J = 25°C, I_R = 500µA
I_{RM}	Reverse Leakage Current	30µA max	T_J = 25°C, V_R = 1200V

Mechanical Data

Nominal Backmetal Composition, (Thickness)	Cr- Ni - Ag, (1kA - 4kA - 6kA)
Nominal Front Metal Composition, (Thickness)	99% Al/1% Si, (3µm)
Dimensions	0.234" x 0.443"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness, Tolerance	310µm, +/-15µm
Relevant Die Mechanical Dwg. Number	01-5364
Minimum Street Width	100µm
Reject Ink Dot Size	0.25mm diameter minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300°C

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

01-5364

Fig.1 - Typical Diode Recovery
V_{CC}=600V; Rg=5Ω; T_J=125°C;
L=200µH; Driver=IRGC75B120KB

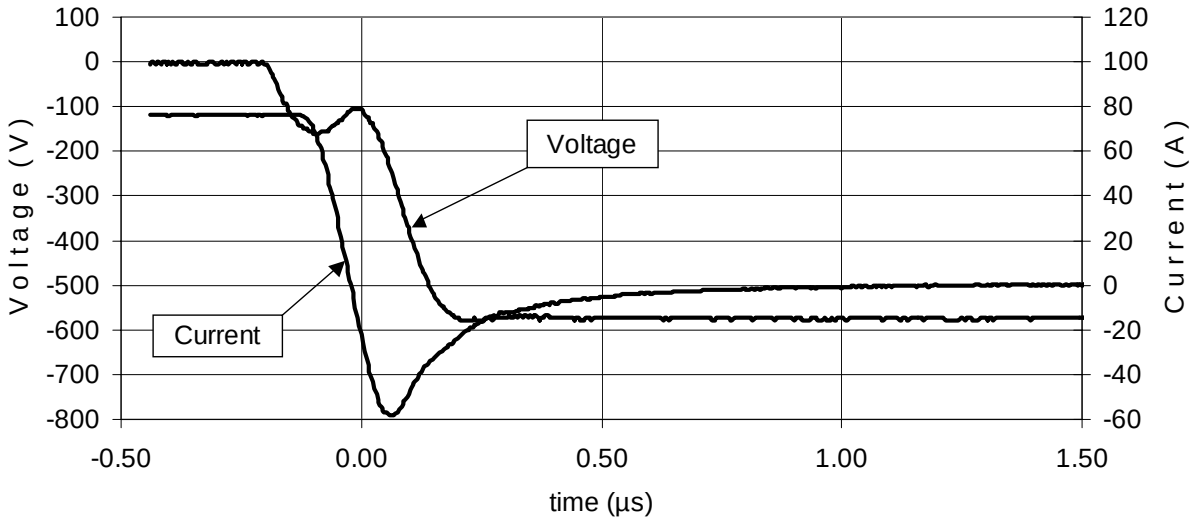


Fig.2 - Typical Diode Forward Characteristic
tp=300µs

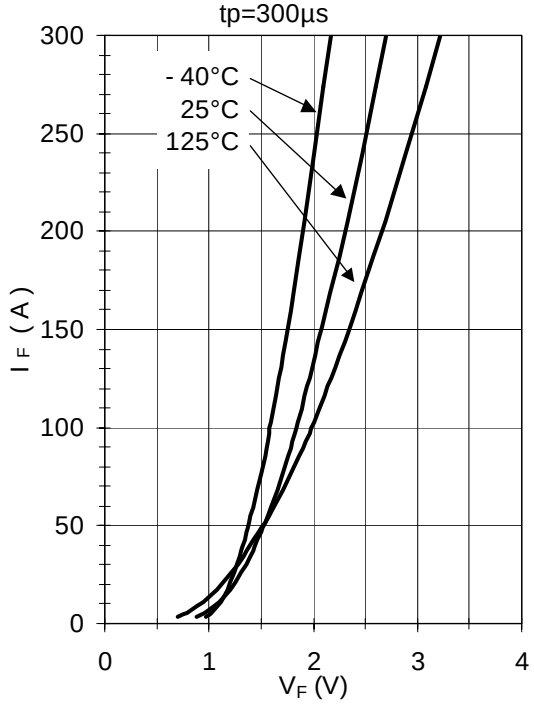
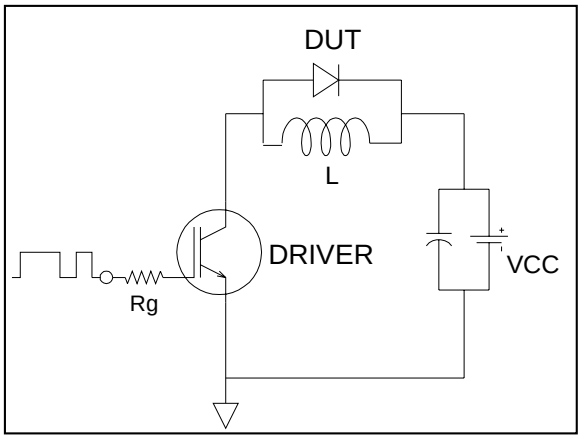


Fig. 3 - Diode Recovery Circuit



International
IOR Rectifier

HF72D120ACE

Hexfred Die in Wafer Form

Features
- GEN3 Hexfred Technology
- Low V_F
- Low I_{RR}
- Low t_{RR}
- Soft Reverse Recovery

Benefits
- Benchmark Efficiency for Motor Control Applications
- Rugged Transient Performance
- Low EMI
- Excellent Current Sharing in Parallel Operation

1200V
$I_{F(nom)}$=100A
$V_{F(typ)}$= 1.82V @ $I_{F(nom)}$ @ 25°C
Motor Control Antiparallel Diode
125mm Wafer

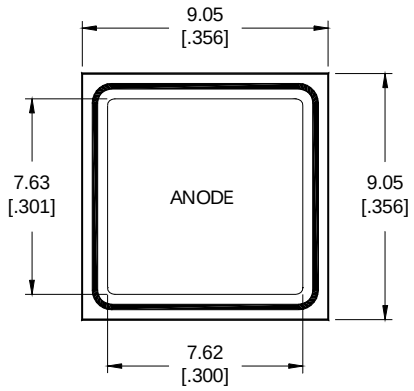
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (min, max)	Test Conditions
V_F	Forward Voltage Drop	0.98 V min,1.25 V max	I_F = 10A, T_J = 25°C
BV_R	Reverse Breakdown Voltage	1200V min	T_J = 25°C, I_R = 500µA
I_{RM}	Reverse Leakage Current	40µA max	T_J = 25°C, V_R = 1200V

Mechanical Data

Nominal Backmetal Composition, (Thickness)	Cr- Ni - Ag, (1kA - 4kA - 6kA)
Nominal Front Metal Composition, (Thickness)	99% Al/1% Si, (3µm)
Dimensions	0.356" x 0.356"
Wafer Diameter	125mm, with std. < 100 > flat
Wafer Thickness, Tolerance	310µm, +/-15µm
Relevant Die Mechanical Dwg. Number	01-5319
Minimum Street Width	100µm
Reject Ink Dot Size	0.25mm diameter minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300°C

Die Outline



01-5319

NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE = +/- 0.013
WIDTH	< [.0250] TOLERANCE = +/- [.0005]
&	> 0.635 TOLERANCE = +/- 0.025
LENGTH	> [.0250] TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270 TOLERANCE = +/- 0.102
WIDTH	< [.050] TOLERANCE = +/- [.004]
&	> 1.270 TOLERANCE = +/- 0.203
LENGTH	> [.050] TOLERANCE = +/- [.008]

Fig.1 - Typical Diode Recovery
V_{CC}=600V; Rg=5Ω; T_J=125°C;
L=200µH; Driver=IRGC100B120KB

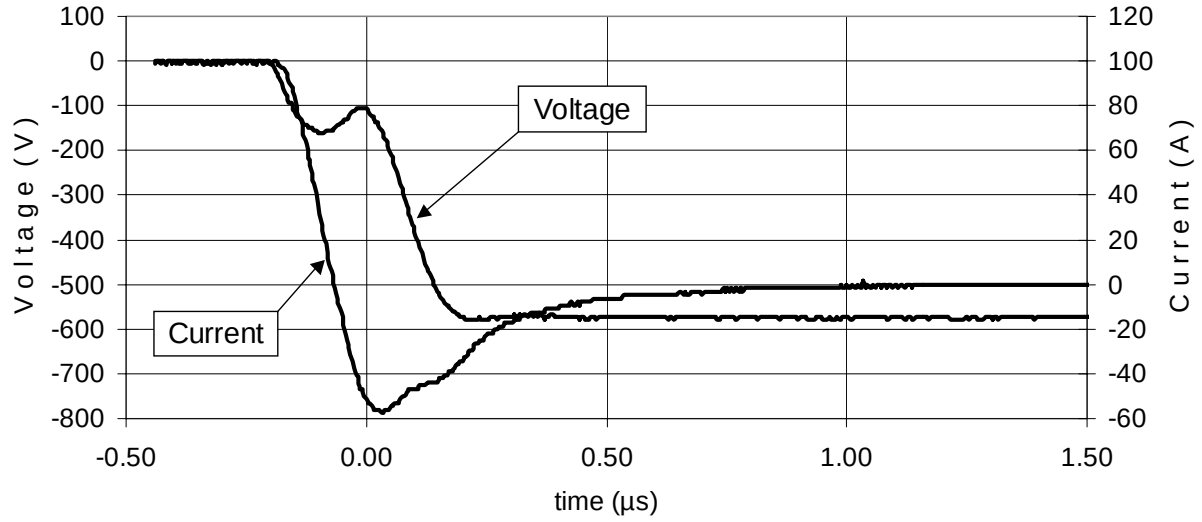


Fig.2 - Typical Diode Forward Characteristic
tp=300µs

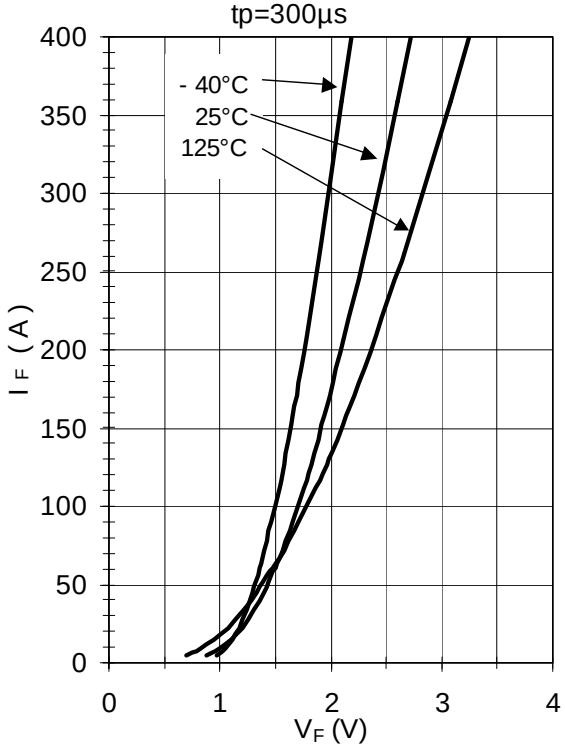
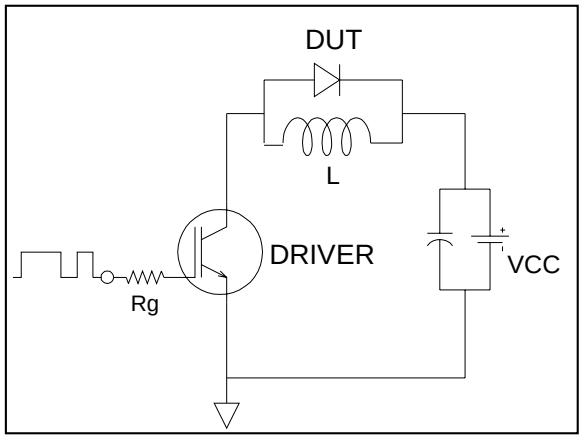


Fig. 3 - Diode Recovery Circuit



International
IOR Rectifier

Data Sheet No. PD60043-N

IR2101(S)
IR2102(S)

HIGH AND LOW SIDE DRIVER

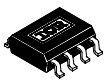
Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 3.3V, 5V, and 15V logic input compatible
- Matched propagation delay for both channels
- Outputs in phase with inputs (IR2101) or out of phase with inputs (IR2102)

Product Summary

V_{OFFSET}	600V max.
I_O+/-	130 mA / 270 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	160 & 150 ns
Delay Matching	50 ns

Packages



8 Lead SOIC

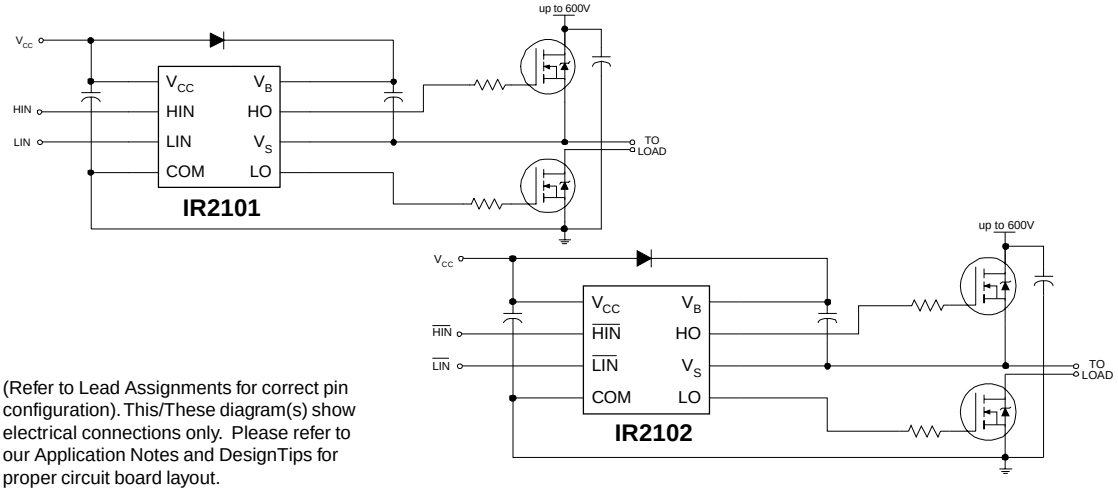


8 Lead PDIP

Description

The IR2101(S)/IR2102(S) are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN)		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN) (IR2101) & ($\overline{HIN}$ & $\overline{LIN}$) (IR2102)	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

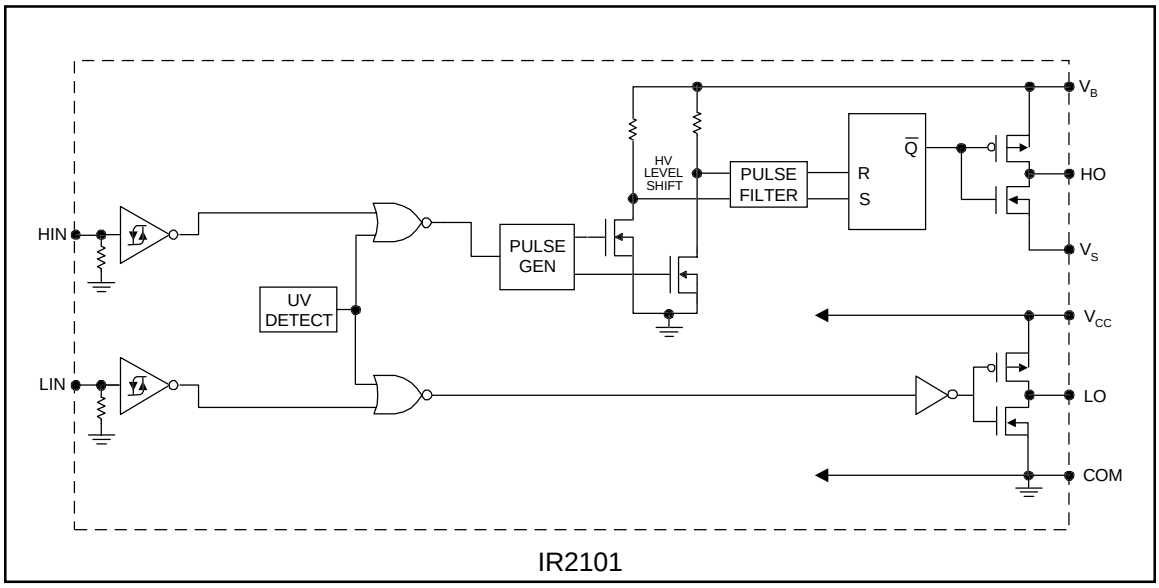
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	160	220	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	150	220		V_S = 600V
t_r	Turn-on rise time	—	100	170		
t_f	Turn-off fall time	—	50	90		
MT	Delay matching, HS & LS turn-on/off	—	—	50		

Static Electrical Characteristics

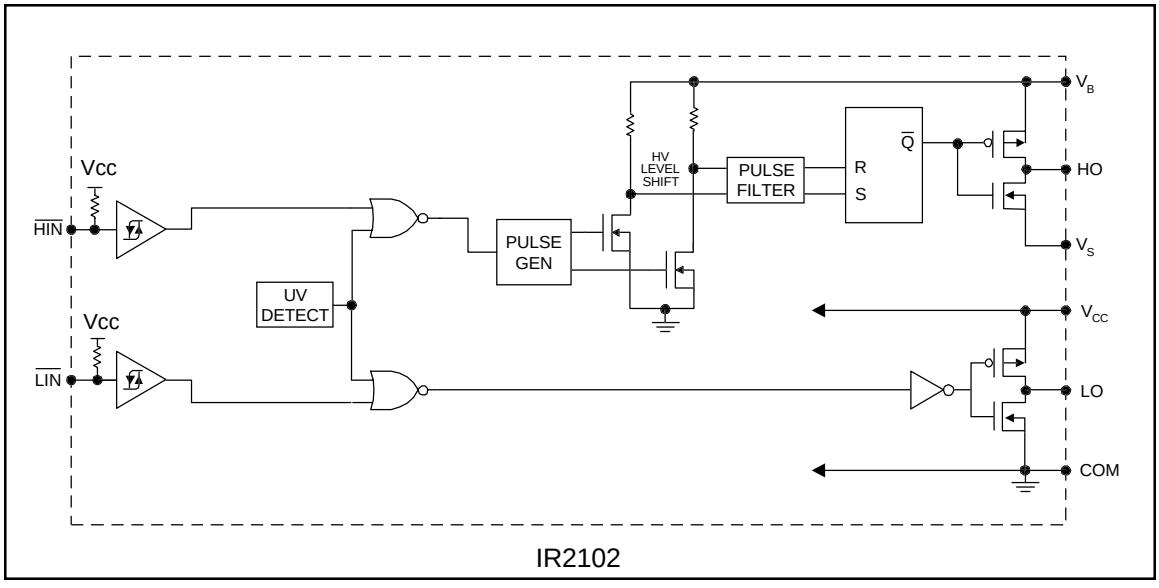
V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” input voltage (IR2101) Logic “0” input voltage (IR2102)	3	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic “0” input voltage (IR2101) Logic “1”input voltage (IR2102)	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	100	mV	I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	100		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	—	30	55		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	—	150	270		V_{IN} = 0V or 5V
I_{IN+}	Logic “1” input bias current	—	3	10		V_{IN} = 5V (IR2101) V_{IN} = 0V (IR2102)
I_{IN-}	Logic “0” input bias current	—	—	1		V_{IN} = 0V (IR2101) V_{IN} = 5V (IR2102)
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8	8.9	9.8	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9		
I_{O+}	Output high short circuit pulsed current	130	210	—	mA	V_O = 0V V_{IN} = Logic “1” PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	270	360	—		V_O = 15V V_{IN} = Logic “0” PW ≤ 10 µs

Functional Block Diagram



IR2101

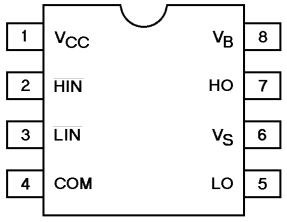


IR2102

Lead Definitions

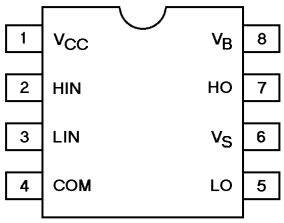
Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase (IR2101)
$\overline{\text{HIN}}$	Logic input for high side gate driver output (HO), out of phase (IR2102)
LIN	Logic input for low side gate driver output (LO), in phase (IR2101)
$\overline{\text{LIN}}$	Logic input for low side gate driver output (LO), out of phase (IR2102)
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



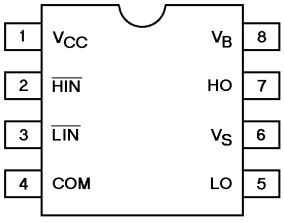
8 Lead PDIP

IR2101



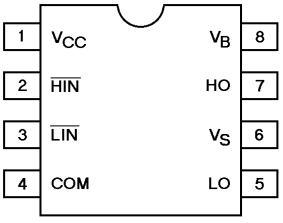
8 Lead SOIC

IR2101S



8 Lead PDIP

IR2102



8 Lead SOIC

IR2102S

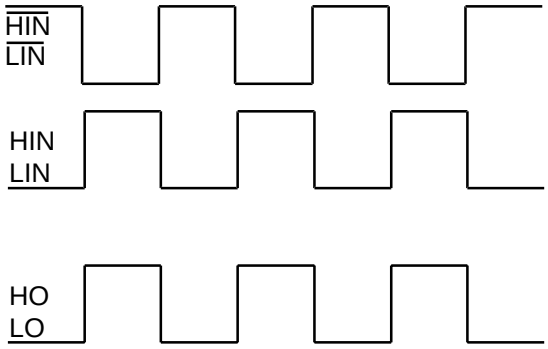


Figure 1. Input/Output Timing Diagram

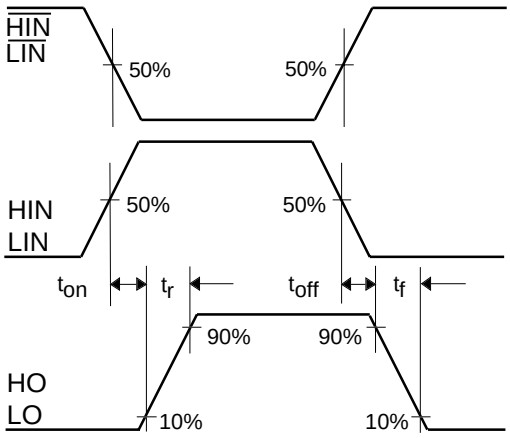


Figure 2. Switching Time Waveform Definitions

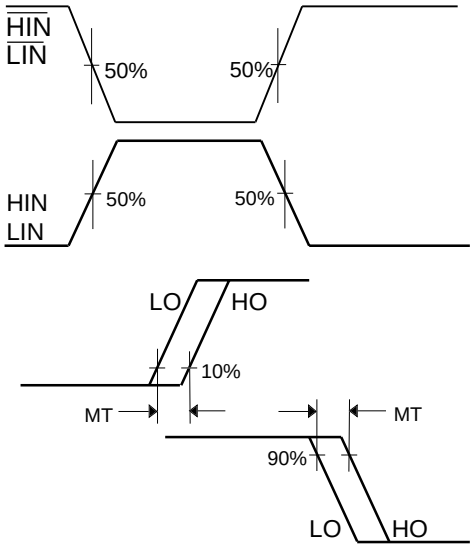


Figure 3. Delay Matching Waveform Definitions

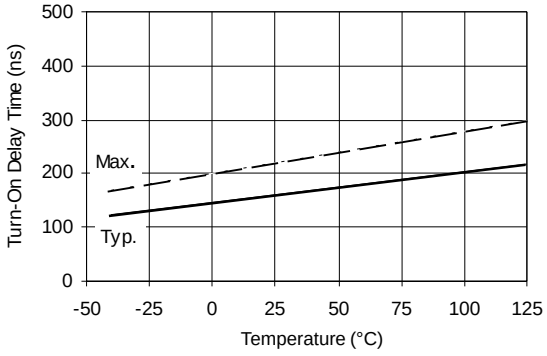


Figure 6A. Turn-On Time vs Temperature

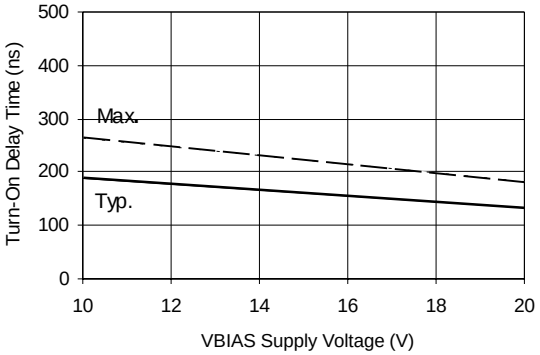


Figure 6B. Turn-On Time vs Supply Voltage

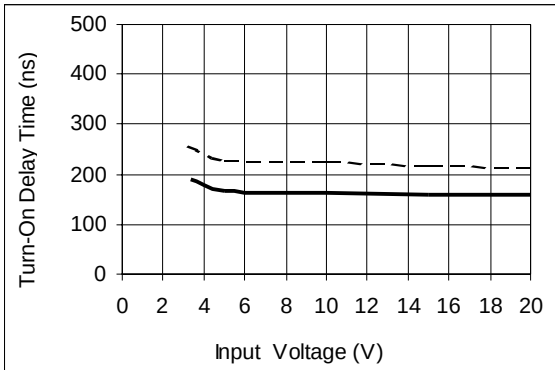


Figure 6C. Turn-On Time vs Input Voltage

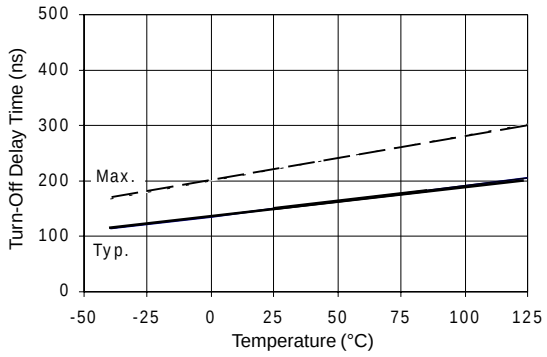


Figure 7A. Turn-Off Time vs Temperature

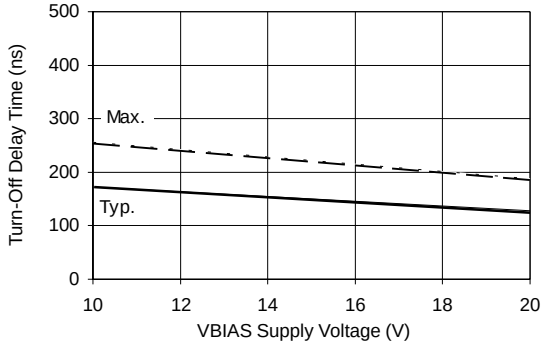


Figure 7B. Turn-Off Time vs Supply Voltage

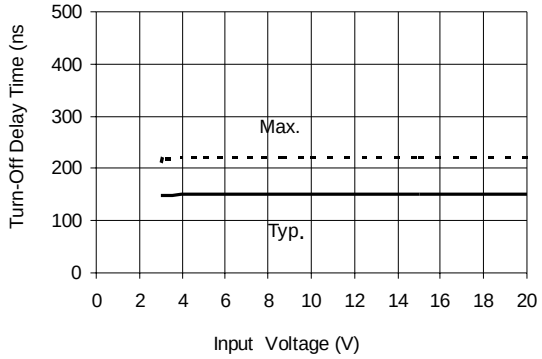


Figure 7C. Turn-Off Time vs Input Voltage

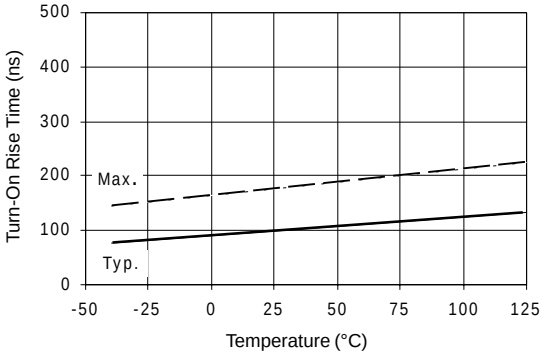


Figure 9A. Turn-On Rise Time vs Temperature

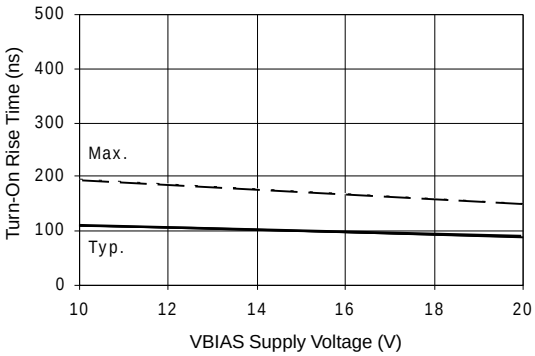


Figure 9B. Turn-On Rise Time vs Voltage

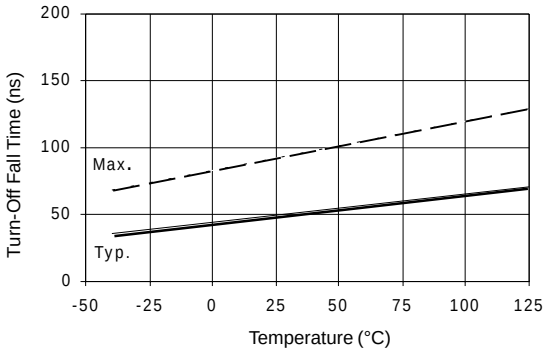


Figure 10A. Turn-Off Fall Time vs Temperature

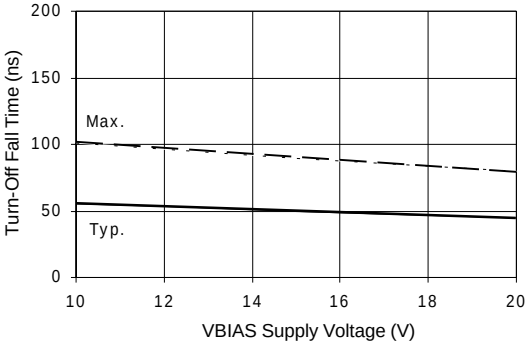


Figure 10B. Turn-Off Fall Time vs Voltage

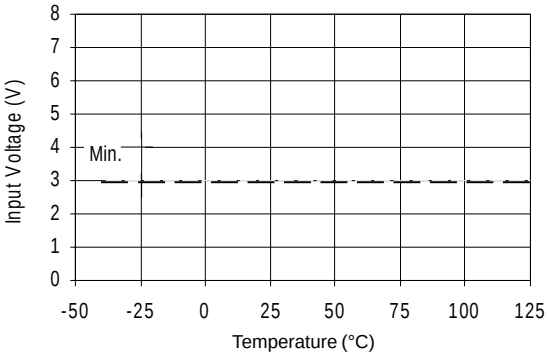


**Figure 12A. Logic "1" Input Voltage (IR2101)
Logic "0" Input Voltage (IR2102)
vs Temperature**

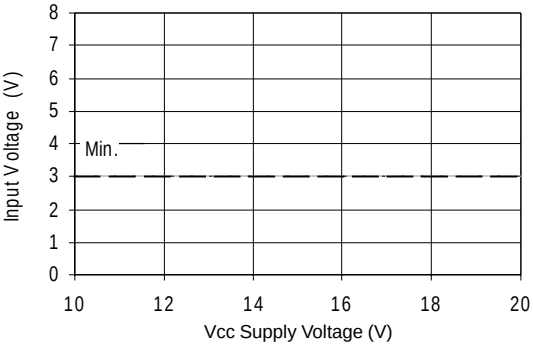


**Figure 12B. Logic "1" Input Voltage (IR2101)
Logic "0" Input Voltage (IR2102)
vs Voltage**

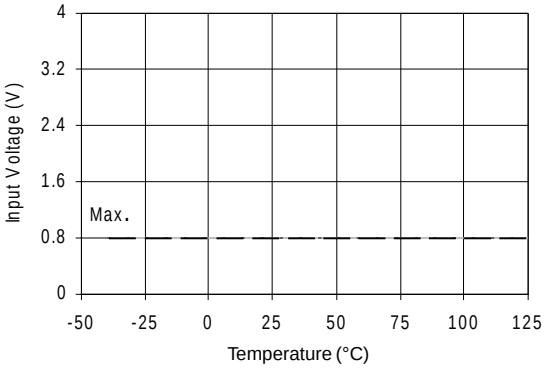


**Figure 13A. Logic "0" Input Voltage (IR2101)
Logic "1" Input Voltage (IR2102)
vs Temperature**

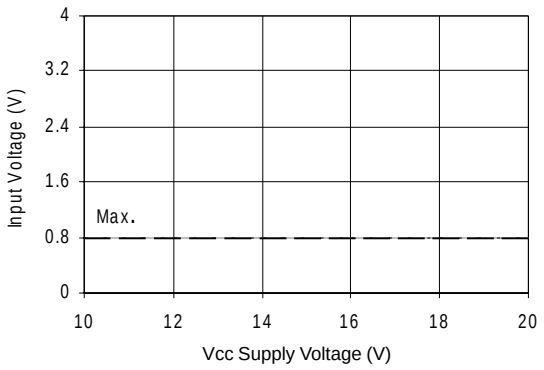


**Figure 13B. Logic "0" Input Voltage (IR2101)
Logic "1" Input Voltage (IR2102)
vs Voltage**

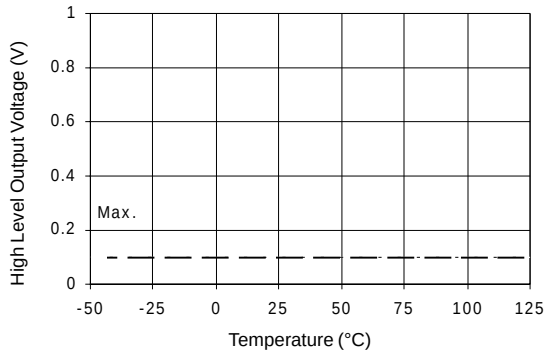


**Figure 14A. High Level Output
vs Temperature**

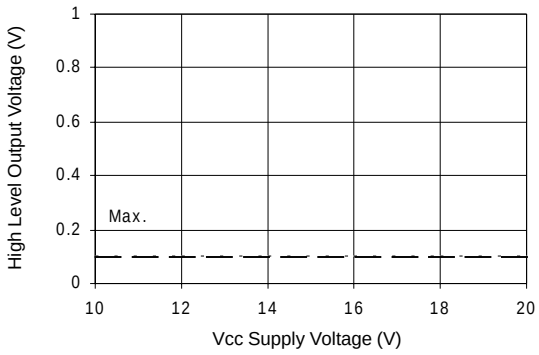


Figure 14B. High Level Output vs Voltage

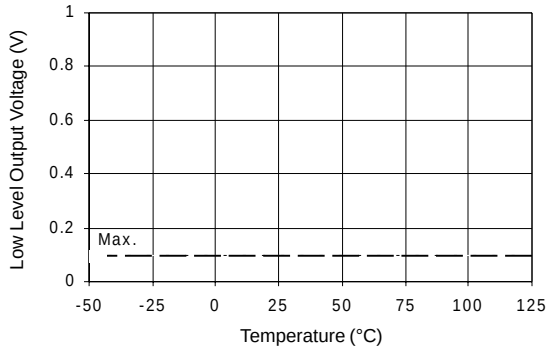


**Figure 15A. Low Level Output
vs Temperature**

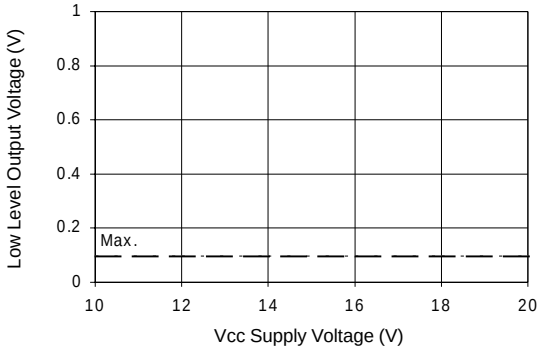


Figure 15B. Low level Output vs Voltage

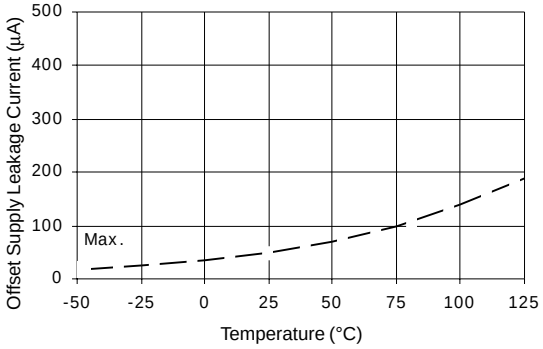


Figure 16A. Offset Supply Current vs Temperature

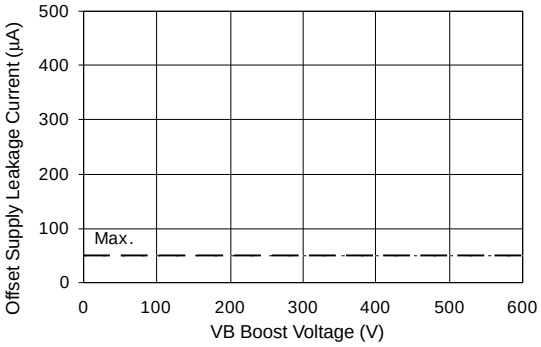


Figure 16B. Offset Supply Current vs Voltage

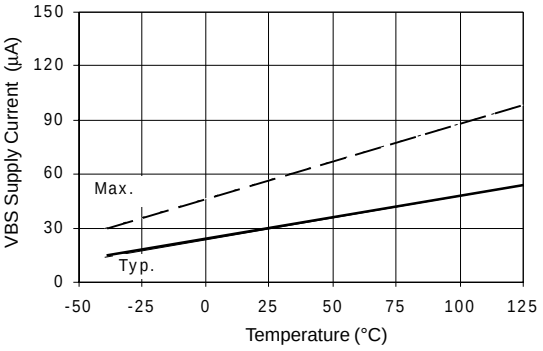


Figure 17A. V_{BS} Supply Current vs Temperature

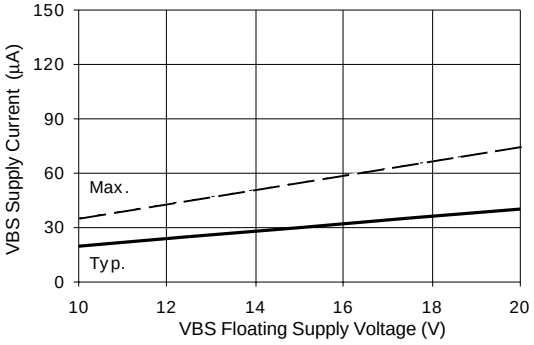


Figure 17B. V_{BS} Supply Current vs Voltage

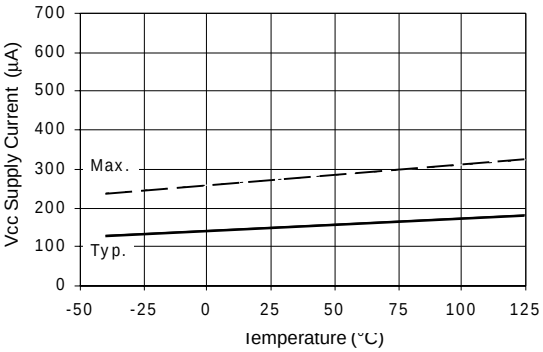


Figure 18A. Vcc Supply Current vs Temperature

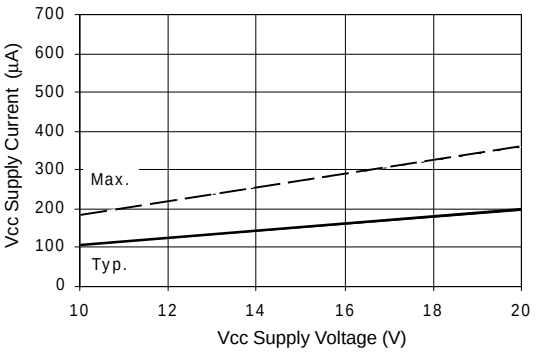


Figure 18B. Vcc Supply Current vs Voltage

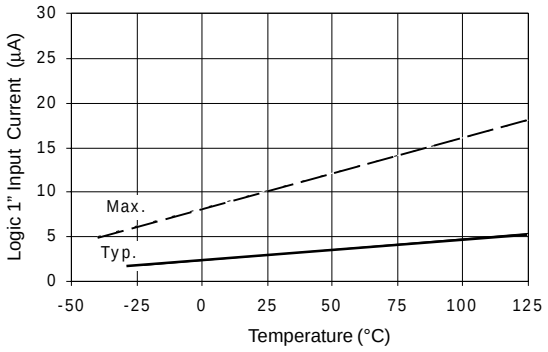


Figure 19A. Logic"1" Input Current vs Temperature

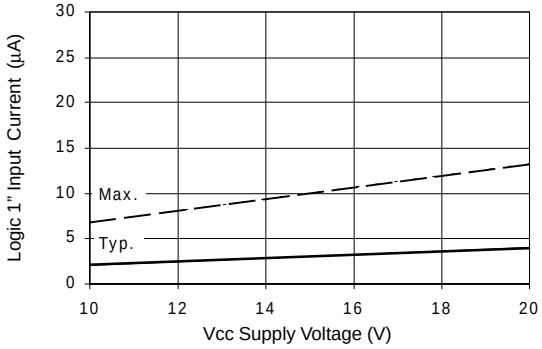


Figure 19B. Logic"1" Input Current vs Voltage

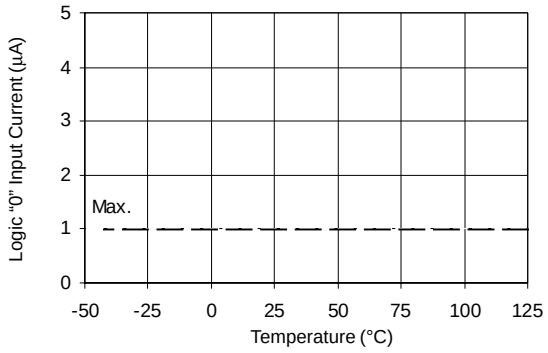


Figure 20A. Logic "0" Input Current vs Temperature

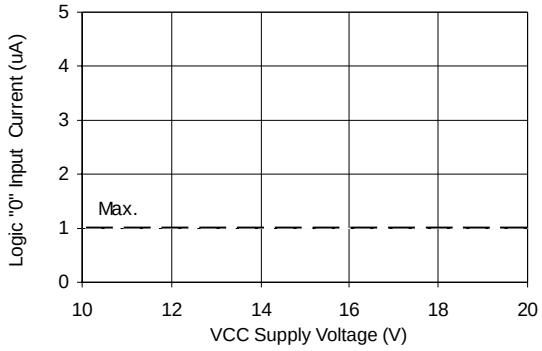


Figure 20B. Logic "0" Input Current vs Voltage

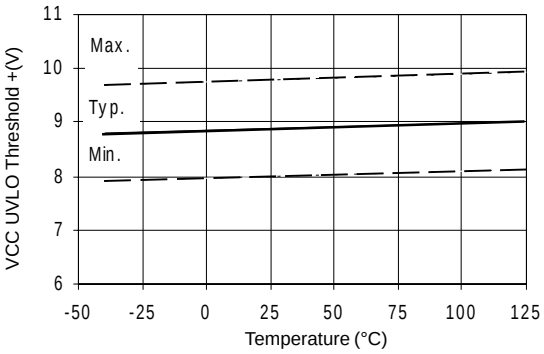


Figure 21A. Vcc Undervoltage Threshold(+) vs Temperature

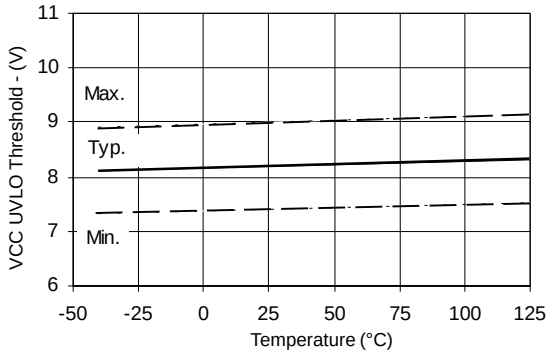


Figure 21B. Vcc Undervoltage Threshold(-) vs Temperature

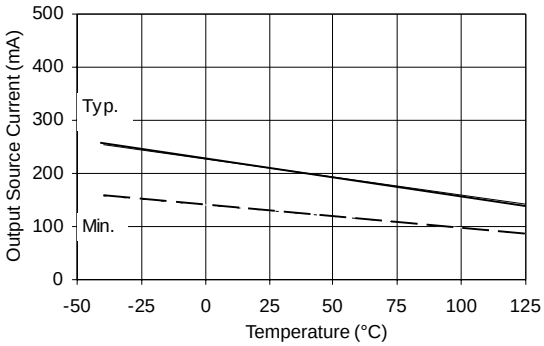


Figure 22A. Output Source Current vs Temperature

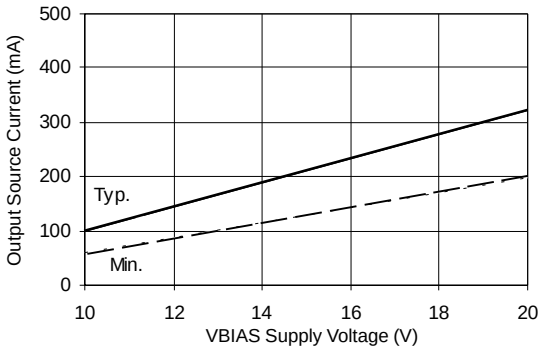


Figure 22B. Output Source Current vs Voltage

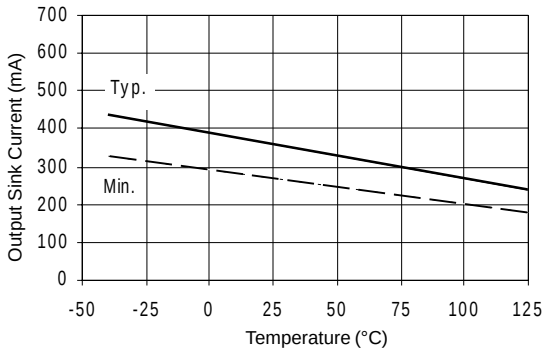


Figure 23A. Output Sink Current vs Temperature

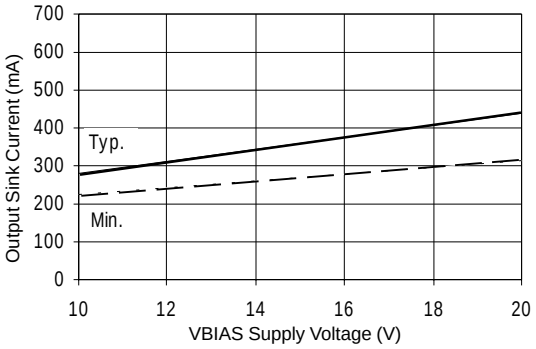
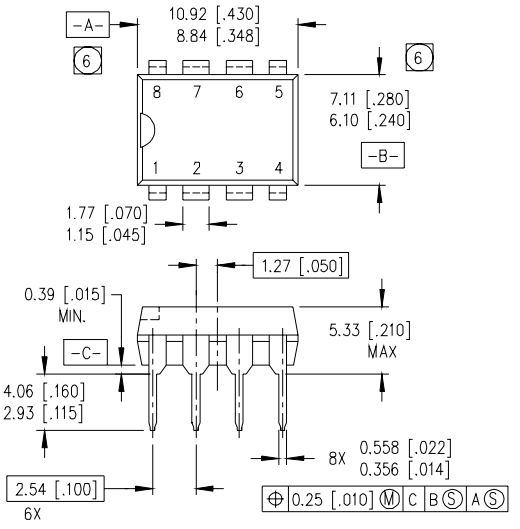


Figure 23B. Output Sink Current vs Voltage

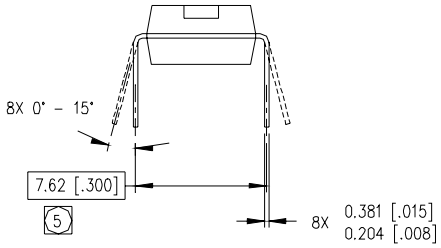
Case outlines



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.

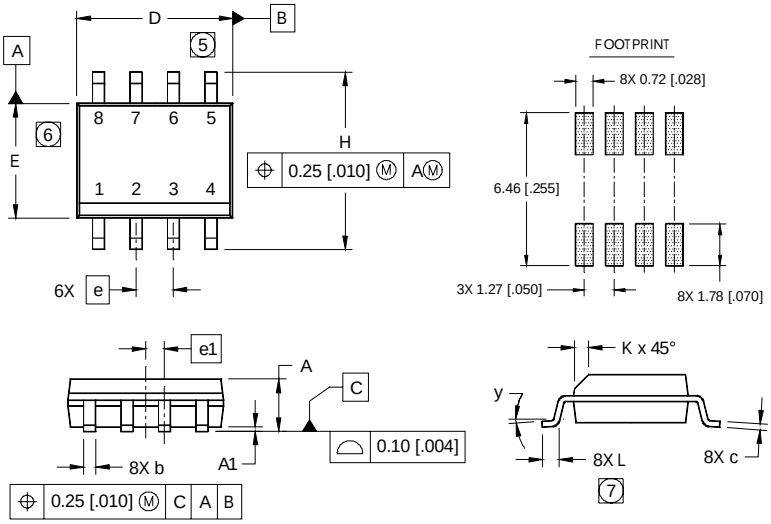
(5) MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8 Lead PDIP

01-6014
01-3003 01 (MS-001AB)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

(5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

(6) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

(7) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

01-6027
01-0021 11 (MS-012AA)

International
IOR Rectifier

Data Sheet No. PD60045-N

IR2103(S)

HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 3.3V, 5V and 15V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- High side output in phase with HIN input
- Low side output out of phase with $\overline{\text{LIN}}$ input

Product Summary

V_{OFFSET}	600V max.
I_O+/-	130 mA / 270 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	680 & 150 ns
Deadtime (typ.)	520 ns

Packages



8-Lead SOIC
IR2103S

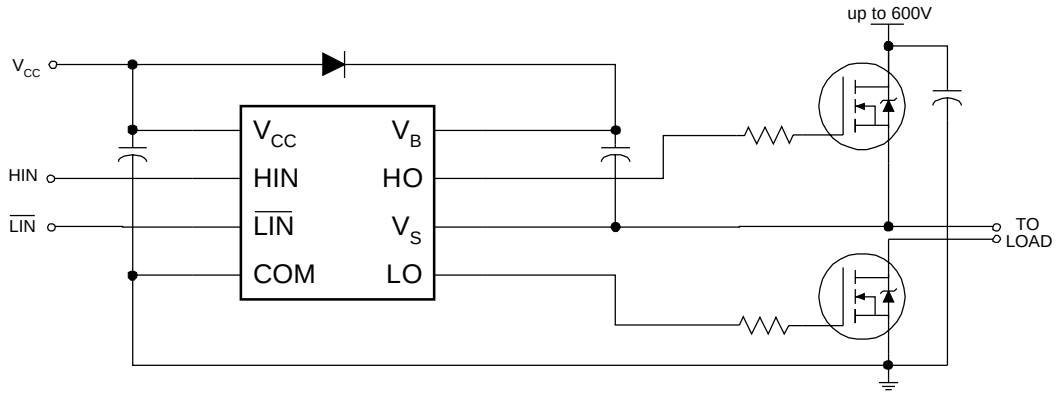


8-Lead PDIP
IR2103

Description

The IR2103(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



(Refer to Lead Assignments for correct configuration). This/These diagram(s) show electrical connections only.
Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 Lead PDIP)	—	1.0	W
		(8 Lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 Lead PDIP)	—	125	°C/W
		(8 Lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

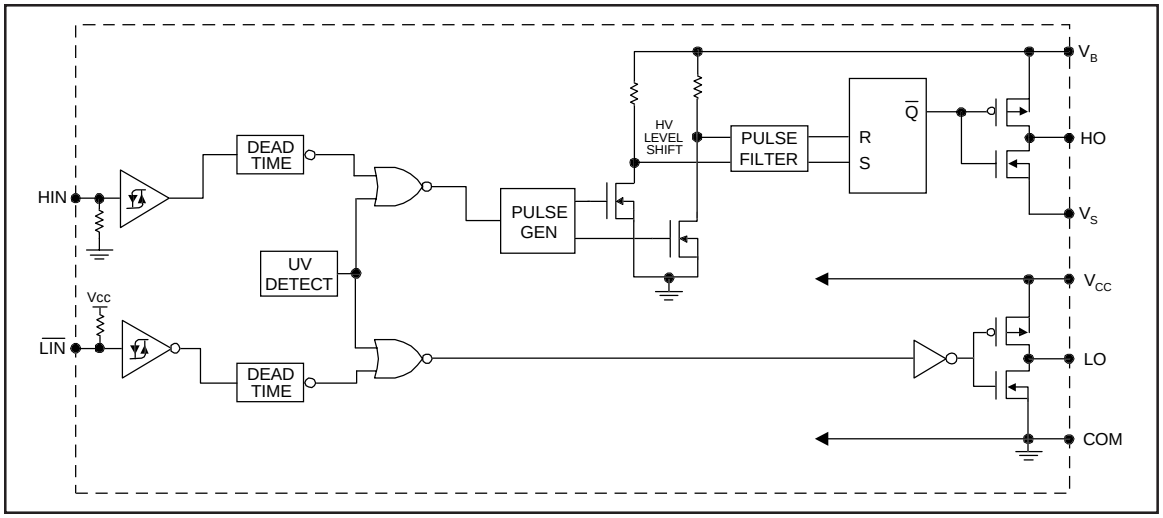
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	680	820	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	150	220		V_S = 600V
t_r	Turn-on rise time	—	100	170		
t_f	Turn-off fall time	—	50	90		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	400	520	650		
MT	Delay matching, HS & LS turn-on/off	—	—	60		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” (HIN) & Logic “0” ($\overline{LIN}$) input voltage	3	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic “0” (HIN) & Logic “1” ($\overline{LIN}$) input voltage	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	100	mV	I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	100		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	—	30	55		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	—	150	270		V_{IN} = 0V or 5V
I_{IN+}	Logic “1” input bias current	—	3	10		HIN = 5V, $\overline{LIN}$ = 0V
I_{IN-}	Logic “0” input bias current	—	—	1		HIN = 0V, $\overline{LIN}$ = 5V
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8	8.9	9.8	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9		
I_{O+}	Output high short circuit pulsed current	130	210	—	mA	V_O = 0V, V_{IN} = V_{IH} PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	270	360	—		V_O = 15V, V_{IN} = V_{IL} PW ≤ 10 µs

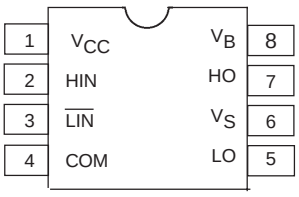
Functional Block Diagram



Lead Definitions

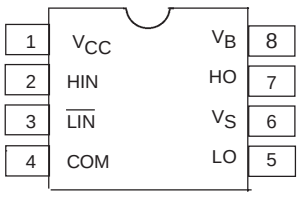
Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
$\overline{LIN}$	Logic input for low side gate driver output (LO), out of phase
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



8 Lead PDIP

IR2103



8 Lead SOIC

IR2103S

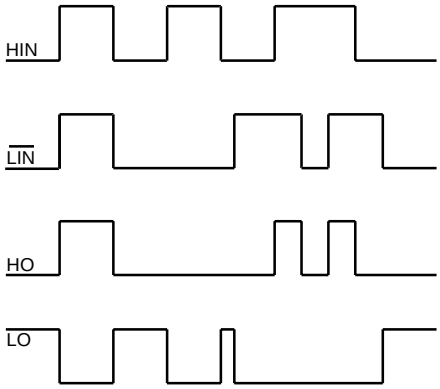


Figure 1. Input/Output Timing Diagram

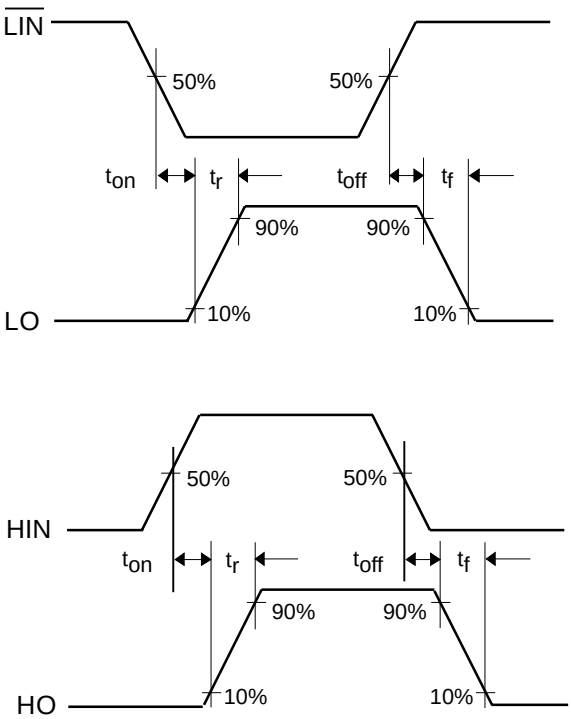


Figure 2. Switching Time Waveform Definitions

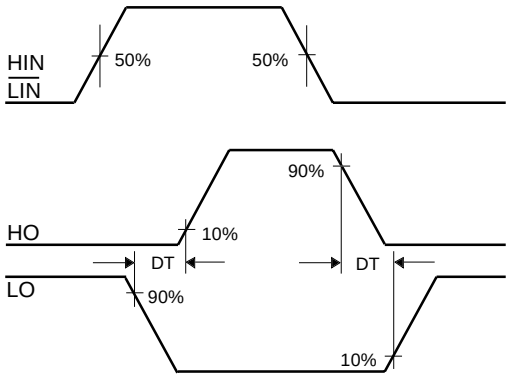


Figure 4. Deadtime Waveform Definitions

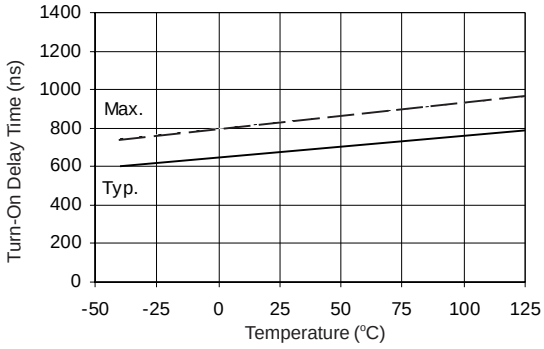


Figure 6A. Turn-On Time vs Temperature

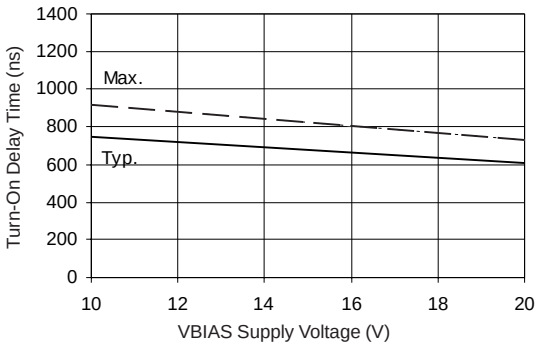


Figure 6B. Turn-On Time vs Supply Voltage

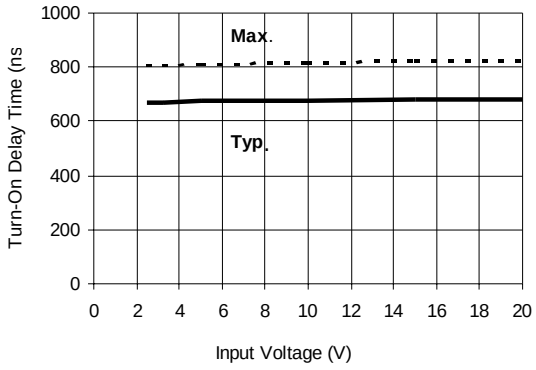


Figure 6C. Turn-On Time vs Input Voltage

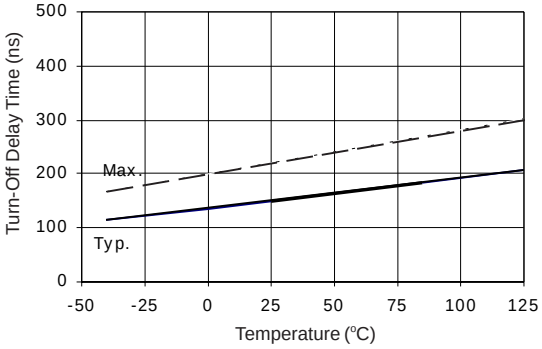


Figure 7A. Turn-Off Time vs Temperature

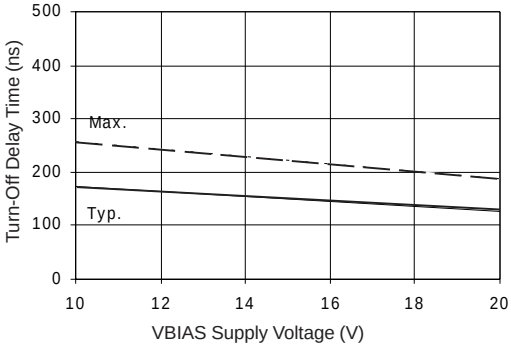


Figure 7B. Turn-Off Time vs Supply Voltage

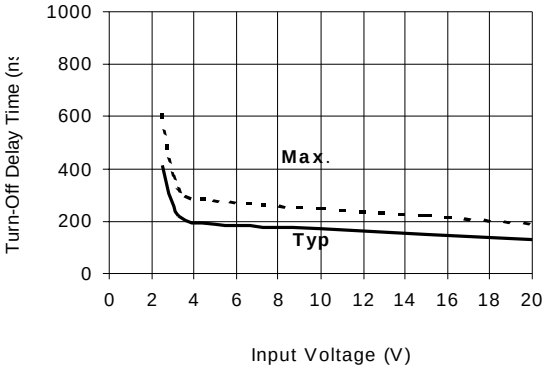


Figure 7C. Turn-Off Time vs Input Voltage

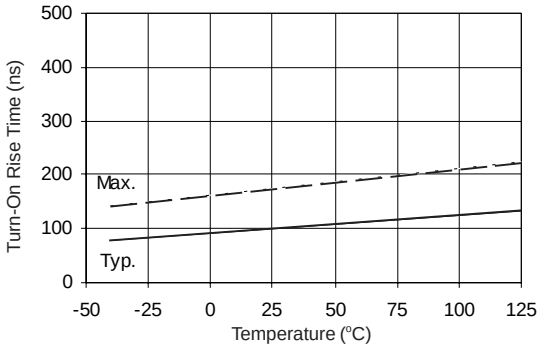


Figure 9A. Turn-On Rise Time vs Temperature

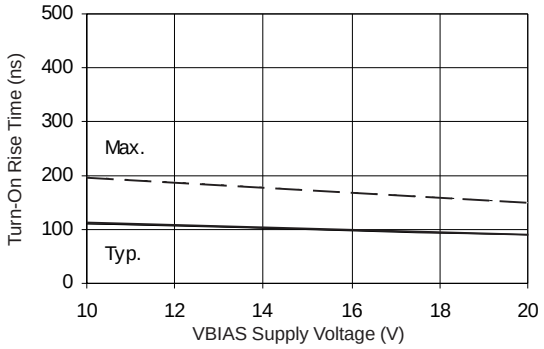


Figure 9B. Turn-On Rise Time vs Voltage

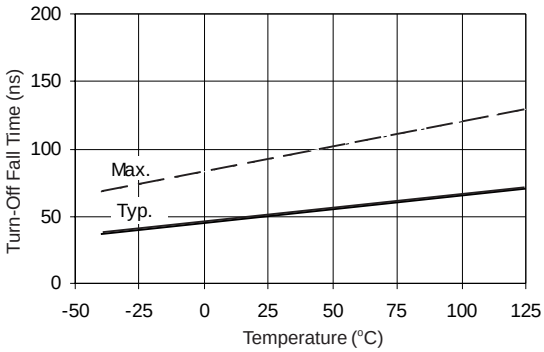


Figure 10A. Turn Off Fall Time vs Temperature

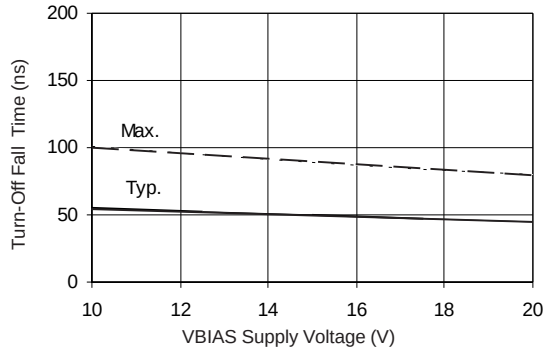


Figure 10B. Turn Off Fall Time vs Voltage

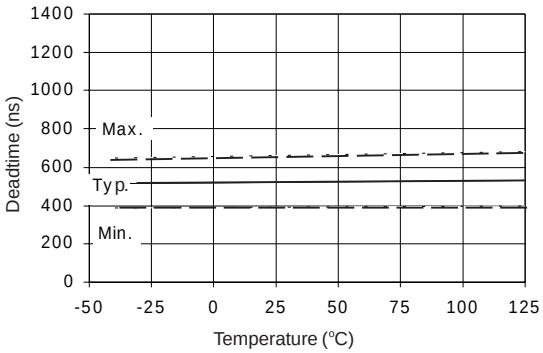


Figure 11A. Deadtime vs Temperature

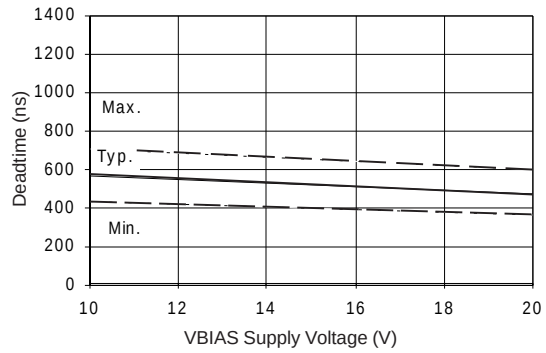


Figure 11B. Deadtime vs Voltage

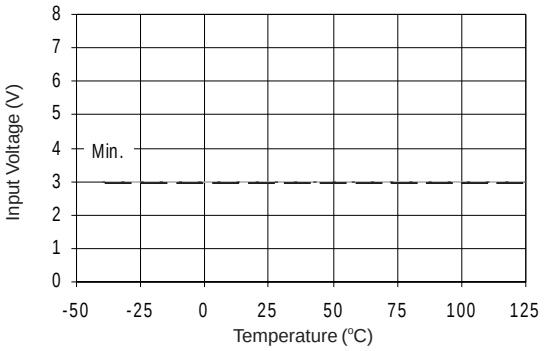


Figure12A. Logic "1" ($\overline{HIN}$) & Logic "0" ($\overline{LIN}$) Input Voltage vs Temperature

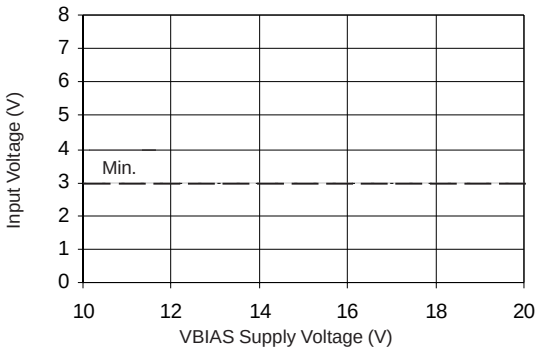


Figure 12B. Logic "1" ($\overline{HIN}$) & Logic "0" ($\overline{LIN}$) Input Voltage vs Voltage

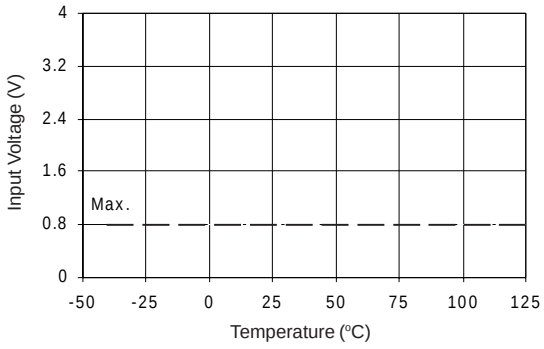


Figure 13A. Logic "0"($\overline{HIN}$) & Logic "1"($\overline{LIN}$) Input Voltage vs Temperature

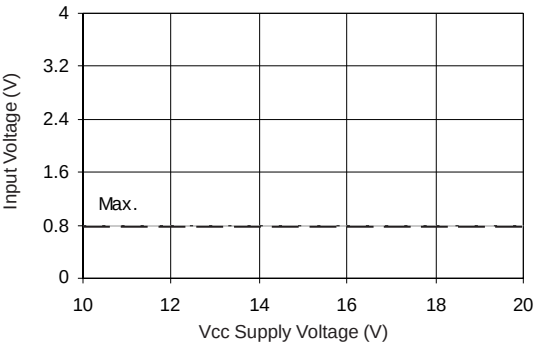


Figure 13B. Logic "0"(HIN) & Logic "1"(LIN) Input Voltage vs Voltage

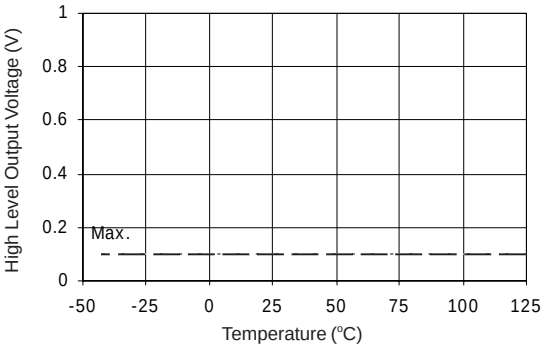


Figure 14A. High Level Output vs Temperature

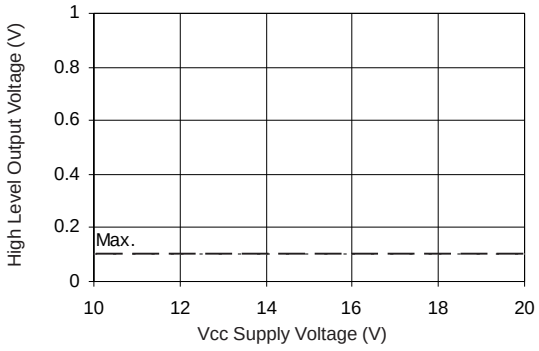


Figure 14B. High Level Output vs Voltage

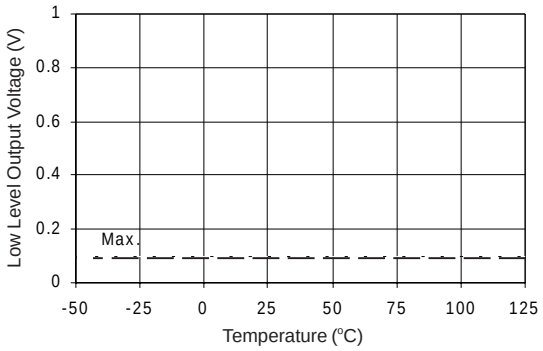


Figure 15A. Low Level Output vs Temperature

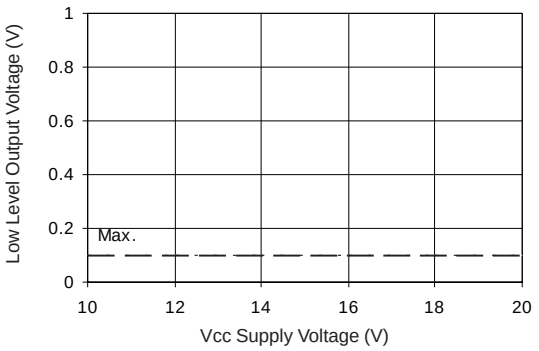


Figure 15B. Low Level Output vs Voltage

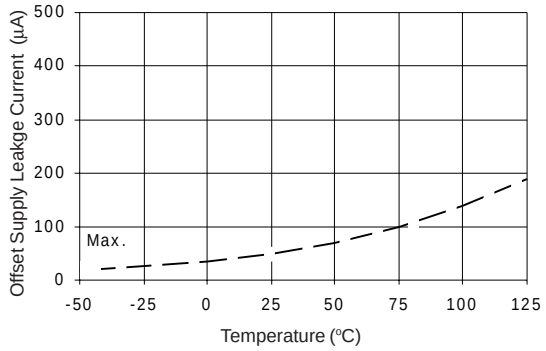


Figure 16A. Offset Supply Current vs Temperature

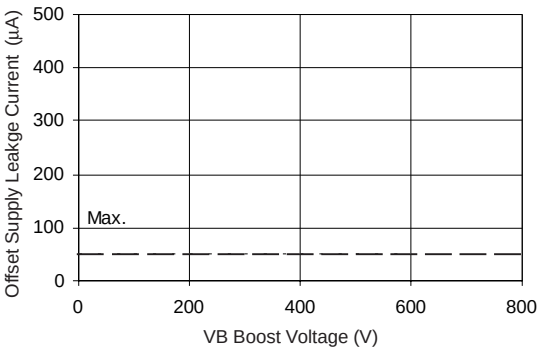


Figure 16B. Offset Supply Current vs Voltage

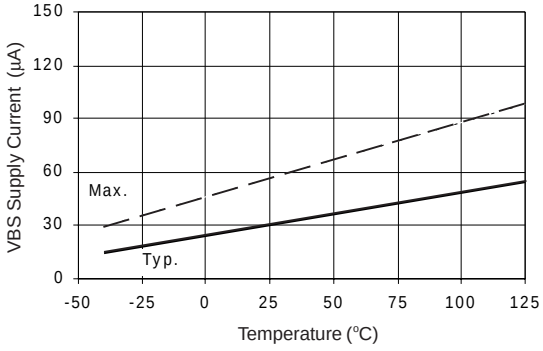


Figure 17A. VBS Supply Current vs Temperature

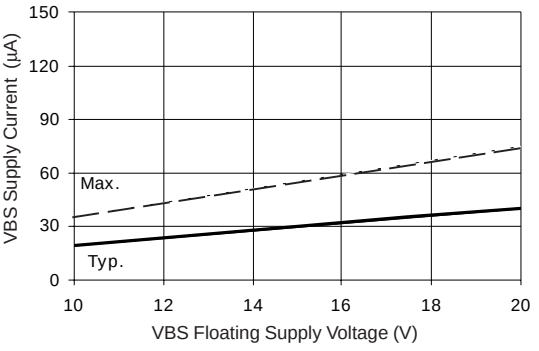


Figure 17B. VBS Supply Current vs Voltage

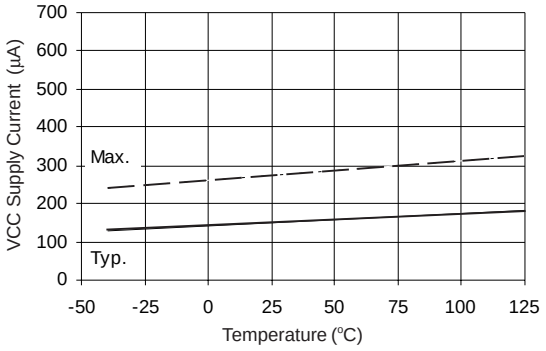


Figure 18A. Vcc Supply Current vs Temperature

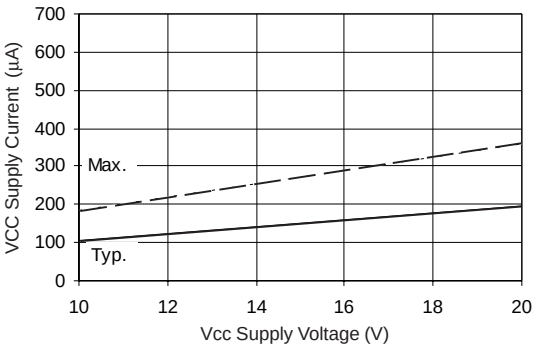


Figure 18B. Vcc Supply Current vs Voltage

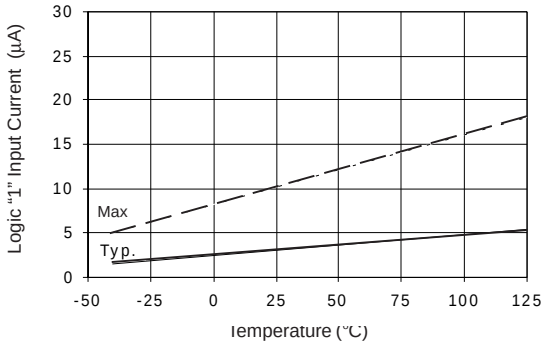


Figure 19A. Logic "1" Input Current vs Temperature

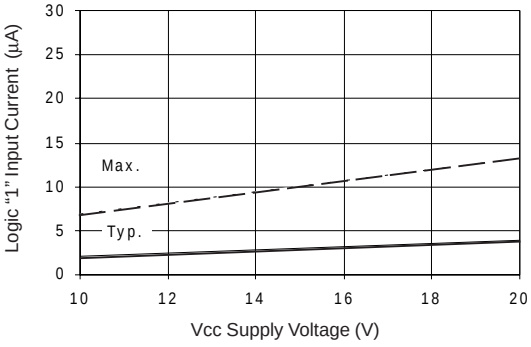


Figure 19B. Logic "1" Input Current vs Voltage

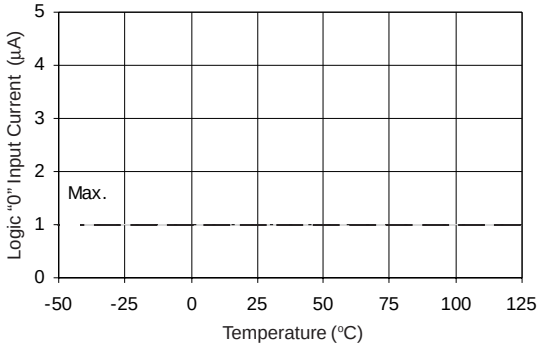


Figure 20A. Logic "0" Input Current vs Temperature

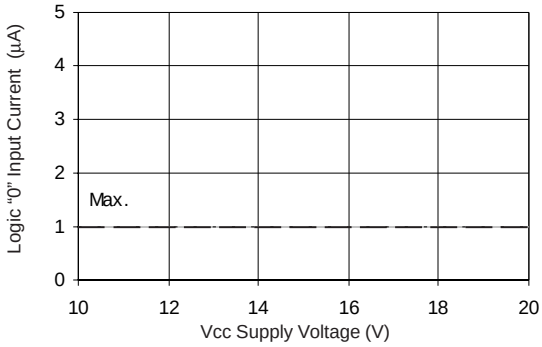


Figure 20B. Logic "0" Input Current vs Voltage

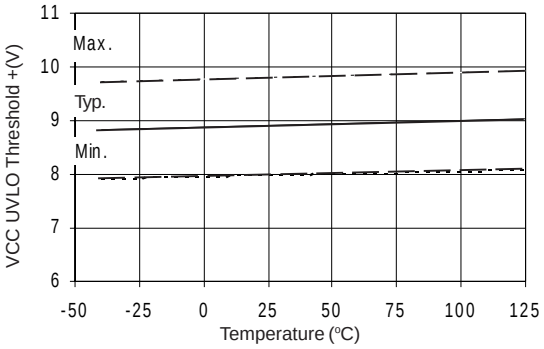


Figure 21A. Vcc Undervoltage Threshold(+) vs Temperature

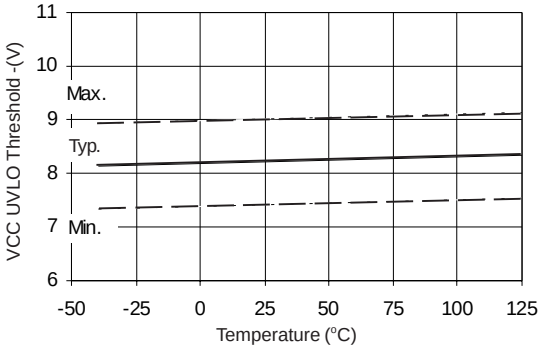


Figure 21B. Vcc UndervoltageThreshold (-) vs Temperature

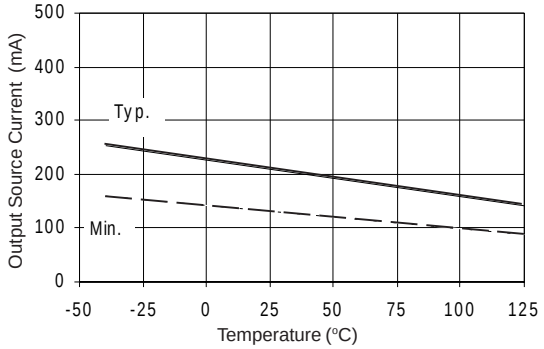


Figure 22A. Output Source Current vs Temperature

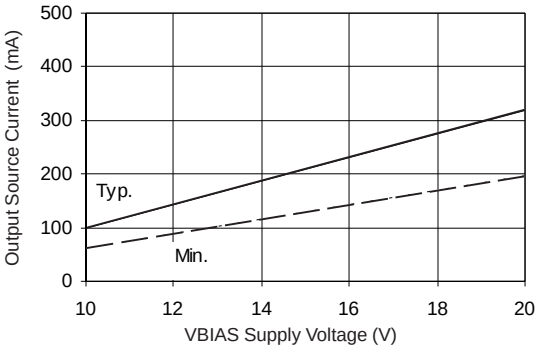


Figure 22B. Output Source Current vs Voltage

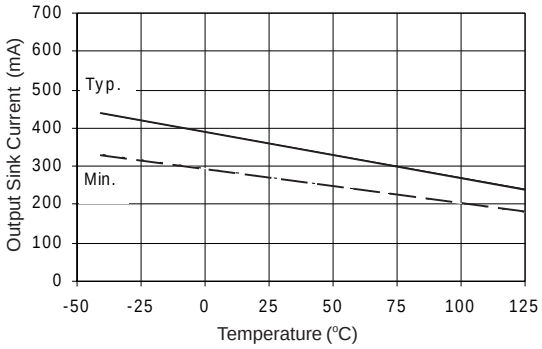


Figure 23A. Output Sink Current vs Temperature

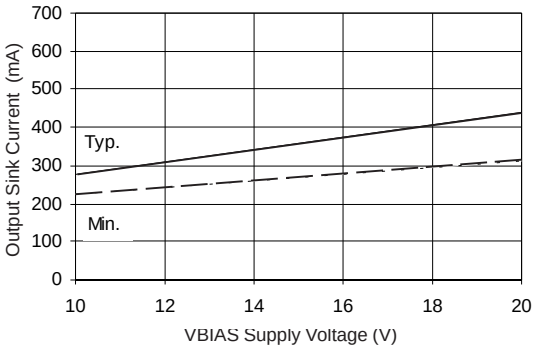
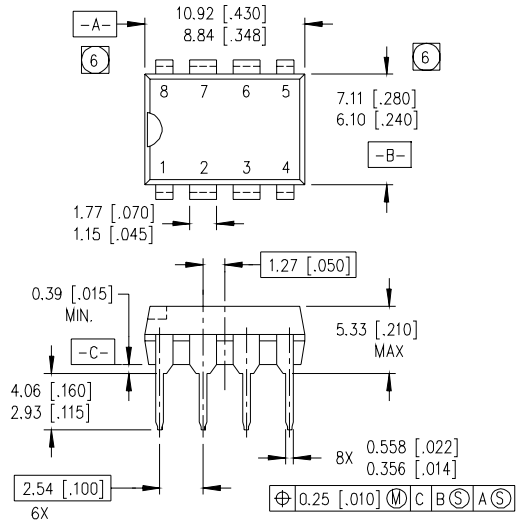
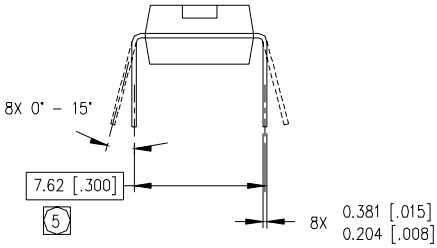


Figure 23B. Output Sink Current vs Voltage

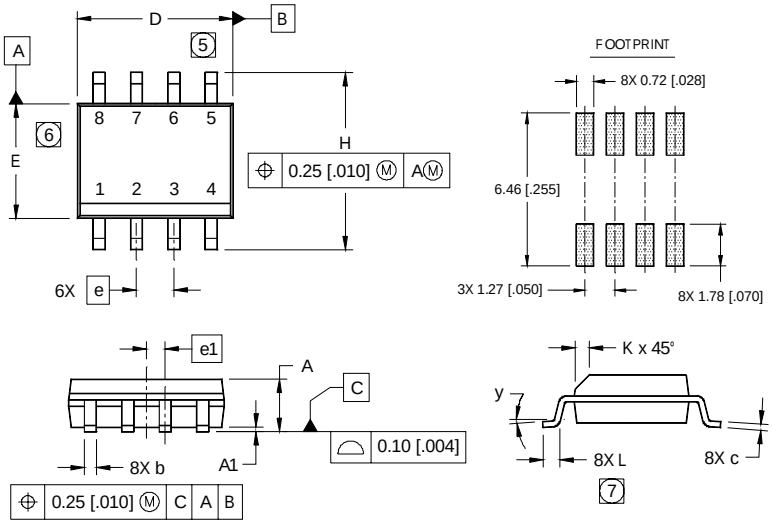


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8-Lead PDIP

01-6014
01-3003 01 (MS-001AB)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8-Lead SOIC

01-6027
01-0021 11 (MS-012AA)

International
IOR Rectifier

Data Sheet No. PD60046-P

IR2104(S)

HALF-BRIDGE DRIVER

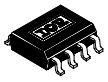
Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Internally set deadtime
- High side output in phase with input
- Shut down input turns off both channels
- Matched propagation delay for both channels

Product Summary

V_{OFFSET}	600V max.
I_O+/-	130 mA / 270 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	680 & 150 ns
Deadtime (typ.)	520 ns

Packages



8 Lead SOIC
IR2104S

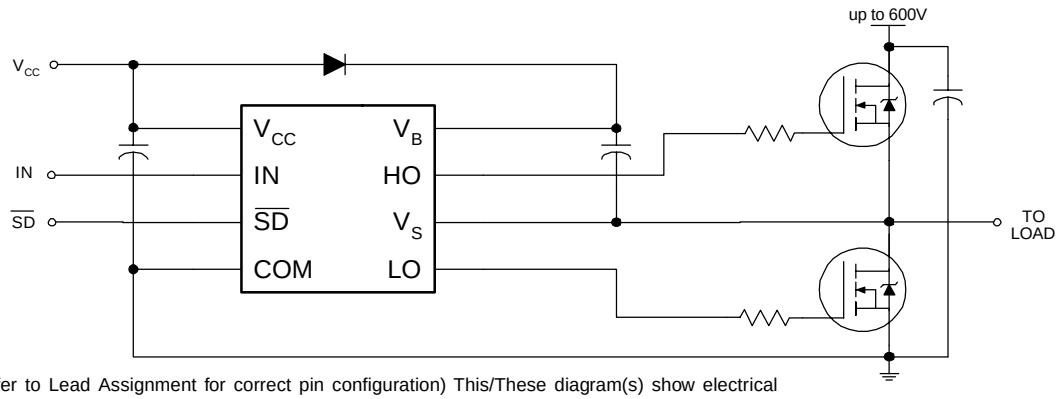


8 Lead PDIP
IR2104

Description

The IR2104(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates from 10 to 600 volts.

Typical Connection



(Refer to Lead Assignment for correct pin configuration) This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

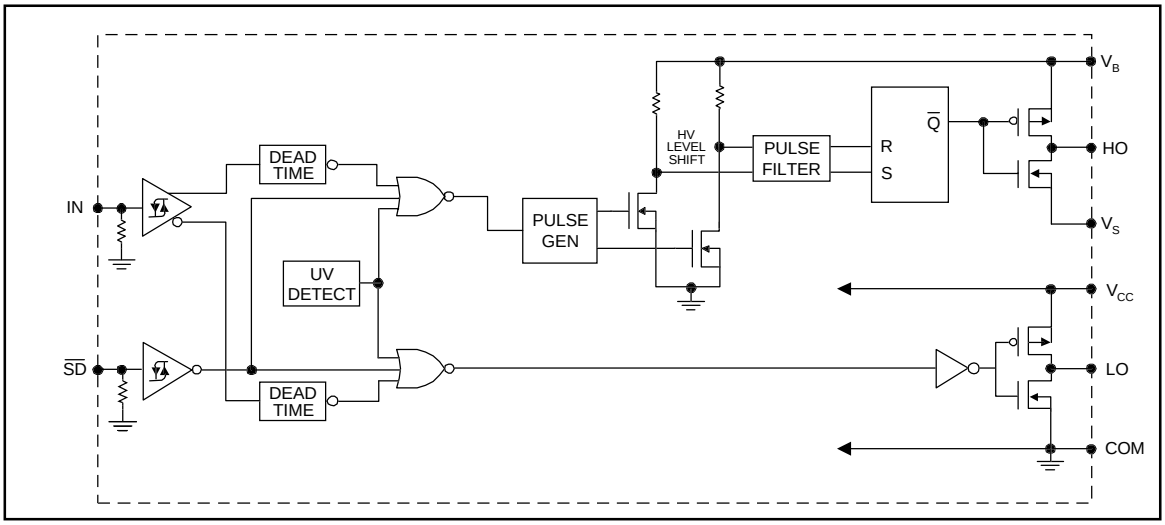
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	680	820	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	150	220		V_S = 600V
t_{sd}	Shutdown propagation delay	—	160	220		
t_r	Turn-on rise time	—	100	170		
t_f	Turn-off fall time	—	50	90		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	400	520	650		
MT	Delay matching, HS & LS turn-on/off	—	—	60		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” (HO) & Logic “0” (LO) input voltage	3	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic “0” (HO) & Logic “1” (LO) input voltage	—	—	0.8		V_{CC} = 10V to 20V
$V_{SD,TH+}$	SD input positive going threshold	3	—	—		V_{CC} = 10V to 20V
$V_{SD,TH-}$	SD input negative going threshold	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	100	mV	I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	100		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	—	30	55		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	—	150	270		V_{IN} = 0V or 5V
I_{IN+}	Logic “1” input bias current	—	3	10		V_{IN} = 5V
I_{IN-}	Logic “0” input bias current	—	—	1		V_{IN} = 0V
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8	8.9	9.8	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9		
I_{O+}	Output high short circuit pulsed current	130	210	—	mA	V_O = 0V PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	270	360	—		V_O = 15V PW ≤ 10 µs

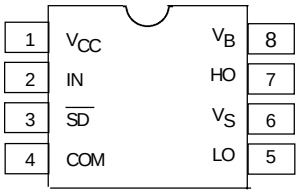
Functional Block Diagram



Lead Definitions

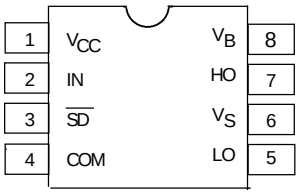
Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO
$\overline{SD}$	Logic input for shutdown
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



8 Lead PDIP

IR2104



8 Lead SOIC

IR2104S

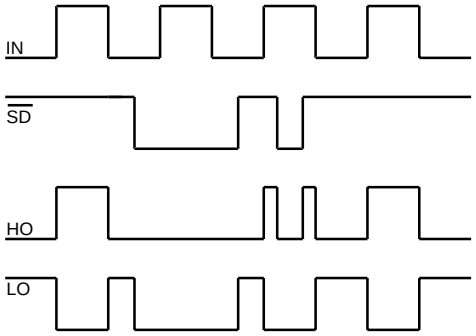


Figure 1. Input/Output Timing Diagram

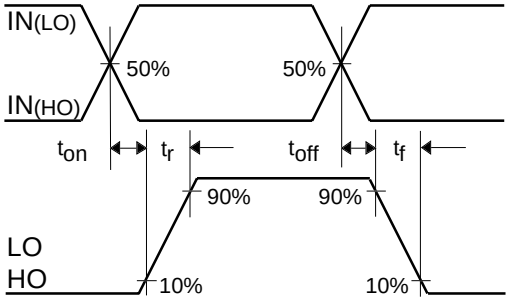


Figure 2. Switching Time Waveform Definitions

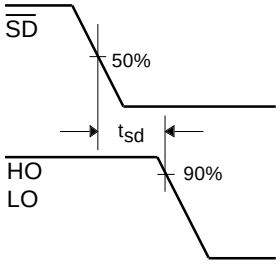


Figure 3. Shutdown Waveform Definitions

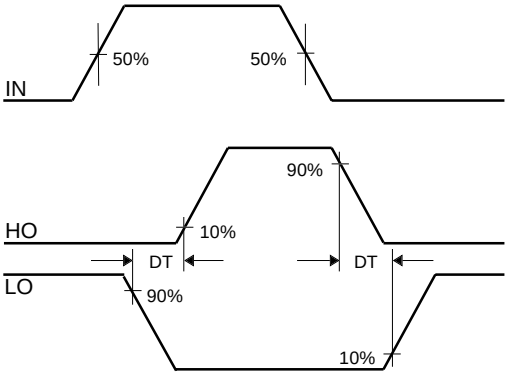


Figure 4. Deadtime Waveform Definitions

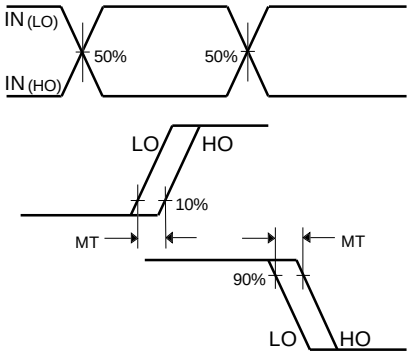


Figure 5. Delay Matching Waveform Definitions

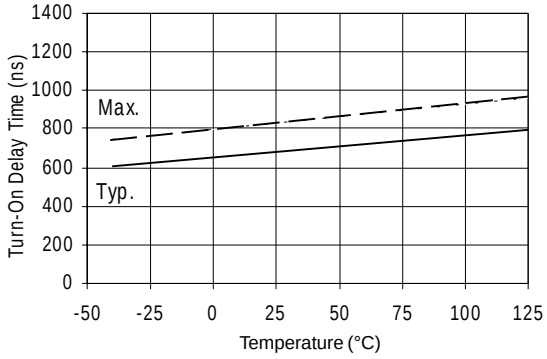


Figure 6A. Turn-On Time vs Temperature

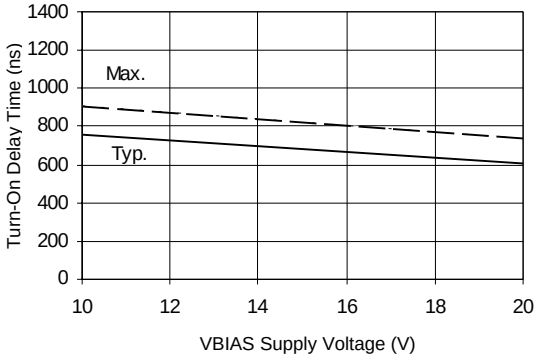


Figure 6B. Turn-On Time vs Supply Voltage

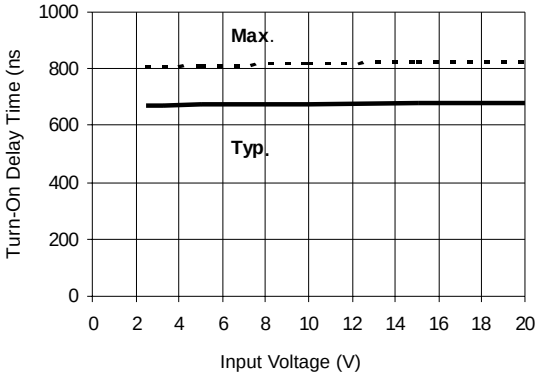


Figure 6C. Turn-On Time vs Input Voltage

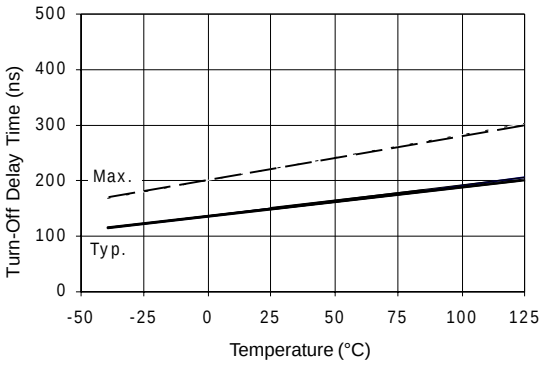


Figure 7A. Turn-Off Time vs Temperature

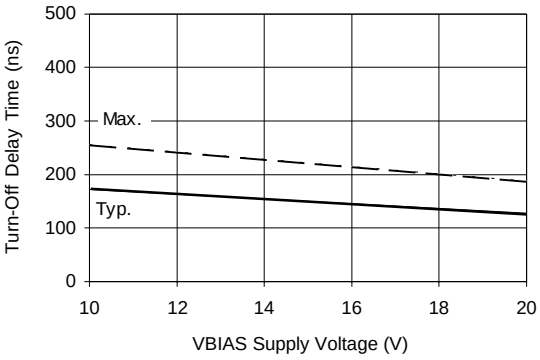


Figure 7B. Turn-Off Time vs Supply Voltage

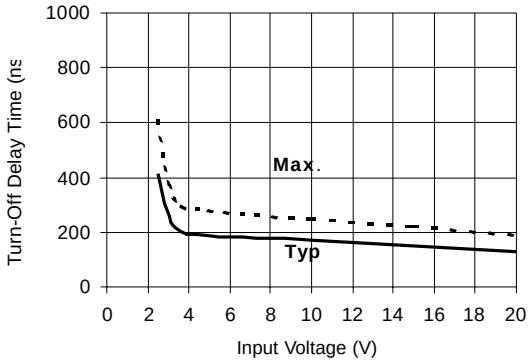


Figure 7C. Turn-Off Time vs Input Voltage

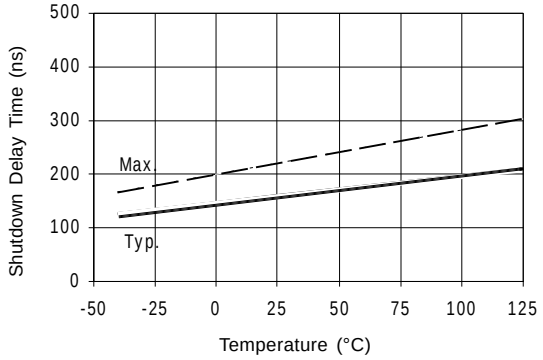


Figure 8A. Shutdown Time vs Temperature

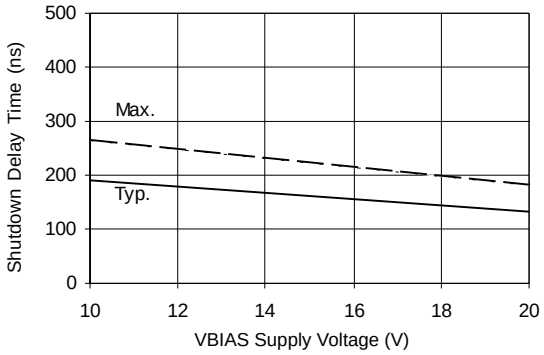


Figure 8B. Shutdown Time vs Voltage

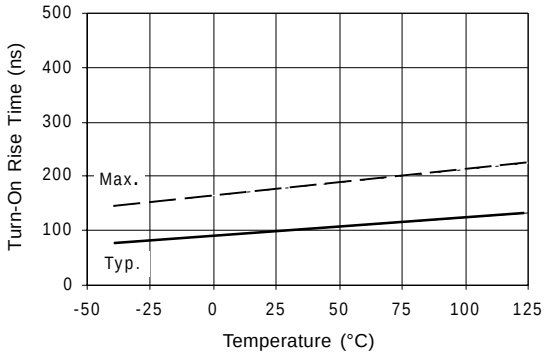


Figure 9A. Turn-On Rise Time vs Temperature

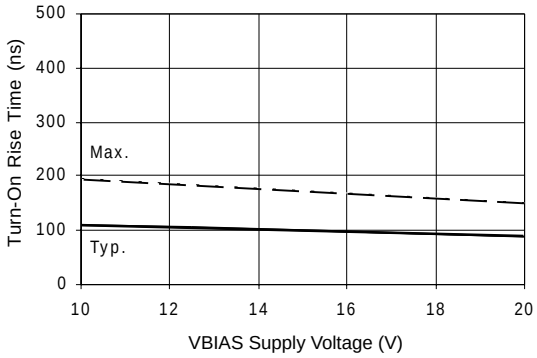


Figure 9B. Turn-On Rise Time vs Voltage

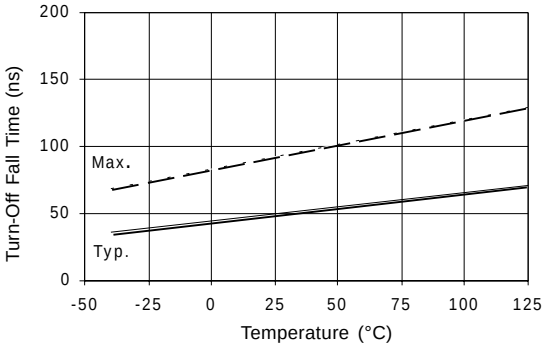


Figure 10A. Turn-Off Fall Time vs Temperature

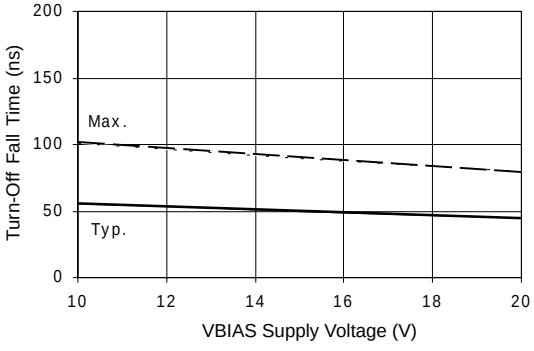


Figure 10B. Turn-Off Fall Time vs Voltage

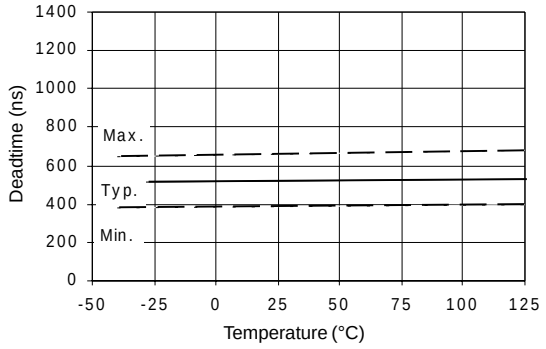


Figure 11A. Deadtime vs Temperature

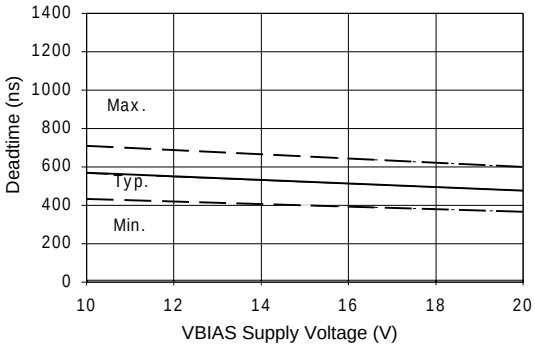


Figure 11B. Deadtime vs Voltage

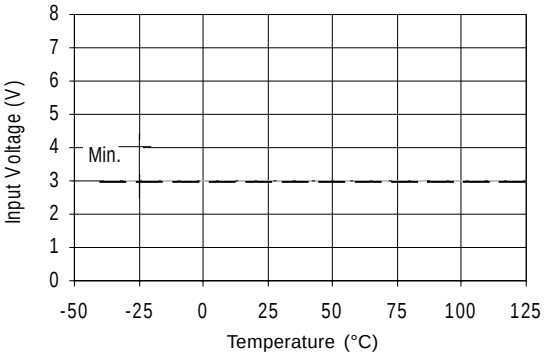


Figure 12A. Logic "1" (HO) & Logic “0” (LO) & Inactive SD Input Voltage vs Temperature

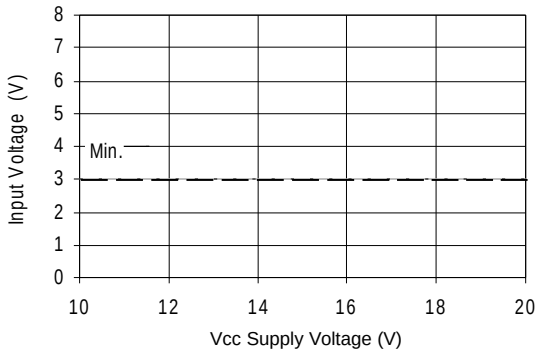


Figure 12B. Logic "1" (HO) & Logic “0” (LO) & Inactive SD Input Voltage vs Voltage

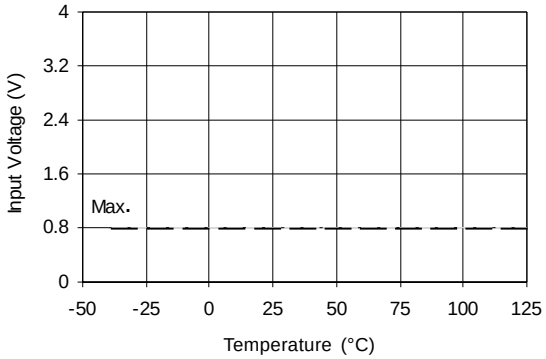


Figure 13A. Logic "0" (HO) & Logic “1” (LO) & Active SD Input Voltage vs Temperature

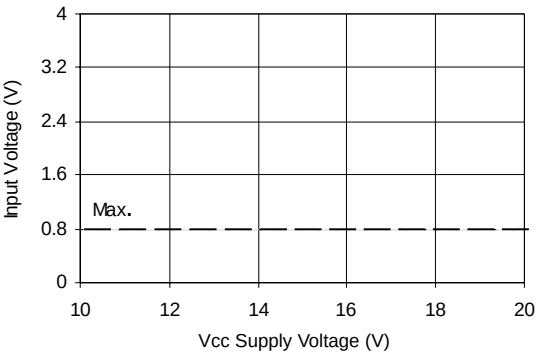


Figure 13B. Logic "0" (HO) & Logic “1” (LO) & Active SD Input Voltage vs Voltage

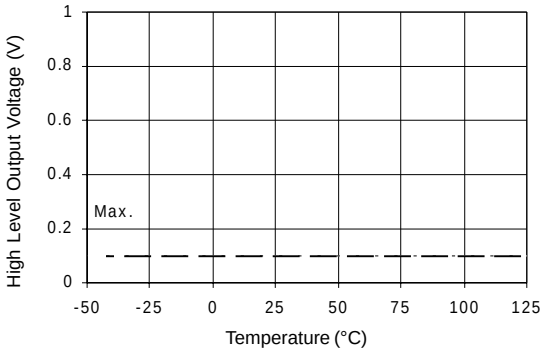


Figure 14A. High Level Output vs Temperature

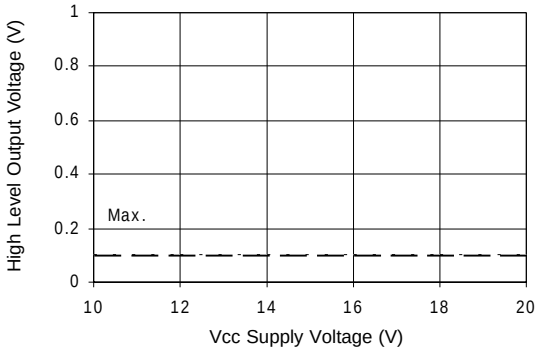


Figure 14B. High Level Output vs Voltage

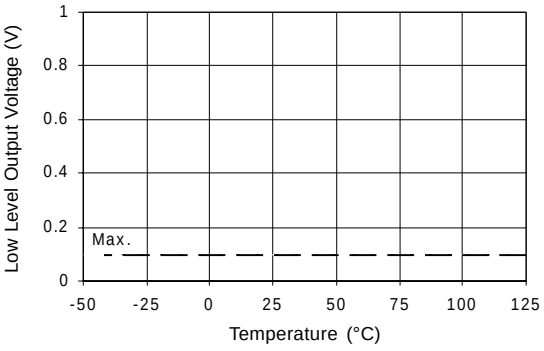


Figure 15A. Low Level Output vs Temperature

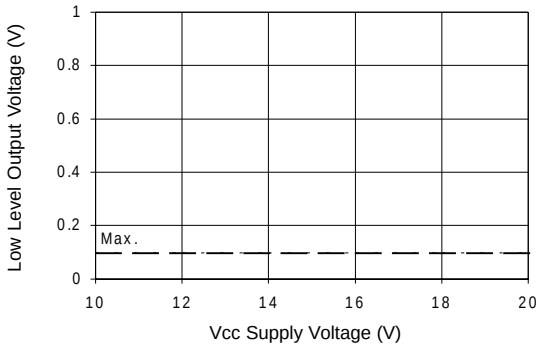


Figure 15B. Low level Output vs Voltage

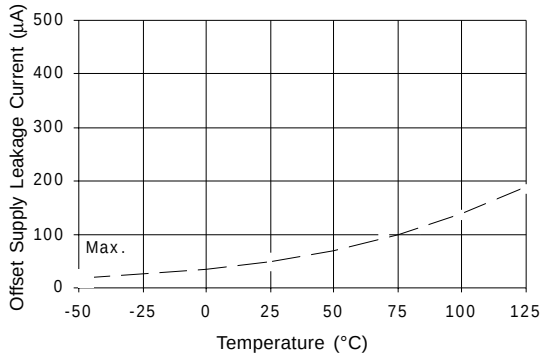


Figure 16A. Offset Supply Current vs Temperature

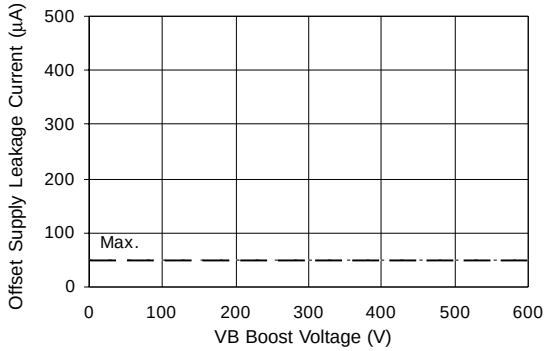


Figure 16B. Offset Supply Current vs Voltage

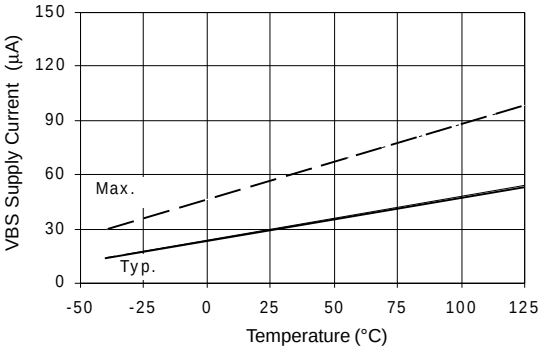


Figure 17A. V_{BS} Supply Current vs Temperature

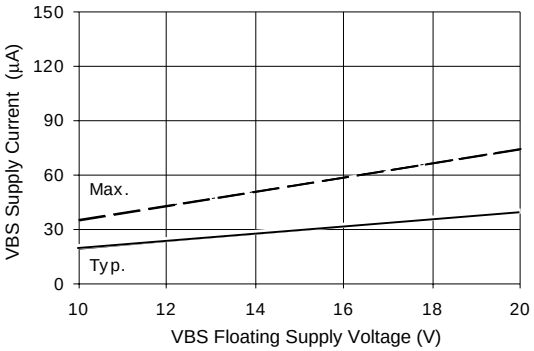


Figure 17B. V_{BS} Supply Current vs Voltage

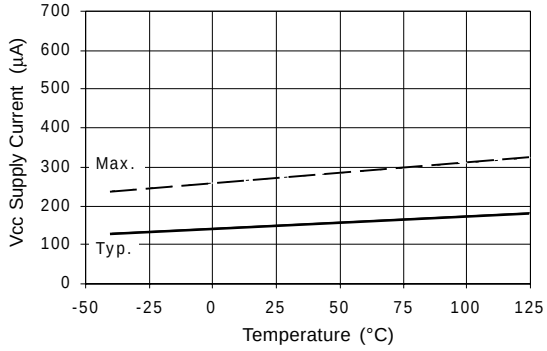


Figure 18A. Vcc Supply Current vs Temperature

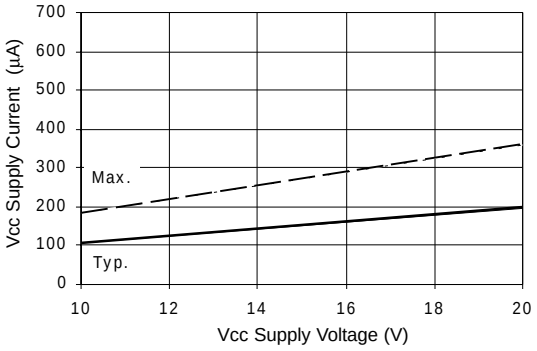


Figure 18B. Vcc Supply Current vs Voltage

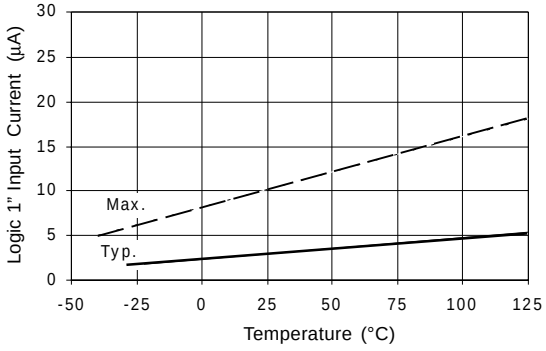


Figure 19A. Logic"1" Input Current vs Temperature

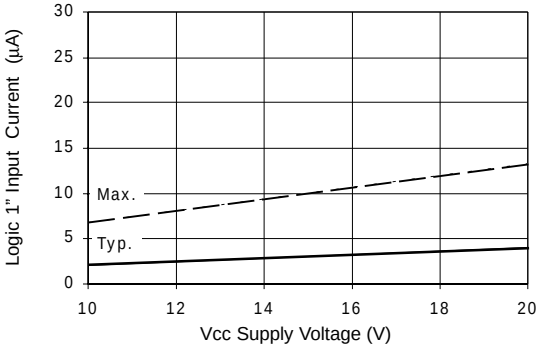


Figure 19B. Logic"1" Input Current vs Voltage

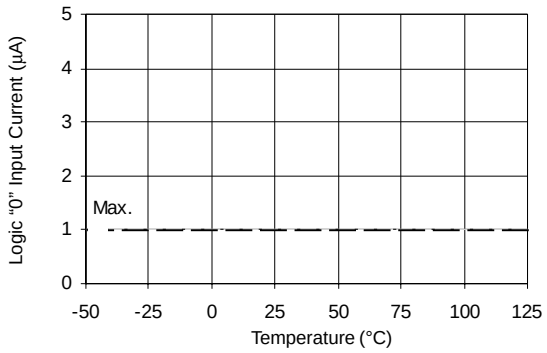


Figure 20A. Logic "0" Input Current vs Temperature

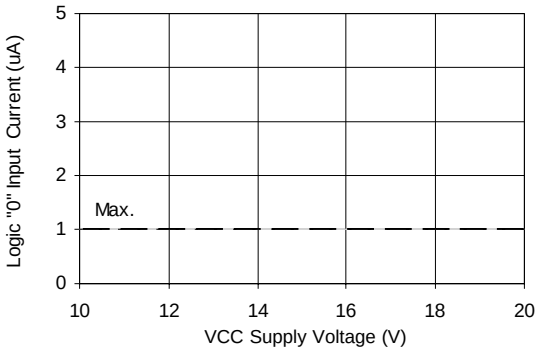


Figure 20B. Logic "0" Input Current vs Voltage

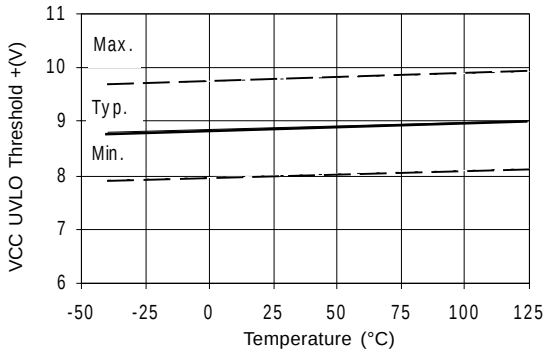


Figure 21A. Vcc Undervoltage Threshold(+) vs Temperature

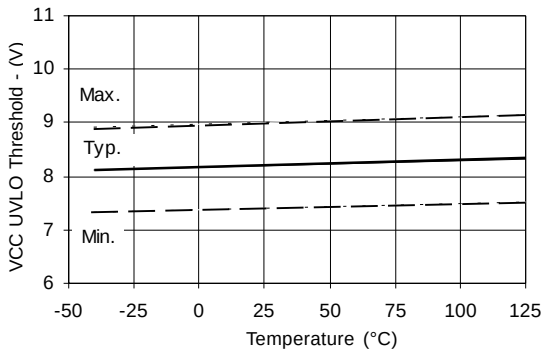


Figure 21B. Vcc Undervoltage Threshold(-) vs Temperature

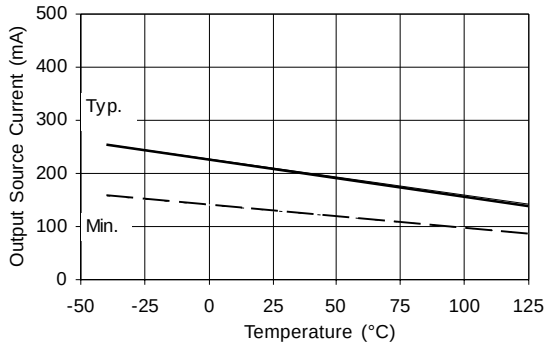


Figure 22A. Output Source Current vs Temperature

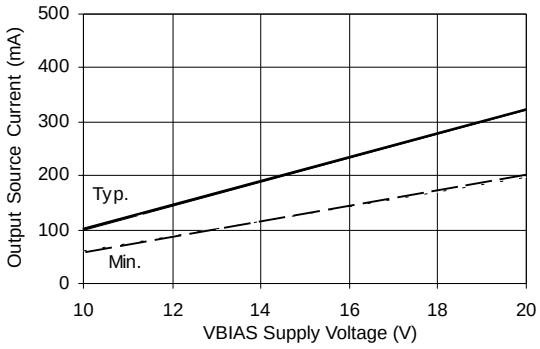


Figure 22B. Output Source Current vs Voltage

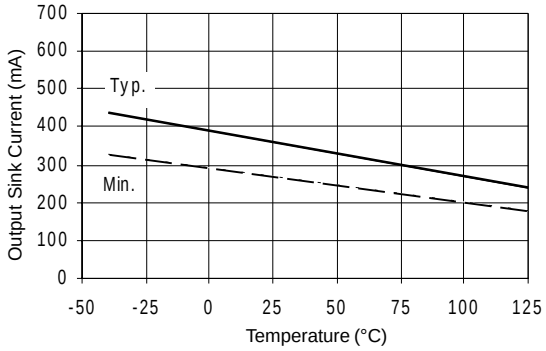


Figure 23A. Output Sink Current vs Temperature

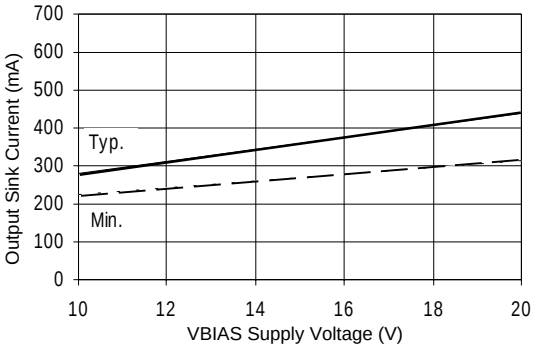
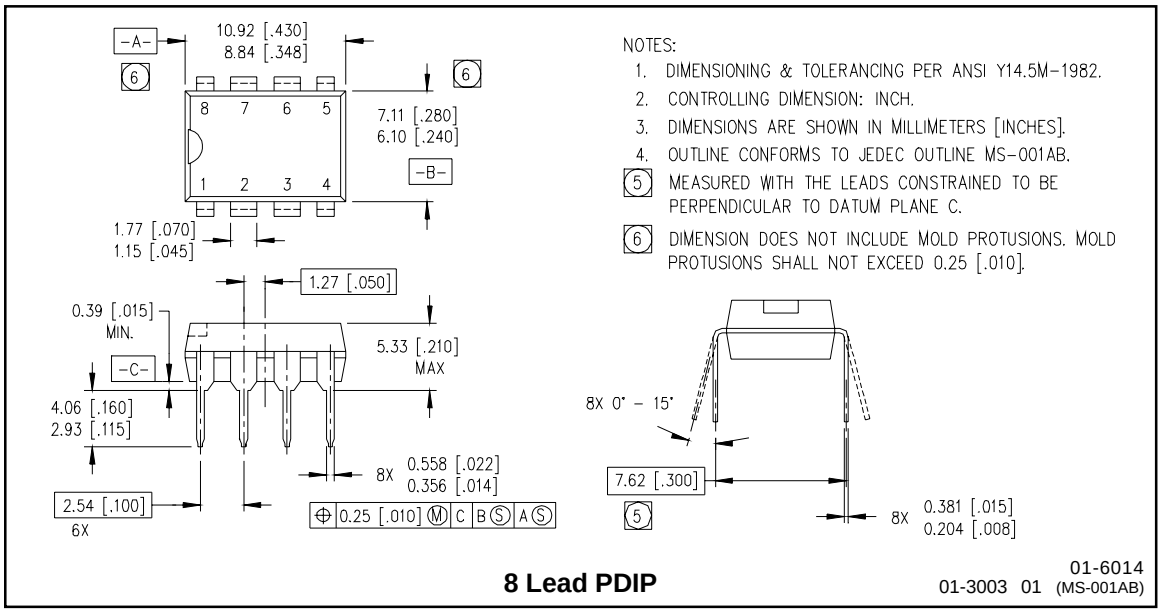
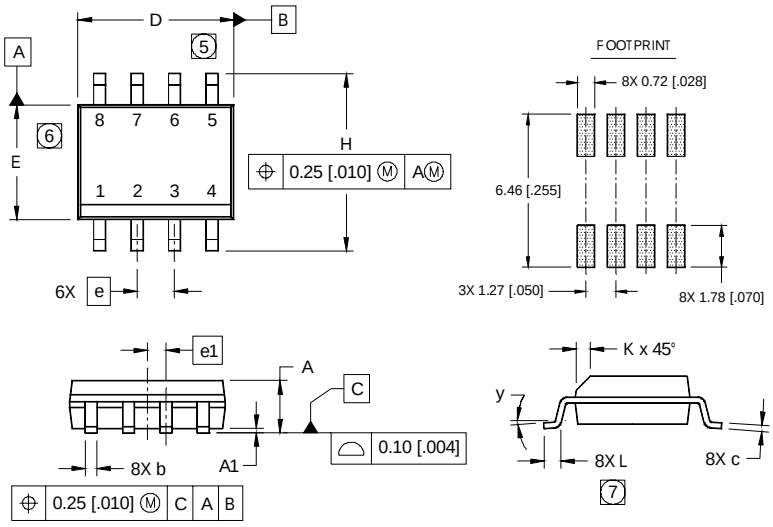


Figure 23B. Output Sink Current vs Voltage

Case Outlines





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

8 Lead SOIC

Data Sheet No. PD60162-N

International
IOR Rectifier

IR2106(4) (S)

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V (IR2106(4))
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs (IR2106)

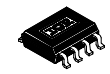
Description

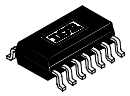
The IR2106(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Product Summary

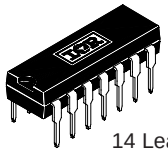
V_{OFFSET}	600V max.	
I_O+/-	120 mA / 250 mA	
V_{OUT}	10 - 20V (IR2106(4))	7 - 20V (IR2186)
$t_{on/off}$ (typ.)	180 ns	
Delay matching	50 ns	

Packages

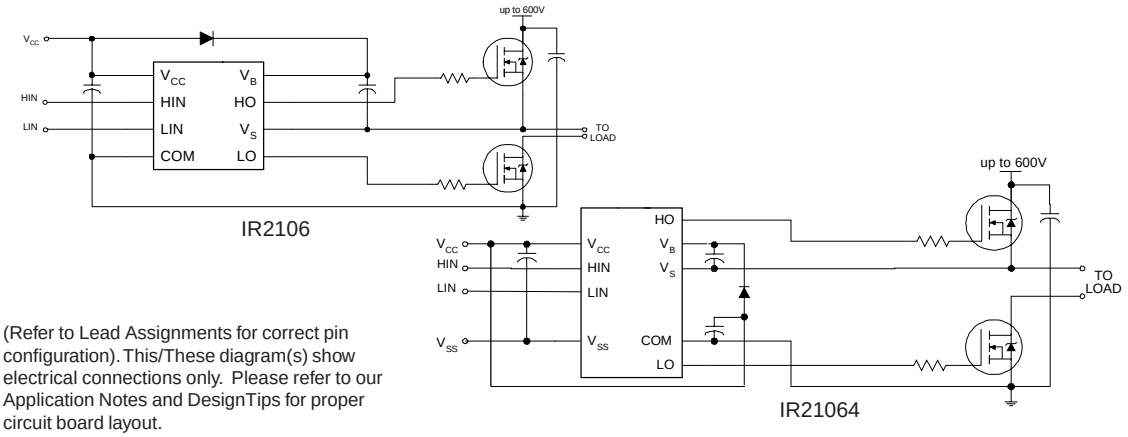

8 Lead SOIC


14 Lead SOIC


8 Lead PDIP


14 Lead PDIP

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage		V_{SS} - 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground (IR21064 only)		V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
VB	High side floating supply absolute voltage IR2106(4)	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage IR2106(4)	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21064 only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C.

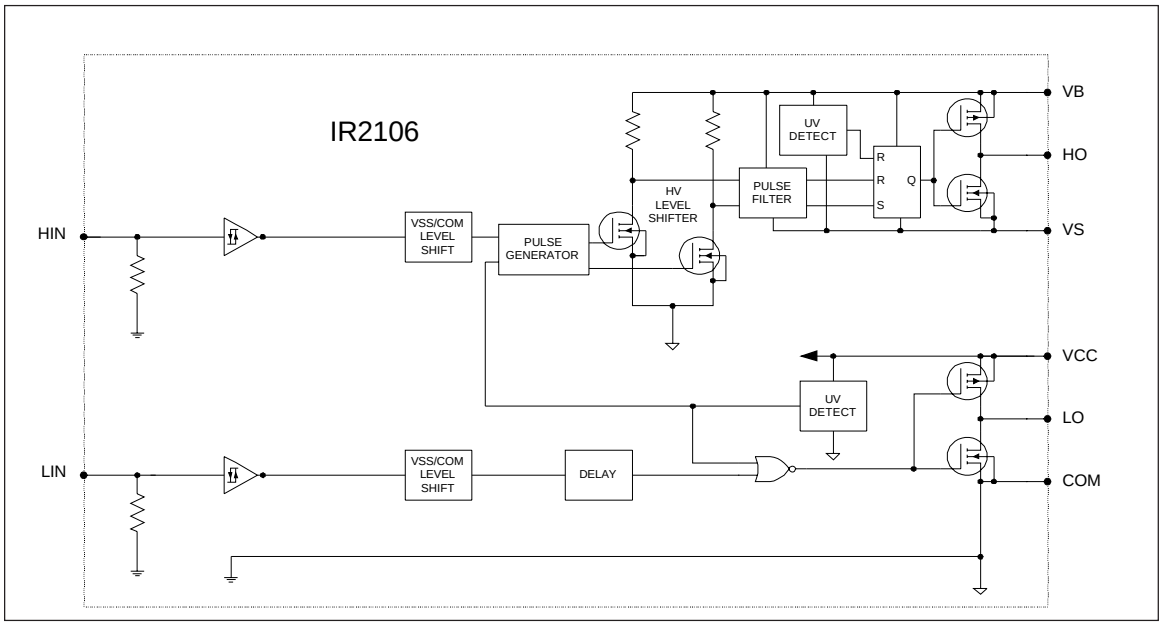
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	220	300	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	200	280		V_S = 0V or 600V
MT	Delay matching, HS & LS turn-on/off	—	0	30		
t_r	Turn-on rise time	—	150	220		V_S = 0V
t_f	Turn-off fall time	—	50	80		V_S = 0V

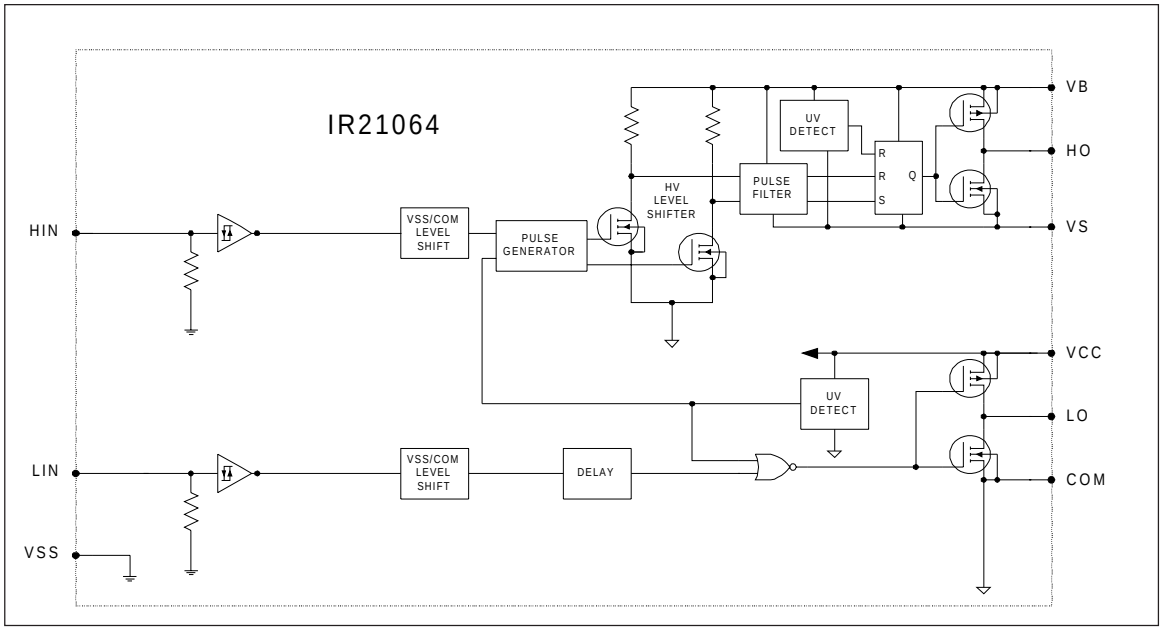
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads. The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage (IR2106(4))	2.9	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic "0" input voltage (IR2106(4))	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.8	1.4		I_O = 20 mA
V_{OL}	Low level output voltage, V_O	—	0.3	0.6		I_O = 20 mA
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	50	120	240		V_{IN} = 0V or 5V
I_{IN+}	Logic "1" input bias current V_{IN} = 5V (IR2106(4))	—	5	20		
I_{IN-}	Logic "0" input bias current V_{IN} = 0V (IR2106(4))	—	1	2		
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	V_O = 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	250	350	—		V_O = 15V, PW ≤ 10 µs

Functional Block Diagrams

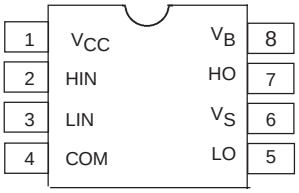




Lead Definitions

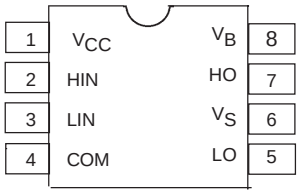
Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), in phase
VSS	Logic Ground (IR21064 only)
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



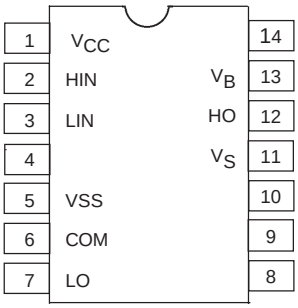
8 Lead PDIP

IR2106



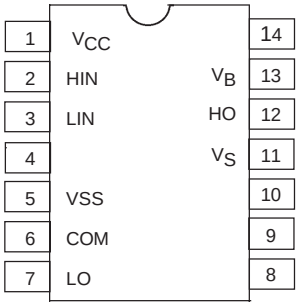
8 Lead SOIC

IR2106S



14 Lead PDIP

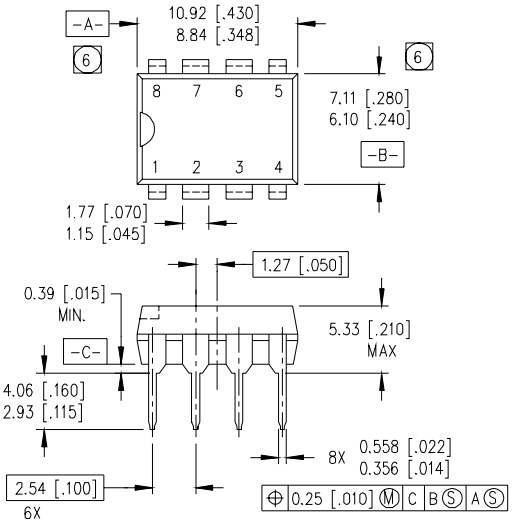
IR21064



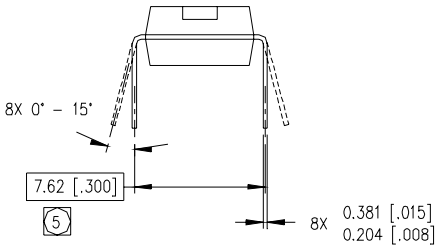
14 Lead SOIC

IR21064S

Case Outlines

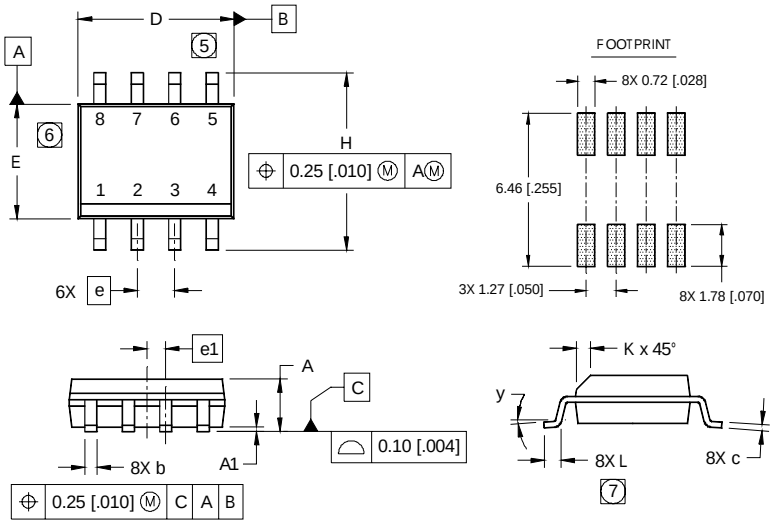


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8 Lead PDIP

01-6014
01-3003 01 (MS-001AB)

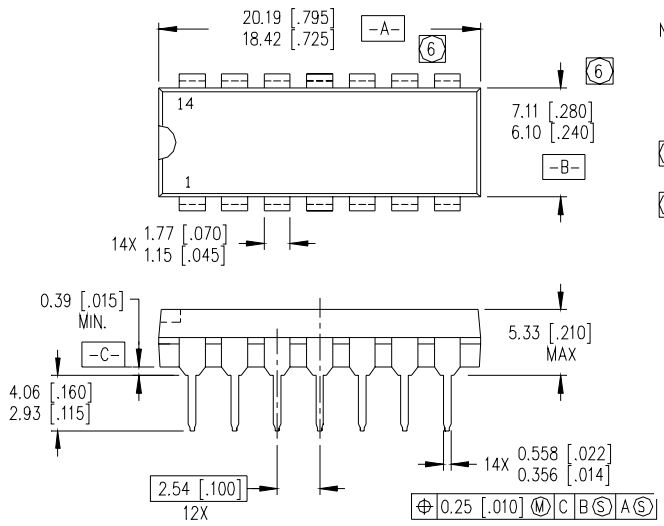


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

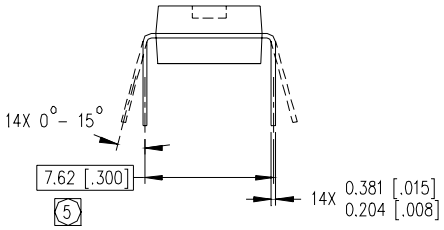
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

01-6027
01-0021 11 (MS-012AA)

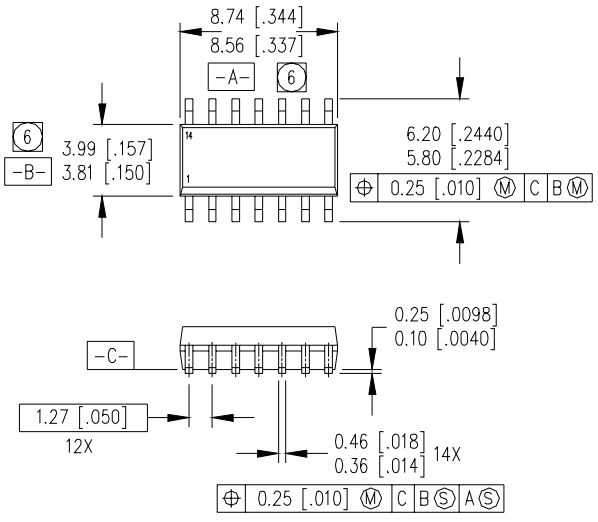


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

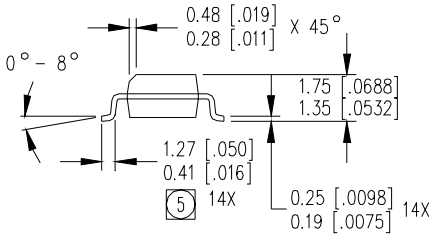


14 Lead PDIP

01-6010
01-3002 03 (MS-001AC)



NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2 CONTROLLING DIMENSION: MILLIMETER
3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4 OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AB.
5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



14 Lead SOIC (narrow body)

01-6019
01-3063 00 (MS-012AB)

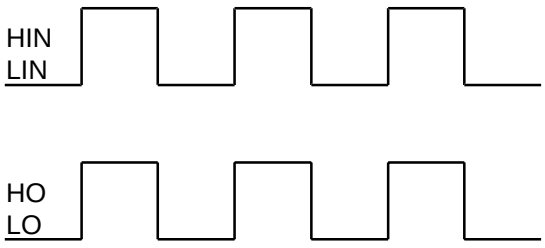


Figure 1. Input/Output Timing Diagram

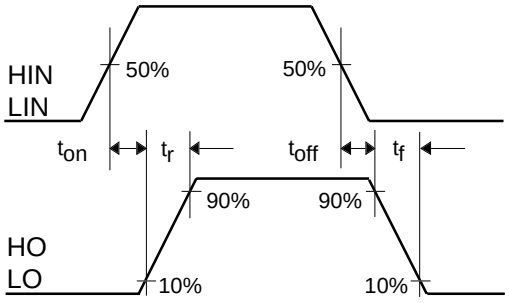


Figure 2. Switching Time Waveform Definitions

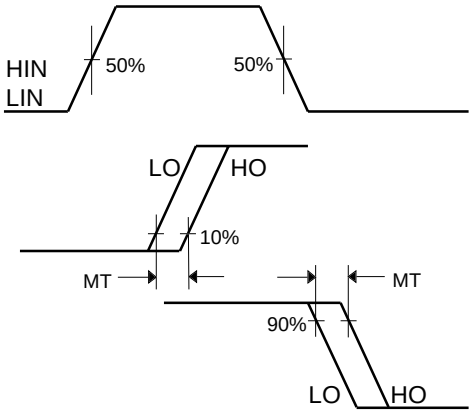


Figure 3. Delay Matching Waveform Definitions

International
IOR Rectifier

IR2108(4) (S)

HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High side output in phase with HIN input
- Low side output out of phase with $\overline{\text{LIN}}$ input
- Logic and power ground +/- 5V offset.
- Internal 540ns dead-time, and programmable up to 5us with one external R_{DT} resistor (IR21084)
- Lower di/dt gate driver for better noise immunity

Description

The IR2108(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Product Summary

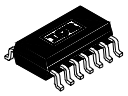
V_{OFFSET}	600V max.
I_O+/-	120 mA / 250 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	220 & 200 ns
Deadtime (typ.)	540 ns

(programmable up to 5uS for IR21084)

Packages



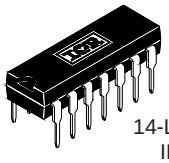
8-Lead SOIC
IR2108S



14-Lead SOIC
IR21084S

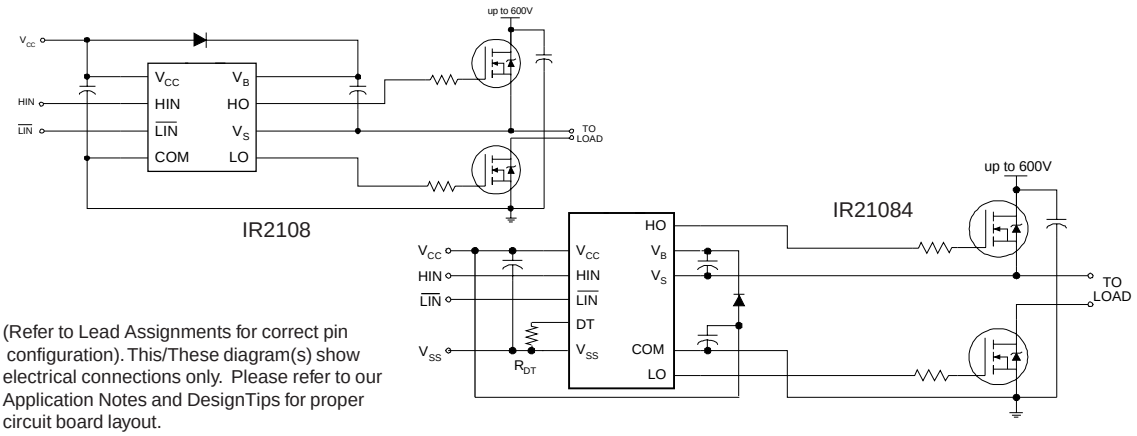


8-Lead PDIP
IR2108



14-Lead PDIP
IR21084

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
DT	Programmable dead-time pin voltage (IR21084 only)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground (IR21084 only)		V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
VB	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)	V_{SS}	V_{CC}	
DT	Programmable dead-time pin voltage (IR21084 only)	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21084 only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C, DT = VSS unless otherwise specified.

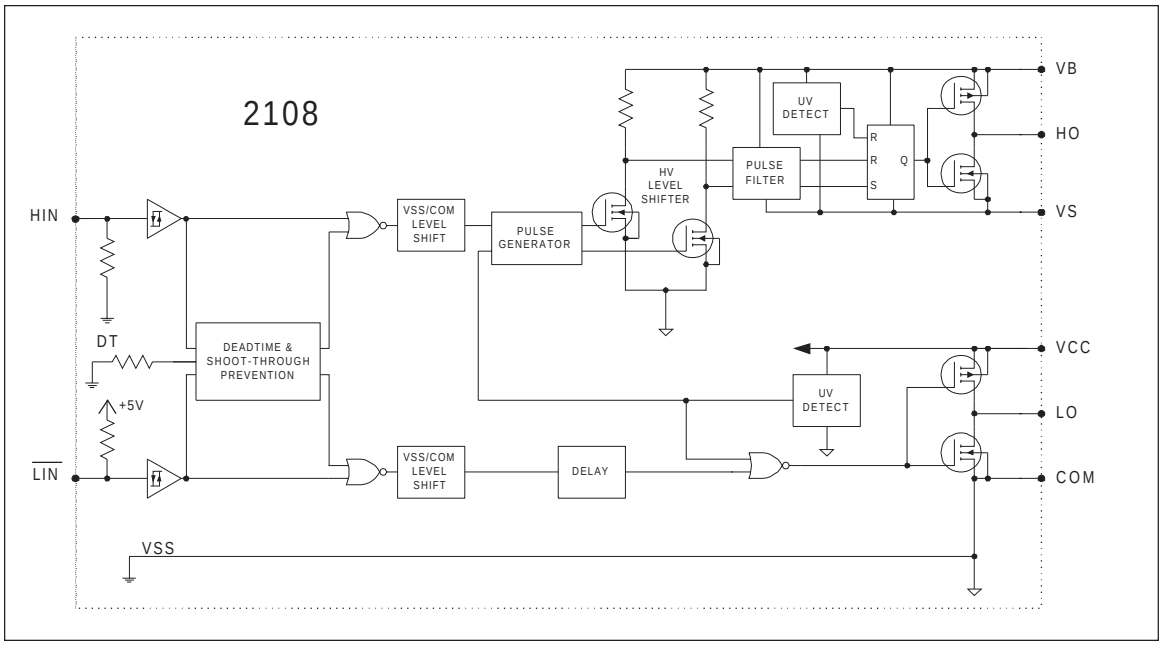
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	220	300	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	200	280		V_S = 0V or 600V
MT	Delay matching $\lvert t_{on} - t_{off} \rvert$	—	0	30		
t_r	Turn-on rise time	—	150	220		V_S = 0V
t_f	Turn-off fall time	—	50	80		V_S = 0V
DT	Deadtime: LO turn-off to HO turn-on(DT_{LO-HO}) &	400	540	680		RDT= 0
	HO turn-off to LO turn-on (DT_{HO-LO})	4	5	6	usec	RDT = 200k (IR21084)
MDT	Deadtime matching = $\lvert DT_{LO-HO} - DT_{HO-LO} \rvert$	—	0	60	nsec	RDT=0
		—	0	600		RDT = 200k (IR21084)

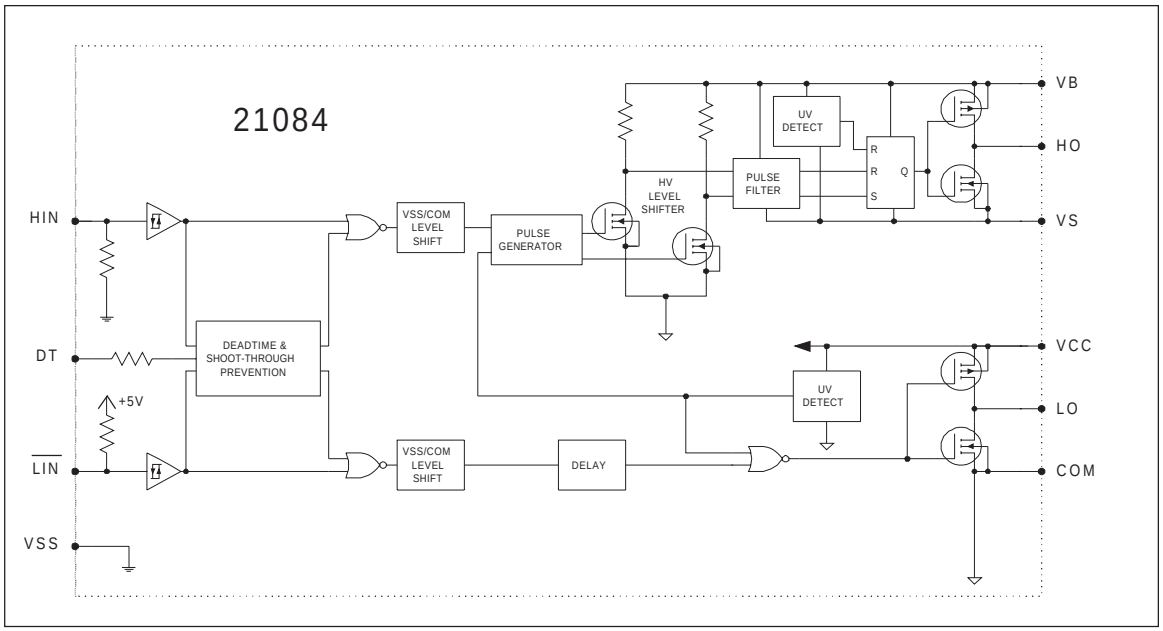
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, DT= V_{SS} and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads: $\overline{HIN}$ and LIN. The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” input voltage for HIN & logic “0” for $\overline{LIN}$	2.9	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic “0” input voltage for HIN & logic “1” for $\overline{LIN}$	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.8	1.4		I_O = 20 mA
V_{OL}	Low level output voltage, V_O	—	0.3	0.6		I_O = 20 mA
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	V_{IN} = 0V or 5V RDT=0
I_{IN+}	Logic “1” input bias current	—	5	20	µA	HIN = 5V, $\overline{LIN}$ = 0V
I_{IN-}	Logic “0” input bias current	—	1	2		HIN = 0V, $\overline{LIN}$ = 5V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	V_O = 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	250	350	—		V_O = 15V, PW ≤ 10 µs

Functional Block Diagram

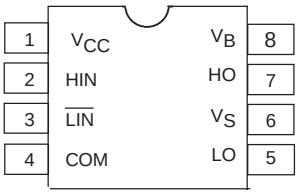




Lead Definitions

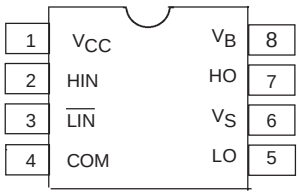
Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase (referenced to COM for IR2108 and VSS for IR21084)
$\overline{\text{LIN}}$	Logic input for low side gate driver output (LO), out of phase (referenced to COM for IR2108 and VSS for IR21084)
DT	Programmable dead-time lead, referenced to VSS. (IR21084 only)
VSS	Logic Ground (21084 only)
V_B	High side floating supply
HO	High side gate driver output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate driver output
COM	Low side return

Lead Assignments



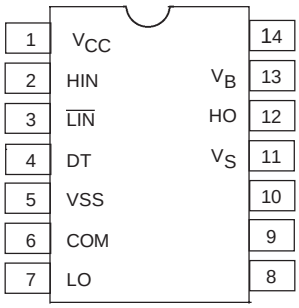
8 Lead PDIP

IR2108



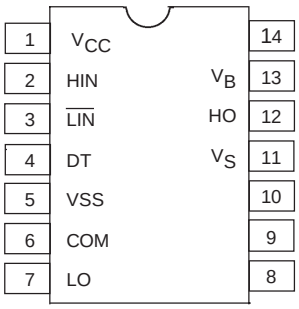
8 Lead SOIC

IR2108S



14 Lead PDIP

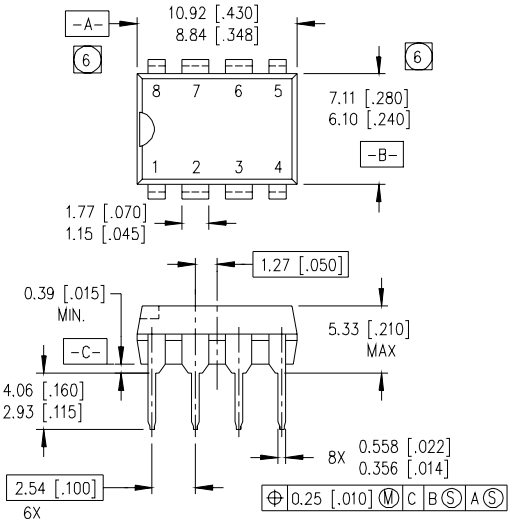
IR21084



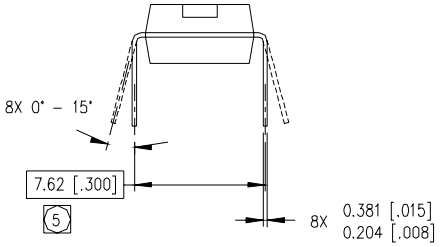
14 Lead SOIC

IR21084S

Case outlines

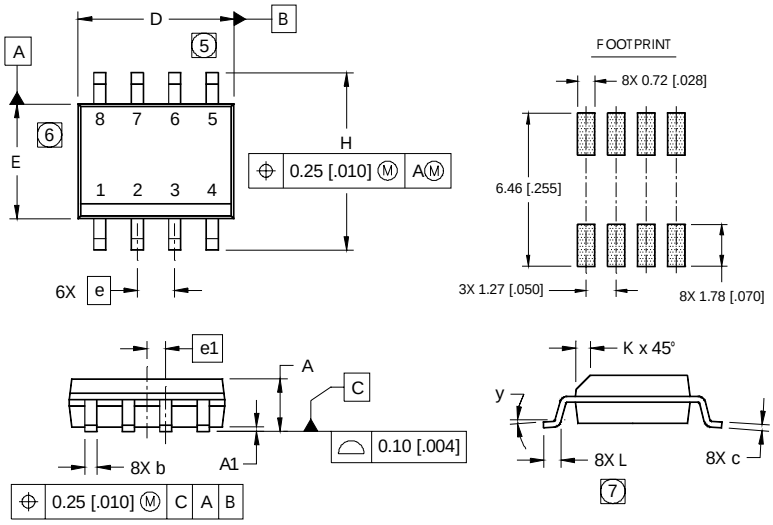


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8-Lead PDIP

01-6014
01-3003 01 (MS-001AB)

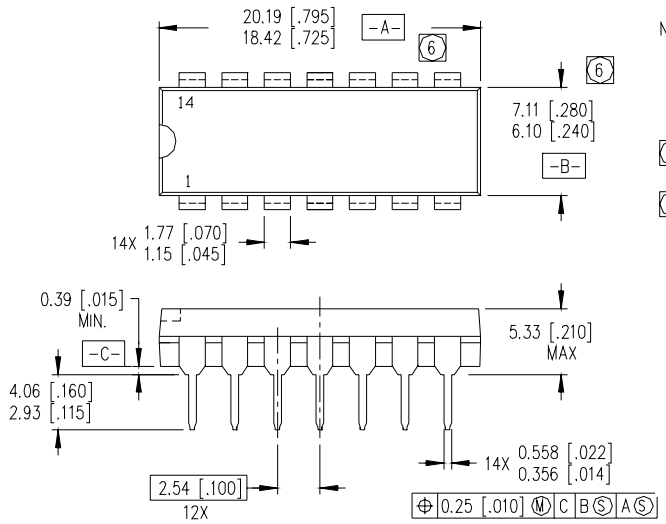


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

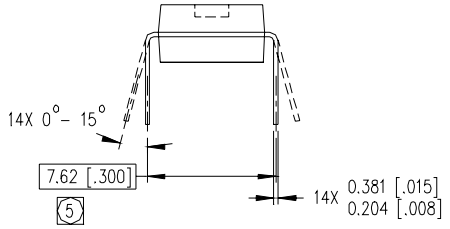
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8-Lead SOIC

01-6027
01-0021 11 (MS-012AA)

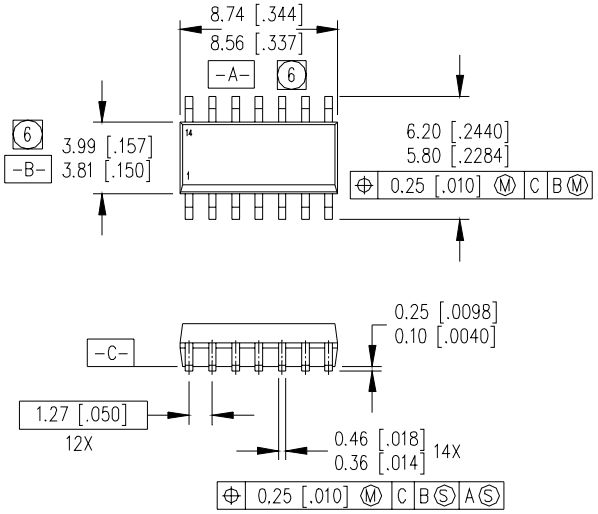


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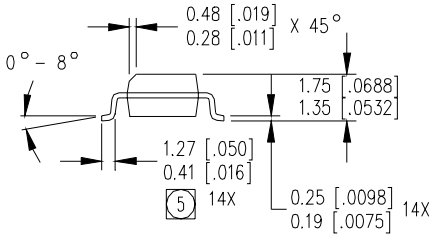


14-Lead PDIP

01-6010
01-3002 03 (MS-001AC)



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14-Lead SOIC (narrow body)

01-6019
01-3063 00 (MS-012AB)

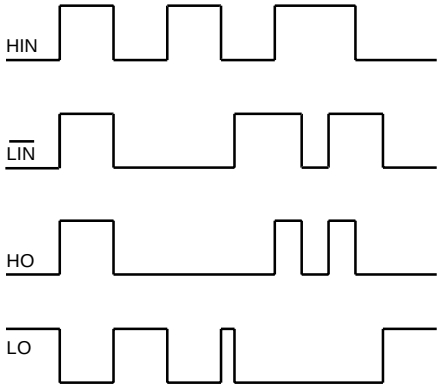
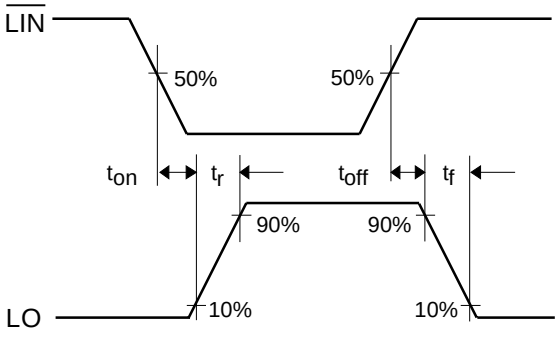


Figure 1. Input/Output Timing Diagram



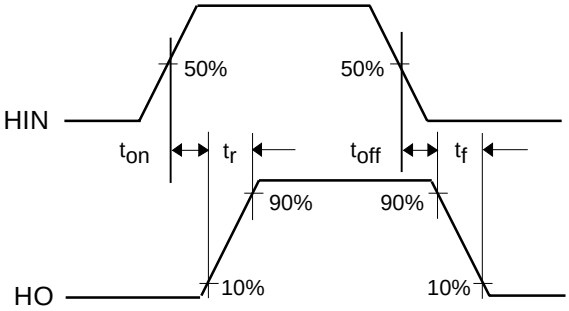


Figure 2. Switching Time Waveform Definitions

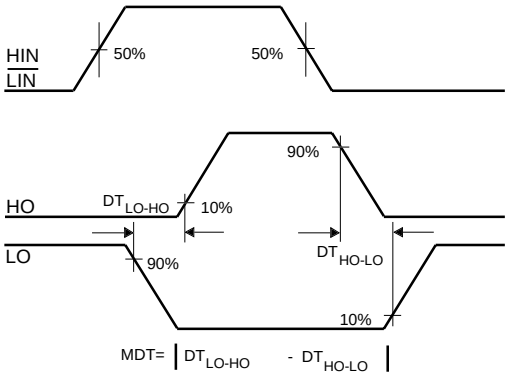


Figure 3. Deadtime Waveform Definitions

IR WORLD HEADQUARTERS: 233 Kansas Street, El Segundo, California 90245 Tel: (310) 252-7105

Data and specifications subject to change without notice. 5/29/12001

Data Sheet No. PD60163-P

International
IOR Rectifier

IR2109(4) (S)

HALF-BRIDGE DRIVER

Features

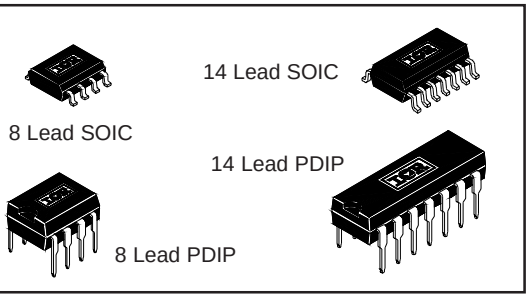
- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High side output in phase with IN input
- Logic and power ground +/- 5V offset.
- Internal 540ns dead-time, and programmable up to 5us with one external R_{DT} resistor (IR21094)
- Lower di/dt gate driver for better noise immunity
- Shut down input turns off both channels.

Product Summary

V_{OFFSET}	600V max.
I_O+/-	120 mA / 250 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	750 & 200 ns
Dead Time	540 ns

(programmable up to 5uS for IR21094)

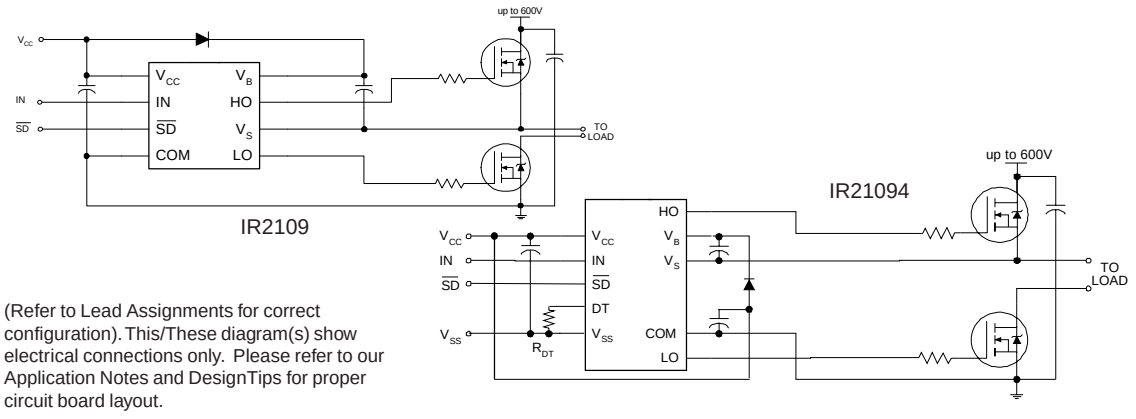
Packages



Description

The IR2109(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



(Refer to Lead Assignments for correct configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
DT	Programmable dead-time pin voltage (IR21094 only)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground (IR21094/IR21894 only)		V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 Lead PDIP)	—	1.0	W
		(8 Lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8 Lead PDIP)	—	125	°C/W
		(8 Lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
VB	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)	V_{SS}	V_{CC}	
DT	Programmable dead-time pin voltage (IR21094 only)	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21094 only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C, DT = VSS unless otherwise specified.

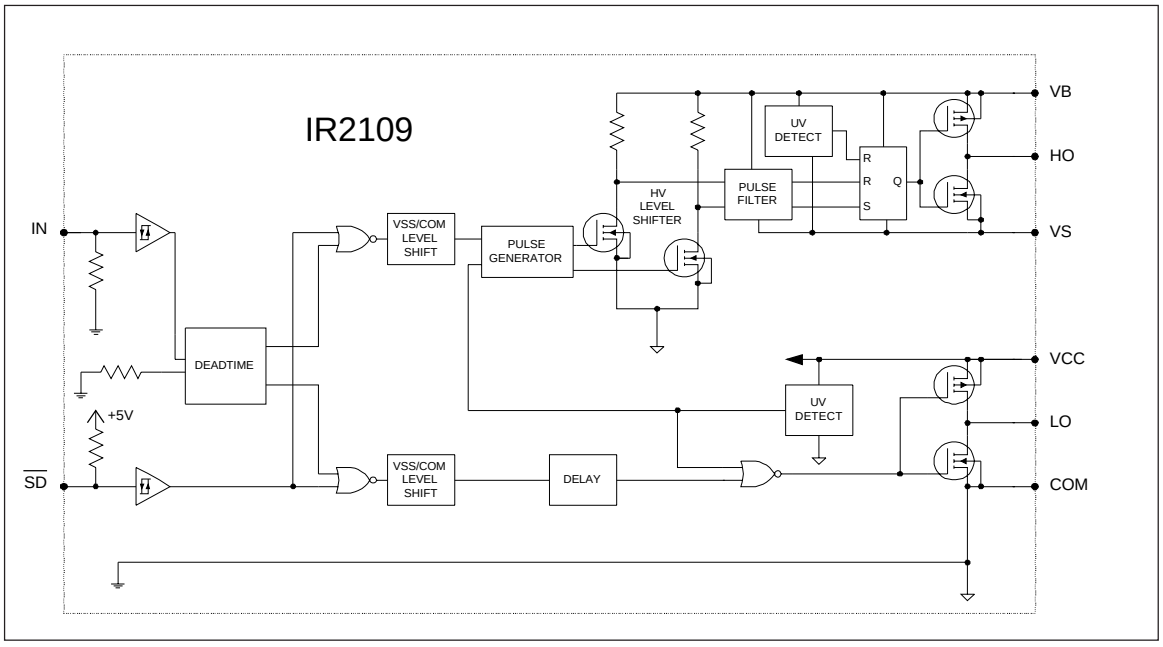
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	750	950	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	200	280		V_S = 0V or 600V
t_{sd}	Shut-down propagation delay	—	200	280		
MT	Delay matching, HS & LS turn-on/off	—	0	70		
t_r	Turn-on rise time	—	150	220		V_S = 0V
t_f	Turn-off fall time	—	50	80		V_S = 0V
DT	Deadtime: LO turn-off to HO turn-on(DT_{LO-HO}) &	400	540	680		RDT= 0
	HO turn-off to LO turn-on (DT_{HO-LO})	4	5	6	usec	RDT = 200k (IR21094)
MDT	Deadtime matching = $DT_{LO - HO}$ - DT_{HO-LO}	—	0	60	nsec	RDT=0
		—	0	600		RDT = 200k (IR21094)

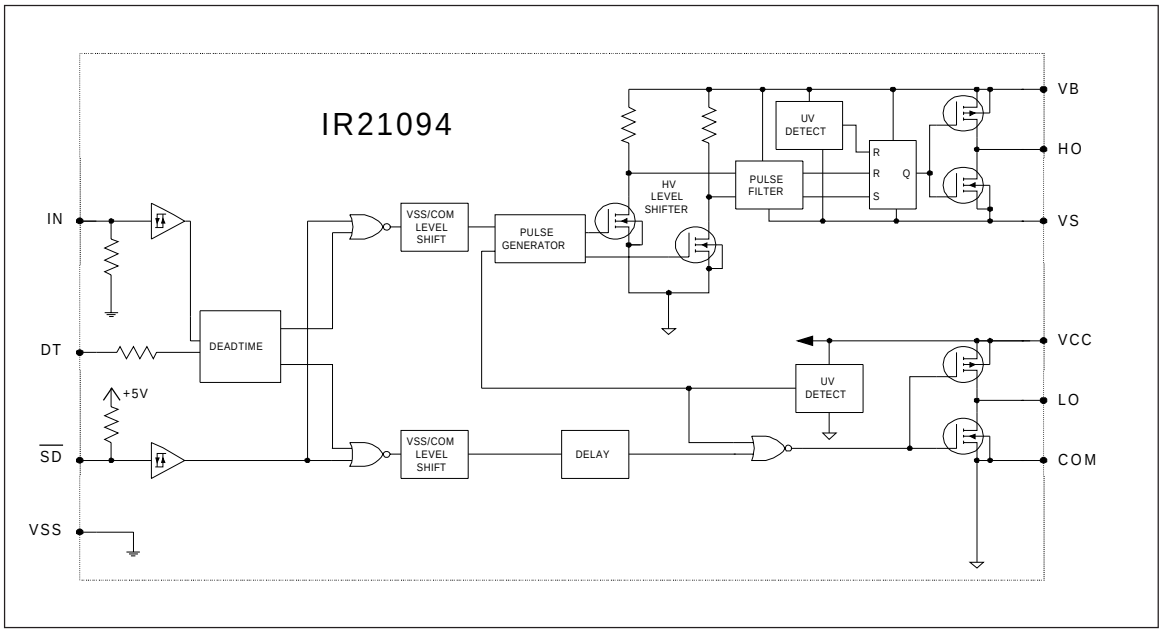
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, DT= V_{SS} and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS} /COM and are applicable to the respective input leads: IN and $\overline{SD}$. The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HO & logic "0" for LO	2.9	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic "0" input voltage for HO & logic "1" for LO	—	—	0.8		V_{CC} = 10V to 20V
$V_{SD,TH+}$	$\overline{SD}$ input positive going threshold	2.9	—	—		V_{CC} = 10V to 20V
$V_{SD,TH-}$	$\overline{SD}$ input negative going threshold	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.8	1.4		I_O = 20 mA
V_{OL}	Low level output voltage, V_O	—	0.3	0.6		I_O = 20 mA
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	V_{IN} = 0V or 5V RDT = 0
I_{IN+}	Logic "1" input bias current	—	5	20	µA	IN = 5V, $\overline{SD}$ = 0V
I_{IN-}	Logic "0" input bias current	—	1	2		IN = 0V, SD = 5V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed vurrent	120	200	—	mA	V_O = 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	250	350	—		V_O = 15V,PW ≤ 10 µs

Functional Block Diagrams

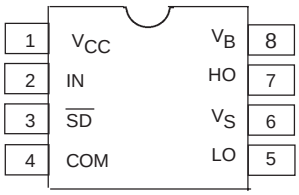




Lead Definitions

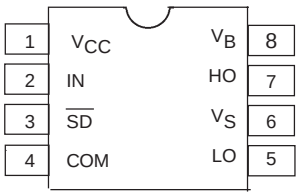
Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO (referenced to COM for IR2109 and VSS for IR21094)
$\overline{SD}$	Logic input for shutdown (referenced to COM for IR2109 and VSS for IR21094)
DT	Programmable dead-time lead, referenced to VSS. (IR21094 only)
VSS	Logic Ground (21094 only)
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



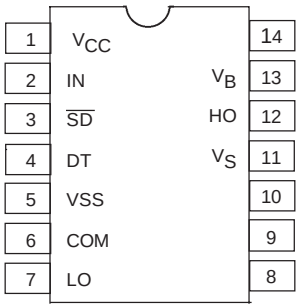
8 Lead PDIP

IR2109



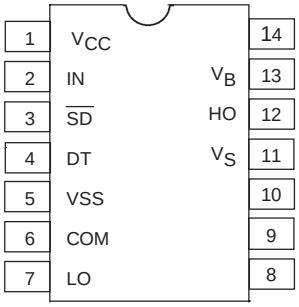
8 Lead SOIC

IR2109S



14 Lead PDIP

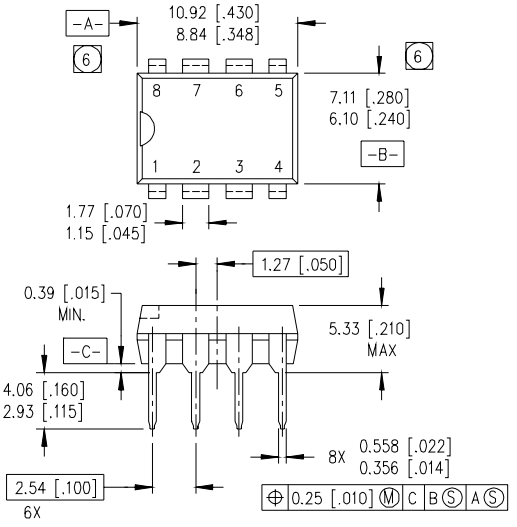
IR21094



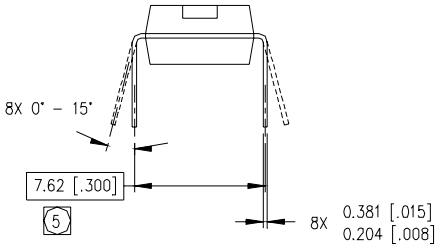
14 Lead SOIC

IR21094S

Case Outlines

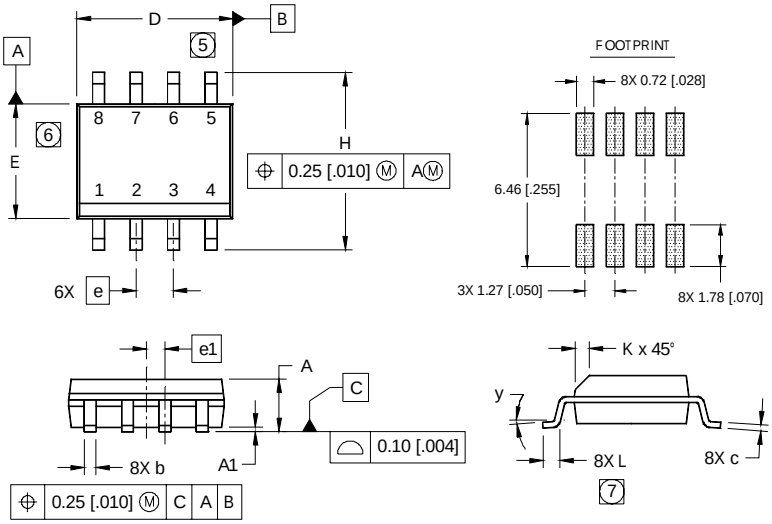


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8 Lead PDIP

01-6014
01-3003 01 (MS-001AB)

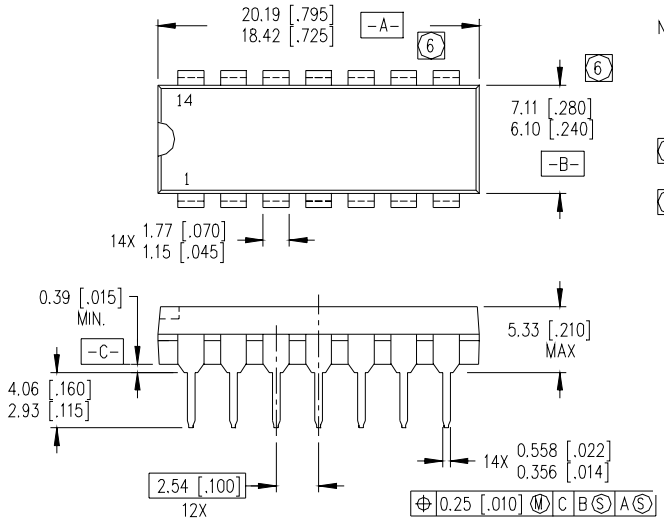


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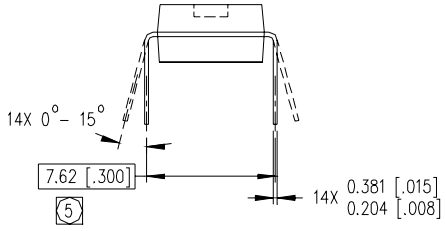
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8 Lead SOIC

01-6027
01-0021 11 (MS-012AA)

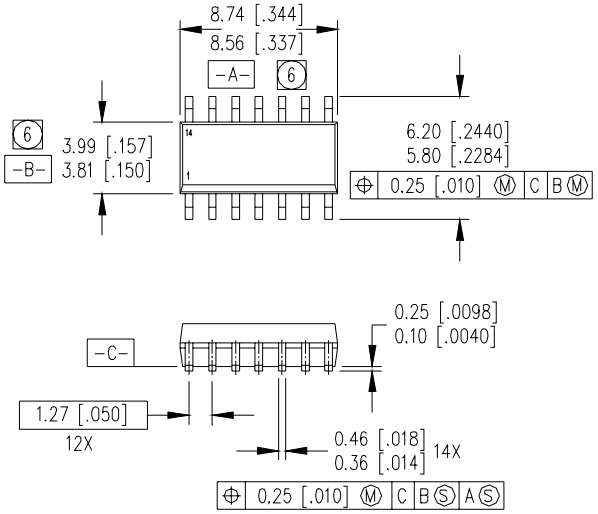


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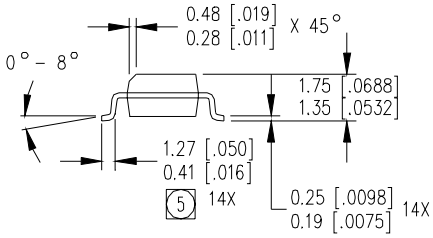


14 Lead PDIP

01-6010
01-3002 03 (MS-001AC)



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14 Lead SOIC (narrow body)

01-6019
01-3063 00 (MS-012AB)

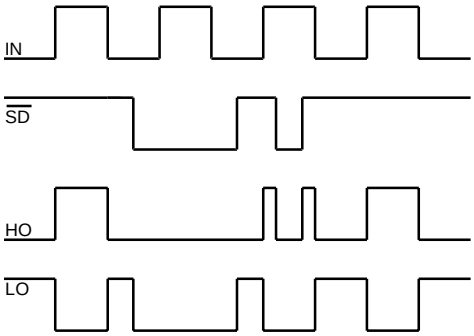


Figure 1. Input/Output Timing Diagram

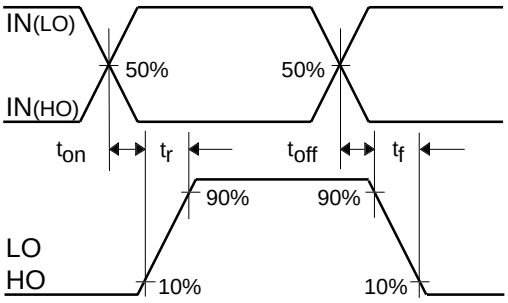


Figure 2. Switching Time Waveform Definitions

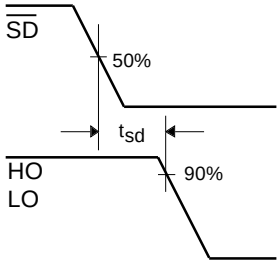


Figure 3. Shutdown Waveform Definitions

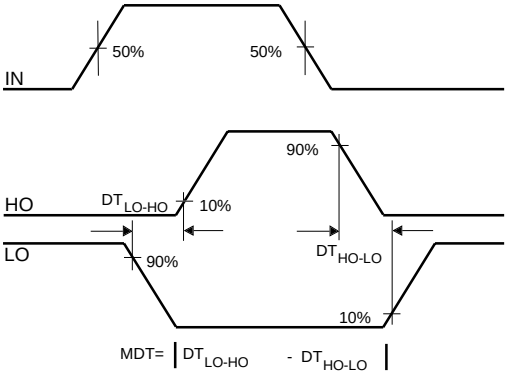


Figure 4. Deadtime Waveform Definitions

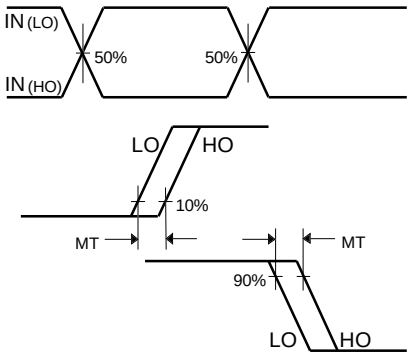


Figure 5. Delay Matching Waveform Definitions

Data Sheet No. PD60147-P

International
IOR Rectifier

IR2110/IR2113 (S)

HIGH AND LOW SIDE DRIVER

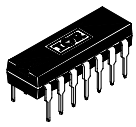
Features

- Floating channel designed for bootstrap operation
  Fully operational to +500V or +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
  Separate logic supply range from 3.3V to 20V
  Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

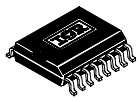
Product Summary

V_{OFFSET} (IR2110)	500V max.
(IR2113)	600V max.
I_O+/-	2A / 2A
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	120 & 94 ns
Delay Matching	10 ns

Packages



14-Lead PDIP
IR2110/IR2113

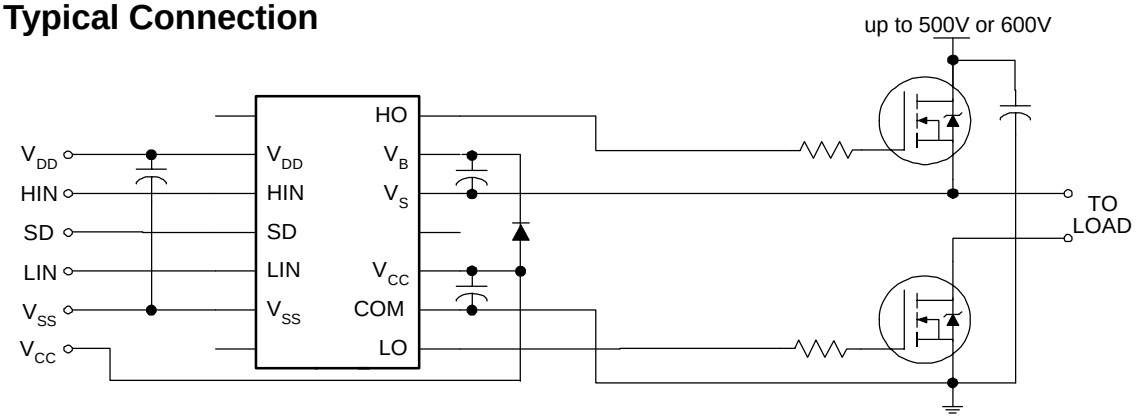


16-Lead SOIC
IR2110S/IR2113S

Description

The IR2110/IR2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage	(IR2110)	-0.3	525	V
		(IR2113)	-0.3	625	
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{DD}	Logic supply voltage		-0.3	V_{SS} + 25	
V_{SS}	Logic supply offset voltage		V_{CC} - 25	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN, LIN & SD)		V_{SS} - 0.3	V_{DD} + 0.3	
dV_S/dt	Allowable offset supply voltage transient (figure 2)		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(14 lead DIP)	—	1.6	W
		(16 lead SOIC)	—	1.25	
R_{THJA}	Thermal resistance, junction to ambient	(14 lead DIP)	—	75	°C/W
		(16 lead SOIC)	—	100	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in figures 36 and 37.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply absolute voltage		V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	(IR2110)	Note 1	500	
		(IR2113)	Note 1	600	
V_{HO}	High side floating output voltage		V_S	V_B	
V_{CC}	Low side fixed supply voltage		10	20	
V_{LO}	Low side output voltage		0	Vcc	
V_{DD}	Logic supply voltage		V_{SS} + 3	V_{SS} + 20	
V_{SS}	Logic supply offset voltage		-5 (Note 2)	5	
V_{IN}	Logic input voltage (HIN, LIN & SD)		V_{SS}	V_{DD}	
T_A	Ambient temperature		-40	125	°C

Note 1: Logic operational for V_S of -4 to +500V. Logic state held for V_S of -4V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).
Note 2: When $V_{DD} < 5V$, the minimum V_{SS} offset is limited to $-V_{DD}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

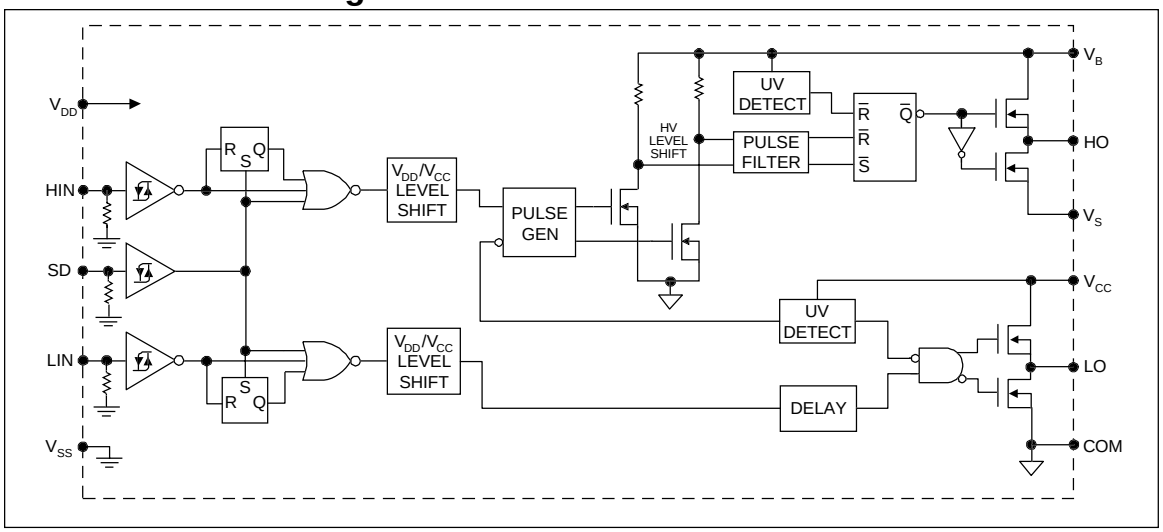
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	7	—	120	150	ns	V_S = 0V
t_{off}	Turn-off propagation delay	8	—	94	125		V_S = 500V/600V
t_{sd}	Shutdown propagation delay	9	—	110	140		V_S = 500V/600V
t_r	Turn-on rise time	10	—	25	35		
t_f	Turn-off fall time	11	—	17	25		
MT	Delay matching, HS & LS turn-on/off	—	—	—	10		Figure 5

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” input voltage	12	9.5	—	—	V	
V_{IL}	Logic “0” input voltage	13	—	—	6.0		
V_{OH}	High level output voltage, V_{BIAS} - V_O	14	—	—	1.2		I_O = 0A
V_{OL}	Low level output voltage, V_O	15	—	—	0.1		I_O = 0A
I_{LK}	Offset supply leakage current	16	—	—	50	µA	V_B=V_S = 500V/600V
I_{QBS}	Quiescent V_{BS} supply current	17	—	125	230		V_{IN} = 0V or V_{DD}
I_{QCC}	Quiescent V_{CC} supply current	18	—	180	340		V_{IN} = 0V or V_{DD}
I_{QDD}	Quiescent V_{DD} supply current	19	—	15	30		V_{IN} = 0V or V_{DD}
I_{IN+}	Logic “1” input bias current	20	—	20	40		V_{IN} = V_{DD}
I_{IN-}	Logic “0” input bias current	21	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	22	7.5	8.6	9.7	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	23	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	24	7.4	8.5	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	25	7.0	8.2	9.4		
I_{O+}	Output high short circuit pulsed current	26	2.0	2.5	—	A	V_O = 0V, V_{IN} = V_{DD} PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	27	2.0	2.5	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

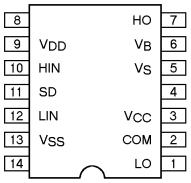
Functional Block Diagram



Lead Definitions

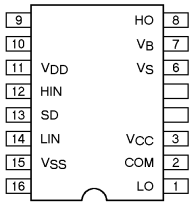
Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



14 Lead PDIP

IR2110/IR2113



16 Lead SOIC (Wide Body)

IR2110S/IR2113S

Part Number

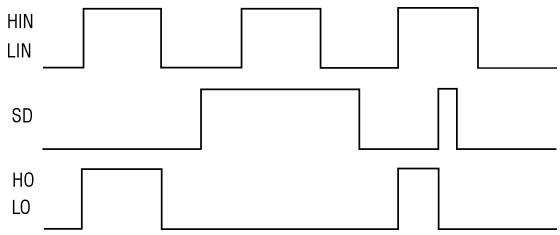


Figure 1. Input/Output Timing Diagram

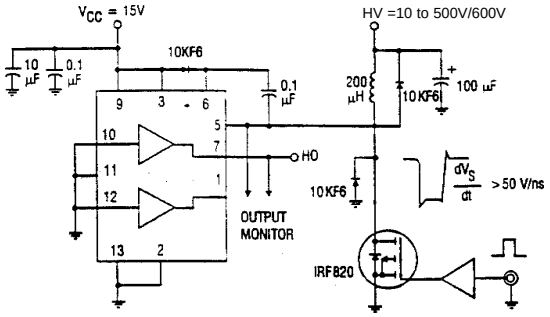


Figure 2. Floating Supply Voltage Transient Test Circuit

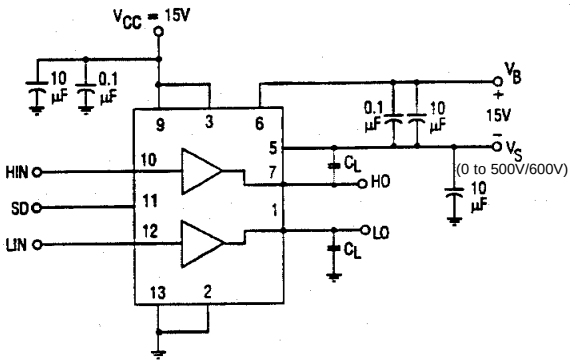


Figure 3. Switching Time Test Circuit

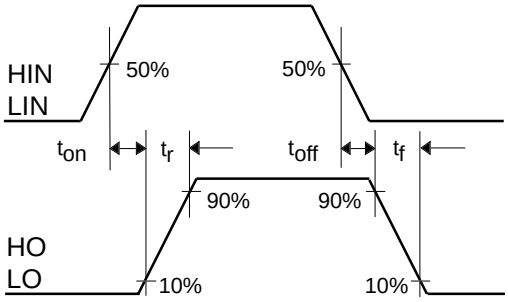


Figure 4. Switching Time Waveform Definition

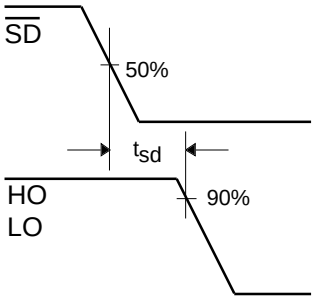


Figure 5. Shutdown Waveform Definitions

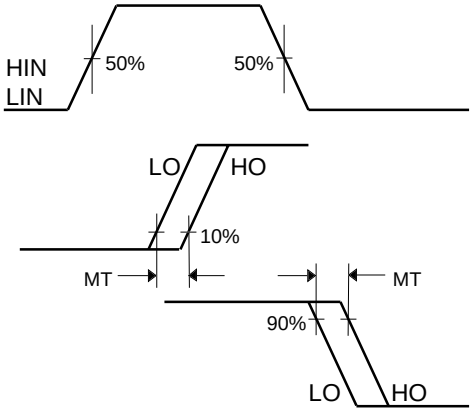


Figure 6. Delay Matching Waveform Definitions

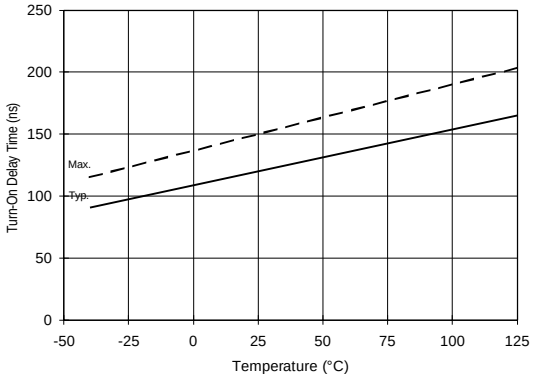


Figure 7A. Turn-On Time vs. Temperature

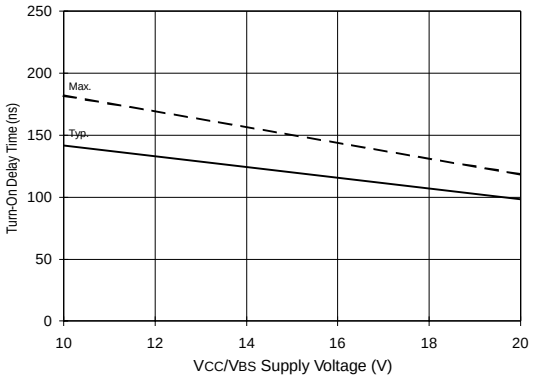


Figure 7B. Turn-On Time vs. VCC/VBS Supply Voltage

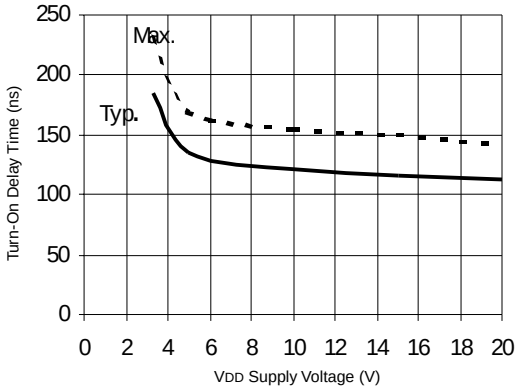


Figure 7C. Turn-On Time vs. VDD Supply Voltage

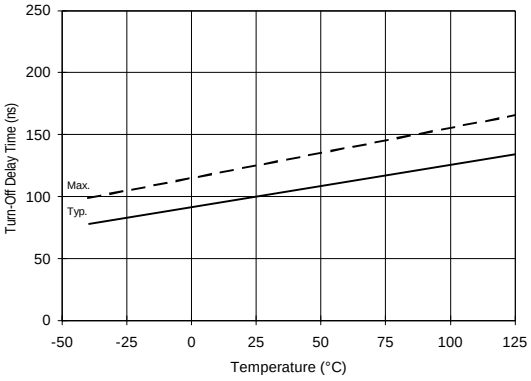


Figure 8A. Turn-Off Time vs. Temperature

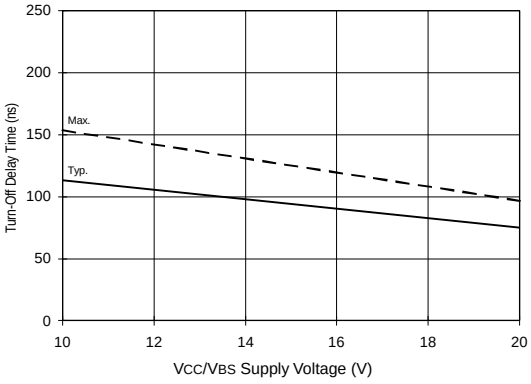


Figure 8B. Turn-Off Time vs. VCC/VBS Supply Voltage

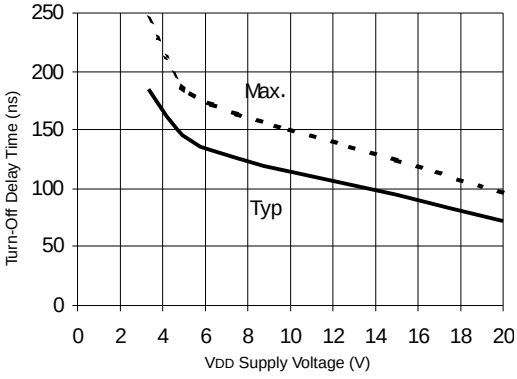


Figure 8C. Turn-Off Time vs. VDD Supply Voltage

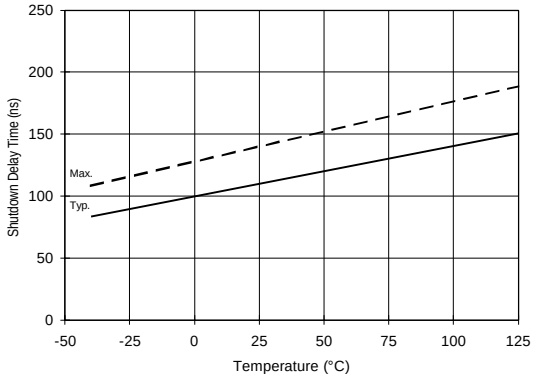


Figure 9A. Shutdown Time vs. Temperature

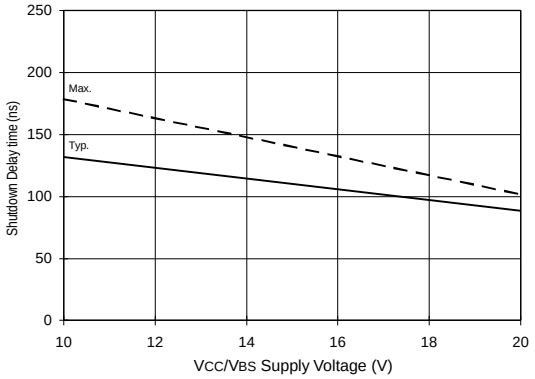


Figure 9B. Shutdown Time vs. V_{CC}/V_{BS} Supply Voltage

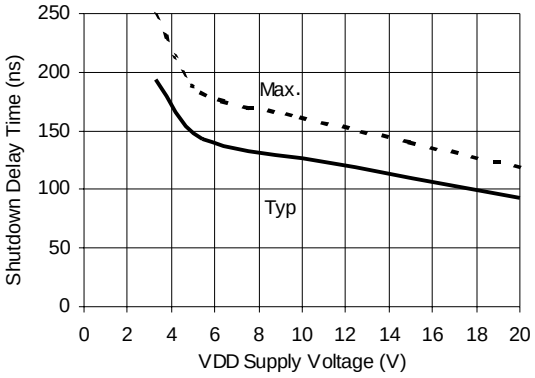


Figure 9C. Shutdown Time vs. V_{DD} Supply Voltage

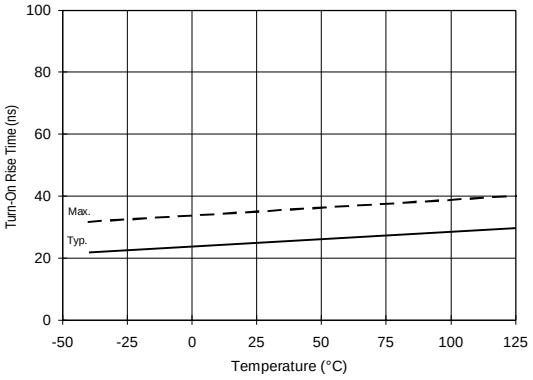


Figure 10A. Turn-On Rise Time vs. Temperature

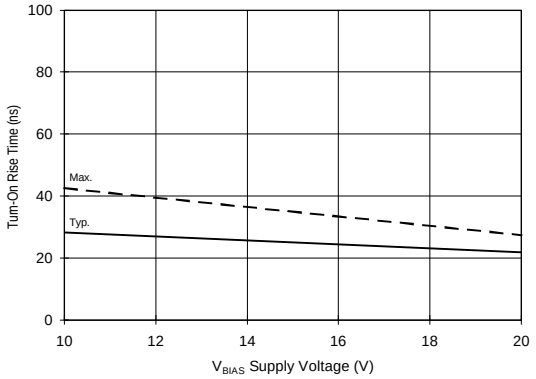


Figure 10B. Turn-On Rise Time vs. Voltage

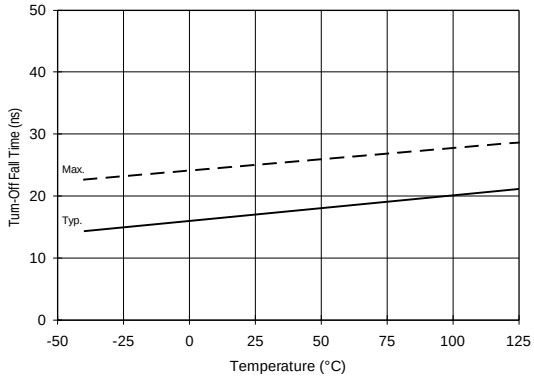


Figure 11A. Turn-Off Fall Time vs. Temperature

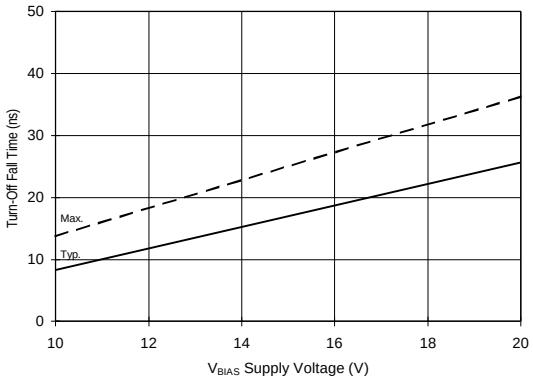


Figure 11B. Turn-Off Fall Time vs. Voltage

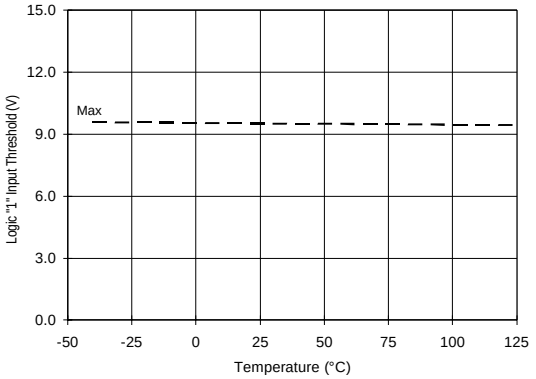


Figure 12A. Logic "1" Input Threshold vs. Temperature

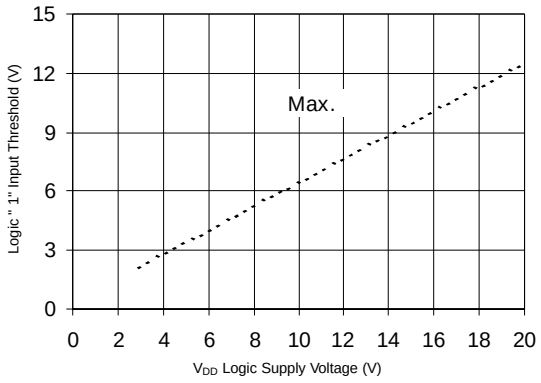


Figure 12B. Logic "1" Input Threshold vs. Voltage

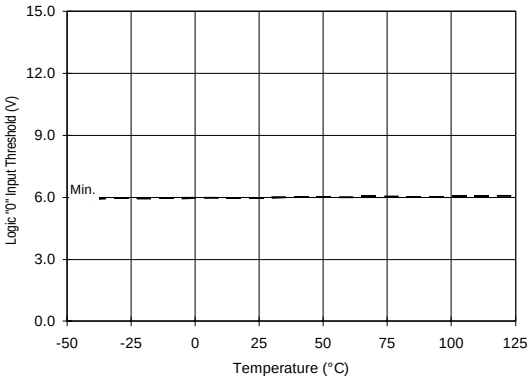


Figure 13A. Logic "0" Input Threshold vs. Temperature

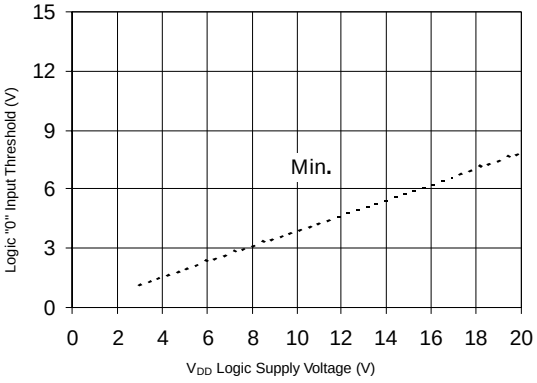


Figure 13B. Logic "0" Input Threshold vs. Voltage

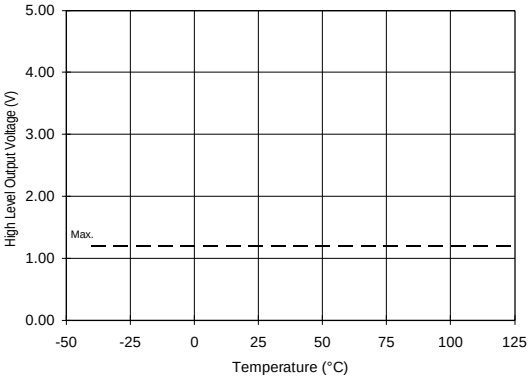


Figure 14A. High Level Output vs. Temperature

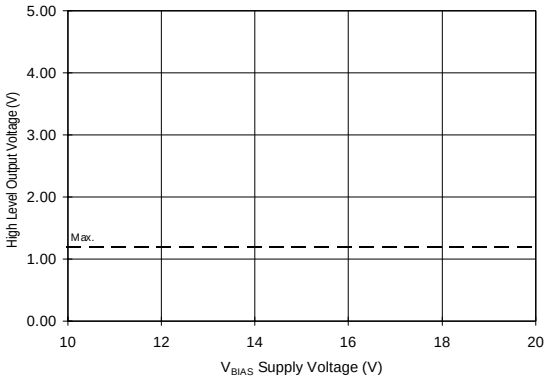


Figure 14B. High Level Output vs. Voltage

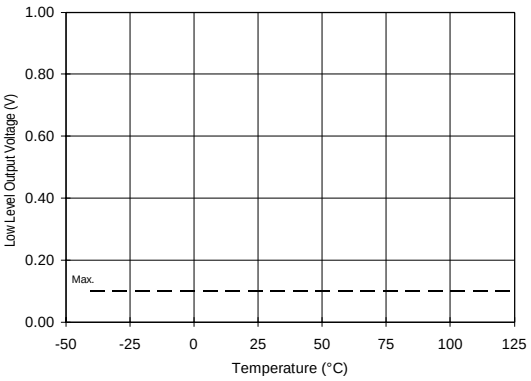


Figure 15A. Low Level Output vs. Temperature

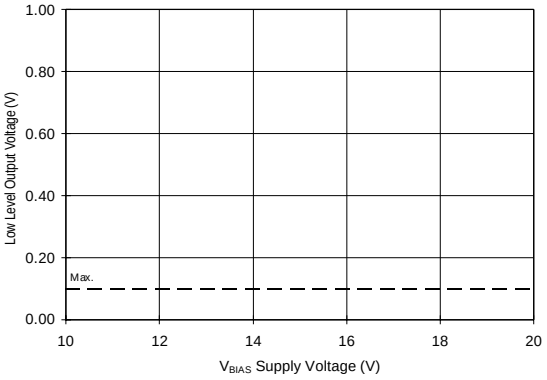


Figure 15B. Low Level Output vs. Voltage

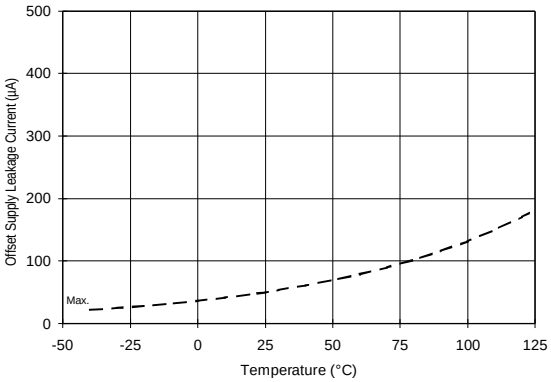


Figure 16A. Offset Supply Current vs. Temperature

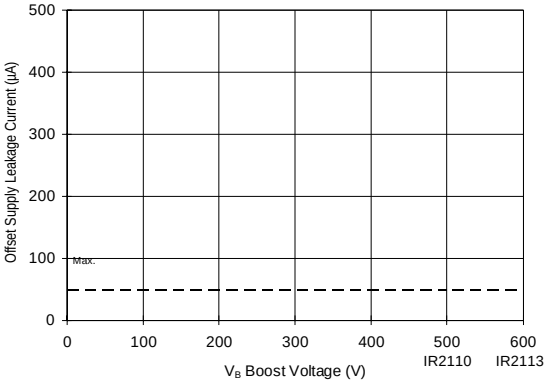


Figure 16B. Offset Supply Current vs. Voltage

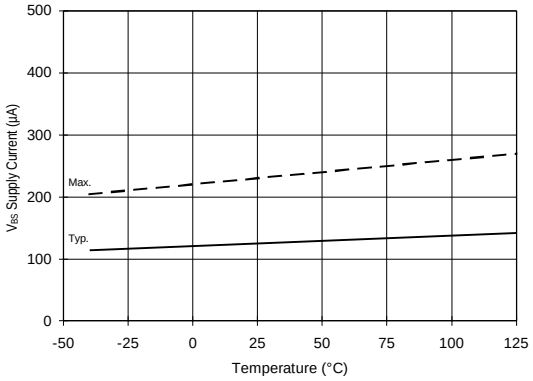


Figure 17A. V_{BS} Supply Current vs. Temperature

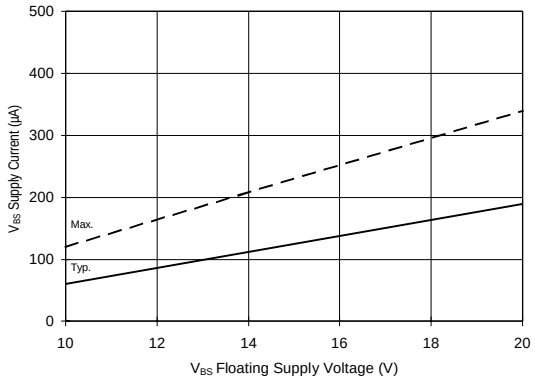


Figure 17B. V_{BS} Supply Current vs. Voltage

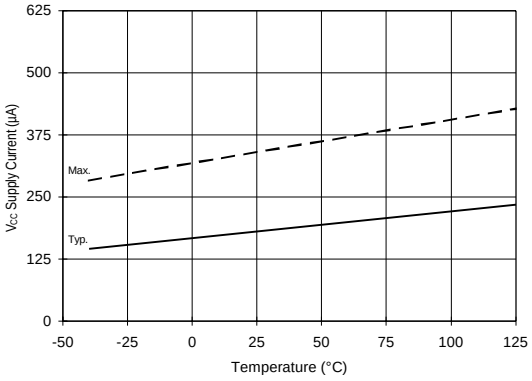


Figure 18A. V_{CC} Supply Current vs. Temperature

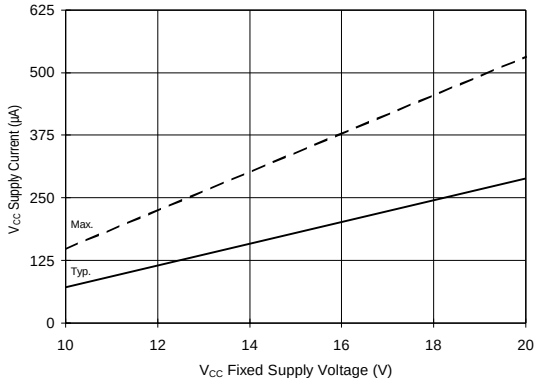


Figure 18B. V_{CC} Supply Current vs. Voltage

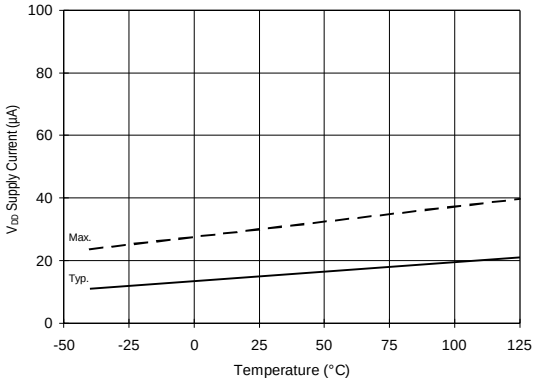


Figure 19A. V_{DD} Supply Current vs. Temperature

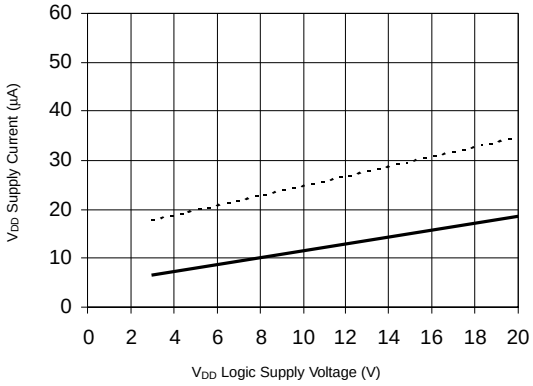


Figure 19B. V_{DD} Supply Current vs. V_{DD} Voltage

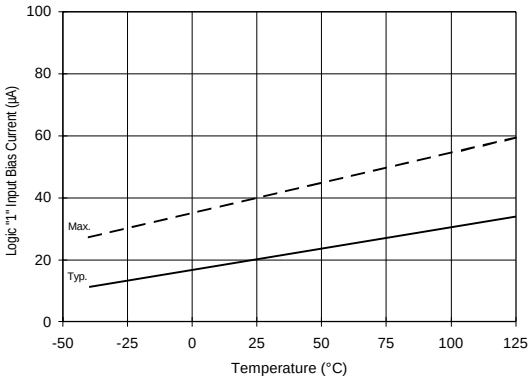


Figure 20A. Logic "1" Input Current vs. Temperature

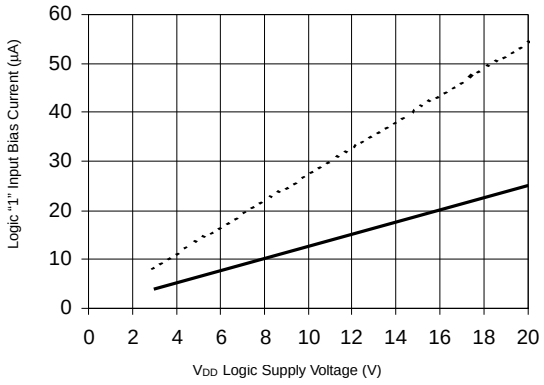


Figure 20B. Logic "1" Input Current vs. V_{DD} Voltage

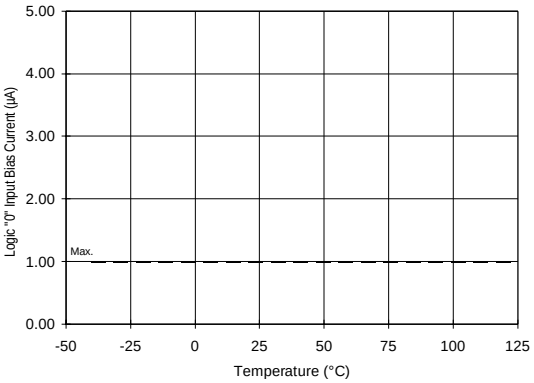


Figure 21A. Logic "0" Input Current vs. Temperature

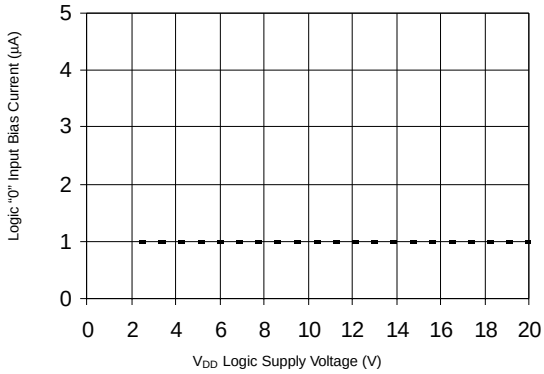


Figure 21B. Logic "0" Input Current vs. V_{DD} Voltage

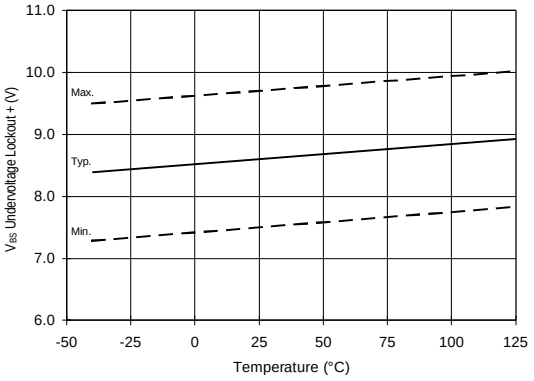


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

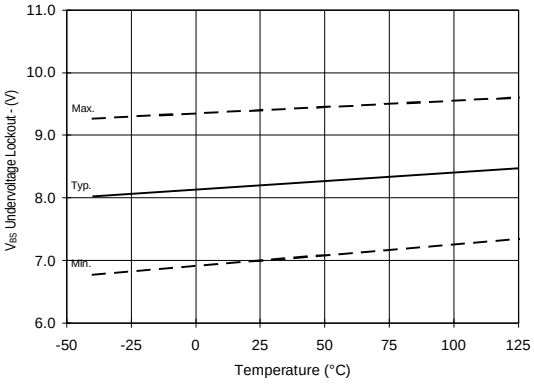


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

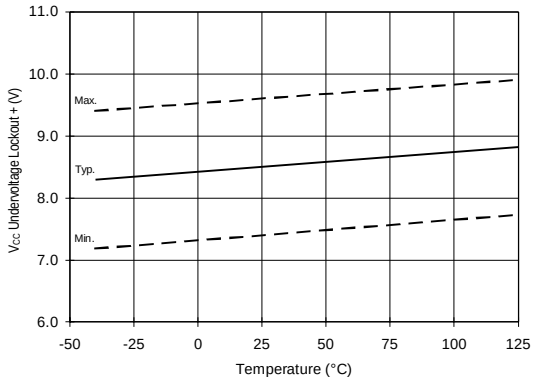


Figure 24. V_{CC} Undervoltage (+) vs. Temperature

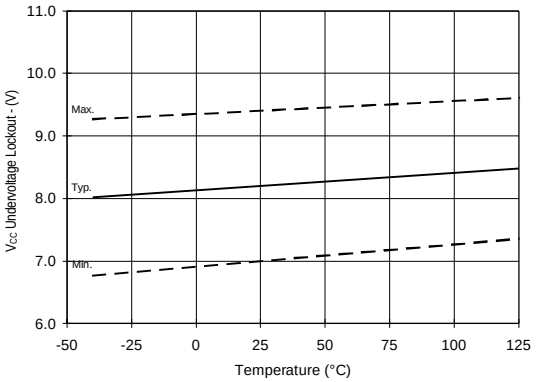


Figure 25. V_{CC} Undervoltage (-) vs. Temperature

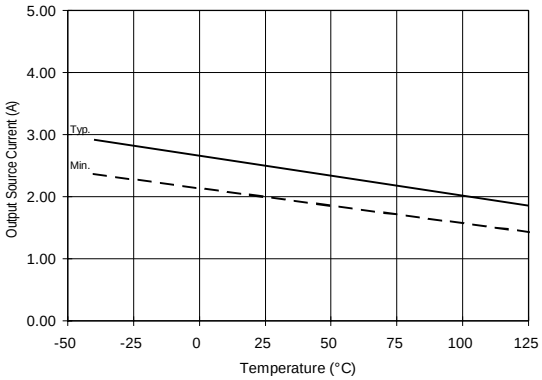


Figure 26A. Output Source Current vs. Temperature

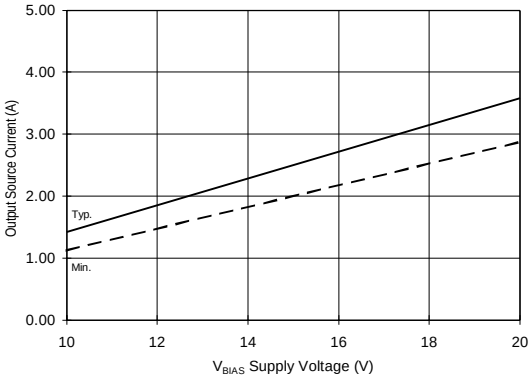


Figure 26B. Output Source Current vs. Voltage

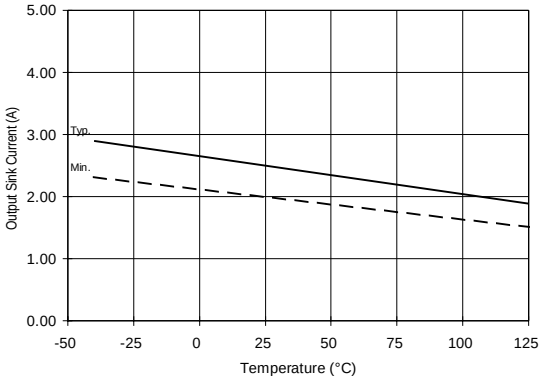


Figure 27A. Output Sink Current vs. Temperature

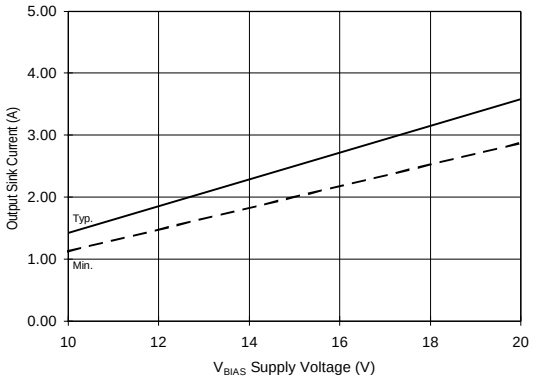


Figure 27B. Output Sink Current vs. Voltage

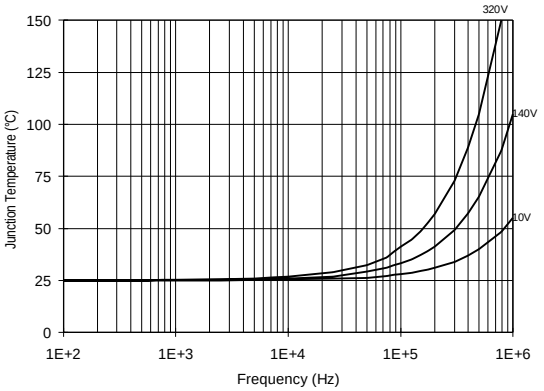


Figure 28. IR2110/IR2113 T_J vs. Frequency (IRFBC20) R_{GATE} = 33Ω, V_{CC} = 15V

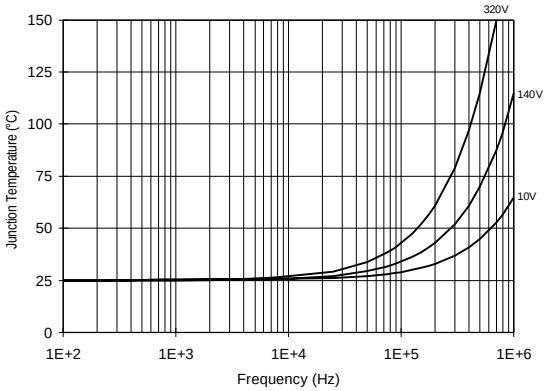


Figure 29. IR2110/IT2113 T_J vs. Frequency (IRFBC30) R_{GATE} = 22Ω, V_{CC} = 15V

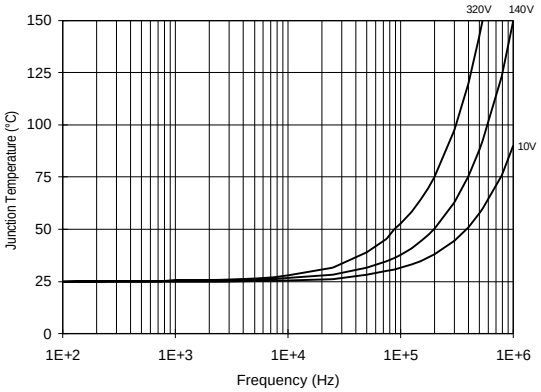


Figure 30. IR2110/IR2113 T_J vs. Frequency (IRFBC40) R_{GATE} = 15Ω, V_{CC} = 15V

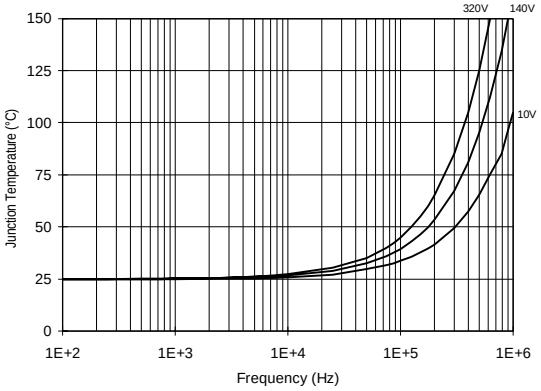


Figure 31. IR2110/IR2113 T_J vs. Frequency (IRFPE50) R_{GATE} = 10Ω, V_{CC} = 15V

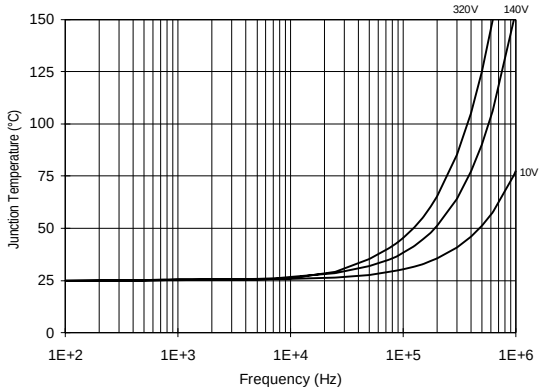


Figure 32. IR2110S/IR2113S T_J vs. Frequency (IRFBC20) R_{GATE} = 33Ω, V_{CC} = 15V

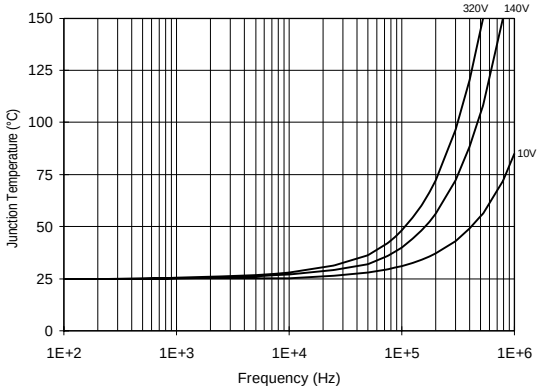


Figure 33. IR2110S/IR2113S T_J vs. Frequency (IRFBC30) R_{GATE} = 22Ω, V_{CC} = 15V

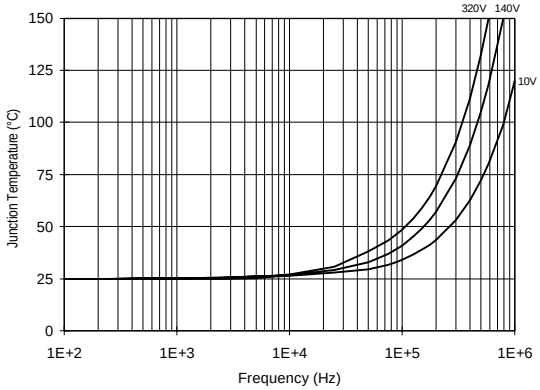


Figure 34. IR2110S/IR2113S T_J vs. Frequency (IRFBC40) R_{GATE} = 15Ω, V_{CC} = 15V

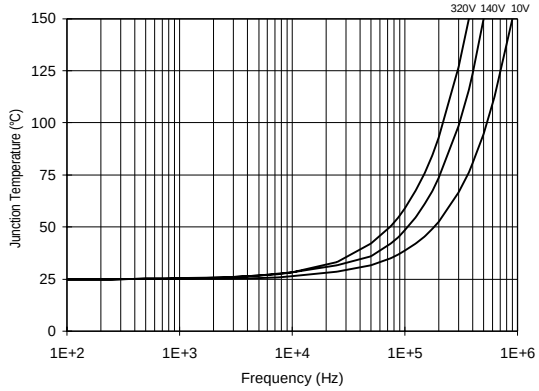


Figure 35. IR2110S/IR2113S T_J vs. Frequency (IRFPE50) R_{GATE} = 10Ω, V_{CC} = 15V

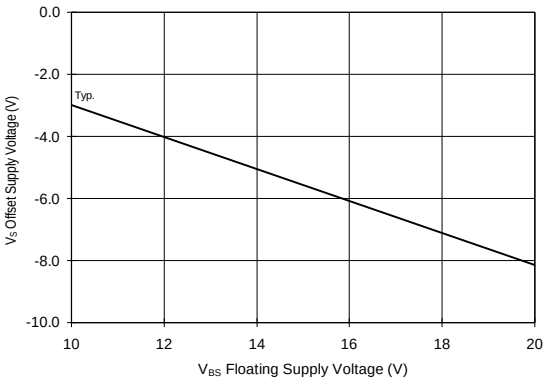


Figure 36. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

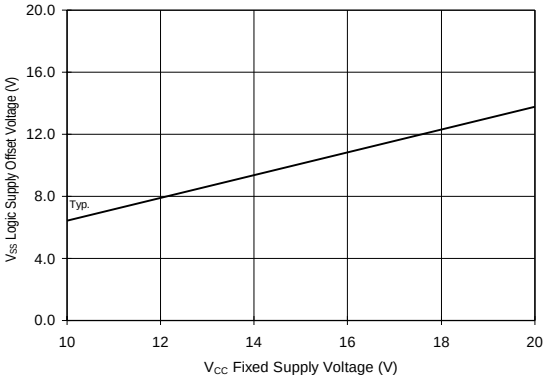
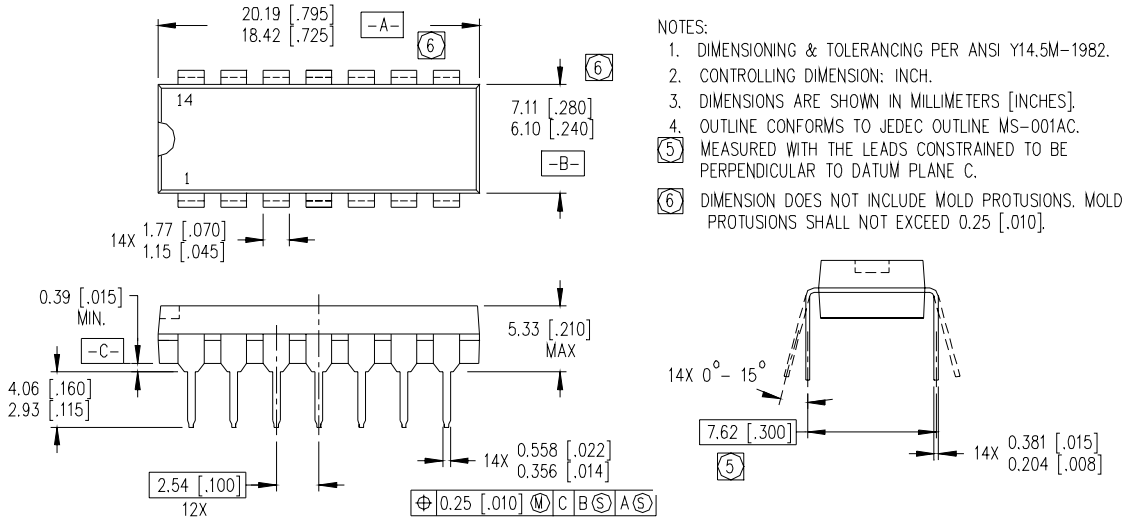


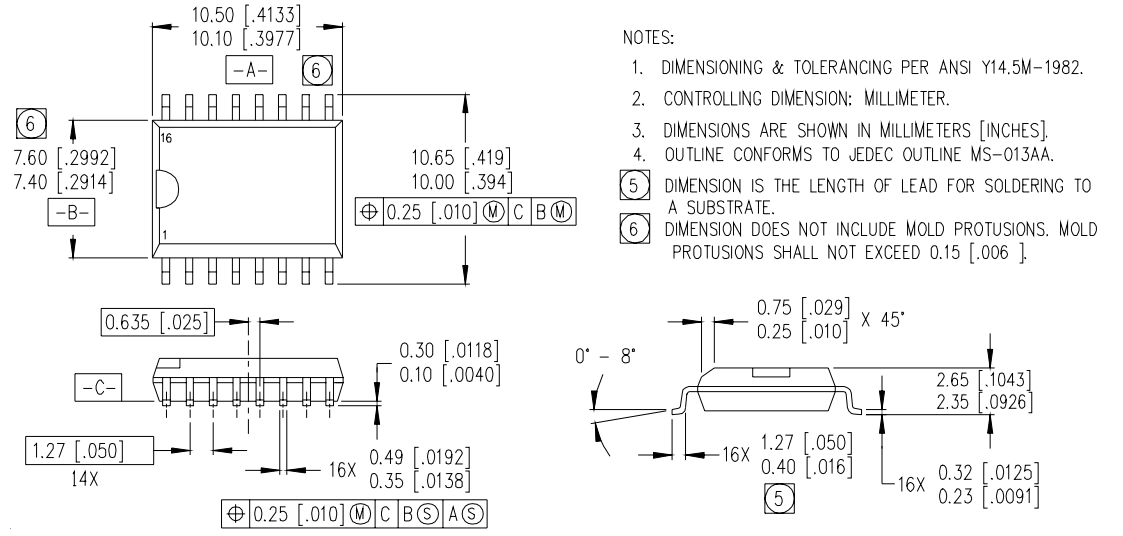
Figure 37. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage

Case Outlines



14-Lead PDIP

01-6010
01-3002 03 (MS-001AC)



16-Lead SOIC (wide body)

01 6015
01-3014 03 (MS-013AA)

IR2111

HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- CMOS Schmitt-triggered inputs with pull-down
- Matched propagation delay for both channels
- Internally set deadtime
- High side output in phase with input

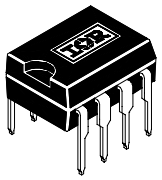
Product Summary

V_{OFFSET}	600V max.
I_O+/-	200 mA / 420 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	750 & 150 ns
Deadtime (typ.)	650 ns

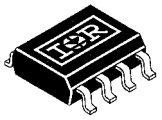
Description

The IR2111 is a high voltage, high speed power MOSFET and IGBT driver with dependent high and low side referenced output channels designed for half-bridge applications. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic input is compatible with standard CMOS outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Internal deadtime is provided to avoid shoot-through in the output half-bridge. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Packages

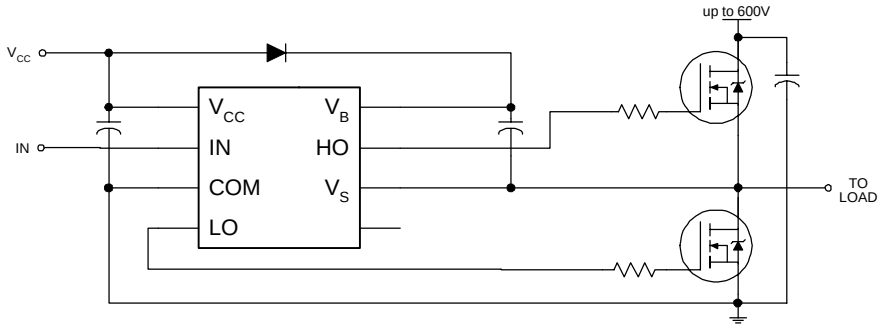


8-Lead PDIP



8-Lead SOIC

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in figures 7 through 10.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient (figure 2)		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 Lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in figure 3.

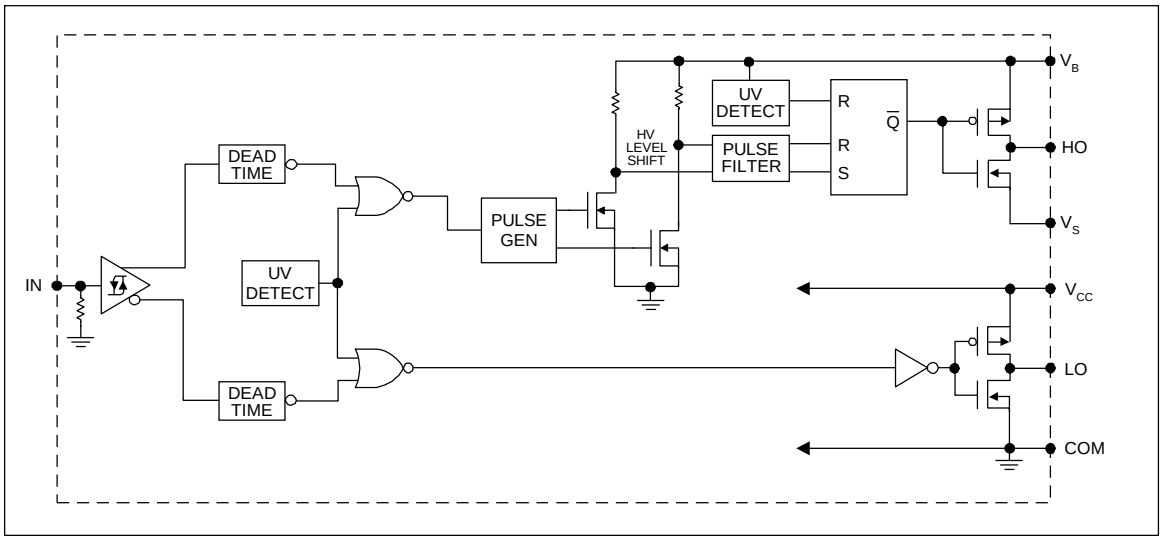
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	750	1,000	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	150	180		V_S = 600V
t_r	Turn-on rise time	—	80	130		
t_f	Turn-off fall time	—	40	65		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-off to LS turn-on	—	650	900		
MT	Delay matching, HS & LS turn-on/off	—	30	—		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” input voltage for HO & logic “0” for LO	6.4	—	—	V	V_{CC} = 10V
		9.5	—	—		V_{CC} = 15V
		12.6	—	—		V_{CC} = 20V
V_{IL}	Logic “0” input voltage for HO & logic “1” for LO	—	—	3.8		V_{CC} = 10V
		—	—	6.0		V_{CC} = 15V
		—	—	8.3		V_{CC} = 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	100	mV	I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	100		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	—	50	100		V_{IN} = 0V or V_{CC}
I_{QCC}	Quiescent V_{CC} supply current	—	70	180		V_{IN} = 0V or V_{CC}
I_{IN+}	Logic “1” input bias current	—	30	50		V_{IN} = V_{CC}
I_{IN-}	Logic “0” input bias current	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	7.6	8.6	9.6	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.2	8.2	9.2		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	7.6	8.6	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.2	8.2	9.2		
I_{O+}	Output high short circuit pulsed current	200	250	—	mA	V_O = 0V, V_{IN} = V_{CC} PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	420	500	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

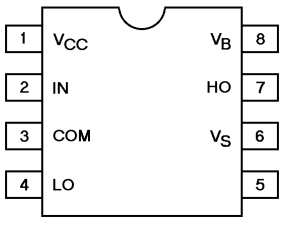
Functional Block Diagram



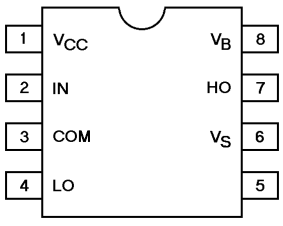
Lead Definitions

Symbol	Description
IN	Logic input for high side and low side gate driver outputs (HO & LO), in phase with HO
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



8 Lead DIP



8 Lead SOIC

IR2111	IR2111S
Part Number	

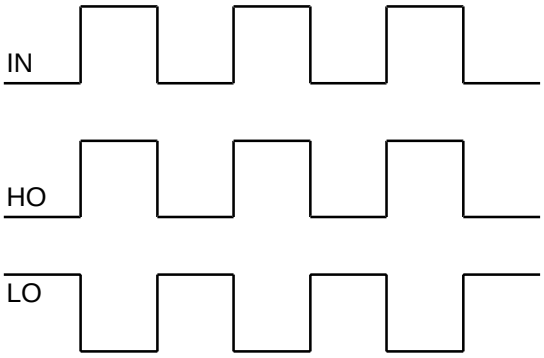


Figure 1. Input/Output Timing Diagram

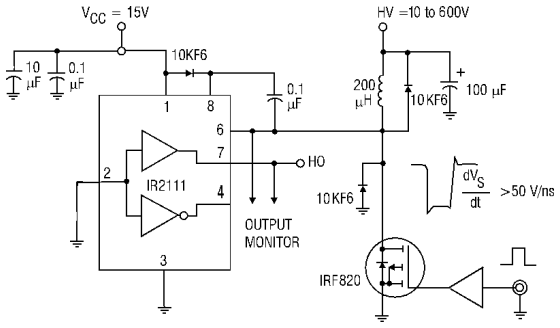


Figure 2. Floating Supply Voltage Transient Test Circuit

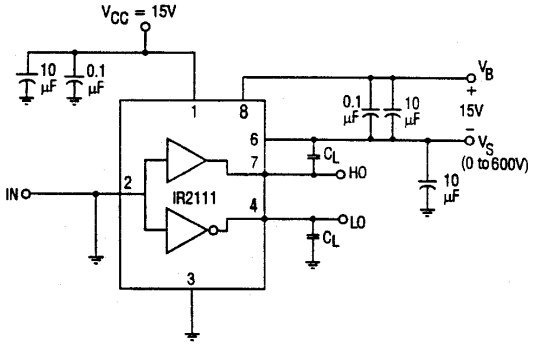


Figure 3. Switching Time Test Circuit

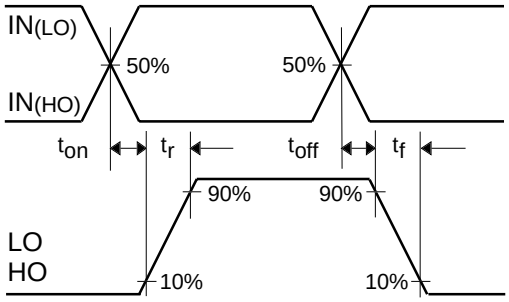


Figure 4. Switching Time Waveform Definition

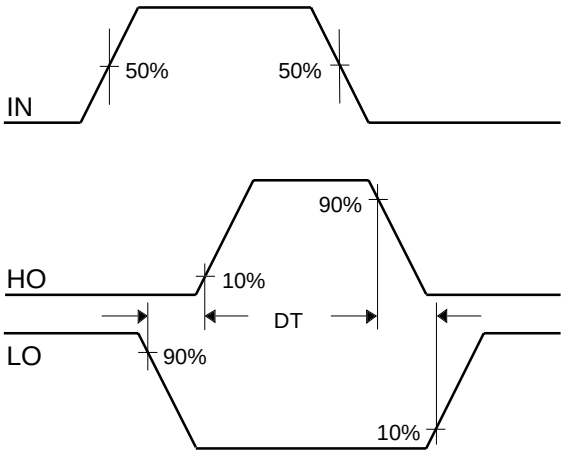


Figure 5. Deadtime Waveform Definitions

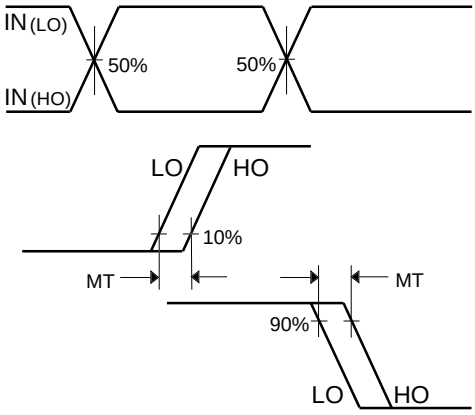


Figure 6. Delay Matching Waveform Definitions

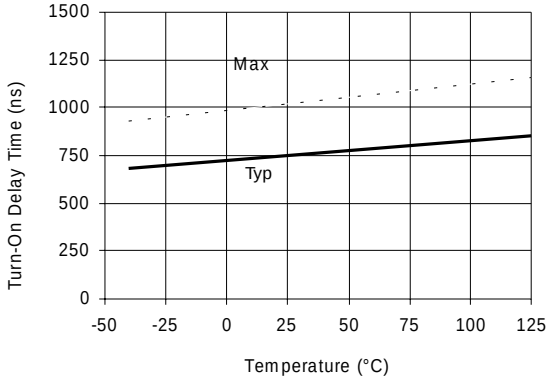


Figure 11A Turn-On Time vs Temperature

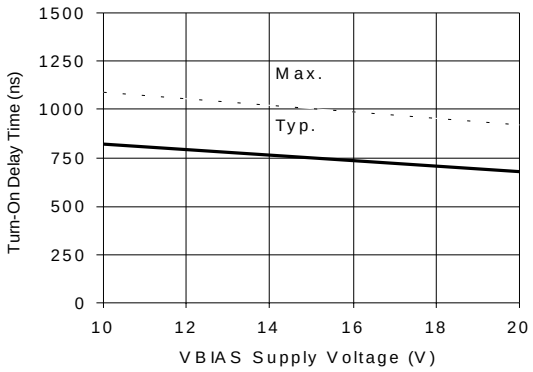


Figure 11B Turn-On Time vs Voltage

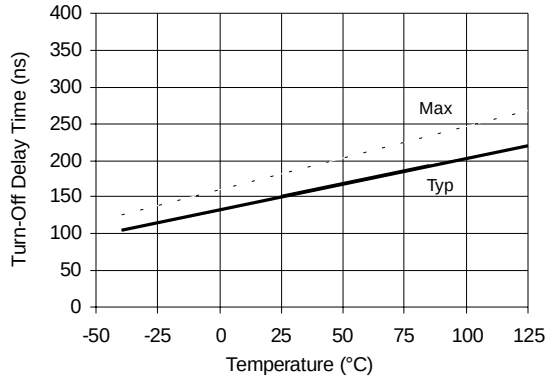


Figure 12A Turn-Off Time vs Temperature

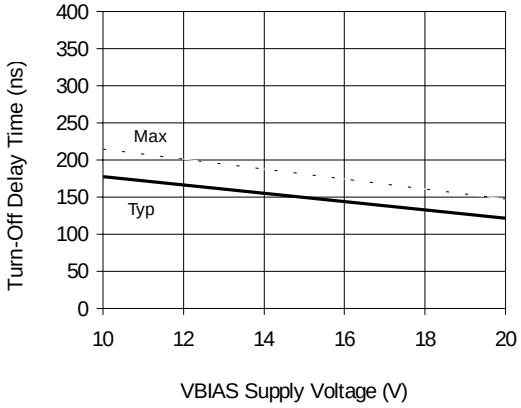


Figure 12B Turn-Off Time vs Voltage

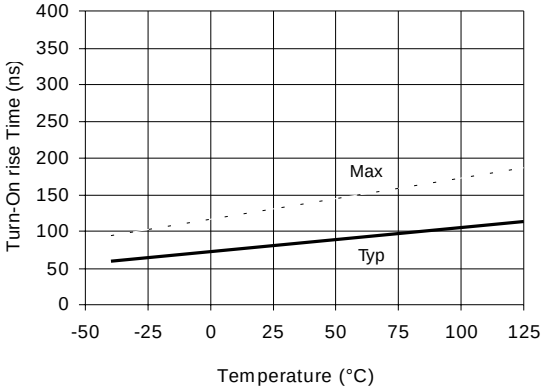


Figure 13A Turn-On RiseTime vs Temperature

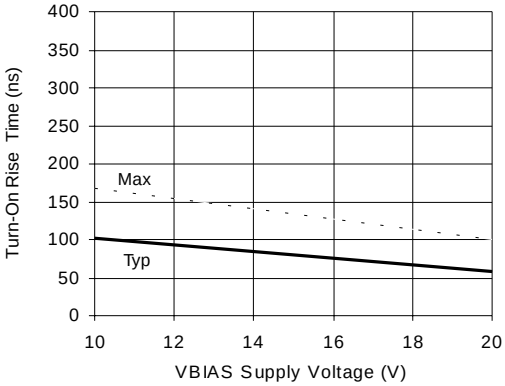


Figure 13B Turn-On RiseTime vs Voltage

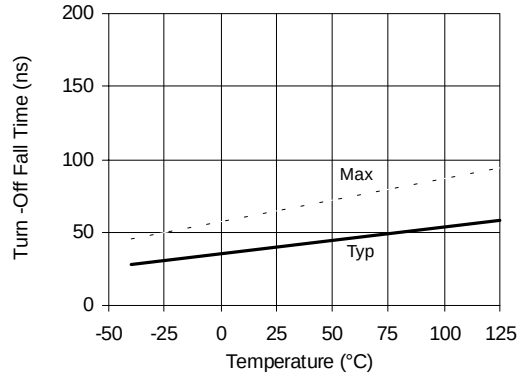


Figure 14A Turn-Off Fall Time vs Temperature

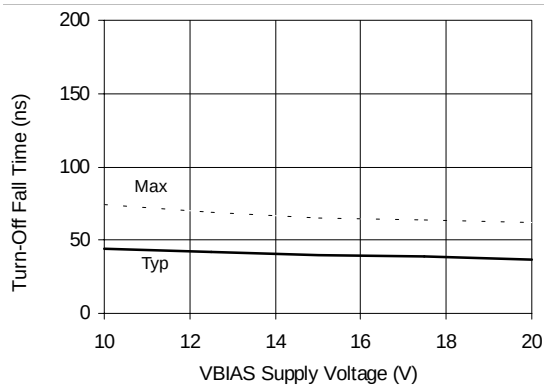


Figure 14B Turn-Off Fall Time vs Voltage

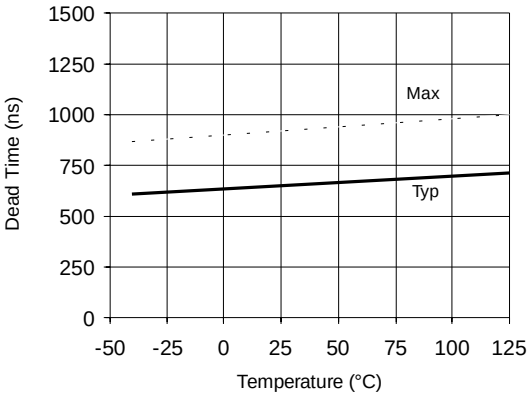


Figure 15A Dead Time vs Temperature

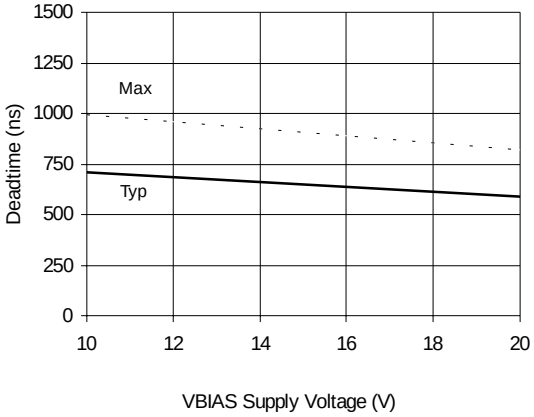


Figure 15B Dead Time vs Voltage

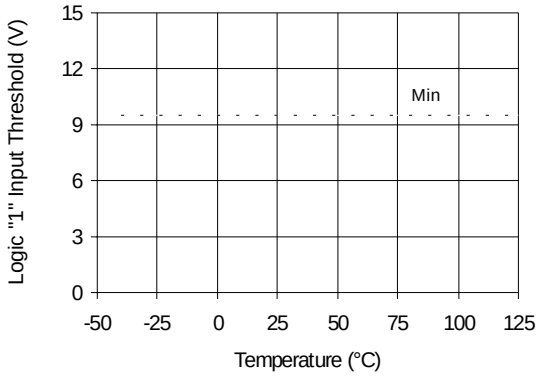


Figure 16A Logic “I” Input voltage for HO & Logic “0” for LO vs Temperature

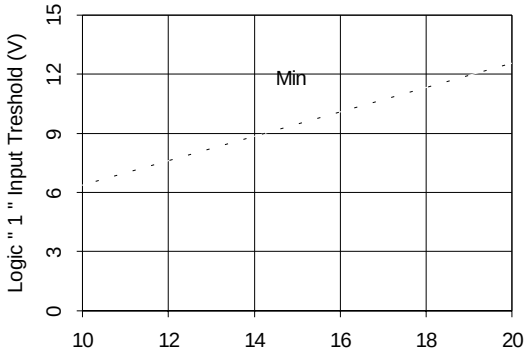


Figure 16B Logic “I” Input voltage for HO & Logic “0” for LO vs Voltage

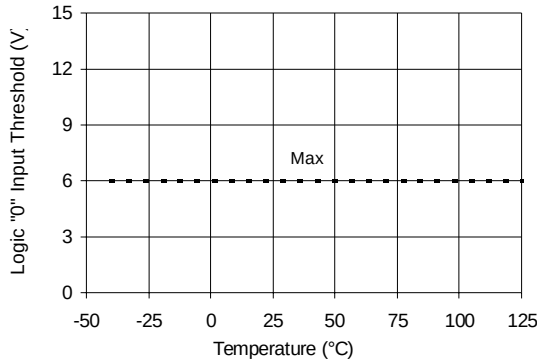


Figure 17A Logic "0" Input voltage for HO & Logic "I" for LO vs Temperature

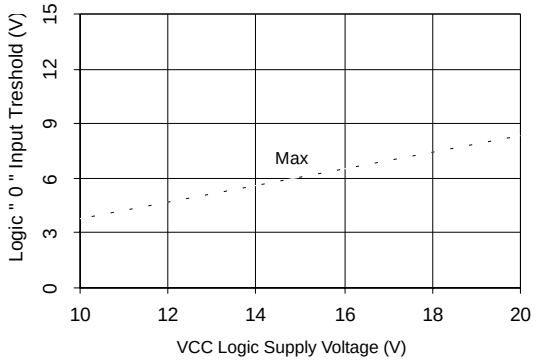


Figure 17B Logic "0" Input voltage for HO & Logic "I" for LO vs Voltage

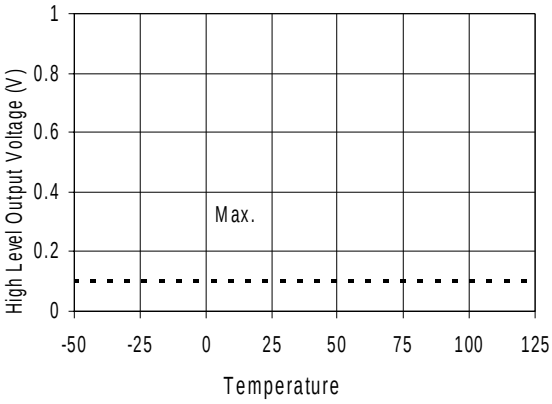


Figure 18A. High Level Output vs. Temperature

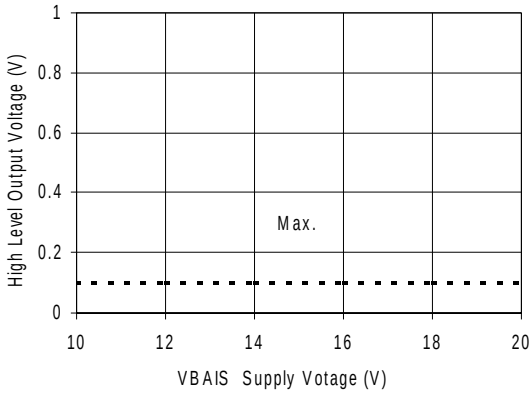


Figure 18B. High Level Output vs. Voltage

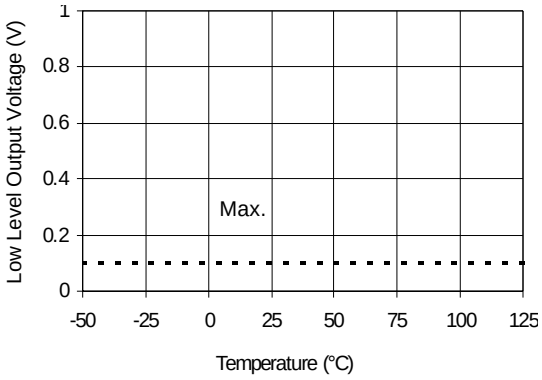


Figure 19A. Low Level Output vs. Temperature

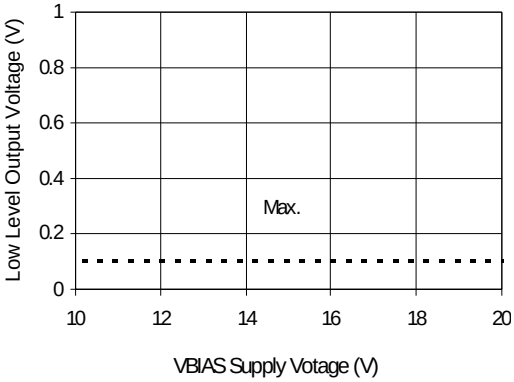


Figure 19B. Low Level Output vs. Voltage

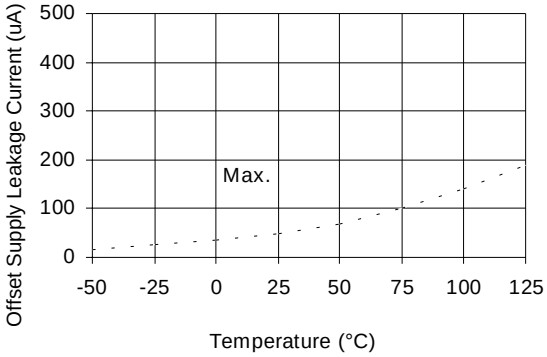


Figure 20A Offset Supply Current vs Temperature

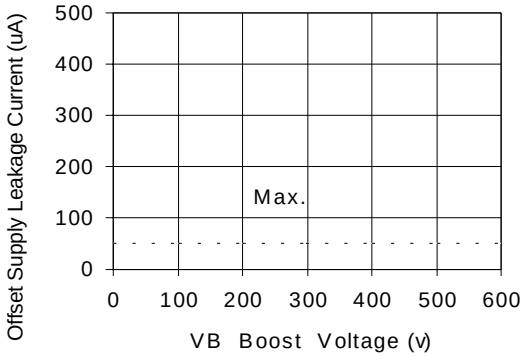


Figure 20B Offset Supply Current vs Voltage

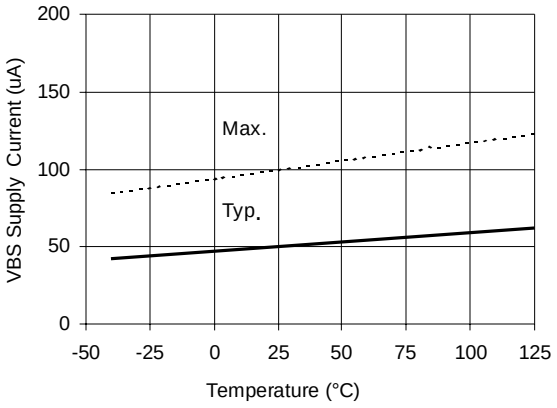


Figure 21A VBS Supply Current vs Temperature

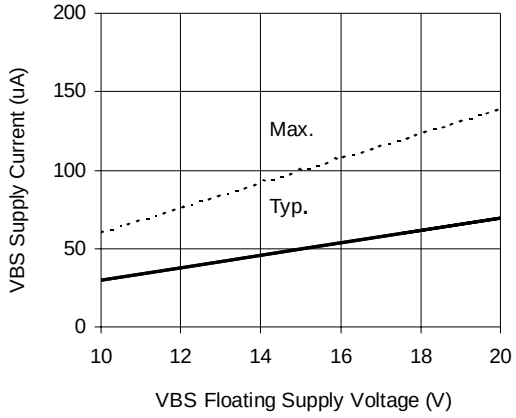


Figure 21B VBS Supply Current vs Voltage

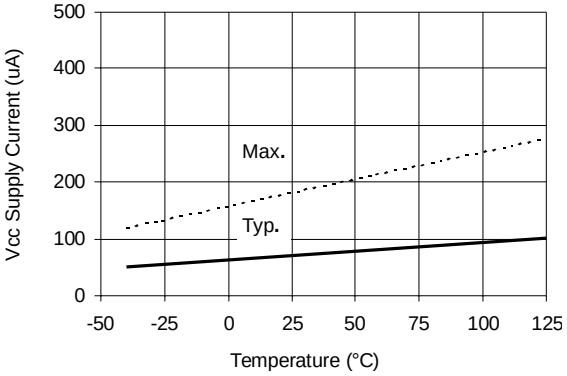


Figure 22A VCC Supply Current vs Temperature

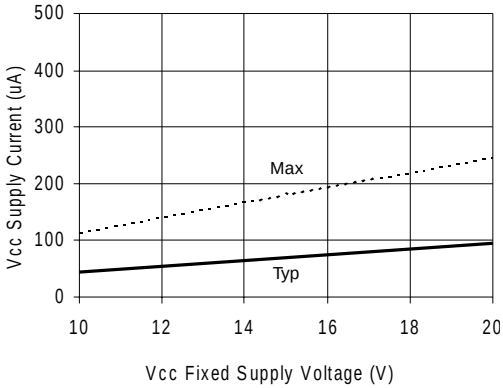


Figure 22B VCC Supply Current vs Voltage

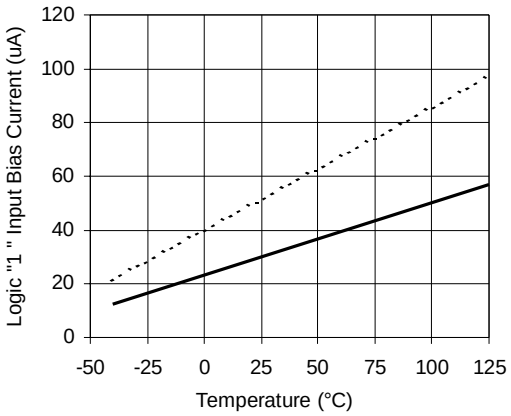


Figure 23A Logic "1" Input Current vs Temperature

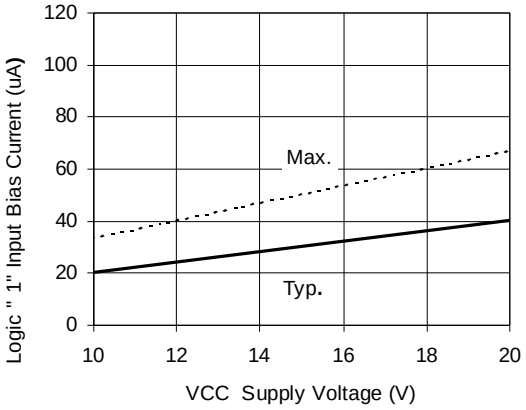


Figure 23B Logic "1" Input Current vs V_{CC} Voltage

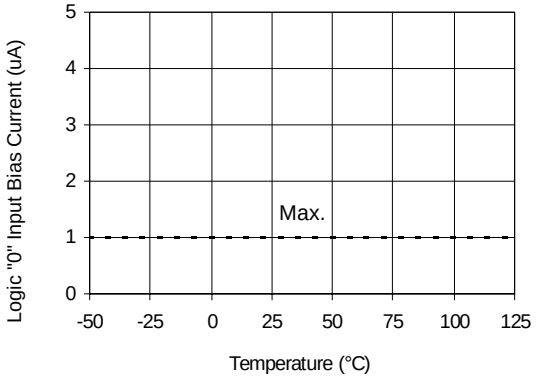


Figure 24A. Logic "0" Input Current vs. Temperature

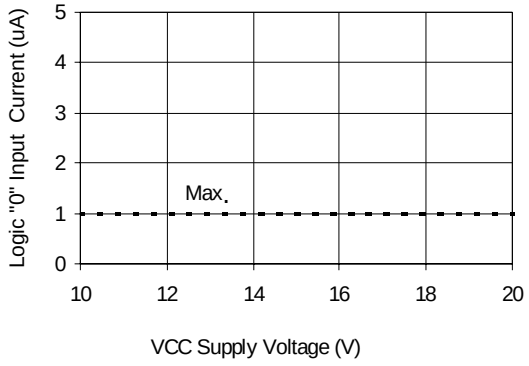


Figure 24B. Logic "0" Input Current vs. V_{CC} Voltage

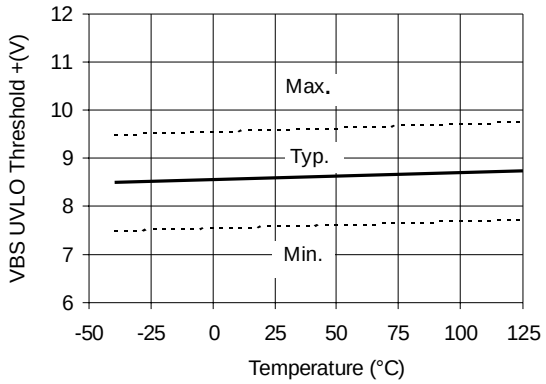


Figure 25 VBS Undervoltage Threshold (+) vsTemperature

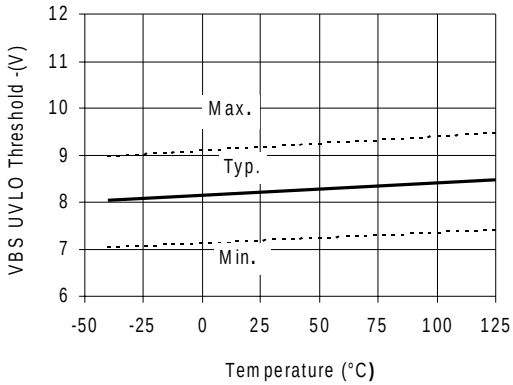


Figure 26 VBS Undervoltage Threshold (-) vsTemperature

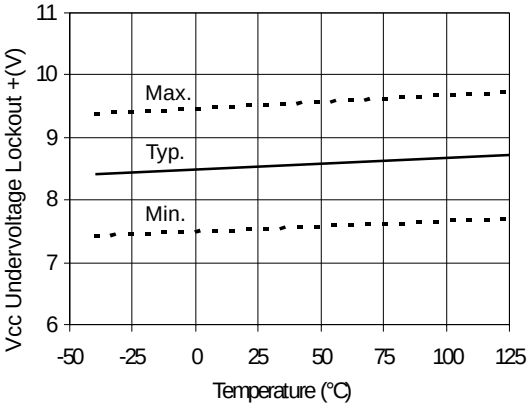


Figure 27 Vcc Undervoltage (-) vs Temperature

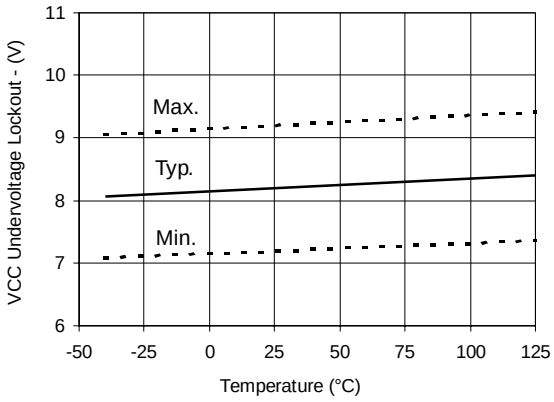


Figure 28 Vcc Undervoltage (-) vs Temperature

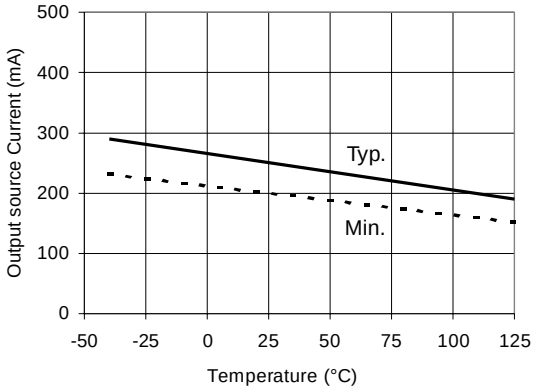


Figure 29A Output Source Current vs Temperature

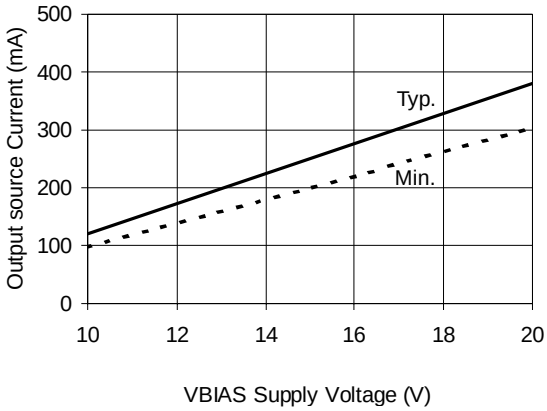


Figure 29B Output Source Current vs Voltage

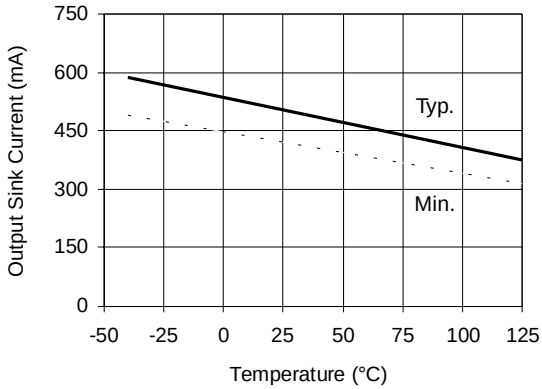


Figure 30A Output Sink Current vs Temperature

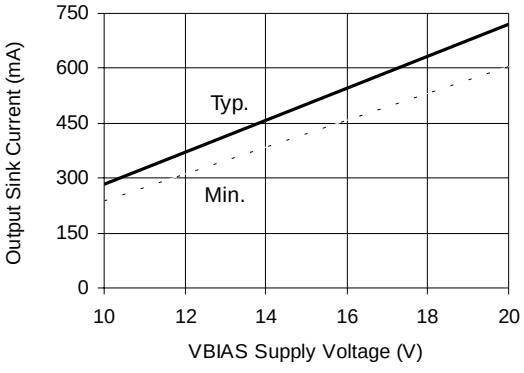


Figure 30B Output Sink Current vs Voltage

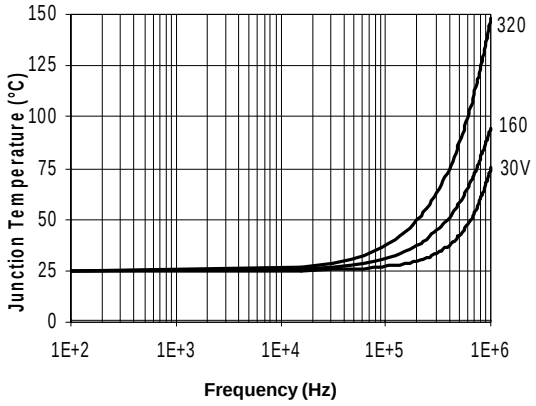


Figure 31. IR2111 T_J vs. Frequency (IRFBC20)
R_{GATE} = 33Ω, V_{CC} = 15V

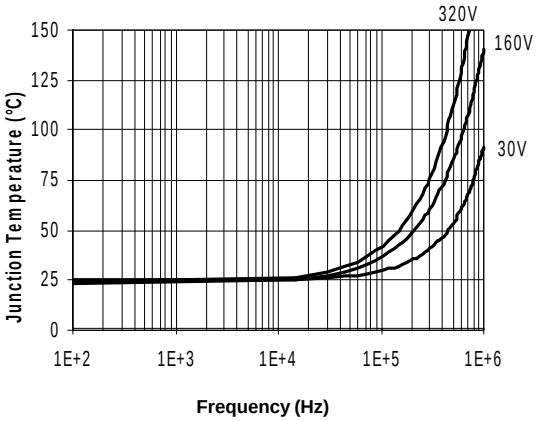


Figure 32. IR2111 T_J vs. Frequency (IRFBC30)
R_{GATE} = 22Ω, V_{CC} = 15V

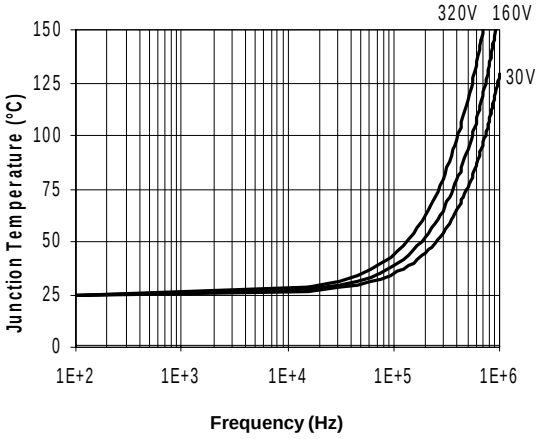


Figure33. IR2111 T_J vs. Frequency (IRFBC40)
R_{GATE} = 15Ω, V_{CC} = 15V

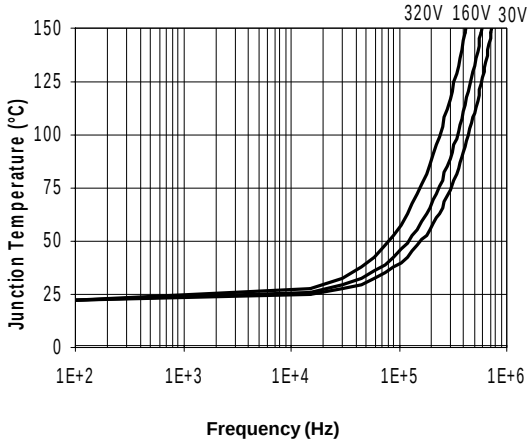


Figure 34. IR2111 T_J vs. Frequency (IRFPC50)
R_{GATE} = 10Ω, V_{CC} = 15V

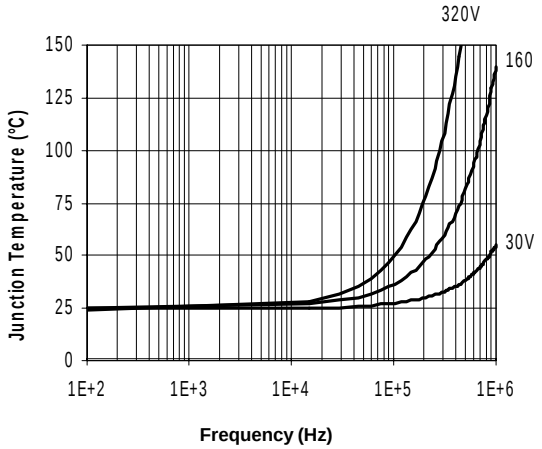


Figure 35. IR2111S T_J vs. Frequency (IRFBC20)
R_{GATE} = 33Ω, V_{CC} = 15V

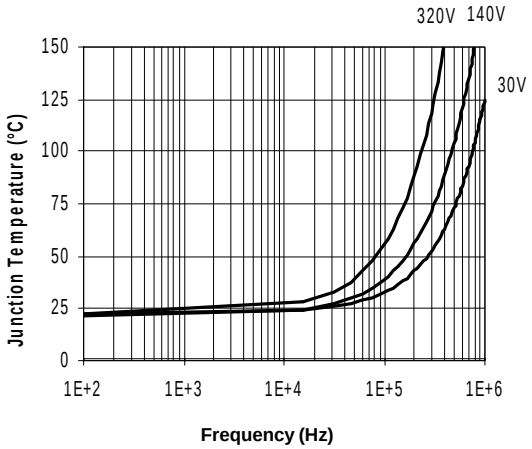


Figure 36. IR2111S T_J vs. Frequency (IRFBC30)
R_{GATE} = 22Ω, V_{CC} = 15V

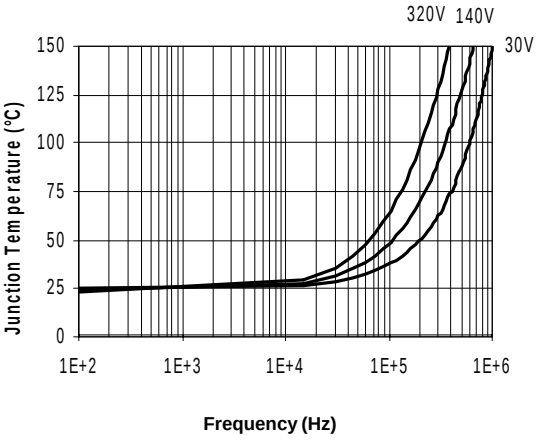


Figure 37. IR2111S T_J vs. Frequency (IRFBC40)
R_{GATE} = 15Ω, V_{CC} = 15V

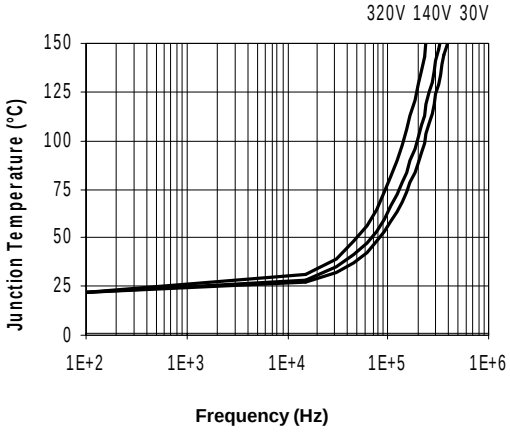
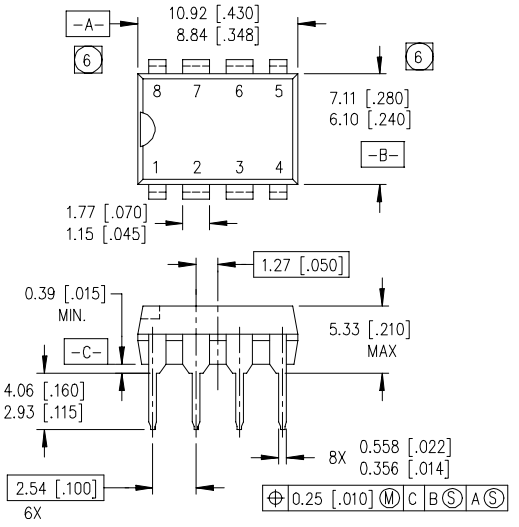


Figure 38. IR2111S T_J vs. Frequency (IRFPC50)
R_{GATE} = 10Ω, V_{CC} = 15V

Case outlines

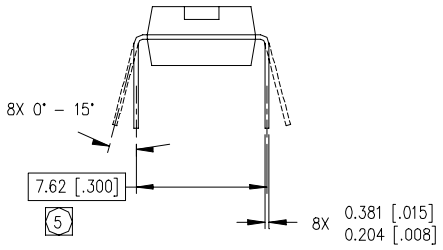


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.

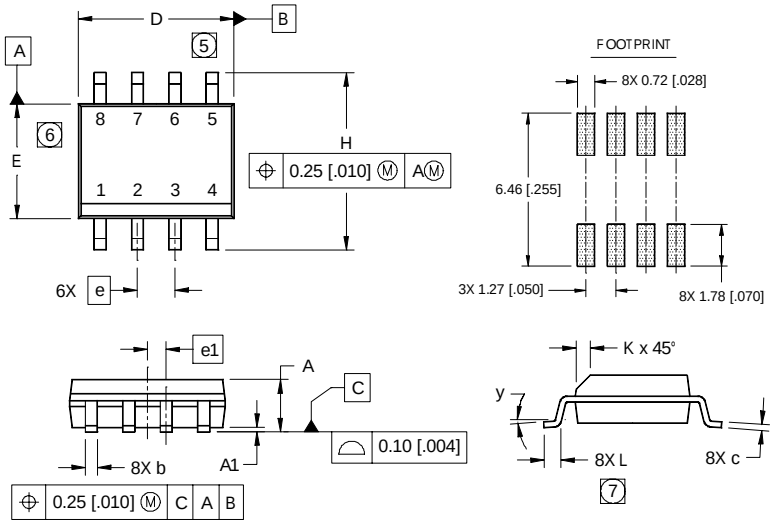
(5) MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8-Lead PDIP

01-6014
01-3003 01 (MS-001AB)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

(5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

(6) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

(7) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8-Lead SOIC

01-6027
01-0021 11 (MS-012AA)

6/21/2001

International
IOR Rectifier

Data Sheet No. PD60026-N

IR2112(S)

HIGH AND LOW SIDE DRIVER

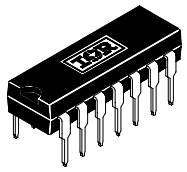
Features

- Floating channel designed for bootstrap operation
- Fully operational to +600V
- Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
  Separate logic supply range from 3.3V to 20V
  Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

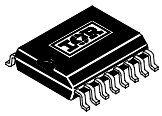
Product Summary

V_{OFFSET}	600V max.
I_O+/-	200 mA / 420 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	125 & 105 ns
Delay Matching	30 ns

Packages



14-Lead PDIP

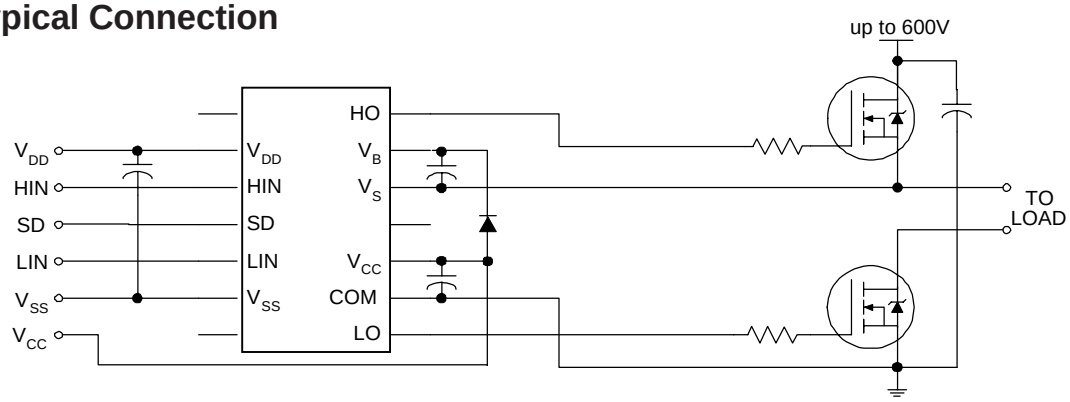


16-Lead SOIC
(wide body)

Description

The IR2112(S) is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	-0.3	625	V
V_S	High Side Floating Supply Offset Voltage	V_B - 25	V_B + 0.3	
V_{HO}	High Side Floating Output Voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low Side Fixed Supply Voltage	-0.3	25	
V_{LO}	Low Side Output Voltage	-0.3	V_{CC} + 0.3	
V_{DD}	Logic Supply Voltage	-0.3	V_{SS} + 25	
V_{SS}	Logic Supply Offset Voltage	V_{CC} - 25	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS} - 0.3	V_{DD} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient (Figure 2)	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$ (14 Lead DIP)	—	1.6	W
	(16 Lead SOIC)	—	1.25	
R_{THJA}	Thermal Resistance, Junction to Ambient (14 Lead DIP)	—	75	°C/W
	(16 Lead SOIC)	—	100	
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figures 36 and 37.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Absolute Voltage	V_S + 10	V_S + 20	V
V_S	High Side Floating Supply Offset Voltage	Note 1	600	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Low Side Fixed Supply Voltage	10	20	
V_{LO}	Low Side Output Voltage	0	V_{CC}	
V_{DD}	Logic Supply Voltage	V_{SS} + 3	V_{SS} + 20	
V_{SS}	Logic Supply Offset Voltage	-5 (Note 2)	5	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Note 2: When $V_{DD} < 5V$, the minimum V_{SS} offset is limited to $-V_{DD}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

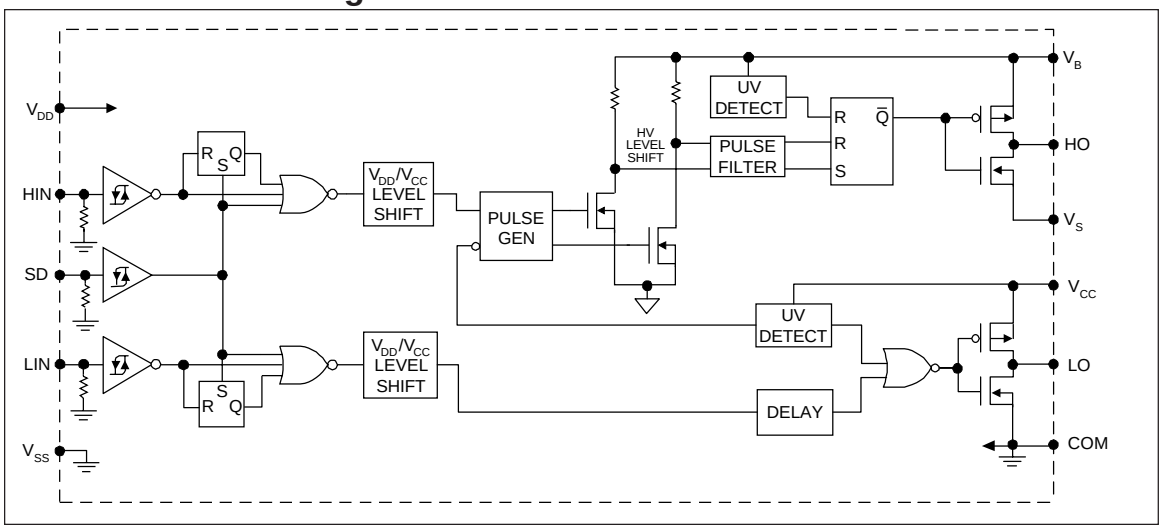
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	7	—	125	180	ns	V_S = 0V
t_{off}	Turn-Off Propagation Delay	8	—	105	160		V_S = 600V
t_{sd}	Shutdown Propagation Delay	9	—	105	160		V_S = 600V
t_r	Turn-On Rise Time	10	—	80	130		
t_f	Turn-Off Fall Time	11	—	40	65		
MT	Delay Matching, HS & LS Turn-On/Off	—	—	—	30		Figure 5

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” Input Voltage	12	9.5	—	—	V	
V_{IL}	Logic “0” Input Voltage	13	—	—	6.0		
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	14	—	—	100	mV	I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	15	—	—	100		I_O = 0A
I_{LK}	Offset Supply Leakage Current	16	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} Supply Current	17	—	25	60		V_{IN} = 0V or V_{DD}
I_{QCC}	Quiescent V_{CC} Supply Current	18	—	80	180		V_{IN} = 0V or V_{DD}
I_{QDD}	Quiescent V_{DD} Supply Current	19	—	2.0	5.0		V_{IN} = 0V or V_{DD}
I_{IN+}	Logic “1” Input Bias Current	20	—	20	40		V_{IN} = V_{DD}
I_{IN-}	Logic “0” Input Bias Current	21	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	22	7.4	8.5	9.6	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	23	7.0	8.1	9.2		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	24	7.6	8.6	9.6		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	25	7.2	8.2	9.2		
I_{O+}	Output High Short Circuit Pulsed Current	26	200	250	—	mA	V_O = 0V, V_{IN} = V_{DD} PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	27	420	500	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

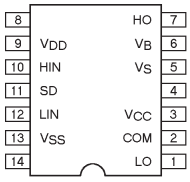
Functional Block Diagram



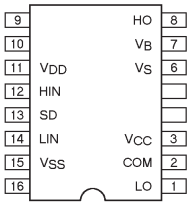
Lead Definitions

Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



14 Lead DIP



16 Lead SOIC (Wide Body)

IR2112	IR2112S
Part Number	

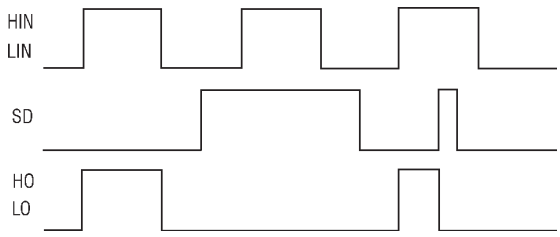


Figure 1. Input/Output Timing Diagram

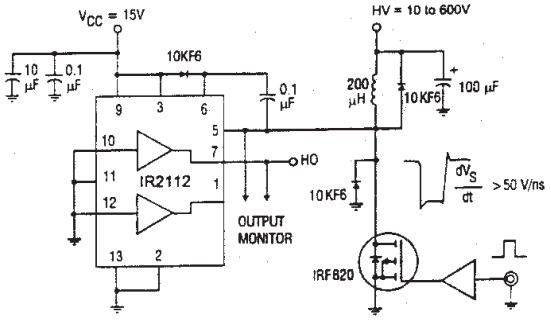


Figure 2. Floating Supply Voltage Transient Test Circuit

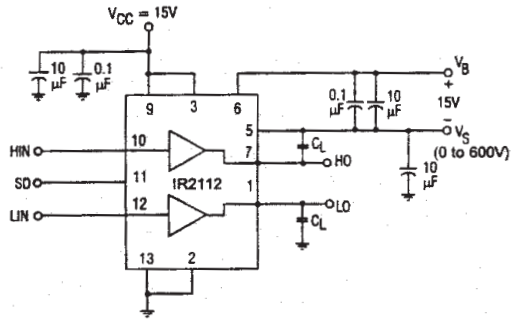


Figure 3. Switching Time Test Circuit

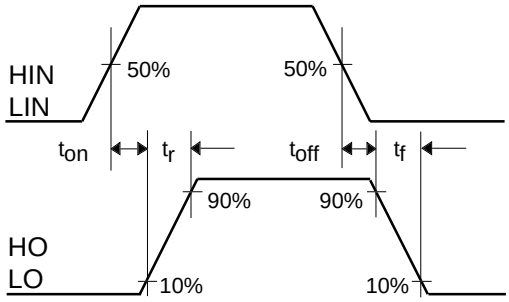


Figure 4. Switching Time Waveform Definition

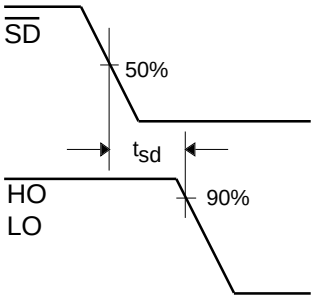


Figure 5. Shutdown Waveform Definitions

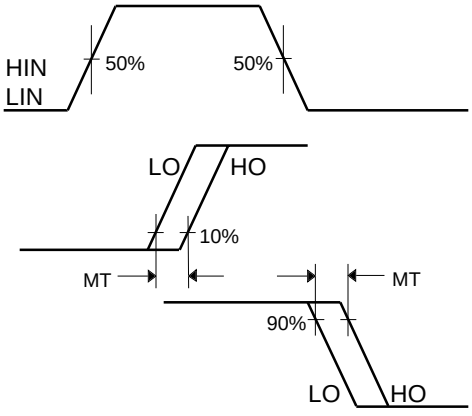


Figure 6. Delay Matching Waveform Definitions

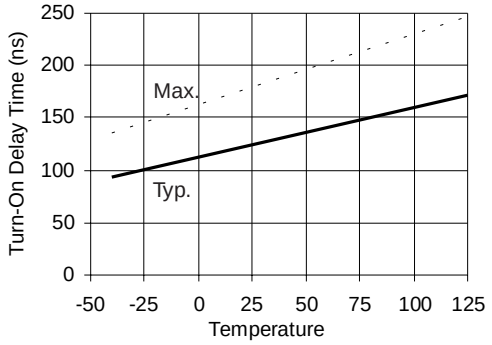


Figure 7A. Turn-On Time vs. Temperature

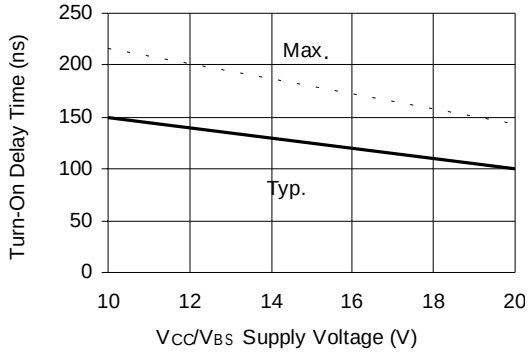


Figure 7B. Turn-On Time vs. VCC/VBS Supply Voltage

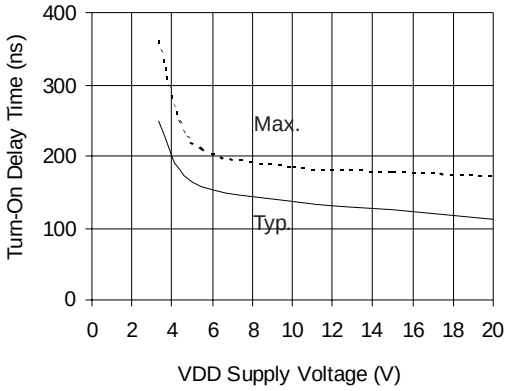


Figure 7C. Turn-On Time vs. VDD Supply Voltage

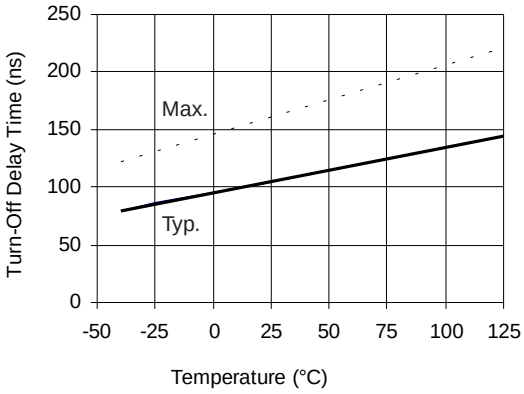


Figure 8A. Turn-Off Time vs. Temperature

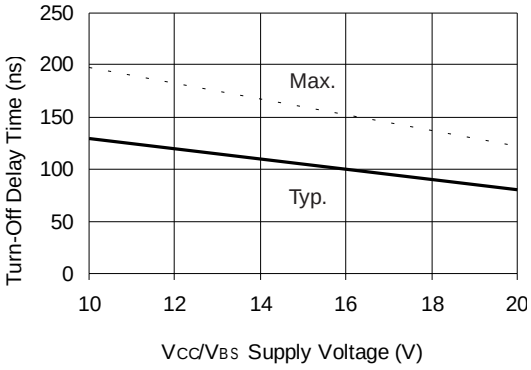


Figure 8B. Turn-Off Time vs. VCC/VBS Supply Voltage

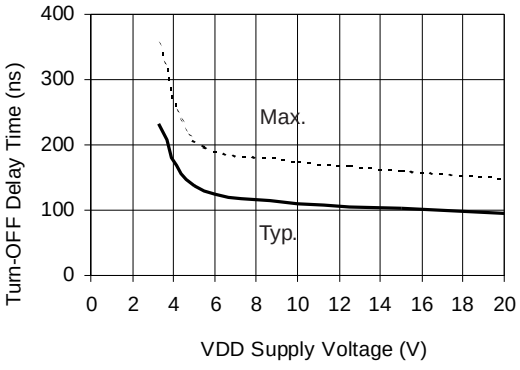


Figure 8C. Turn-Off Time vs. VDD Supply Voltage

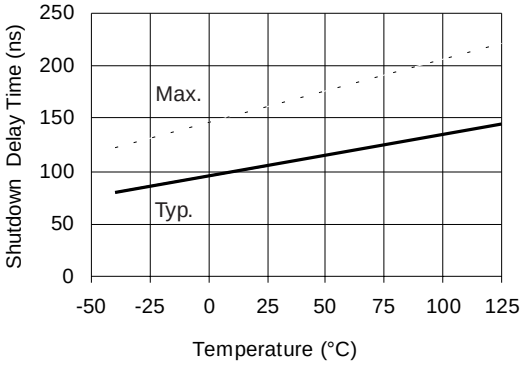


Figure 9A. Shutdown Time vs. Temperature

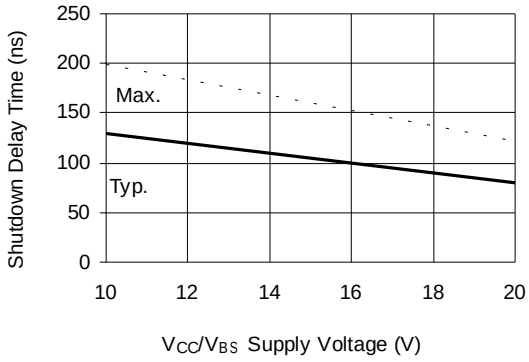


Figure 9B. Shutdown Delay Time vs. V_{CC}/V_{BS} Supply Voltage

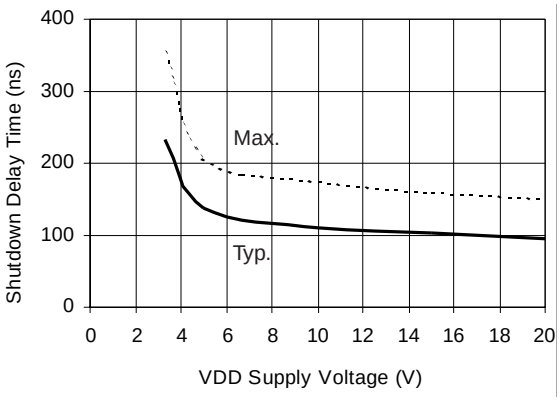


Figure 9C. Shutdown Time vs. V_{DD} Supply Voltage

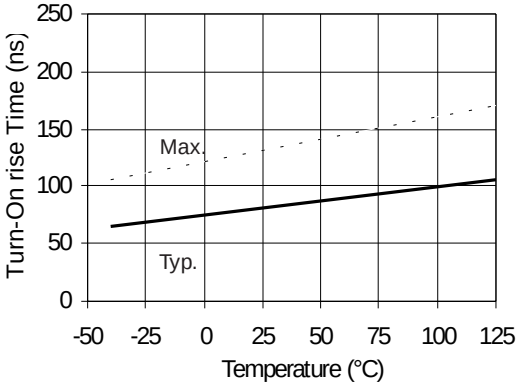


Figure 10A. Turn-On Rise Time vs. Temperature

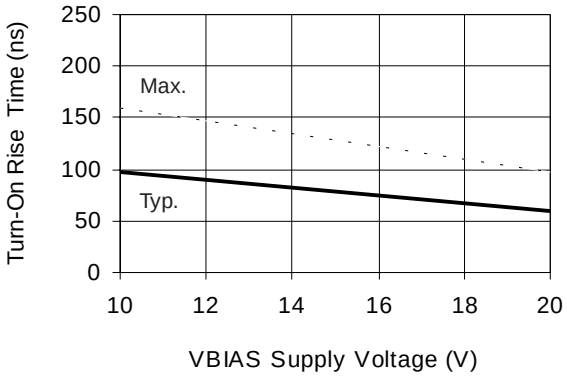


Figure 10B. Turn-On Rise Time vs. Voltage

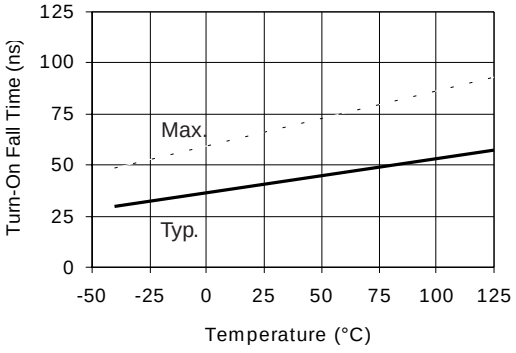


Figure 11A Turn-On Fall Time vs. Temperature

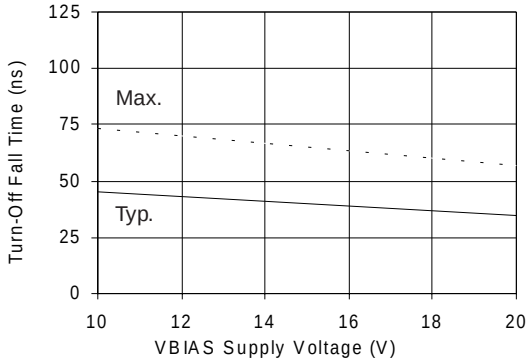


Figure 11B. Turn-Off Fall Time vs. Voltage

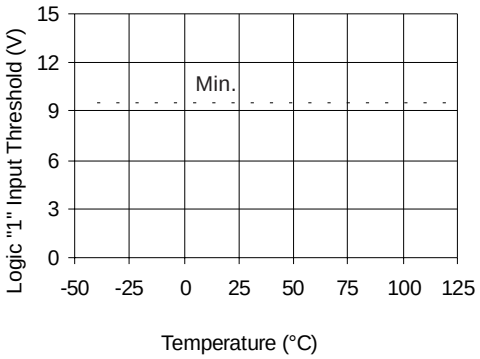


Figure 12A. Logic "I" Input Threshold vs. Temperature

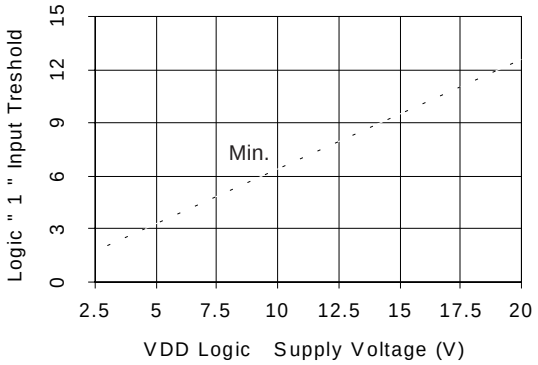


Figure 12B. Logic "I" Input Threshold vs. Voltage

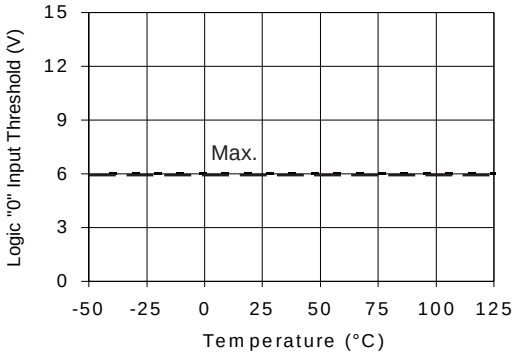


Figure 13A. Logic "0" Input Threshold vs. Temperature

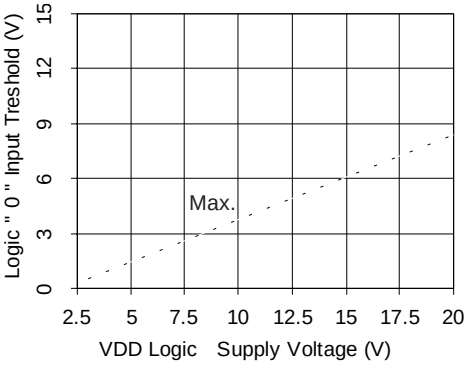


Figure 13B. Logic "0" Input Threshold vs. Voltage

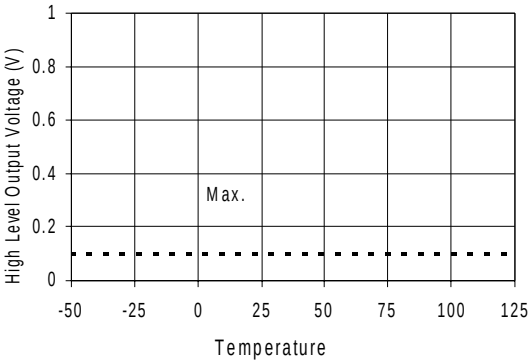


Figure 14A. High Level Output vs. Temperature

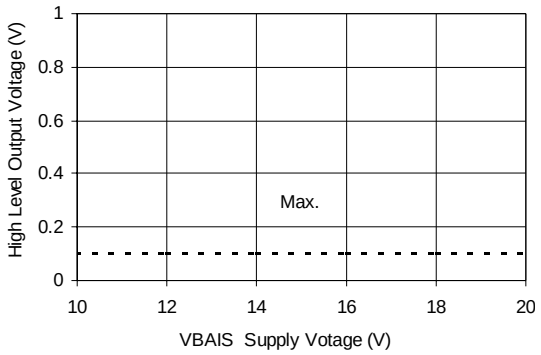


Figure 14B. High Level Output vs. Voltage

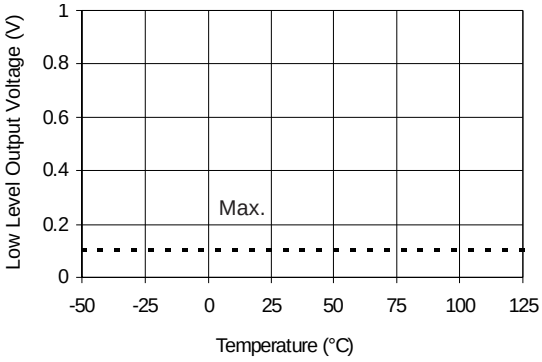


Figure 15A. Low Level Output vs. Temperature

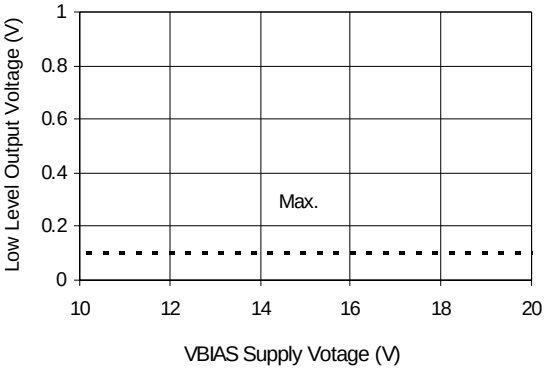


Figure 15B. Low Level Output vs. Voltage

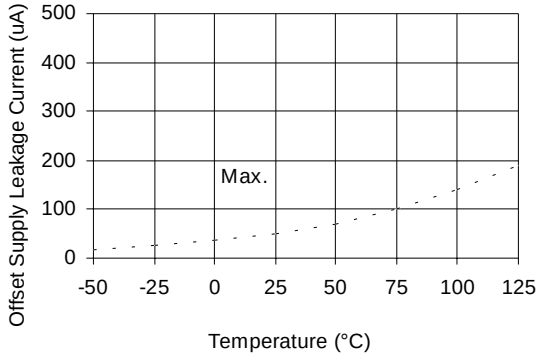


Figure 16A. Offset Supply Current vs. Temperature

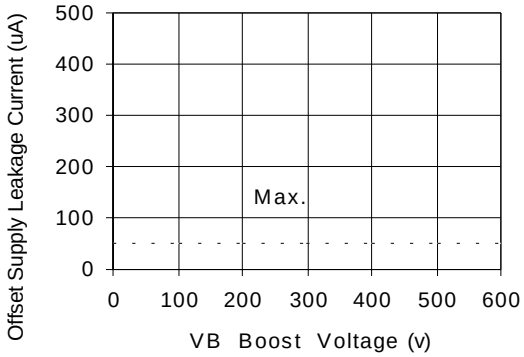


Figure 16B. Offset Supply Current vs. Voltage

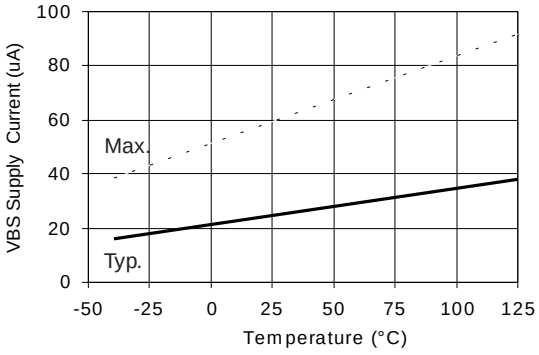


Figure 17A. V_{BS} Supply Current vs. Temperature

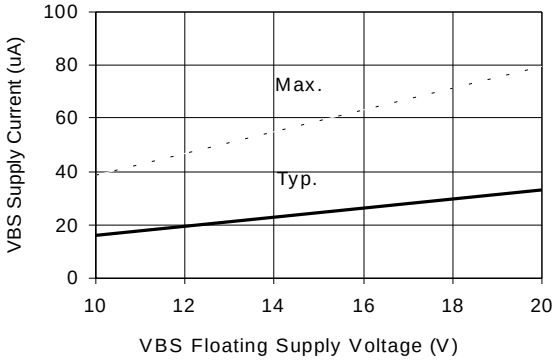


Figure 17B. V_{BS} Supply Current vs. Voltage

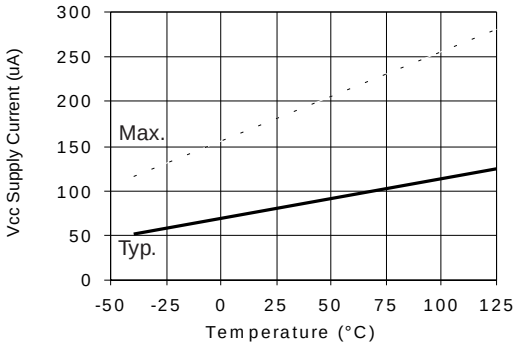


Figure 18A. V_{CC} Supply Current vs. Temperature

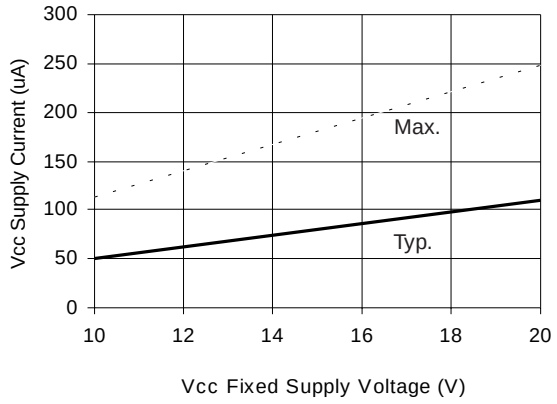


Figure 18B. V_{CC} Supply Current vs. Voltage

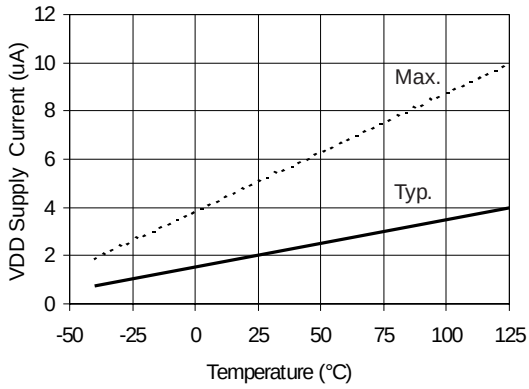


Figure 19A. V_{DD} Supply Current vs. Temperature

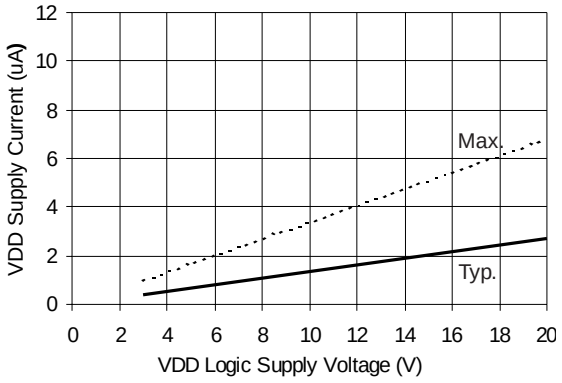


Figure 19B. V_{DD} Supply Current vs. V_{DD} Voltage

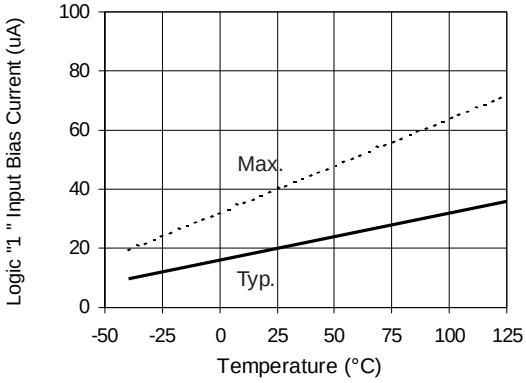


Figure 20A. Logic "I" Input Current vs. Temperature

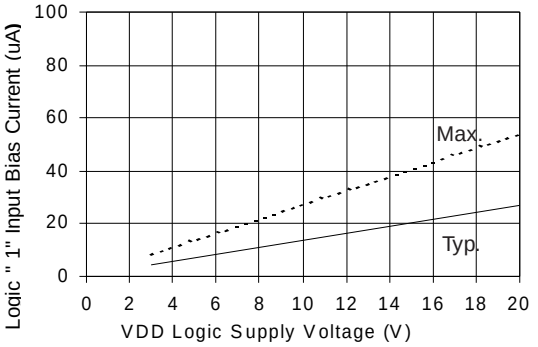


Figure 20B. Logic "1" Input Current vs. V_{DD} Voltage

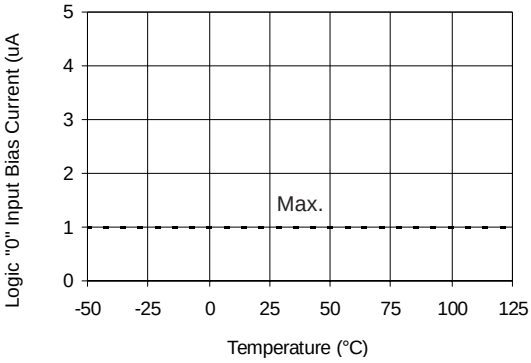


Figure 21A. Logic "0" Input Current vs. Temperature

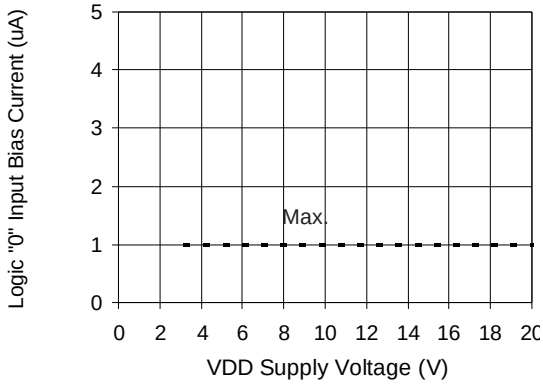


Figure 21B. Logic "0" Input Current vs. V_{DD} Voltage

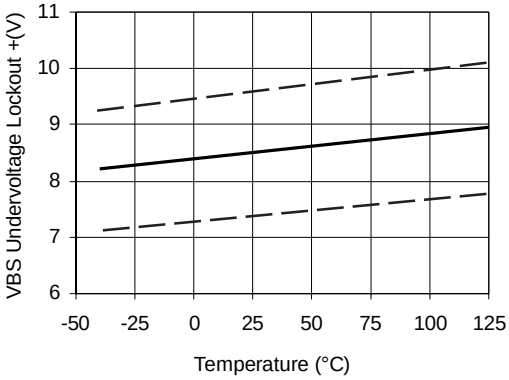


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

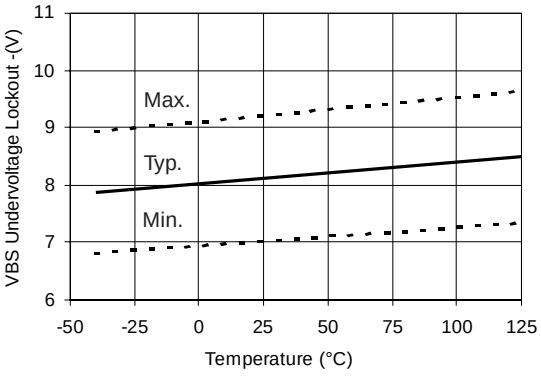


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

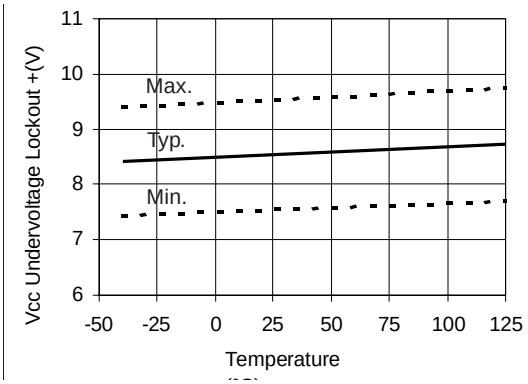


Figure 24. V_{CC} Undervoltage (-) vs. Temperature

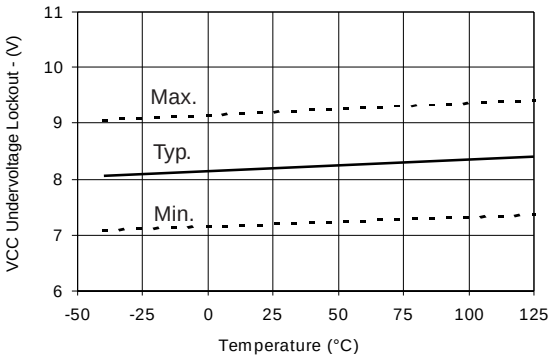


Figure 25. VCC Undervoltage (-) vs. Temperature

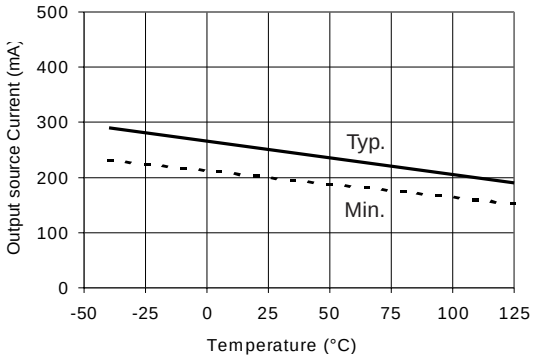


Figure 26A. Output Source Current vs. Temperature

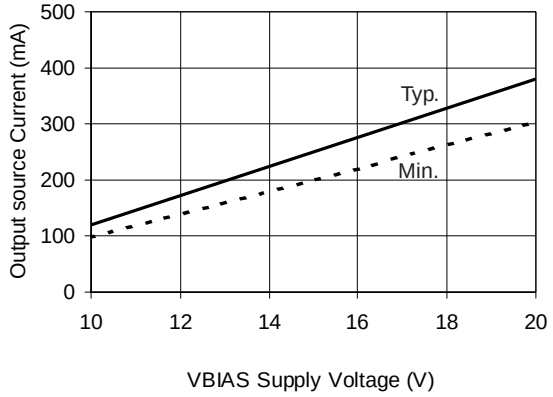


Figure 26B. Output Source Current vs. Voltage

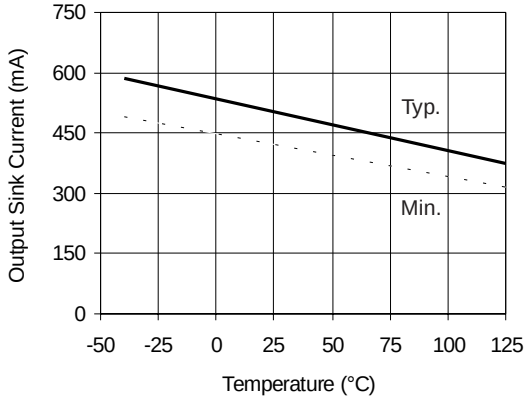


Figure 27A. Output Sink Current vs. Temperature

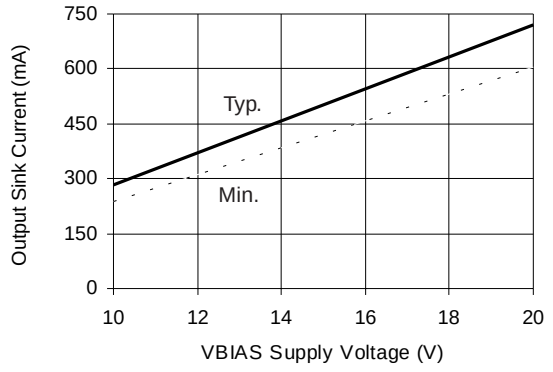


Figure 27B. Output Sink Current vs. Voltage

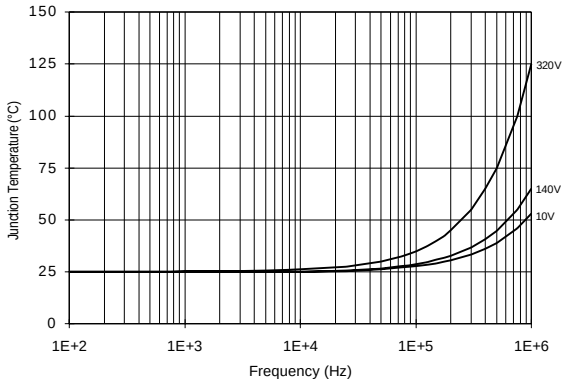


Figure 28. IR2112 T_J vs. Frequency (IRFBC20)
R_{GATE} = 33Ω, V_{CC} = 15V

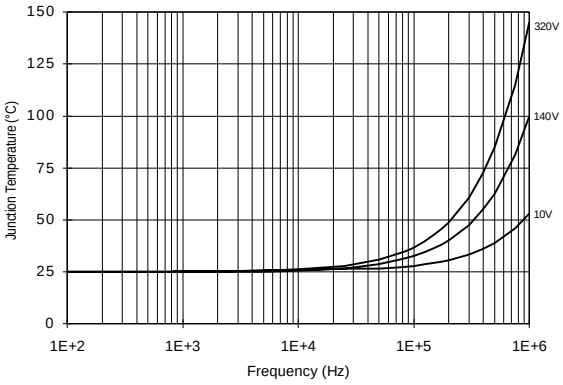


Figure 29. IR2112 T_J vs. Frequency (IRFBC30)
R_{GATE} = 22Ω, V_{CC} = 15V

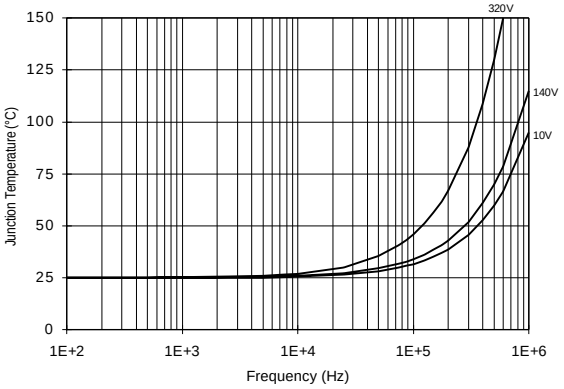


Figure 30. IR2112 T_J vs. Frequency (IRFBC40)
R_{GATE} = 15Ω, V_{CC} = 15V

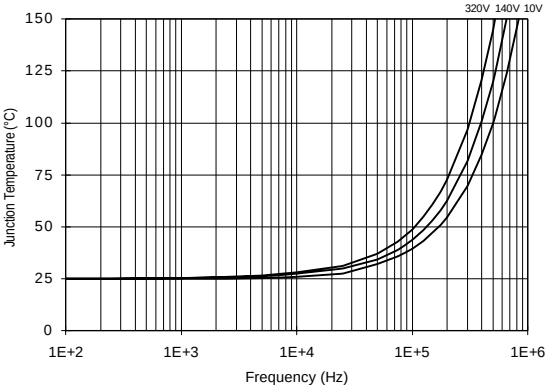


Figure 31. IR2112 T_J vs. Frequency (IRFPE50)
R_{GATE} = 10Ω, V_{CC} = 15V

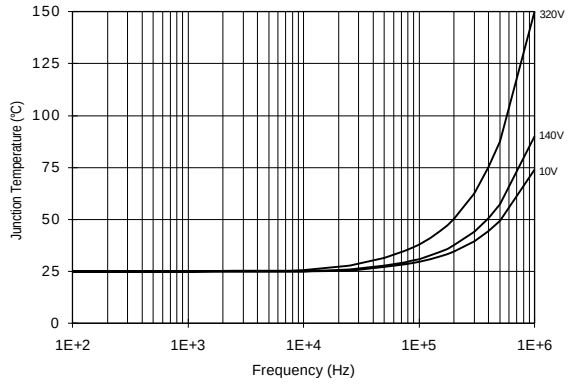


Figure 32. IR2112S T_J vs. Frequency (IRFBC20)
R_{GATE} = 33Ω, V_{CC} = 15V

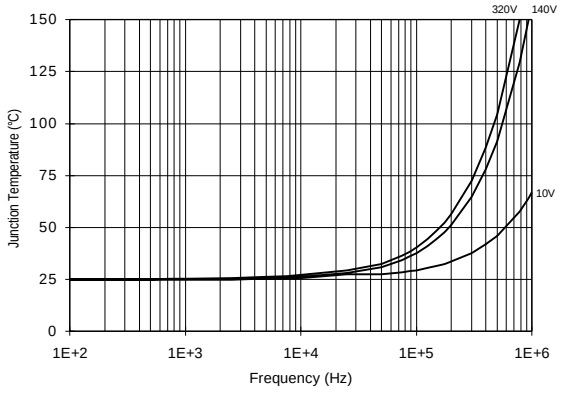


Figure 33. IR2112S T_J vs. Frequency (IRFBC30)
R_{GATE} = 22Ω, V_{CC} = 15V

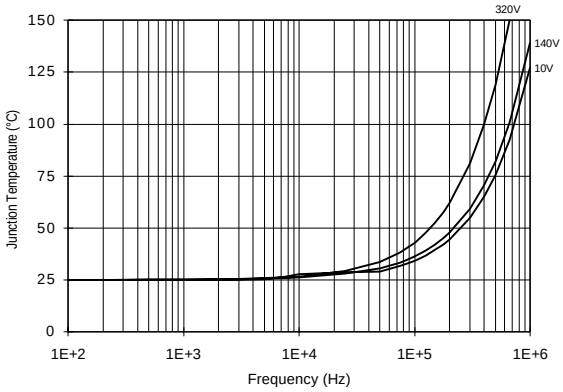


Figure 34. IR2112S T_J vs. Frequency (IRFBC40)
R_{GATE} = 15Ω, V_{CC} = 15V

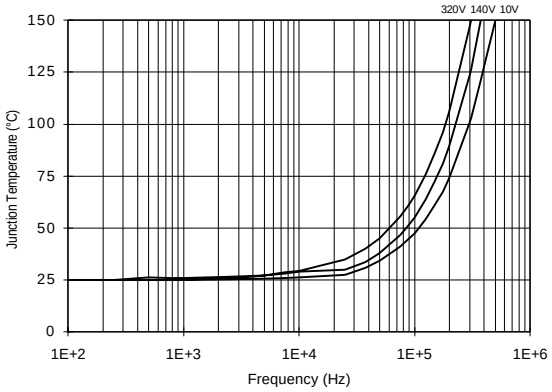


Figure 35. IR2112S T_J vs. Frequency (IRFPE50)
R_{GATE} = 10Ω, V_{CC} = 15V

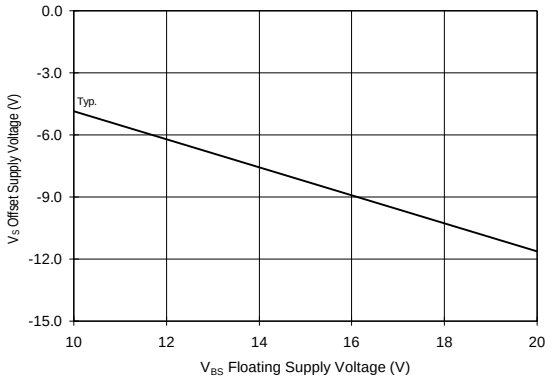


Figure 36. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

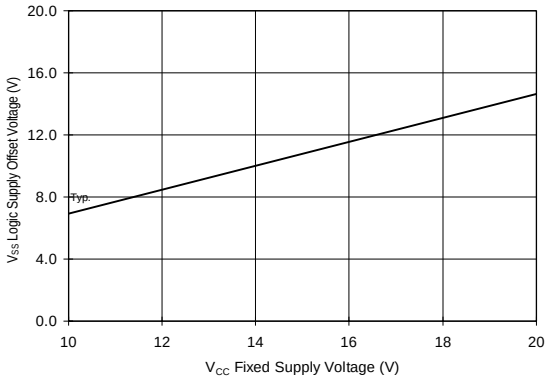
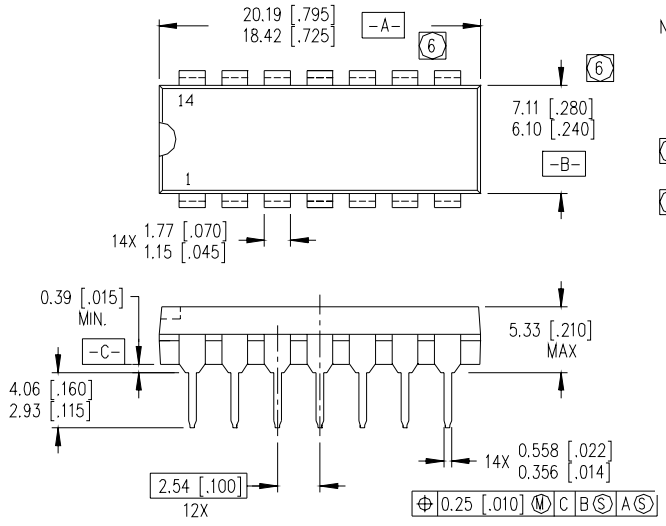
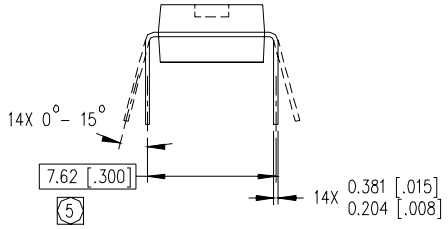


Figure 37. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage

Case outline

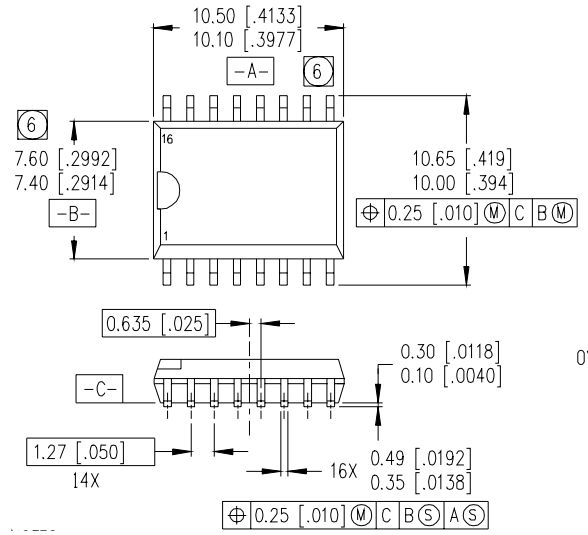


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

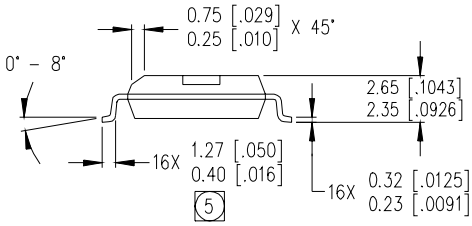


14-Lead PDIP

01-6010
01-3002 03 (MS-001AC)



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AA.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



16-Lead SOIC (wide body)

01 6015
01-3014 03 (MS-013AA)

International
IOR Rectifier

IR2117/IR2118 (S)

SINGLE CHANNEL DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- CMOS Schmitt-triggered inputs with pull-down
- Output in phase with input (IR2117) or out of phase with input (IR2118)

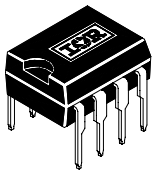
Product Summary

V_{OFFSET}	600V max.
I_O+/-	200 mA / 420 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	125 & 105 ns

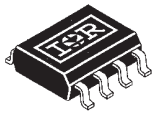
Description

The IR2117/IR2118(S) is a high voltage, high speed power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS outputs. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high or low side configuration which operates up to 600 volts.

Packages

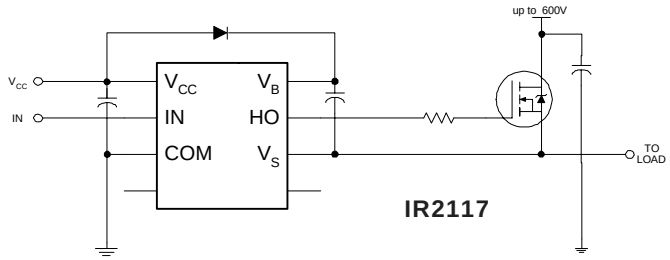


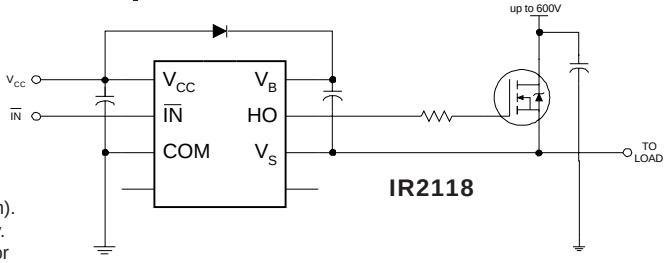
8-Lead PDIP
IR2117/IR2118



8-Lead SOIC
IR2117S/IR2118S

Typical Connection





(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 5 through 8.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Logic supply voltage		-0.3	25	
V_{IN}	Logic input voltage		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient (figure 2)		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Logic supply voltage	10	20	
V_{IN}	Logic input voltage	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

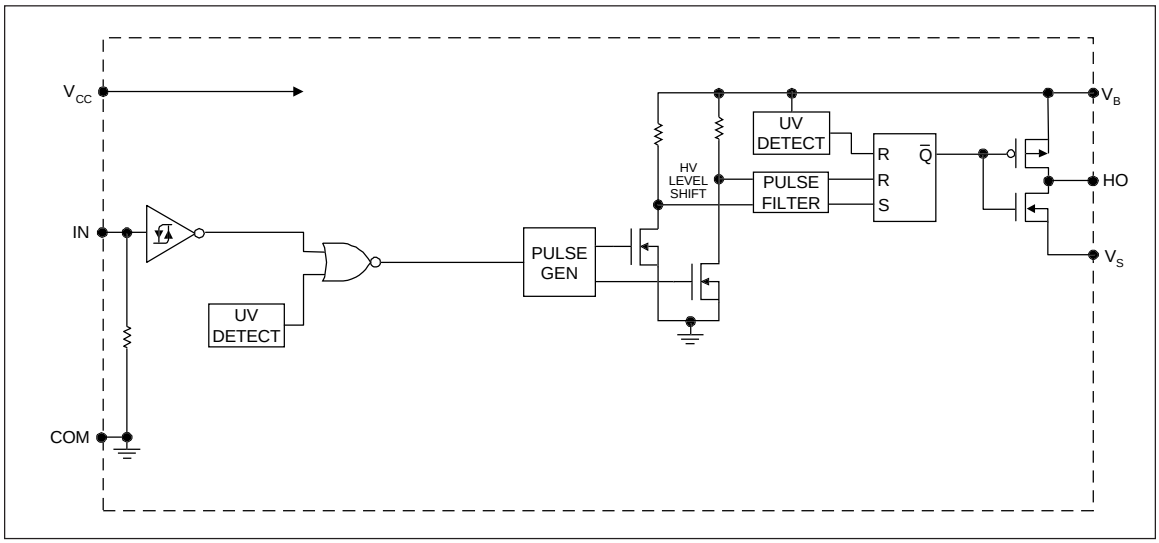
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	125	200	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	105	180		V_S = 600V
t_r	Turn-on rise time	—	80	130		
t_f	Turn-off fall time	—	40	65		

Static Electrical Characteristics

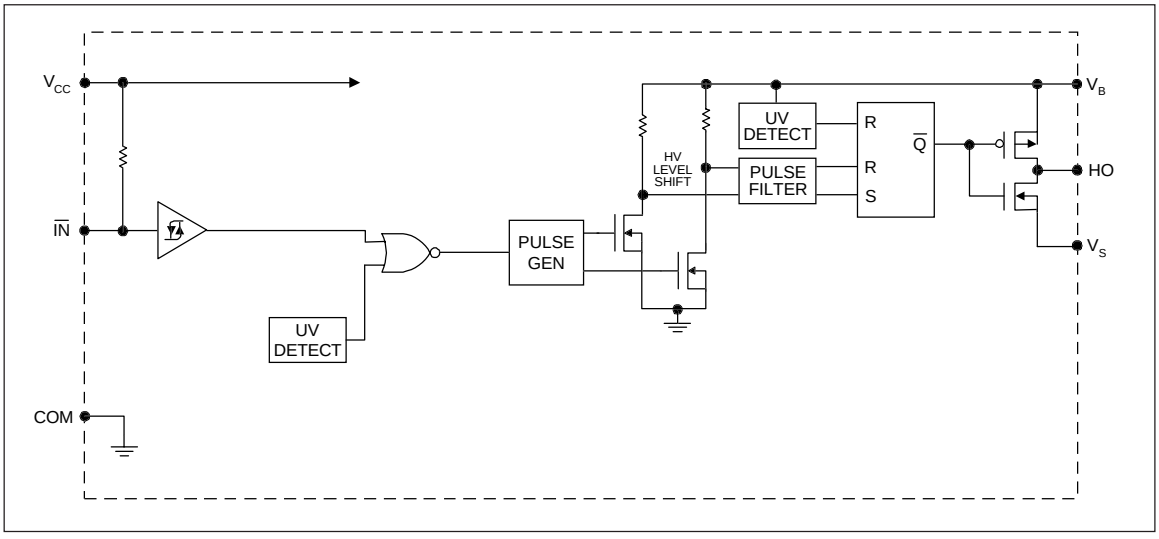
V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition		Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	input voltage - logic “1” (IR2117) logic “0” (IR2118)		9.5	—	—	V	
V_{IL}	Input voltage - logic “0” (IR2117) logic “1” (IR2118)		—	—	6.0		
V_{OH}	High level output voltage, V_{BIAS} - V_O		—	—	100	mV	I_O = 0A
V_{OL}	Low level output voltage, V_O		—	—	100		I_O = 0A
I_{LK}	Offset supply leakage current		—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current		—	50	240		V_{IN} = 0V or V_{CC}
I_{QCC}	Quiescent V_{CC} Supply Current		—	70	340		V_{IN} = 0V or V_{CC}
I_{IN+}	Logic “1” input bias current	(IR2117)	—	20	40		V_{IN} = V_{CC}
		(IR2118)					V_{IN} = 0V
I_{IN-}	Logic “0” input bias current	(IR2117)	—	—	1.0		V_{IN} = 0V
		(IR2118)					V_{IN} = V_{CC}
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold		7.6	8.6	9.6	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold		7.2	8.2	9.2		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold		7.6	8.6	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold		7.2	8.2	9.2		
I_{O+}	Output high short circuit pulsed current		200	250	—	mA	V_O = 0V V_{IN} = Logic “1” PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current		420	500	—		V_O = 15V V_{IN} = Logic “0” PW ≤ 10 µs

Functional Block Diagram (IR2117)



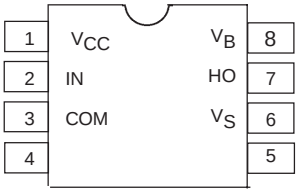
Functional Block Diagram (IR2118)



Lead Definitions

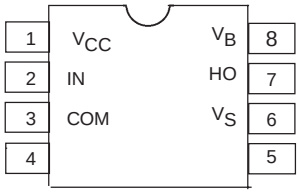
Symbol	Description
V_{CC}	Logic and gate drive supply
IN	Logic input for gate driver output (HO), in phase with HO (IR2117)
$\overline{IN}$	Logic input for gate driver output (HO), out of phase with HO (IR2118)
COM	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return

Lead Assignments



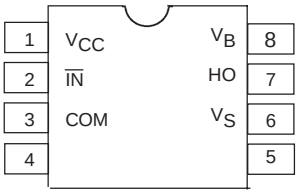
8 Lead PDIP

IR2117



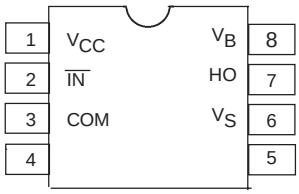
8 Lead SOIC

IR2117S



8 Lead PDIP

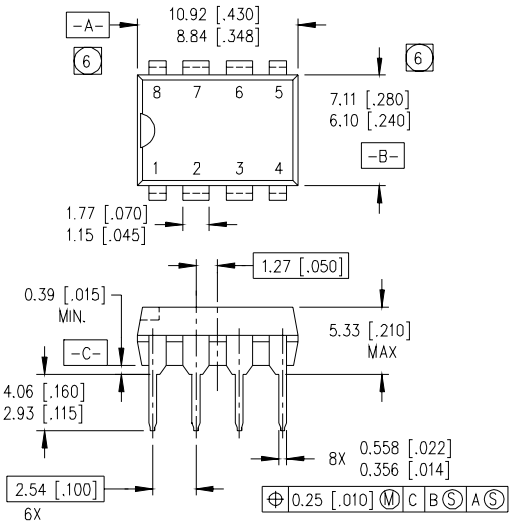
IR2118



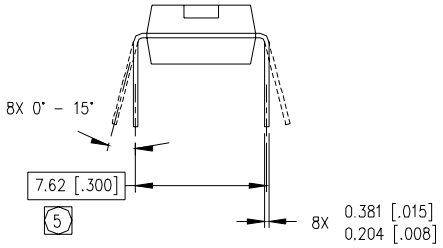
8 Lead SOIC

IR2118S

Case outlines

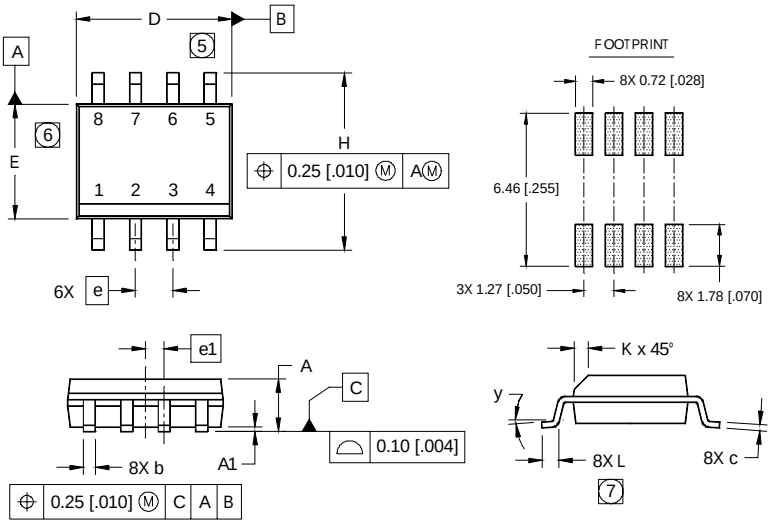


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8-Lead PDIP

01-6014
01-3003 01 (MS-001AB)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8-Lead SOIC

01-6027
01-0021 11 (MS-012AA)

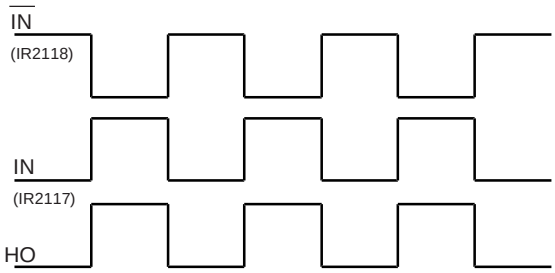


Figure 1. Input/Output Timing Diagram

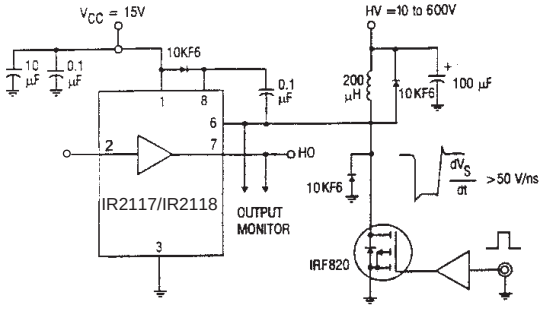


Figure 2. Floating Supply Voltage Transient Test Circuit

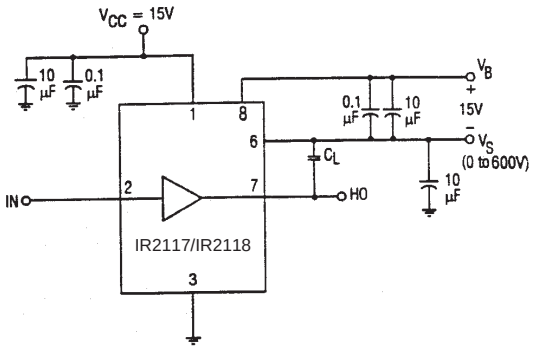


Figure 3. Switching Time Test Circuit

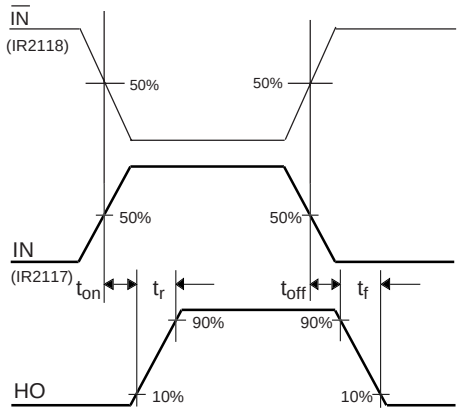


Figure 4. Switching Time Waveform Definition

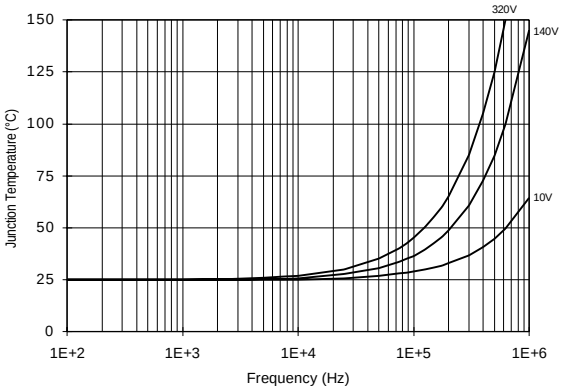


Figure 5. IR2117/IR2118 T_J vs. Frequency (IRFBC20)
R_{GATE} = 33Ω, V_{CC} = 15V

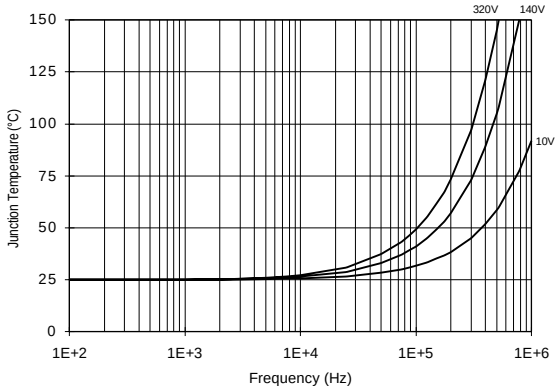


Figure 6. IR2117/IR2118 T_J vs. Frequency (IRFBC30)
R_{GATE} = 22Ω, V_{CC} = 15V

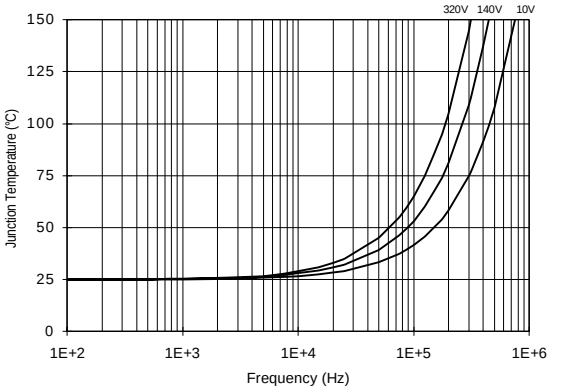


Figure 7. IR2117/IR2118 T_J vs. Frequency (IRFBC40)
R_{GATE} = 15Ω, V_{CC} = 15V

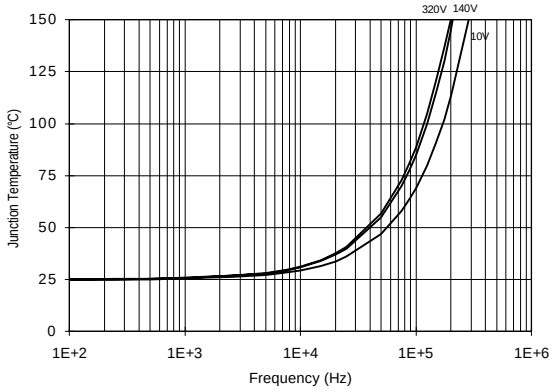


Figure 8. IR2117/IR2118 T_J vs. Frequency (IRFPE50)
R_{GATE} = 10Ω, V_{CC} = 15V

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 322 3331

Data and specifications subject to change without notice. 5/1/2001

Data Sheet No. PD60018-K

International
IOR Rectifier

IR2121

CURRENT LIMITING LOW SIDE DRIVER

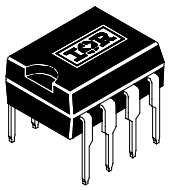
Features

- Gate drive supply range from 12 to 18V
- Undervoltage lockout
- Current detection and limiting loop to limit driven power transistor current
- Error lead indicates fault conditions and programs shutdown time
- Output in phase with input
- 2.5V, 5V and 15V input logic compatible

Product Summary

V_{OFFSET}	5V max.
I_O+/-	1A / 2A
V_{OUT}	12 - 18V
V_{CSth}	230 mV
$t_{on/off}$ (typ.)	150 & 150 ns

Package

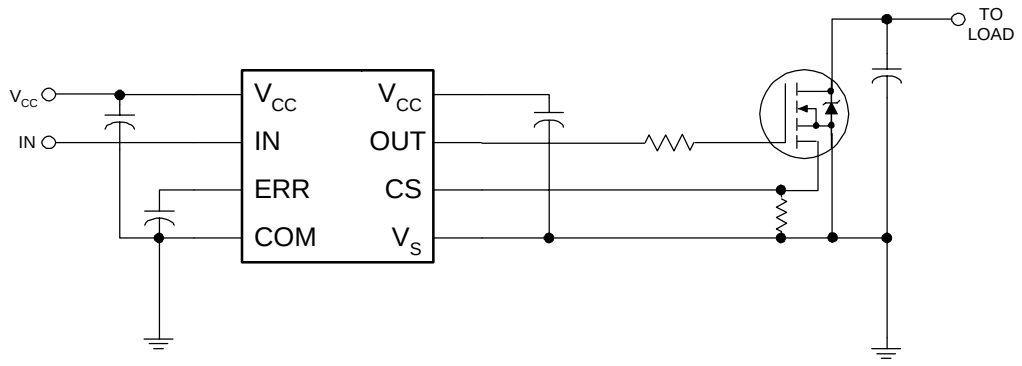


8-Lead PDIP

Description

The IR2121 is a high speed power MOSFET and IGBT driver with over-current limiting protection circuitry. Latch immune CMOS technology enables ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 2.5V logic. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The protection circuitry detects over-current in the driven power transistor and limits the gate drive voltage. Cycle-by-cycle shutdown is programmed by an external capacitor which directly controls the time interval between detection of the over-current limiting condition and latched shutdown. The output can be used to drive an N-channel power MOSFET or IGBT in the low side configuration.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
V_{CC}	Fixed Supply Voltage	-0.3	25	V
V_S	Gate Drive Return Voltage	V_{CC} - 25	V_{CC} + 0.3	
V_O	Output Voltage	V_S - 0.3	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage	-0.3	V_{CC} + 0.3	
V_{ERR}	Error Signal Voltage	-0.3	V_{CC} + 0.3	
V_{CS}	Current Sense Voltage	V_S - 0.3	V_{CC} + 0.3	
P_D	Package Power Dissipation @ $T_A \leq +25°C$	—	1.0	W
Rth_{JA}	Thermal Resistance, Junction to Ambient	—	125	°C/W
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
V_{CC}	Fixed Supply Voltage	V_S + 12	V_S + 18	V
V_S	Gate Drive Return Voltage	-5	5	
V_O	Output Voltage	V_S	V_{CC}	
V_{IN}	Logic Input Voltage	0	V_{CC}	
V_{ERR}	Error Signal Voltage	0	V_{CC}	
V_{CS}	Current Sense Signal Voltage	V_S	V_{CC}	
T_A	Ambient Temperature	-40	125	°C

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}) = 15V, C_L = 3300 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are defined in Figures 2 through 5.

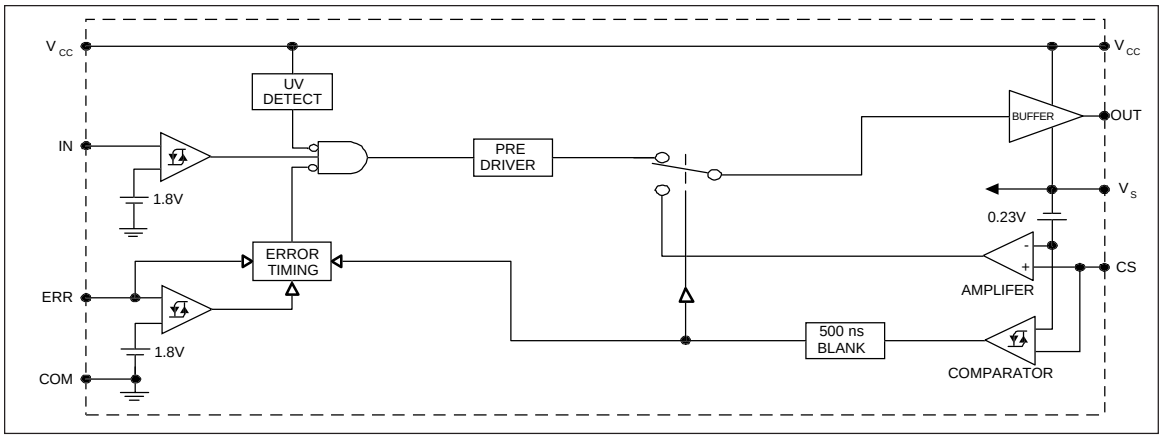
Parameter			Value				
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	7	—	150	200	ns	V_{IN} = 0 & 5V
t_{off}	Turn-Off Propagation Delay	8	—	150	190		
t_{sd}	ERR Shutdown Propagation Delay	9	—	1.7	2.2	µs	
t_r	Turn-On Rise Time	10	—	43	60	ns	
t_f	Turn-Off Fall Time	11	—	26	35		
t_{cs}	CS Shutdown Propagation Delay	12	—	0.7	1.2	µs	
t_{err}	CS to ERR Pull-Up Propagation Delay	13	—	9.0	12		C_{ERR} = 270 pF

Static Electrical Characteristics

V_{BIAS} (V_{CC}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S .

Parameter			Value				
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” Input Voltage	14	2.2	—	—	V	
V_{IL}	Logic “0” Input Voltage	15	—	—	0.8		
V_{CSTH+}	CS Input Positive Going Threshold	16	150	230	320	mV	
V_{CSTH-}	CS Input Negative Going Threshold	17	130	200	260		
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	18	—	—	100		I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	19	—	—	100		I_O = 0A
I_{QCC}	Quiescent VCC Supply Current	20	—	1.1	2.2	mA	V_{IN} = V_{CS} = 0V or 5V
I_{IN+}	Logic “1” Input Bias Current	21	—	4.5	10	µA	V_{IN} = 5V
I_{IN-}	Logic “0” Input Bias Current	22	—	—	1.0		V_{IN} = 0V
I_{CS+}	“High” CS Bias Current	23	—	4.5	10		V_{CS} = 3V or 5V
I_{CS-}	“Low” CS Bias Current	24	—	—	1.0		V_{CS} = 0V
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	25	8.3	8.9	9.6	V	
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	26	7.3	8.0	8.7		
I_{ERR}	ERR Timing Charge Current	27	65	100	130	µA	V_{IN} = 5V, V_{CS} = 3V ERR < V_{ERR+}
I_{ERR+}	ERR Pull-Up Current	28	8.0	15	—	mA	V_{IN} = 5V, V_{CS} = 3V ERR > V_{ERR+}
I_{ERR-}	ERR Pull-Down Current	29	16	30	—		V_{IN} = 0V
I_{O+}	Output High Short Circuit Pulsed Current	30	1.0	1.6	—	A	V_O = 0V, V_{IN} = 5V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	31	2.0	3.3	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

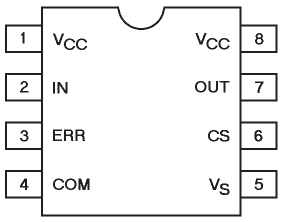
Functional Block Diagram



Lead Definitions

Lead Symbol	Description
V_{CC}	Logic and gate drive supply
IN	Logic input for gate driver output (OUT), in phase with OUT
ERR	Serves multiple functions; status reporting, linear mode timing and cycle by cycle logic shutdown
COM	Logic ground
OUT	Gate drive output
V_S	Gate drive supply return
CS	Current sense input to current sense comparator

Lead Assignments



8 Lead PDIP

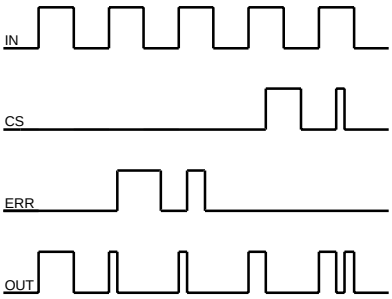


Figure 1. Input/Output Timing Diagram

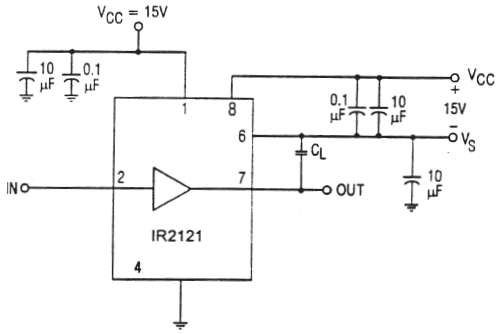


Figure 2. Switching Time Test Circuit

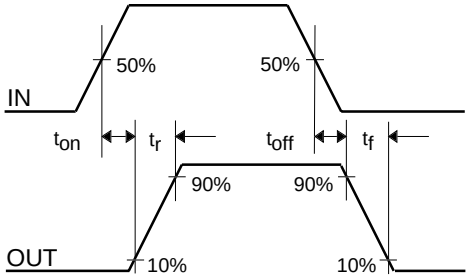


Figure 3. Switching Time Waveform Definitions

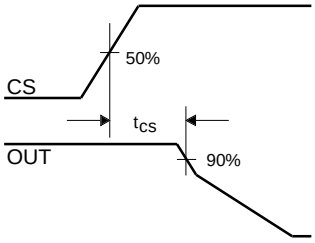


Figure 4. ERR Shutdown Waveform Definitions

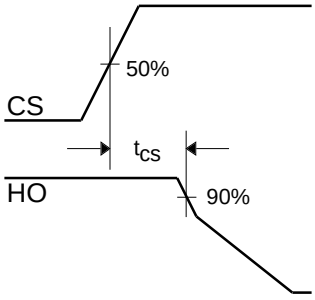
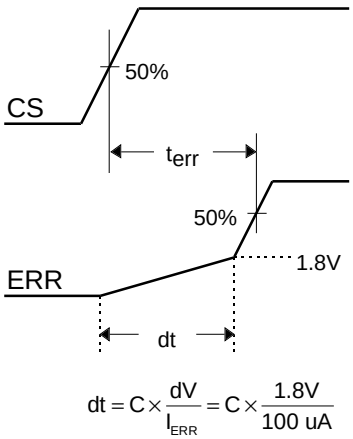


Figure 5. CS Shutdown Waveform Definitions



$$dt = C \times \frac{dV}{I_{ERR}} = C \times \frac{1.8V}{100\ uA}$$

Figure 6. CS to ERR Waveform Definitions

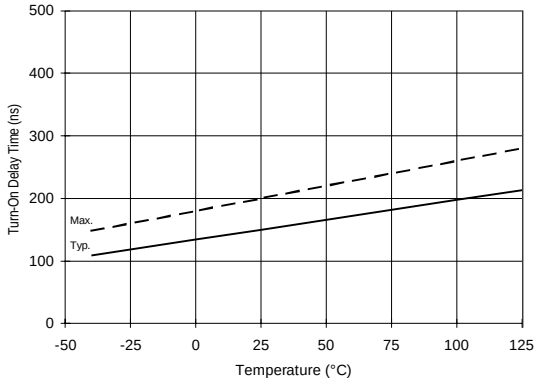


Figure 7A. Turn-On Time vs. Temperature

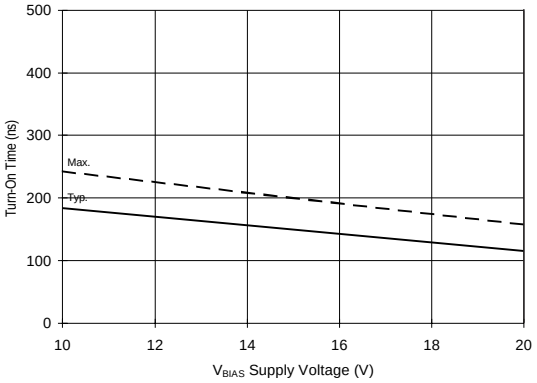


Figure 7B. Turn-On Time vs. Voltage

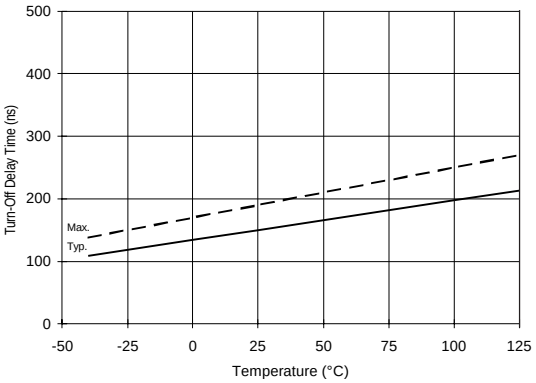


Figure 8A. Turn-Off Time vs. Temperature

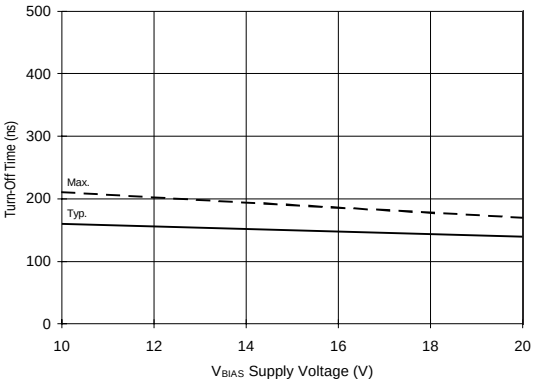


Figure 8B. Turn-Off Time vs. Voltage

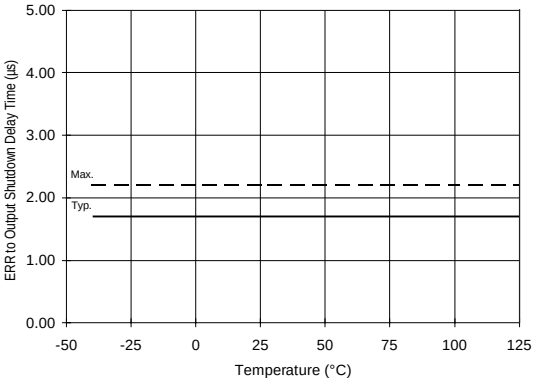


Figure 9A. ERR to Output Shutdown vs. Temperature

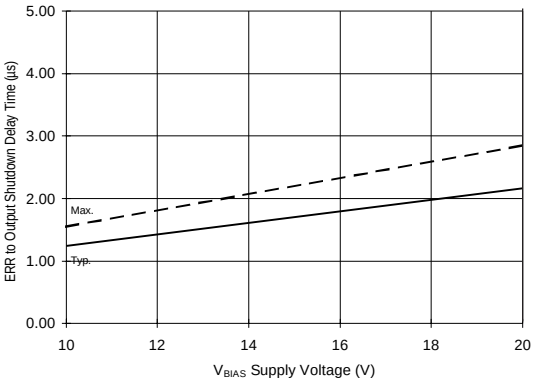


Figure 9B. ERR to Output Shutdown vs. Voltage

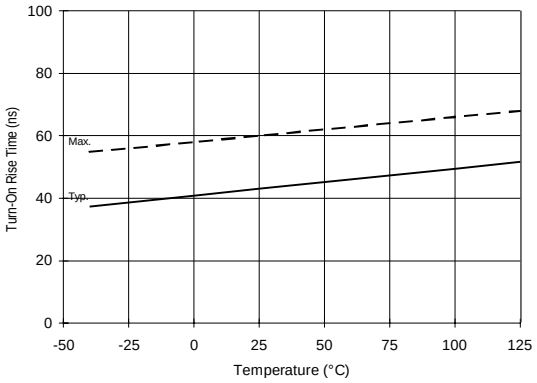


Figure 10A. Turn-On Rise Time vs. Temperature

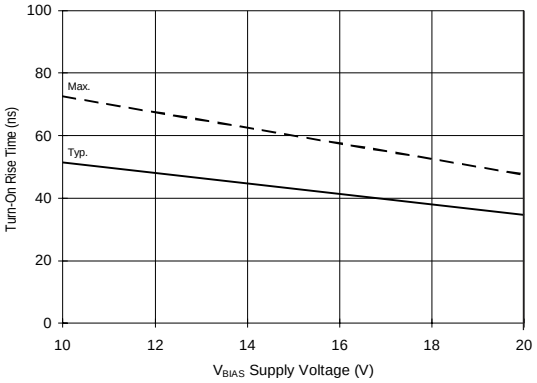


Figure 10B. Turn-On Rise Time vs. Voltage

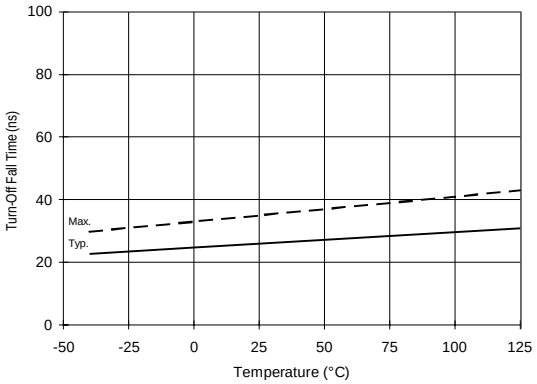


Figure 11A. Turn-Off Fall Time vs. Temperature

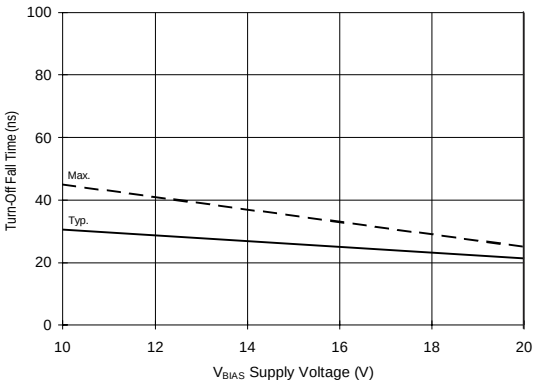


Figure 11B. Turn-Off Fall Time vs. Voltage

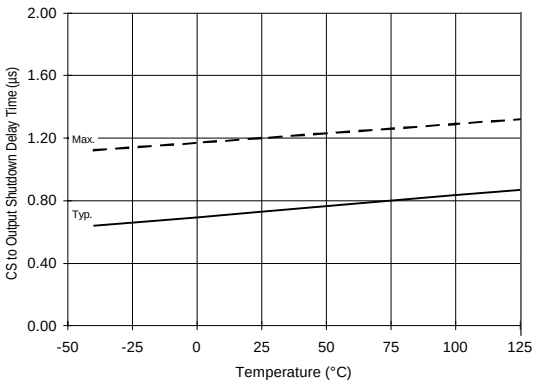


Figure 12A. CS to Output Shutdown vs. Temperature

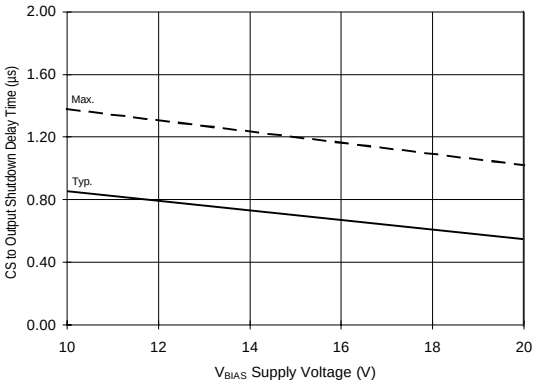


Figure 12B. CS to Output Shutdown vs. Voltage

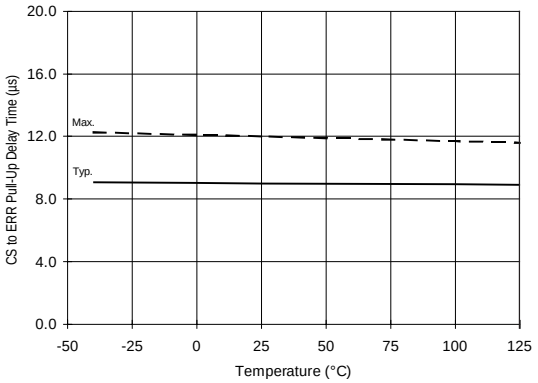


Figure 13A. CS to ERR Pull-Up vs. Temperature

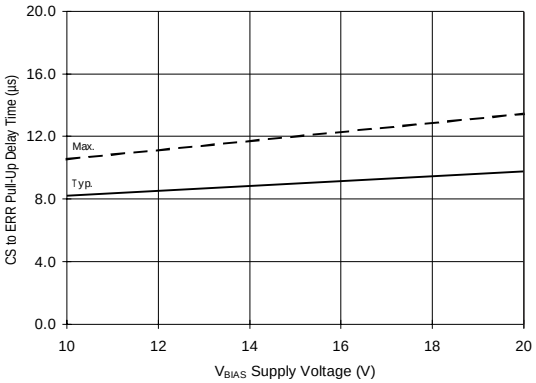


Figure 13B. CS to ERR Pull-Up vs. Voltage

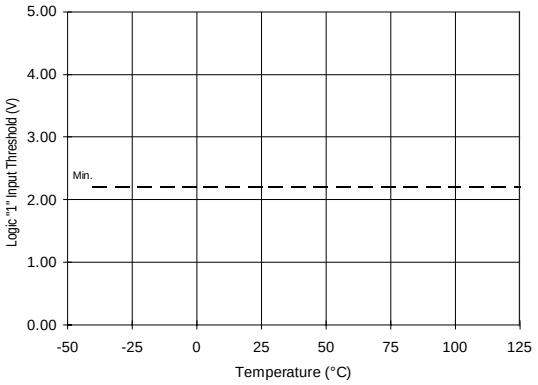


Figure 14A. Logic "1" Input Threshold vs. Temperature

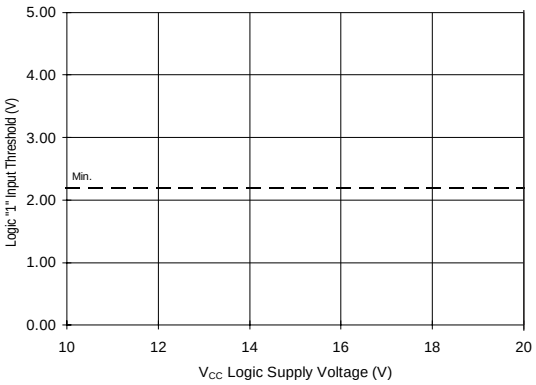


Figure 14B. Logic "1" Input Threshold vs. Voltage

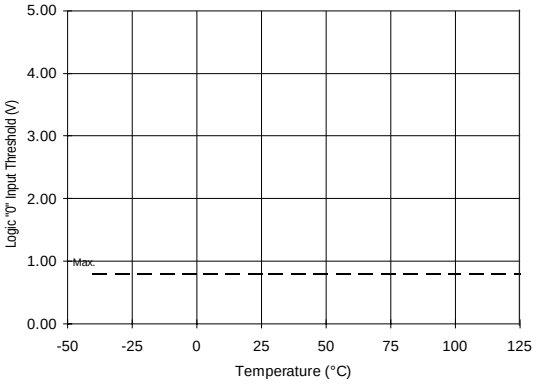


Figure 15A. Logic "0" Input Threshold vs. Temperature

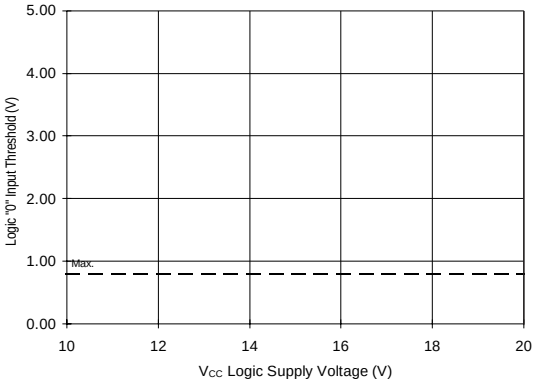


Figure 15B. Logic "0" Input Threshold vs. Voltage

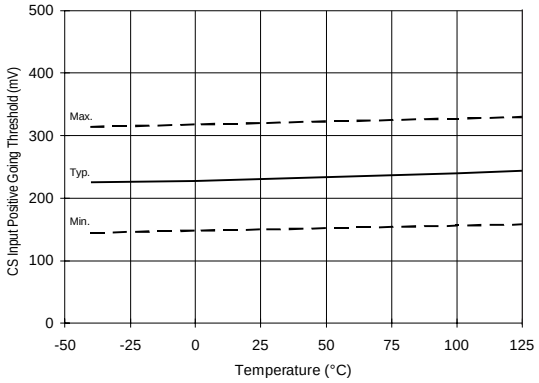


Figure 16A. CS Input Threshold (+) vs. Temperature

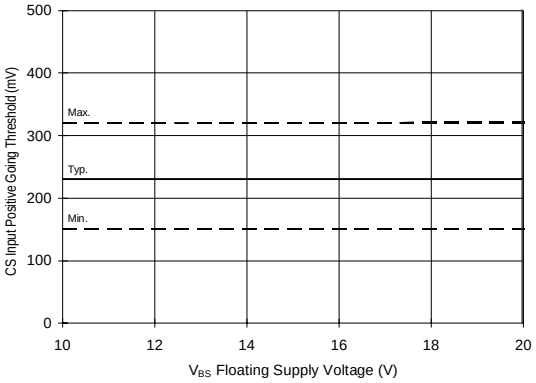


Figure 16B. CS Input Threshold (+) vs. Voltage

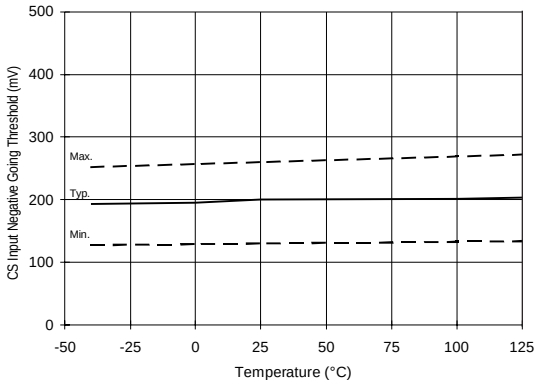


Figure 17A. CS Input Threshold (-) vs. Temperature

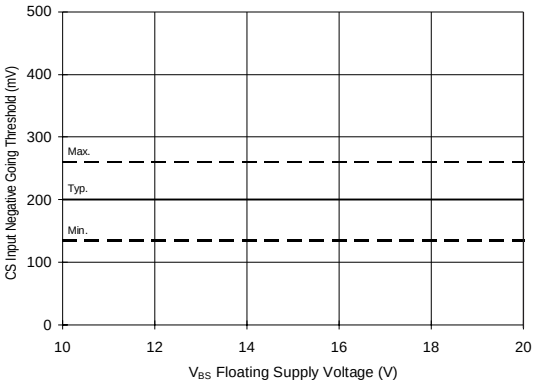


Figure 17B. CS Input Threshold (-) vs. Voltage

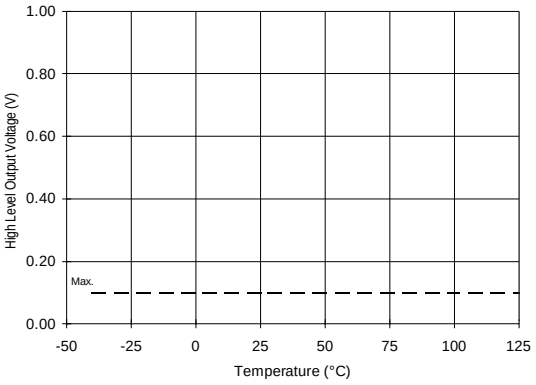


Figure 18A. High Level Output vs. Temperature

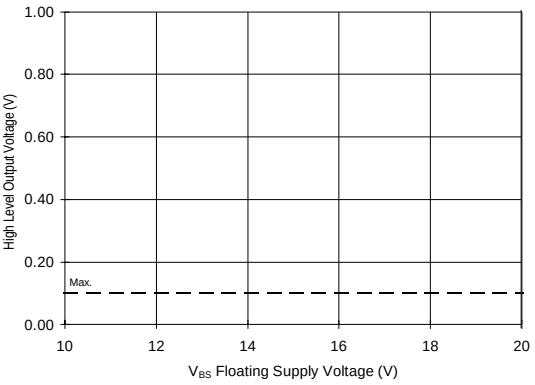


Figure 18B. High Level Output vs. Voltage

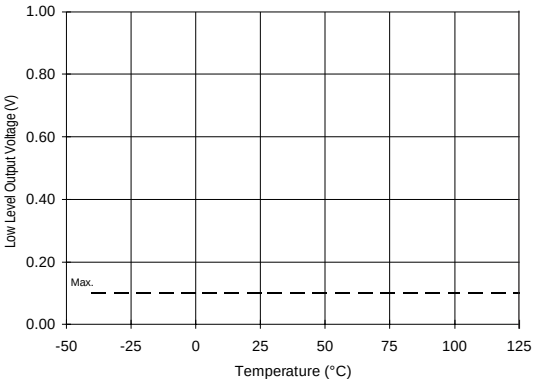


Figure 19A. Low Level Output vs. Temperature

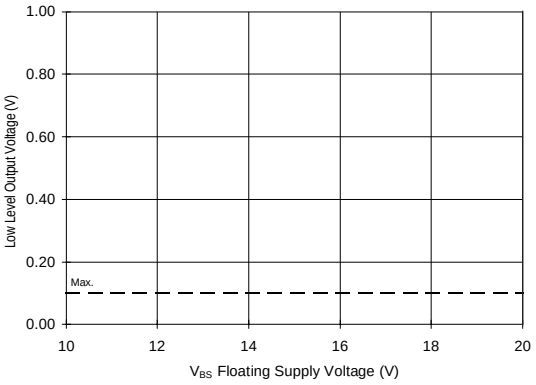


Figure 19B. Low Level Output vs. Voltage

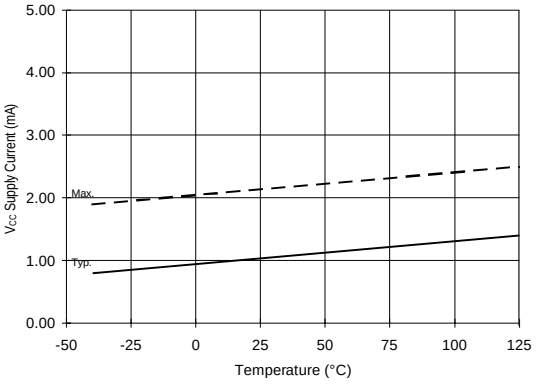


Figure 20A. V_{CC} Supply Current vs. Temperature

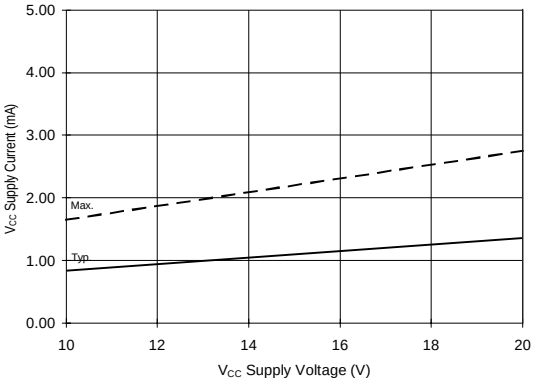


Figure 20B. V_{CC} Supply Current vs. Voltage

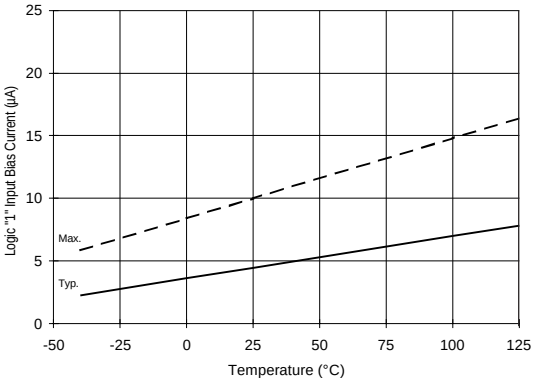


Figure 21A. Logic "1" Input Current vs. Temperature

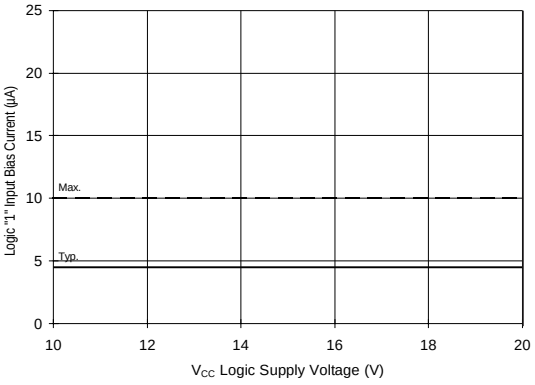


Figure 21B. Logic "1" Input Current vs. Voltage

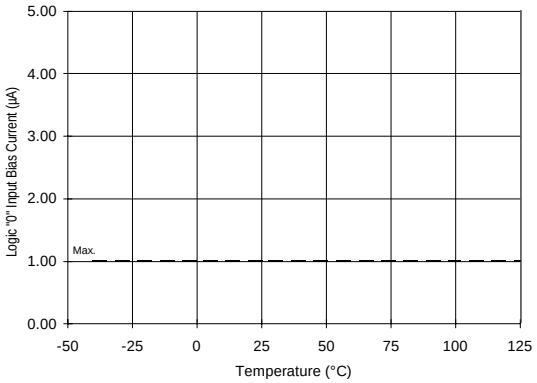


Figure 22A. Logic "0" Input Current vs. Temperature

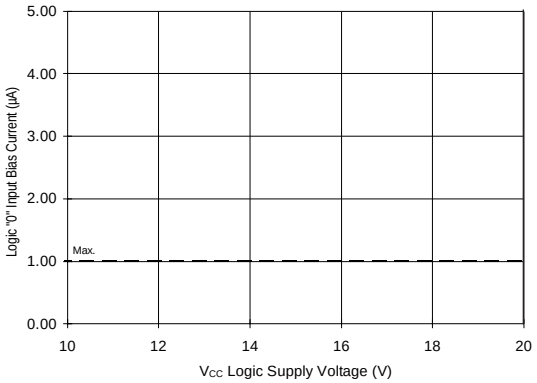


Figure 22B. Logic "0" Input Current vs. Voltage

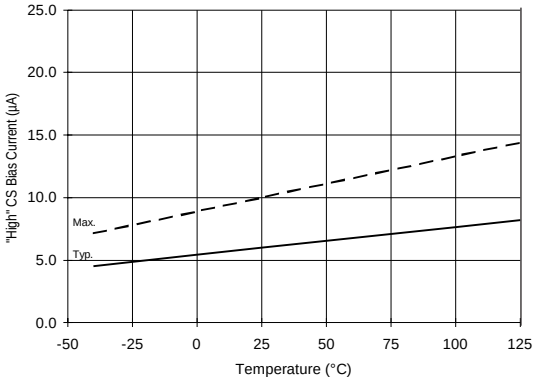


Figure 23A. "High" CS Bias Current vs. Temperature

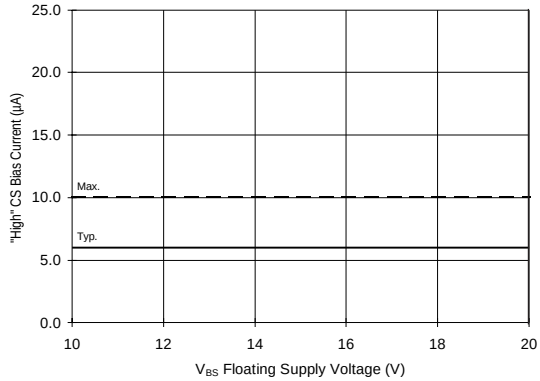


Figure 23B. "High" CS Bias Current vs. Voltage

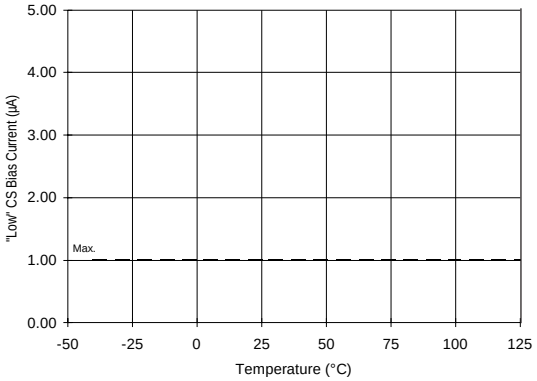


Figure 24A. "Low" CS Bias Current vs. Temperature

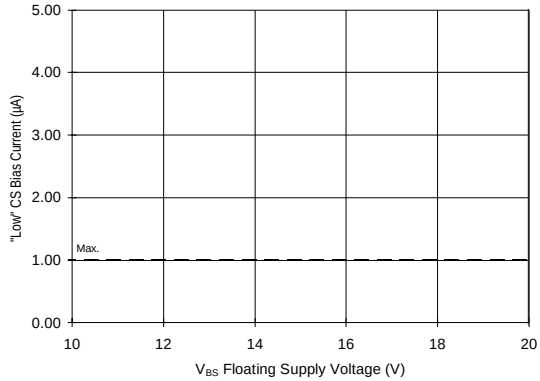


Figure 24B. "Low" CS Bias Current vs. Voltage

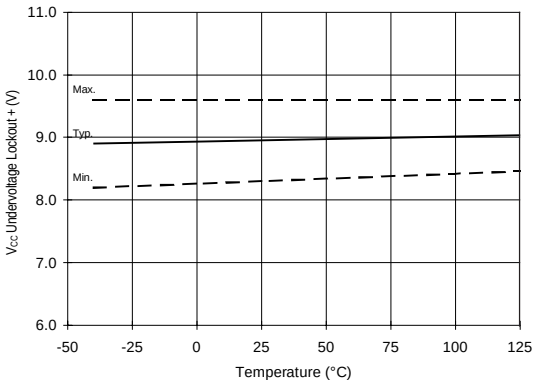


Figure 25. V_{CC} Undervoltage (+) vs. Temperature

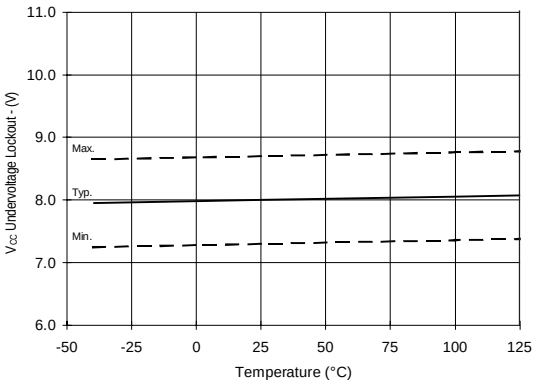


Figure 26. V_{CC} Undervoltage (-) vs. Temperature

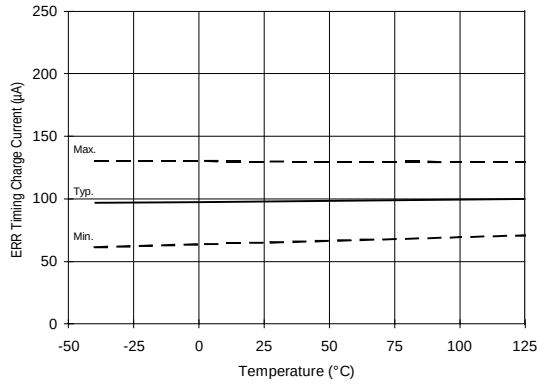


Figure 27A. ERR Timing Charge Current vs. Temperature

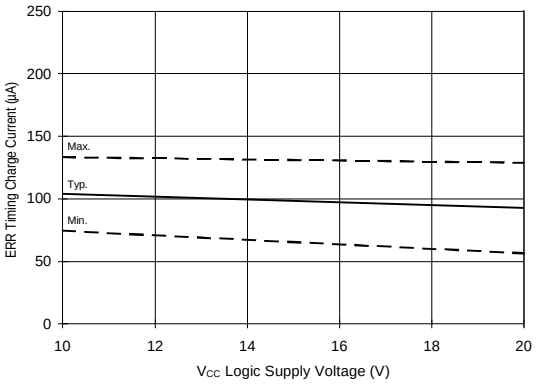


Figure 27B. ERR Timing Charge Current vs. Voltage

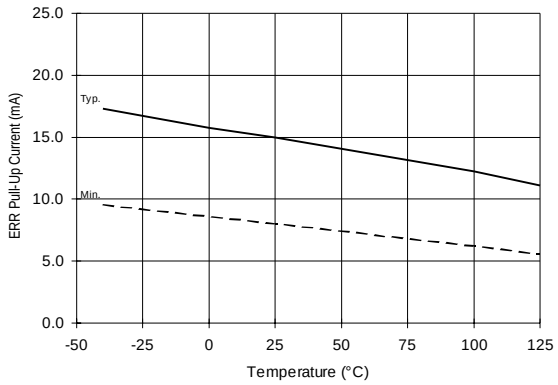


Figure 28A. ERR Pull-Up Current vs. Temperature

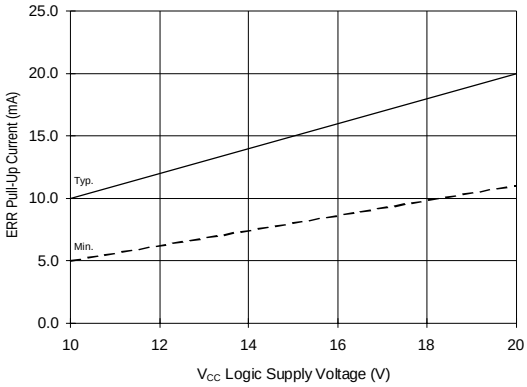


Figure 28B. ERR Pull-Up Current vs. Voltage

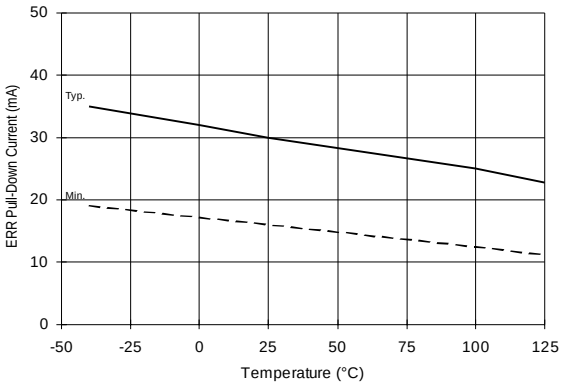


Figure 29A. ERR Pull-Down Current vs.Temperature

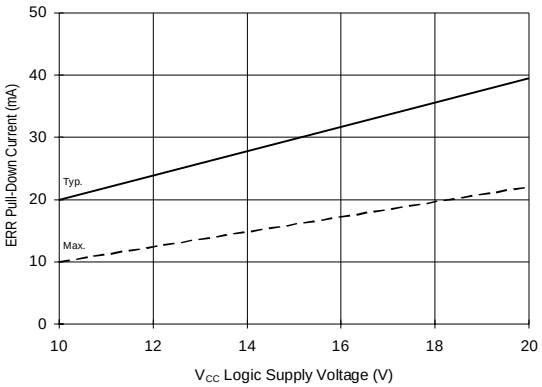


Figure 29B. ERR Pull-Down Current vs. Voltage

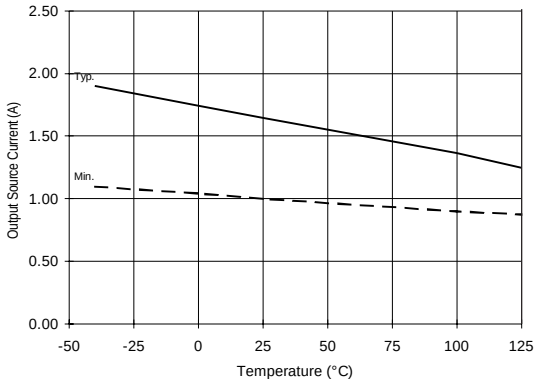


Figure 30A. Output Source Current vs.Temperature

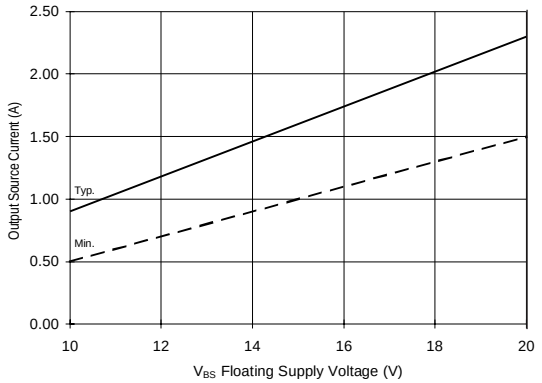


Figure 30B. Output Source Current vs. Voltage

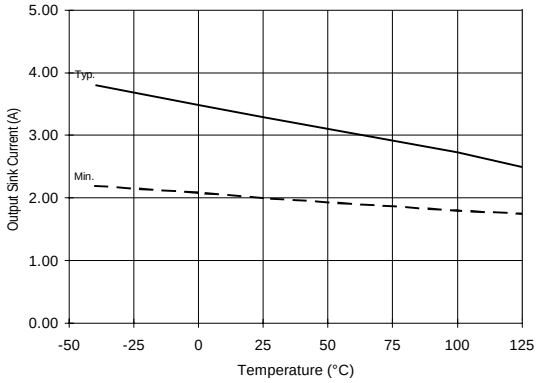


Figure 31A. Output Sink Current vs.Temperature

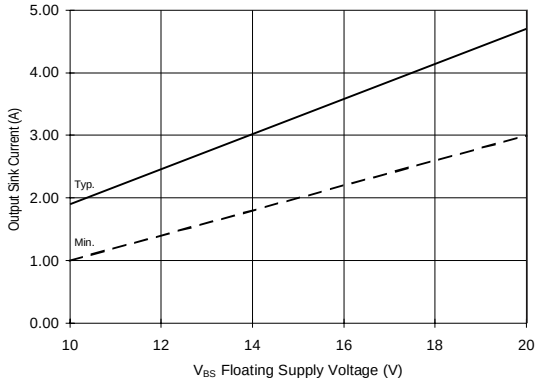


Figure 31B. Output Sink Current vs. Voltage

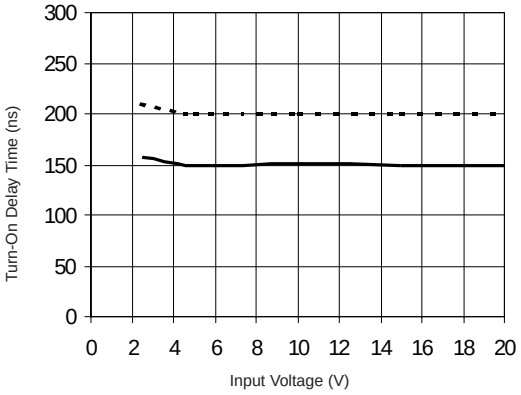


Figure 32A. Turn-On Time vs. Input Voltage

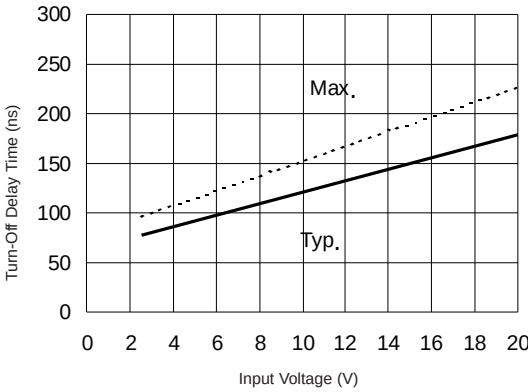


Figure 32B. Turn-Off Time vs. Input Voltage

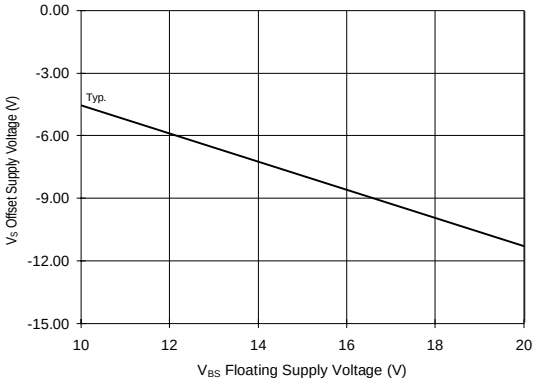
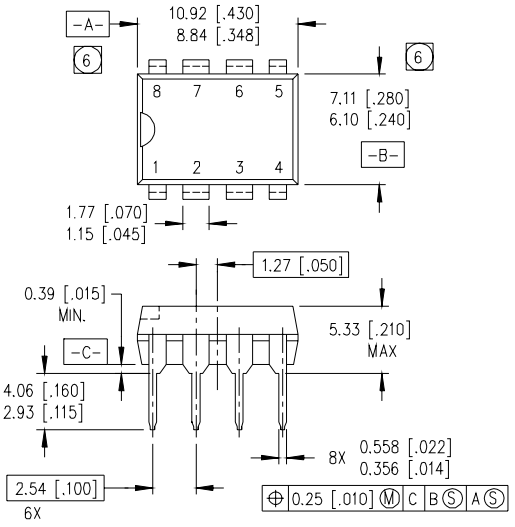


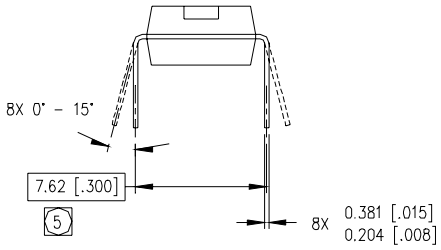
Figure 33. Maximum V_S Negative Offset vs. Supply Voltage

Case outline



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8-Lead PDIP

01-6014
01-3003 01 (MS-001AB)

Preliminary Data Sheet No. PD60130-J

International
IOR Rectifier

IR2122(S)

CURRENT SENSING SINGLE CHANNEL DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 3.3V, 5V and 15V input logic compatible
- $\overline{\text{FAULT}}$ lead indicates shutdown has occured
- Output out of phase with input

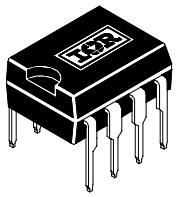
Description

The IR2122(S) is a high voltage, high speed power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL outputs, down to 3.3V. The protection circuity detects over-current in the driven power transistor and terminates the gate drive voltage. An open drain $\overline{\text{FAULT}}$ signal is provided to indicate that an over-current shutdown has occurred. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side or low side configuration which operates up to 600 volts.

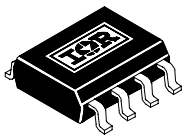
Product Summary

V_{OFFSET}	600V max.
I_O+/-	110 mA / 110 mA
V_{OUT}	10 - 20V
V_{CSth}	500 mV
$t_{on/off}$ (typ.)	250 & 200 ns

Packages

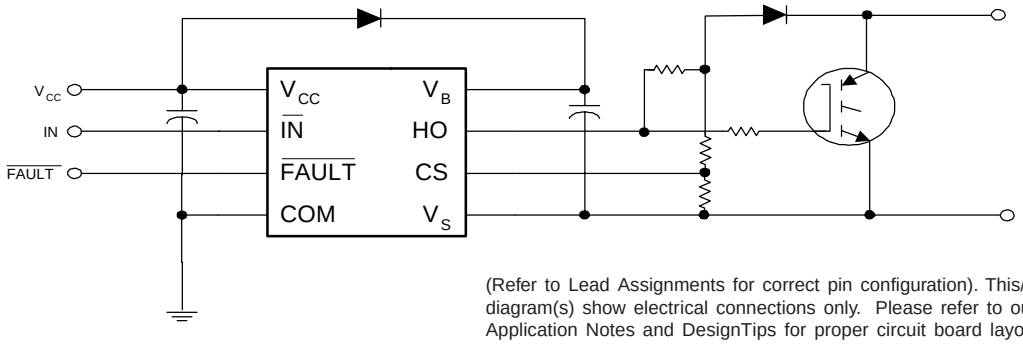


8-Lead PDIP



8-Lead SOIC

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	-0.3	625	V
V_S	High Side Floating Offset Voltage	V_B - 25	V_B + 0.3	
V_{HO}	High Side Floating Output Voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Logic Supply Voltage	-0.3	25	
V_{IN}	Logic Input Voltage	-0.3	V_{CC} + 0.3	
V_{FLT}	$\overline{\text{FAULT}}$ Output Voltage	-0.3	V_{CC} + 0.3	
V_{CS}	Current Sense Voltage	V_S - 0.3	V_B + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$ (8 Lead DIP)	—	1.0	W
	(8 Lead SOIC)	—	0.625	
R_{THJA}	Thermal Resistance, Junction to Ambient (8 Lead DIP)	—	125	°C/W
	(8 Lead SOIC)	—	200	
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	V_S + 13	V_S + 20	V
V_S	High Side Floating Offset Voltage	Note 1	600	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Logic Supply Voltage	13	20	
V_{IN}	Logic Input Voltage	0	V_{CC}	
V_{FLT}	$\overline{\text{FAULT}}$ Output Voltage	0	V_{CC}	
V_{CS}	Current Sense Signal Voltage	V_S	V_S + 5	
T_A	Ambient Temperature	-40	150	℃

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

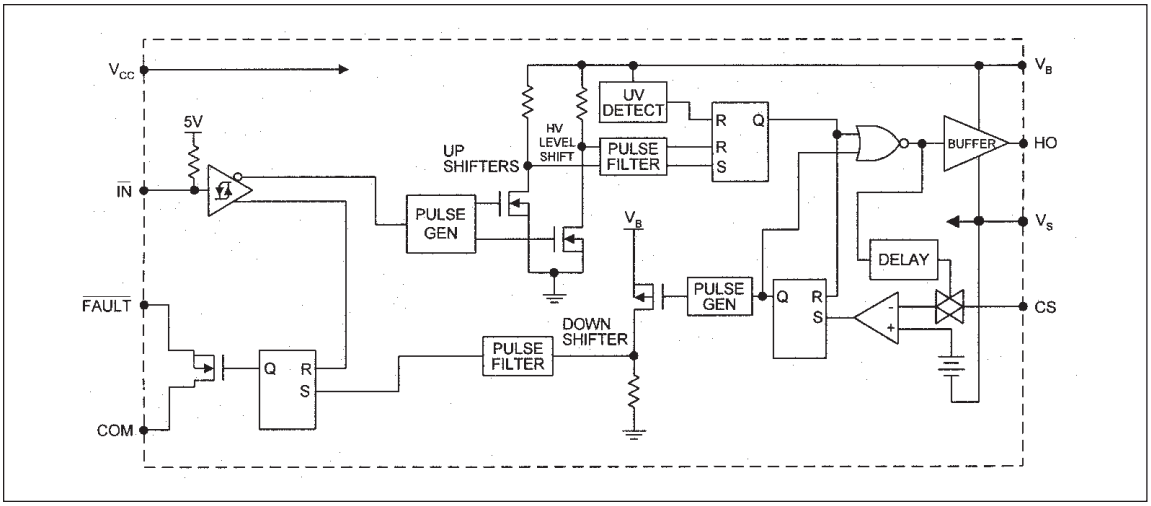
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	—	250	—	ns	V_S = 0V
t_{off}	Turn-Off Propagation Delay	—	200	—		V_S = 600V
t_r	Turn-On Rise Time	—	250	—		C_L = 1000 pF
t_f	Turn-Off Fall Time	—	250	—		C_L = 1000 pF
t_{bl}	Start-Up Blanking Time	500	900	—		
t_{cs}	CS Shutdown Propagation Delay	—	350	—		
t_{flt}	CS to $\overline{\text{FAULT}}$ Pull-Up Propagation Delay	—	450	—		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “0” Input Voltage (OUT = LO)	3.0	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic “1” Input Voltage (OUT = HI)	—	—	0.8		V_{CC} = 10V to 20V
V_{CSTH+}	CS Input Positive Going Threshold	350	500	650		V_{CC} = 10V to 20V
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	—	—	100	mV	I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	—	—	100		I_O = 0A
I_{LK}	Offset Supply Leakage Current	—	—	50		V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} Supply Current	—	150	350	µA	V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	—	60	120		V_{IN} = 0V or 5V
I_{IN+}	Logic “1” Input Bias Current	—	7.0	15		V_{IN} = 0V
I_{IN-}	Logic “0” Input Bias Current	—	—	1.0		V_{IN} = 5V
I_{CS+}	“High” CS Bias Current	—	—	1.0		V_{CS} = 3V
I_{CS-}	“High” CS Bias Current	—	—	1.0		V_{CS} = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	10.0	11.4	13.0	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	9.5	10.4	12.5		
I_{O+}	Output High Short Circuit Pulsed Current	110	130	—	mA	V_O = 0V, V_{IN} = 0V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	110	130	—		V_O = 15V, V_{IN} = 5V PW ≤ 10 µs

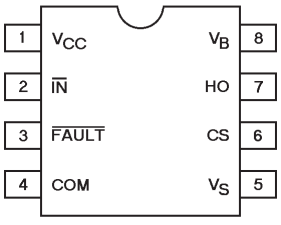
Functional Block Diagram



Lead Definitions

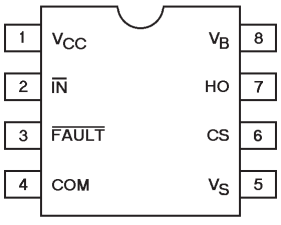
Lead Symbol	Description
V_{CC}	Logic and gate drive supply
$\overline{IN}$	Logic input for gate driver output (HO), out of phase with HO
$\overline{FAULT}$	Indicates over-current shutdown has occurred, negative logic
COM	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
CS	Current sense input to current sense comparator

Lead Assignments



8 Lead PDIP

IR2122



8 Lead SOIC

IR2122S

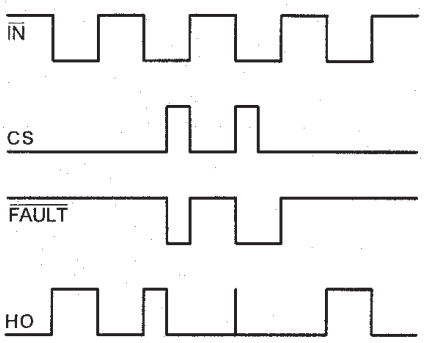


Figure 1. Input/Output Timing Diagram

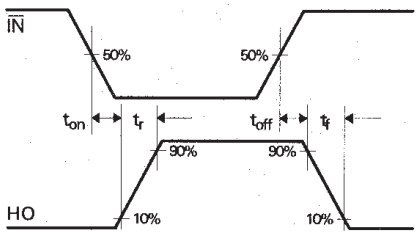


Figure 2. Switching Time Waveform Definition

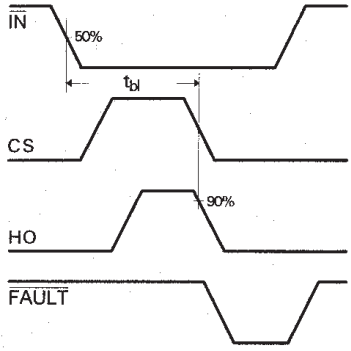


Figure3. Start-up Blanking Time Waveform Definitions

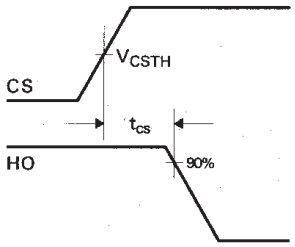


Figure 4. CS Shutdown Waveform Definitions

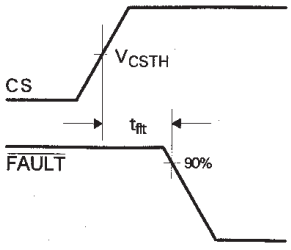
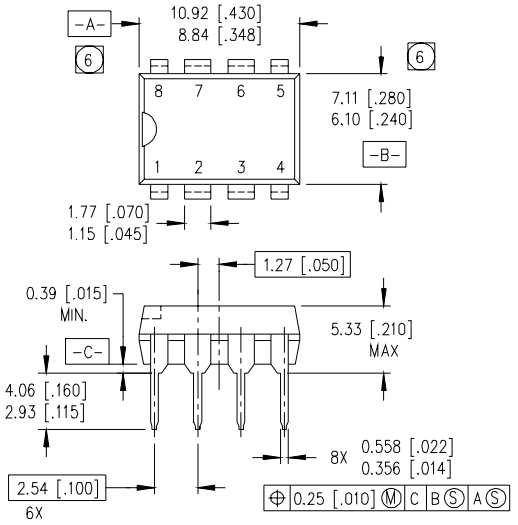


Figure 5. CS to $\overline{\text{FAULT}}$ Waveform Definitions

Case outlines

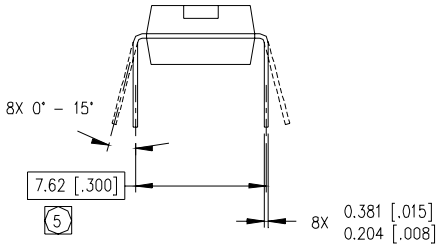


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.

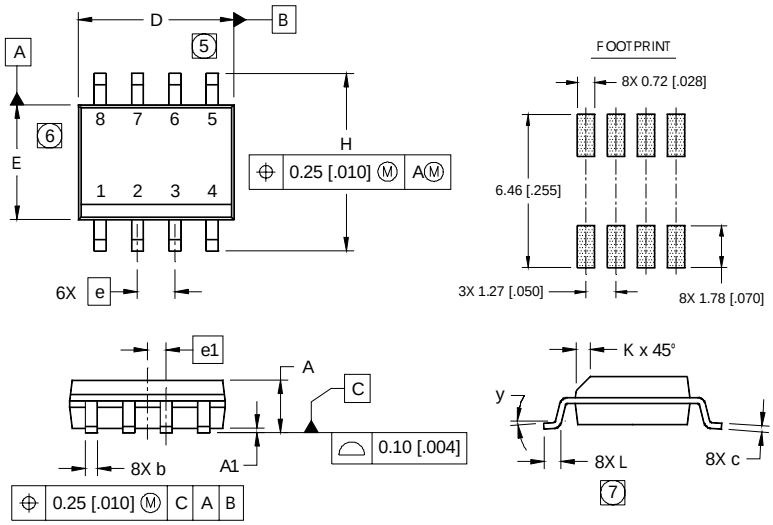
(5) MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8-Lead PDIP

01-6014
01-3003 01 (MS-001AB)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

(5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

(6) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

(7) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8-Lead SOIC

01-6027
01-0021 11 (MS-012AA)

IR2125(S)

CURRENT LIMITING SINGLE CHANNEL DRIVER

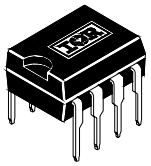
Features

- Floating channel designed for bootstrap operation
  Fully operational to +500V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 12 to 18V
- Undervoltage lockout
- Current detection and limiting loop to limit driven power transistor current
- Error lead indicates fault conditions and programs shutdown time
- Output in phase with input
- 2.5V, 5V and 15V input logic compatible

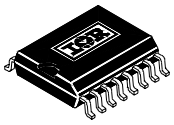
Product Summary

V_{OFFSET}	500V max.
I_O+/-	1A / 2A
V_{OUT}	12 - 18V
V_{CSth}	230 mV
$t_{on/off}$ (typ.)	150 & 150 ns

Packages



8-Lead PDIP

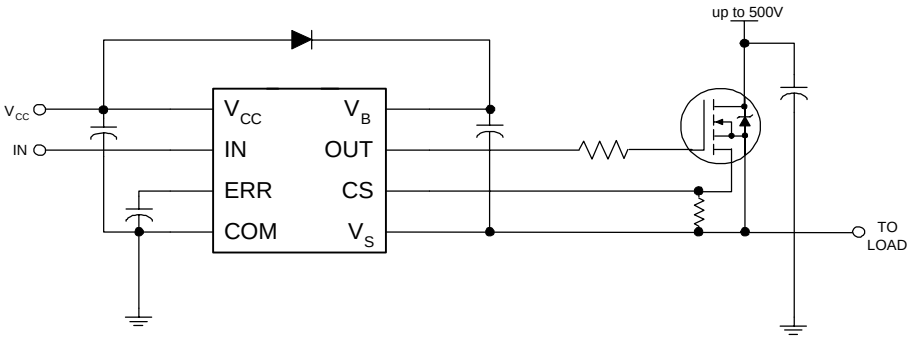


16-Lead SOIC
(Wide Body)

Description

The IR2125(S) is a high voltage, high speed power MOSFET and IGBT driver with over-current limiting protection circuitry. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 2.5V logic. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. The protection circuitry detects over-current in the driven power transistor and limits the gate drive voltage. Cycle by cycle shutdown is programmed by an external capacitor which directly controls the time interval between detection of the over-current limiting conditions and latched shutdown. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high or low side configuration which operates up to 500 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	-0.3	525	V
V_S	High Side Floating Offset Voltage	V_B - 25	V_B + 0.3	
V_{HO}	High Side Floating Output Voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Logic Supply Voltage	-0.3	25	
V_{IN}	Logic Input Voltage	-0.3	V_{CC} + 0.3	
V_{ERR}	Error Signal Voltage	-0.3	V_{CC} + 0.3	
V_{CS}	Current Sense Voltage	V_S - 0.3	V_B + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$ (8 lead PDIP)	—	1.0	W
	(16 lead SOIC)	—	1.25	
Rth_{JA}	Thermal Resistance, Junction to Ambient (8 lead PDIP)	—	125	°C/W
	(16lLead SOIC)	—	100	
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	V_S + 12	V_S + 18	V
V_S	High Side Floating Offset Voltage	Note 1	500	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Logic Supply Voltage	0	18	
V_{IN}	Logic Input Voltage	0	V_{CC}	
V_{ERR}	Error Signal Voltage	0	V_{CC}	
V_{CS}	Current Sense Signal Voltage	V_S	V_B	
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +500V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 3300 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figures 3 through 6.

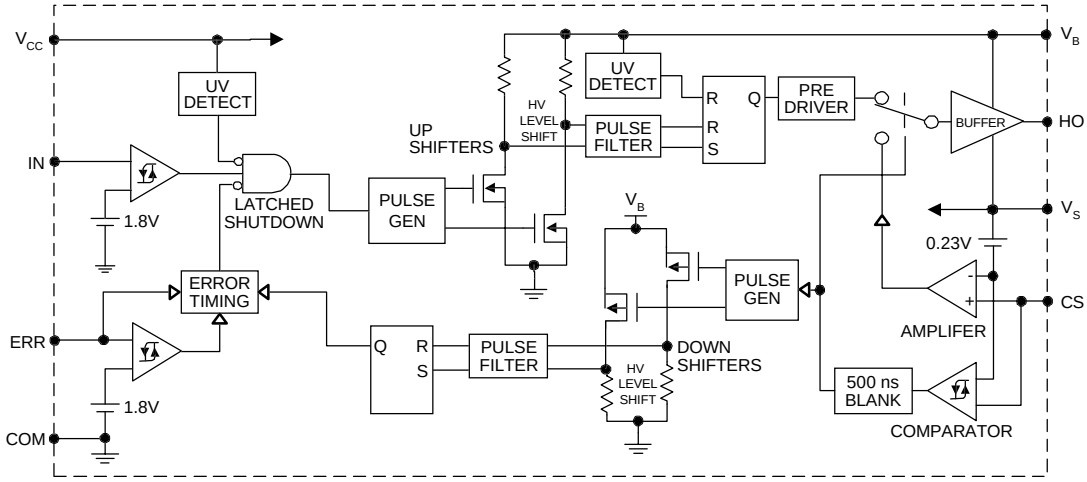
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	7	—	150	200	ns	V_{IN} = 0 & 5V V_S = 0 to 600V
t_{off}	Turn-Off Propagation Delay	8	—	150	190		
t_{sd}	ERR Shutdown Propagation Delay	9	—	1.7	2.2	µs	
t_r	Turn-On Rise Time	10	—	43	60	ns	
t_f	Turn-Off Fall Time	11	—	26	35		
t_{cs}	CS Shutdown Propagation Delay	12	—	0.7	1.2	µs	
t_{err}	CS to ERR Pull-Up Propagation Delay	13	—	9.0	12		C_{ERR} = 270 pF

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" Input Voltage	14	2.2	—	—	V	
V_{IL}	Logic "0" Input Voltage	15	—	—	0.8		
V_{CSTH+}	CS Input Positive Going Threshold	16	150	230	320	mV	
V_{CSTH-}	CS Input Negative Going Threshold	17	130	200	260		
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	18	—	—	100		I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	19	—	—	100		I_O = 0A
I_{LK}	Offset Supply Leakage Current	20	—	—	50	µA	V_B = V_S = 500V
I_{QBS}	Quiescent V_{BS} Supply Current	21	—	400	1000		V_{IN} = V_{CS} = 0V or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	22	—	700	1200		V_{IN} = V_{CS} = 0V or 5V
I_{IN+}	Logic "1" Input Bias Current	23	—	4.5	10		V_{IN} = 5V
I_{IN-}	Logic "0" Input Bias Current	24	—	—	1.0		V_{IN} = 0V
I_{CS+}	"High" CS Bias Current	25	—	4.5	10		V_{CS} = 3V
I_{CS-}	"Low" CS Bias Current	26	—	—	1.0		V_{CS} = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	27	8.5	9.2	10.0	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	28	7.7	8.3	9.0		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	29	8.3	8.9	9.6		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	30	7.3	8.0	8.7		
I_{ERR}	ERR Timing Charge Current	31	65	100	130	µA	V_{IN} = 5V, V_{CS} = 3V ERR < V_{ERR+}
I_{ERR+}	ERR Pull-Up Current	32	8.0	15	—	mA	V_{IN} = 5V, V_{CS} = 3V ERR > V_{ERR+}
I_{ERR-}	ERR Pull-Down Current	33	16	30	—		V_{IN} = 0V
I_{O+}	Output High Short Circuit Pulsed Current	34	1.0	1.6	—	A	V_O = 0V, V_{IN} = 5V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	35	2.0	3.3	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

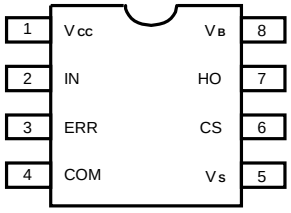
Functional Block Diagram



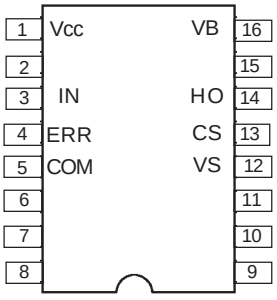
Lead Definitions

Symbol	Description
V_{CC}	Logic and gate drive supply
IN	Logic input for gate driver output (HO), in phase with HO
ERR	Serves multiple functions; status reporting, linear mode timing and cycle by cycle logic shutdown
COM	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
CS	Current sense input to current sense comparator

Lead Assignments



8 Lead PDIP



16 Lead SOIC (Wide Body)

IR2125	Part Number	IR2125S

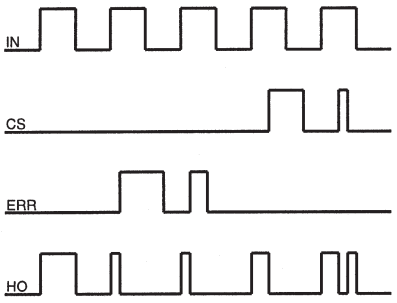


Figure 1. Input/Output Timing Diagram

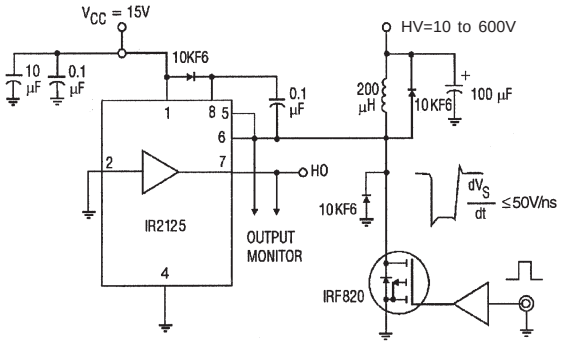


Figure 2. Floating Supply Voltage Transient Test Circuit

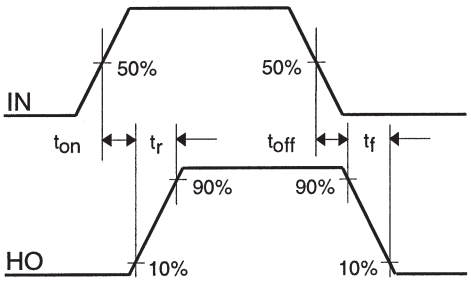


Figure 3. Switching Time Waveform Definitions

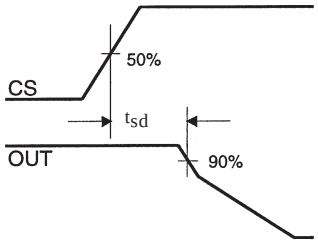


Figure 4. ERR Shutdown Waveform Definitions

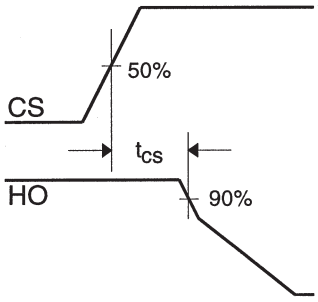
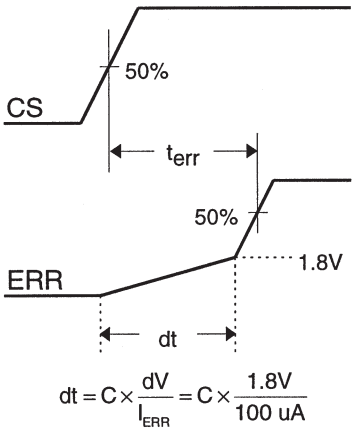


Figure 5. CS Shutdown Waveform Definitions



$$dt = C \times \frac{dV}{I_{ERR}} = C \times \frac{1.8V}{100\ uA}$$

Figure 6. CS to ERR Waveform Definitions

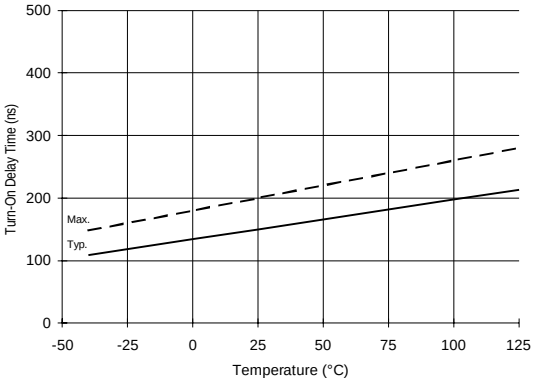


Figure 7A. Turn-On Time vs. Temperature

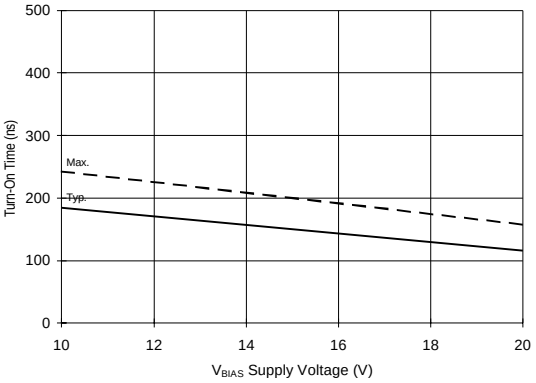


Figure 7B. Turn-On Time vs. Voltage

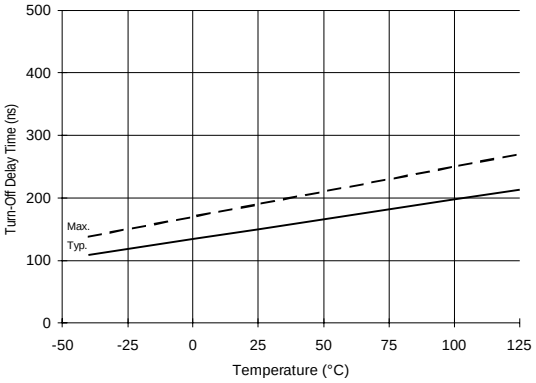


Figure 8A. Turn-Off Time vs. Temperature

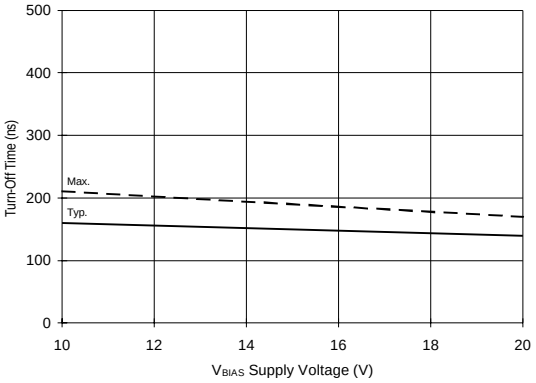


Figure 8B. Turn-Off Time vs. Voltage

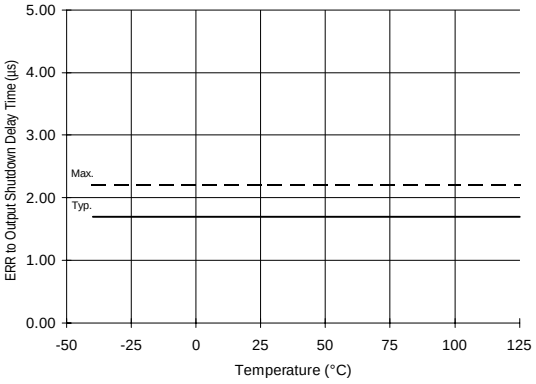


Figure 9A. ERR to Output Shutdown vs. Temperature

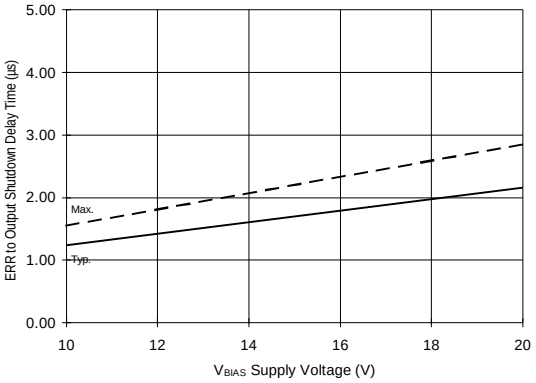


Figure 9B. ERR to Output Shutdown vs. Voltage

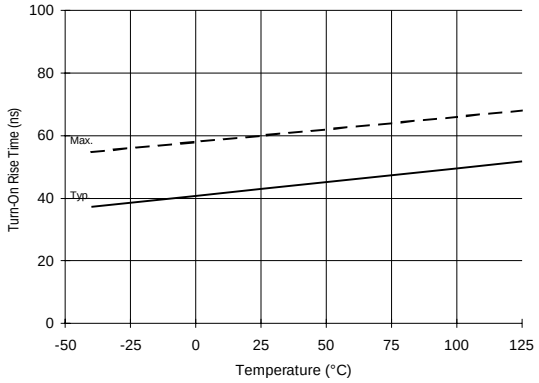


Figure 10A. Turn-On Rise Time vs. Temperature

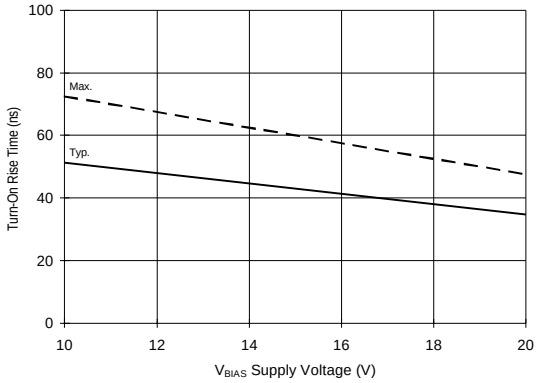


Figure 10B. Turn-On Rise Time vs. Voltage

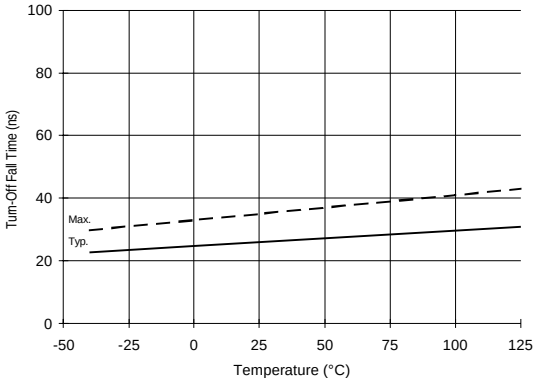


Figure 11A. Turn-Off Fall Time vs. Temperature

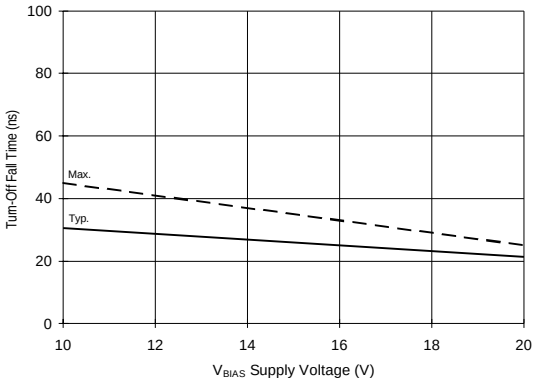


Figure 11B. Turn-Off Fall Time vs. Voltage

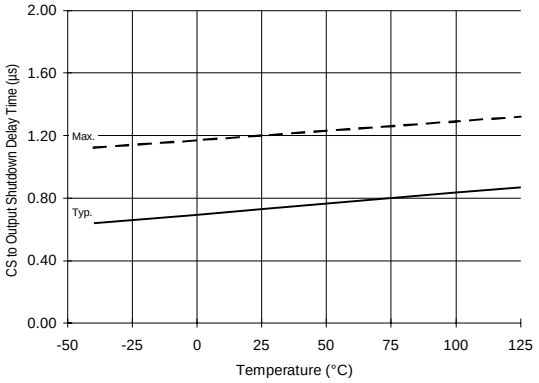


Figure 12A. CS to Output Shutdown vs. Temperature

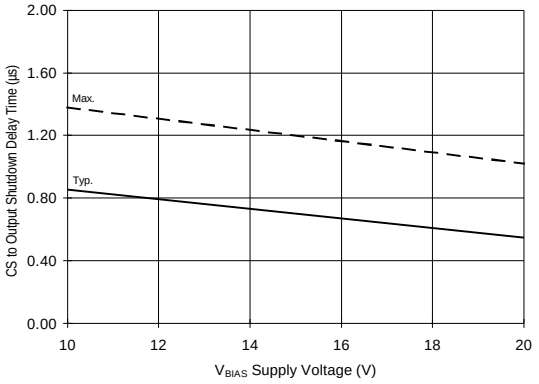


Figure 12B. CS to Output Shutdown vs. Voltage

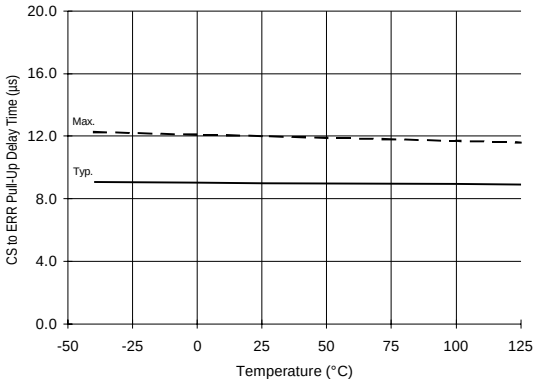


Figure 13A. CS to ERR Pull-Up vs. Temperature

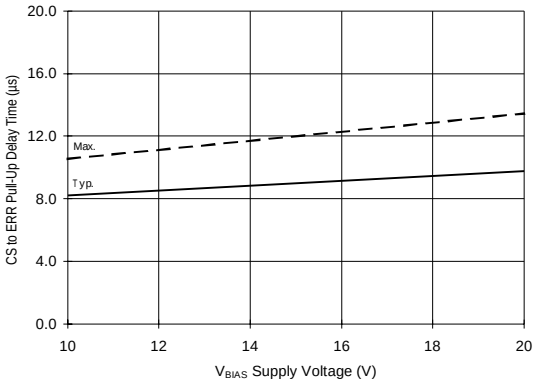


Figure 13B. CS to ERR Pull-Up vs. Voltage

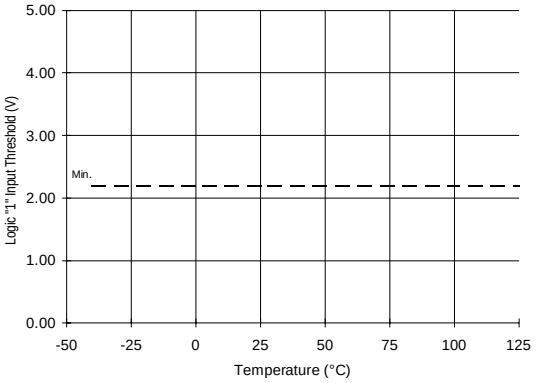


Figure 14A. Logic “1” Input Threshold vs. Temperature

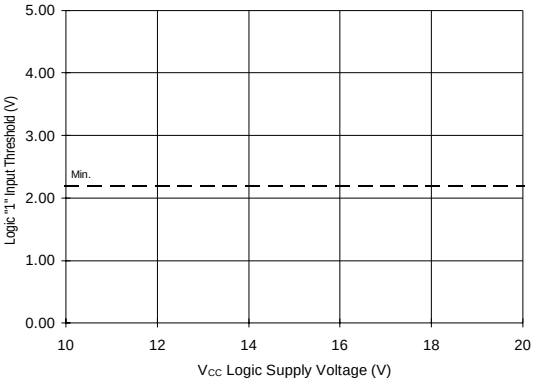


Figure 14B. Logic “1” Input Threshold vs. Voltage

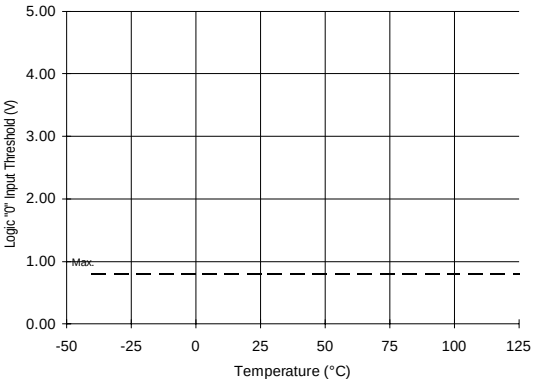


Figure 15A. Logic “0” Input Threshold vs. Temperature

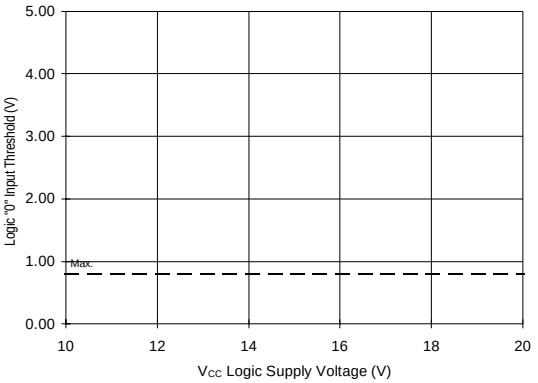


Figure 15B. Logic “0” Input Threshold vs. Voltage

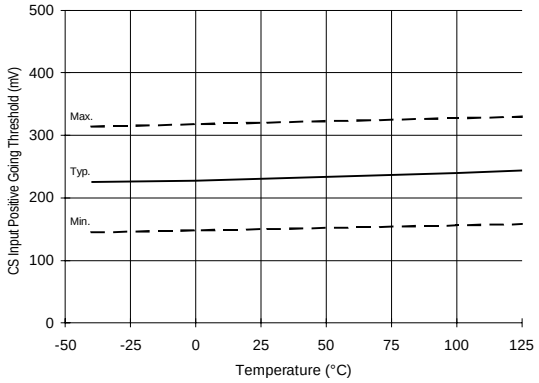


Figure 16A. CS Input Threshold (+) vs. Temperature

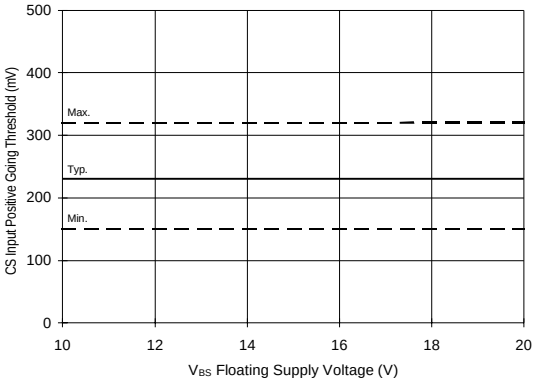


Figure 16B. CS Input Threshold (+) vs. Voltage

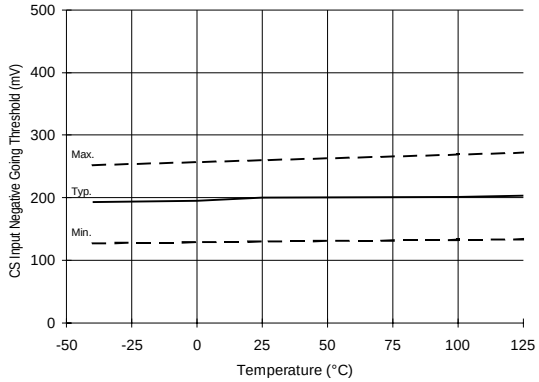


Figure 17A. CS Input Threshold (-) vs. Temperature

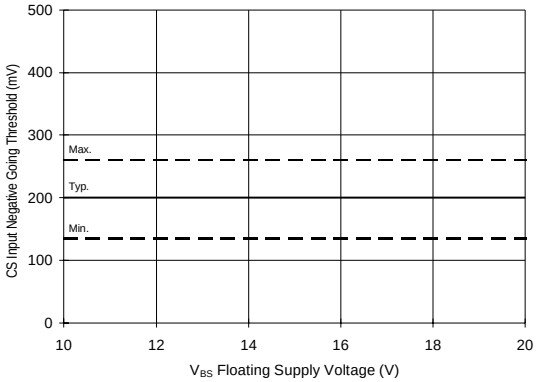


Figure 17B. CS Input Threshold (-) vs. Voltage

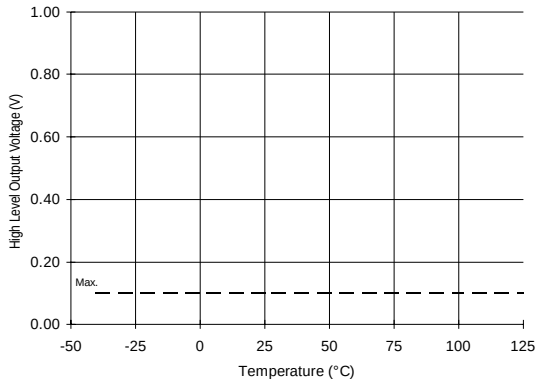


Figure 18A. High Level Output vs. Temperature

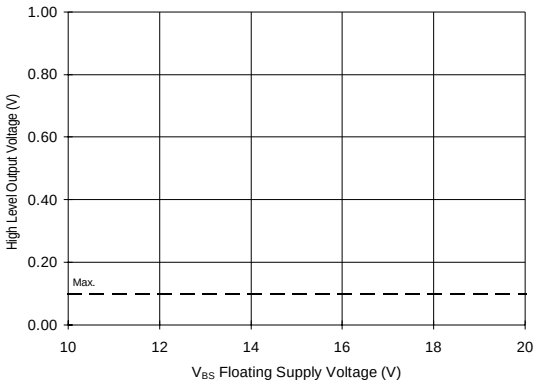


Figure 18B. High Level Output vs. Voltage

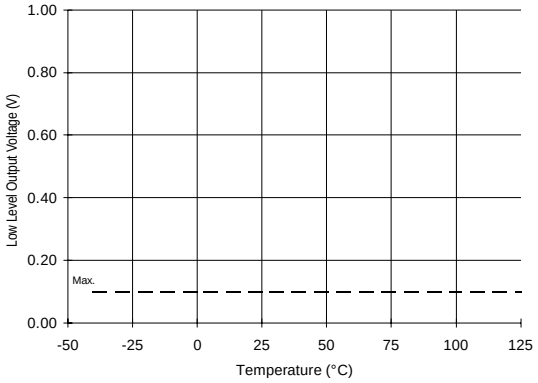


Figure 19A. Low Level Output vs. Temperature

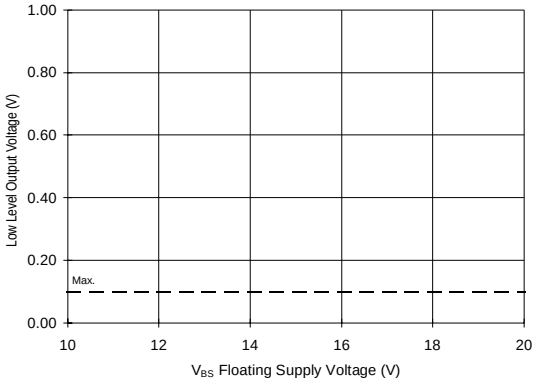


Figure 19B. Low Level Output vs. Voltage

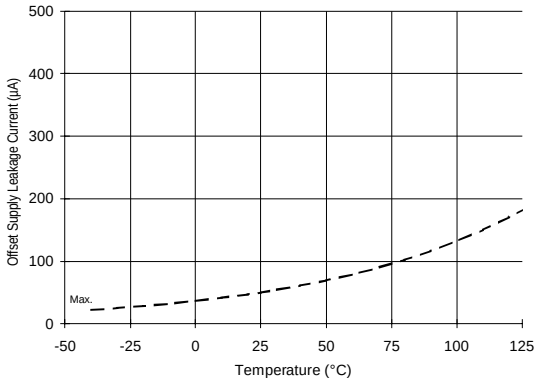


Figure 20A. Offset Supply Current vs. Temperature

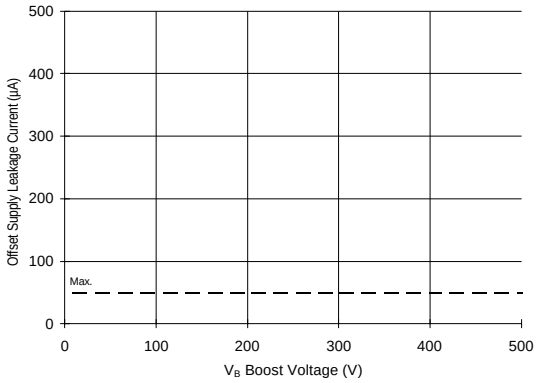


Figure 20B. Offset Supply Current vs. Voltage

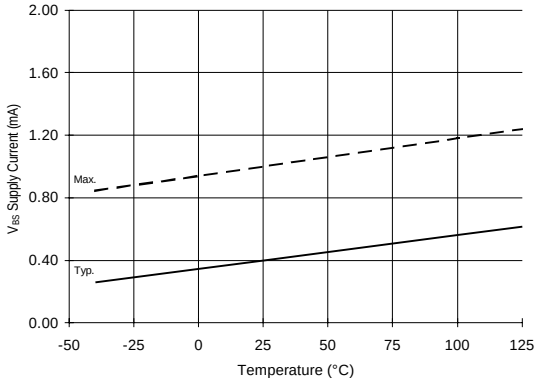


Figure 21A. V_{BS} Supply Current vs. Temperature

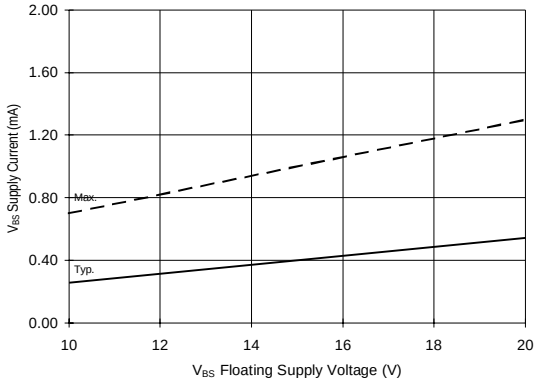


Figure 21B. V_{BS} Supply Current vs. Voltage

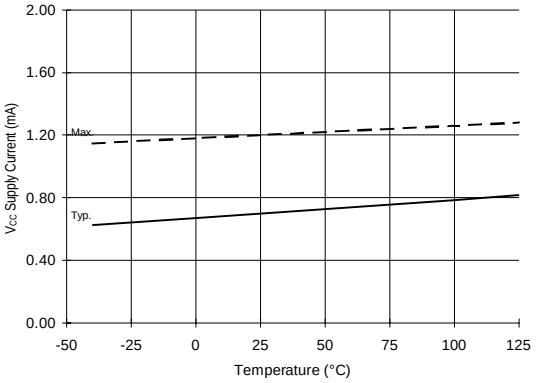


Figure 22A. V_{CC} Supply Current vs. Temperature

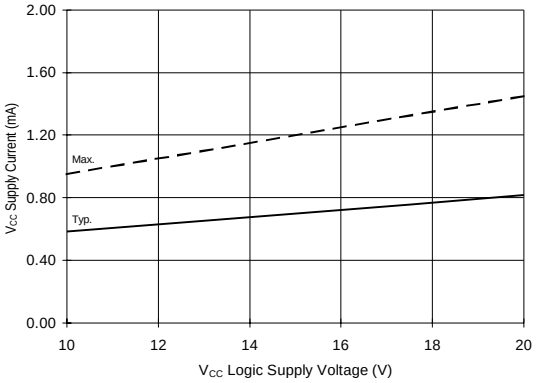


Figure 22B. V_{CC} Supply Current vs. Voltage

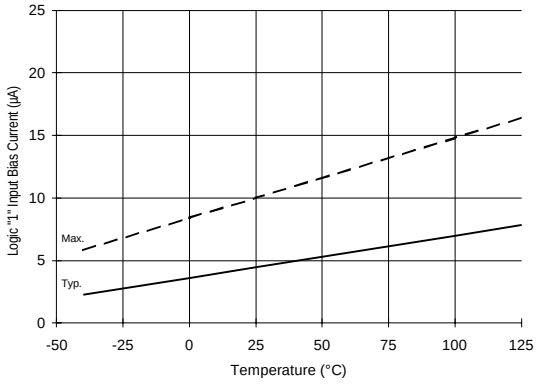


Figure 23A. Logic "1" Input Current vs. Temperature

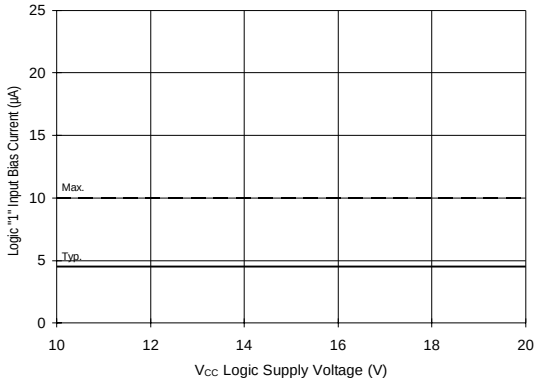


Figure 23B. Logic "1" Input Current vs. Voltage

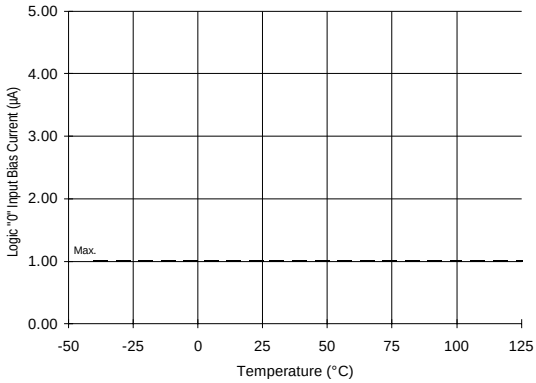


Figure 24A. Logic "0" Input Current vs. Temperature

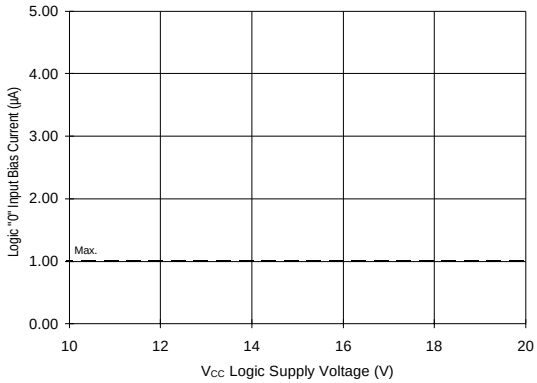


Figure 24B. Logic "0" Input Current vs. Voltage

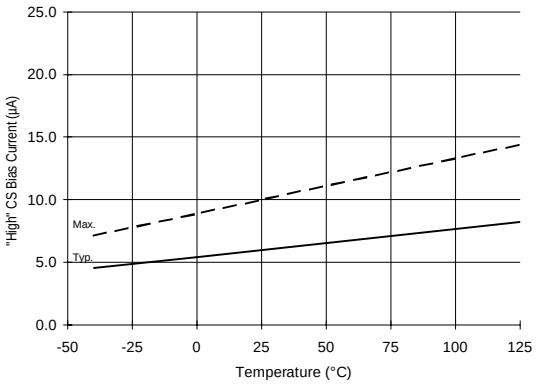


Figure 25A. "High" CS Bias Current vs. Temperature

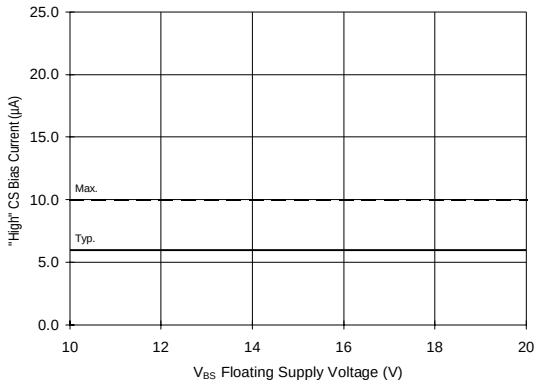


Figure 25B. "High" CS Bias Current vs. Voltage

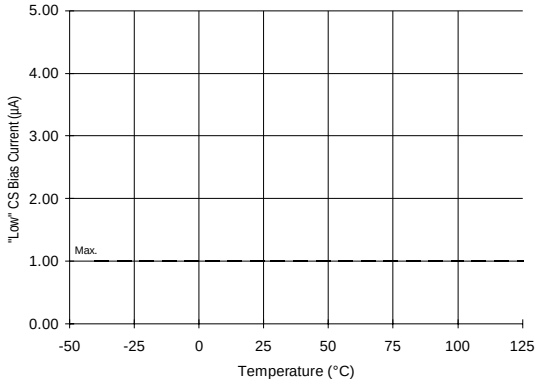


Figure 26A. "Low" CS Bias Current vs. Temperature

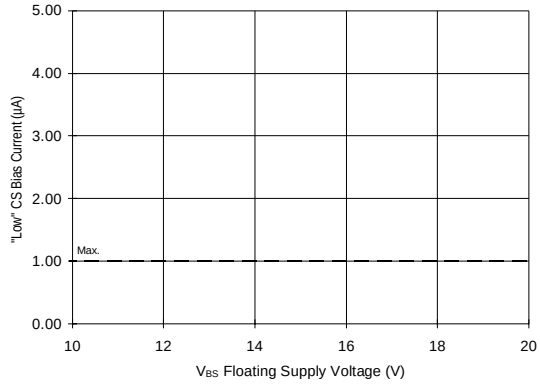


Figure 26B. "Low" CS Bias Current vs. Voltage

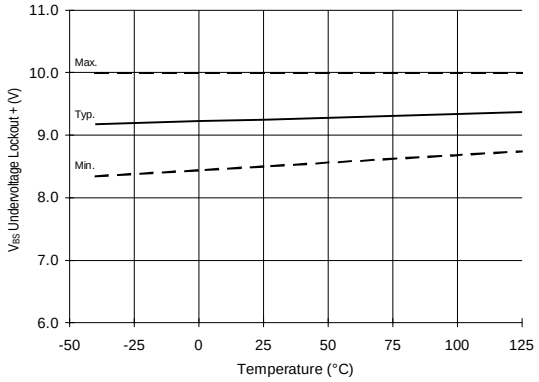


Figure 27. V_{BS} Undervoltage (+) vs. Temperature

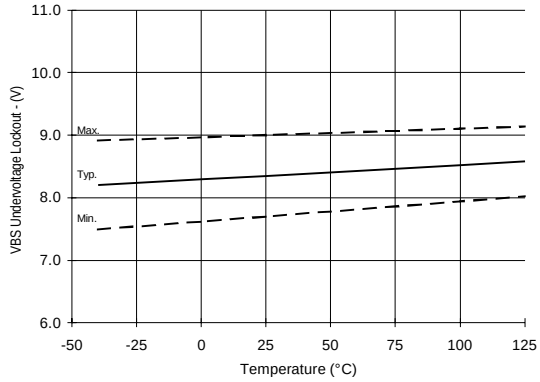


Figure 28. V_{BS} Undervoltage (-) vs. Temperature

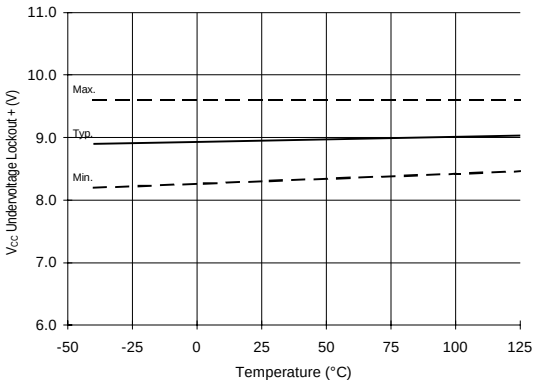


Figure 29. V_{CC} Undervoltage (+) vs. Temperature

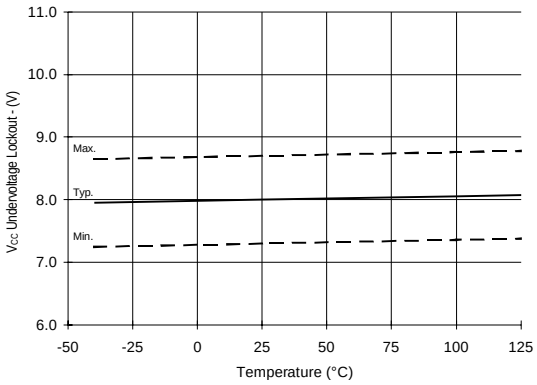


Figure 30. V_{CC} Undervoltage (-) vs. Temperature

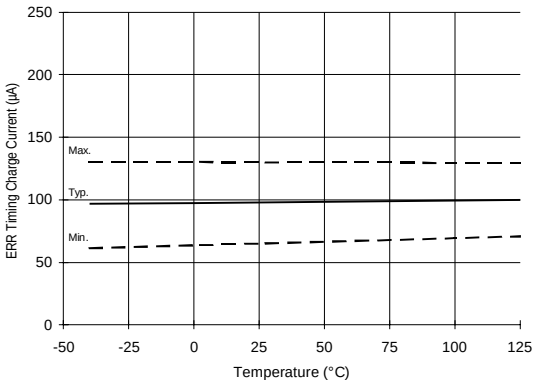


Figure 31A. ERR Timing Charge Current vs. Temperature

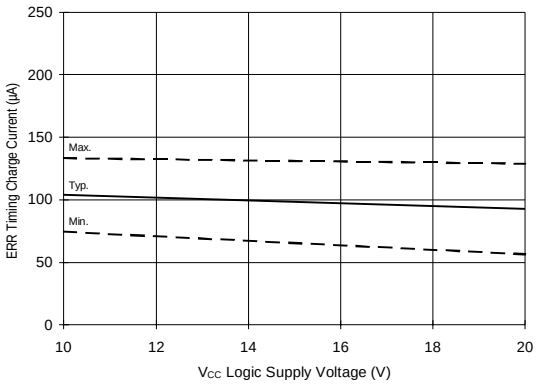


Figure 31B. ERR Timing Charge Current vs. Voltage

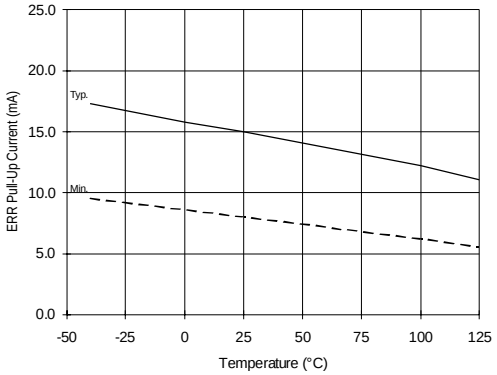


Figure 32A. ERR Pull-Up Current vs. Temperature

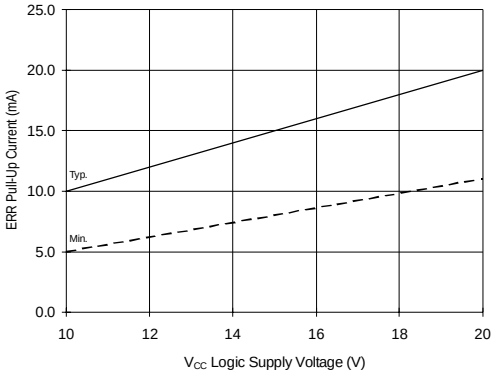


Figure 32B. ERR Pull-Up Current vs. Voltage

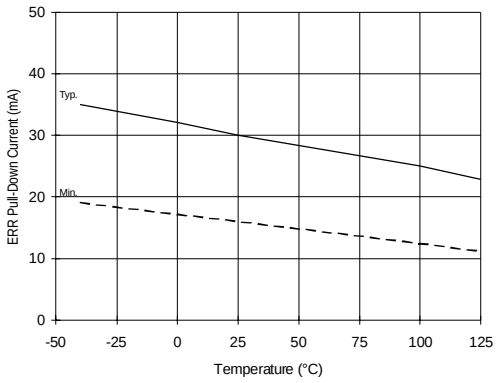


Figure 33A. ERR Pull-Down Current vs.Temperature

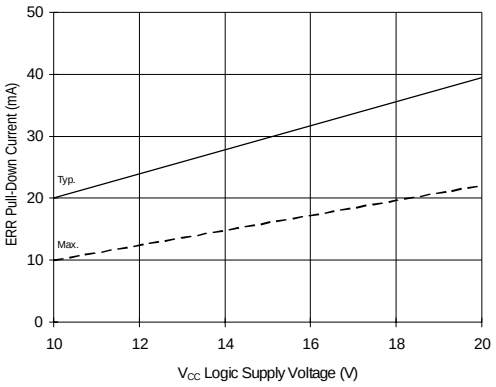


Figure 33B. ERR Pull-Down Current vs. Voltage

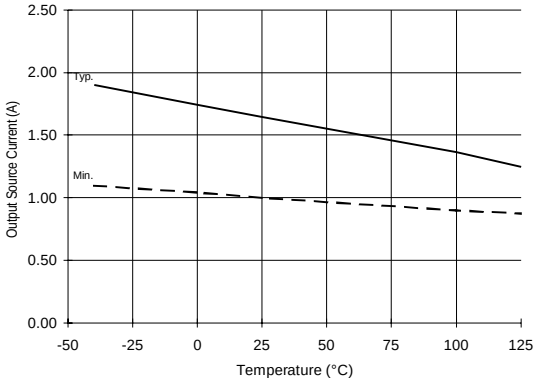


Figure 34A. Output Source Current vs. Temperature

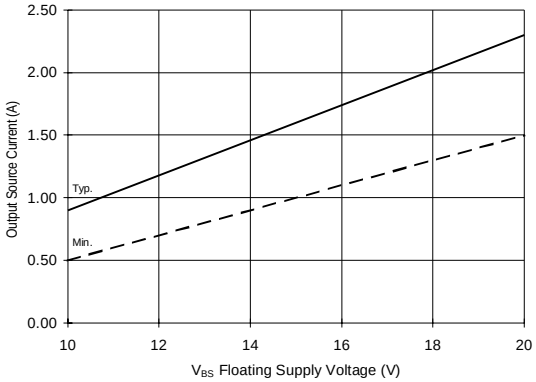


Figure 34B. Output Source Current vs. Voltage

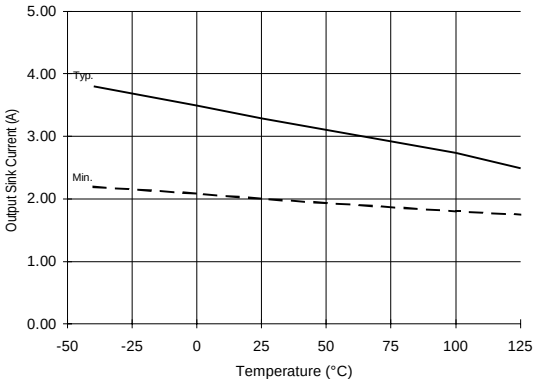


Figure 35A. Output Sink Current vs.Temperature

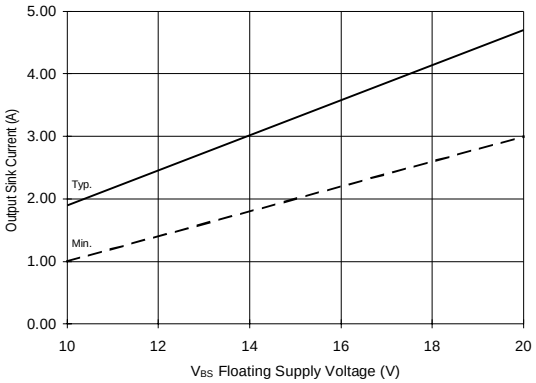


Figure 35B. Output Sink Current vs. Voltage

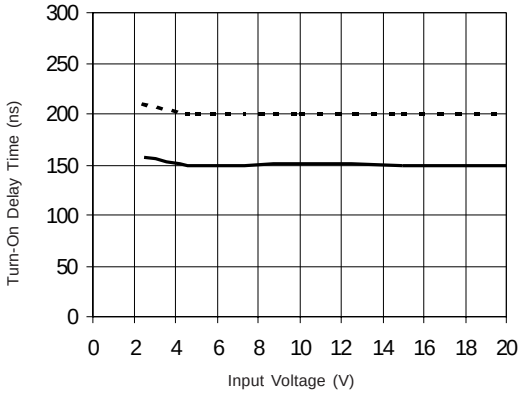


Figure 36A. Turn-On Time vs. Input Voltage

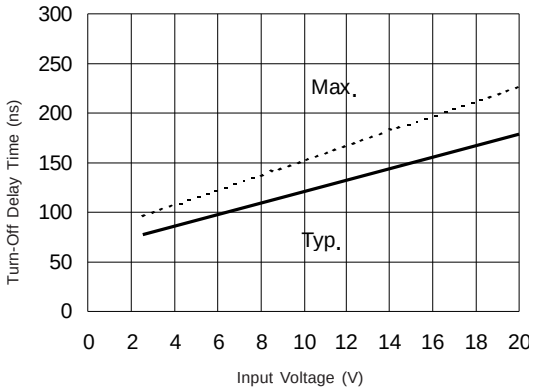


Figure 36B. Turn-Off Time vs. Input Voltage

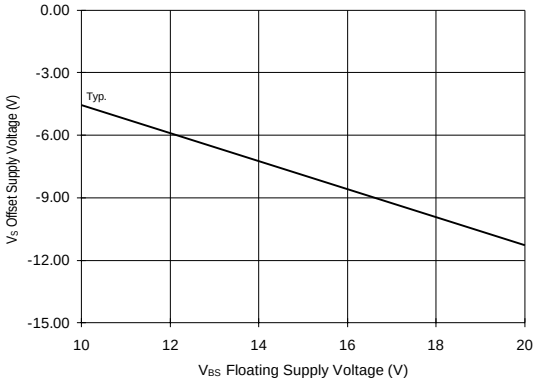
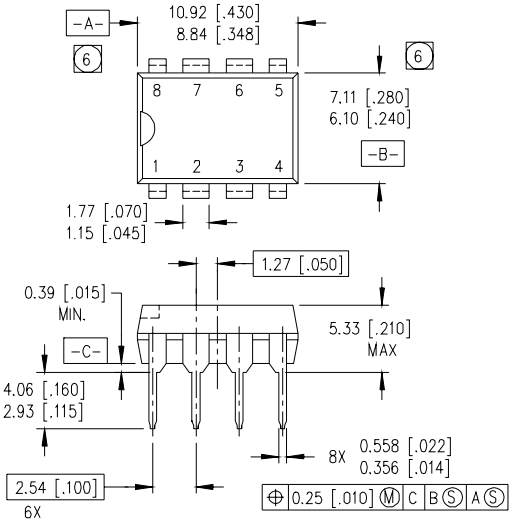
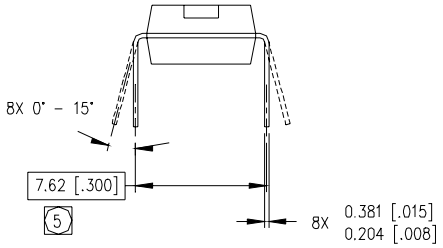


Figure 37. Maximum V_S Negative Offset vs. Supply Voltage

Case outlines

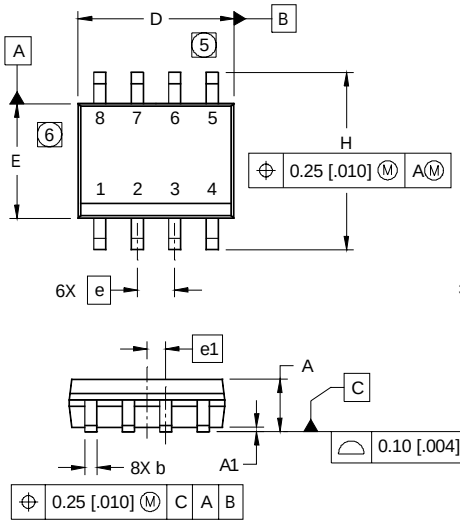


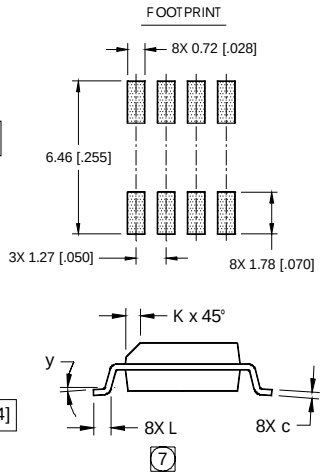
NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8-Lead PDIP

01-6014
01-3003 01 (MS-001AB)





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8-Lead SOIC

01-6027
01-0021 11 (MS-012AA)

WORLD HEADQUARTERS: 233 Kansas Street, El Segundo, California 90245 Tel: (310) 252-7105
Data and specifications subject to change without notice. 5/15/2001

International
IOR Rectifier

Data Sheet No. PD60143-N

IR2127(S) / IR2128(S)
IR21271(S)

CURRENT SENSING SINGLE CHANNEL DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage dV/dt immune
- Application- specific gate drive range:
  Motor Drive: 12 to 20V (IR2127/IR2128)
  Automotive: 9 to 20V (IR21271)
- Undervoltage lockout
- 3.3V, 5V and 15V input logic compatible
- $\overline{\text{FAULT}}$ lead indicates shutdown has occured
- Output in phase with input (IR2127/IR21271)
- Output out of phase with input (IR2128)

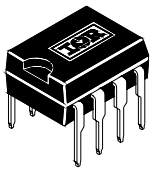
Description

The IR2127/IR2128/IR21271(S) is a high voltage, high speed power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL outputs, down to 3.3V. The protection circuity detects over-current in the driven power transistor and terminates the gate drive voltage. An open drain $\overline{\text{FAULT}}$ signal is provided to indicate that an over-current shutdown has occurred. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side or low side configuration which operates up to 600 volts.

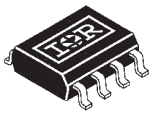
Product Summary

V_{OFFSET}	600V max.	
I_O+/-	200 mA / 420 mA	
V_{OUT}	12 - 20V (IR2127/IR2128)	9 - 20V (IR21271)
V_{CSth}	250 mV or 1.8V	
$t_{on/off}$ (typ.)	200 & 150 ns	

Packages

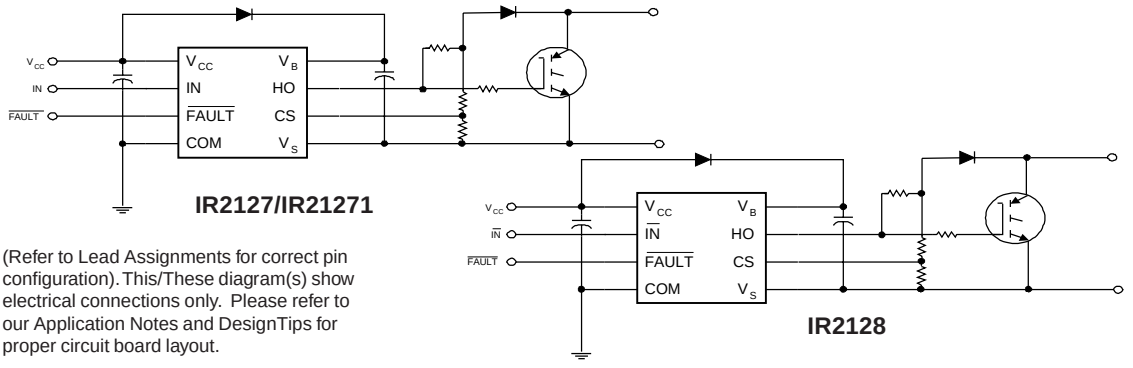


8-Lead PDIP



8-Lead SOIC

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High Side Floating Supply Voltage		-0.3	625	V
V_S	High Side Floating Offset Voltage		V_B - 25	V_B + 0.3	
V_{HO}	High Side Floating Output Voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Logic Supply Voltage		-0.3	25	
V_{IN}	Logic Input Voltage		-0.3	V_{CC} + 0.3	
V_{FLT}	$\overline{\text{FAULT}}$ Output Voltage		-0.3	V_{CC} + 0.3	
V_{CS}	Current Sense Voltage		V_S - 0.3	V_B + 0.3	
dV_s/dt	Allowable Offset Supply Voltage Transient		—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$	(8 Lead DIP)	—	1.0	W
		(8 Lead SOIC)	—	0.625	
Rth_{JA}	Thermal Resistance, Junction to Ambient	(8 Lead DIP)	—	125	°C/W
		(8 Lead SOIC)	—	200	
T_J	Junction Temperature		—	150	°C
T_S	Storage Temperature		-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition		Min.	Max.	Units
V_B	High Side Floating Supply Voltage	(IR2127/IR2128)	V_S + 12	V_S + 20	V
		(IR21271)	V_S + 9	V_S + 20	
V_S	High Side Floating Offset Voltage		Note 1	600	
V_{HO}	High Side Floating Output Voltage		V_S	V_B	
V_{CC}	Logic Supply Voltage		10	20	
V_{IN}	Logic Input Voltage		0	V_{CC}	
V_{FLT}	$\overline{\text{FAULT}}$ Output Voltage		0	V_{CC}	
V_{CS}	Current Sense Signal Voltage		V_S	V_S + 5	
T_A	Ambient Temperature		-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

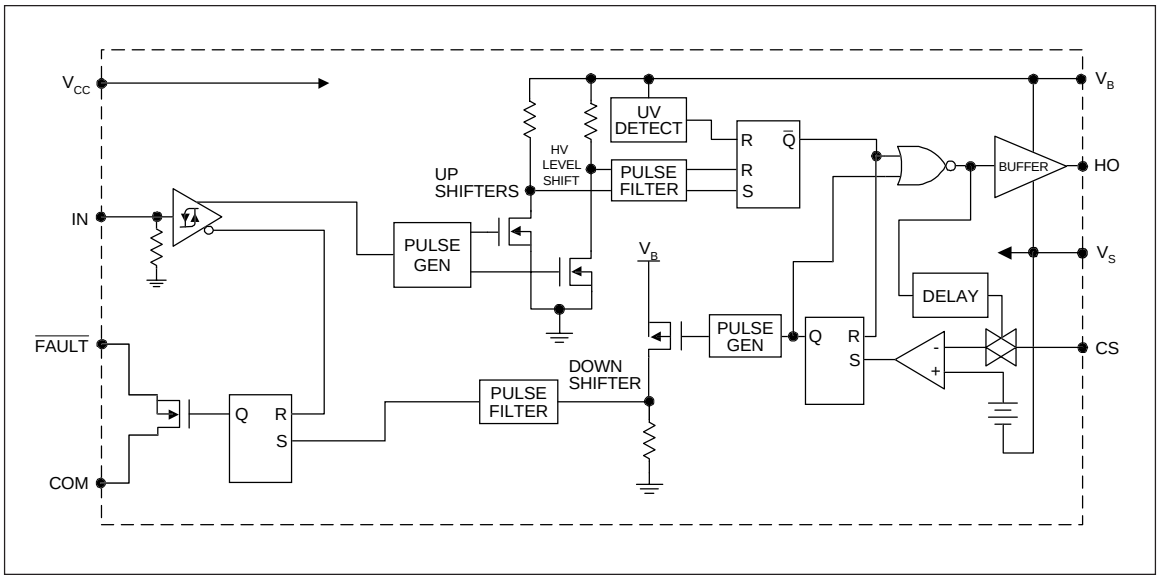
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	—	200	250	ns	V_S = 0V
t_{off}	Turn-Off Propagation Delay	—	150	200		V_S = 600V
t_r	Turn-On Rise Time	—	80	130		
t_f	Turn-Off Fall Time	—	40	65		
t_{bl}	Start-Up Blanking Time	500	700	900		
t_{cs}	CS Shutdown Propagation Delay	—	240	360		
t_{flt}	CS to $\overline{\text{FAULT}}$ Pull-Up Propagation Delay	—	340	510		

Static Electrical Characteristics

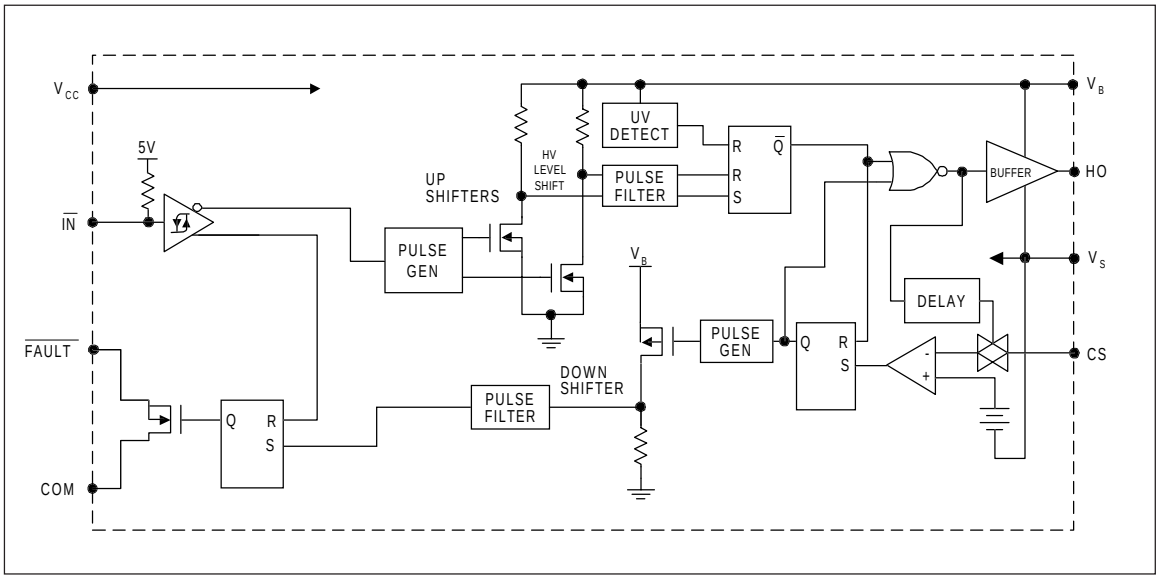
V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S.

Symbol	Definition		Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” Input Voltage Logic “0” Input Voltage	(IR2127/IR21271) (IR2128)	3.0	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic “0” Input Voltage Logic “1” Input Voltage	(IR2127/IR21271) (IR2128)	—	—	0.8	V	V_{CC} = 10V to 20V
V_{CSTH+}	CS Input Positive Going Threshold	(IR2127/IR2128) (IR21271)	180 —	250 1.8	320 —	mV V	V_{CC} = 10V to 20V
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O		—	—	100	mV	I_O = 0A
V_{OL}	Low Level Output Voltage, V_O		—	—	100	mV	I_O = 0A
I_{LK}	Offset Supply Leakage Current		—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} Supply Current		—	200	400	µA	V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} Supply Current		—	60	120	µA	V_{IN} = 0V or 5V
I_{IN+}	Logic “1” Input Bias Current		—	7.0	15	µA	V_{IN} = 5V
I_{IN-}	Logic “0” Input Bias Current		—	—	1.0	µA	V_{IN} = 0V
I_{CS+}	“High” CS Bias Current		—	—	1.0	µA	V_{CS} = 3V
I_{CS-}	“High” CS Bias Current		—	—	1.0	µA	V_{CS} = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	(IR2127/IR2128) (IR21271)	8.8 6.3	10.3 7.2	11.8 8.2	V V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	(IR2127/IR2128) (IR21271)	7.5 6.0	9.0 6.8	10.6 7.7	V V	
I_{O+}	Output High Short Circuit Pulsed Current		200	250	—	mA	V_O = 0V, V_{IN} = 5V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current		420	500	—	mA	V_O = 15V, V_{IN} = 0V PW ≤ 10 µs
Ron, FLT	FAULT - Low on Resistance		—	125	—	Ω	

Functional Block Diagram IR2127/IR21271



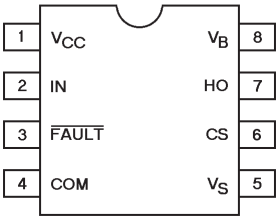
Functional Block Diagram IR2128



Lead Definitions

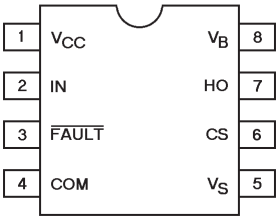
Symbol	Description
V_{CC}	Logic and gate drive supply
IN	Logic input for gate driver output (HO), in phase with HO (IR2127/IR21271) out of phase with HO (IR2128)
$\overline{FAULT}$	Indicates over-current shutdown has occurred, negative logic
COM	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
CS	Current sense input to current sense comparator

Lead Assignments



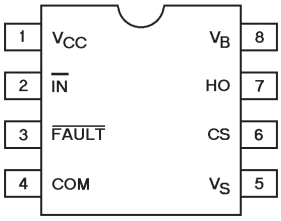
8 Lead PDIP

IR2127/IR21271



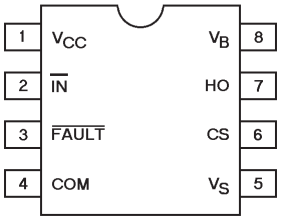
8 Lead SOIC

IR2127S/IR21271S



8 Lead PDIP

IR2128



8 Lead SOIC

IR2128S

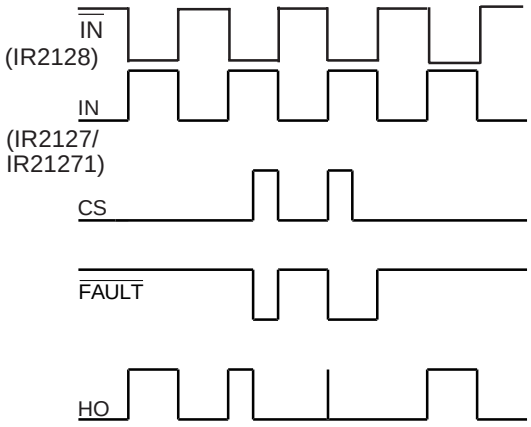


Figure 1. Input/Output Timing Diagram

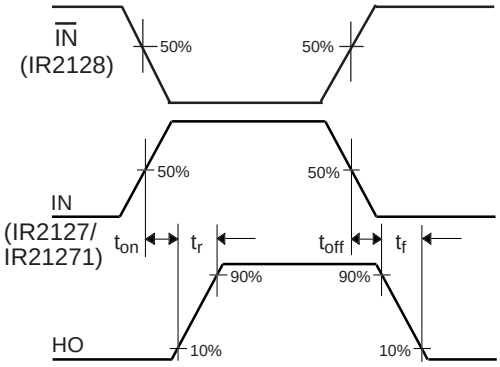


Figure 2. Switching Time Waveform Definition

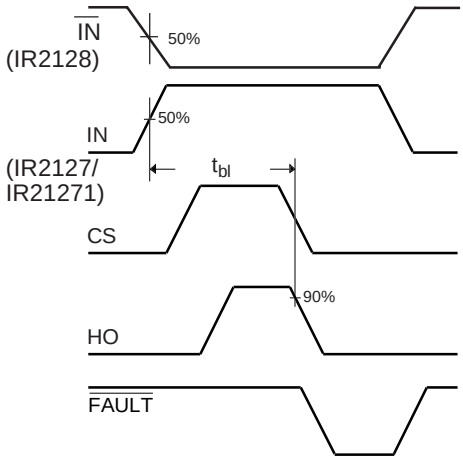


Figure 3. Start-up Blanking Time Waveform Definitions

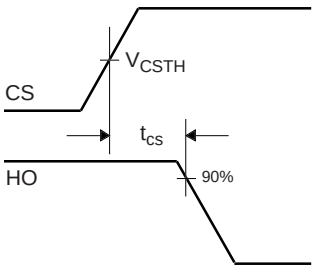


Figure 4. CS Shutdown Waveform Definitions

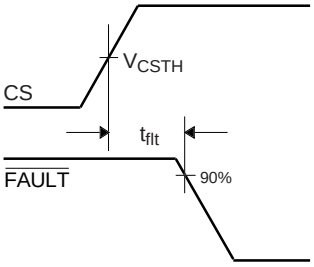


Figure 5. CS to $\overline{\text{FAULT}}$ Waveform Definitions

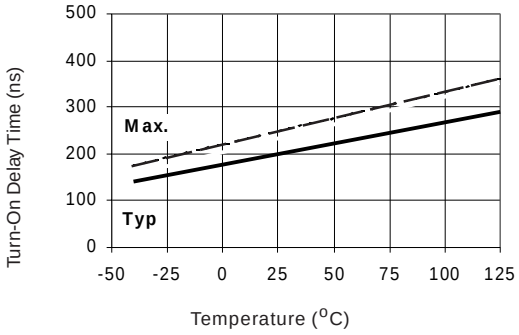


Figure 10A Turn-On Time vs. Temperature

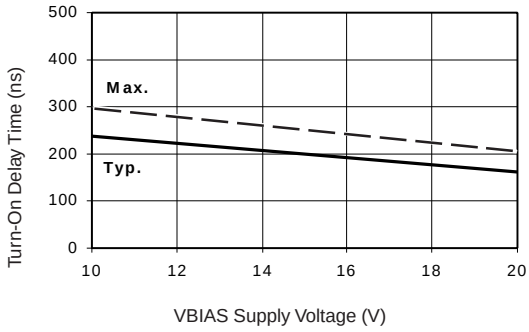


Figure 10B Turn-On Time vs. Supply Voltage

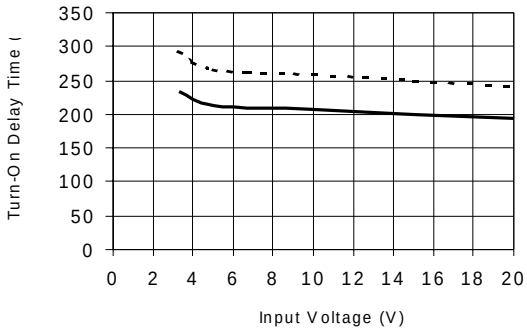


Figure 10C Turn-On Time vs. Input Voltage

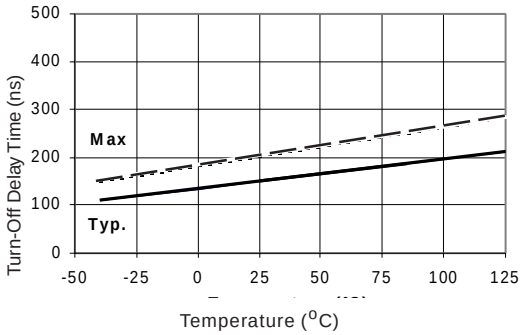


Figure 11A Turn-Off Time vs. Temperature

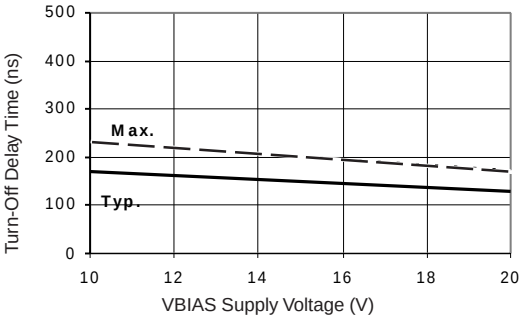


Figure 11B Turn-Off Time vs. Supply Voltage

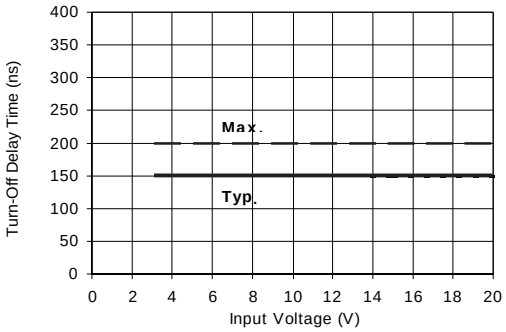


Figure 11C Turn-OffTime vs. Input Voltage

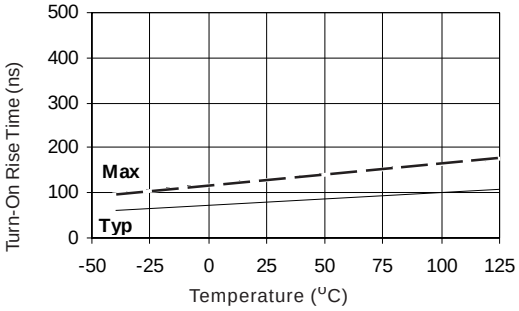


Figure 12A Turn-On Rise Time vs. Temperature

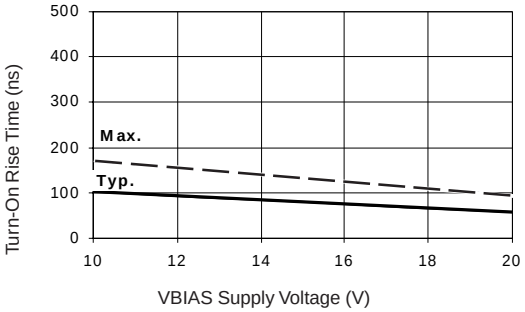


Figure 12B Turn-On Rise Time vs. Supply Voltage

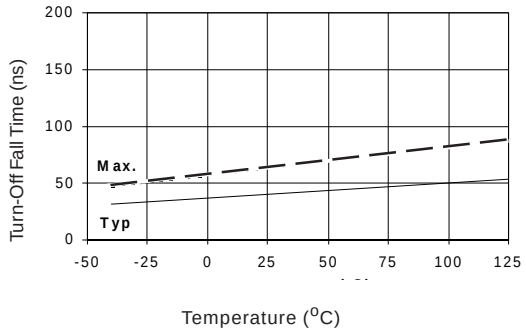


Figure 13A Turn-Off Fall Time vs. Temperature

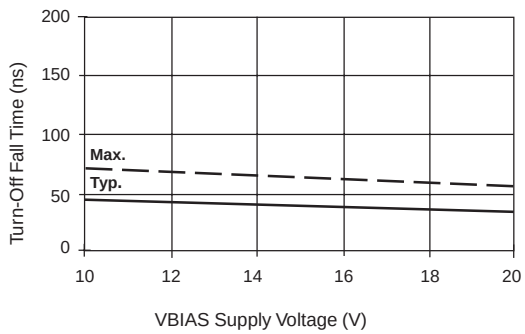


Figure 13B Turn-Off Fall Time vs. Voltage

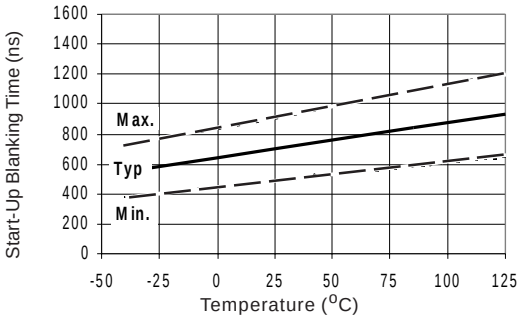


Figure 14A Start-Up Blanking Time vs. Temperature

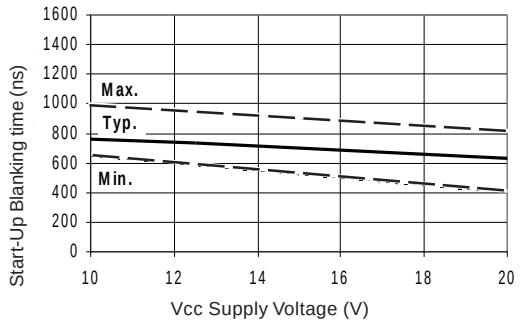


Figure 14B Start-Up Blanking Time vs Voltage

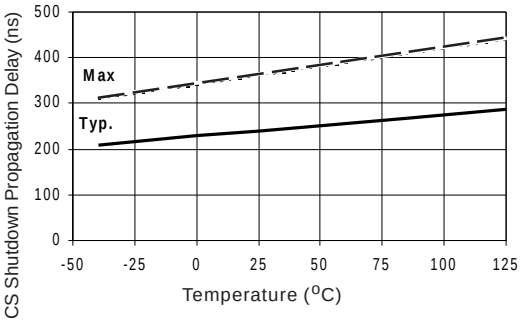


Figure 15A CS Shutdown Propagation Delay vs. Temperature

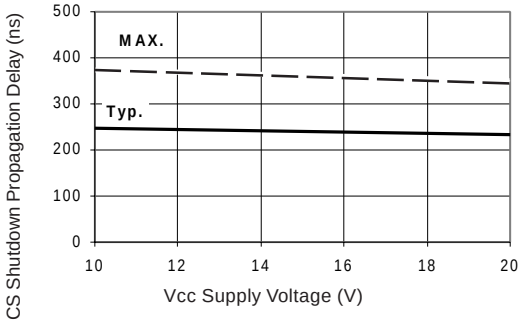


Figure 15B CS Shutdown Propagation Delay vs. Voltage

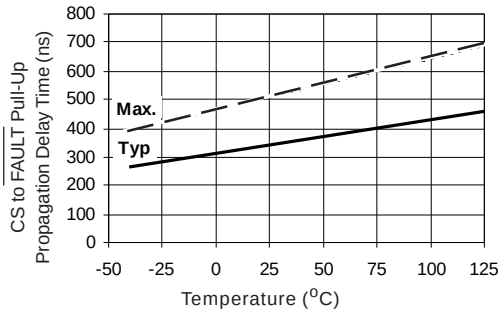


Figure 16A CS to $\overline{\text{FAULT}}$ Pull-Up Propagation Delay vs. Temperature

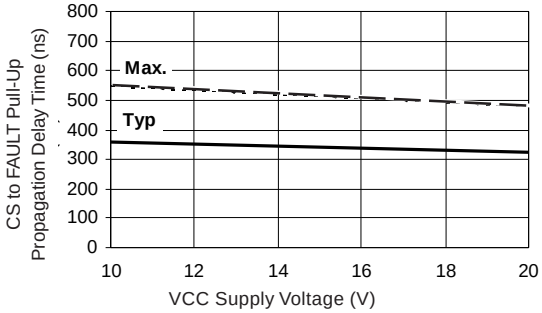


Figure 16B CS to $\overline{\text{FAULT}}$ Pull-Up Propagation Delay vs. Voltage

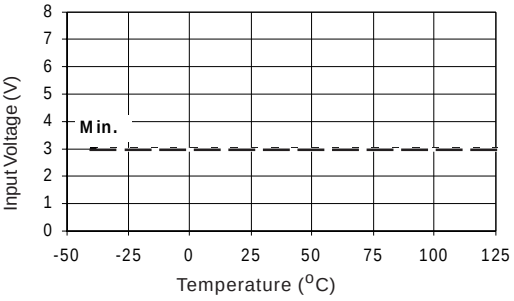


Figure 17A Logic "1" Input Voltage (IR2127) Logic "0" Input Voltage (IR2128) vs Temperature

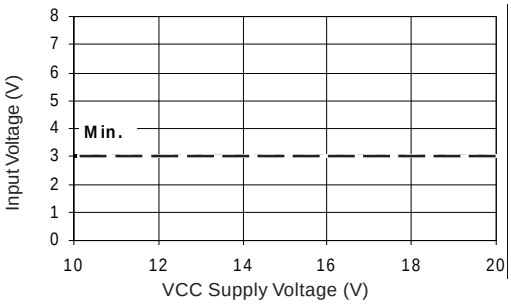


Figure 17B Logic "1" Input Voltage (IR2127) Logic "0" Input Voltage (IR2128) vs Voltage

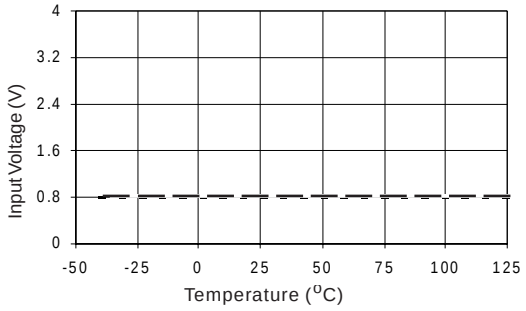


**Figure 18A Logic "0" Input Voltage (IR2127)
Logic "1" Input Voltage (IR2128)
vs Temperature**

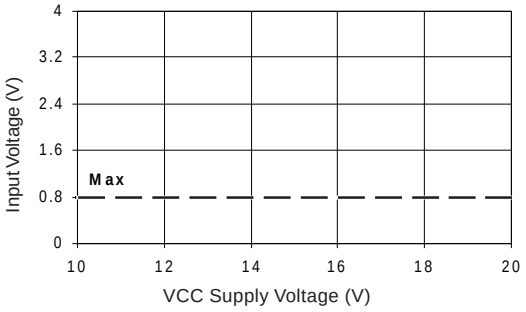


**Figure 18B Logic "0" Input Voltage (IR2127)
Logic "1" Input Voltage (IR2128)
vs Voltage**

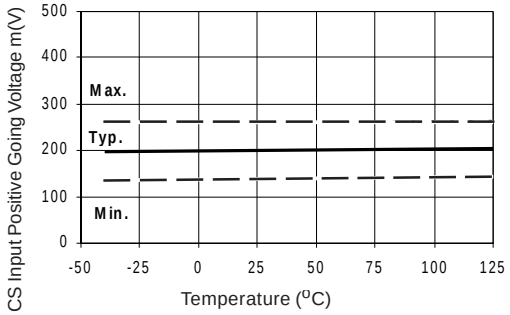


**Figure 19A CS Input Positive Going Voltage
vs Temperature (IR2127/IR2128)**

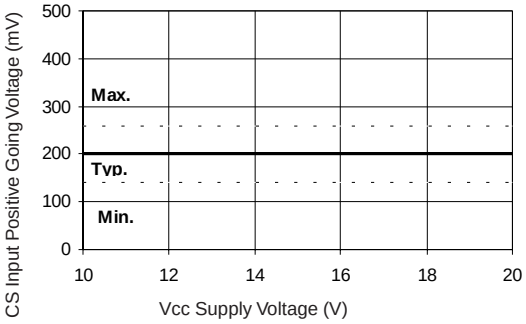


**Figure 19B CS Input Positive Going Voltage
vs Voltage (IR2127/IR2128)**

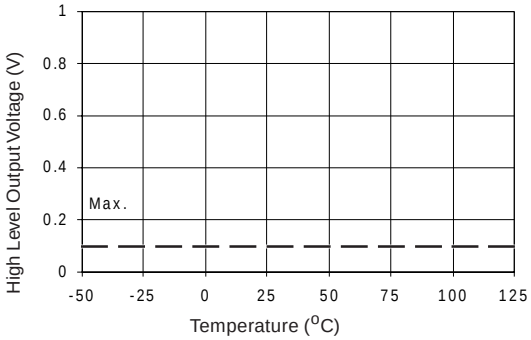


Figure 20A High Level Output vs Temperature

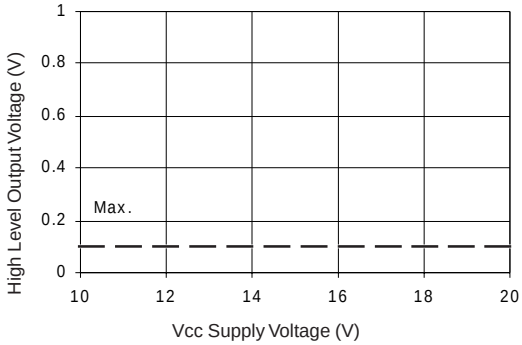


Figure 20B High Level Output vs Voltage

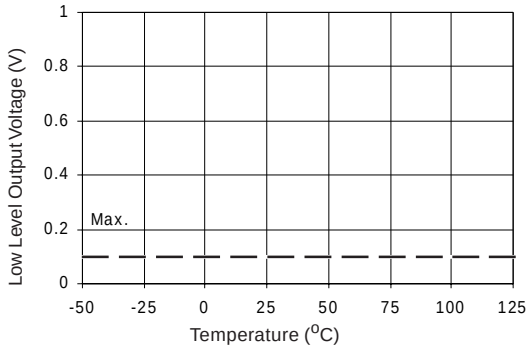


Figure 21A Low Level Output vs Temperature

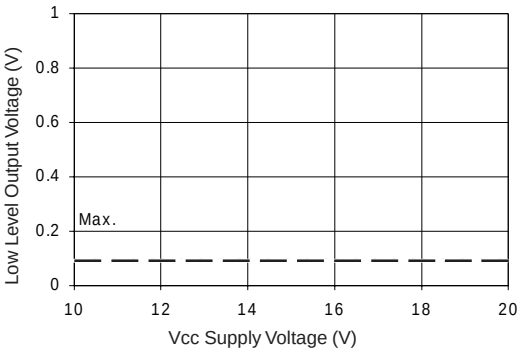


Figure 21B Low Level Output vs Voltage

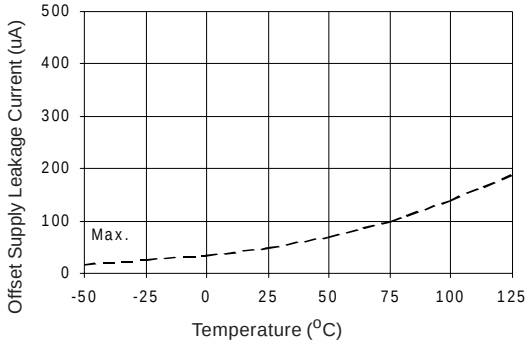


Figure 22A Offset Supply Current vs Temperature

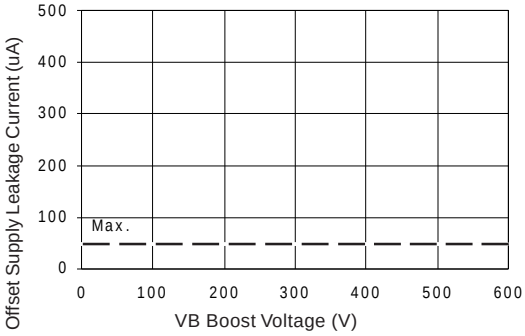


Figure 22B Offset Supply Current vs Voltage

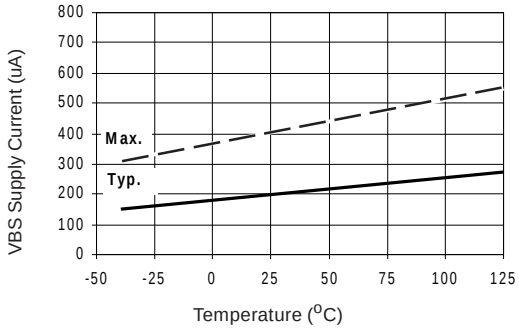


Figure 23A VBS Supply Current vs Temperature

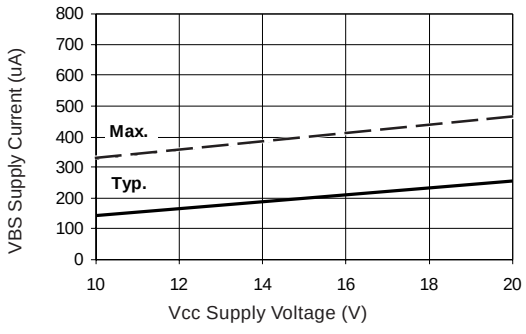


Figure 23B VBS Supply Current vs Voltage

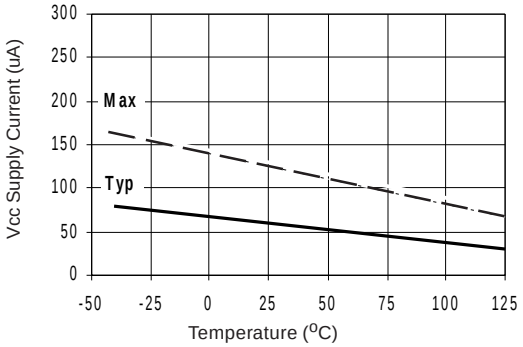


Figure 24A Vcc Supply Current vs Temperature

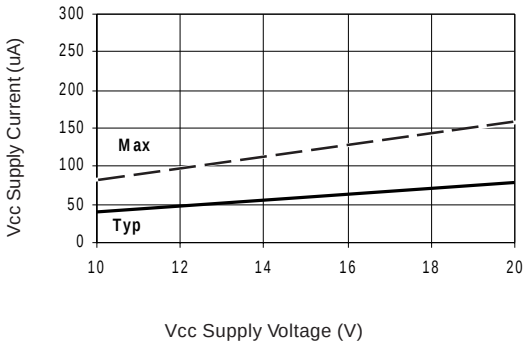


Figure 24B Vcc Supply Current vs Voltage

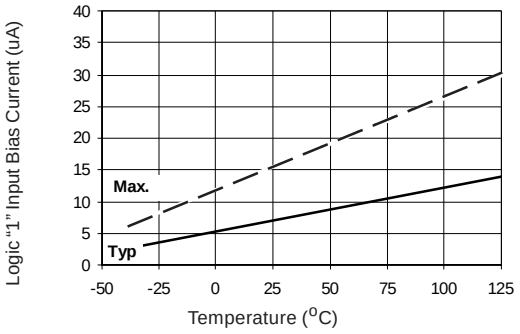


Figure 25A Logic "1" Input Current vs Temperature

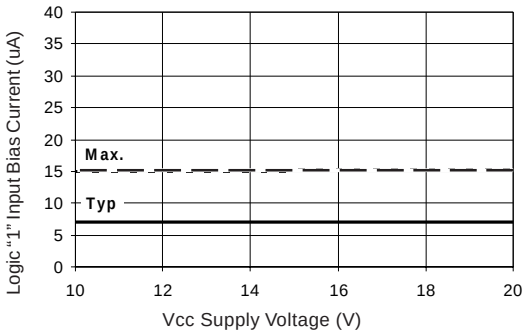


Figure 25B Logic "1" Input Current vs Voltage

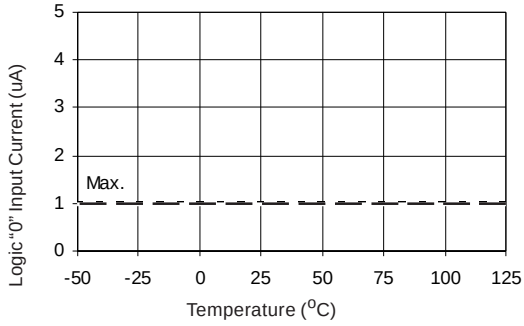


Figure 26A Logic "0" Input Current vs Temperature

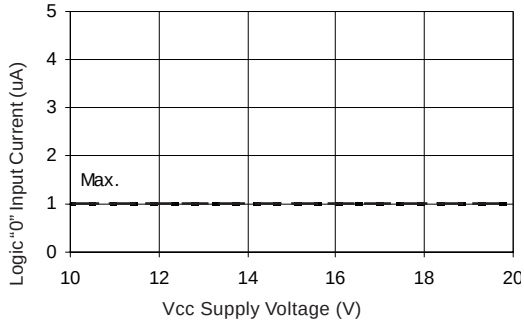


Figure 26B Logic "0" Input Current vs Voltage

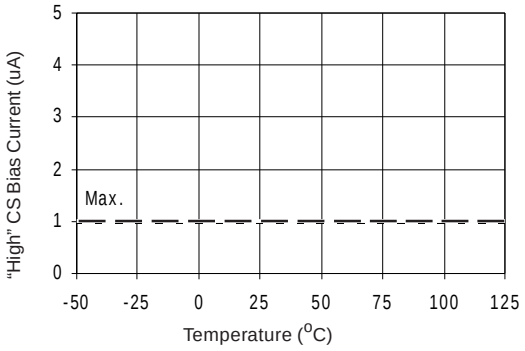


Figure 27A "High" CS Bias Current vs Temperature

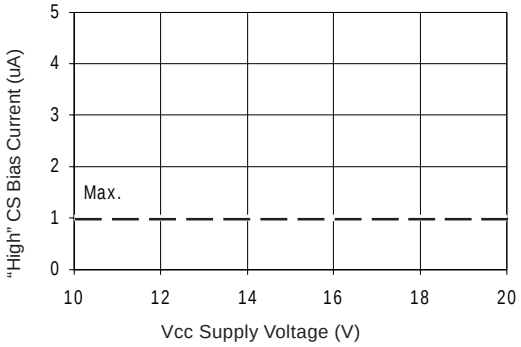


Figure 27B "High" CS Bias Current vs Voltage

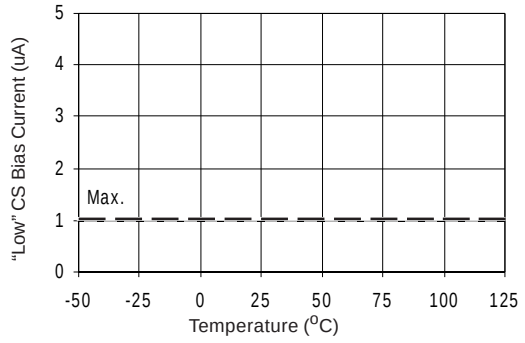


Figure 28A "Low" CS Bias Current vs Temperature

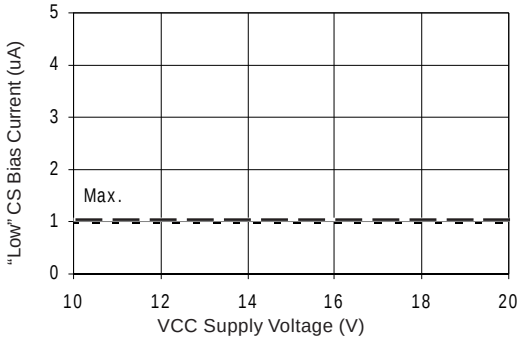


Figure 28B "Low" CS Bias Current vs Voltage

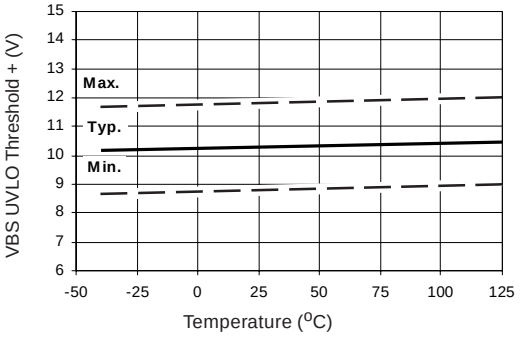


Figure 29A VBS Undervoltage Threshold (+) vs Temperature (IR2127/IR2128)

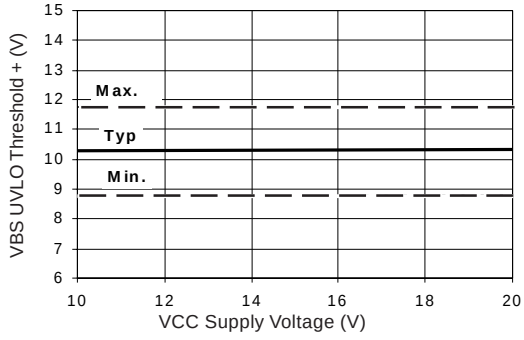


Figure 29B VBS Undervoltage Threshold (+) vs Voltage (IR2127/IR2128)

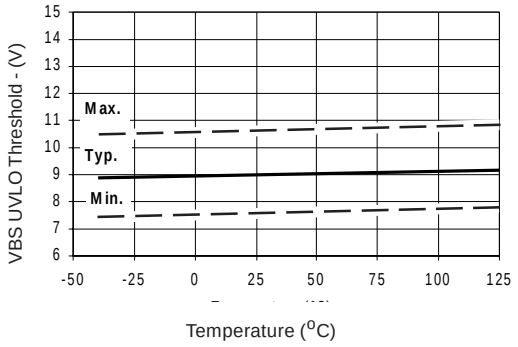


Figure 30A VBS Undervoltage Threshold (-) vs Temperature (IR2127/IR2128)

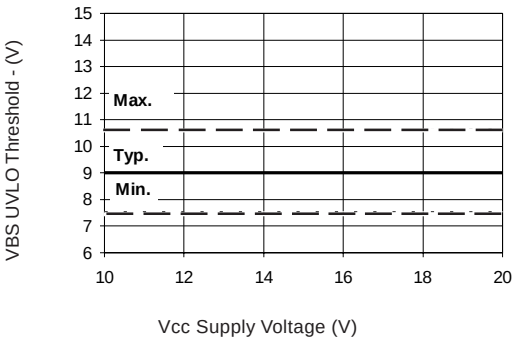


Figure 30B VBS Undervoltage Threshold (-) vs Voltage (IR2127/IR2128)

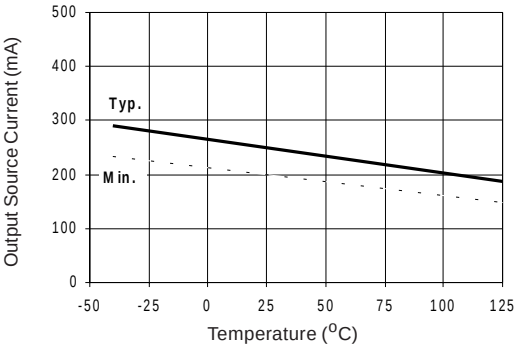


Figure 31A Output Source Current vs Temperature

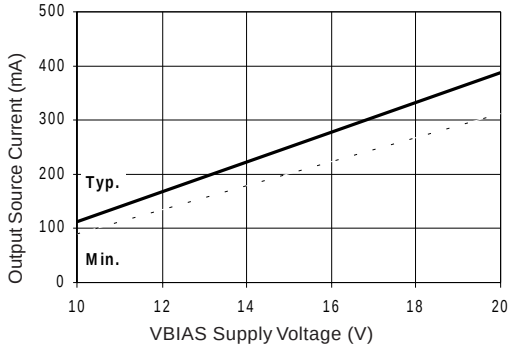


Figure 31B Output Source Current vs Voltage

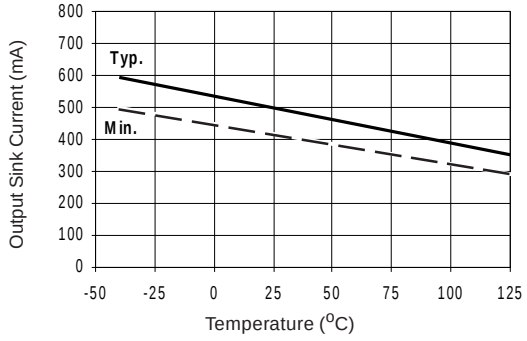


Figure 32A Output Sink Current vs Temperature

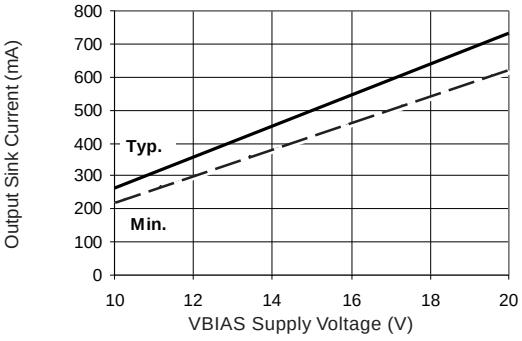
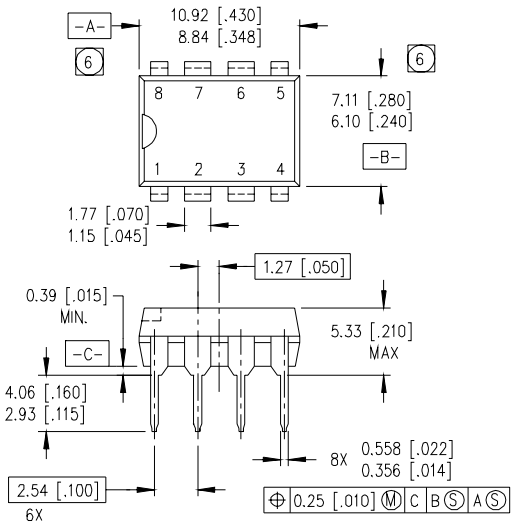
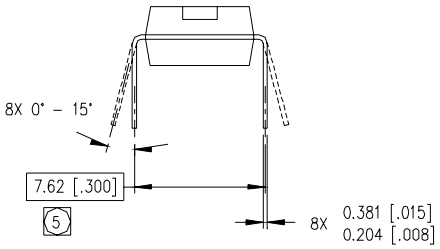


Figure 32B Output Sink Current vs Voltage

Case outlines

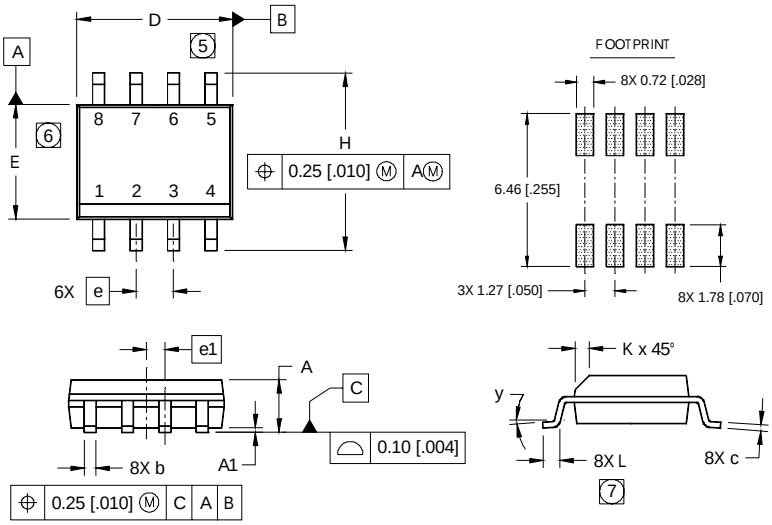


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8-Lead PDIP

01-6014
01-3003 01 (MS-001AB)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8-Lead SOIC

01-6027
01-0021 11 (MS-012AA)

5/15/2001

Data Sheet No. PD60019-M

International
IOR Rectifier

IR2130/IR2132 (J)(S)

3-PHASE BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent half-bridge drivers
- Matched propagation delay for all channels
- 2.5V logic compatible
- Outputs out of phase with inputs
- Cross-conduction prevention logic

Product Summary

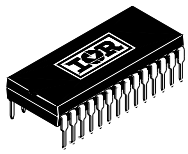
V_{OFFSET}	600V max.
I_O+/-	200 mA / 420 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	675 & 425 ns
Deadtime (typ.)	2.5 µs (IR2130) 0.8 µs (IR2132)

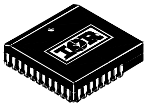
Description

The IR2130/IR2132(J)(S) is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 2.5V logic. A ground-referenced operational amplifier provides analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs is also derived from this resistor. An open drain $\overline{\text{FAULT}}$ signal indicates if an over-current or undervoltage shutdown has occurred. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use at high frequencies. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operate up to 600 volts.

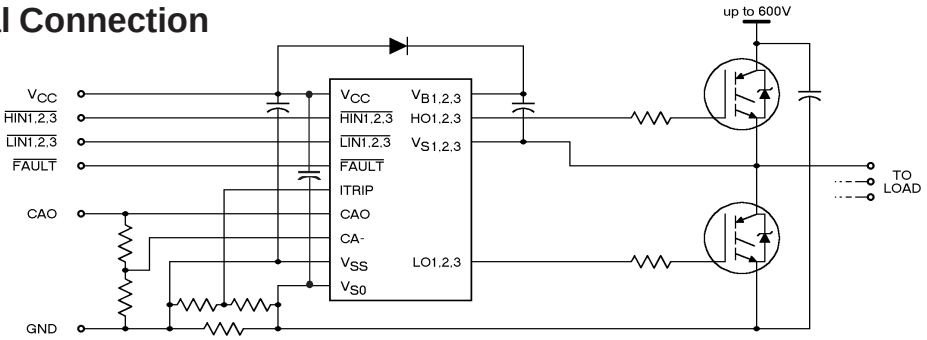
Packages


28-Lead SOIC


28-Lead PDIP


44-Lead PLCC w/o 12 Leads

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{S0}. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 50 through 53.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Voltage	-0.3	625	
$V_{S1,2,3}$	High Side Floating Offset Voltage	$V_{B1,2,3}$ - 25	$V_{B1,2,3}$ + 0.3	V
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Low Side and Logic Fixed Supply Voltage	-0.3	25	
V_{SS}	Logic Ground	V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low Side Output Voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage ($\overline{HIN1,2,3}$, $\overline{LIN1,2,3}$ & ITRIP)	V_{SS} - 0.3	V_{SS} + 15	
V_{FLT}	$\overline{FAULT}$ Output Voltage	V_{SS} - 0.3	V_{CC} + 0.3	
V_{CAO}	Operational Amplifier Output Voltage	V_{SS} - 0.3	V_{CC} + 0.3	
V_{CA-}	Operational Amplifier Inverting Input Voltage	V_{SS} - 0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$ (28 Lead DIP)	—	1.5	
	(28 Lead SOIC)	—	1.6	W
	(44 Lead PLCC)	—	2.0	
Rth_{JA}	Thermal Resistance, Junction to Ambient (28 Lead DIP)	—	83	
	(28 Lead SOIC)	—	78	°C/W
	(44 Lead PLCC)	—	63	
T_J	Junction Temperature	—	150	
T_S	Storage Temperature	-55	150	°C
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{S0}. The V_S offset rating is tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figure 54.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Voltage	$V_{S1,2,3}$ + 10	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	Note 1	600	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Low Side and Logic Fixed Supply Voltage	10	20	
V_{SS}	Logic Ground	-5	5	
$V_{LO1,2,3}$	Low Side Output Voltage	0	V_{CC}	
V_{IN}	Logic Input Voltage ($\overline{HIN1,2,3}$, $\overline{LIN1,2,3}$ & ITRIP)	V_{SS}	V_{SS} + 5	
V_{FLT}	$\overline{FAULT}$ Output Voltage	V_{SS}	V_{CC}	
V_{CAO}	Operational Amplifier Output Voltage	V_{SS}	V_{SS} + 5	
V_{CA-}	Operational Amplifier Inverting Input Voltage	V_{SS}	V_{SS} + 5	
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of (V_{S0} - 5V) to (V_{S0} + 600V). Logic state held for V_S of (V_{S0} - 5V) to (V_{S0} - V_{BS}). (Please refer to the Design Tip DT97-3 for more details).
Note 2: All input pins, CA- and CAO pins are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS}, C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are defined in Figures 3 through 5.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	11	500	675	850	ns	
t_{off}	Turn-Off Propagation Delay	12	300	425	550		V_{IN} = 0 & 5V
t_r	Turn-On Rise Time	13	—	80	125		$V_{S1,2,3}$ = 0 to 600V
t_f	Turn-Off Fall Time	14	—	35	55		
t_{itrip}	ITRIP to Output Shutdown Prop. Delay	15	400	660	920		V_{IN}, V_{ITRIP} = 0 & 5V
t_{bl}	ITRIP Blanking Time	16	—	—	400		V_{ITRIP} = 1V
t_{flt}	ITRIP to $\overline{FAULT}$ Indication Delay	16	335	590	845		V_{IN}, V_{ITRIP} = 0 & 5V
$t_{flt,in}$	Input Filter Time (All Six Inputs)	—	—	310	—		V_{IN} = 0 & 5V
t_{fltclr}	$\overline{LIN1,2,3}$ to $\overline{FAULT}$ Clear Time	17	6.0	9.0	12.0	µs	V_{IN}, V_{ITRIP} = 0 & 5V
DT	Deadtime (IR2130)	18	1.3	2.5	3.7		V_{IN} = 0 & 5V
	(IR2132)	18	0.4	0.8	1.2		
SR+	Operational Amplifier Slew Rate (+)	19	4.4	6.2	—	V/µs	
SR-	Operational Amplifier Slew Rate (-)	20	2.4	3.2	—		

NOTE: For high side PWM, HIN pulse width must be ≥ 1.5µsec

Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS} and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: $\overline{HIN1,2,3}$ & $\overline{LIN1,2,3}$. The V_O and I_O parameters are referenced to $V_{S0,1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

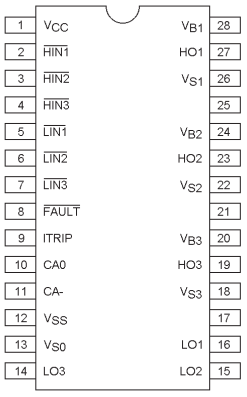
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “0” Input Voltage (OUT = LO)	21	2.2	—	—	V	
V_{IL}	Logic “1” Input Voltage (OUT = HI)	22	—	—	0.8		
$V_{IT,TH+}$	ITRIP Input Positive Going Threshold	23	400	490	580	mV	
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	24	—	—	100		V_{IN} = 0V, I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	25	—	—	100		V_{IN} = 5V, I_O = 0A
I_{LK}	Offset Supply Leakage Current	26	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} Supply Current	27	—	15	30		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	28	—	3.0	4.0	mA	V_{IN} = 0V or 5V
I_{IN+}	Logic “1” Input Bias Current (OUT = HI)	29	—	450	650	µA	V_{IN} = 0V
I_{IN-}	Logic “0” Input Bias Current (OUT = LO)	30	—	225	400		V_{IN} = 5V
I_{ITRIP+}	“High” ITRIP Bias Current	31	—	75	150		ITRIP = 5V
I_{ITRIP-}	“Low” ITRIP Bias Current	32	—	—	100	nA	ITRIP = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	33	7.5	8.35	9.2	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	34	7.1	7.95	8.8		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	35	8.3	9.0	9.7		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	36	8.0	8.7	9.4		
$R_{on,FLT}$	$\overline{FAULT}$ Low On-Resistance	37	—	55	75	Ω	

Static Electrical Characteristics -- Continued

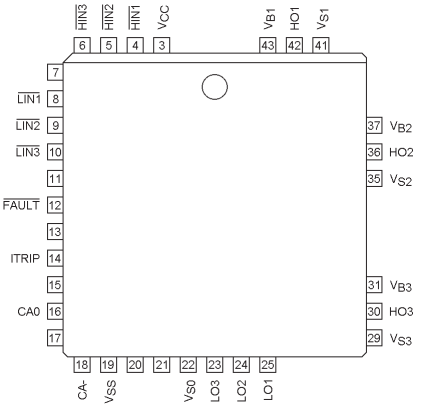
V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS} and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: $\overline{HIN1,2,3}$ & $\overline{LIN1,2,3}$. The V_O and I_O parameters are referenced to $V_{S0,1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
I_{O+}	Output High Short Circuit Pulsed Current	38	200	250	—	mA	V_O = 0V, V_{IN} = 0V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	39	420	500	—		V_O = 15V, V_{IN} = 5V PW ≤ 10 µs
V_{OS}	Operational Amplifer Input Offset Voltage	40	—	—	30	mV	V_{S0} = V_{CA-} = 0.2V
I_{CA-}	CA- Input Bais Current	41	—	—	4.0	nA	V_{CA-} = 2.5V
CMRR	Op. Amp. Common Mode Rejection Ratio	42	60	80	—	dB	V_{S0}=V_{CA-}=0.1V & 5V
PSRR	Op. Amp. Power Supply Rejection Ratio	43	55	75	—		V_{S0} = V_{CA-} = 0.2V V_{CC} = 10V & 20V
$V_{OH,AMP}$	Op. Amp. High Level Output Voltage	44	5.0	5.2	5.4	V	V_{CA-} = 0V, V_{S0} = 1V
$V_{OL,AMP}$	Op. Amp. Low Level Output Voltage	45	—	—	20	mV	V_{CA-} = 1V, V_{S0} = 0V
$I_{SRC,AMP}$	Op. Amp. Output Source Current	46	2.3	4.0	—	mA	V_{CA-} = 0V, V_{S0} = 1V V_{CAO} = 4V
$I_{SRC,AMP}$	Op. Amp. Output Sink Current	47	1.0	2.1	—		V_{CA-} = 1V, V_{S0} = 0V V_{CAO} = 2V
$I_{O+,AMP}$	Operational Amplifier Output High Short Circuit Current	48	—	4.5	6.5		V_{CA-} = 0V, V_{S0} = 5V V_{CAO} = 0V
$I_{O-,AMP}$	Operational Amplifier Output Low Short Circuit Current	49	—	3.2	5.2		V_{CA-} = 5V, V_{S0} = 0V V_{CAO} = 5V

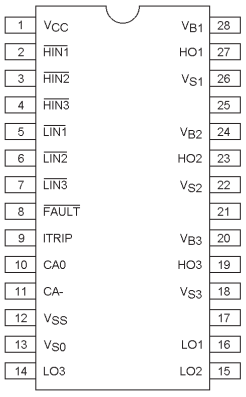
Lead Assignments



28 Lead PDIP



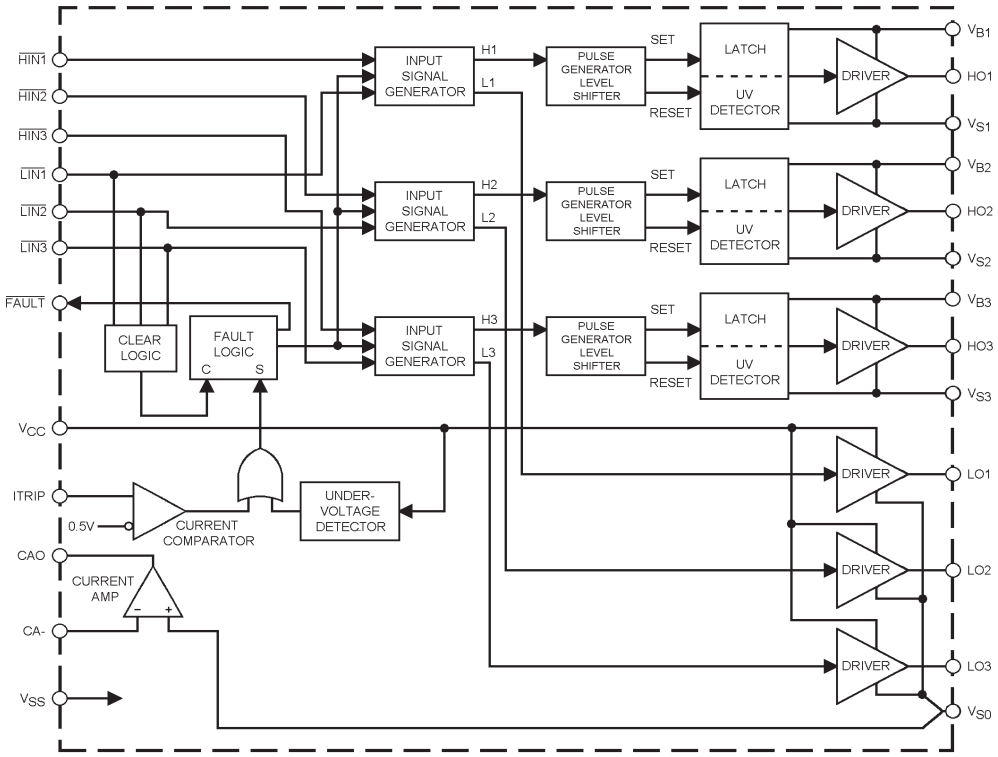
44 Lead PLCC w/o 12 Leads



28 Lead SOIC (Wide Body)

IR2130 / IR2132	IR2130J / IR2132J	IR2130S / IR2132S
Part Number		

Functional Block Diagram



Lead Definitions

Symbol	Description
$\overline{HIN1,2,3}$	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase
$\overline{LIN1,2,3}$	Logic inputs for low side gate driver output (LO1,2,3), out of phase
$\overline{FAULT}$	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic
V_{CC}	Low side and logic fixed supply
ITRIP	Input for over-current shutdown
CAO	Output of current amplifier
CA-	Negative input of current amplifier
V_{SS}	Logic ground
$V_{B1,2,3}$	High side floating supplies
HO1,2,3	High side gate drive outputs
$V_{S1,2,3}$	High side floating supply returns
LO1,2,3	Low side gate drive outputs
V_{S0}	Low side return and positive input of current amplifier

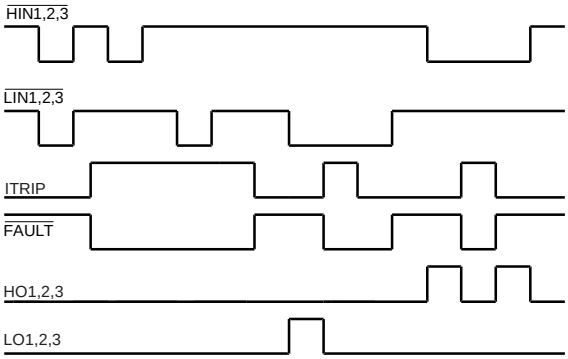


Figure 1. Input/Output Timing Diagram

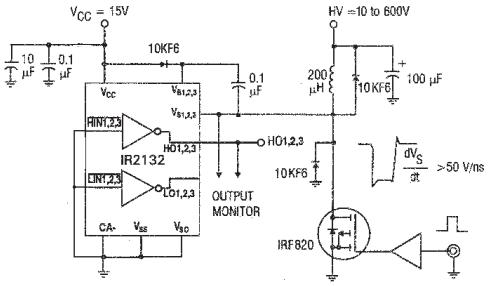


Figure 2. Floating Supply Voltage Transient Test Circuit

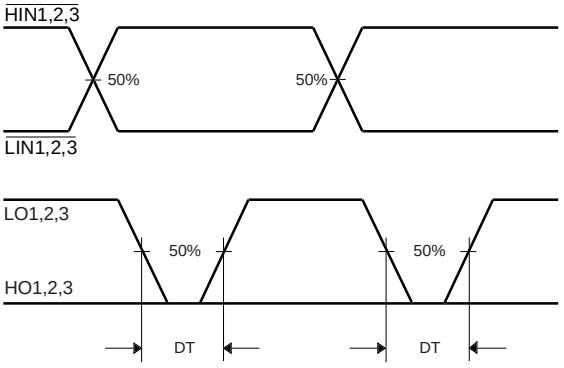


Figure 3. Deadtime Waveform Definitions

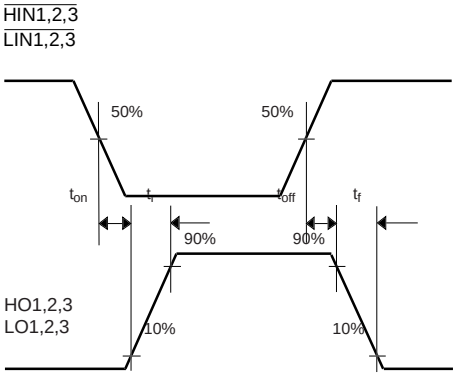


Figure 4. Input/Output Switching Time Waveform Definitions

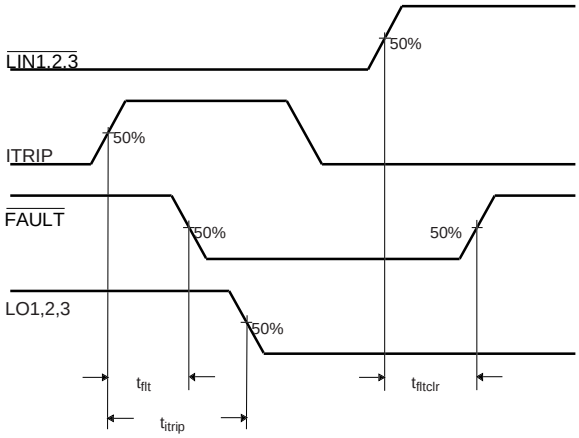


Figure 5. Overcurrent Shutdown Switching Time Waveform Definitions

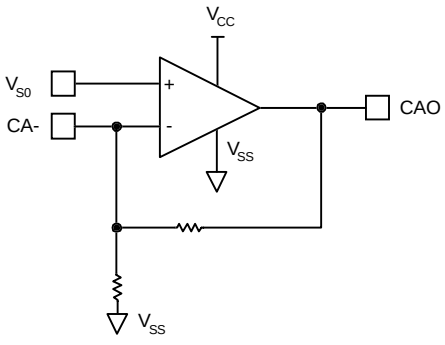


Figure 6. Diagnostic Feedback Operational Amplifier Circuit

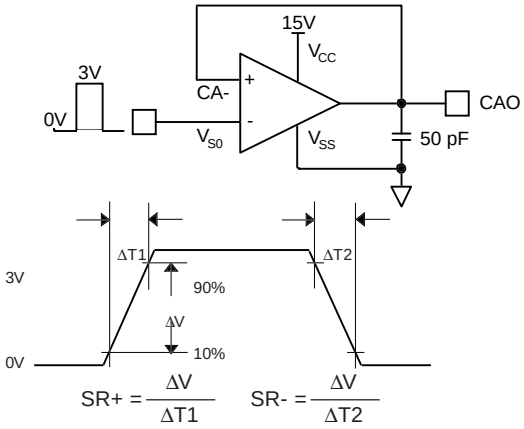


Figure 7. Operational Amplifier Slew Rate Measurement

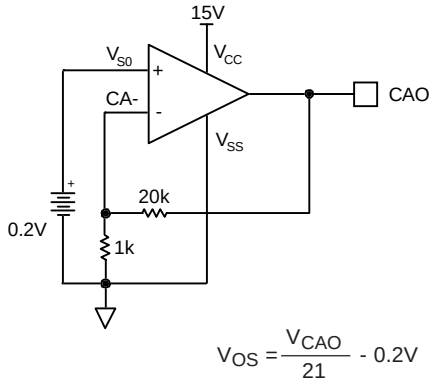
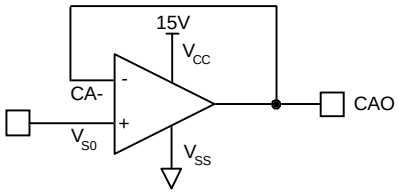


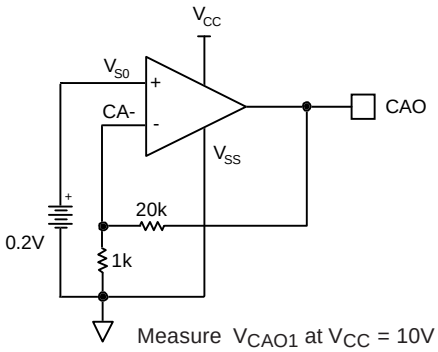
Figure 8. Operational Amplifier Input Offset Voltage Measurement



Measure V_{CAO1} at V_{S0} = 0.1V
V_{CAO2} at V_{S0} = 5V

$$CMRR = -20*LOG \left| \frac{(V_{CAO1}-0.1V) - (V_{CAO2}-5V)}{4.9V} \right| (dB)$$

Figure 9. Operational Amplifier Common Mode Rejection Ratio Measurements



Measure V_{CAO1} at V_{CC} = 10V
V_{CAO2} at V_{CC} = 20V

$$PSRR = -20*LOG \left| \frac{V_{CAO1} - V_{CAO2}}{(10V)\ (21)} \right|$$

Figure 10. Operational Amplifier Power Supply Rejection Ratio Measurements

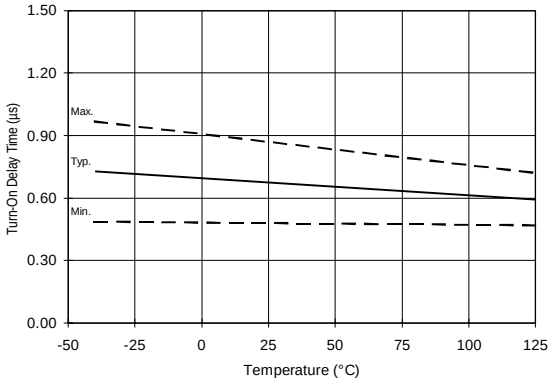


Figure 11A. Turn-On Time vs. Temperature

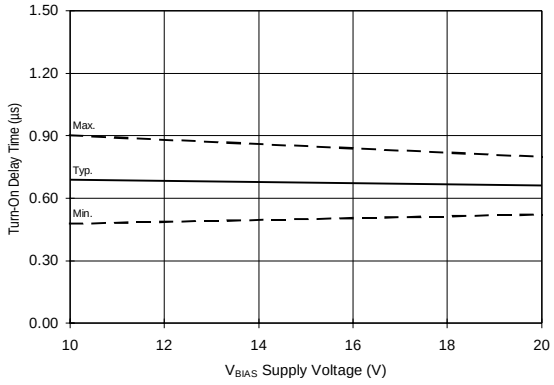


Figure 11B. Turn-On Time vs. Supply Voltage

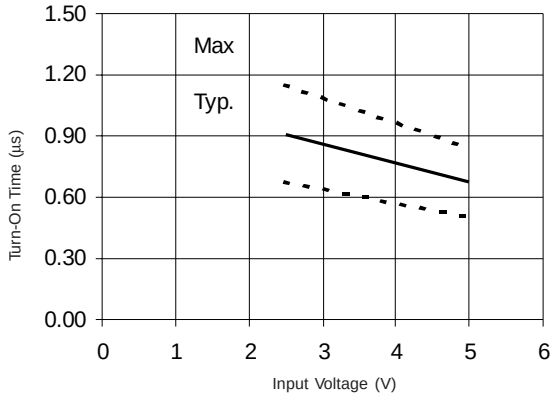


Figure 11C. Turn-On Time vs. Voltage

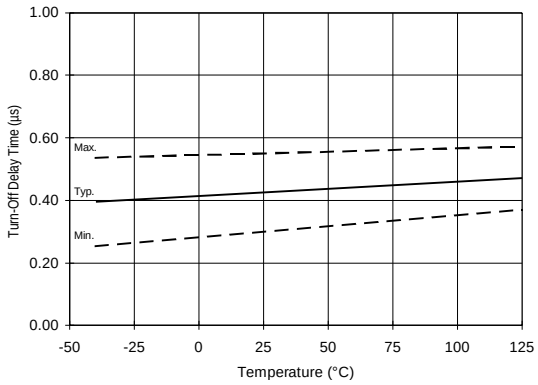


Figure 12A. Turn-Off Time vs. Temperature

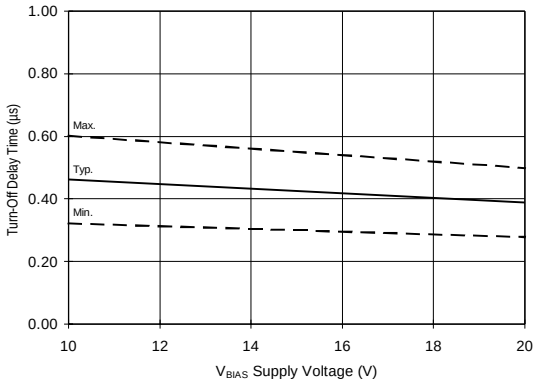


Figure 12B. Turn-Off Time vs. Supply Voltage

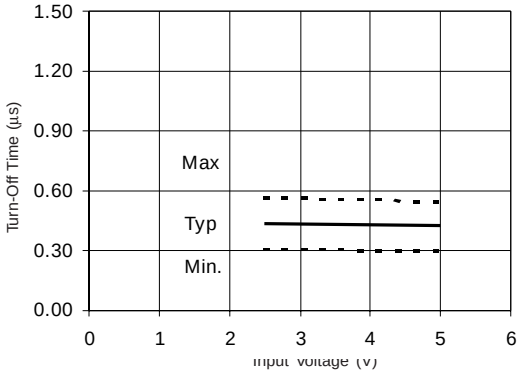


Figure 12C. Turn-Off Time vs. Input Voltage

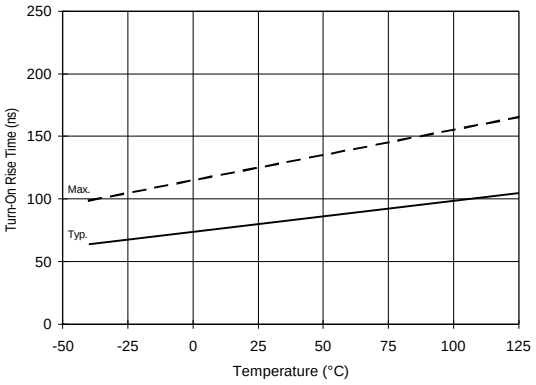


Figure 13A. Turn-On Rise Time vs. Temperature

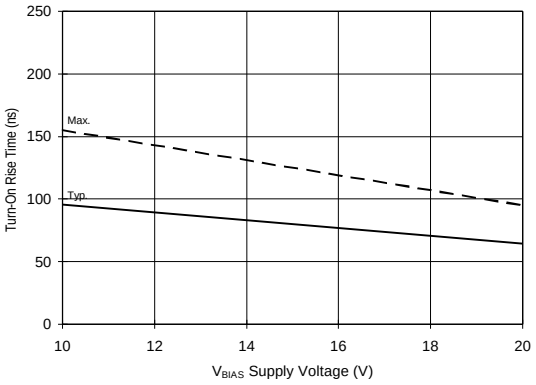


Figure 13B. Turn-On Rise Time vs. Voltage

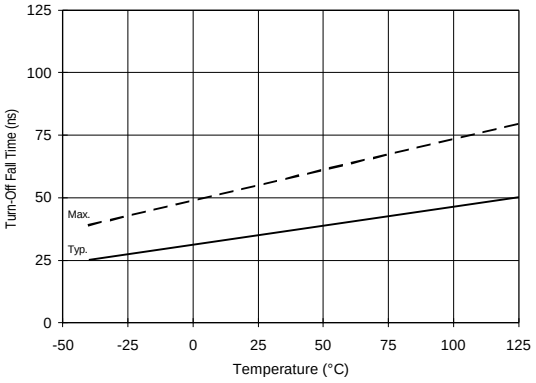


Figure 14A. Turn-Off Fall Time vs. Temperature

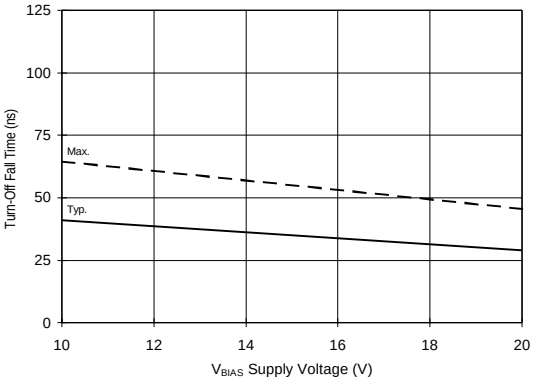


Figure 14B. Turn-Off Fall Time vs. Voltage

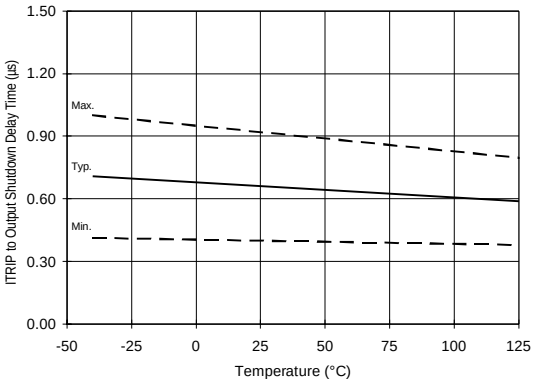


Figure 15A. ITRIP to Output Shutdown Time vs. Temperature

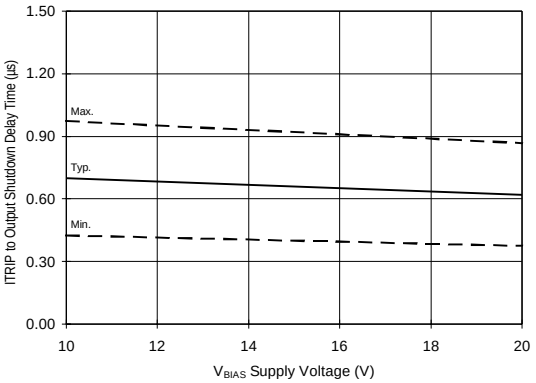


Figure 15B. ITRIP to Output Shutdown Time vs. Voltage

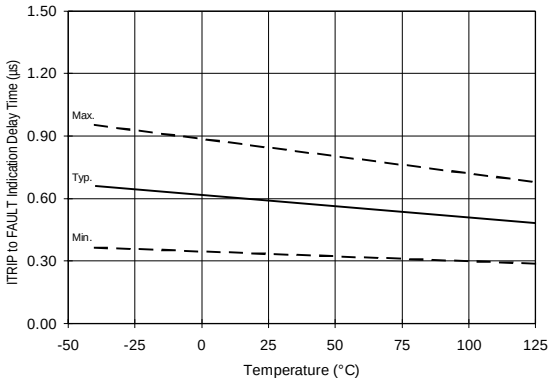


Figure 16A. ITRIP to $\overline{\text{FAULT}}$ Indication Time vs. Temperature

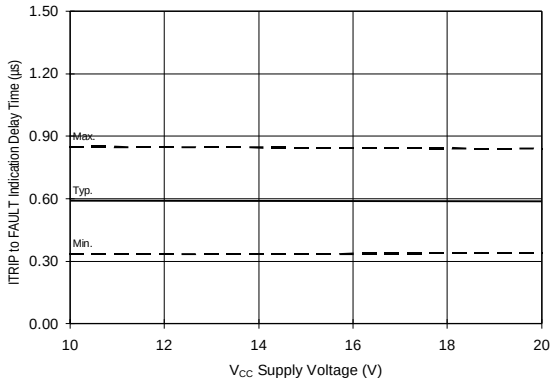


Figure 16B. ITRIP to $\overline{\text{FAULT}}$ Indication Time vs. Voltage

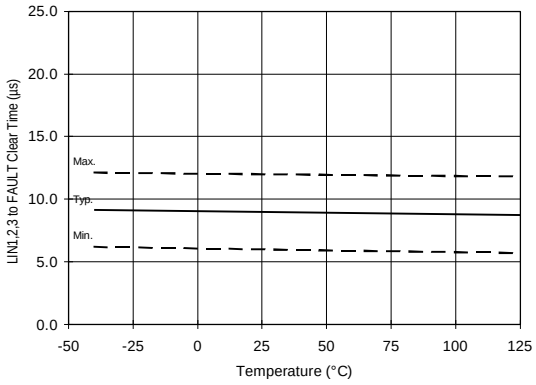


Figure 17A. $\overline{\text{LIN1,2,3}}$ to $\overline{\text{FAULT}}$ Clear Time vs. Temperature

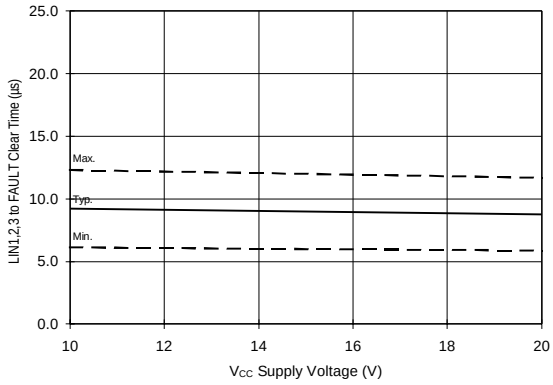


Figure 17B. $\overline{\text{LIN1,2,3}}$ to $\overline{\text{FAULT}}$ Clear Time vs. Voltage

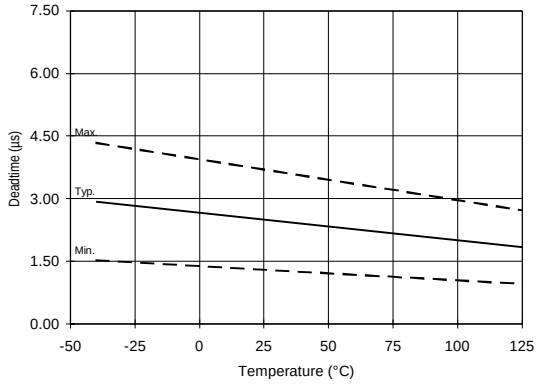


Figure 18A. Deadtime vs. Temperature (IR2130)

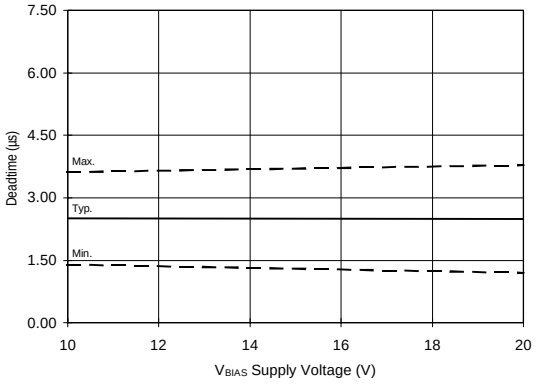


Figure 18B. Deadtime vs. Voltage (IR2130)

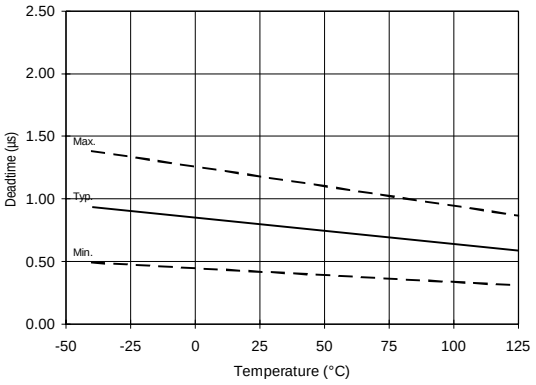


Figure 18C. Deadtime vs. Temperature (IR2132)

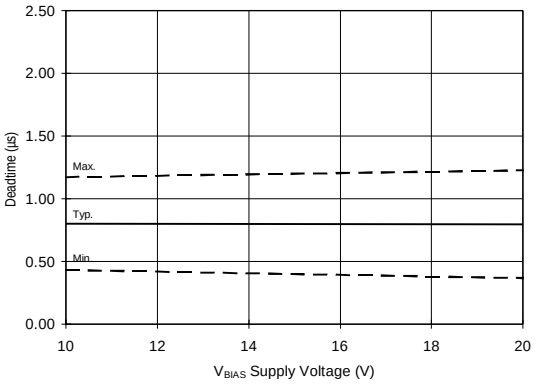


Figure 18D. Deadtime vs. Voltage (IR2132)

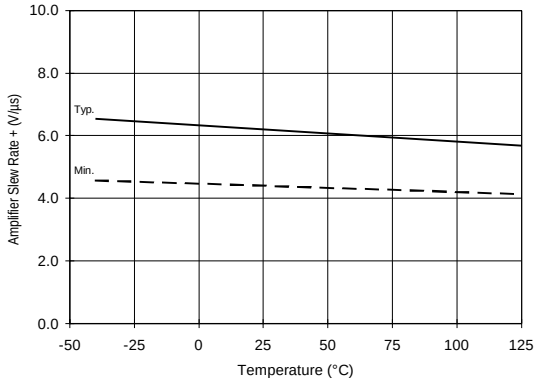


Figure 19A. Amplifier Slew Rate (+) vs. Temperature

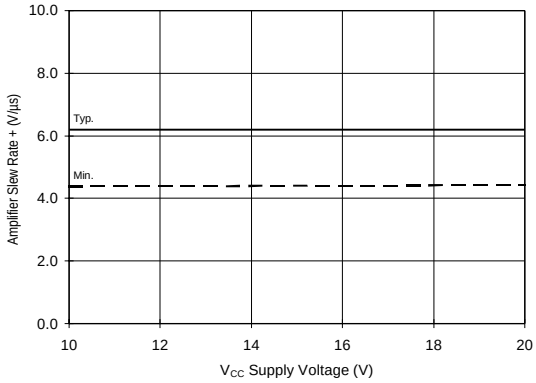


Figure 19B. Amplifier Slew Rate (+) vs. Voltage

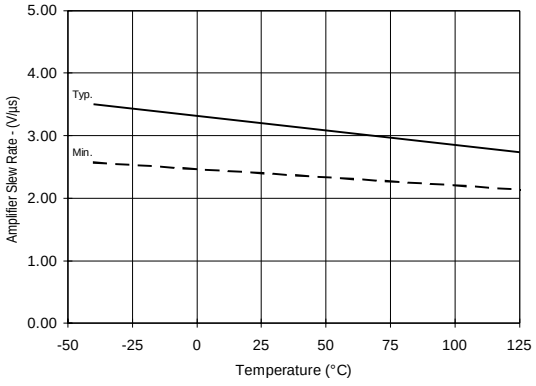


Figure 20A. Amplifier Slew Rate (-) vs. Temperature

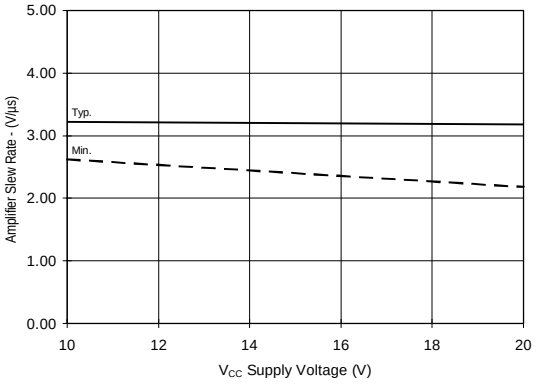


Figure 20B. Amplifier Slew Rate (-) vs. Voltage

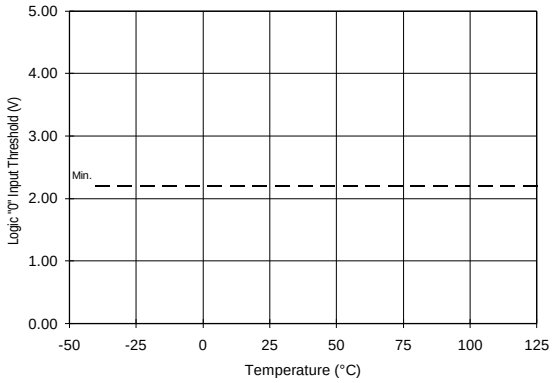


Figure 21A. Logic "0" Input Threshold vs. Temperature

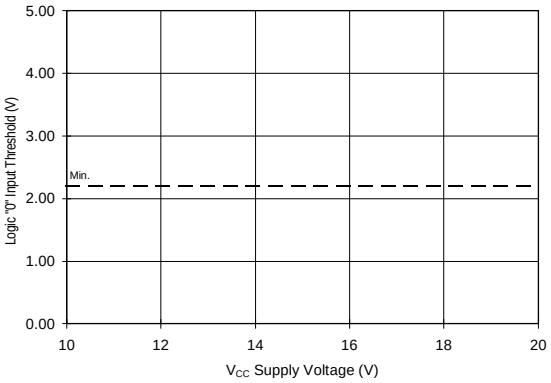


Figure 20B. Logic "0" Input Threshold vs. Voltage

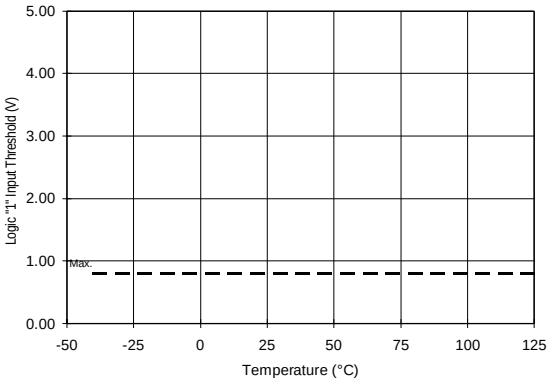


Figure 22A. Logic "1" Input Threshold vs. Temperature

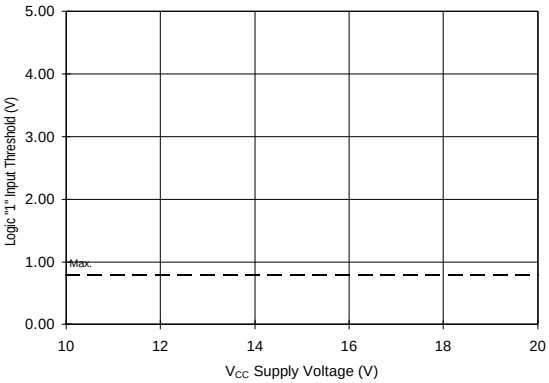


Figure 22B. Logic "1" Input Threshold vs. Voltage

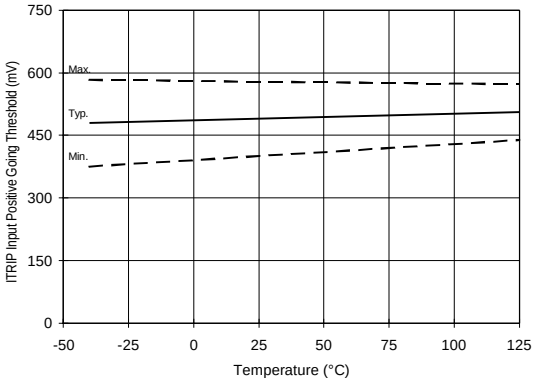


Figure 23A. ITRIP Input Positive Going Threshold vs. Temperature

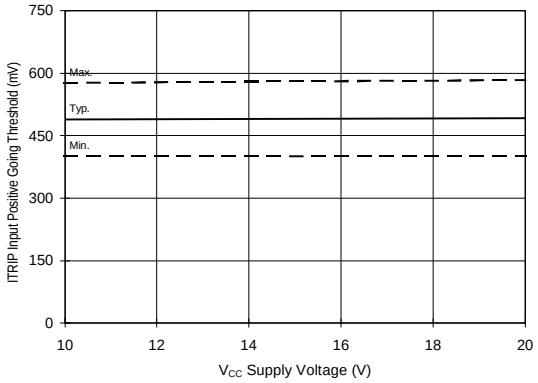


Figure 23B. ITRIP Input Positive Going Threshold vs. Voltage

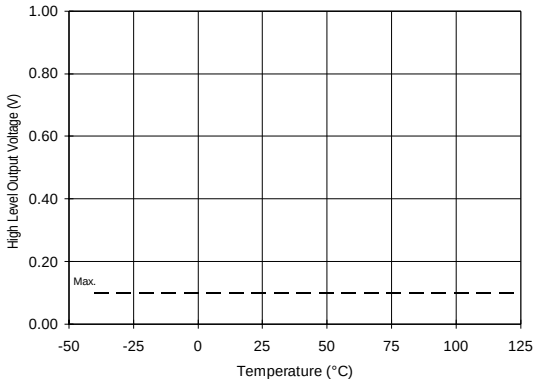


Figure 24A. High Level Output vs. Temperature

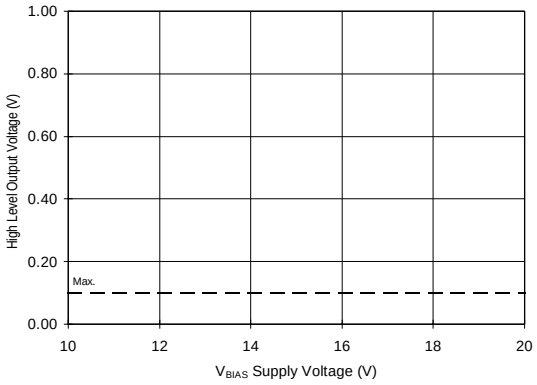


Figure 24B. High Level Output vs. Voltage

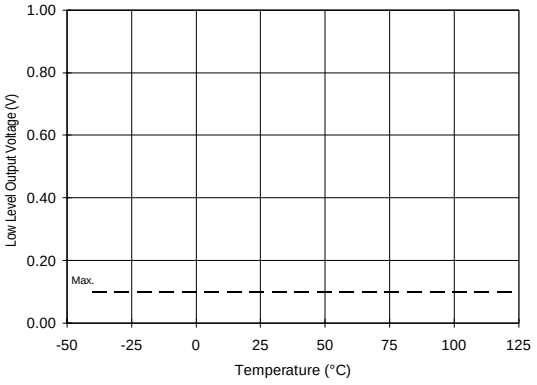


Figure 25A. Low Level Output vs. Temperature

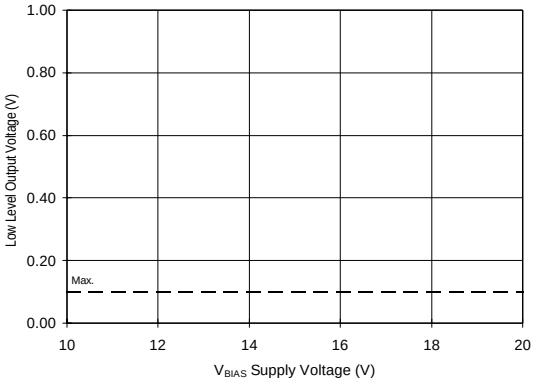


Figure 25B. Low Level Output vs. Voltage

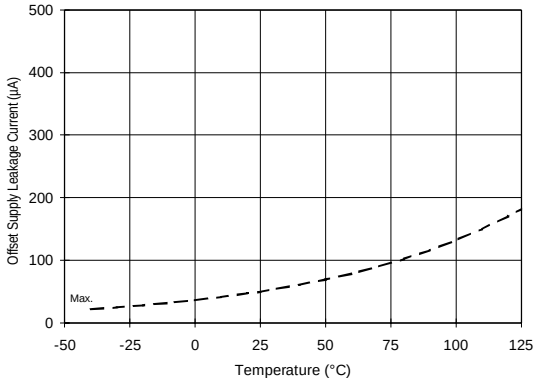


Figure 26A. Offset Supply Leakage Current vs. Temperature

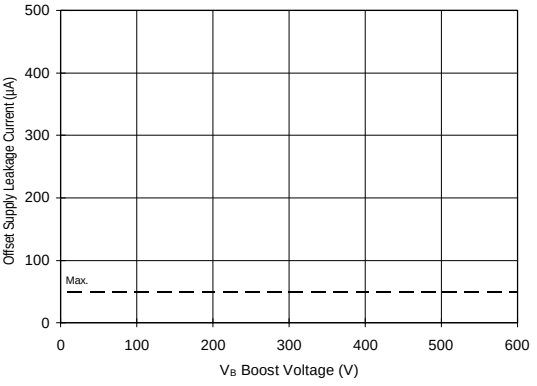


Figure 26B. Offset Supply Leakage Current vs. Voltage

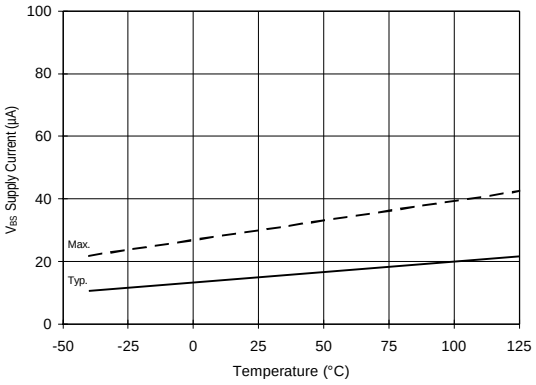


Figure 27A. V_{BS} Supply Current vs. Temperature

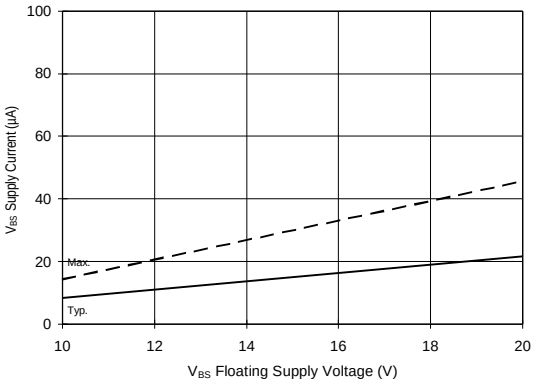


Figure 27B. V_{BS} Supply Current vs. Voltage

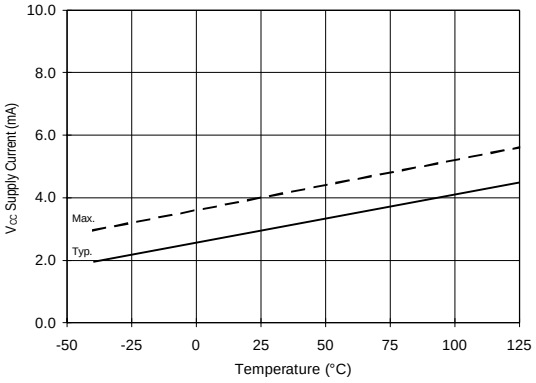


Figure 28A. V_{CC} Supply Current vs. Temperature

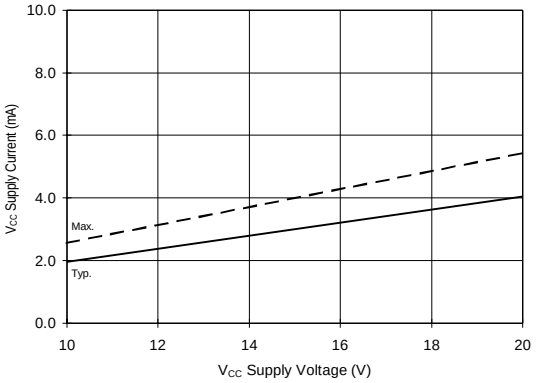


Figure 28B. V_{CC} Supply Current vs. Voltage

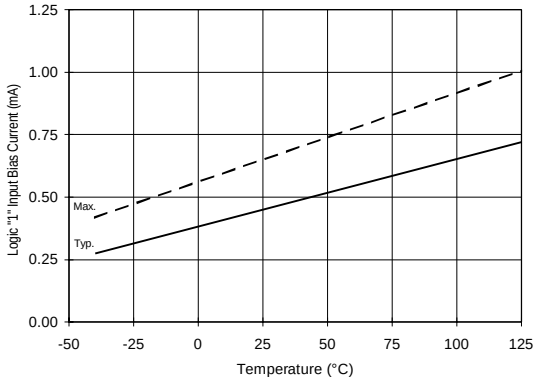


Figure 29A. Logic "1" Input Current vs. Temperature

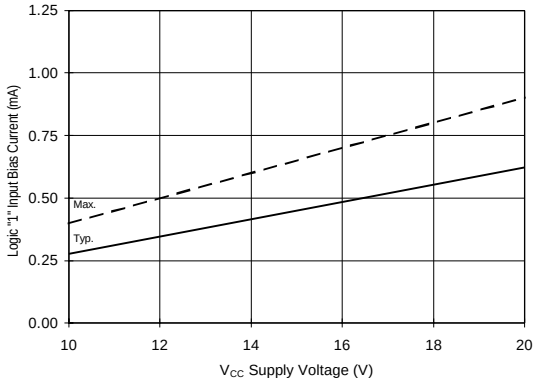


Figure 29A. Logic "1" Input Current vs. Voltage

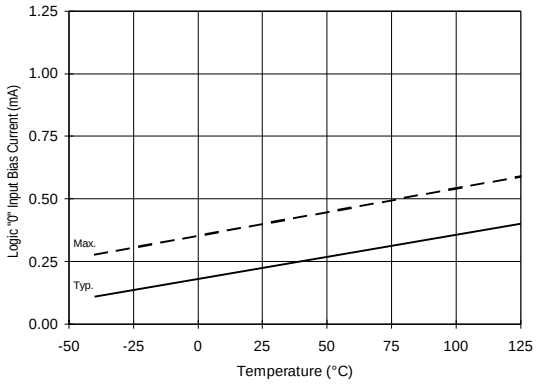


Figure 30A. Logic "0" Input Current vs. Temperature

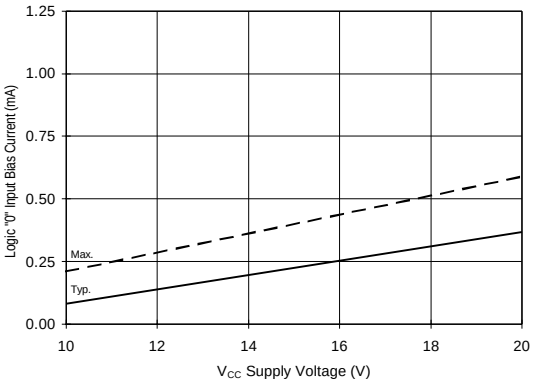


Figure 30B. Logic "0" Input Current vs. Voltage

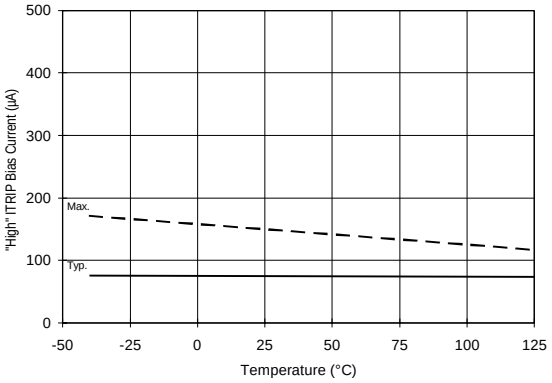


Figure 31A. "High" ITRIP Current vs. Temperature

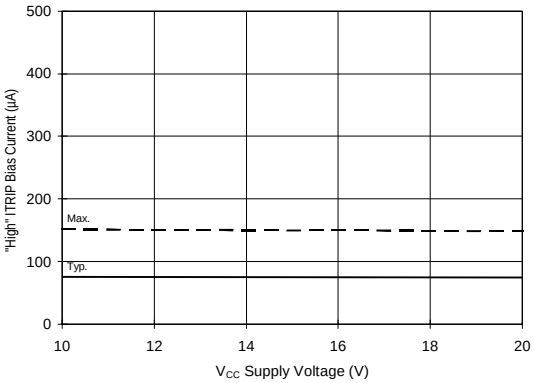


Figure 31B. "High" ITRIP Current vs. Voltage

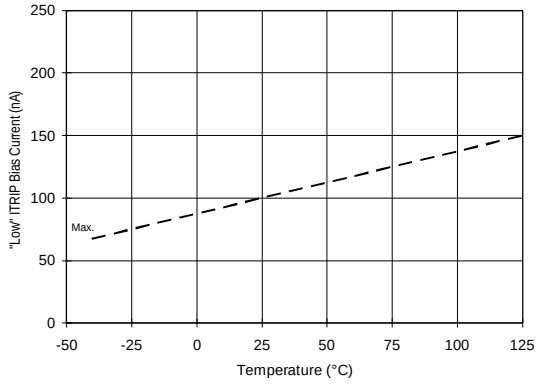


Figure 32A. "Low" ITRIP Current vs. Temperature

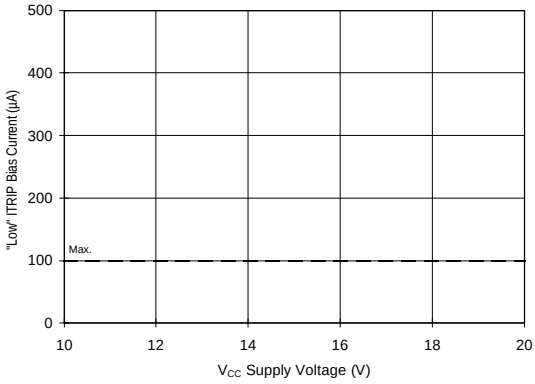


Figure 32B. "Low" ITRIP Current vs. Voltage

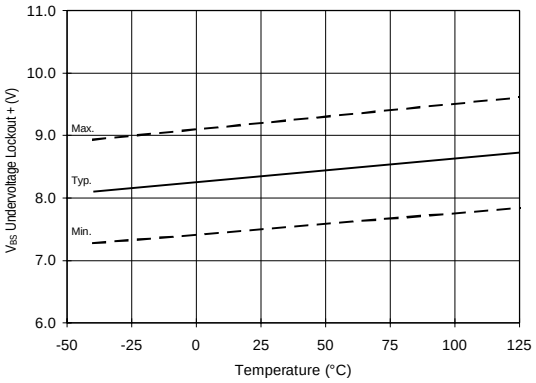


Figure 33. V_{BS} Undervoltage (+) vs. Temperature

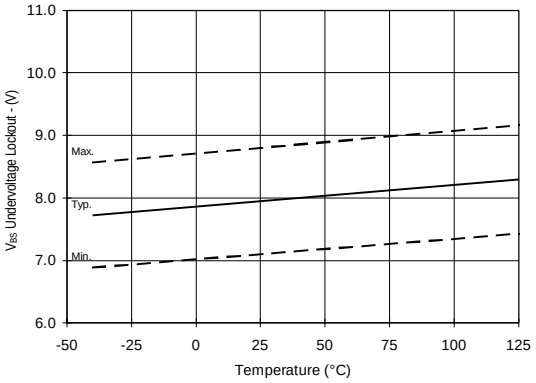


Figure 34. V_{BS} Undervoltage (-) vs. Temperature

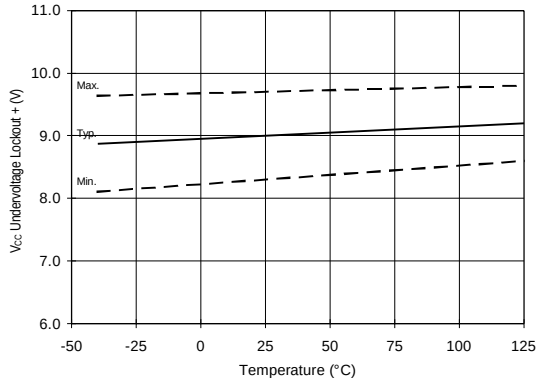


Figure 35. V_{CC} Undervoltage (+) vs. Temperature

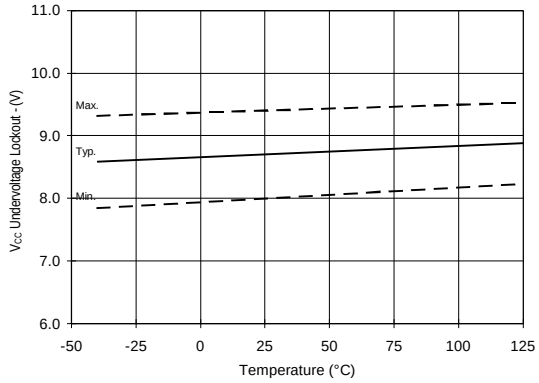


Figure 36. V_{CC} Undervoltage (-) vs. Temperature

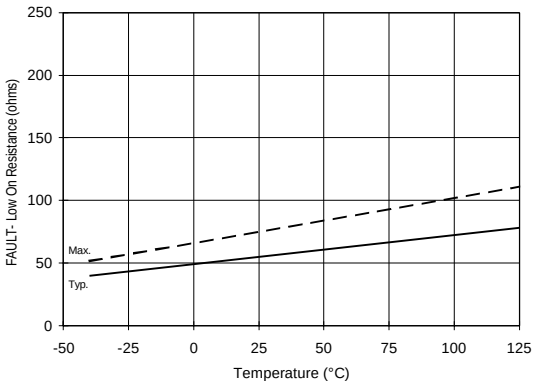


Figure 37A. $\overline{\text{FAULT}}$ Low On Resistance vs. Temperature

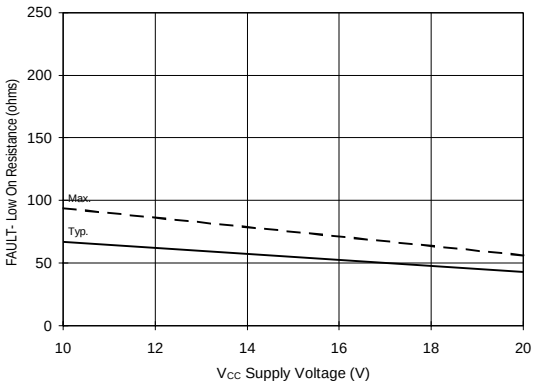


Figure 37B. $\overline{\text{FAULT}}$ Low On Resistance vs. Voltage

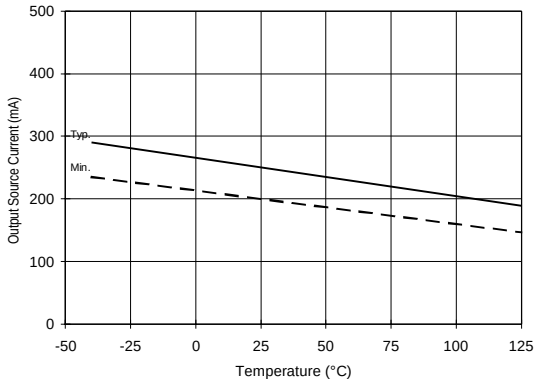


Figure 38A. Output Source Current vs. Temperature

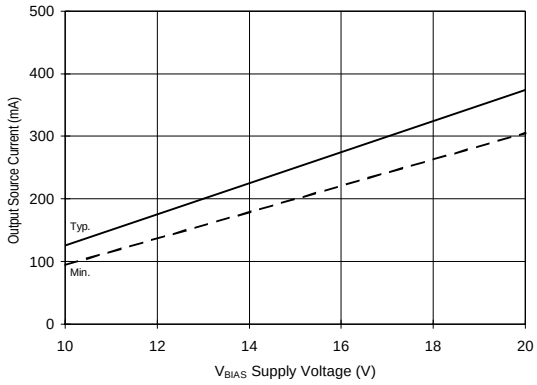


Figure 38B. Output Source Current vs. Voltage

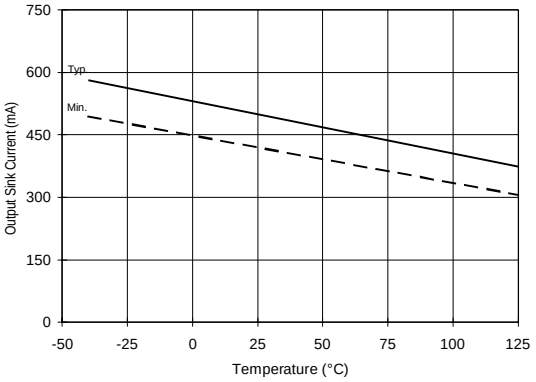


Figure 39A. Output Sink Current vs. Temperature

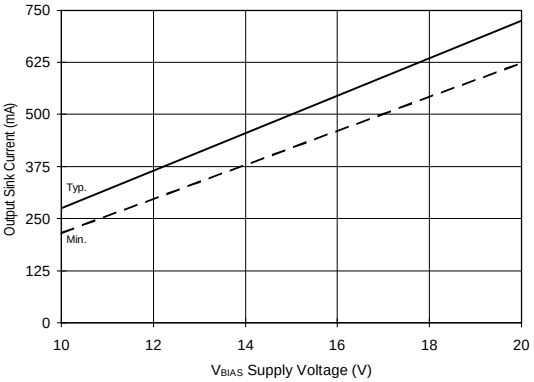


Figure 39B. Output Sink Current vs. Voltage

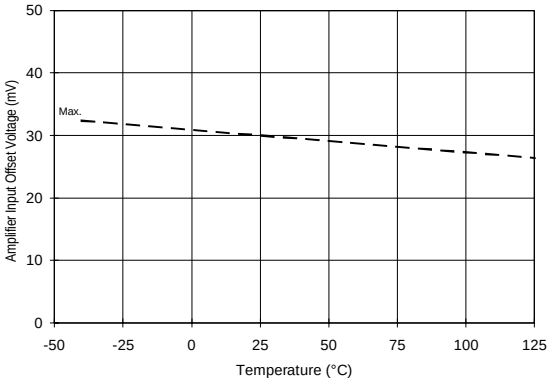


Figure 40A. Amplifier Input Offset vs. Temperature

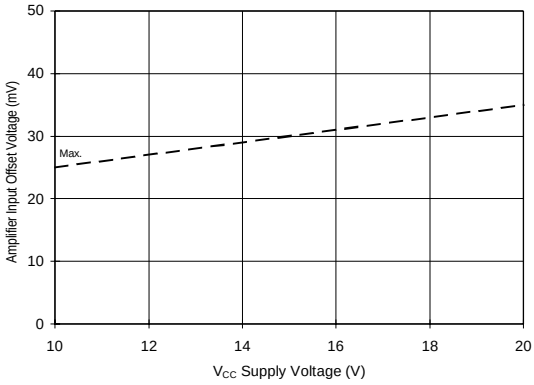


Figure 40B. Amplifier Input Offset vs. Voltage

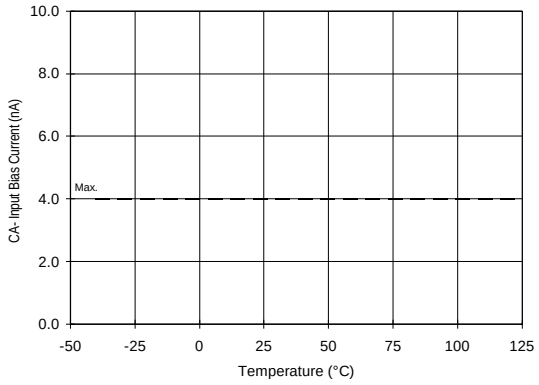


Figure 41A. CA- Input Current vs. Temperature

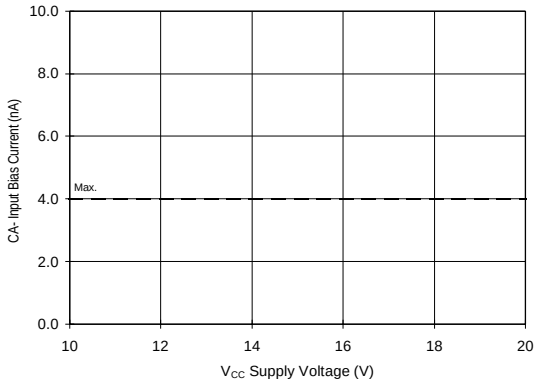


Figure 41B. CA- Input Current vs. Voltage

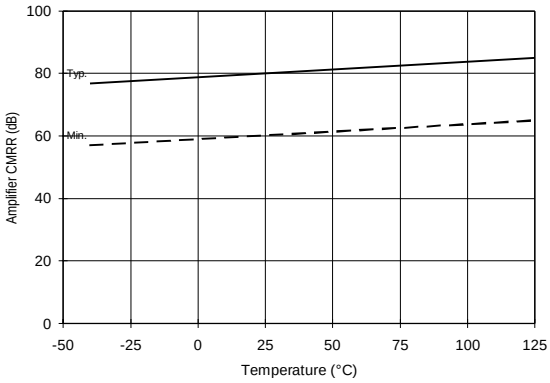


Figure 42A. Amplifier CMRR vs. Temperature

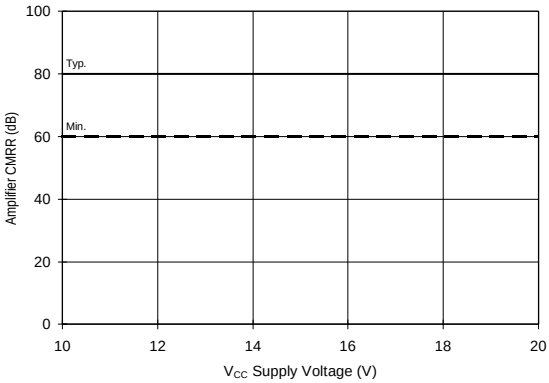


Figure 42B. Amplifier CMRR vs. Voltage

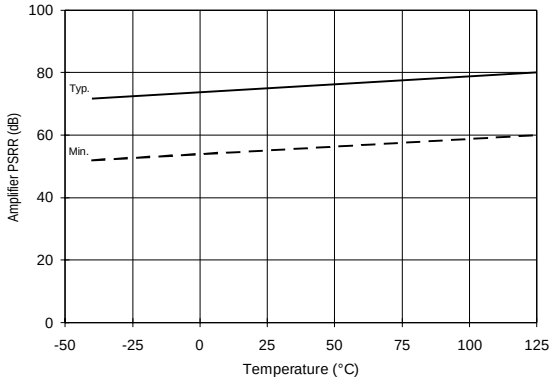


Figure 43A. Amplifier PSRR vs. Temperature

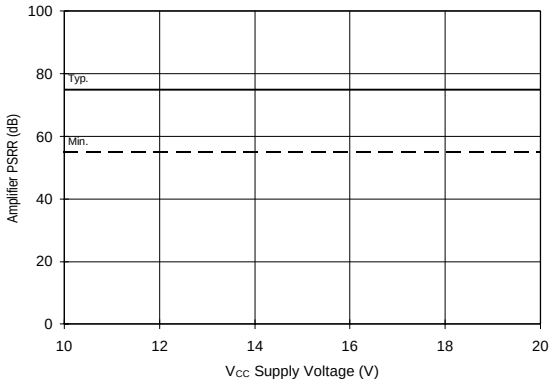


Figure 43B. Amplifier PSRR vs. Voltage

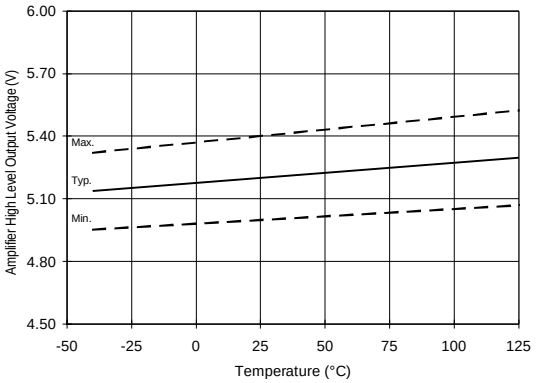


Figure 44A. Amplifier High Level Output vs. Temperature

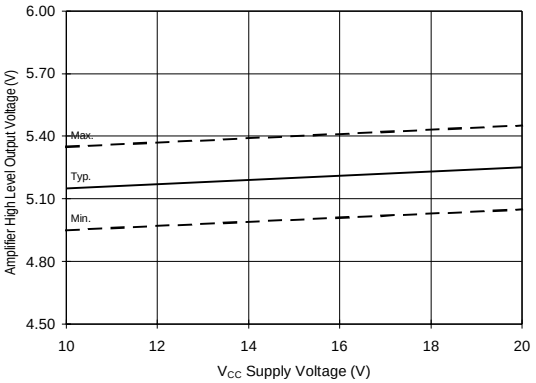


Figure 44B. Amplifier High Level Output vs. Voltage

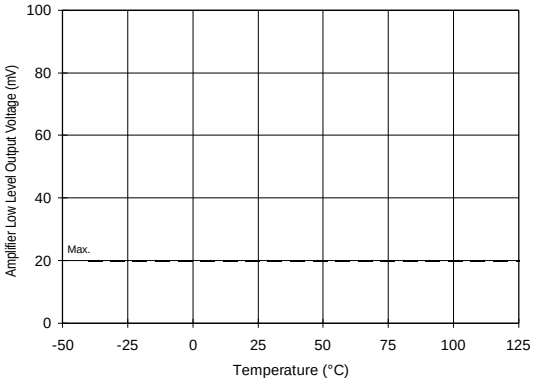


Figure 45A. Amplifier Low Level Output vs. Temperature

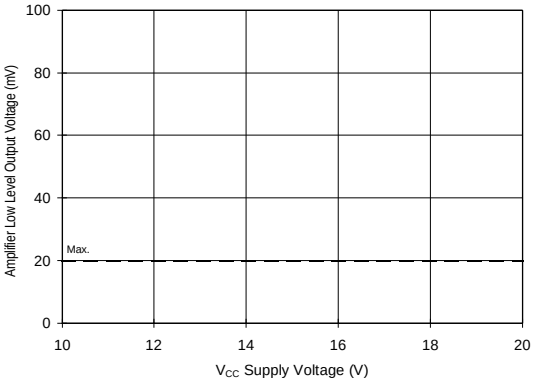


Figure 45B. Amplifier Low Level Output vs. Voltage

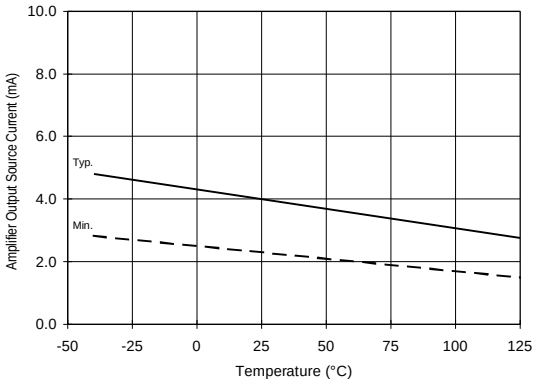


Figure 46A. Amplifier Output Source Current vs. Temperature

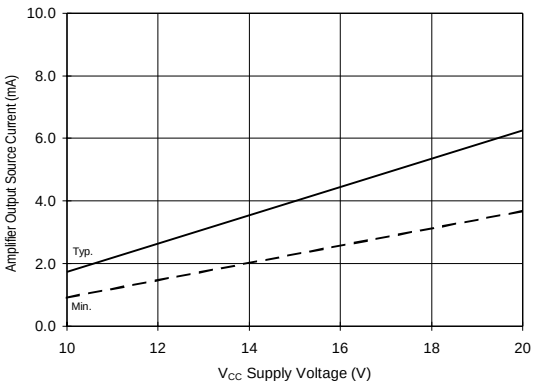


Figure 46B. Amplifier Output Source Current vs. Voltage

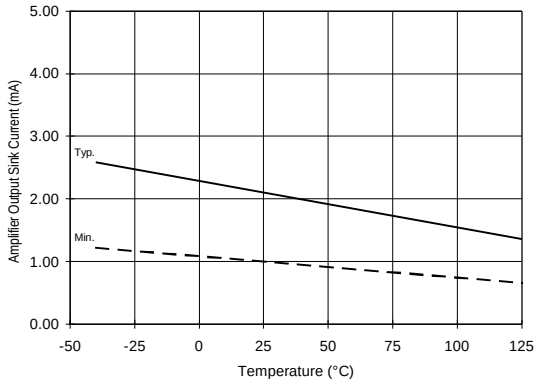


Figure 47A. Amplifier Output Sink Current vs. Temperature

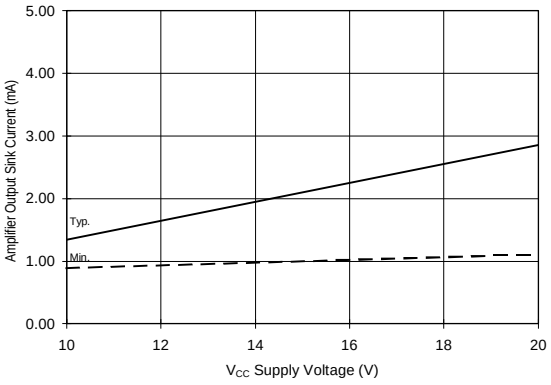


Figure 47B. Amplifier Output Sink Current vs. Voltage

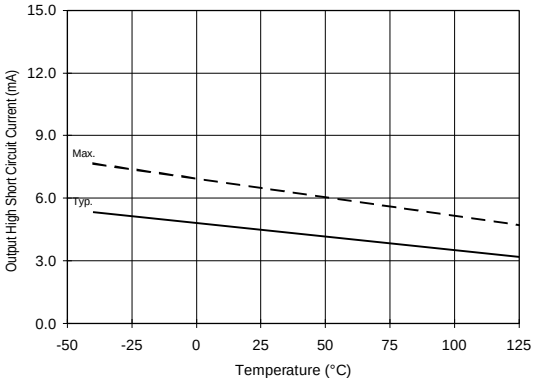


Figure 48A. Amplifier Output High Short Circuit Current vs. Temperature

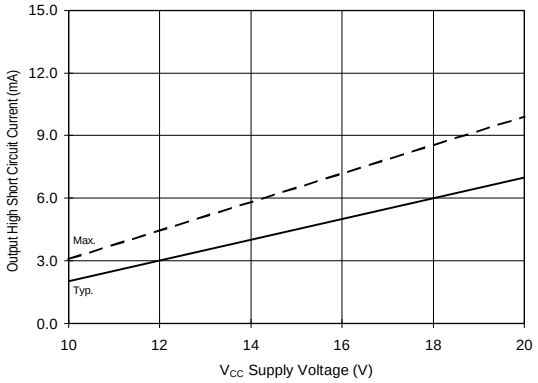


Figure 48B. Amplifier Output High Short Circuit Current vs. Voltage

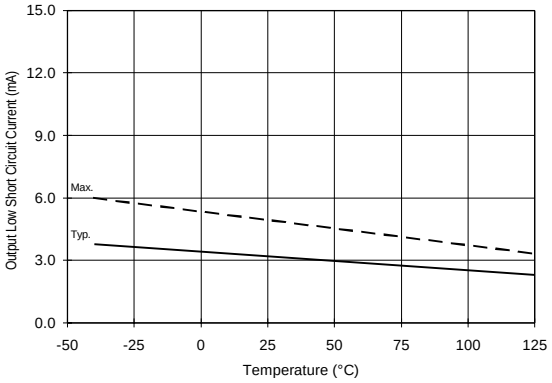


Figure 49A. Amplifier Output Low Short Circuit Current vs. Temperature

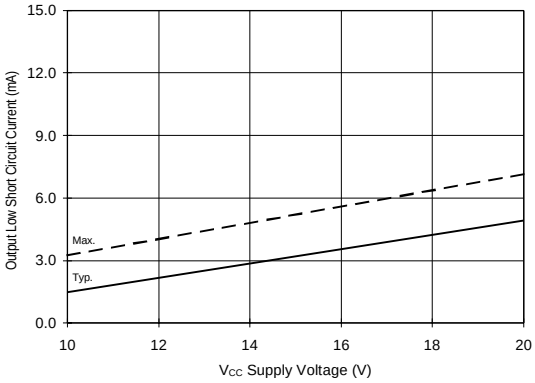


Figure 49B. Amplifier Output Low Short Circuit Current vs. Voltage

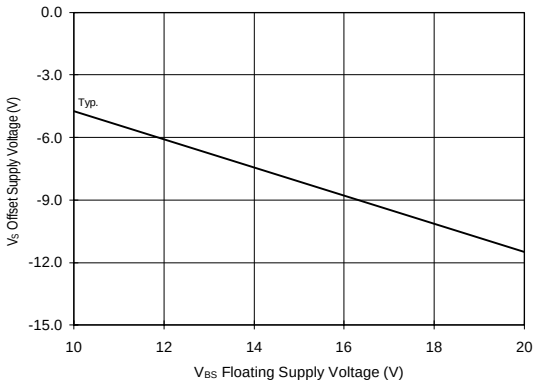


Figure 50. Maximum VS Negative Offset vs. V_{BS} Supply Voltage

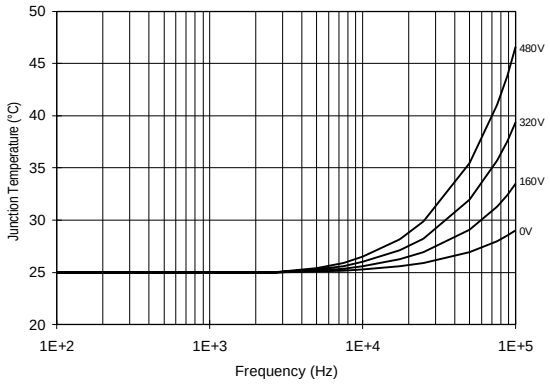


Figure 51. IR2130/IR2132 T_J vs. Frequency (IRF820)
R_{GATE} = 33Ω, V_{CC} = 15V

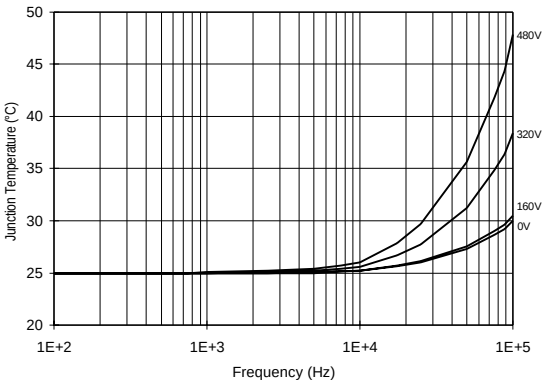


Figure 52. IR2130/IR2132 T_J vs. Frequency (IRF830)
R_{GATE} = 20Ω, V_{CC} = 15V

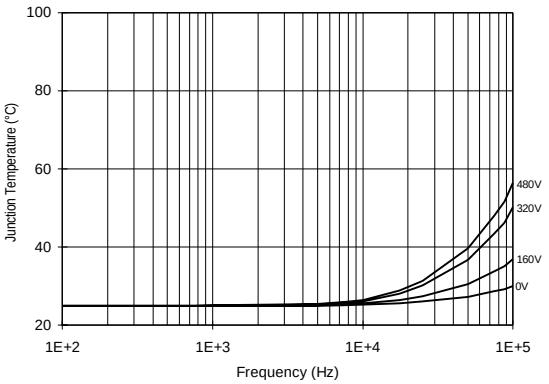


Figure 53. IR2130/IR2132 T_J vs. Frequency (IRF840)
R_{GATE} = 15Ω, V_{CC} = 15V

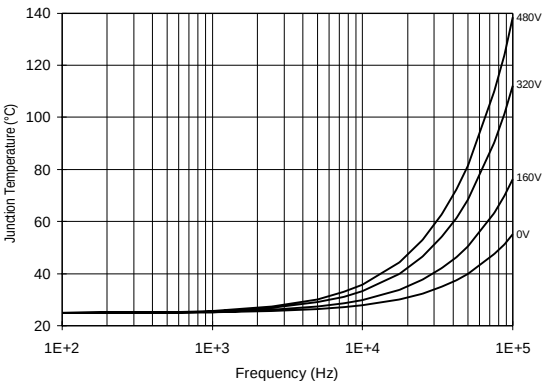


Figure 54. IR2130/IR2132 T_J vs. Frequency (IRF450)
R_{GATE} = 10Ω, V_{CC} = 15V

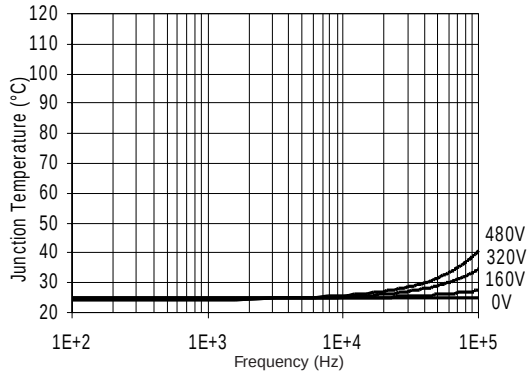


Figure 55. IR2130J/IR2132J
T_J vs. Frequency (IRGPC20KD2)
R_{GATE} = 33Ω, V_{CC} = 15V

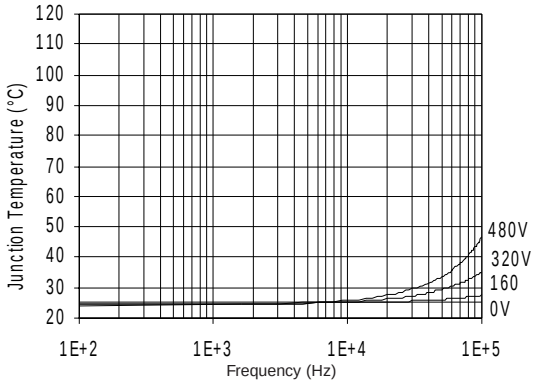


Figure 56. IR2130J/IR2132J
T_J vs. Frequency (IRGPC30KD2)
R_{GATE} = 20Ω, V_{CC} = 15V

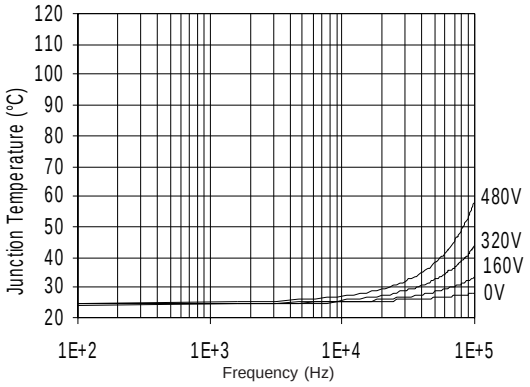


Figure 57. IR2130J/IR2132J
T_J vs. Frequency (IRGPC40KD2)
R_{GATE} = 15Ω, V_{CC} = 15V

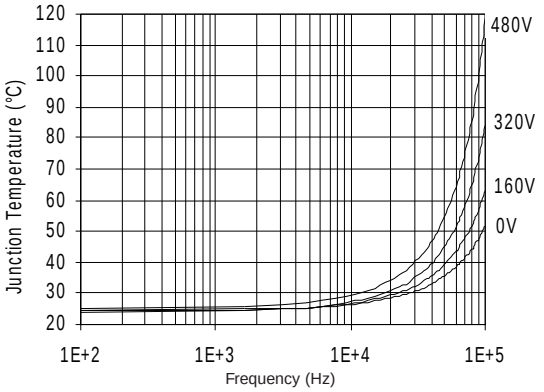
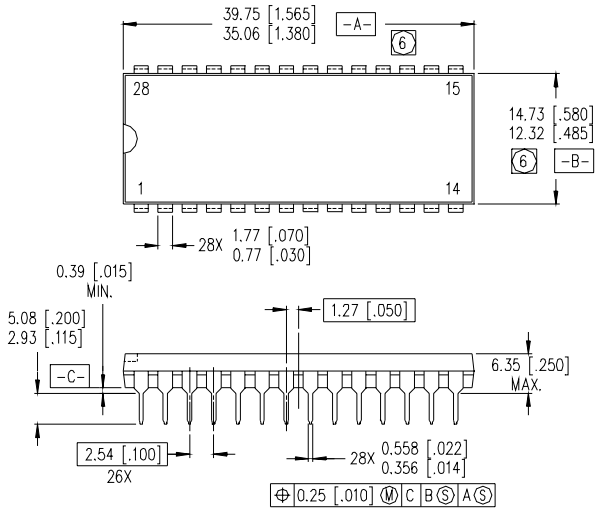
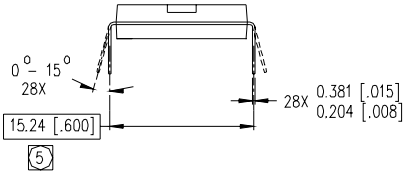


Figure 58. IR2130J/IR2132J
T_J vs. Frequency (IRGPC50KD2)
R_{GATE} = 10Ω, V_{CC} = 15V

Case outlines

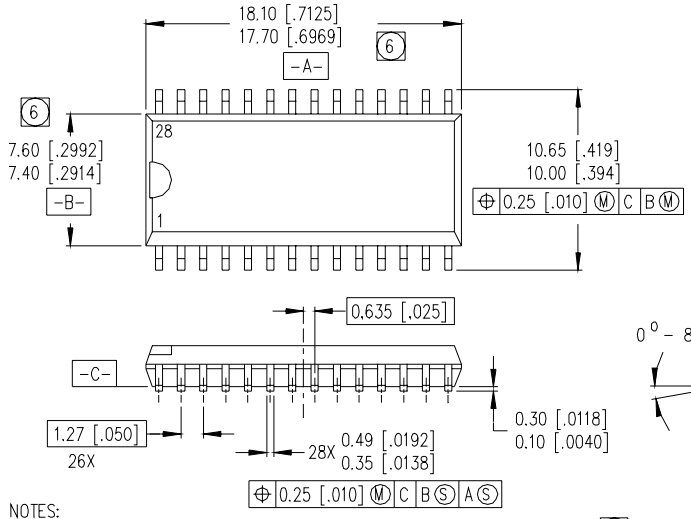


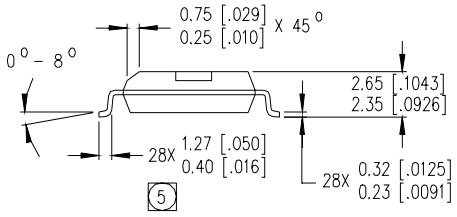
NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-011AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



28-Lead PDIP (wide body)

01-6011
01-3024 02 (MS-011AB)





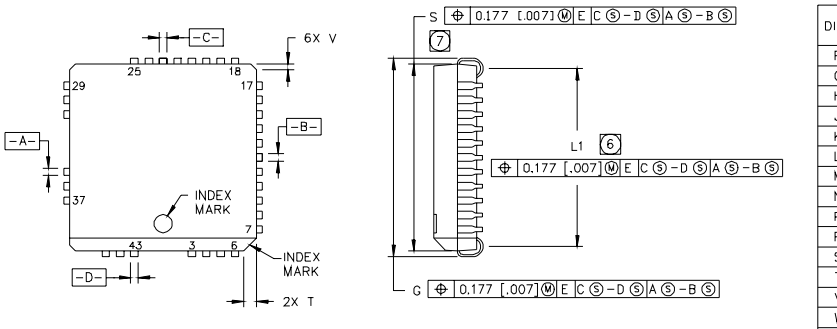
NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AE.

5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

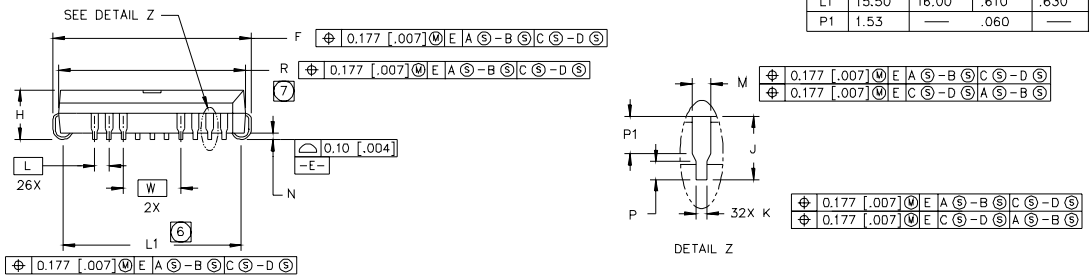
28-Lead SOIC (wide body)

01-6013
01-304002 (MS-013AE)

Case outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F	17.40	17.65	.685	.695
G	17.40	17.65	.685	.695
H	4.20	4.57	.165	.180
J	2.29	3.04	.090	.120
K	0.33	0.48	.013	.019
L	1.27 BSC		.050 BSC	
M	0.66	0.81	.026	.032
N	0.51	—	.020	—
P	0.64	—	.025	—
R	16.51	16.66	.650	.656
S	16.51	16.66	.650	.656
T	1.07	1.21	.042	.048
V	—	0.50	—	.020
W	5.08 BSC		.200 BSC	
L1	15.50	16.00	.610	.630
P1	1.53	—	.060	—



NOTES

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M-1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS-018AC.
5. DATUMS -A-, -B-, -C-, & -D- ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.
6. TO BE MEASURED AT -E- SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

44-Lead PLCC w/o 12 leads

01-6009 00
01-3004 02(mod.) (MS-018AC)

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

Data and specifications subject to change without notice. 5/16/2001

International
IOR Rectifier

Preliminary Data Sheet No. PD60032-M

IR2131(J)(S)

3 HIGH SIDE AND 3 LOW SIDE DRIVER

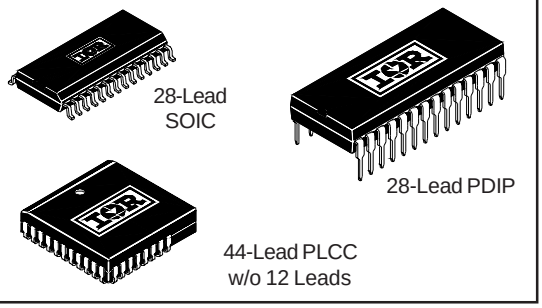
Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 high side & 3 low side drivers
- Matched propagation delay for all channels
- 2.5V logic compatible
- Outputs out of phase with inputs

Product Summary

V_{OFFSET}	600V max.
I_O+/-	160 mA / 360 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	1.3 & 0.6 µs
Deadtime (typ.)	700 ns

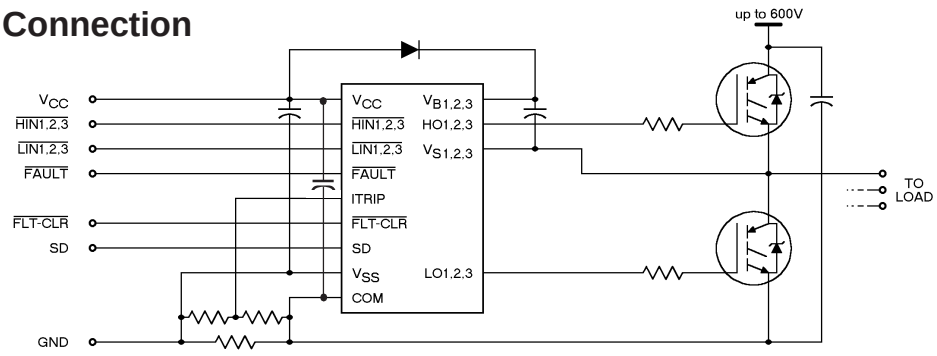
Packages



Description

The IR2131(J)(S) is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 2.5V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. A shutdown input is provided for a customized shutdown function. An open drain $\overline{\text{FAULT}}$ signal is provided to indicate that any of the shutdowns has occurred. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operate up to 600 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional Information is shown in Figures 7 through 10.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Voltage	-0.3	625	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	$V_{B1,2,3}$ - 25	$V_{B1,2,3}$ + 0.3	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Low Side and Logic Fixed Supply Voltage	-0.3	25	
V_{SS}	Logic Ground	V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low Side Output Voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage ($\overline{HIN1,2,3}$, $\overline{LIN1,2,3}$, $\overline{FLT-CLR}$, SD & ITRIP)	V_{SS} - 0.3	V_{SS} + 15	
V_{FLT}	$\overline{FAULT}$ Output Voltage	V_{SS} - 0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$ (28 Lead DIP)	—	1.5	W
	(28 Lead SOIC)	—	1.6	
	(44 Lead PLCC)	—	2.0	
Rth_{JA}	Thermal Resistance, Junction to Ambient (28 Lead DIP)	—	83	°C/W
	(28 Lead SOIC)	—	78	
	(44 Lead PLCC)	—	63	
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Voltage	$V_{S1,2,3}$ + 10	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	Note 1	600	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Low Side and Logic Fixed Supply Voltage	10	20	
V_{SS}	Logic Ground	-5	5	
$V_{LO1,2,3}$	Low Side Output Voltage	0	V_{CC}	
V_{IN}	Logic Input Voltage ($\overline{HIN1,2,3}$, $\overline{LIN1,2,3}$, $\overline{FLT-CLR}$, SD & ITRIP)	V_{SS}	V_{SS} + 5	
V_{FLT}	$\overline{FAULT}$ Output Voltage	V_{SS}	V_{CC}	
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of -5V to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).
Note 2: All input pins, CA- and CAO pins are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S1,2,3}$ = V_{SS} = COM, C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are defined in Figures 4 through 5.

Parameter		Value				
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	0.6	1.3	2.0	µs	V_{IN} = 0 & 5V $V_{S1,2,3}$ = 0 to 600V
t_{off}	Turn-Off Propagation Delay	0.2	0.6	1.0		
t_r	Turn-On Rise Time	—	80	150	ns	
t_f	Turn-Off Fall Time	—	40	100		
t_{itrip}	ITRIP to Output Shutdown Propagation Delay	400	700	1000		V_{IN}, V_{ITRIP} = 0 & 5V
t_{bl}	ITRIP Blanking Time	—	400	—		V_{ITRIP} = 1V
t_{flt}	ITRIP to $\overline{FAULT}$ Indication Delay	400	700	1000		V_{IN}, V_{ITRIP} = 0 & 5V
$t_{flt,in}$	Input Filter Time (All Six Inputs)	—	310	—		V_{IN} = 0 & 5V
t_{fltclr}	$\overline{FLT-CLR}$ to $\overline{FAULT}$ Clear Time	400	800	1200		V_{IN}, V_{IT}, V_{FC} = 0&5V
t_{sd}	SD to Output Shutdown Propagation Delay	400	700	1000		V_{IN}, V_{SD} = 0 & 5V
DT	Deadtime	400	700	1200		V_{IN} = 0 & 5V

NOTE: For high side PWM, HIN pulse width must be ≥ 1.5µsec

Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S1,2,3}$ = V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: $\overline{HIN1,2,3}$ & $\overline{LIN1,2,3}$. The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

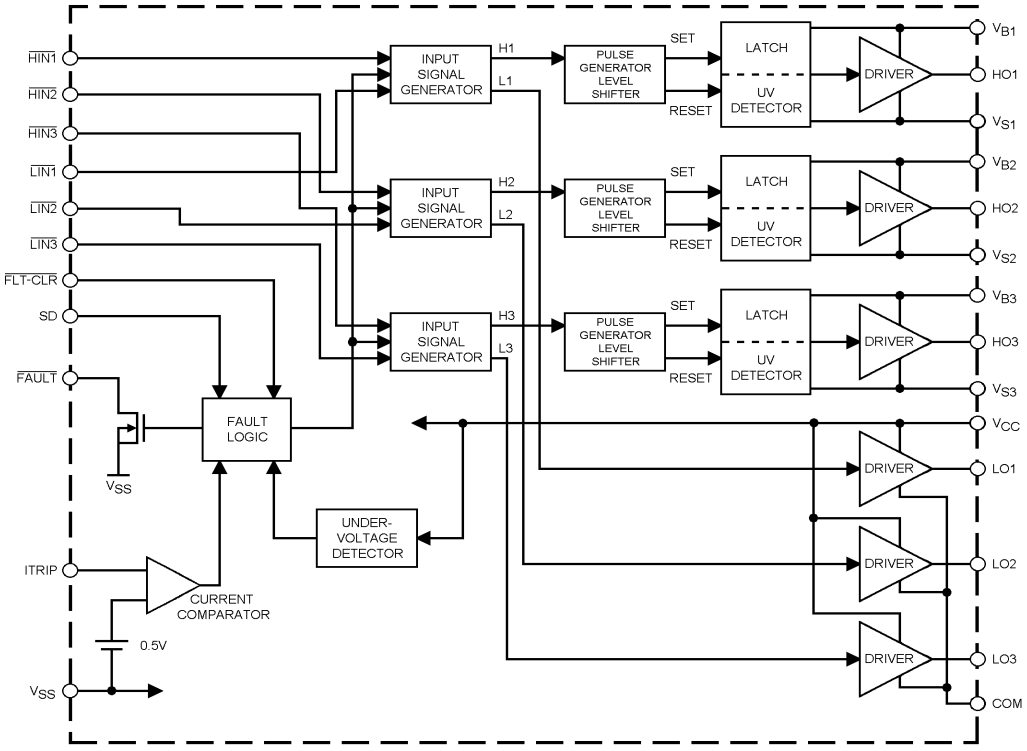
Parameter		Value				
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “0” Input Voltage (OUT = LO)	2.2	—	—	V	
V_{IL}	Logic “1” Input Voltage (OUT = HI)	—	—	0.8		
$V_{FCLR,IH}$	Logic “0” Fault Clear Input Voltage	2.2	—	—		
$V_{FCLR,IL}$	Logic “1” Fault Clear Input Voltage	—	—	0.8		
$V_{SD,TH+}$	Shutdown Input Positive Going Threshold	1.2	1.8	2.1		
$V_{SD,TH-}$	Shutdown Input Negative Going Threshold	0.9	1.5	1.8		
$V_{IT,TH+}$	ITRIP Input Positive Going Threshold	250	485	600	mV	
$V_{IT,TH-}$	ITRIP Input Negative Going Threshold	200	400	550		
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	—	—	100		V_{IN} = 0V, I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	—	—	100		V_{IN} = 5V, I_O = 0A
I_{LK}	Offset Supply Leakage Current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} Supply Current	—	30	100		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	—	3.0	4.5	mA	V_{IN} = 0V or 5V
I_{IN+}	Logic “1” Input Bias Current (OUT = HI)	—	190	300	µA	V_{IN} = 0V
I_{IN-}	Logic “0” Input Bias Current (OUT = LO)	—	50	100		V_{IN} = 5V
I_{ITRIP+}	“High” ITRIP Bias Current	—	75	150		ITRIP = 5V
I_{ITRIP-}	“Low” ITRIP Bias Current	—	—	100	nA	ITRIP = 0V
I_{FCLR+}	Logic “1” Fault Clear Bias Current	—	125	250	µA	$\overline{FLT-CLR}$ = 0V
I_{FCLR-}	Logic “0” Fault Clear Bias Current	—	75	150		$\overline{FLT-CLR}$ = 5V
I_{SD+}	Logic “1” Shutdown Bias Current	—	75	150		SD = 5V
I_{SD-}	Logic “0” Shutdown Bias Current	—	—	100	nA	SD = 0V

Static Electrical Characteristics -- Continued

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S1,2,3}$ = V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: $\overline{HIN1,2,3}$ & $\overline{LIN1,2,3}$. The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

Parameter		Value				
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	8.2	8.7	9.2	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	7.8	8.3	8.8		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	8.2	8.7	9.2		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	7.8	8.3	8.8		
$R_{on,FLT}$	$\overline{FAULT}$ Low On-Resistance	—	55	75	Ω	
I_{O+}	Output High Short Circuit Pulsed Current	160	250	—	mA	V_O = 0V, V_{IN} = 0V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	360	500	—		V_O = 15V, V_{IN} = 5V PW ≤ 10 µs

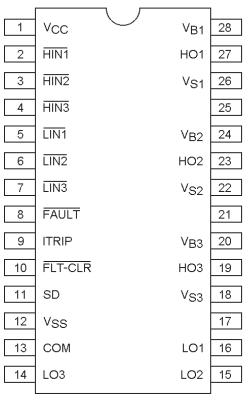
Functional Block Diagram



Lead Definitions

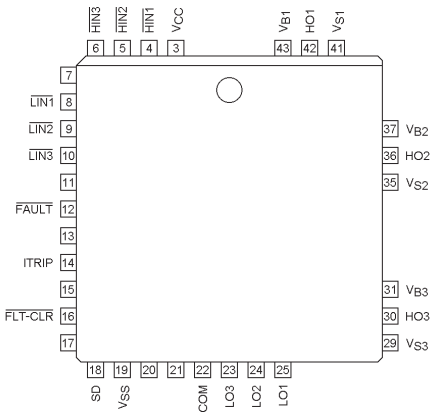
Lead Symbol	Description
$\overline{HIN1,2,3}$	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase
$\overline{LIN1,2,3}$	Logic inputs for low side gate driver output (LO1,2,3), out of phase
$\overline{FLT-CLR}$	Logic input for fault clear
SD	Logic input for shutdown
$\overline{FAULT}$	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic
V_{CC}	Low side and logic fixed supply
ITRIP	Input for over-current shutdown
V_{SS}	Logic ground
$V_{B1,2,3}$	High side floating supplies
HO1,2,3	High side gate drive outputs
$V_{S1,2,3}$	High side floating supply returns
LO1,2,3	Low side gate drive outputs
COM	Low side return

Lead Assignments



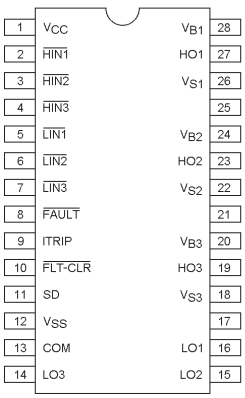
28 Lead DIP

IR2131



44 Lead PLCC w/o 12 Leads

IR2131J



28 Lead SOIC (Wide Body)

IR2131S

Part Number

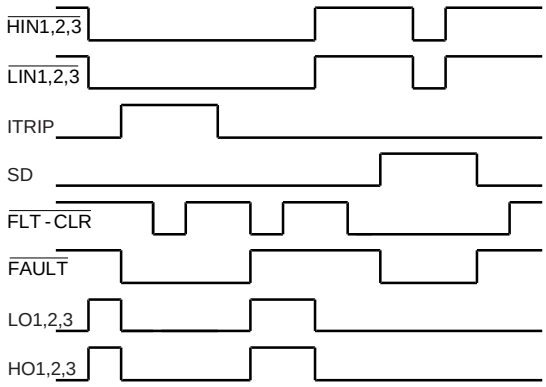


Figure 1. Input/Output Timing Diagram

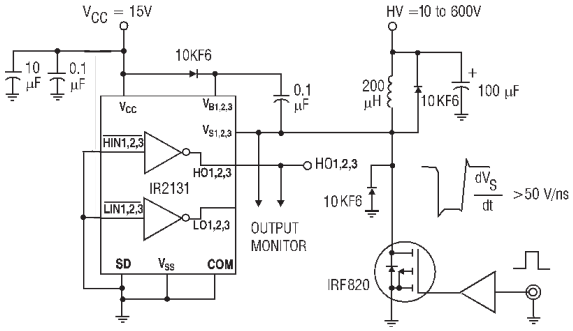


Figure 2. Floating Supply Voltage Transient Test Circuit

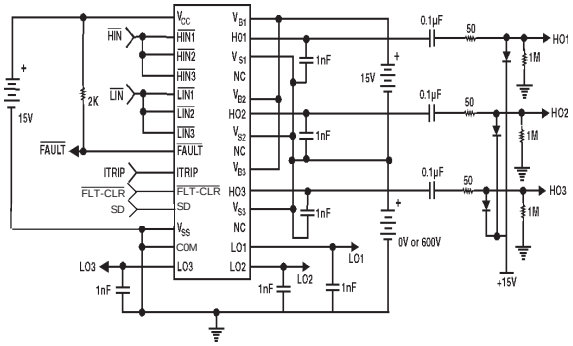


Figure 3. Switching Time Test Circuit

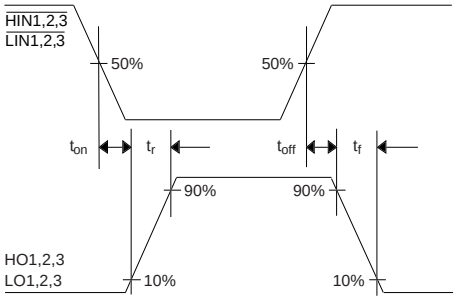


Figure 4. Switching Time Waveform Definitions

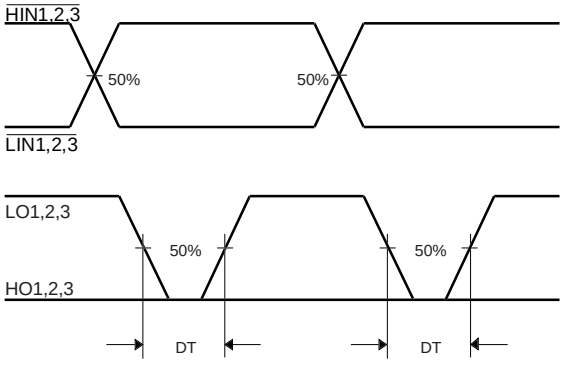


Figure 5. Deadtime Waveform Definitions

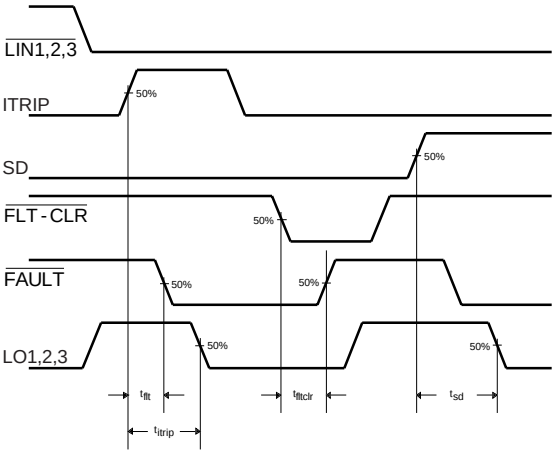


Figure 6. Shutdown Waveform Definitions

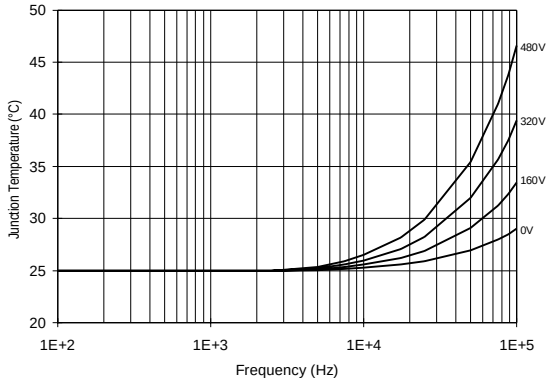


Figure 7. IR2131 T_J vs. Frequency (IRF820)
R_{GATE} = 33Ω, V_{CC} = 15V

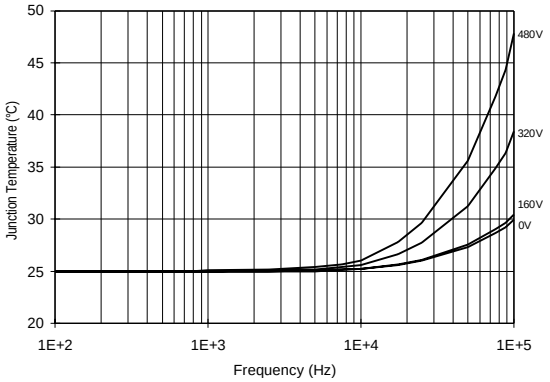


Figure 8. IR2131 T_J vs. Frequency (IRF830)
R_{GATE} = 20Ω, V_{CC} = 15V

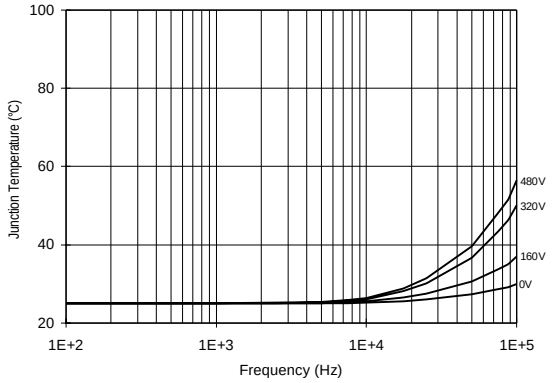


Figure 9. IR2131 T_J vs. Frequency (IRF840)
R_{GATE} = 15Ω, V_{CC} = 15V

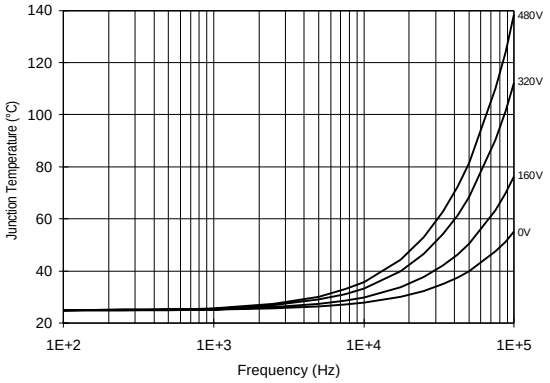
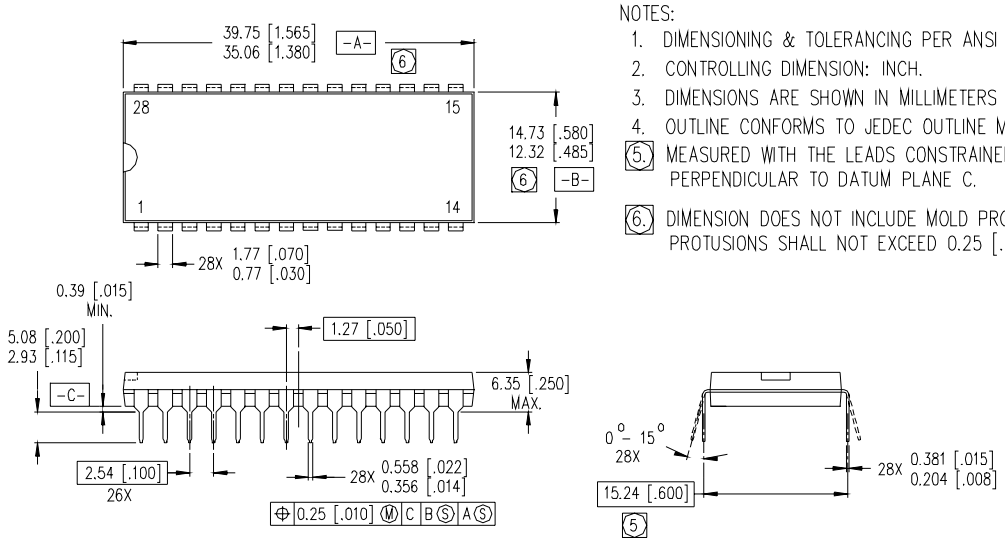


Figure 10. IR2131 T_J vs. Frequency (IRF450)
R_{GATE} = 10Ω, V_{CC} = 15V

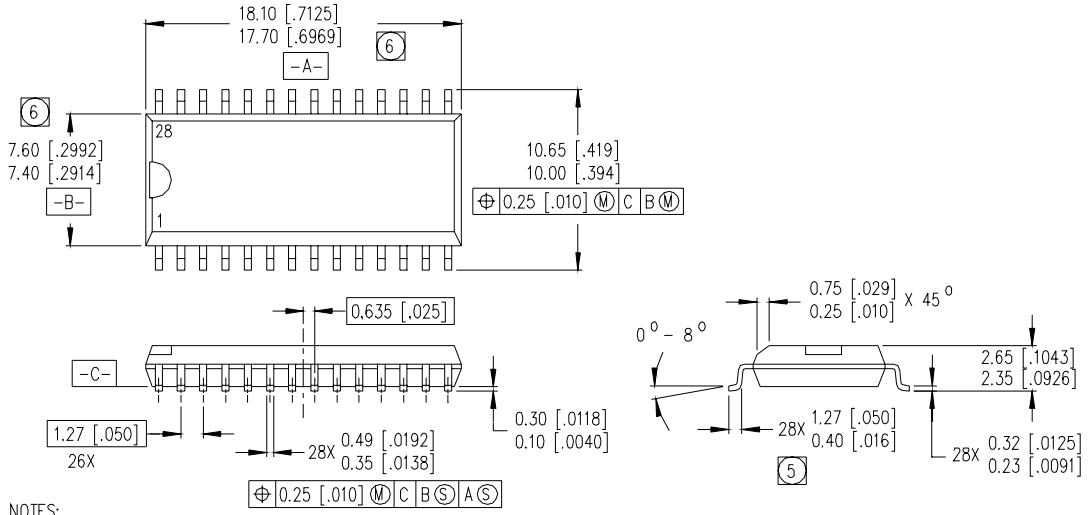
Case outlines



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-011AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

28-Lead PDIP (wide body)

01-6011
01-3024 02 (MS-011AB)

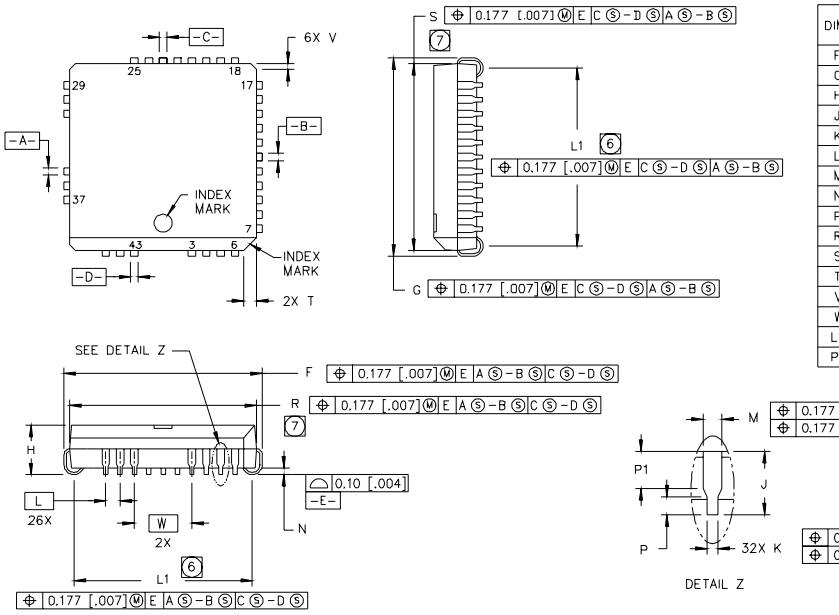


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AE.

5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

28-Lead SOIC (wide body)

01-6013
01-3040 02 (MS-013AE)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F	17.40	17.65	.685	.695
G	17.40	17.65	.685	.695
H	4.20	4.57	.165	.180
J	2.29	3.04	.090	.120
K	0.33	0.48	.013	.019
L	1.27 BSC		.050 BSC	
M	0.66	0.81	.026	.032
N	0.51	—	.020	—
P	0.64	—	.025	—
R	16.51	16.66	.650	.656
S	16.51	16.66	.650	.656
T	1.07	1.21	.042	.048
V	—	0.50	—	.020
W	5.08 BSC		.200 BSC	
L1	15.50	16.00	.610	.630
P1	1.53	—	.060	—

NOTES

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M-1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS-018AC.
5. DATUMS -A-, -B-, -C-, & -D- ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.
6. TO BE MEASURED AT -E- SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

44-Lead PLCC w/o 12 leads

01-6009 00
01-3004 02(mod.) (MS-018AC)

International
IOR Rectifier

Data Sheet No. PD60107-P

IR2133/IR2135 (J&S)
IR2233/IR2235 (J&S)

3-PHASE BRIDGE DRIVER

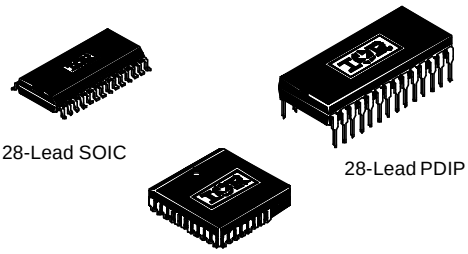
Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V or+1200V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10V/12V to 20V DC and up to 25V for transient
- Undervoltage lockout for all channels
- Over-current shut down turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- 2.5V logic compatible
- Outputs out of phase with inputs

Product Summary

V_{OFFSET}	600V or 1200V max.
$I_{O+/-}$	200 mA / 420 mA
V_{OUT}	10 - 20V or 12 - 20V
$t_{on/off}$ (typ.)	750/700 ns
Deadtime (typ.)	250 ns

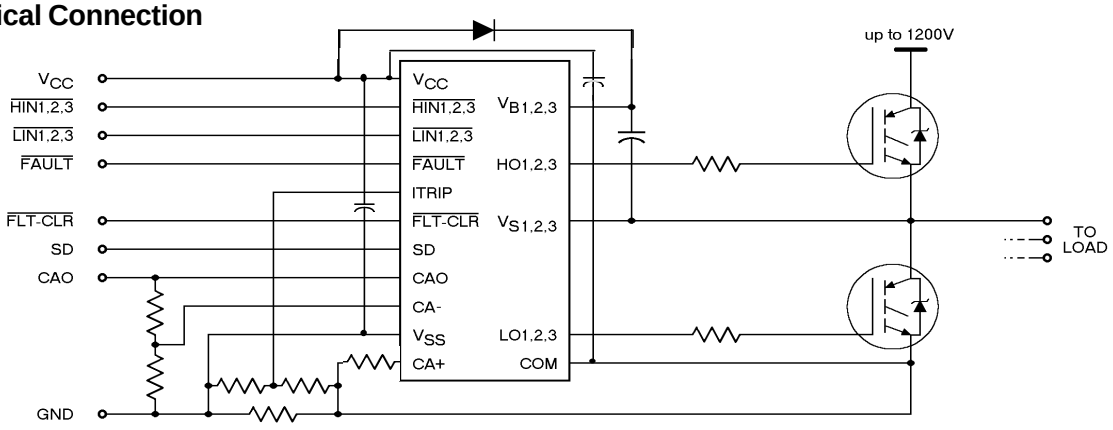
Packages



Description

The IR2133IR2135/IR2233IR2355 (J&S) are high voltage, high speed power MOSFET and IGBT driver with three independent high side and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 2.5V logic. An independent operational amplifier provides an analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs can also be derived from this resistor. A shutdown function is available to terminate all six outputs. An open drain $\overline{\text{FAULT}}$ signal is provided to indicate that an over-current or undervoltage shutdown has occurred. Fault conditions are cleared with the $\overline{\text{FLT-CLR}}$ lead. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 volts or 1200 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only.
Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage (IR2133/IR2135)	-0.3	625	V
	(IR2233/IR2235)	-0.3	1225	
$V_{S1,2,3}$	High side floating supply offset voltage	$V_{B1,2,3}$ - 25	$V_{B1,2,3}$ + 0.3	
$V_{HO1,2,3}$	High side floating output voltage	$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Fixed supply voltage	-0.3	25	
V_{SS}	Logic ground	V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low side output voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage ($\overline{HIN}$, $\overline{LIN}$, ITRIP, SD & $\overline{FLT\text{-}CLR}$)	V_{SS} - 0.3	V_{SS} + 15	
$V_{IN,AMP}$	Op amp input voltage (CA+ & CA-)	V_{SS} - 0.3	V_{CC} + 0.3	
$V_{OUT,AMP}$	Op amp output voltage (CAO)	V_{SS} - 0.3	V_{CC} + 0.3	
V_{FLT}	$\overline{FAULT}$ output voltage	V_{SS} - 0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq 25^oC$ (28 Lead PDIP)	—	1.5	W
	(28 Lead SOIC)	—	1.6	
	(44 lead PLCC)	—	2.0	
Rth_{JA}	Thermal resistance, junction to ambient (28 Lead PDIP)	—	83	°C/W
	(28 Lead SOIC)	—	78	
	(44 lead PLCC)	—	63	
T_J	Junction temperature	—	125	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Parameter Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	$V_{S1,2,3}$ + 10/12	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High side floating supply offset voltage (IR2133/IR2135)	Note 1	600	
	(IR2233/IR2235)	Note 1	1200	
$V_{HO1,2,3}$	High side floating output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Fixed supply voltage	10 or 12	20	
V_{SS}	Low side driver return	-5	5	
$V_{LO1,2,3}$	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage ($\overline{HIN}$, $\overline{LIN}$, ITRIP, SD & $\overline{FLT\text{-}CLR}$)	V_{SS}	V_{SS} + 5	
$V_{IN,AMP}$	Op amp input voltage (CA+ & CA-)	V_{SS}	V_{SS} + 5	
$V_{OUT,AMP}$	Op amp output voltage (CAO)	V_{SS}	V_{SS} + 5	
V_{FLT}	$\overline{FAULT}$ output voltage	V_{SS}	V_{CC}	

Note 1: Logic operational for V_S of COM - 5V to COM + 600V/1200V. Logic state held for V_S of COM -5V to COM -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Note 2: All input pins, op amp input and output pins are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S1,2,3}$ = V_{SS}, T_A = 25°C and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	500	750	1000	ns	V_{IN} = 0 & 5V $V_{S1,2,3}$ = 0 to 600V or 1200V
t_{off}	Turn-off propagation delay	450	700	950		
t_r	Turn-on rise time	—	90	150		
t_f	Turn-off fall time	—	40	70		
t_{sd}	SD to output shutdown propagation delay	500	750	1000		V_{IN},V_{SD} = 0 & 5V
t_{itrip}	ITRIP to output shutdown propagation delay	600	850	1100		V_{IN},V_{ITRIP} = 0 & 5V
t_{bl}	ITRIP blanking time	—	400	—		ITRIP = 1V
t_{flt}	ITRIP to $\overline{FAULT}$ propagation delay	400	650	900		V_{IN},V_{ITRIP} = 0 & 5V
$t_{fil,in}$	Input filter time ($\overline{HIN}$, $\overline{LIN}$ and SD)	—	310	—		V_{IN} = 0 & 5V
t_{fltclr}	$\overline{FLT\text{-}CLR}$ to $\overline{FAULT}$ clear time	600	850	1100		V_{IN},V_{ITRIP} = 0 & 5V
DT	Deadtime, LS turn-off to HS turn-on & HS turn-off to LS turn-on	100	250	400		V_{IN} = 0 & 5V
SR+	Amplifier slew rate (positive)	5	10	—	V/µs	
SR-	Amplifier slew rate (negative)	2	2.5	—		

NOTE: For high side PWM, HIN pulse width must be ≥ 1µ sec

Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V unless otherwise specified and T_A = 25°C. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels ($H_{S1,2,3}$ & $L_{S1,2,3}$). The VO and IO parameters are referenced to V_{SS} and $V_{S1,2,3}$ and are applicable to the respective output leads: $H_{O1,2,3}$ or $L_{O1,2,3}$.

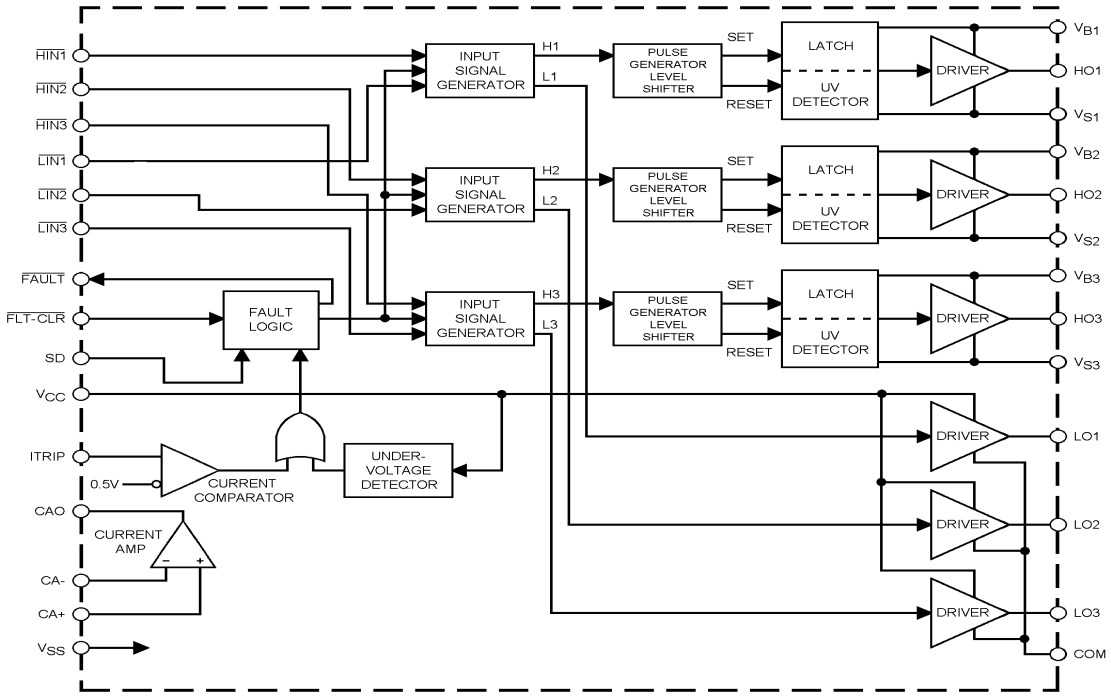
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" Input Voltage (OUT = LO)	2.2	—	—	V	
V_{IL}	Logic "1" Input Voltage (OUT = HI)	—	—	0.8		
$V_{FCLR,IH}$	Logic "0" Fault Clear Input Voltage	2.2	—	—		
$V_{FCLR,IL}$	Logic "1" Fault Clear Input Voltage	—	—	0.8		
$V_{SD,TH+}$	SD Input Positive Going Threshold	1.2	1.65	2.1		
$V_{SD,TH-}$	SD Input Negative Going Threshold	0.9	1.35	1.8		
$V_{IT,TH+}$	I_{ITRIP} Input Positive Going Threshold	420	520	620	mV	
$V_{IT,TH-}$	I_{ITRIP} Input Negative Going Threshold	340	440	540		
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	—	—	100		V_{IN} = 0V, I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	—	—	100		V_{IN} = 5V, I_O = 0A
I_{LK}	Offset Supply Leakage Current (IR2133/IR2135)	—	—	50	µA	$V_{B1,2,3}$=$V_{S1,2,3}$ = 600V
	(IR2233/IR2235)	—	—	50		$V_{B1,2,3}$=$V_{S1,2,3}$ = 1200V
I_{QBS}	Quiescent V_{BS} Supply Current	—	50	100		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	—	4	8	mA	V_{IN} = 0V or 5V
I_{IN+}	Logic "1" Input Bias Current (OUT = HI)	—	200	350	µA	V_{IN} = 0V
I_{IN-}	Logic "0" Input Bias Current (OUT = LO)	—	100	250		V_{IN} = 5V
I_{SD+}	"High" Shutdown Bias Current	—	30	100		SD = 5V
I_{SD-}	"Low" Shutdown Bias Current	—	—	100	nA	SD = 0V
I_{ITRIP+}	"High" I_{ITRIP} Bias Current	—	30	100	µA	I_{ITRIP} = 5V
I_{ITRIP-}	"Low" I_{ITRIP} Bias Current	—	—	100	nA	I_{ITRIP} = 0V

Static Electrical Characteristics — Continued

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (HS1,2,3 & LS1,2,3). The VO and IO parameters are referenced to V_{SS} and $V_{S0,1,2,3}$ and are applicable to the respective output leads: HO or LO.

Symbol	Parameter Definition	Min.	Typ.	Max.	Units	Test Conditions
$I_{FLTCLR+}$	"High" Fault Clear Input Bias Current	—	200	350	µA	$\overline{\text{FLT-CLR}}$ = 0V
$I_{FLTCLR-}$	"Low" Fault Clear Input Bias Current	—	100	250		$\overline{\text{FLT-CLR}}$ = 5V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold				V	
	(for IR2133/IR2233)	7.6	8.6	9.6		
	(for IR2135/IR2235)	9.2	10.4	11.6		
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold					
	(for IR2133/IR2233)	7.2	8.2	9.2		
	(for IR2135/IR2235)	8.3	9.4	10.5		
V_{BSUVH}	V_{BS} Supply Undervoltage Lockout Hysteresis					
	(for IR2133/IR2233)	—	0.4	—		
	(for IR2135/IR2235)	—	1	—		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold					
	(for IR2133/IR2233)	7.6	8.6	9.6		
	(for IR2135/IR2235)	9.2	10.4	11.6		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold					
	(for IR2133/IR2233)	7.2	8.2	9.2		
	(for IR2135/IR2235)	8.3	9.4	10.5		
V_{CCUVH}	V_{CC} Supply Undervoltage Lockout Hysteresis					
	(for IR2133/IR2233)	—	0.4	—		
	(for IR2135/IR2235)	—	1	—		
$R_{on,FLT}$	FAULT- Low On Resistance	—	70	100	Ω	
I_{O+}	Output High Short Circuit Pulsed Current	190	250	—	mA	V_{OUT} = 0V, V_{IN} = 0V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	380	500	—		V_{OUT} = 15V, V_{IN} = 5V PW ≤ 10 µs
V_{OS}	Amplifier Input Offset Voltage	—	0	30	mV	CA+=0.2V, CA-=CAO
$I_{IN,AMP}$	Amplifier Input Bias Current	—	—	4	nA	CA+ = CA- = 2.5V
CMRR	Amplifier Common Mode Rejection Ratio	50	70	—	dB	CA+ = 0.1V & 5V, CA- = CAO
PSRR	Amplifier Power Supply Rejection Ratio	50	70	—		CA+=0.2V, CA-=CAO V_{CC} = 10V & 20V
$V_{OH,Amp}$	Amplifier High Level Output Voltage	5	5.2	5.4	V	CA+ = 1V, CA- = 0V
$V_{OL,Amp}$	Amplifier Low Level Output Voltage	—	—	20	mV	CA+ = 0V, CA- = 1V
$I_{SRC,Amp}$	Amplifier Output Source Current	4	7	—	mA	CA+ = 1V, CA- = 0V, CAO = 4V
$I_{SNK,Amp}$	Amplifier Output Sink Current	0.5	1	—		CA+ = 0V, CA- = 1V, CAO = 2V
$I_{O+,Amp}$	Amplifier Output High Short Circuit Current	—	10	—		CA+ = 5V, CA- = 0V, CAO = 0V
$I_{O-,Amp}$	Amplifier Output Low Short Circuit Current	—	4	—		CA+ = 0V, CA- = 5V, CAO = 5V

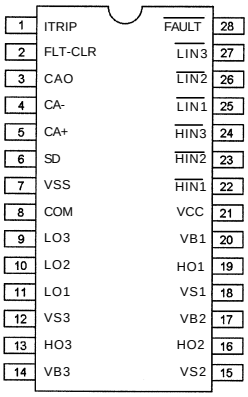
Functional Block Diagram



Lead Definitions

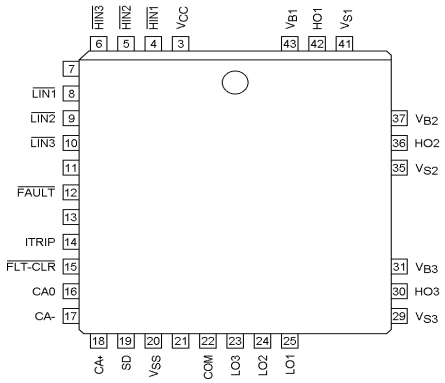
Symbol	Lead Description
$\overline{\text{HIN1,2,3}}$	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase.
$\overline{\text{LIN1,2,3}}$	Logic inputs for low side gate driver outputs (LO1,2,3), out of phase.
$\overline{\text{FAULT}}$	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic.
V_{CC}	Logic and low side fixed supply.
ITRIP	Input for over-current shut down.
$\overline{\text{FLT-CLR}}$	Logic input for fault clear, negative logic.
SD	Logic input for shut down.
CAO	Output of current amplifier.
CA-	Negative input of current amplifier.
CA+	Positive input of current amplifier.
V_{SS}	Logic ground.
COM	Low side return.
$V_{B1,2,3}$	High side floating supplies.
HO1,2,3	High side gate drive outputs.
$V_{S1,2,3}$	High side floating supply returns.
LO1,2,3	Low side gate drive outputs

Lead Assignments



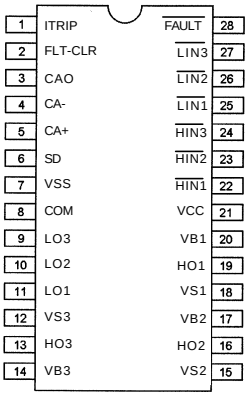
28 Lead DIP

IR2133
IR2135
IR2233
IR2235



44 Lead PLCC w/o 12 Leads

IR2133J
IR2135J
IR2233J
IR2235J



28 Lead SOIC (Wide Body)

IR2133S
IR2135S
IR2233S
IR2235S

Part Number

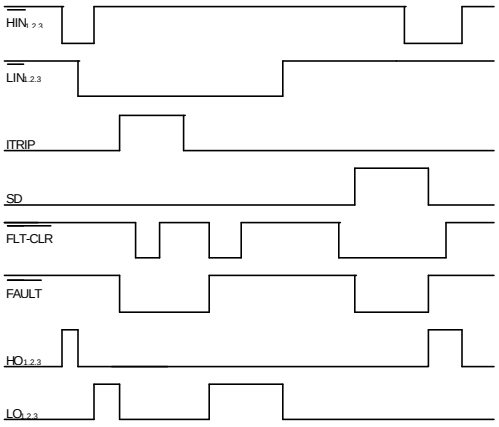


Figure 1. Input/Output Timing Diagram

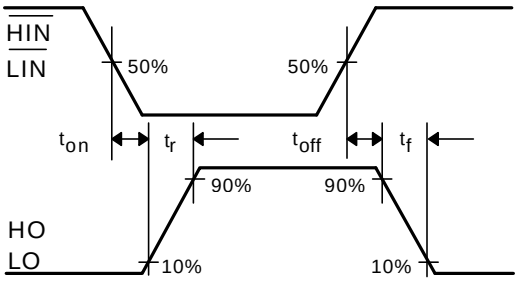


Figure 2. Switching Time Waveform Definitions

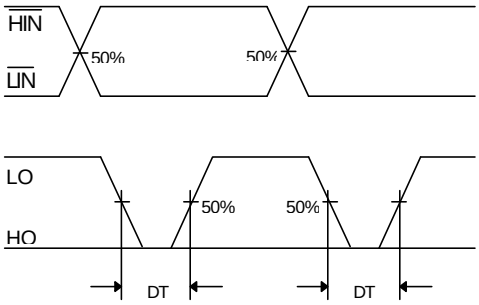


Figure 3. Deadtime Waveform Definitions

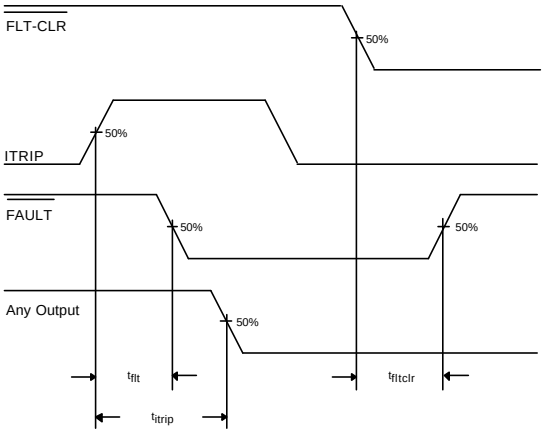


Figure 4. Overcurrent Shutdown Waveform

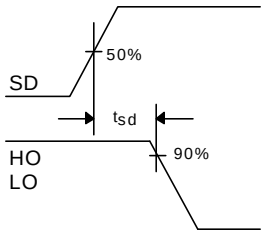


Figure 5. Shutdown Waveform Definitions

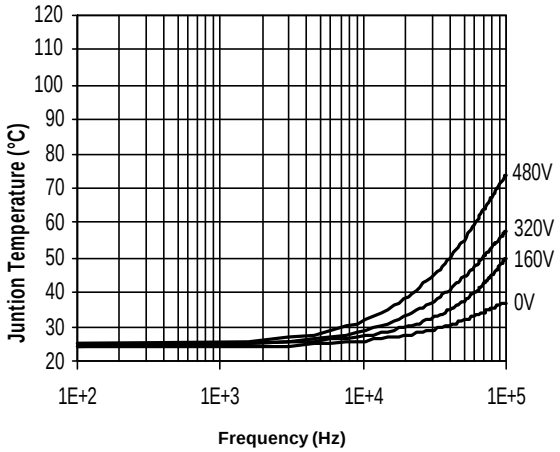


Figure 7. IR2133J Junction Temperature vs Frequency Driving (IRGPC20KD2) Rgate = 5.1Ω @ Vcc = 15V

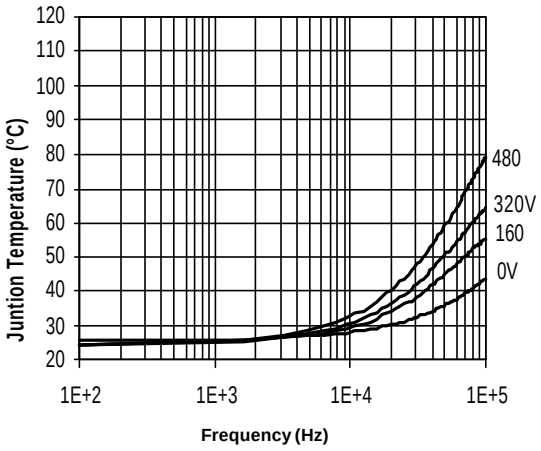


Figure 8. IR2133J Junction Temperature vs Frequency Driving (IRGPC30KD2) Rgate = 5.1Ω @ Vcc = 15V

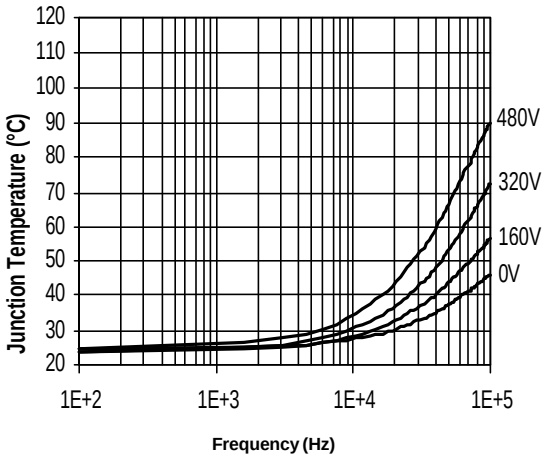


Figure 9. IR2133J Junction Temperature vs Frequency Driving (IRGPC40KD2) Rgate = 5.1Ω @ Vcc = 15V

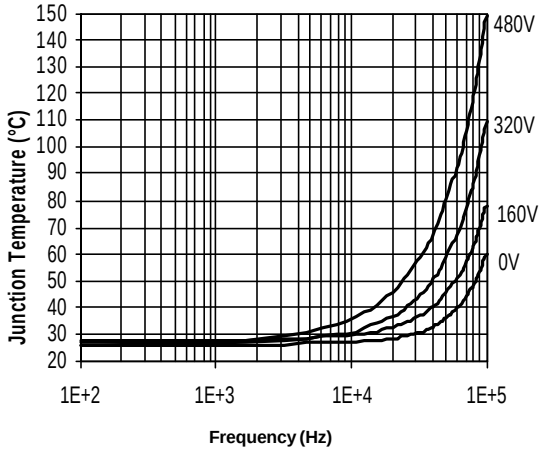


Figure 10. IR2133J Junction Temperature vs Frequency Driving (IRGPC50KD2) Rgate = 5.1Ω @ Vcc = 15V

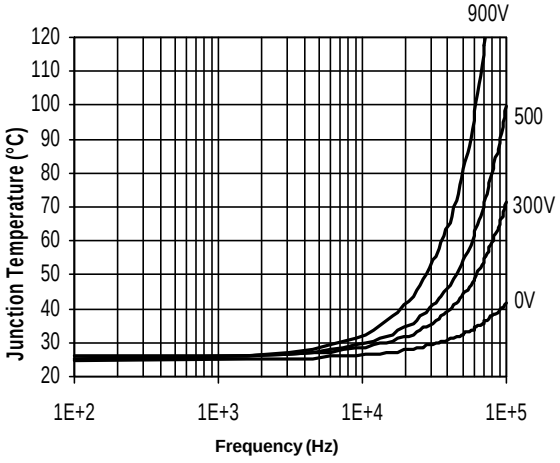


Figure 11. IR2233J Junction Temperature vs Frequency Driving (IRG4PH30KD) Rgate = 20Ω @ Vcc = 15V

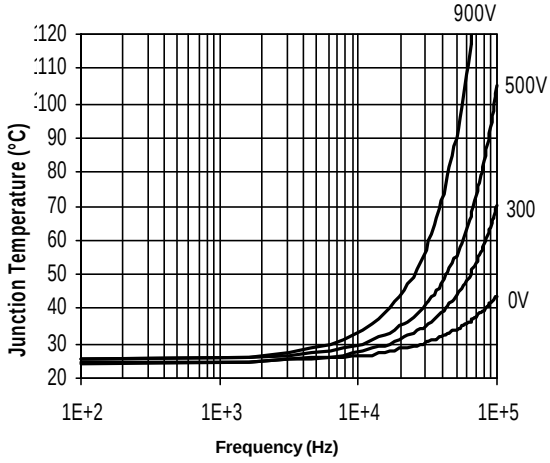


Figure 12. IR2233J Junction Temperature vs Frequency Driving (IRG4PH40KD) Rgate = 15Ω @ Vcc = 15V

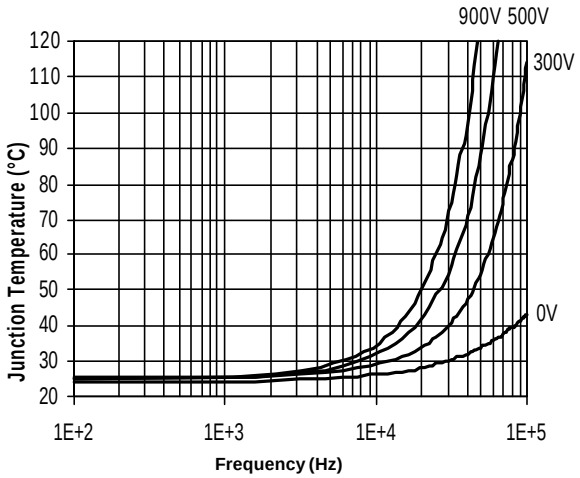


Figure 13. IR2233J Junction Temperature vs Frequency Driving (IRG4PH50KD) Rgate = 10Ω @ Vcc = 15V

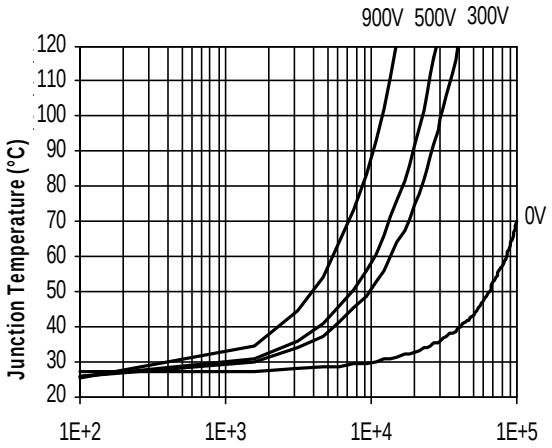
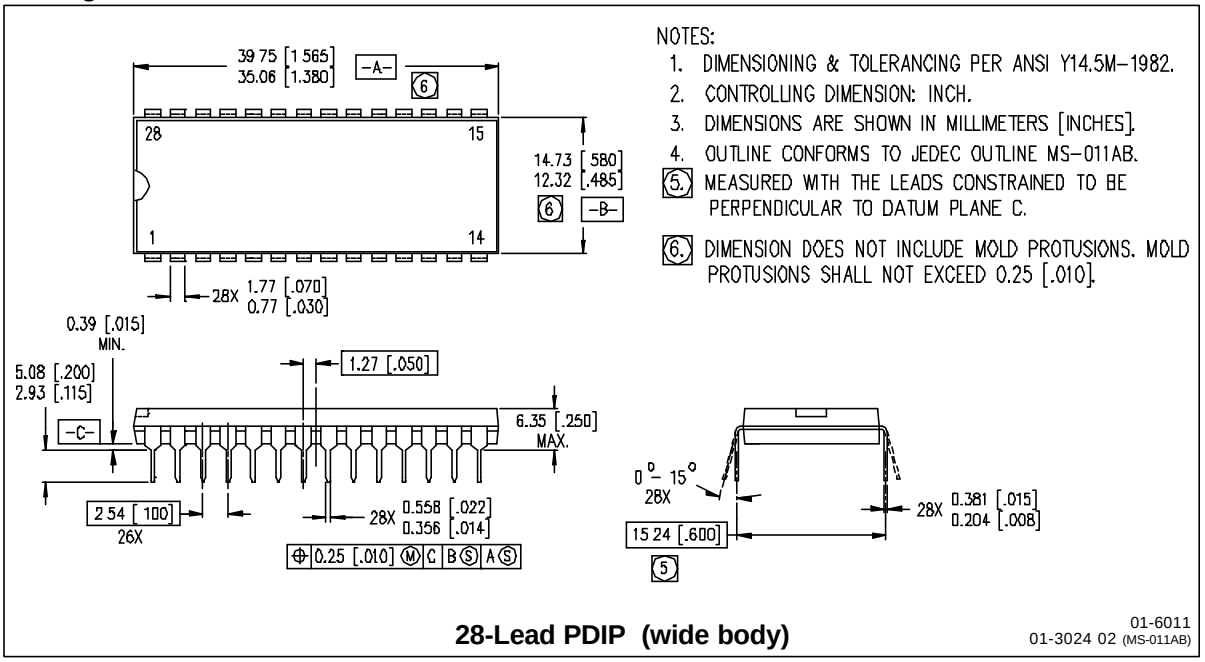
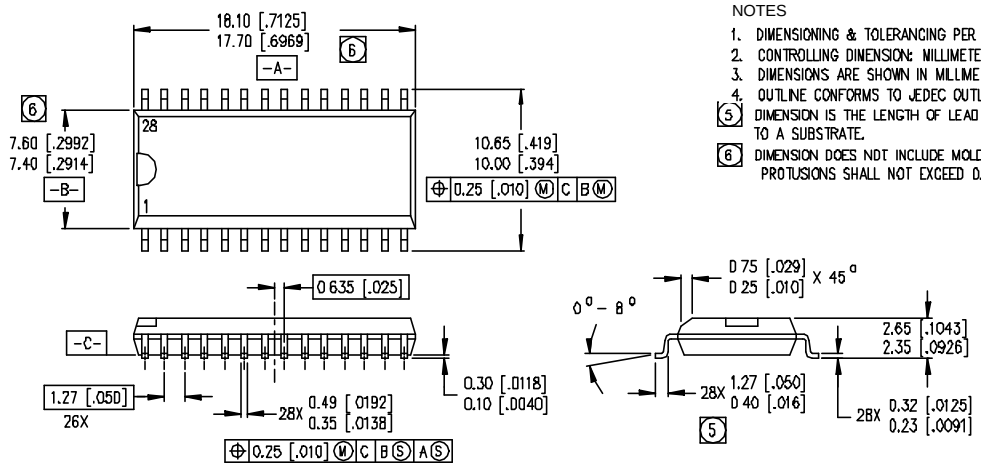


Figure 14. IR2133J Junction Temperature vs Frequency Driving (IRG4ZH71KD) Rgate = 5Ω @ Vcc = 15V

Package Dimensions



28-Lead PDIP (wide body)

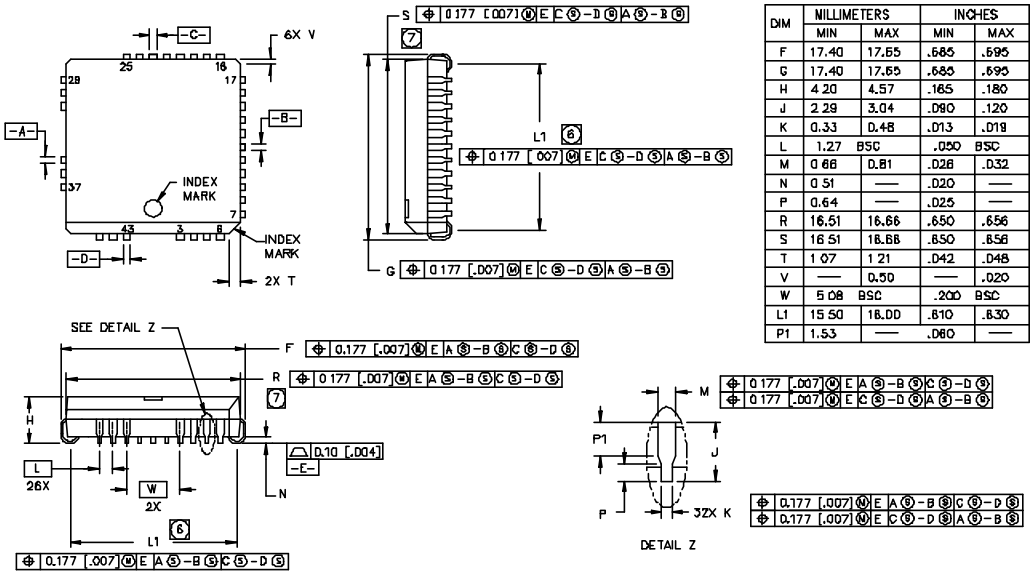


NOTES

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AE.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

28-Lead SOIC (wide body)

01-6013
01-3040 02 (MS-013AE)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F	17.40	17.65	.685	.695
G	17.40	17.65	.685	.695
H	4.20	4.57	.165	.180
J	2.29	3.04	.090	.120
K	0.33	0.48	.013	.019
L	1.27 BSC		.050 BSC	
M	0.66	0.81	.026	.032
N	0.51	—	.020	—
P	0.64	—	.025	—
R	16.51	16.66	.650	.656
S	16.51	16.66	.650	.656
T	1.07	1.21	.042	.048
V	—	0.50	—	.020
W	5.08 BSC		.200 BSC	
L1	15.50	16.00	.610	.630
P1	1.53	—	.060	—

NOTES:

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M-1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH
4. CONFORMS TO JEDEC OUTLINE MS-018AC.
5. DATUMS -A-, -B-, -C-, & -D- ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.
6. TO BE MEASURED AT -E- SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

44-Lead PLCC w/o 12 leads

01-6009 00
01-3004 02(mod.) (MS-018AC)

10/3/2001

Preliminary Data Sheet No. PD60166-G

International
IOR Rectifier

IR2136/IR21362/IR21363 (J&S)

3-PHASE BRIDGE DRIVER

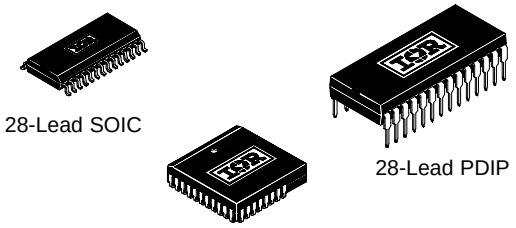
Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V (IR2136/ IR21363) or 12 to 20V (IR21362)
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- Lowside outputs out of phase with inputs. High side outputs out of phase (IR2136/IR21363) or in phase (IR21362) with inputs.
- Cross-conduction prevention logic
- 3.3V logic compatible
- Lower di/dt gate driver for better noise immunity
- Externally programmable delay for automatic fault clear

Product Summary

V_{OFFSET}	600V max.
I_O+/-	120 mA / 250 mA
V_{OUT}	10 - 20V or 12V - 20V
Deadtime (typ.)	200 nsec
$t_{on/off}$ (typ.)	400 nsec

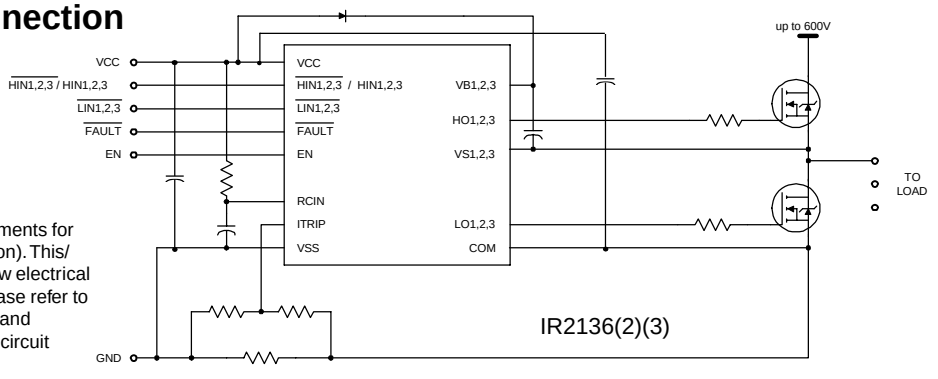
Packages



Description

The IR2136/IR21362/IR21363(J&S) are high votage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/ These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	High side offset voltage		-0.3	600	V
V_{BS}	High side floating supply voltage		-0.3	25	
V_{HO}	High side floating output voltage		$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{SS}	Logic ground		V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Input voltage $\overline{LIN}$,$\overline{HIN}$(IR2136/IR21363),HIN (IR21362) ITRIP, EN, RCIN		V_{SS} - 0.3	V_{SS} + 15	
V_{FLT}	FAULT output voltage		V_{SS} - 0.3	V_{CC} + 0.3	
dV/dt	Allowable offset voltage slew rate		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(28 lead PDIP)	—	1.5	W
		(28 lead SOIC)	—	1.6	
		(44 lead PLCC)	—	2.0	
Rth_{JA}	Thermal resistance, junction to ambient	(28 lead PDIP)	—	83	°C/W
		(28 lead SOIC)	—	78	
		(44 lead PLCC)	—	63	
T_J	Junction temperature		—	125	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	$V_{S1,2,3}$ + 10	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High side floating supply offset voltage	Note 1	600	
$V_{HO1,2,3}$	High side output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{LO1,2,3}$	Low side output voltage	0	V_{CC}	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{SS}	Logic ground	-5	5	
V_{FLT}	$\overline{FAULT}$ output voltage	V_{SS}	V_{CC}	
V_{RCIN}	RCIN input voltage	V_{SS}	V_{CC}	
V_{ITRIP}	ITRIP input voltage	V_{SS}	V_{SS} +5	
V_{IN}	Logic input voltage $\overline{LIN}$, $\overline{HIN}$ (IR2136), HIN(IR21362), EN	V_{SS}	V_{SS} +5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of COM -5 to COM +600V. Logic state held for V_S of COM -5V to -COM -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).
Note 2: All input pins and the ITRIP pin are internally clamped with a 5.2V zener diode.

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}1,2,3) = 15V unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (H_S1,2,3 and L_S1,2,3). The V_O and I_O parameters are referenced to COM and V_S1,2,3 and are applicable to the respective output leads: $H_{O1,2,3}$ and $L_{O1,2,3}$.

Symbol	Definition		Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$ Logic "1" input voltage HIN1,2,3		3	—	—	V	
V_{IL}	Logic "1" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$ Logic "0" input voltage HIN1,2,3		—	—	0.8	V	
$V_{EN,TH+}$	EN positive going threshold		—	—	3	V	
$V_{EN,TH-}$	EN negative going threshold		0.8	—	—	V	
$V_{IT,TH+}$	ITRIP positive going threshold		370	460	550	mV	
$V_{IT,HYS}$	ITRIPinput hysteresis		—	70	—	mV	
$V_{RCIN,TH+}$	RCIN positive going threshold		—	8	—	V	
$V_{RCIN,HYS}$	RCIN input hysteresis		—	3	—	V	
V_{OH}	High level output voltage, V_{BIAS} - V_O		—	0.8	1.4	V	I_O = 20 mA
V_{OL}	Low level output voltage, V_O		—	0.3	0.6	V	I_O = 20 mA
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	IR2136	8.0	8.9	9.8	V	
		IR21362	9.6	10.4	11.2	V	
		IR21363	10.7	11.2	11.7	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	IR2136	7.4	8.2	9.0	V	
		IR21362	8.6	9.4	10.2	V	
		IR21363	10.5	11.0	11.5	V	
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage lockout hysteresis	IR2136	0.3	0.7	—	V	
		IR21362	0.5	1.0	—	V	
		IR21363	—	0.2	—	V	
I_{LK}	Offset supply leakage current		—	—	50	µA	$V_{B1,2,3}$=$V_{S1,2,3}$ = 600V
I_{QBS}	Quiescent V_{BS} supply current		20	60	150	µA	V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current		—	1	2	mA	V_{IN} = 0V or 5V
$V_{IN, CLAMP}$	Input clamp voltage (HIN, LIN, ITRIP and EN)		4.9	5.2	5.5	V	I_{IN} =100µA
I_{LIN+}	Input bias current (LOUT = HI)		—	150	400	µA	V_{LIN} = 0V
I_{LIN-}	Input bias current (LOUT = LO)		—	100	250	µA	V_{LIN} = 5V
I_{HIN+}	Input bias current (HOUT = HI)	IR2136(3)	—	150	300	µA	V_{HIN} = 0V
		IR21362	—	—	100	µA	V_{HIN} = 5V
I_{HIN-}	Input bias current (HOUT = LO)	IR2136(3)	—	100	250	µA	V_{HIN} = 5V
		IR21362	—	0	1	µA	V_{HIN} = 0V
I_{ITRIP+}	"high" ITRIP input bias current		—	—	100	µA	V_{ITRIP} = 5V
I_{ITRIP-}	"low" ITRIP input bias current		—	0	1	µA	V_{ITRIP} = 0V

Static Electrical Characteristics cont.

V_{BIAS} (V_{CC}, V_{BS}1,2,3) = 15V unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (H_S1,2,3 and L_S1,2,3). The V_O and I_O parameters are referenced to COM and V_S1,2,3 and are applicable to the respective output leads: $H_{O1,2,3}$ and $L_{O1,2,3}$.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{EN+}	"high" ENABLE input bias current	—	—	100	µA	V_{ENABLE}= 5V
I_{EN-}	"low" ENABLE input bias current	—	0	1		V_{ENABLE} = 0V
I_{RCIN}	RCIN input bias current	—	0	1		V_{RCIN} = 0V or 15V
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	V_O=0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	250	350	—		V_O=15V, PW ≤10 µs
$R_{ON,RCIN}$	RCIN low on resistance	—	60	—	Ω	
$R_{ON,FLT}$	FAULT low on resistance	—	60	—		

Dynamic Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS} = 15V, $V_{S1,2,3}$ = V_{SS} = COM, TA = 25ºC and C_L = 1000 pF unless otherwise specified.

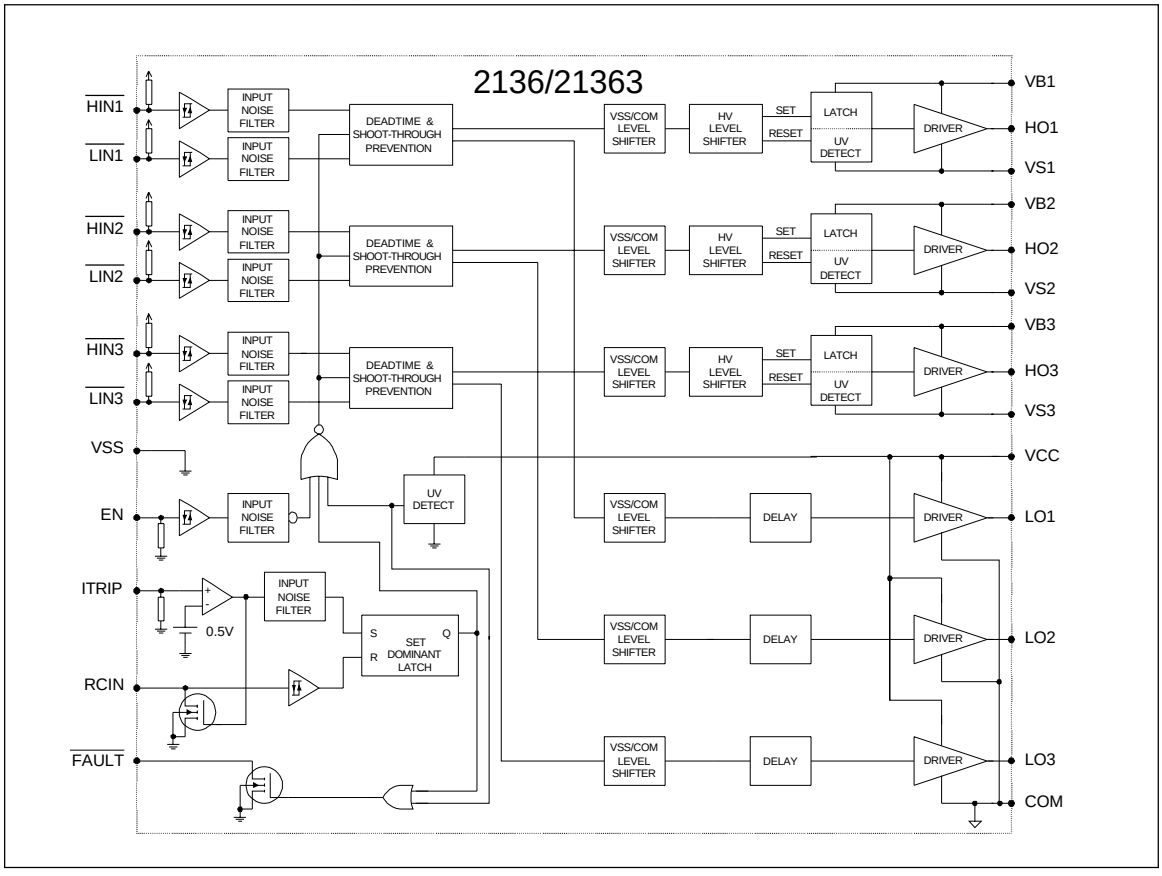
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	400	—	nS	V_{IN} = 0 & 5V $V_{S1,2,3}$ = 0 to 600V
t_{off}	Turn-off propagation delay	—	380	—		
t_r	Turn-on rise time	—	110	—		
t_f	Turn-off fall time	—	50	—		
t_{EN}	ENABLE low to output shutdown propagation delay	—	400	—		V_{IN}, V_{EN} = 0V or 5V
t_{ITRIP}	ITRIP to output shutdown propagation delay	—	700	—		V_{ITRIP} = 5V
t_{bl}	ITRIP blanking time	100	150	—		V_{IN} = 0V or 5V V_{ITRIP} = 5V
t_{FLT}	ITRIP to FAULT propagation delay	—	500	—		V_{IN} = 0V or 5V V_{ITRIP} = 5V
t_{FILIN}	Input filter time (HIN, LIN, EN)	100	200	—		V_{IN} = 0 & 5V
t_{FLTCLR}	FAULT clear time RCIN: R=2meg, C=1nF	—	1.8	—	mS	V_{IN} = 0V or 5V V_{ITRIP} = 0V
DT	Deadtime	—	250	—	nS	V_{IN} = 0 & 5V
MT	Matching delay ON and OFF	—	0	80		
MDT	Matching delay, max (t_{on},t_{off}) - min (t_{on},t_{off}), (ton,toff are applicable to all 3 channels)	—	0	75		External dead time >400nsec
PM	Output pulse width matching, PWin - PWout (fig.2)	—	0	75		

NOTE: For high side PWM, HIN pulse width must be ≥ 1µsec

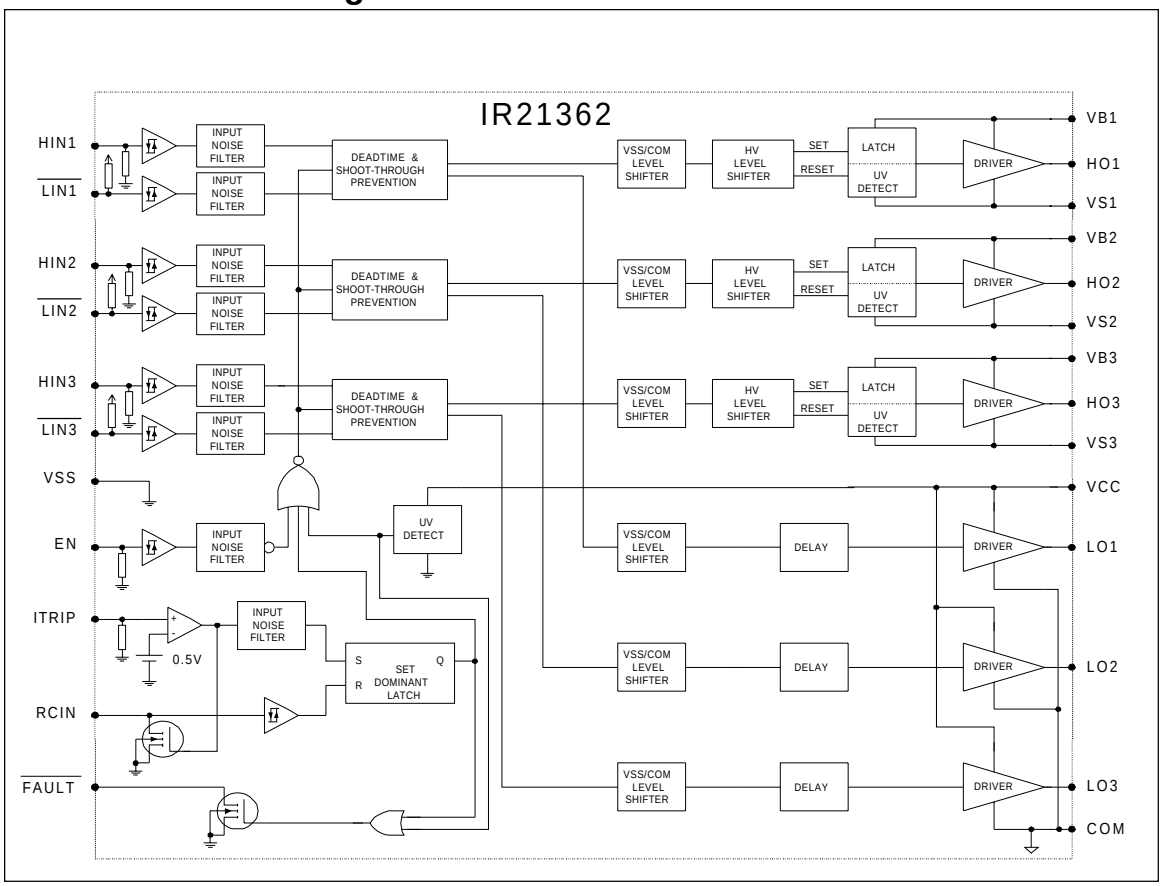
VCC	VBS	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
<UVCC	X	X	X	0 (note 1)	0	0
15V	<UVBS	0V	5V	high imp	LIN1,2,3	0
15V	15V	0V	5V	high imp	LIN1,2,3	HIN1,2,3
15V	15V	>V_{ITRIP}	5V	0 (note 2)	0	0
15V	15V	0V	0V	high imp	0	0

Note: A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.
Note 1: UVCC is not latched, when VCC>UVCC, FAULT returns to high impedance.
Note 2: When ITRIP <V_{ITRIP}, FAULT returns to high-impedance after RCIN pin becomes greater than 8V (@ VCC = 15V)

Functional Block Diagram



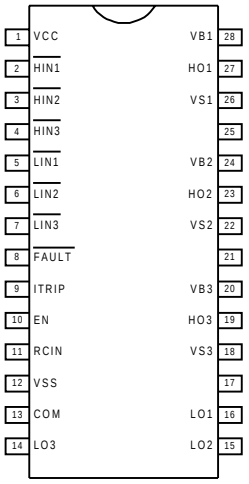
Functional Block Diagram



Lead Definitions

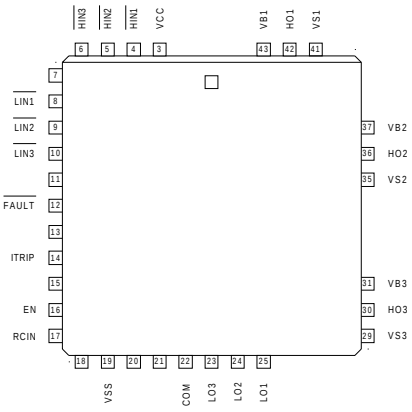
Symbol	Description
V_{CC}	Low side and logic fixed supply
VSS	Logic Ground
$\overline{HIN1,2,3}$ HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase (IR2136/IR21363) Logic inputs for high side gate driver outputs (HO1,2,3), in phase (IR21362)
$\overline{LIN1,2,3}$	Logic inputs for low side gate driver outputs (LO1,2,3), out of phase
FAULT	Indicates over-current (ITRIP) or low-side undervoltage lockout has occured. Negative logic, open-drain output
EN	Logic input to enable I/O functionality. Positive logic, i.e. I/O logic functions when ENABLE is high. No effect on FAULT and not latched
ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time T_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
RCIN	External RC network input used to define FAULT CLEAR delay, T_{FLTCLR}, approximately equal to R*C. When RCIN>8V, the FAULT pin goes back into open-drain high-impedance
COM	Low side gate driver return
V_B1,2,3	High side floating supply
HO1,2,3	High side gate driver outputs
$V_{S1,2,3}$	High voltage floating supply returns
LO1,2,3	Low side gate driver output

Lead Assignments



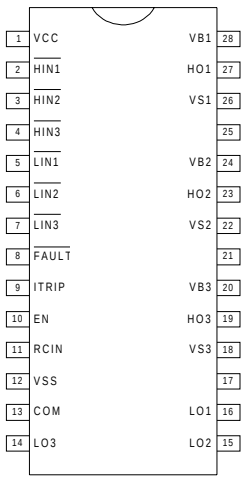
28 Lead PDIP

IR2136/IR21363



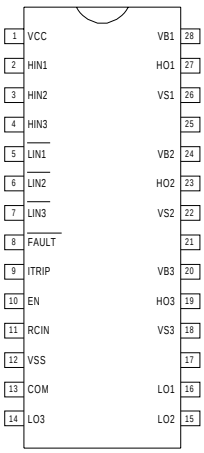
44 Lead PLCC w/o 12 leads

IR2136J/IR21363J



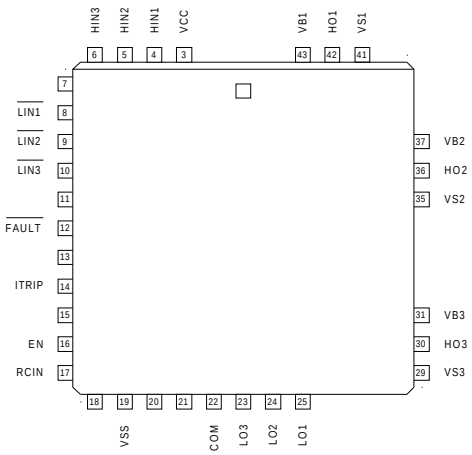
28 lead SOIC (wide body)

IR2136S/IR21363S



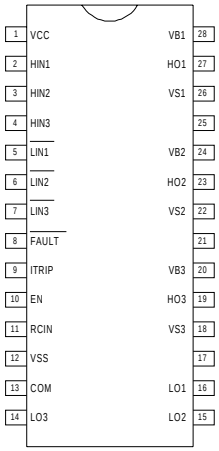
28 Lead PDIP

IR21362



44 Lead PLCC w/o 12 leads

IR21362J



28 lead SOIC (wide body)

IR21362S

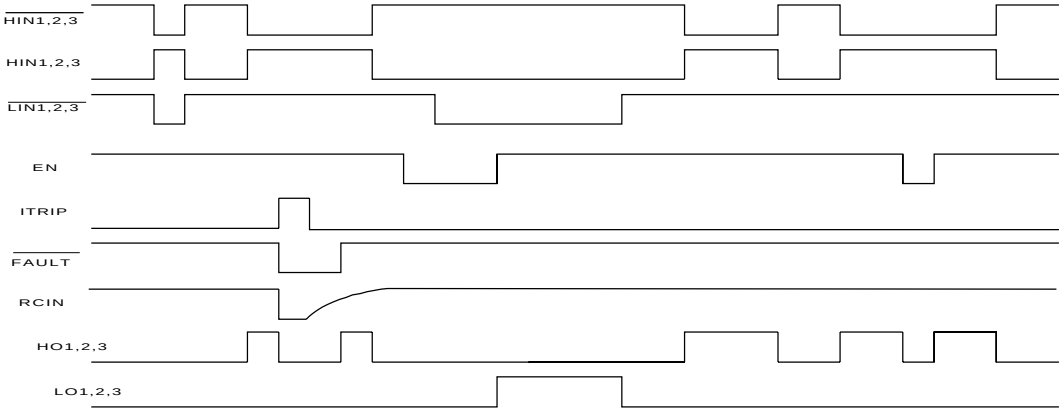


Figure 1. Input/Output Timing Diagram

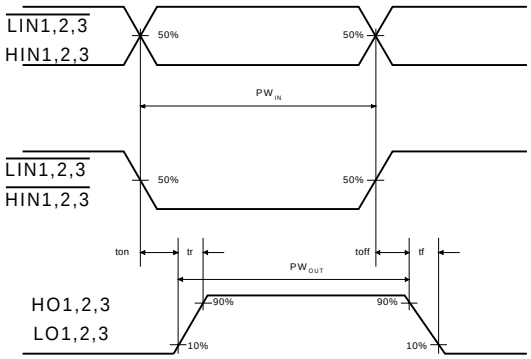


Figure 2. Switching Time Waveforms

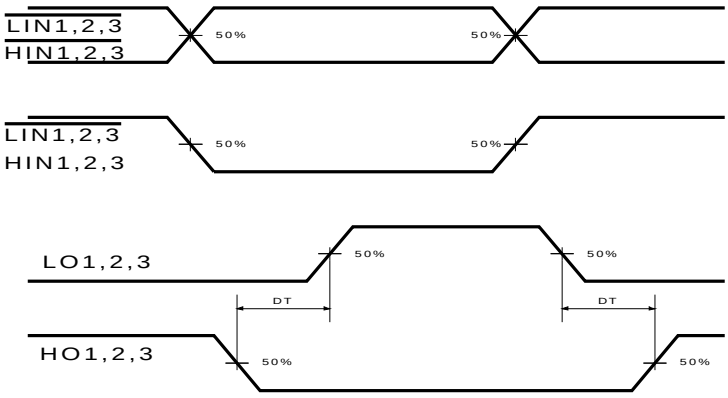


Figure 3. Internal Deadtime Timing Waveforms

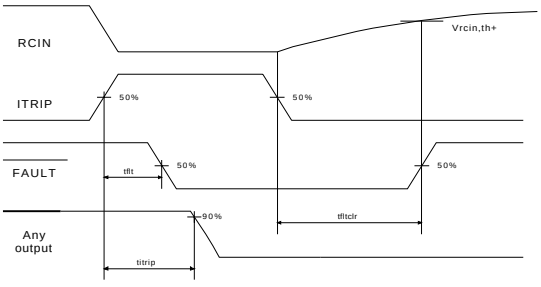


Figure 4. ITRIP/RCIN Timing Waveforms

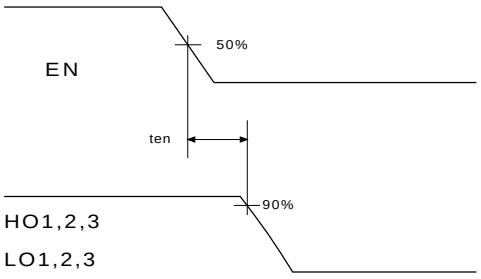
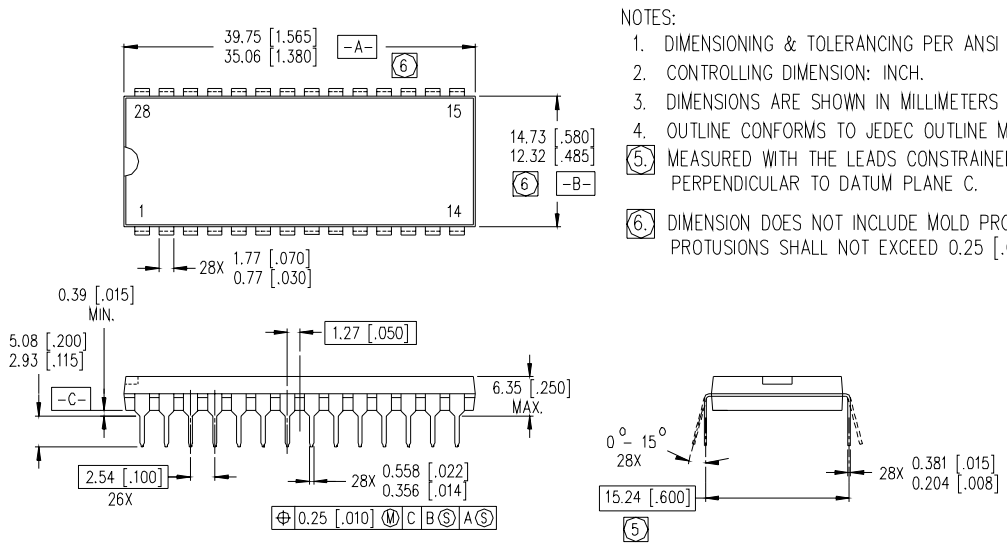


Figure 5. Output Enable Timing Waveform

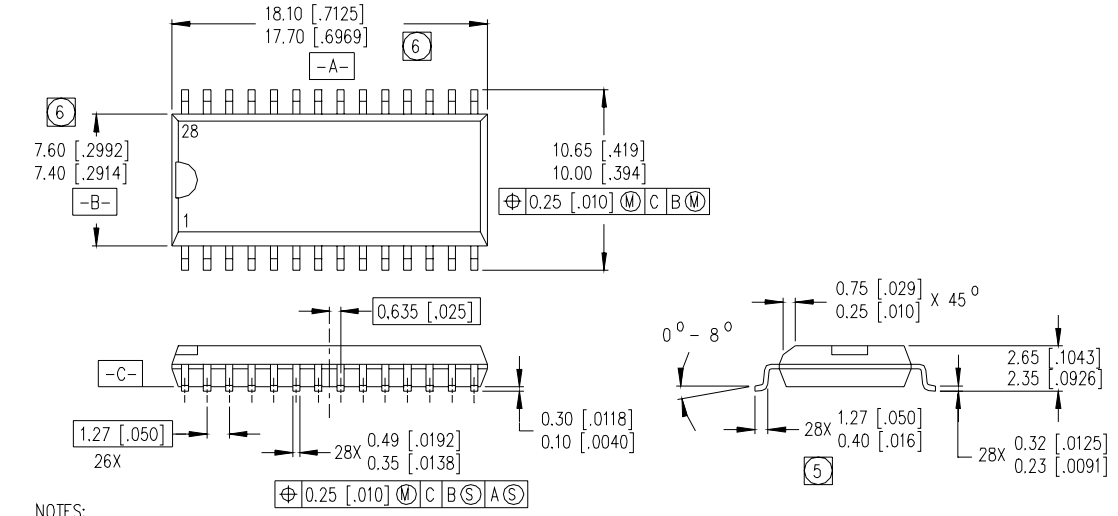
Case outlines



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-011AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

28-Lead PDIP (wide body)

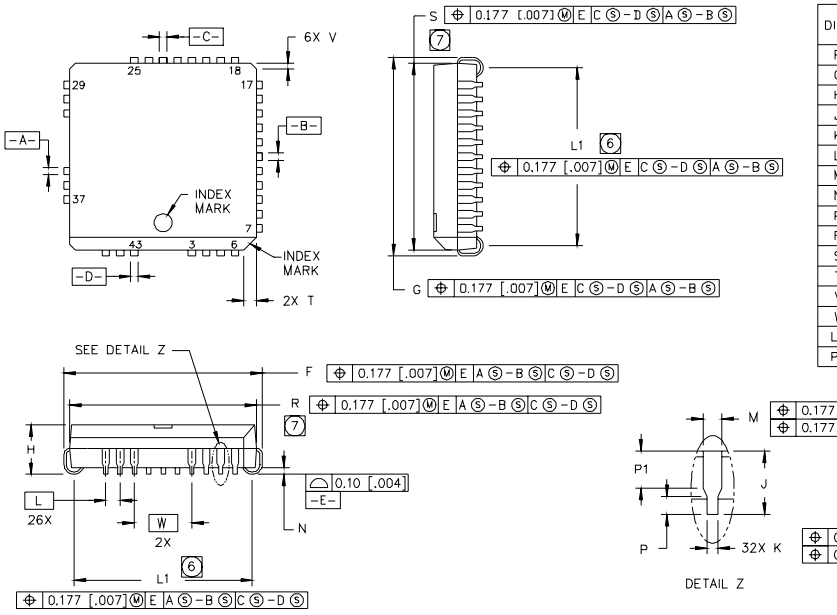
01-6011
01-3024 02 (MS-011AB)



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AE.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

28-Lead SOIC (wide body)

01-6013
01-3040 02 (MS-013AE)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F	17.40	17.65	.685	.695
G	17.40	17.65	.685	.695
H	4.20	4.57	.165	.180
J	2.29	3.04	.090	.120
K	0.33	0.48	.013	.019
L	1.27 BSC		.050 BSC	
M	0.66	0.81	.026	.032
N	0.51	—	.020	—
P	0.64	—	.025	—
R	16.51	16.66	.650	.656
S	16.51	16.66	.650	.656
T	1.07	1.21	.042	.048
V	—	0.50	—	.020
W	5.08 BSC		.200 BSC	
L1	15.50	16.00	.610	.630
P1	1.53	—	.060	—

NOTES

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M-1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS-018AC.
5. DATUMS -A-, -B-, -C-, & -D- ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.
6. TO BE MEASURED AT -E- SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

44-Lead PLCC w/o 12 leads

01-6009 00
01-3004 02(mod.) (MS-018AC)

IR2137/IR2237(J)(Q)

3-PHASE BRIDGE DRIVER

Features

- Floating channel up to +600V or +1200V
- "soft" over-current shutdown turns off all six outputs
- Integrated high side desaturation circuit
- Controlled "soft" turn on for EMI reduction
- Integrated brake IGBT driver
- Three independent low side COM pins
- Separate pull-up/pull-down output drive pins
- Matched delay outputs
- 3.3V logic compatible
- Under voltage lockout with hysteresis band

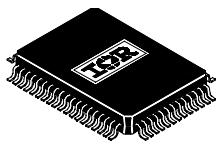
Description

The IR2137/IR2237(J)(Q) are a high voltage, high speed 3-phase IGBT driver best suited for AC motor drive applications. Integrated desaturation logic provides ground fault protection as well as other mode of over current protection. Soft shutdown is initiated in the event of any overcurrent/ground fault conditions, and all six outputs are simultaneously turned off. Output drivers have separate turn on/off pins to facilitate independent gate drive impedance with EMI soft turn on. Optimum matched delays between phases, and between high/low side enables small deadtime, thus improving low speed performance. The brake driver eliminates additional circuits.

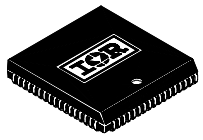
Product Summary

V_{OFFSET}	600V max. or 1200V max.
I_O+/-	220mA / 460mA
V_{OUT}	12.5V - 20V
Brake Io+/-	40mA/80mA
Matched delay	75nsec
Deadtime (typ.)	300 nsec
DESAT Blanking time (typ.)	2.0usec
DESAT input voltage threshold (typ.)	Vt+ = 5.0V

Packages

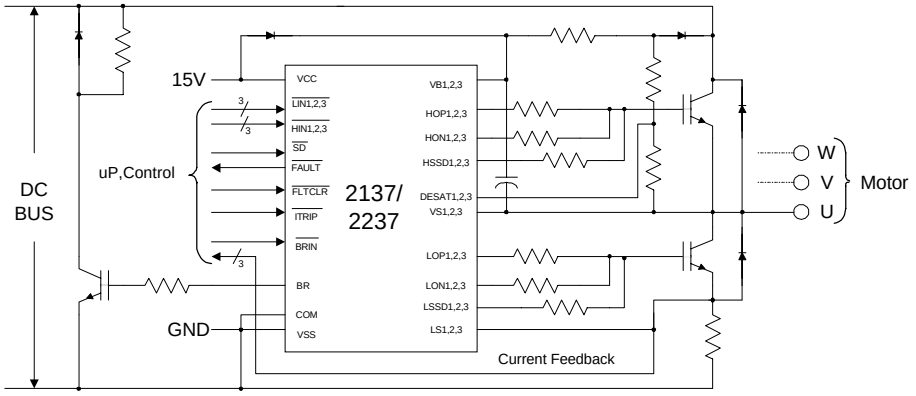


64-Lead MQFP



68-Lead PLCC

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
$V_{S1,2,3}$	High side offset voltage	$V_{B1,2,3}$ -25	$V_{B1,2,3}$ +0.3	V
$V_{B1,2,3}$	High side floating supply voltage (IR2137)	-0.3	625	
	(IR2237)	-0.3	1225	
V_{HO}	High side floating output voltage (HOP, HON, HSSD)	$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Low side and logic fixed supply voltage	-0.3	25	
V_{SS}	Logic ground	V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low side output voltage (LOP, LON, LSSD)	$V_{LS1,2,3}$ -0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage ($\overline{HIN}$, $\overline{LIN}$,$\overline{SD}$, $\overline{ITRIP}$, $\overline{FLTCLR}$, $\overline{BRIN}$)	V_{SS} - 0.3	V_{SS} + 15	
V_{FLT}	FAULT output voltage	V_{SS} - 0.3	V_{CC} + 0.3	
V_{DESAT}	DESAT input voltage	$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{BR}	BRAKE output voltage	- 0.3	V_{CC} + 0.3	
$V_{LS1,2,3}$	Low side output return voltage	V_{CC} - 25	V_{CC} + 0.3	
dV/dt	Allowable offset supply voltage slew rate	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$ (MQFP64)	—	2.0	W
	(PLCC68)		3.0	
Rth_{JA}	Thermal resistance, junction to ambient (MQFP64)	—	60	°C/W
	(PLCC68)	—	40	
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	$V_{S1,2,3}$ + 13	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High side floating supply offset voltage (IR2137)	Note 1	600	
	(IR2237)	Note 1	1200	
$V_{HO1,2,3}$	High side output voltage (HOP, HON, HSSD)	$V_{S1,2,3}$	$V_{S1,2,3}$ + 20	
$V_{LO1,2,3}$	Low side output voltage (LOP, LON, LSSD)	$V_{LS1,2,3}$	V_{CC}	
V_{CC}	Low side and logic fixed supply voltage	12.5	20	
V_{SS}	Logic ground	-5	+5	
V_{IN}	Logic input voltage ($\overline{HIN}$, $\overline{LIN}$,$\overline{SD}$, $\overline{ITRIP}$, $\overline{FLTCLR}$, $\overline{BRIN}$)	V_{SS}	V_{SS} + 5	
V_{BR}	BRAKE output voltage	0	V_{CC}	
V_{FLT}	FAULT output voltage	V_{SS}	V_{CC}	
$V_{LS1,2,3}$	Low side output return voltage	-5.0	+5.0	
V_{DESAT}	DESAT pin input voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of COM -5 to COM +600V/+1200V. Logic state held for V_S of COM -5V to -COM V_{BS}.
Note 2: All input pins are internally clamped with a 5.2V zener diode.

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}1,2,3) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to all six channels (HOP/HON1,2,3 and LOP/LON1,2,3). The V_O and I_O parameters are referenced to V_{LS}1,2,3 and V_S1,2,3 and are applicable to the respective output leads: $H_{O1,2,3}$ and $L_{O1,2,3}$. V_{DESAT} and I_{DESAT} parameters are referenced to $V_{S1,2,3}$

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	10.3	11.4	12.5	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	9.5	10.4	11.3		
V_{CCUVH}	V_{CC} supply undervoltage lockout hysteresis	—	1.0	—		
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	10.3	11.4	12.5		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	9.5	10.4	11.3		
V_{BSUVH}	V_{BS} supply undervoltage lockout hysteresis	—	1.0	—		
I_{LK}	Offset supply leakage current (IR2137)	—	—	50	µA	$V_{B1,2,3} = V_{S1,2,3}$ = 600V
	(IR2237)	—	—	50		$V_{B1,2,3} = V_{S1,2,3}$ = 1200V
I_{QBS}	Quiescent V_{BS} supply current	—	120	200	V	V_{CC} = 12.5 to 20V
I_{QCC}	Quiescent V_{CC} supply current	—	2	6		
V_{IH}	Logic "0" input voltage (OUT=LO) ($\overline{HIN}$,$\overline{LIN}$,$\overline{ITRIP}$,$\overline{SD}$,$\overline{BRIN}$,$\overline{FLTCLR}$)	3.15	—	—		
V_{IL}	Logic "1" input voltage (OUT=HI) ($\overline{HIN}$,$\overline{LIN}$,$\overline{ITRIP}$,$\overline{SD}$,$\overline{BRIN}$,$\overline{FLTCLR}$)	—	—	0.8		
V_{t+}	Logic input positive going threshold ($\overline{HIN}$,$\overline{LIN}$,$\overline{ITRIP}$,$\overline{SD}$,$\overline{BRIN}$,$\overline{FLTCLR}$)	1.6	2.5	3.1		
V_{t-}	Logic input negative going threshold ($\overline{HIN}$,$\overline{LIN}$,$\overline{ITRIP}$,$\overline{SD}$,$\overline{BRIN}$,$\overline{FLTCLR}$)	0.9	1.5	2.4		
V_T	Logic input hysteresis ($\overline{HIN}$,$\overline{LIN}$,$\overline{ITRIP}$,$\overline{SD}$,$\overline{BRIN}$,$\overline{FLTCLR}$)	0.7	1.0	—		
V_{OH}	High level output voltage, V_{BIAS} - V_O (normal switching) HOP, LOP	—	—	100	mV	I_O = 1 mA
V_{OL}	Low level output voltage, V_O (normal switching) HON, LON	—	—	100		
I_{IN+}	Logic "1" input bias current	—	150	—	µA	V_{IN} = 0V
I_{IN-}	Logic "0" input bias current	—	80	—		V_{IN} = 5V
I_{DESAT+}	"high" DESAT input bias current	—	—	15		V_{DESAT} = 15V
I_{DESAT-}	"low" DESAT input bias current	—	—	.1		V_{DESAT} = 0V
I_{O+}	Output high short circuit pulsed current	220	300	—	mA	V_O = 0V, V_{IN} = 0V PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	460	550	—		V_O = 15V, V_{IN} = 5V PW ≤ 10 µs

Static Electrical Characteristics - cont.

V_{BIAS} (V_{CC}, V_{BS}1,2,3) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to all six channels (HOP/HON1,2,3 and LOP/LON1,2,3). The V_O and I_O parameters are referenced to V_{LS}1,2,3 and V_S1,2,3 and are applicable to the respective output leads: $H_{O1,2,3}$ and $L_{O1,2,3}$. V_{DESAT} and I_{DESAT} parameters are referenced to $V_{S1,2,3}$

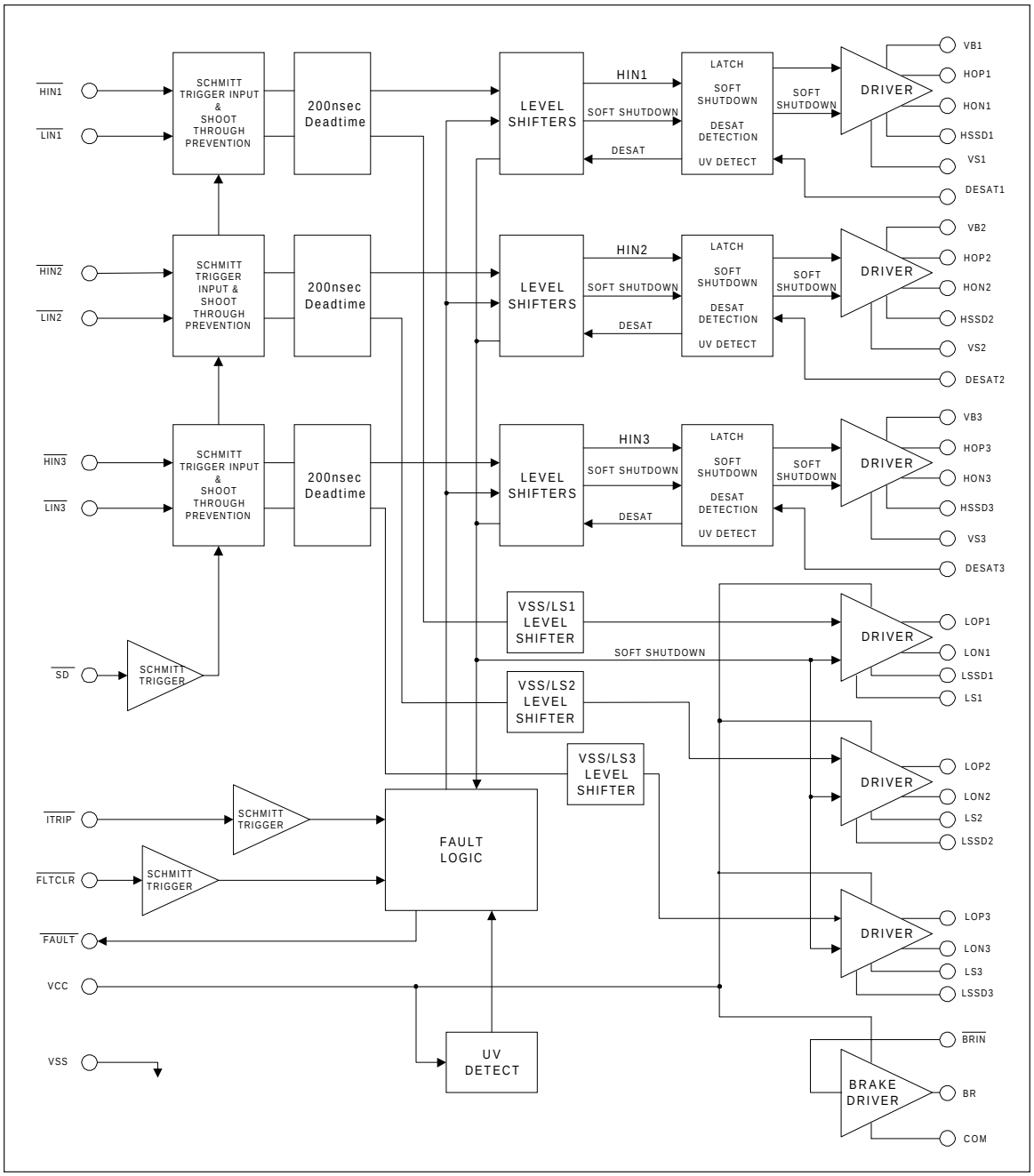
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{OBR+}	BR output high short circuit pulsed current	40	75	—	mA	V_{BR}=0V, V_{BRIN}=0V PW ≤ 10 µs
I_{OBR-}	BR output low short circuit pulsed current	80	120	—		V_{BR}=15V,V_{BRIN}=5V PW ≤ 10 µs
V_{OHB}	BR high level output voltage, V_{BIAS}-V_{BR}	—	—	300	mV	I_{BR} = 1mA
V_{OLB}	BR low level output voltage, V_{BR}	—	—	150		
$R_{ON,SS}$	Soft shutdown on resistance	—	500	—	Ω	ITRIP = 0V
$R_{ON,FLT}$	FAULT low on resistance	—	60	—		
V_{DESAT+}	High DESAT input threshold voltage	—	5.2	—	V	

AC Electrical Characteristics

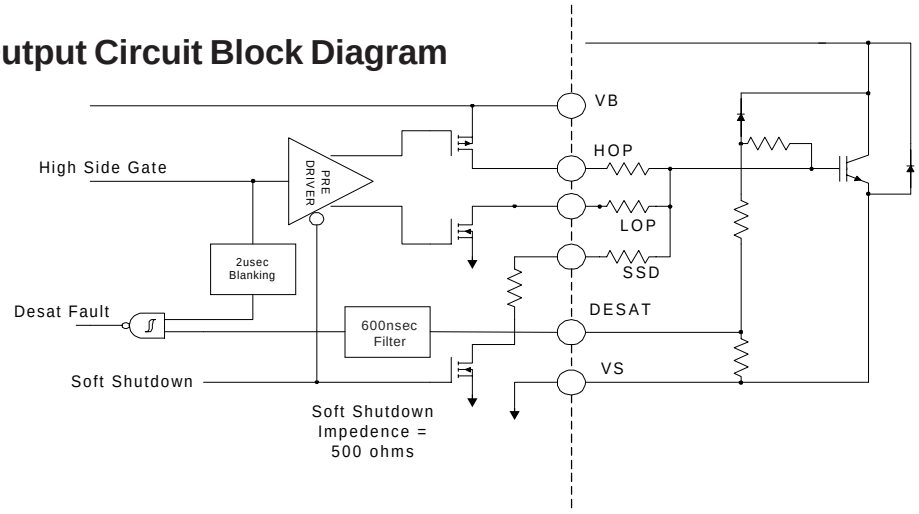
V_{BIAS} (V_{CC}, V_{BS}) = 15V, $V_{S1,2,3}$ = V_{SS}, T_A = 25°C and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation Delay Characteristics						
t_{on}	Turn-on propagation delay	150	400	600	ns	V_{IN} = 0 & 5V $V_{S1,2,3}$ = 0 to 600V or 1200V HOP=HON,LOP=LON Figure 4
t_{off}	Turn-off propagation delay	150	400	600		
t_r	Turn-on rise time	—	115	—		
t_f	Turn-off fall time	—	25	—		
t_{ITRIP}	ITRIP to output shutdown propagation delay	—	1000	1400		V_{IN},V_{DESAT}=0 V_{SD} = 5V
t_{SD}	SD to output shutdown propagation delay	—	1200	1500		V_{IN},V_{DESAT} = 0 V_{ITRIP} = 5V, fig. 7
t_{DESAT1}	DESAT to output shutdown propagation delay at HOPx turn-on	1400	2800	4200		$V_{S1,2,3}$ = 0 to 600V or 1200V V_{HIN} = 0V, V_{SD}, V_{ITRIP} = 5V, V_{DESAT} = 15V, fig. 5
t_{DESAT2}	DESAT to output shutdown propagation delay after blanking	600	1150	1700		
$t_{FLT, IT}$	ITRIP to FAULT output delay	—	800	1100		V_{IN},V_{ITRIP} =0V, V_{SD} = 5V, V_{DESAT}= 0V, fig. 7
t_{FLTCLR}	FLTCLR to FAULT output delay	—	1100	1400		V_{SD} = 5V, V_{DESAT} = 0V, fig. 7
$t_{FLT,DESAT1}$	DESAT to FAULT output delay propagation delay at HOPx turn-on	—	2500	—		$V_{S1,2,3}$ = 0 to 600V or 1200V V_{IN} = 0V, V_{SD}, V_{ITRIP} = 5V, V_{DESAT} = 15V, Figure 5
$t_{FLT,DESAT2}$	DESAT to FAULT output delay propagation delay after blanking	—	850	—		
t_{BL}	DESAT blanking time at turn-on	—	2000	—		
t_{onBR}	BR output turn-on propagation delay	—	120	200		Figure 4
t_{offBR}	BR output turn-off propagation delay	—	85	150		
t_{rBR}	BR output turn-on rise time	—	300	—		
t_{fBR}	BR output turn-off fall time	—	150	—		
Deadtime/Delay Matching Characteristics						
DT	Deadtime	—	300	—	ns	Figure 6
MDT	Matching delay, max (t_{on},t_{off}) - min (t_{on},t_{off}), (ton,toff are applicable to all six channels)	—	0	75		External dead time >400nsec
PM	Output pulse width matching, IPWin - PWoutl (exclude BRIN/BR)	—	0	75		External dead time >400nsec, Fig. 4

Functional Block Diagram



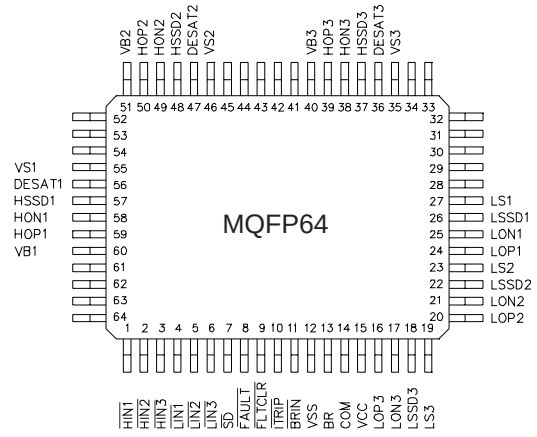
Driver Output Circuit Block Diagram



Lead Definitions

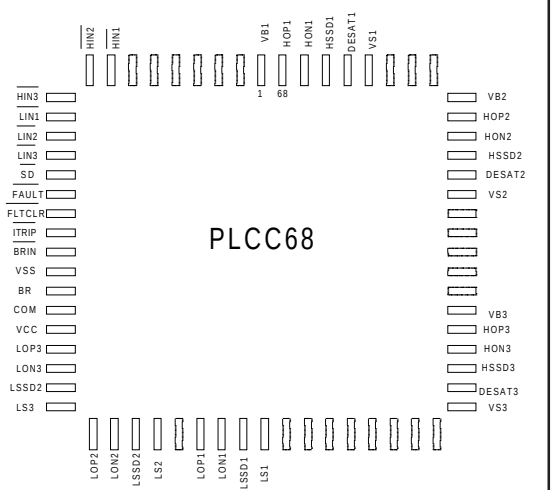
Symbol	Description
V_{CC}	Low side and logic supply voltage
VSS	Logic Ground
$\overline{HIN1,2,3}$	Logic inputs for high side gate driver outputs (HOP1,2,3/HON1,2,3, out of phase)
$\overline{LIN1,2,3}$	Logic inputs for low side gate driver outputs (LOP1,2,3/LON1,2,3, out of phase)
$\overline{SD}$	Logic input for shutdown (hard shutdown, level sensitive signal, negative logic)
$\overline{ITRIP}$	Logic input for overcurrent shutdown (soft shutdown, edge sensitive, negative signal)
$\overline{FLTCLR}$	Logic input for FAULT clear (edge sensitive, negative signal)
$\overline{BRIN}$	Logic input for brake driver, out of phase with BR
$\overline{FAULT}$	Fault output indicates over current and desaturation shutdown (open drain)
BR	Brake driver output
COM	Brake driver return
V_B1,2,3	High side gate drive floating supply
HOP1,2,3	High side driver pull up output
HON1,2,3	High side driver pull down output
HSSD1,2,3	High side soft shutdown output
DESAT1,2,3	IGBT desaturation protection input
$V_{S1,2,3}$	High voltage floating supply return
LOP1,2,3	Low side driver pull up output
LON1,2,3	Low side driver pull down output
LSSD1,2,3	Low side soft shutdown output
LS1,2,3	Low side driver returns

Lead Assignments



64 Lead MQFP

IR2137Q/ IR2237Q



68 Lead PLCC

IR2137J/IR2237J

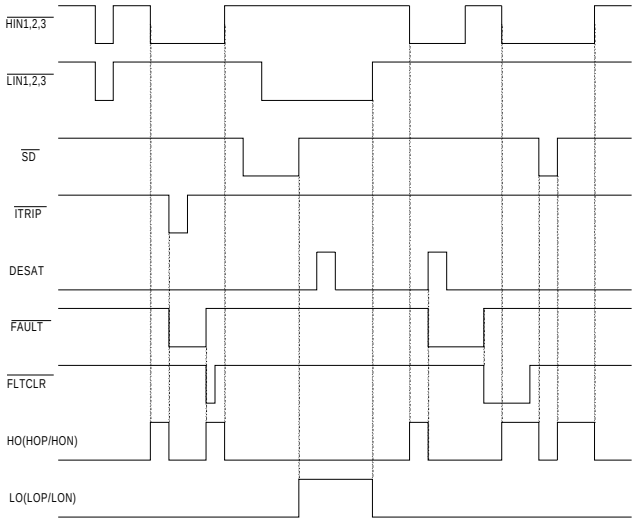


Figure 3. Timing Diagram

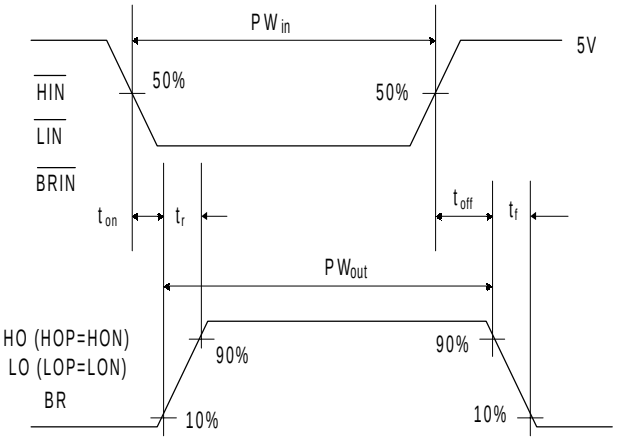


Figure 4. Switching Time Waveforms

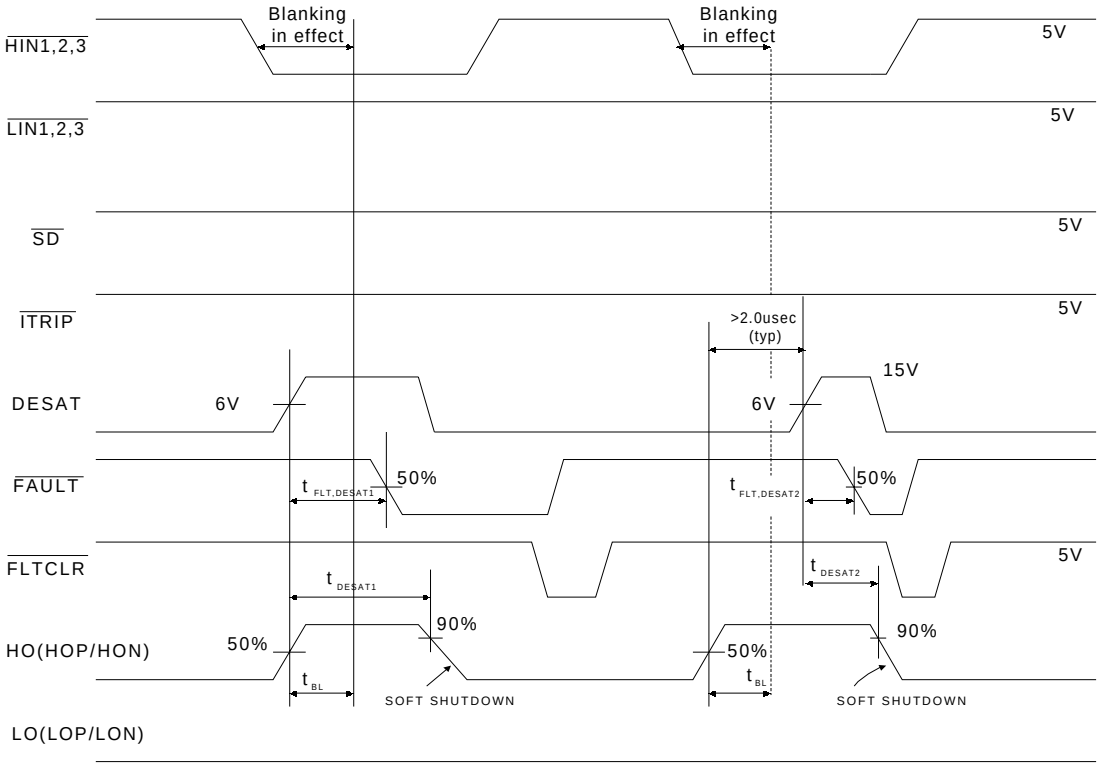


Figure 5. DESAT Timing

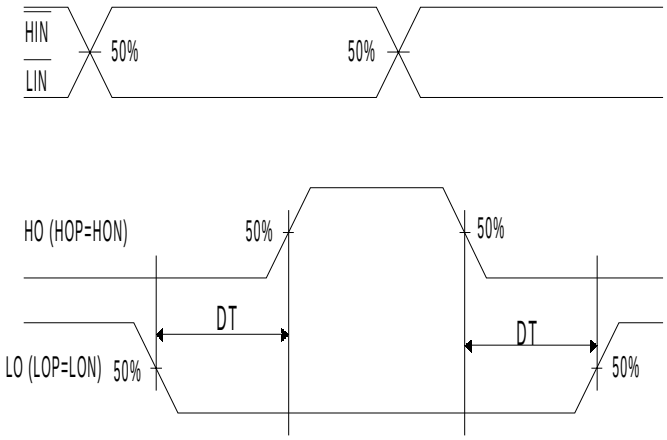


Figure 6. Internal Deadtime Timing

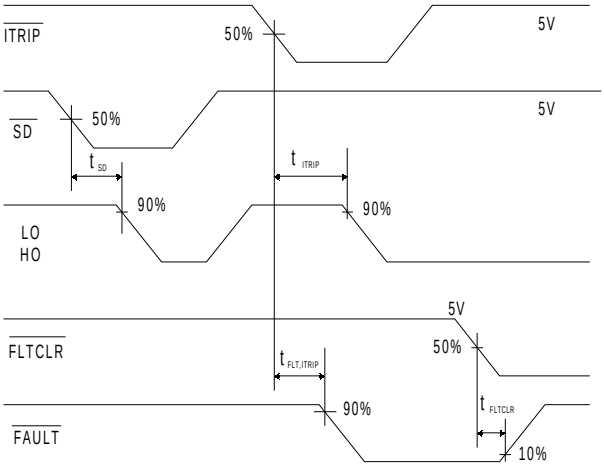
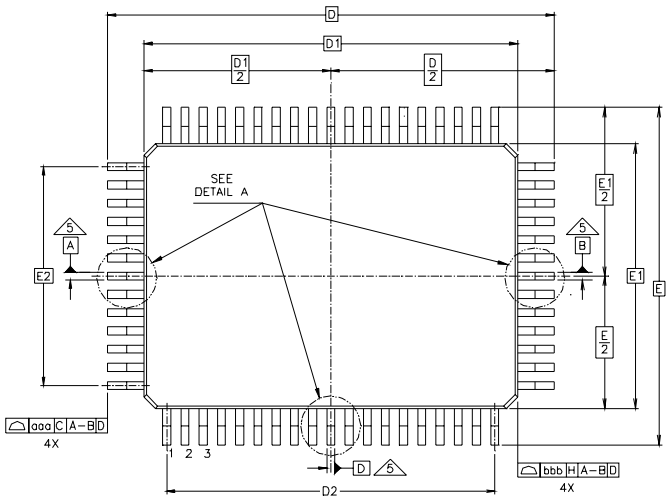


Figure 7. SD, ITRIP Timing

Case outlines



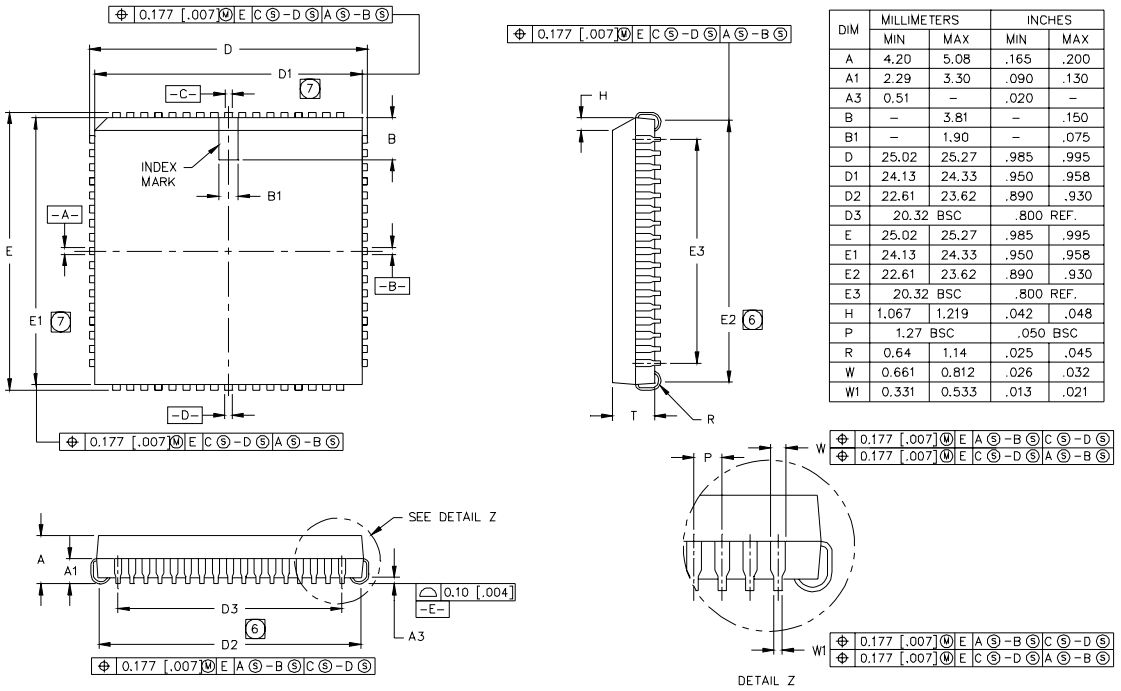
SYMBOL	DIMENSIONS					
	MILLIMETERS			INCHES		
	MS-022GA-2			MS-022GA-2		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.50	2.83	3.15	.098	.111	.124
A1	0.00	0.13	0.25	.000	.005	.010
A2	2.50	2.70	2.90	.098	.106	.114
b	0.35	---	0.50	.014	---	.020
b1	0.35	0.40	0.45	.014	.016	.018
c	0.09	---	0.20	.004	---	.007
c1	0.09	---	0.16	.004	---	.006
D	23.20 BSC			.913 BSC		
D1	20.00 BSC			.787 BSC		
D2	18.00 REF			.709 REF		
E	17.20 BSC			.677 BSC		
E1	14.00 BSC			.551 BSC		
E2	12.00 REF			.472 REF		
e	1.00 BSC			.039 BSC		
L	0.73	0.88	1.03	.029	.035	.040
L1	0.25 BSC			.010 BSC		
α	0°	---	7°	0°	---	7°
aaa	0.25			.010		
bbb	0.20			.008		
ccc	0.20			.008		
ddd	0.10			.004		

NOTES

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
5. DATUM A - B AND D TO BE DETERMINED AT DATUM PLANE H.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. OUTLINE CONFORMS TO JEDEC OUTLINE MS-022GB1.

64-Lead MQFP

01-6054 00
01-2023 01 MS-022GA-2



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.20	5.08	.165	.200
A1	2.29	3.30	.090	.130
A3	0.51	–	.020	–
B	–	3.81	–	.150
B1	–	1.90	–	.075
D	25.02	25.27	.985	.995
D1	24.13	24.33	.950	.958
D2	22.61	23.62	.890	.930
D3	20.32 BSC		.800 REF.	
E	25.02	25.27	.985	.995
E1	24.13	24.33	.950	.958
E2	22.61	23.62	.890	.930
E3	20.32 BSC		.800 REF.	
H	1.067	1.219	.042	.048
P	1.27 BSC		.050 BSC	
R	0.64	1.14	.025	.045
W	0.661	0.812	.026	.032
W1	0.331	0.533	.013	.021

NOTES:

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M–1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS–018AC.
5. DATUMS –A–, –B–, –C–, & –D– ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.

6 TO BE MEASURED AT –E– SEATING PLANE.

7 DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

68-Lead PLCC

01-6055 00
01-3068 01 (MS-018AC)

International
IOR Rectifier

Preliminary Data Sheet No. PD60186-B

IR2170(S)

OVER CURRENT SENSING IC

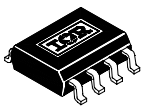
Features

- Floating channel up to +600V
- Monolithic integration
- Overcurrent sensing through shunt resistor
- Low I_{QBS} allows the boot strap power supply
- Independent fast 1µsec overcurrent trip signal
- High common mode noise immunity
- Input overvoltage protection for IGBT short circuit condition
- Open Drain outputs

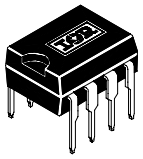
Product Summary

V_{OFFSET}	600Vmax
I_{QBS}	1mA
Overcurrent trip signal delay	1.5usec (typ)
Overcurrent trip level	+/-260mV (typ.)

Packages



8-Lead SOIC

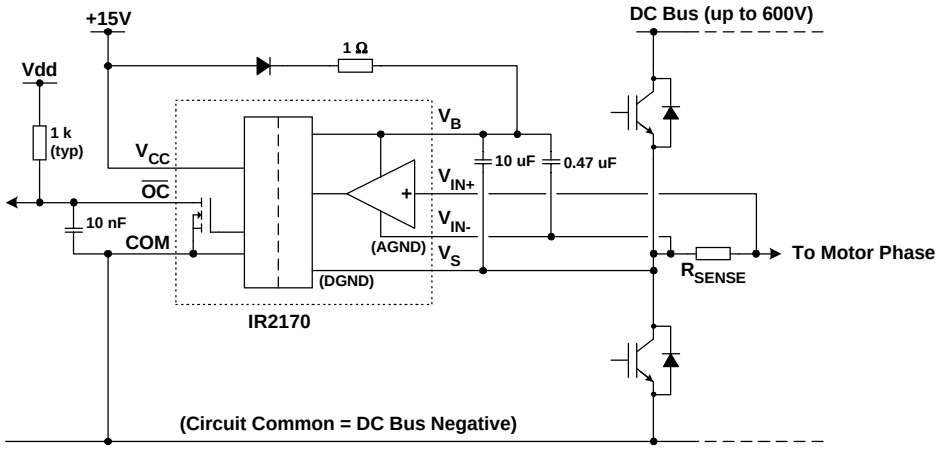


8-Lead PDIP

Description

IR2170(S) is the monolithic over current sensing IC designed for motor drive applications. It senses the motor phase current through an external shunt resistor, detects overcurrent condition, and transfers the signal to the low side. IR's proprietary high voltage isolation technology is implemented to enable the high bandwidth signal processing. The dedicated overcurrent trip ($\overline{OC}$) signal facilitates IGBT short circuit protection. The OC output pulse width can be programmed by the external resistor and capacitor. The open-drain outputs make easy for any interface from 3.3V to 15V.

Typical Application



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	High side offset voltage		-0.3	600	V
V_{BS}	High side floating supply voltage		-0.3	25	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{IN}	Maximum input voltage between V_{IN+} and V_{IN-}		-5	5	
V_{OC}	Overcurrent output voltage		COM -0.3	VCC +0.3	
V_{IN-}	V_{IN-} input voltage (note 1)		V_S -5	V_{B+} 0.3	
dV/dt	Allowable offset voltage slew rate		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	8 lead SOIC	—	.625	W
		8 lead PDIP	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	8 lead SOIC	—	200	°C/W
		8 lead PDIP	—	125	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: Capacitors are required between V_B and Vin-, and between V_B and Vs pins when bootstrap power is used. The external power supply, when used, is required between Vs and Vin-, and between V_B and Vs pins.

Recommended Operating Conditions

The output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	V_S +13.0	V_S +20	V
V_S	High side floating supply offset voltage	note 2	600	
V_{OC}	Overcurrent output voltage	COM	VCC	
V_{CC}	Low side and logic fixed supply voltage	9.5	20	
V_{IN}	Input voltage between V_{IN+} and V_{IN-}	-260	+260	mV
T_A	Ambient temperature	-40	125	°C

Note 2: Logic operation for Vs of -5 to +600V. Logic state held for Vs of -5V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

DC Electrical Characteristics

V_{CC} = V_{BS} = 15V, and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{OC+}	Overcurrent trip positive input voltage	—	260	—	mV	
V_{OC-}	Overcurrent trip negative input voltage	—	-260	—		
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	—	1	2	mA	V_S = 0V
I_{QCC}	Quiescent V_{CC} supply current	—	—	0.5		
I_{OCC}	OC output sink current	10	—	—		V_O = 1V
		1	—	—		V_O = 0.1V

AC Electrical Characteristics cont.

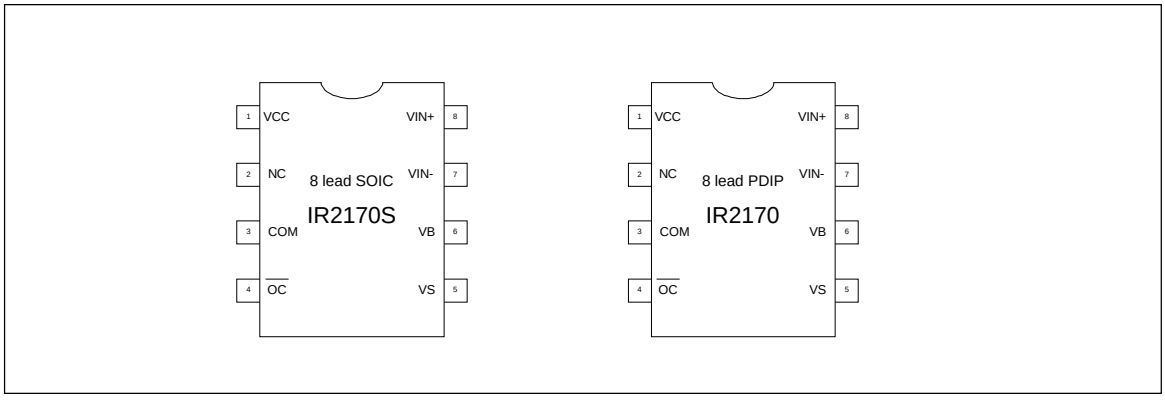
V_{CC} = V_{BS} = 15V, and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Proagation delay characteristics						
tdoc	Propagation delay time of OC	1	1.5	—	µsec	
twoc	Low true pulse width of OC	—	1	—		

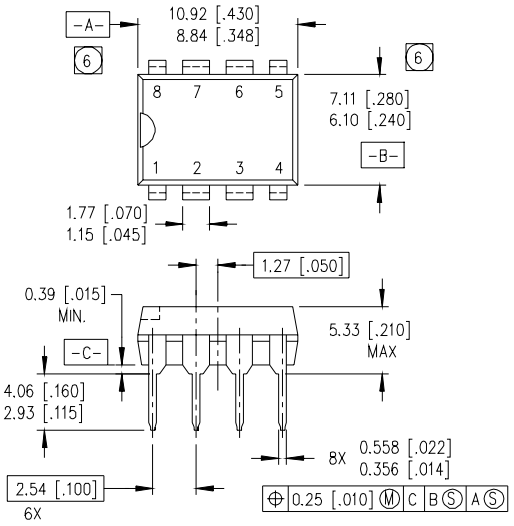
Lead Definitions

Symbol	Description
V_{CC}	Low side and logic supply voltage
COM	Low side logic ground
V_{IN+}	Positive sense input
V_{IN-}	Negative sense input
V_B	High side supply
V_S	High side return
$\overline{OC}$	Overcurrent output (negative logic)
N.C.	No connection

Lead Assignments



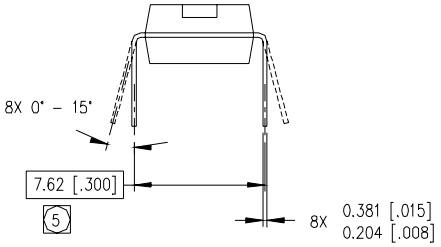
Case outlines



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.

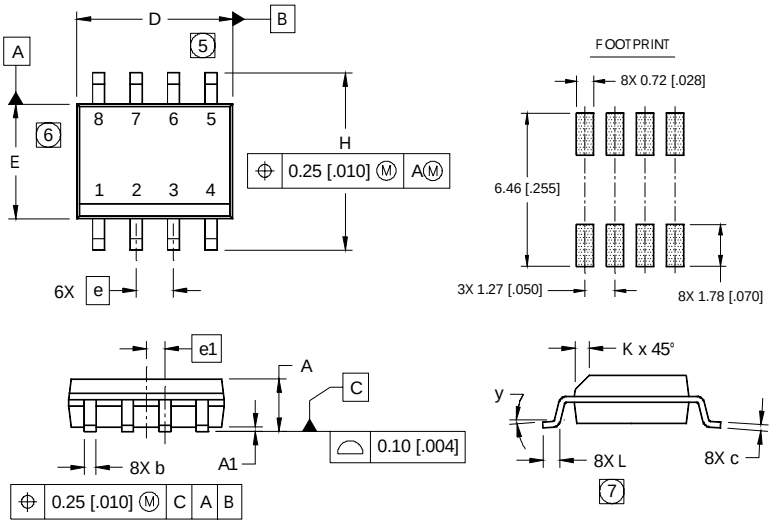
(5) MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8-Lead PDIP

01-6014
01-3003 01 (MS-001AB)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

(5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

(6) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

(7) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8-Lead SOIC

01-6027
01-0021 11 (MS-012AA)

6/28/2001

International
IOR Rectifier

Preliminary Data Sheet No. PD60192

IR2171/IR2172 (S)

LINEAR CURRENT SENSING IC

Features

- Floating channel up to +600V
- Monolithic integration
- Linear current feedback through shunt resistor
- Direct digital PWM output for easy interface
- Low I_{QBS} allows the boot strap power supply
- Independent fast overcurrent trip signal
- High common mode noise immunity
- Input overvoltage protection for IGBT short circuit condition
- Open Drain outputs

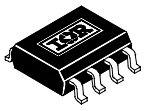
Description

IR2171/IR2172 are monolithic current sensing IC designed for motor drive applications. It senses the motor phase current through an external shunt resistor, converts from analog to digital signal, and transfers the signal to the low side. IR's proprietary high voltage isolation technology is implemented to enable the high bandwidth signal processing. The output format is discrete PWM to eliminate need for the A/D input interface for the IR2172. The dedicated overcurrent trip (OC) signal facilitates IGBT short circuit protection and the OC output pulse can be programmed by the external resistor and capacitor. The open-drain outputs make easy for any interface from 3.3V to 15V.

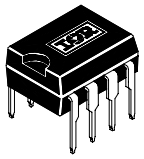
Product Summary

V_{OFFSET}	600Vmax
I_{QBS}	1mA
V_{in}	+/-260mVmax
Gain temp.drift	20ppm/^{o}C (typ.)
f_o	40kHz (typ.)
Overcurrent trip signal delay (IR2172)	1.5usec (typ)
Overcurrent trip level	+/-260mV (typ.)

Packages

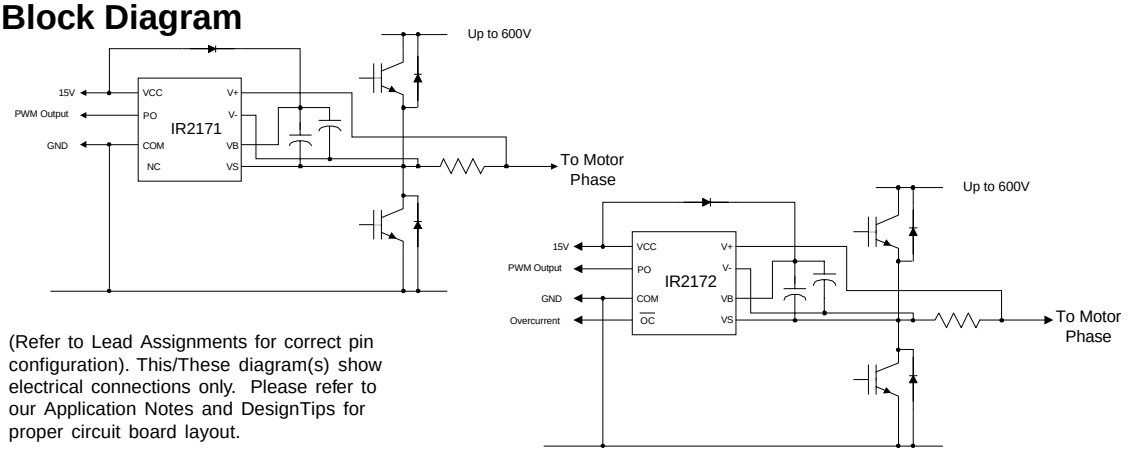


8-Lead SOIC



8-Lead PDIP

Block Diagram



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	High side offset voltage		-0.3	600	V
V_{BS}	High side floating supply voltage		-0.3	25	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{IN}	Maximum input voltage between V_{IN+} and V_{IN-}		-5	5	
V_{PO}	Digital PWM output voltage		COM -0.3	VCC +0.3	
V_{OC}	Overcurrent output voltage (IR2172)		COM -0.3	VCC +0.3	
V_{IN-}	V_{IN-} input voltage (note 1)		V_S -5	V_{B+} 0.3	
dV/dt	Allowable offset voltage slew rate		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	8 lead SOIC	—	.625	W
		8 lead PDIP	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	8 lead SOIC	—	200	°C/W
		8 lead PDIP	—	125	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: Capacitors are required between VB and Vin-, and between VB and Vs pins when bootstrap power is used. The external power supply, when used, is required between Vs and Vin-, and between VB and Vs pins.

Recommended Operating Conditions

The output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	V_S +13.0	V_S +20	V
V_S	High side floating supply offset voltage	note 2	600	
V_{PO}	Digital PWM output voltage	COM	VCC	
V_{OC}	Overcurrent output voltage	COM	VCC	
V_{CC}	Low side and logic fixed supply voltage	9.5	20	
V_{IN}	Input voltage between V_{IN+} and V_{IN-}	-260	+260	mV
T_A	Ambient temperature	-40	125	°C

Note 2: Logic operation for Vs of -5 to +600V. Logic state held for Vs of -5V to -VBS. (Please refer to the Design Tip DT97-3 for more details).

DC Electrical Characteristics

V_{CC} = V_{BS} = 15V, and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IN}	Nominal input voltage range before saturation-260 $\lvert V_{IN+} - V_{IN-} \rvert$	—	260		mV	
V_{OC+}	Overcurrent trip positive input voltage	—	260	—		
V_{OC-}	Overcurrent trip negative input voltage	—	-260	—		
V_{OS}	Input offset voltage	-10	0	10		V_{IN} = 0V (Note 1)
$\Delta V_{OS}/\Delta T_A$	Input offset voltage temperature drift	—	25	—	µV/°C	
G	Gain (duty cycle % per V_{IN})	157	162	167	%/V	max gain error=5% (Note 2)
$\Delta G/\Delta T_A$	Gain temperature drift	—	20	—	ppm/°C	
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	—	1	2	mA	V_S = 0V
I_{QCC}	Quiescent V_{CC} supply current	—	—	0.5		
LIN	Linearity (duty cycle deviation from ideal linearity curve)	—	0.5	1	%	
$\Delta V_{LIN}/\Delta T_A$	Linearity temperature drift	—	.005	—	%/°C	
I_{OPO}	Digital PWM output sink current	20	—	—	mA	V_O = 1V
		2	—	—		V_O = 0.1V
I_{OCC}	OC output sink current (IR2172)	10	—	—		V_O = 1V
		1	—	—		V_O = 0.1V

Note 1: ±10mV offset represents ±1.5% duty cycle fluctuation
Note 2: Gain = (full range of duty cycle in %) / (full input voltage range).

AC Electrical Characteristics

V_{CC} = V_{BS} = 15V, and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation delay characteristics						
fo	Carrier frequency output	—	40	—	kHz	figure 1
$\Delta f/\Delta T_A$	Temperature drift of carrier frequency	—	500	—	ppm/°C	V_{IN} = 0 & 5V
Dmin	Minimum duty	—	7	—	%	V_{IN}+=-260mV,V_{IN}-=0V
Dmax	Maximum duty	—	93	—	%	V_{IN}+=+260mV,V_{IN}-=0V
BW	fo bandwidth		15		kHz	V_{IN}+ = 100mVpk -pk sine wave, gain=-3dB
PHS	Phase shift at 1kHz		-10		°	V_{IN}+ =100mVpk-pk sine wave

AC Electrical Characteristics cont.

V_{CC} = V_{BS} = 15V, unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Proagation delay characteristics						
tdoc	Propagation delay time of OC (IR2172)	1	1.5	—	µsec	
twoc	Low true pulse width of OC (IR2172)	—	1	—		

Timing Waveforms

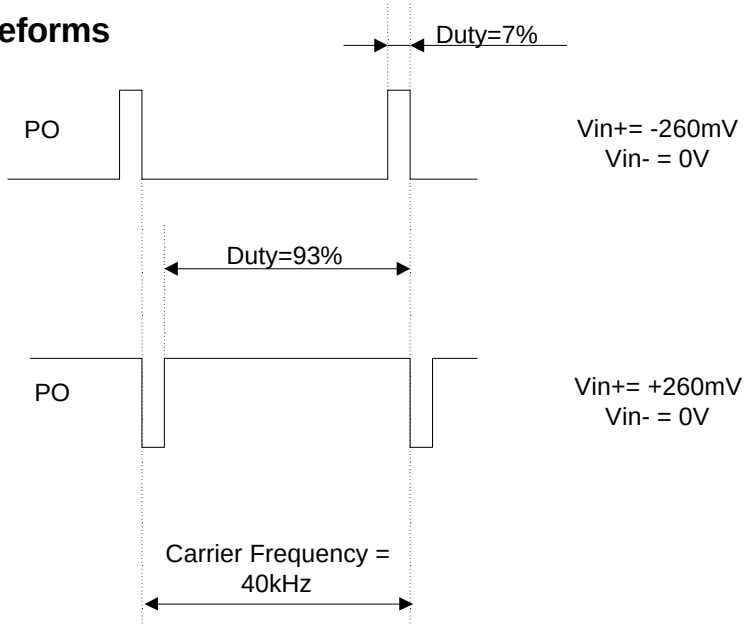


Figure 1 Output waveform

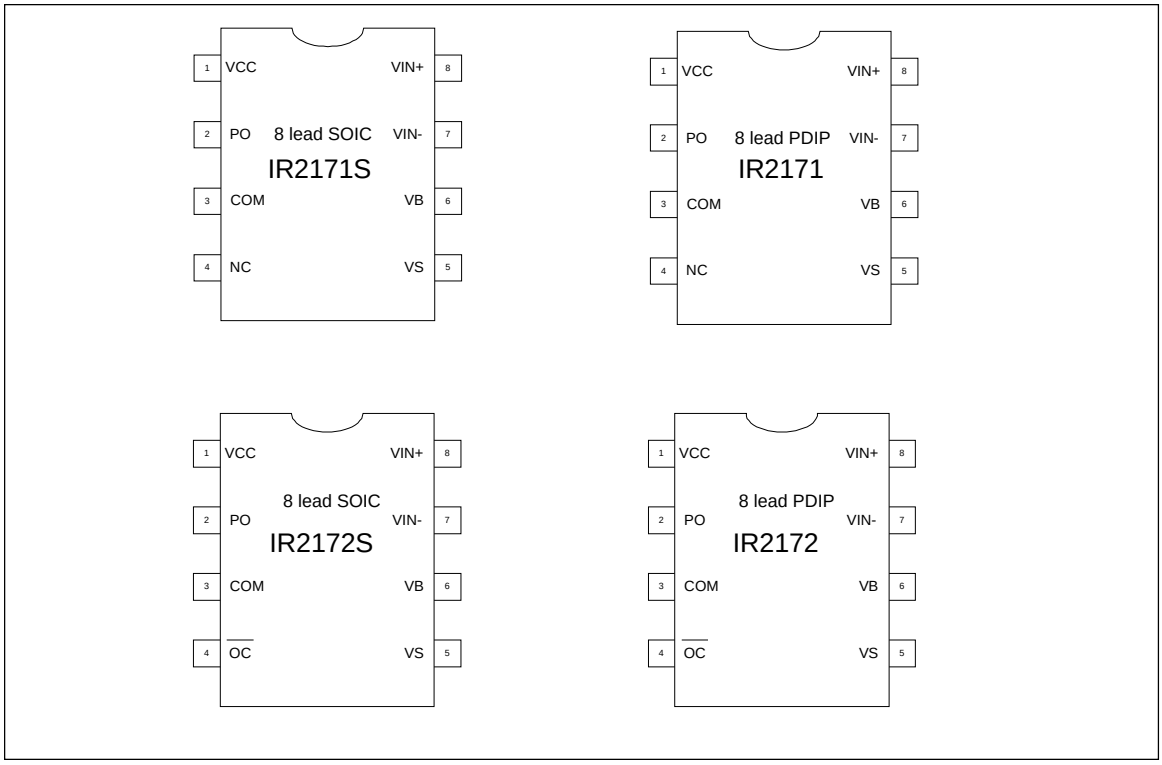
Application Hint:

Temperature drift of the output carrier frequency can be cancelled by measuring both a PWM period and the on-time of PWM (Duty) at the same time. Since both periods vary in the same direction, computing the ratio between these values at each PWM period gives consistent measurement of the current feedback over the temperature drift.

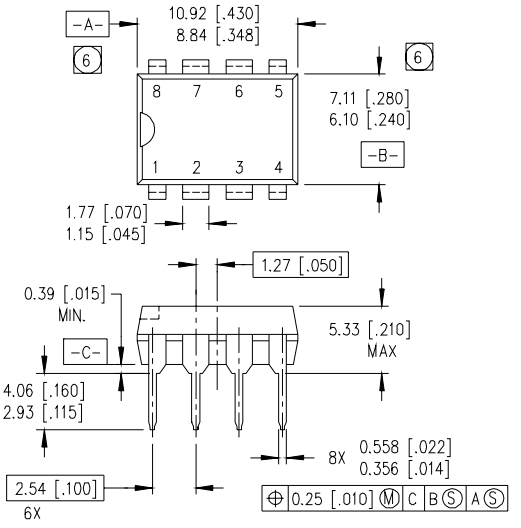
Lead Definitions

Symbol	Description
V_{CC}	Low side and logic supply voltage
COM	Low side logic ground
V_{IN+}	Positive sense input
V_{IN-}	Negative sense input
V_B	High side supply
V_S	High side return
PO	Digital PWM output
$\overline{OC}$	Overcurrent output (negative logic) (IR2172 only)
N.C.	No connection

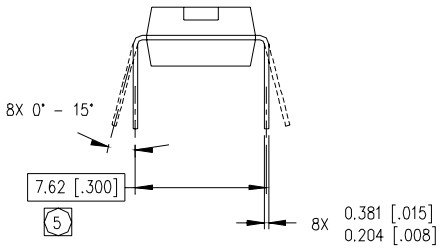
Lead Assignment



Case outlines

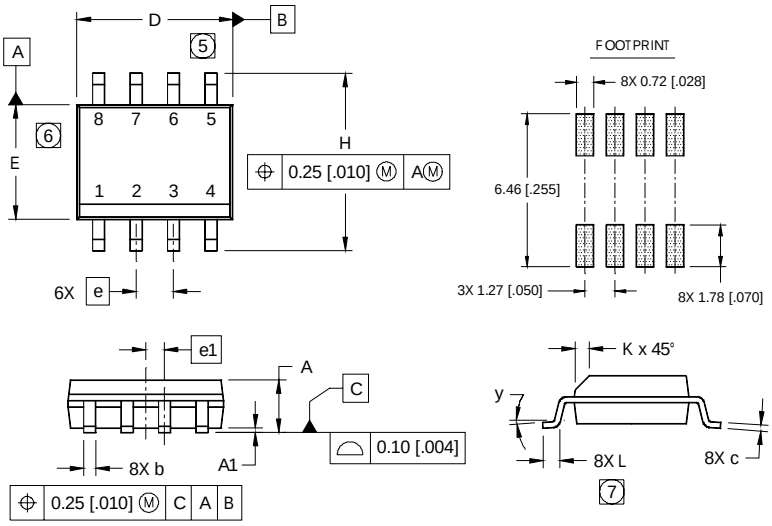


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8 Lead PDIP

01-6014
01-3003 01 (MS-001AB)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

01-6027
01-0021 11 (MS-012AA)

Data Sheet No. PD60172-E

International
IOR Rectifier

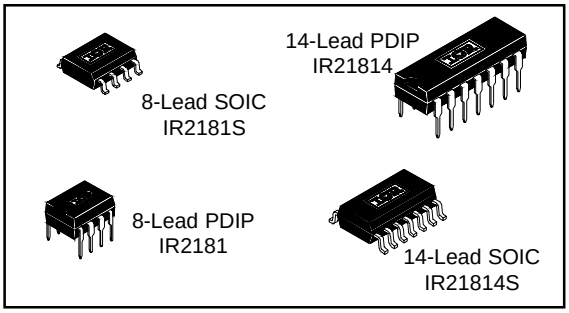
IR2181(4)(S)

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V and 5V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability 1.4A/1.8A

Packages



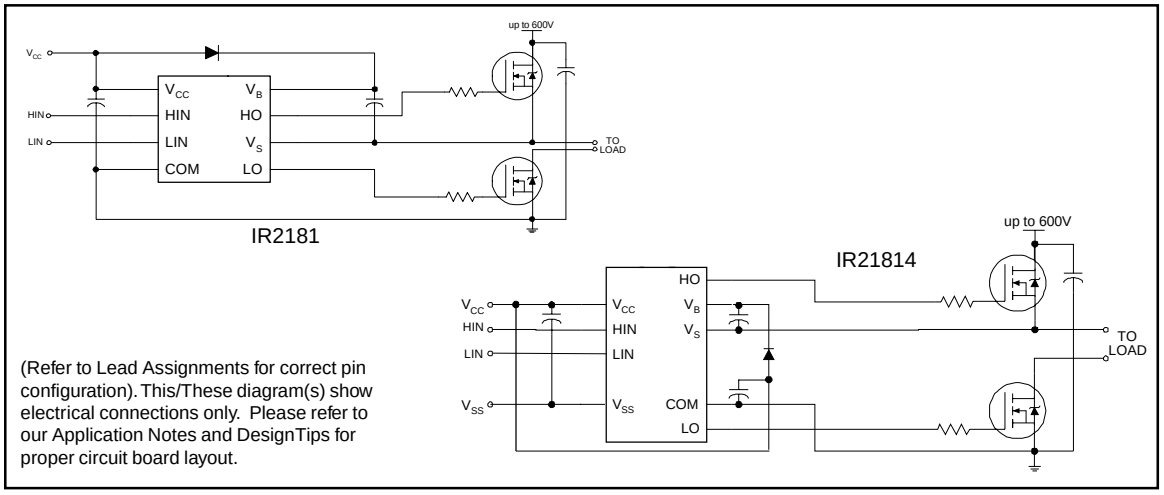
Description

The IR2181(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

IR2181/IR2183/IR2184 Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Dead-Time	Ground Pins	Ton/Toff
2181	HIN/LIN	no	none	COM	180/220 ns
21814				VSS/COM	
2183	HIN/$\overline{\text{LIN}}$	yes	Internal 500ns	COM	180/220 ns
21834			Program 0.4 ~ 5 us	VSS/COM	
2184	IN/$\overline{\text{SD}}$	yes	Internal 500ns	COM	680/270 ns
21844			Program 0.4 ~ 5 us	VSS/COM	

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN - IR2181/IR21814)		V_{SS} - 0.3	V_{SS} + 10	
V_{SS}	Logic ground (IR21814 only)		V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8-lead PDIP)	—	1.0	W
		(8-lead SOIC)	—	0.625	
		(14-lead PDIP)	—	1.6	
		(14-lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8-lead PDIP)	—	125	°C/W
		(8-lead SOIC)	—	200	
		(14-lead PDIP)	—	75	
		(14-lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
VB	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN - IR2181/IR21814)	V_{SS}	V_{SS} + 5	
V_{SS}	Logic ground (IR21814/IR21824 only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).
Note 2: HIN and LIN pins are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C.

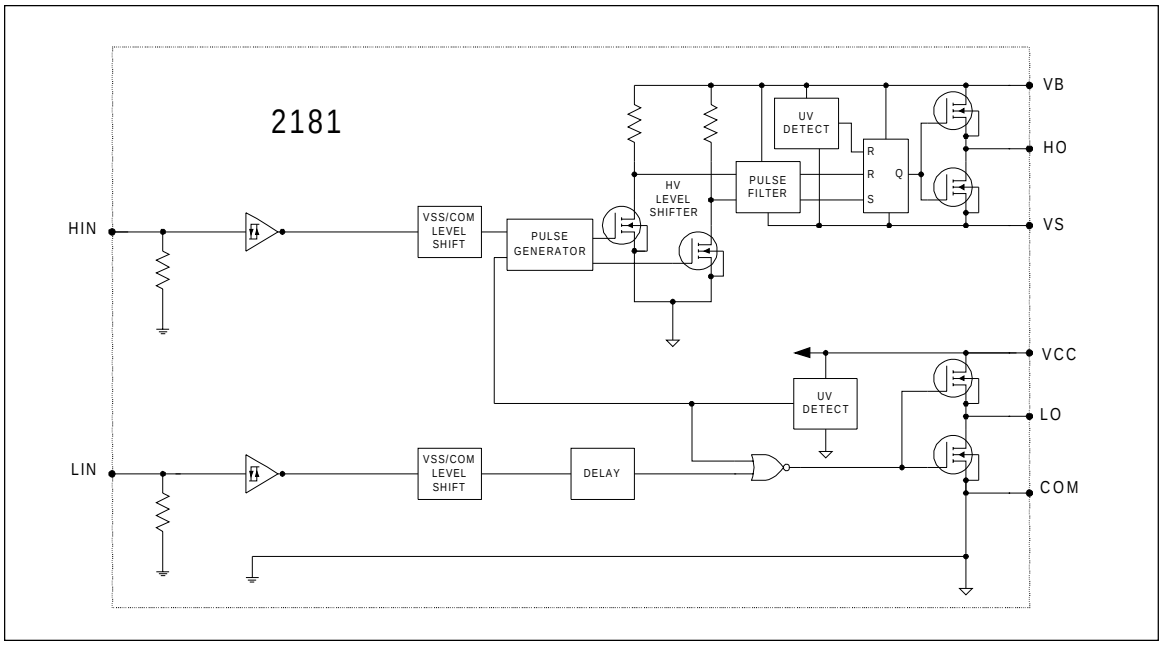
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	180	270	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	220	330		V_S = 0V or 600V
MT	Delay matching, HS & LS turn-on/off	—	0	35		
t_r	Turn-on rise time	—	40	60		V_S = 0V
t_f	Turn-off fall time	—	20	35		V_S = 0V

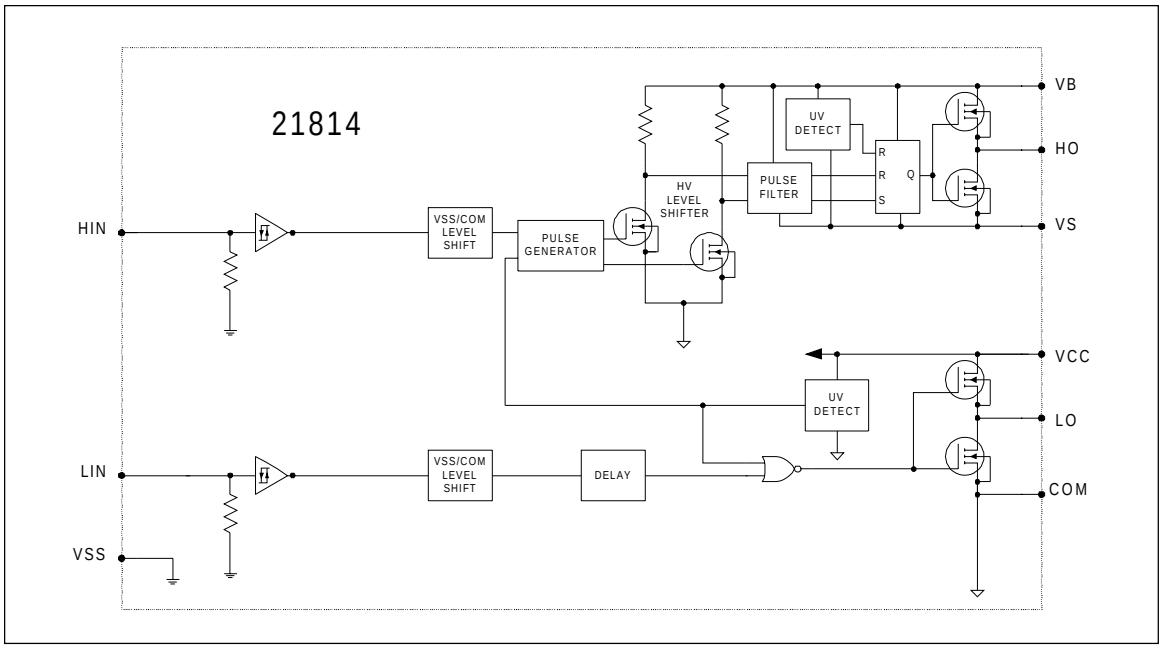
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads HIN and LIN. The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” input voltage (IR2181/IR21814)	2.7	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic “0” input voltage (IR2181/IR21814)	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1.2		I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	0.1		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	50	120	240		V_{IN} = 0V or 5V
I_{IN+}	Logic “1” input bias current	—	25	60		V_{IN} = 5V
I_{IN-}	Logic “0” input bias current	—	—	1.0		V_{IN} = 0V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	1.4	1.9	—	A	V_O = 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	1.8	2.3	—		V_O = 15V, PW ≤ 10 µs

Functional Block Diagrams

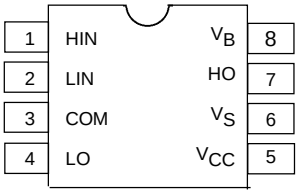




Lead Definitions

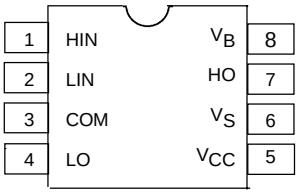
Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase (IR2181/IR21814)
LIN	Logic input for low side gate driver output (LO), in phase (IR2181/IR21814)
VSS	Logic Ground (IR21814 only)
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



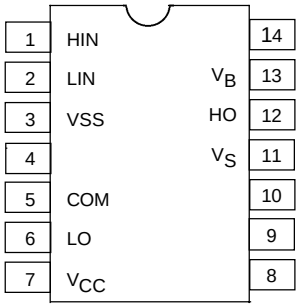
8-Lead PDIP

IR2181



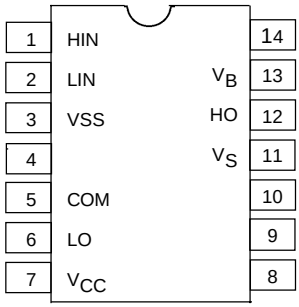
8-Lead SOIC

IR2181S



14-Lead PDIP

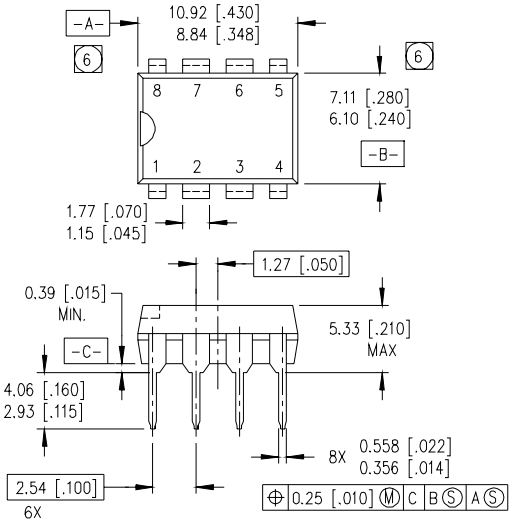
IR21814



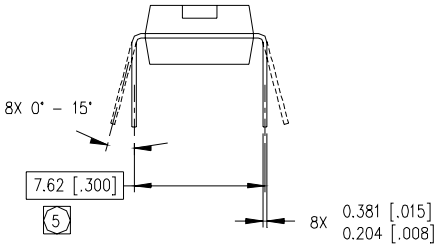
14-Lead SOIC

IR21814S

Case outlines

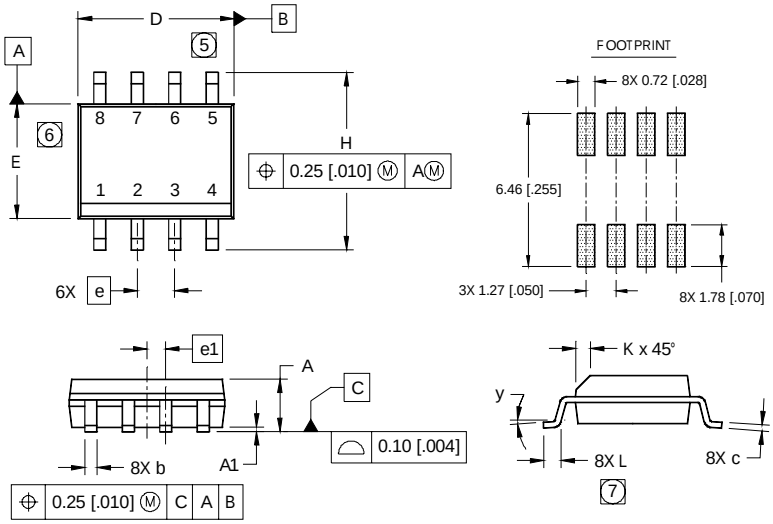


NOTES:
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2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
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6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8-Lead PDIP

01-6014
01-3003 01 (MS-001AB)



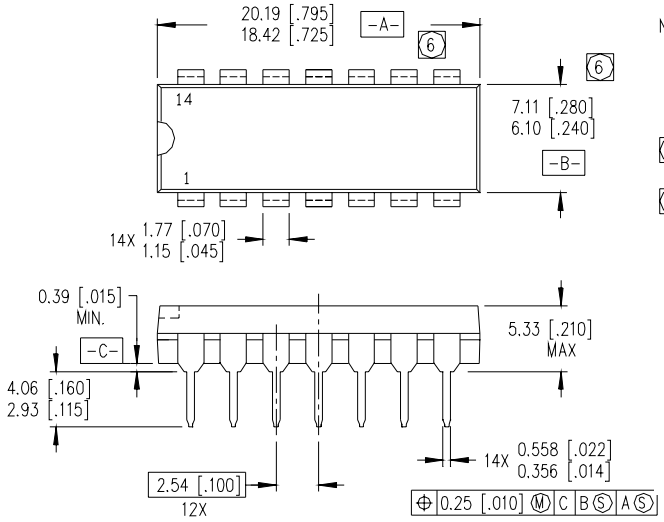
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

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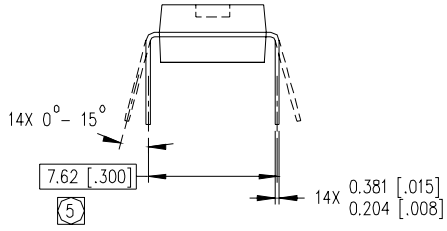
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8-Lead SOIC

01-6027
01-0021 11 (MS-012AA)

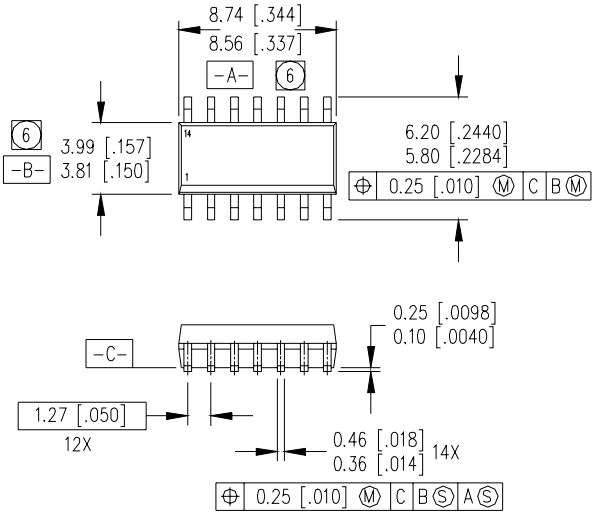


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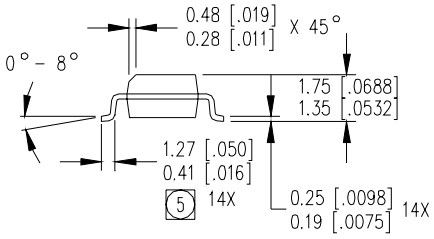


14-Lead PDIP

01-6010
01-3002 03 (MS-001AC)



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14-Lead SOIC (narrow body)

01-6019
01-3063 00 (MS-012AB)

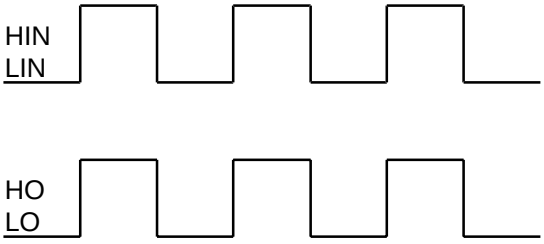


Figure 1. Input/Output Timing Diagram

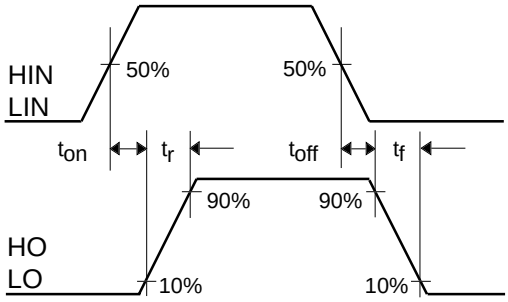


Figure 2. Switching Time Waveform Definitions

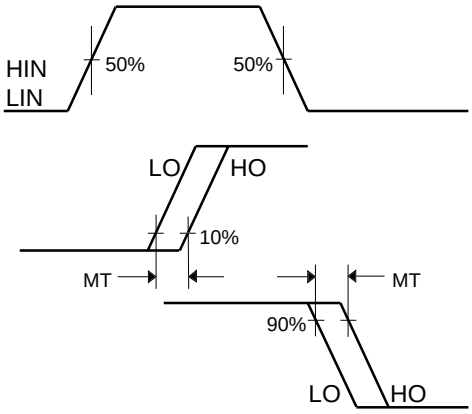


Figure 3. Delay Matching Waveform Definitions

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

Data and specifications subject to change without notice. 7/23/2001

Data Sheet No. PD60173-E

International
IOR Rectifier

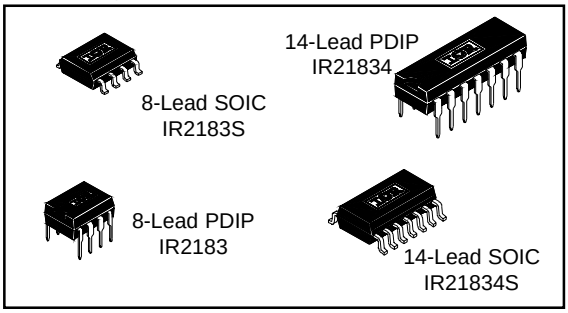
IR2183(4) (S)

HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
  - Fully operational to +600V
  - Tolerant to negative transient voltage
  - dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V and 5V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability 1.4A/1.8A

Packages



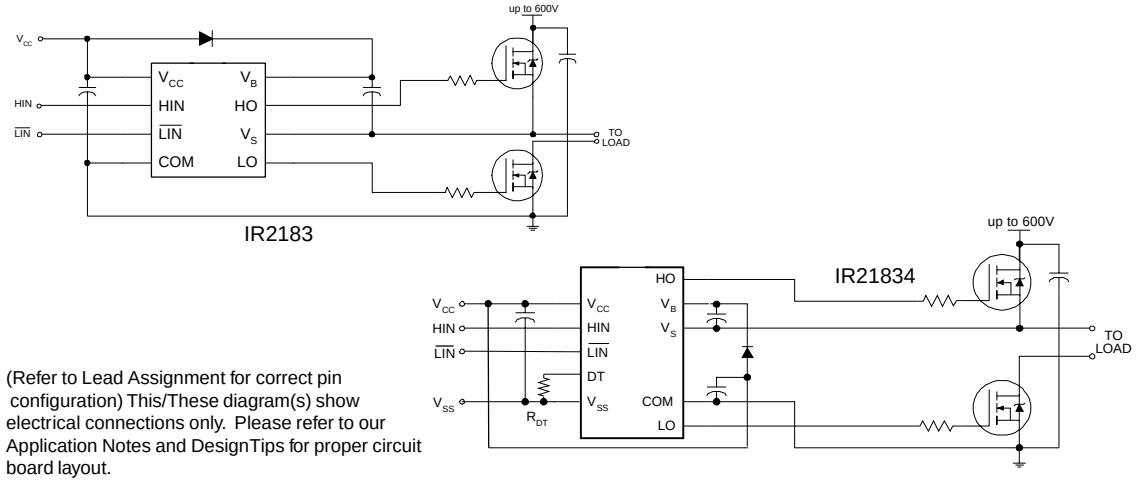
Description

The IR2183(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

IR2181/IR2183/IR2184 Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Dead-Time	Ground Pins	Ton/Toff
2181	HIN/LIN	no	none	COM	180/220 ns
21814				VSS/COM	
2183	HIN/$\overline{\text{LIN}}$	yes	Internal 500ns	COM	180/220 ns
21834			Program 0.4 ~ 5 us	VSS/COM	
2184	IN/$\overline{\text{SD}}$	yes	Internal 500ns	COM	680/270 ns
21844			Program 0.4 ~ 5 us	VSS/COM	

Typical Connection



(Refer to Lead Assignment for correct pin configuration) This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
DT	Programmable dead-time pin voltage (IR21834 only)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)		V_{SS} - 0.3	V_{SS} + 10	
V_{SS}	Logic ground (IR21834 only)		V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8-lead PDIP)	—	1.0	W
		(8-lead SOIC)	—	0.625	
		(14-lead PDIP)	—	1.6	
		(14-lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8-lead PDIP)	—	125	°C/W
		(8-lead SOIC)	—	200	
		(14-lead PDIP)	—	75	
		(14-lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
VB	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)	V_{SS}	V_{SS} + 5	
DT	Programmable dead-time pin voltage (IR21834 only)	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21834 only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Note 2: HIN and $\overline{LIN}$ pins are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C, DT = VSS unless otherwise specified.

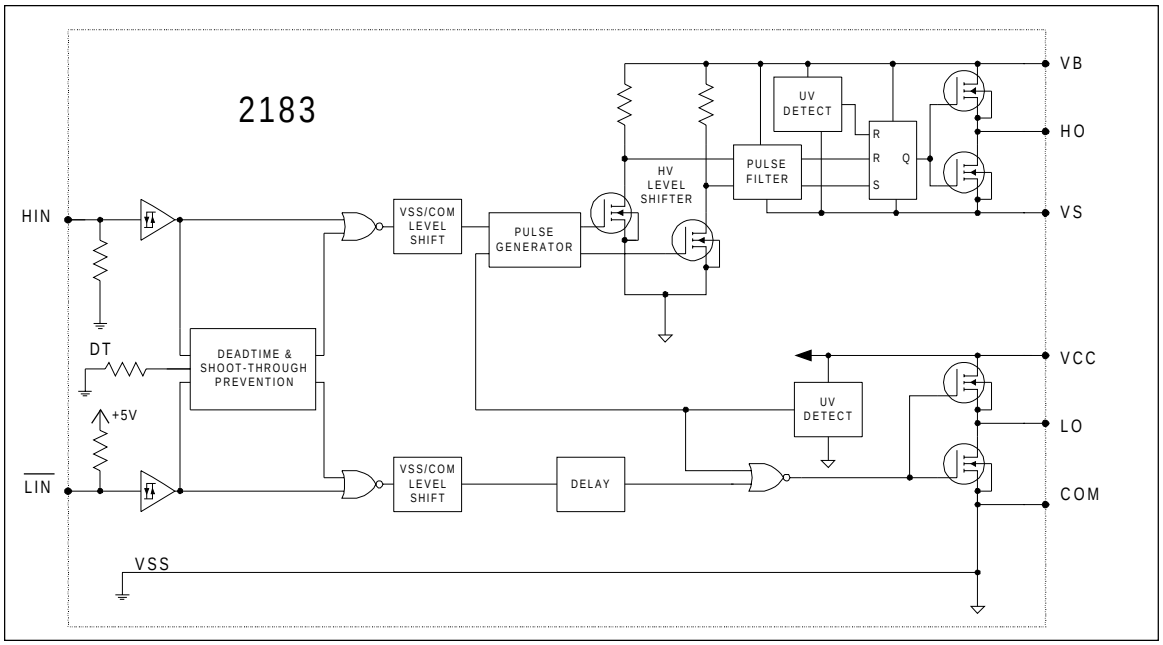
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	180	270	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	220	330		V_S = 0V or 600V
MT	Delay matching $\lvert t_{on} - t_{off} \rvert$	—	0	35		
t_r	Turn-on rise time	—	40	60		V_S = 0V
t_f	Turn-off fall time	—	20	35		V_S = 0V
DT	Deadtime: LO turn-off to HO turn-on(DT_{LO-HO}) &	280	400	520		RDT= 0
	HO turn-off to LO turn-on (DT_{HO-LO})	4	5	6	µsec	RDT = 200k (IR21834)
MDT	Deadtime matching = $\lvert DT_{LO-HO} - DT_{HO-LO} \rvert$	—	0	50	nsec	RDT=0
		—	0	600		RDT = 200k (IR21834)

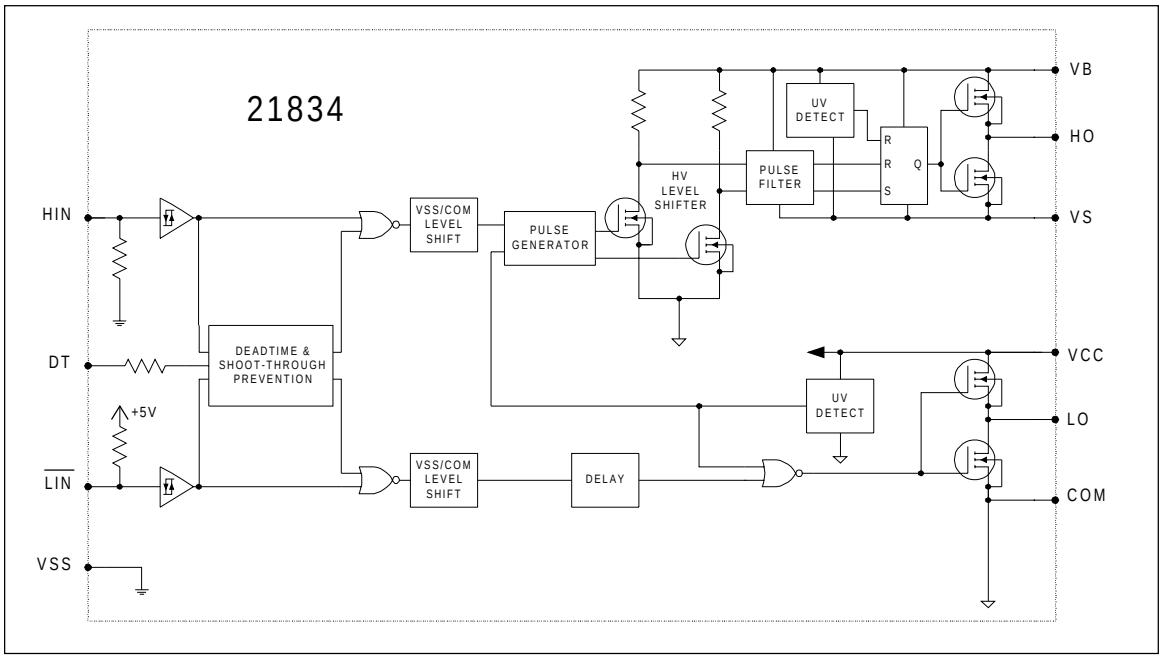
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, DT= V_{SS} and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads: HIN and $\overline{\text{LIN}}$. The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” input voltage for HIN & logic “0” for $\overline{\text{LIN}}$	2.7	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic “0” input voltage for HIN & logic “1” for $\overline{\text{LIN}}$	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1.2		I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	0.1		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	V_{IN} = 0V or 5V
I_{IN+}	Logic “1” input bias current	—	5	20	µA	HIN = 5V, $\overline{\text{LIN}}$ = 0V
I_{IN-}	Logic “0” input bias current	—	1	2		HIN = 0V, $\overline{\text{LIN}}$ = 5V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	1.4	1.9	—	A	V_O = 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	1.8	2.3	—		V_O = 15V, PW ≤ 10 µs

Functional Block Diagrams

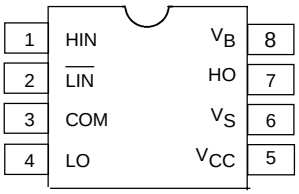




Lead Definitions

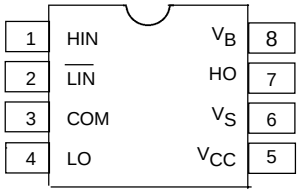
Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase (referenced to COM for IR2183 and VSS for IR21834)
$\overline{\text{LIN}}$	Logic input for low side gate driver output (LO), out of phase (referenced to COM for IR2183 and VSS for IR21834)
DT	Programmable dead-time lead, referenced to VSS. (IR21834 only)
VSS	Logic Ground (21834 only)
V_B	High side floating supply
HO	High side gate driver output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate driver output
COM	Low side return

Lead Assignments



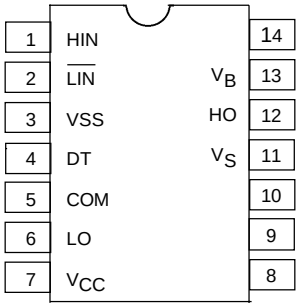
8-Lead PDIP

IR2183



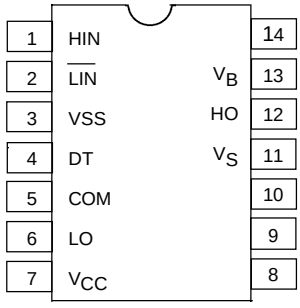
8-Lead SOIC

IR2183S



14-Lead PDIP

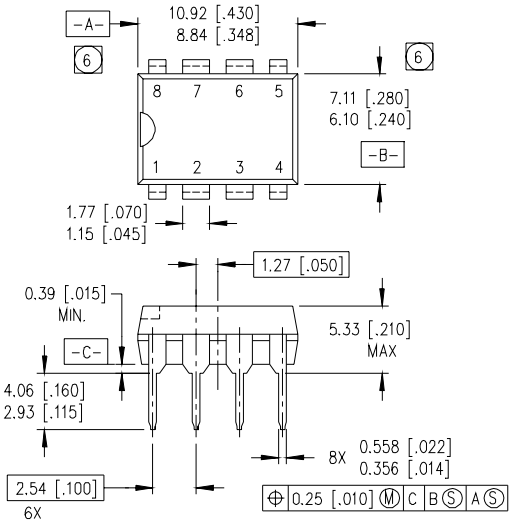
IR21834



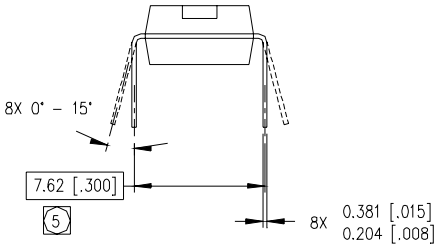
14-Lead SOIC

IR21834S

Case outlines

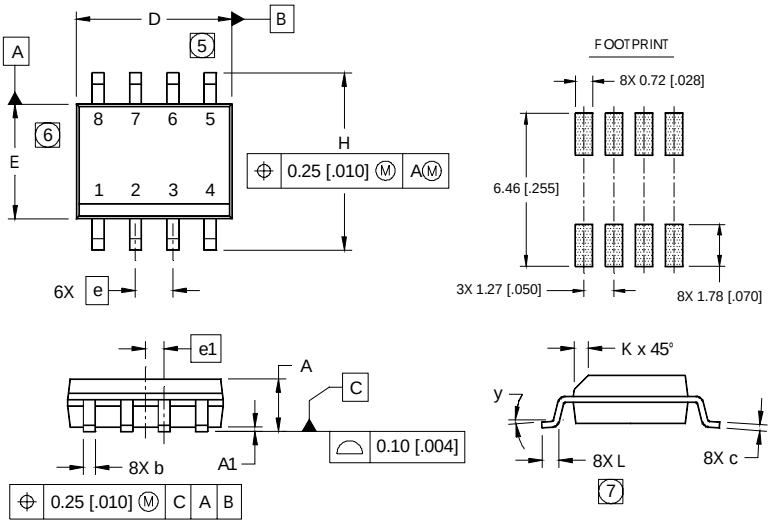


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8-Lead PDIP

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01-3003 01 (MS-001AB)

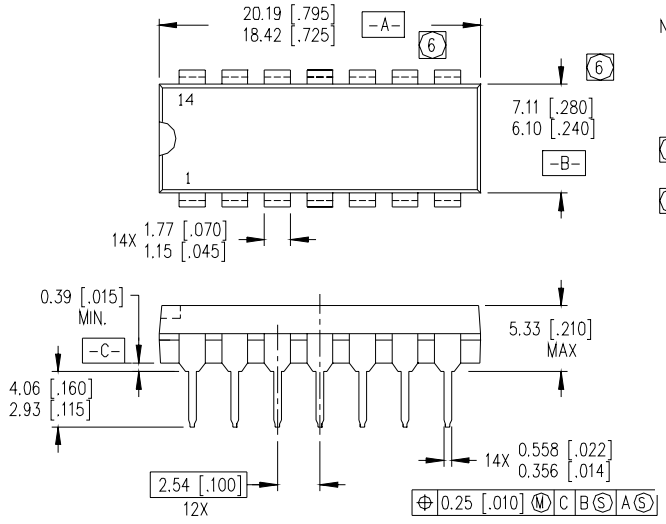


DIM	INCHES		MILLIMETERS	
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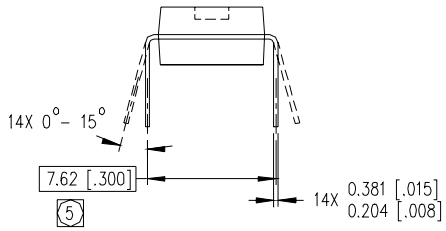
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8-Lead SOIC

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01-0021 11 (MS-012AA)

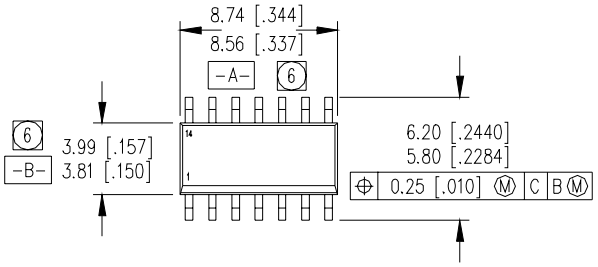


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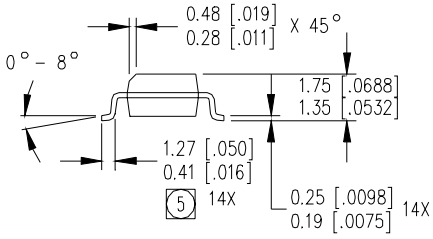


14-Lead PDIP

01-6010
01-3002 03 (MS-001AC)



NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2 CONTROLLING DIMENSION: MILLIMETER
3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4 OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AB.
5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



14-Lead SOIC (narrow body)

01-6019
01-3063 00 (MS-012AB)

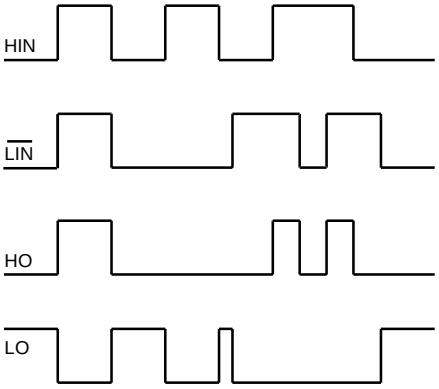


Figure 1. Input/Output Timing Diagram

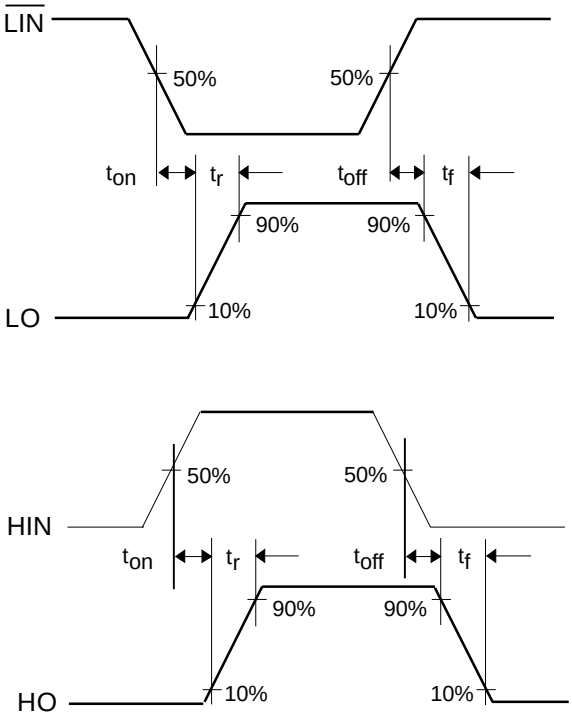


Figure 2. Switching Time Waveform Definitions

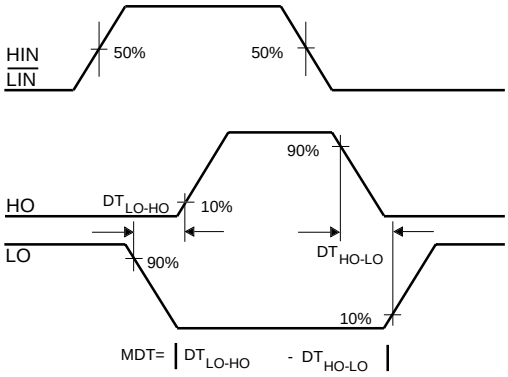


Figure 3. Deadtime Waveform Definitions

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

Data and specifications subject to change without notice. 7/23/2001

Data Sheet No. PD60174-D

International
IOR Rectifier

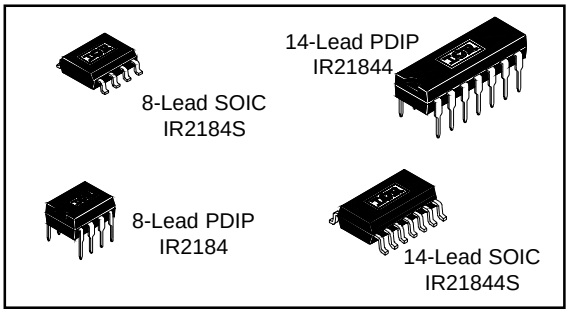
IR2184(4)(S)

HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
  - Fully operational to +600V
  - Tolerant to negative transient voltage
  - dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V and 5V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability 1.4A/1.8A

Packages



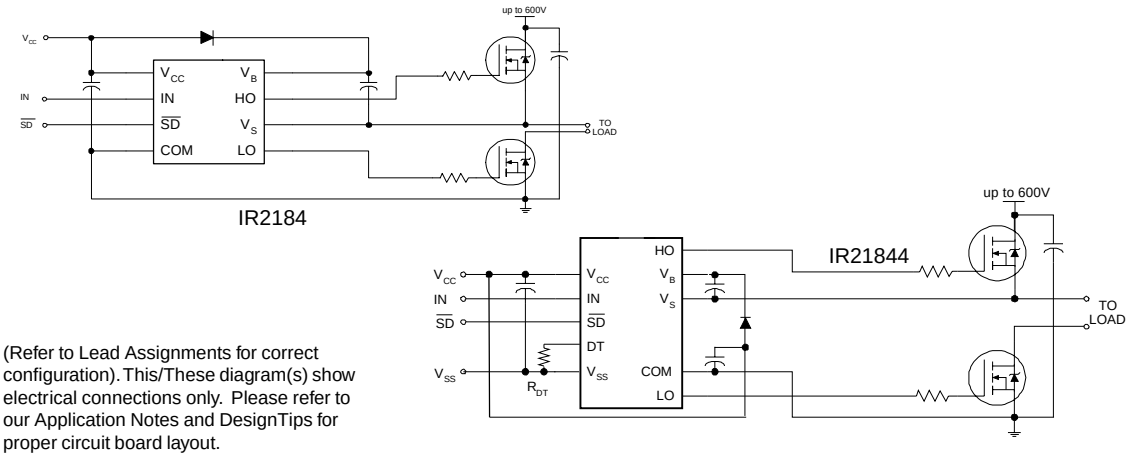
Description

The IR2184(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

IR2181/IR2183/IR2184 Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Dead-Time	Ground Pins	Ton/Toff
2181	HIN/LIN	no	none	COM	180/220 ns
21814				VSS/COM	
2183	HIN/$\overline{\text{LIN}}$	yes	Internal 500ns	COM	180/220 ns
21834			Program 0.4 ~ 5 us	VSS/COM	
2184	IN/$\overline{\text{SD}}$	yes	Internal 500ns	COM	680/270 ns
21844			Program 0.4 ~ 5 us	VSS/COM	

Typical Connection



(Refer to Lead Assignments for correct configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
DT	Programmable dead-time pin voltage (IR21844 only)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)		V_{SS} - 0.3	V_{SS} + 10	
V_{SS}	Logic ground (IR21844 only)		V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8-lead PDIP)	—	1.0	W
		(8-lead SOIC)	—	0.625	
		(14-lead PDIP)	—	1.6	
		(14-lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8-lead PDIP)	—	125	°C/W
		(8-lead SOIC)	—	200	
		(14-lead PDIP)	—	75	
		(14-lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
VB	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)	V_{SS}	V_{SS} + 5	
DT	Programmable dead-time pin voltage (IR21844 only)	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21844 only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).
Note 2: IN and SD are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C, DT = VSS unless otherwise specified.

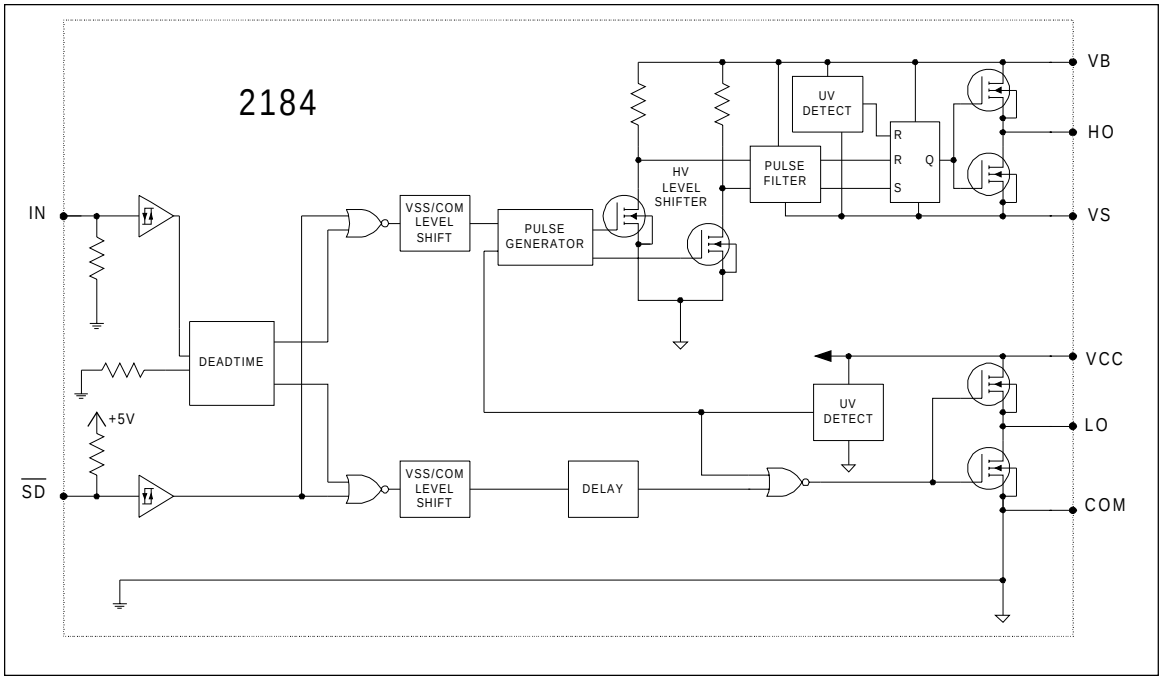
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	680	900	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	270	400		V_S = 0V or 600V
t_{sd}	Shut-down propagation delay	—	180	270		
MTon	Delay matching, HS & LS turn-on	—	0	90		
MToff	Delay matching, HS & LS turn-off	—	0	40		
t_r	Turn-on rise time	—	40	60		V_S = 0V
t_f	Turn-off fall time	—	20	35		V_S = 0V
DT	Deadtime: LO turn-off to HO turn-on(DT_{LO-HO}) &	280	400	520		RDT= 0
	HO turn-off to LO turn-on (DT_{HO-LO})	4	5	6	µsec	RDT = 200k
MDT	Deadtime matching = $DT_{LO\ -\ HO}$ - DT_{HO-LO}	—	0	50	nsec	RDT=0
		—	0	600		RDT = 200k

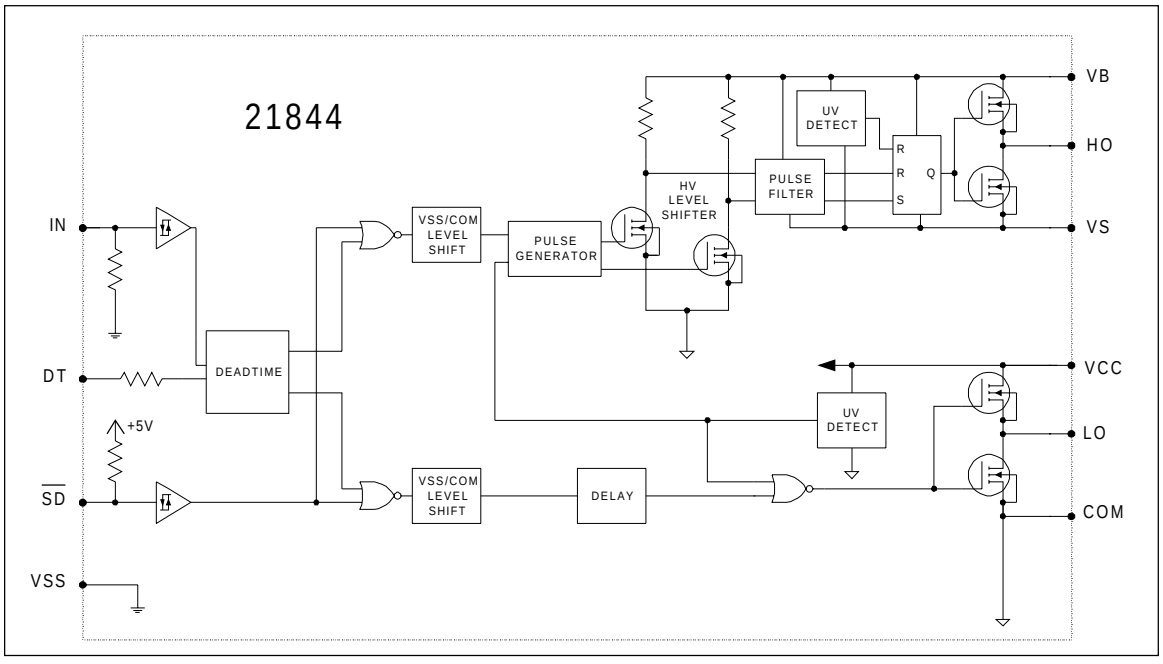
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, DT= V_{SS} and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS} /COM and are applicable to the respective input leads: IN and $\overline{SD}$. The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” input voltage for HO & logic “0” for LO	2.7	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic “0” input voltage for HO & logic “1” for LO	—	—	0.8		V_{CC} = 10V to 20V
$V_{SD,TH+}$	$\overline{SD}$ input positive going threshold	2.7	—	—		V_{CC} = 10V to 20V
$V_{SD,TH-}$	$\overline{SD}$ input negative going threshold	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1.2		I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	0.1		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	V_{IN} = 0V or 5V
I_{IN+}	Logic “1” input bias current	—	5	20	µA	IN = 5V, $\overline{SD}$ = 0V
I_{IN-}	Logic “0” input bias current	—	1	2		IN = 0V, $\overline{SD}$ = 5V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} dupply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed vurrent	1.4	1.9	—	A	V_O = 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	1.8	2.3	—		V_O = 15V, PW ≤ 10 µs

Functional Block Diagrams

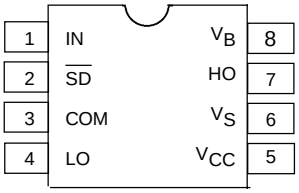




Lead Definitions

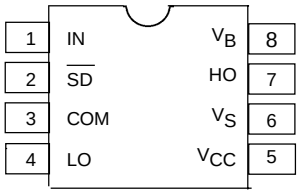
Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO (referenced to COM for IR2184 and VSS for IR21844)
$\overline{SD}$	Logic input for shutdown (referenced to COM for IR2184 and VSS for IR21844)
DT	Programmable dead-time lead, referenced to VSS. (IR21844 only)
VSS	Logic Ground (21844 only)
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



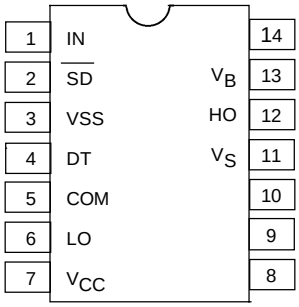
8-Lead PDIP

IR2184



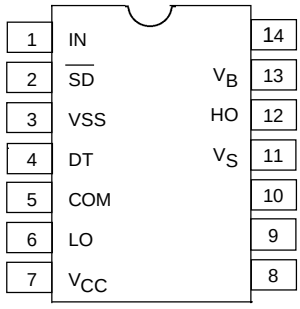
8-Lead SOIC

IR2184S



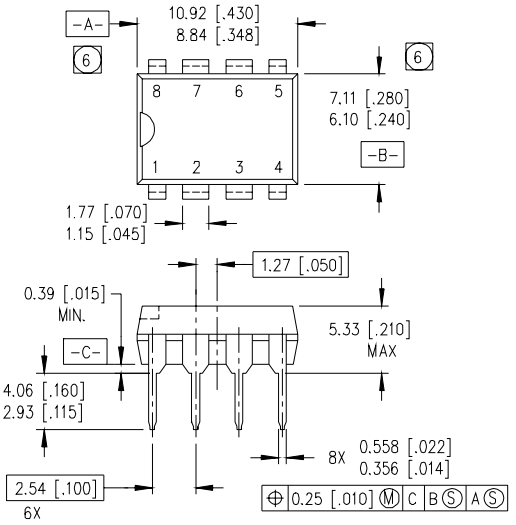
14-Lead PDIP

IR21844

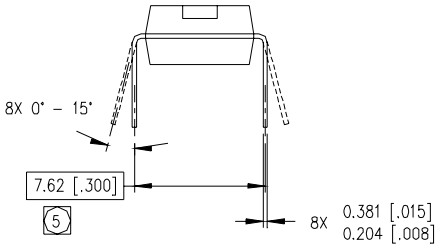


14-Lead SOIC

IR21844S

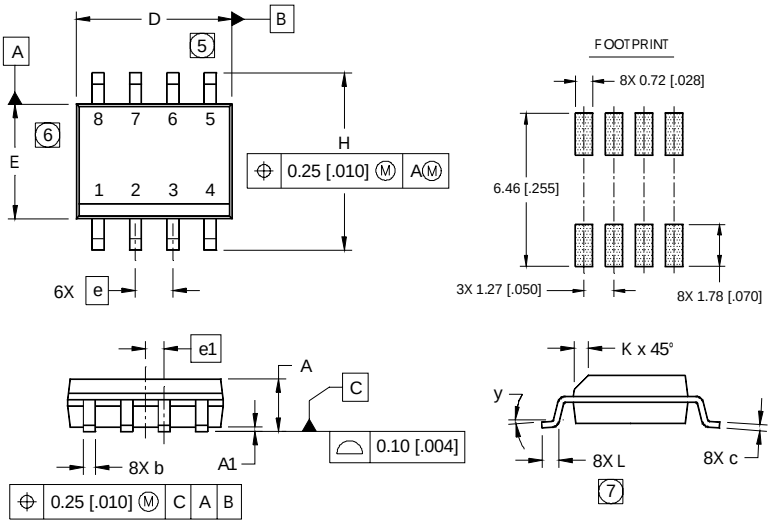


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8-Lead PDIP

01-6014
01-3003 01 (MS-001AB)

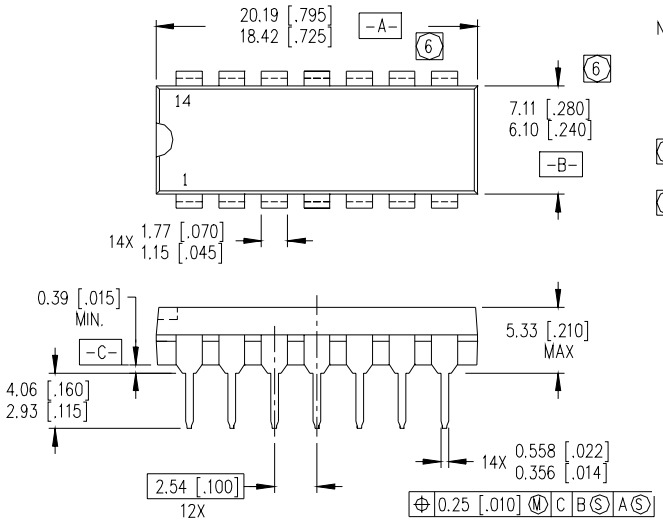


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

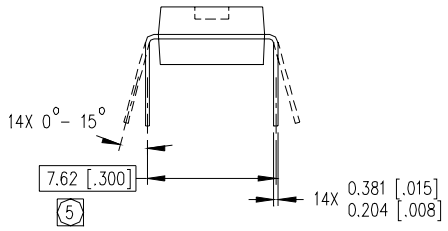
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
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3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
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6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8-Lead SOIC

01-6027
01-0021 11 (MS-012AA)

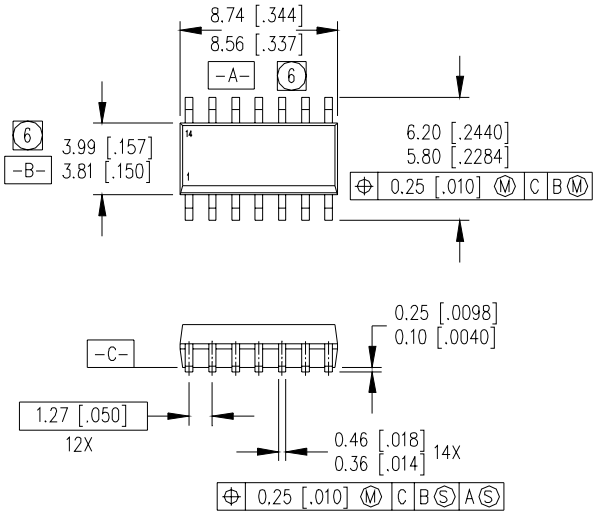


NOTES:
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3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
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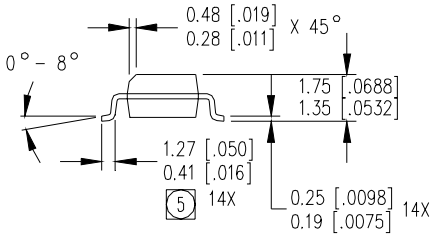


14-Lead PDIP

01-6010
01-3002 03 (MS-001AC)



NOTES:
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5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



14-Lead SOIC (narrow body)

01-6019
01-3063 00 (MS-012AB)

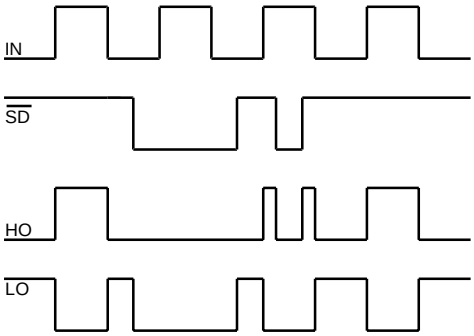


Figure 1. Input/Output Timing Diagram

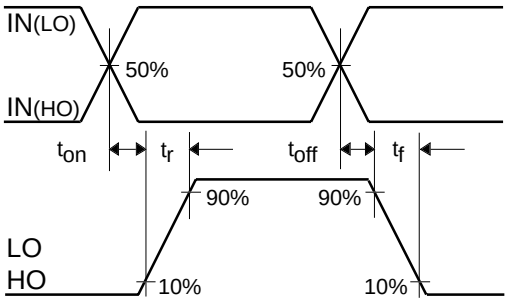


Figure 2. Switching Time Waveform Definitions

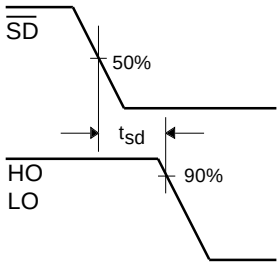


Figure 3. Shutdown Waveform Definitions

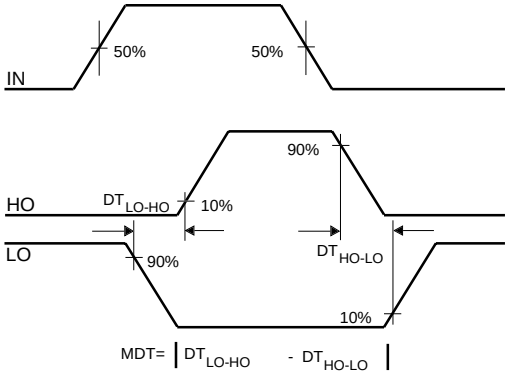


Figure 4. Deadtime Waveform Definitions

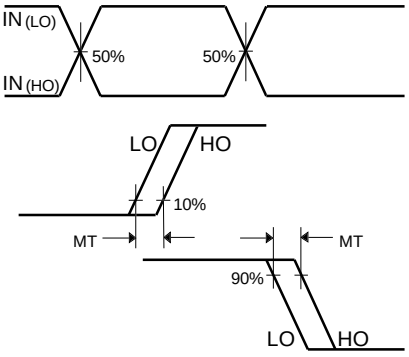


Figure 5. Delay Matching Waveform Definitions

International
IOR Rectifier

IR2213(S)

HIGH AND LOW SIDE DRIVER

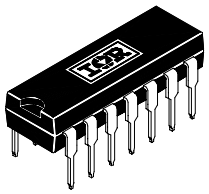
Features

- Floating channel designed for bootstrap operation
  Fully operational to +1200V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 12 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
  Separate logic supply range from 3.3V to 20V
  Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

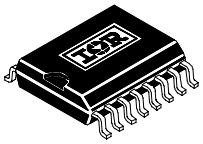
Product Summary

V_{OFFSET}	1200V max.
I_O+/-	1.7A / 2A
V_{OUT}	12 - 20V
$t_{on/off}$ (typ.)	280 & 225 ns
Delay Matching	30 ns

Packages



14-Lead PDIP

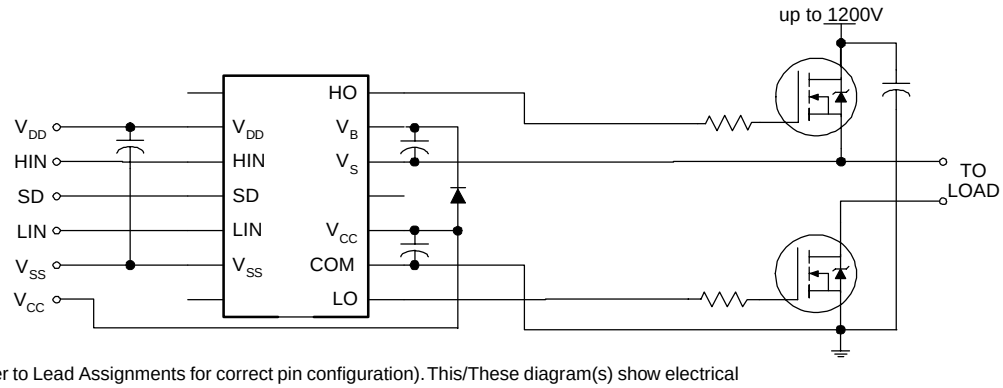


16-Lead SOIC
(wide body)

Description

The IR2213(S) is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 1200 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High Side Floating Supply Voltage		-0.3	1225	
V_S	High Side Floating Supply Offset Voltage		V_B - 25	V_B + 0.3	V
V_{HO}	High Side Floating Output Voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low Side Fixed Supply Voltage		-0.3	25	
V_{LO}	Low Side Output Voltage		-0.3	V_{CC} + 0.3	
V_{DD}	Logic Supply Voltage		-0.3	V_{SS} + 25	
V_{SS}	Logic Supply Offset Voltage		V_{CC} - 25	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)		V_{SS} - 0.3	V_{DD} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient (Figure 2)		—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$	(14 Lead PDIP)	—	1.6	W
		(16 Lead SOIC)	—	1.25	
R_{THJA}	Thermal Resistance, Junction to Ambient	(14 Lead PDIP)	—	75	°C/W
		(16 Lead SOIC)	—	100	
T_J	Junction Temperature		—	125	°C
T_S	Storage Temperature		-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Absolute Voltage	V_S + 12	V_S + 20	V
V_S	High Side Floating Supply Offset Voltage	Note 1	1200	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Low Side Fixed Supply Voltage	12	20	
V_{LO}	Low Side Output Voltage	0	V_{CC}	
V_{DD}	Logic Supply Voltage	V_{SS} + 3	V_{SS} + 20	
V_{SS}	Logic Supply Offset Voltage	-5 (Note 2)	5	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	

Note 1: Logic operational for V_S of -5 to +1200V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).
Note 2: When V_{DD}<5V, the minimum V_{SS} offset is limited to $-V_{DD}$

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

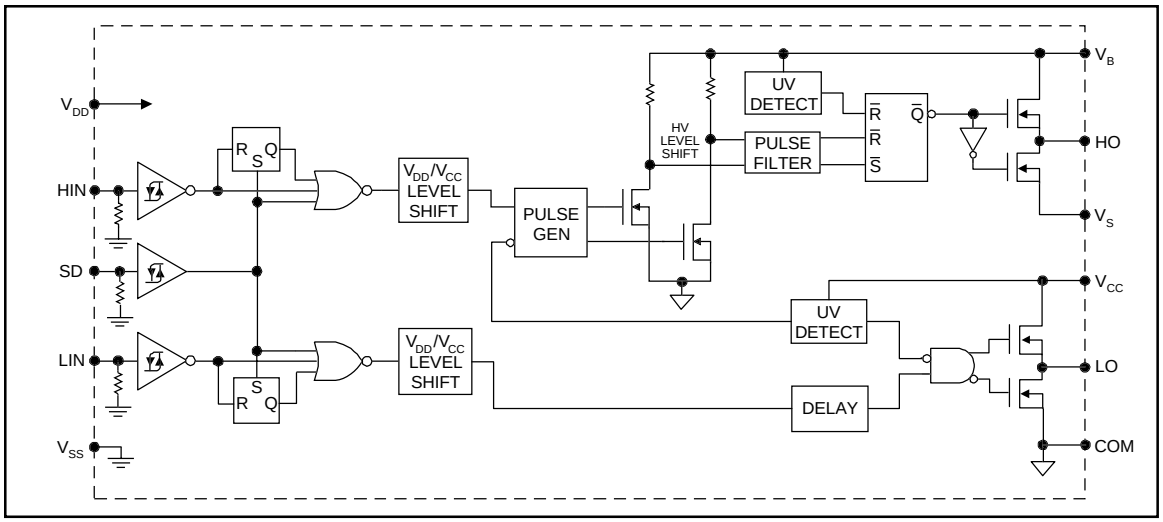
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	—	280	—	ns	V_S = 0V
t_{off}	Turn-Off Propagation Delay	—	225	—		V_S = 1200V
t_{sd}	Shutdown Propagation Delay	—	230	—		V_S = 1200V
t_r	Turn-On Rise Time	—	25	—		
t_f	Turn-Off Fall Time	—	17	—		
MT	Delay Matching, HS & LS Turn-On/Off	—	—	30		Figure 5

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” Input Voltage	9.5	—	—	V	
V_{IL}	Logic “0” Input Voltage	—	—	6.0		
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	—	—	1.2		I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	—	—	0.1		I_O = 0A
I_{LK}	Offset Supply Leakage Current	—	—	50	µA	V_B = V_S = 1200V
I_{QBS}	Quiescent V_{BS} Supply Current	—	125	230		V_{IN} = 0V or V_{DD}
I_{QCC}	Quiescent V_{CC} Supply Current	—	180	340		V_{IN} = 0V or V_{DD}
I_{QDD}	Quiescent V_{DD} Supply Current	—	15	30		V_{IN} = 0V or V_{DD}
I_{IN+}	Logic “1” Input Bias Current	—	20	40		V_{IN} = V_{DD}
I_{IN-}	Logic “0” Input Bias Current	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	8.7	10.2	11.7	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	7.9	9.3	10.7		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	8.7	10.2	11.7		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	7.9	9.3	10.7		
I_{O+}	Output High Short Circuit Pulsed Current	1.7	2.0`	—	A	V_O = 0V, V_{IN} = V_{DD} PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	2.0	2.5	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

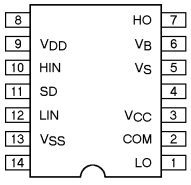
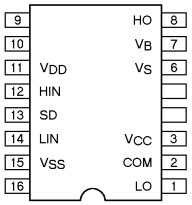
Functional Block Diagram



Lead Definitions

Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

	
14 Lead PDIP	16 Lead SOIC (Wide Body)
IR2213	**IR2213S**
Part Number	

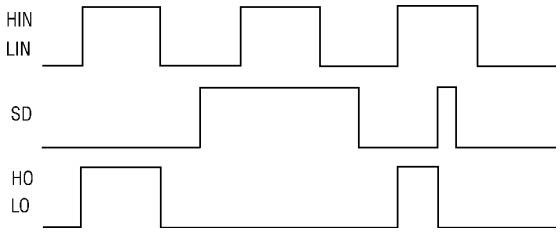


Figure 1. Input/Output Timing Diagram

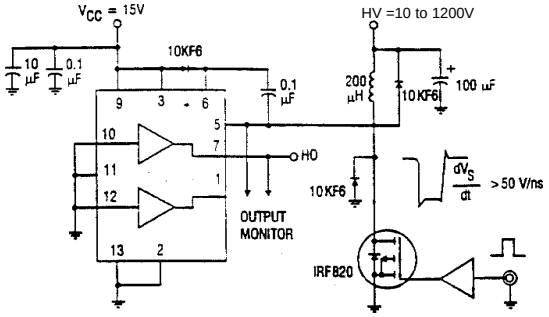


Figure 2. Floating Supply Voltage Transient Test Circuit

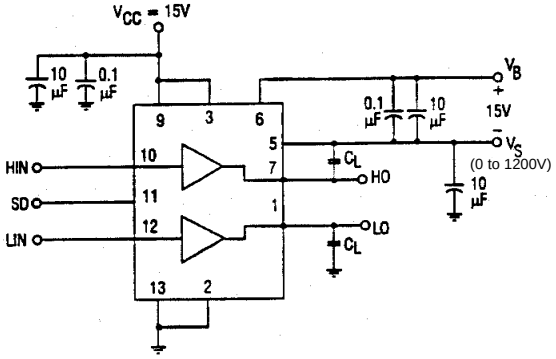


Figure 3. Switching Time Test Circuit

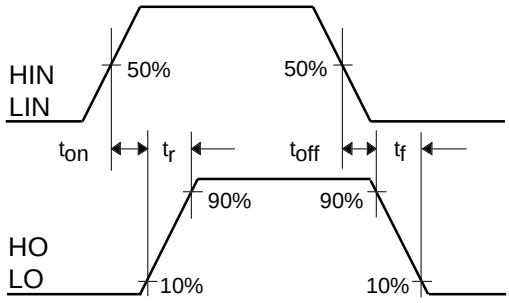


Figure 4. Switching Time Waveform Definition

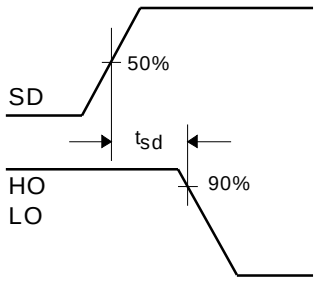


Figure 5. Shutdown Waveform Definitions

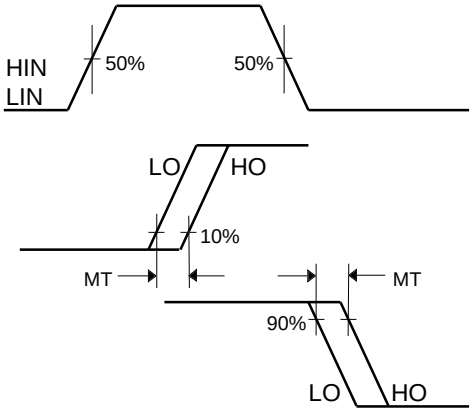


Figure 6. Delay Matching Waveform Definitions

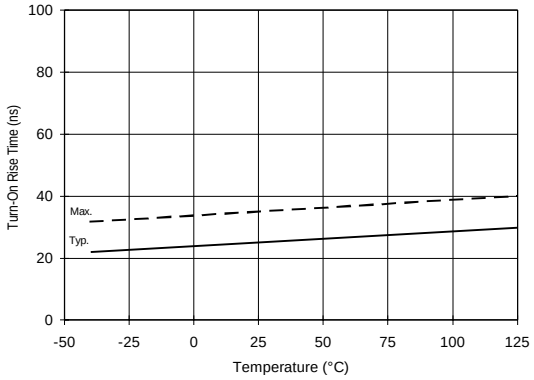


Figure 10A. Turn-On Rise Time vs. Temperature

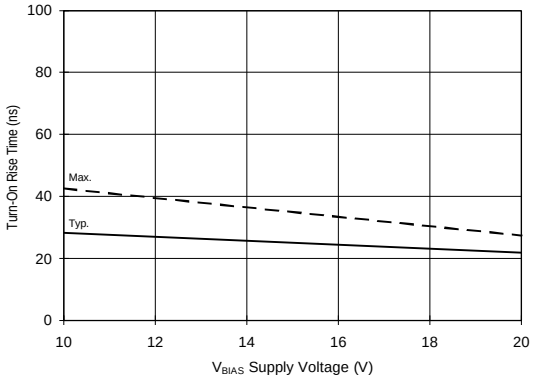


Figure 10B. Turn-On Rise Time vs. Voltage

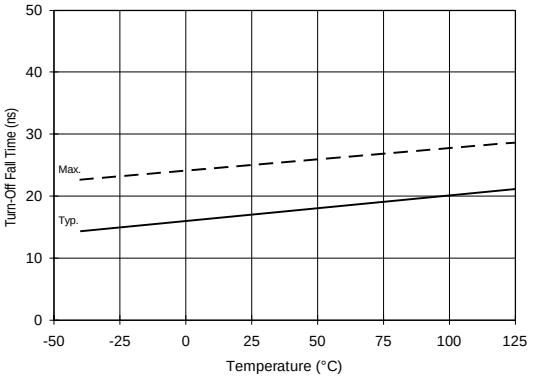


Figure 11A. Turn-Off Fall Time vs. Temperature

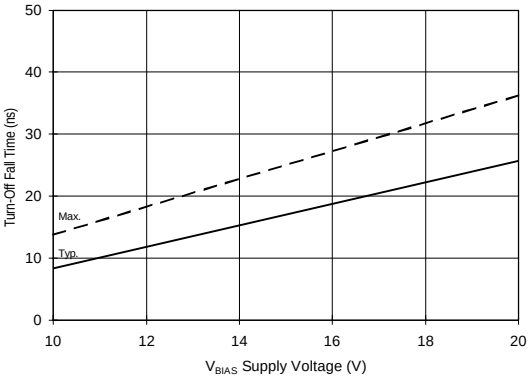


Figure 11B. Turn-Off Fall Time vs. Voltage

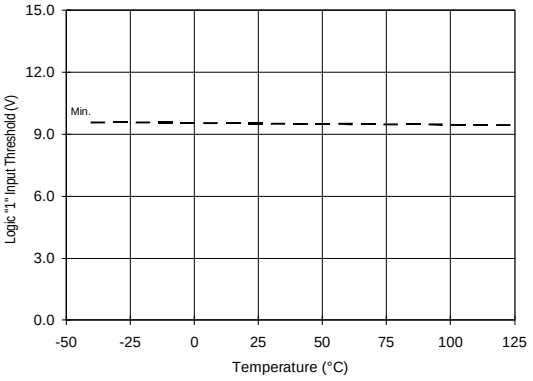


Figure 12A. Logic "1" Input Threshold vs. Temperature

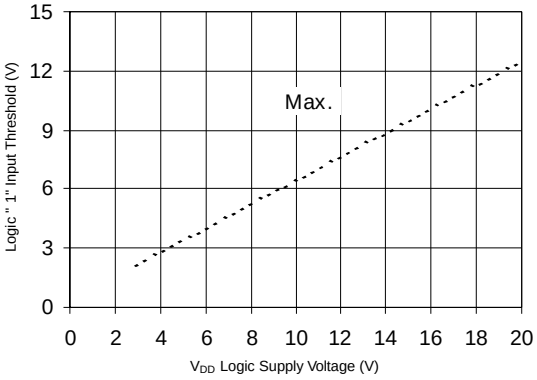


Figure 12B. Logic "1" Input Threshold vs. Voltage

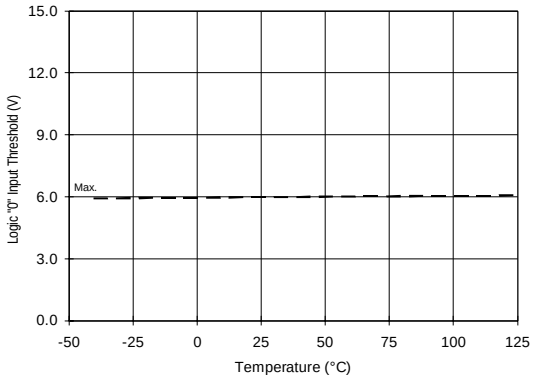


Figure 13A. Logic "0" Input Threshold vs. Temperature

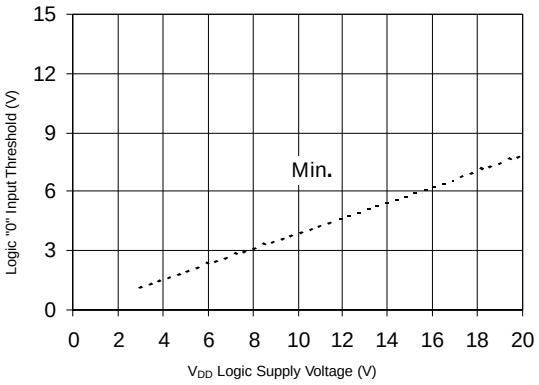


Figure 13B. Logic "0" Input Threshold vs. Voltage

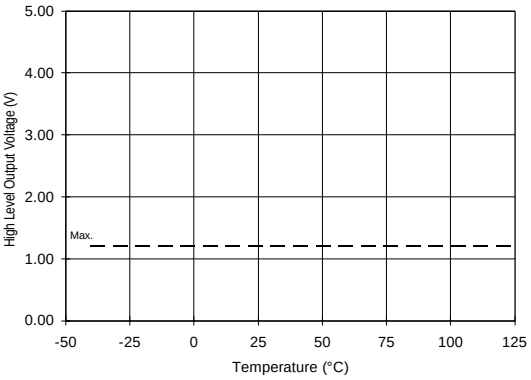


Figure 14A. High Level Output vs. Temperature

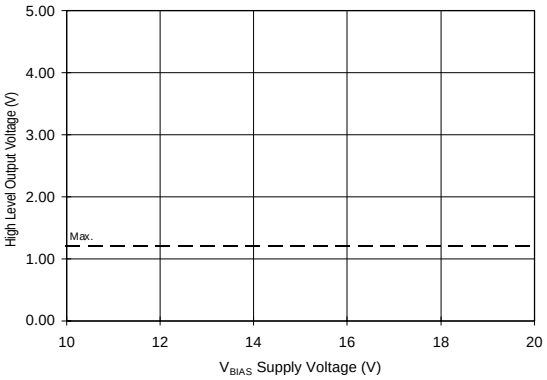


Figure 14B. High Level Output vs. Voltage

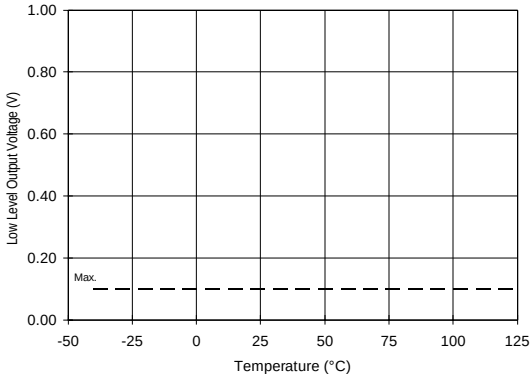


Figure 15A. Low Level Output vs. Temperature

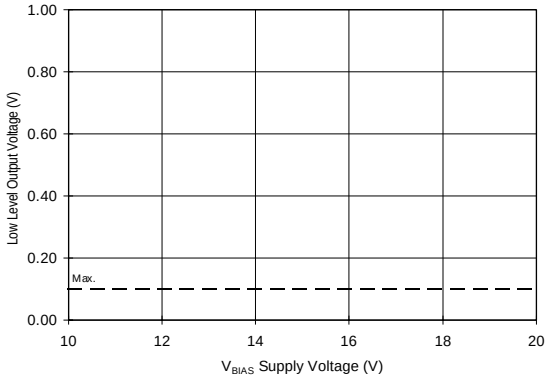


Figure 15B. Low Level Output vs. Voltage

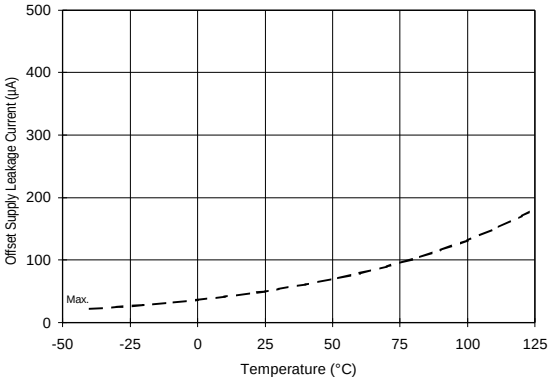


Figure 16A. Offset Supply Current vs. Temperature

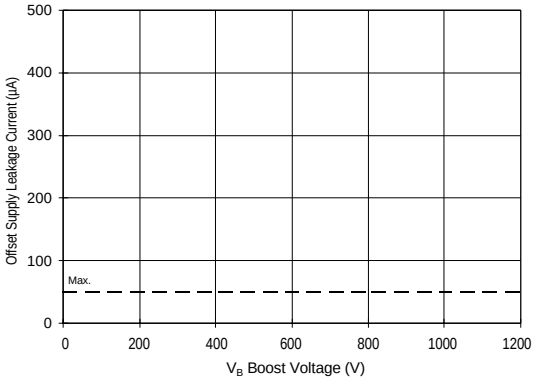


Figure 16B. Offset Supply Current vs. Voltage

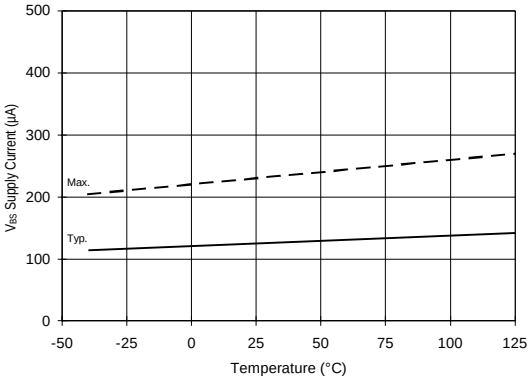


Figure 17A. V_{BS} Supply Current vs. Temperature

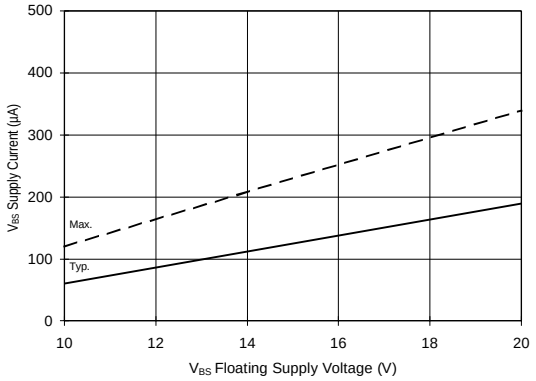


Figure 17B. V_{BS} Supply Current vs. Voltage

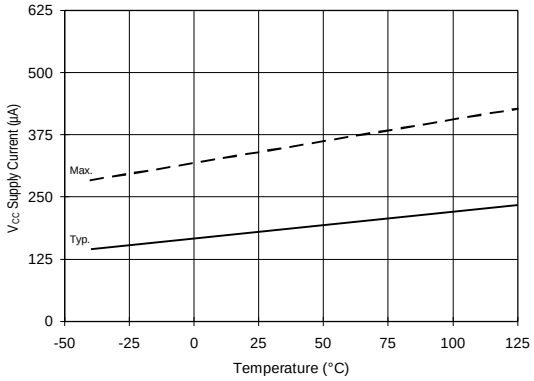


Figure 18A. V_{CC} Supply Current vs. Temperature

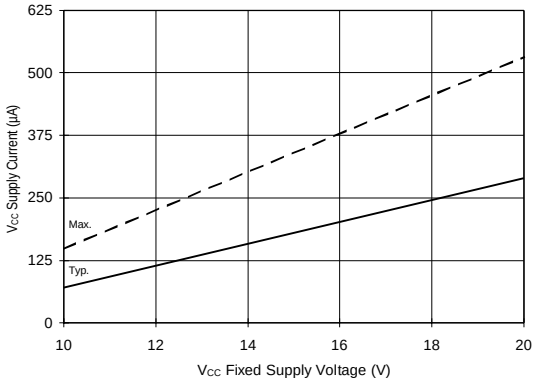


Figure 18B. V_{CC} Supply Current vs. Voltage

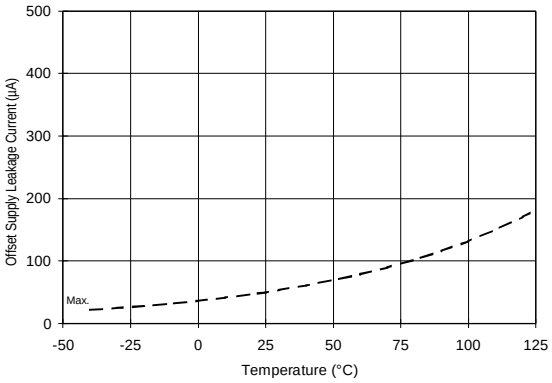


Figure 16A. Offset Supply Current vs. Temperature

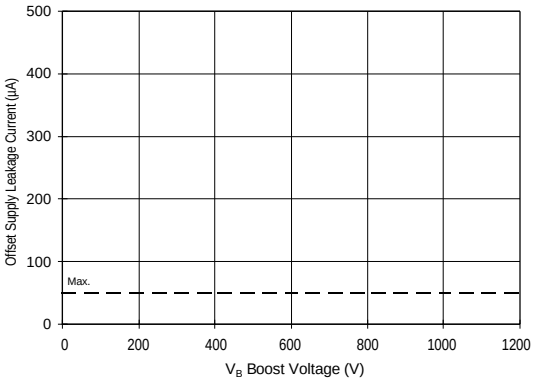


Figure 16B. Offset Supply Current vs. Voltage

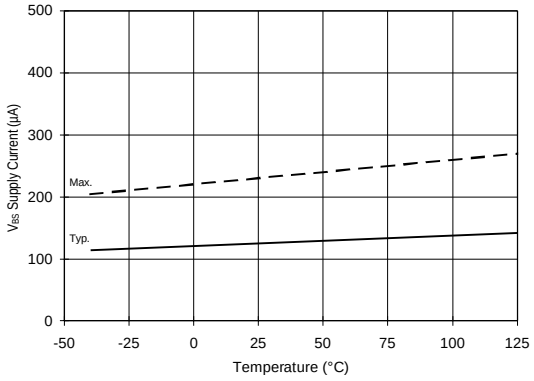


Figure 17A. V_{BS} Supply Current vs. Temperature

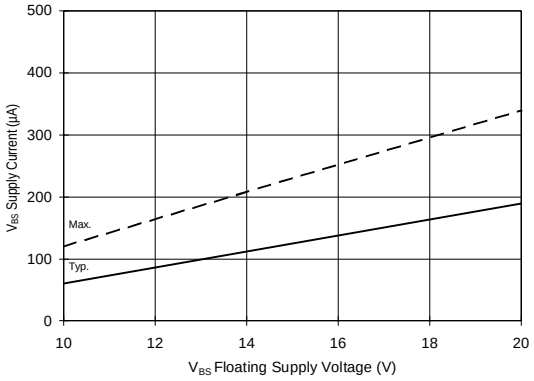


Figure 17B. V_{BS} Supply Current vs. Voltage

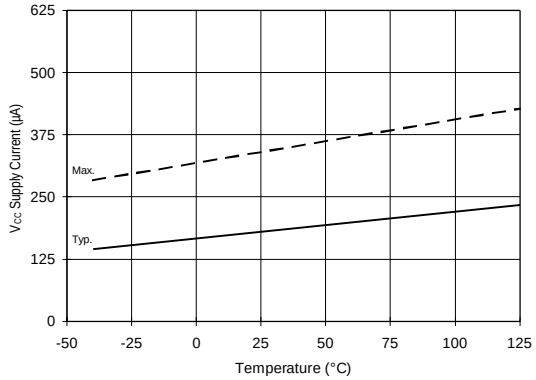


Figure 18A. V_{CC} Supply Current vs. Temperature

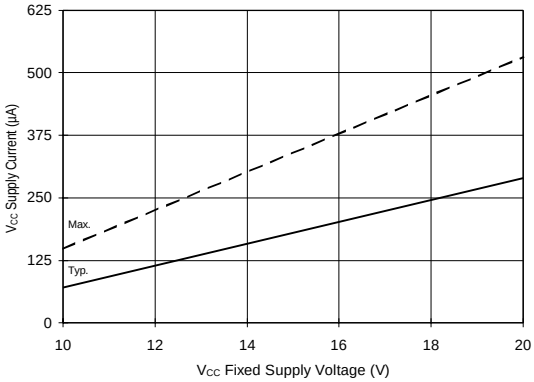


Figure 18B. V_{CC} Supply Current vs. Voltage

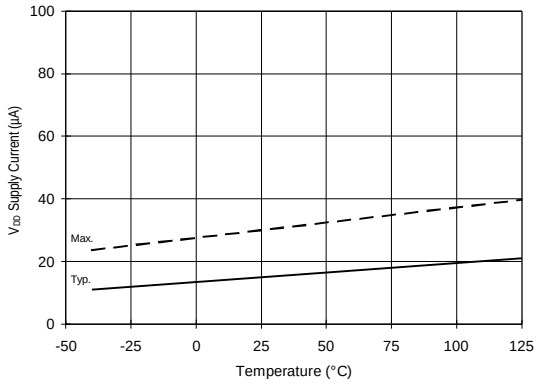


Figure 19A. V_{DD} Supply Current vs. Temperature

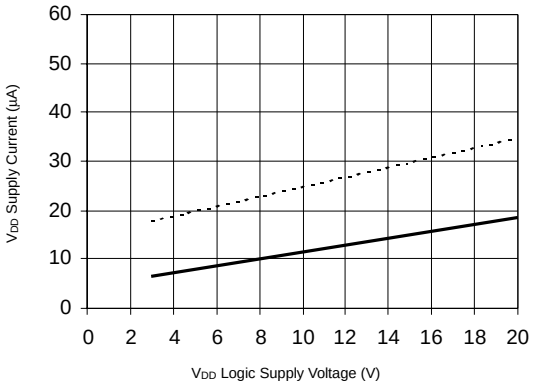


Figure 19B. V_{DD} Supply Current vs. V_{DD} Voltage

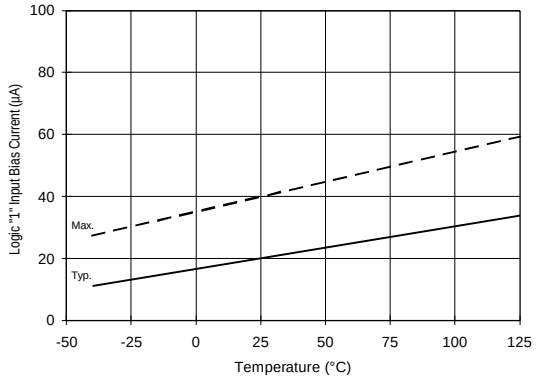


Figure 20A. Logic "1" Input Current vs. Temperature

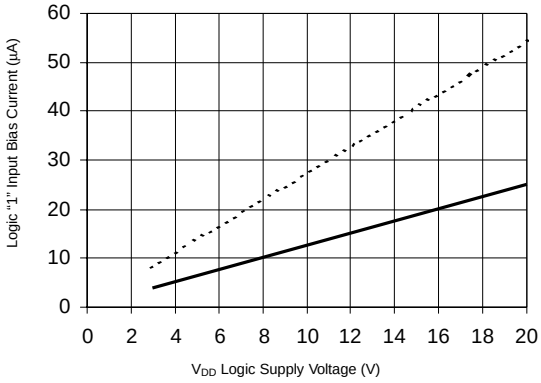


Figure 20B. Logic "1" Input Current vs. V_{DD} Voltage

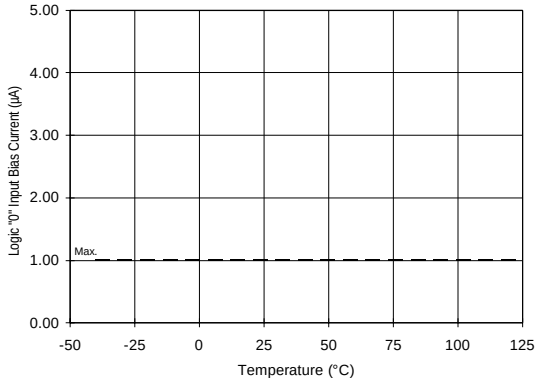


Figure 21A. Logic "0" Input Current vs. Temperature

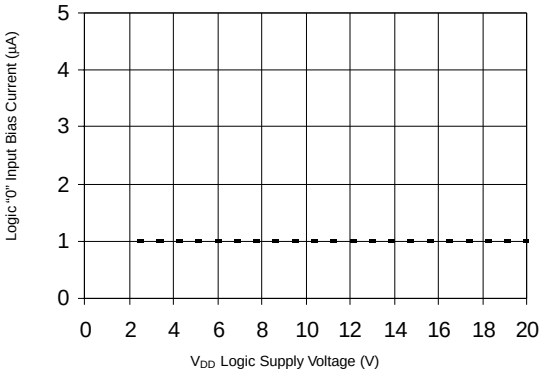


Figure 21B. Logic "0" Input Current vs. V_{DD} Voltage

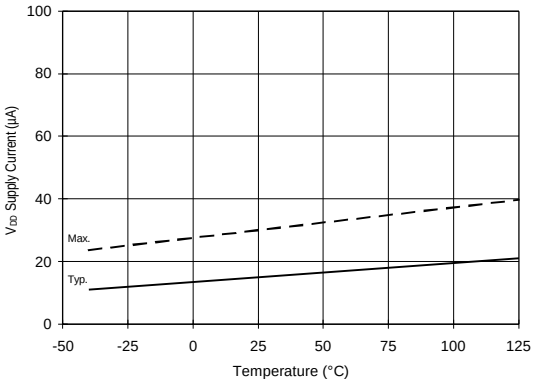


Figure 19A. V_{DD} Supply Current vs. Temperature

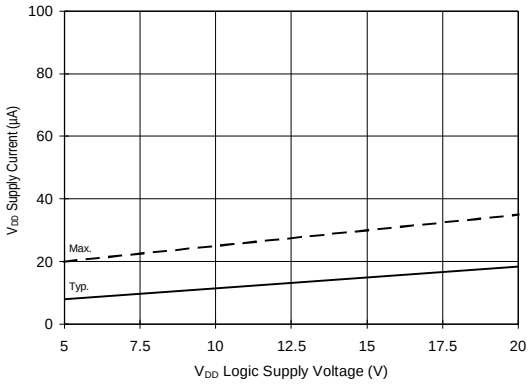


Figure 19B. V_{DD} Supply Current vs. Voltage

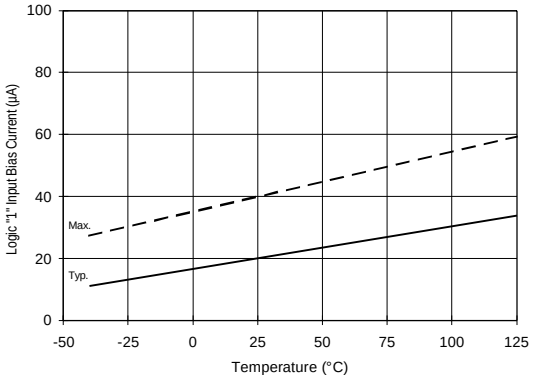


Figure 20A. Logic "1" Input Current vs. Temperature

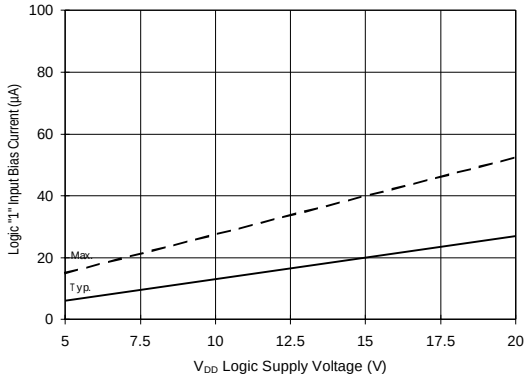


Figure 20B. Logic "1" Input Current vs. Voltage

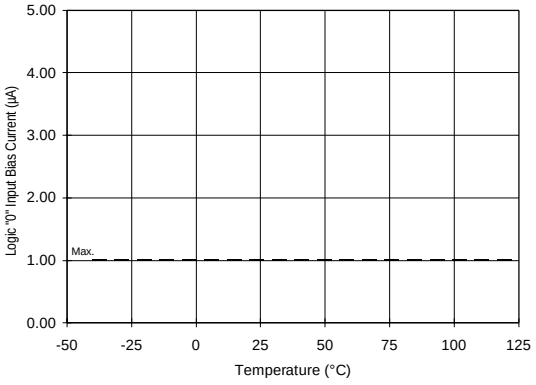


Figure 21A. Logic "0" Input Current vs. Temperature

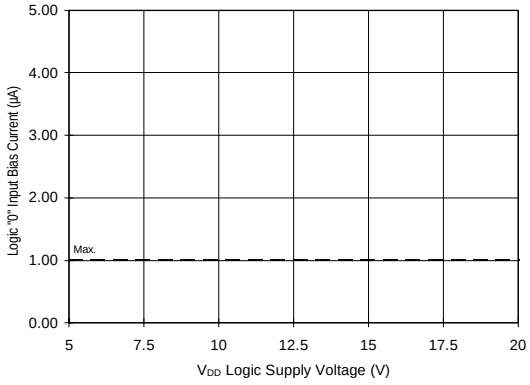


Figure 21B. Logic "0" Input Current vs. Voltage

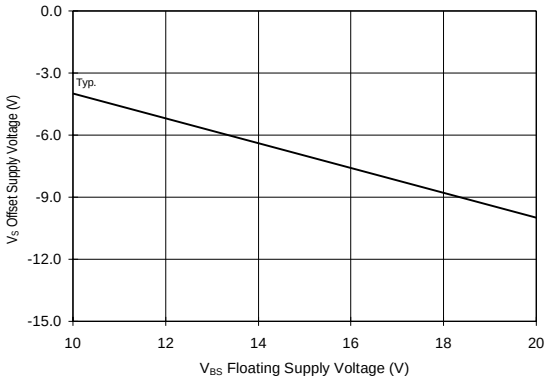


Figure 36. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

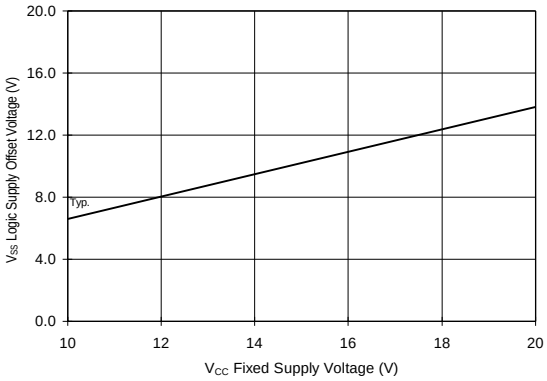
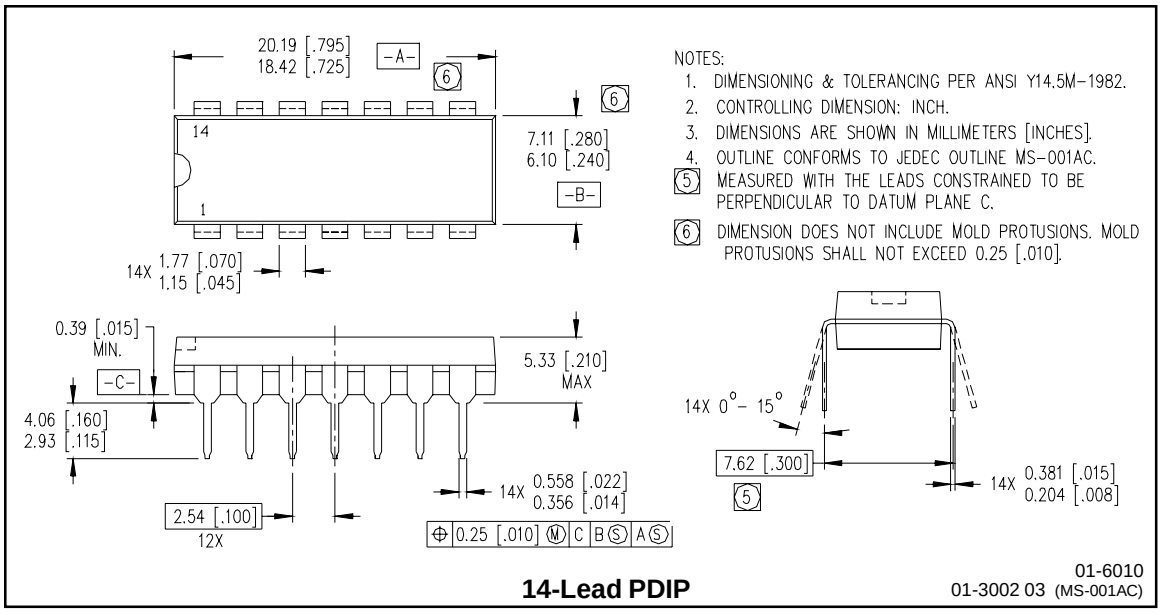
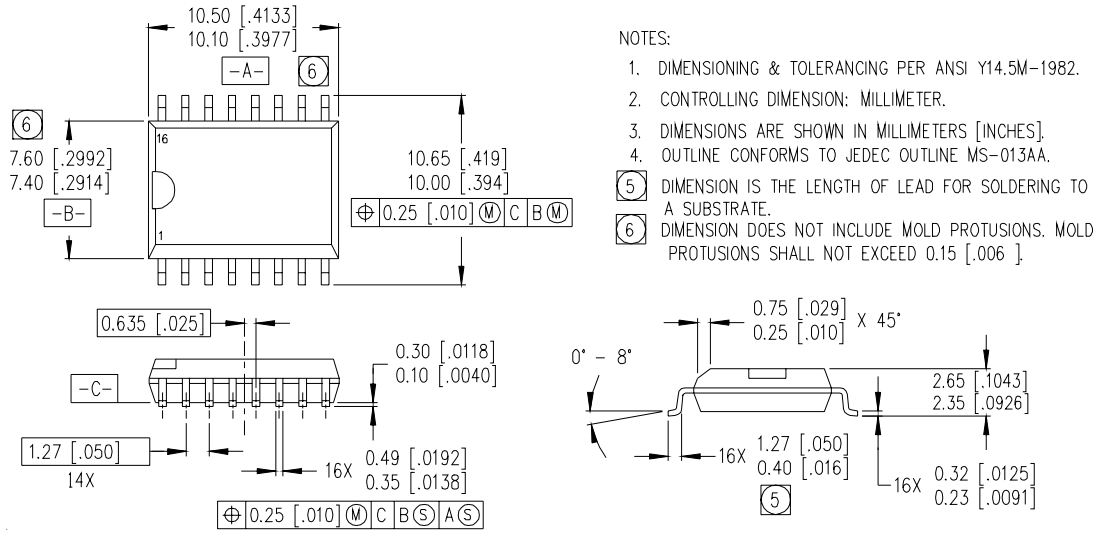


Figure 37. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage

Case outlines



14-Lead PDIP



16-Lead SOIC (wide body)

01 6015
01-3014 03 (MS-013AA)

Data Sheet No. PD60177-C

International
IOR Rectifier

IR4426/IR4427/IR4428

DUAL LOW SIDE DRIVER

Features

- Gate drive supply range from 6 to 20V
- CMOS Schmitt-triggered inputs
- Matched propagation delay for both channels
- Outputs out of phase with inputs (IR4426)
- Outputs in phase with inputs (IR4427)
- OutputA out of phase with inputA and OutputB in phase with inputB (IR4428)

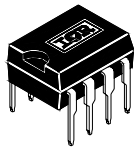
Descriptions

The IR4426/IR4427/IR4428 is a low voltage, high speed power MOSFET and IGBT driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays between two channels are matched.

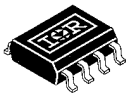
Product Summary

I_O+/-	1.5A / 1.5A
V_{OUT}	6V - 20V
$t_{on/off}$ (typ.)	85 & 65 ns

Packages

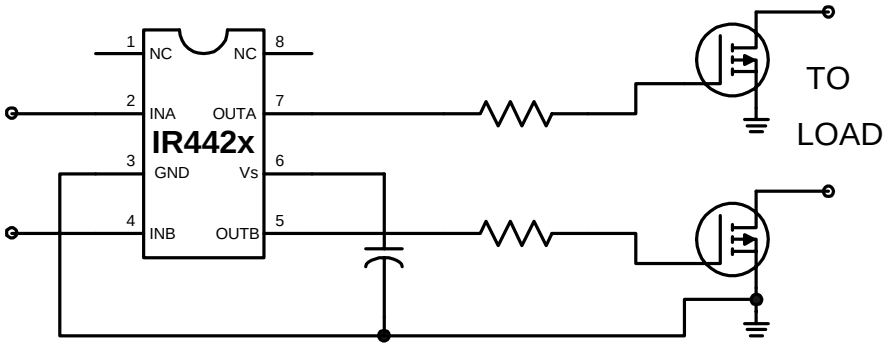


8 Lead PDIP



8 Lead SOIC

Block Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	Fixed supply voltage		-0.3	25	V
V_O	Output voltage		-0.3	V_S + 0.3	
V_{IN}	Logic input voltage		-0.3	V_S + 0.3	
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 Lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND.

Symbol	Definition	Min.	Max.	Units
V_S	Fixed supply voltage	6	20	V
V_O	Output voltage	0	V_S	
V_{IN}	Logic input voltage	0	V_S	
T_A	Ambient temperature	-40	125	°C

DC Electrical Characteristics

V_{BIAS} (V_S) = 15V, T_A = 25°C unless otherwise specified. The V_{IN}, and I_{IN} parameters are referenced to GND and are applicable to input leads: INA and INB. The V_O and I_O parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “0” input voltage (OUTA=LO, OUTB=LO) (IR4426) Logic “1” input voltage (OUTA=HI, OUTB=HI) (IR4427) Logic “0” input voltage (OUTA=LO), Logic “1” input voltage (OUTB=HI) (IR4428)	2.7	—	—	V	

DC Electrical Characteristics cont.

V_{BIAS} (V_S) = 15V, T_A = 25°C unless otherwise specified. The V_{IN}, and I_{IN} parameters are referenced to GND and are applicable to input leads: INA and INB. The V_O and I_O parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

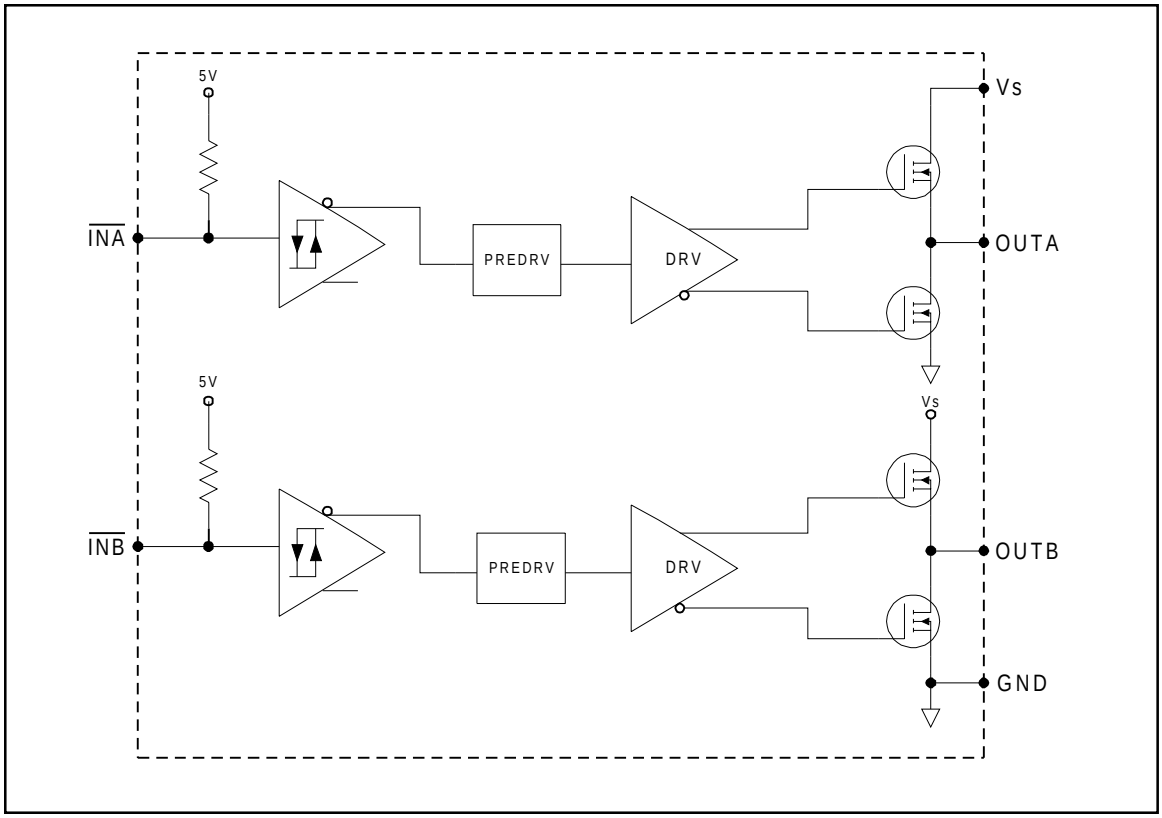
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IL}	Logic "1" input voltage (OUTA=HI, OUTB=HI) (IR4426) Logic "0" input voltage (OUTA=LO, OUTB=LO) (IR4427) Logic "I" input voltage (OUTA=HI), Logic "0" input voltage (OUTB=LO) (IR4428)	—	—	0.8	V	
V_{OH}	High level output voltage, V_{BIAS}-V_O	—	—	1.2		
V_{OL}	Low level output voltage, V_O	—	—	0.1		
I_{IN+}	Logic "1" input bias current (OUT=HI)	—	5	15	µA	V_{IN} = 0V (IR4426) V_{IN} = V_S (IR4427) V_{INA} = 0V (IR4428) V_{INB} = V_S (IR4428)
I_{IN-}	Logic "0" input bias current (OUT=LO)	—	-10	-30		V_{IN} = V_S (IR4426) V_{IN} = 0V (IR4427) V_{INA} = V_S (IR4428) V_{INB} = 0V (IR4428)
I_{QS}	Quiescent Vs supply current	—	100	200		V_{IN} = 0V or V_S
I_{O+}	Output high short circuit pulsed current	1.5	2.3	—	A	V_O = 0V, V_{IN} = 0 (IR4426) V_O = 0V, V_{IN} = V_S (IR4427) V_O = 0V, V_{INA} = 0 (IR4428) V_O = 0V, V_{INB} = V_S (IR4428) PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	1.5	3.3	—		V_O = 15V, V_{IN} = V_S (IR4426) V_O = 15V, V_{IN} = 0 (IR4427) V_O = 15V, V_{INA} = V_S (IR4428) V_O = 15V, V_{INB} = 0 (IR4428) PW ≤ 10 µs

AC Electrical Characteristics

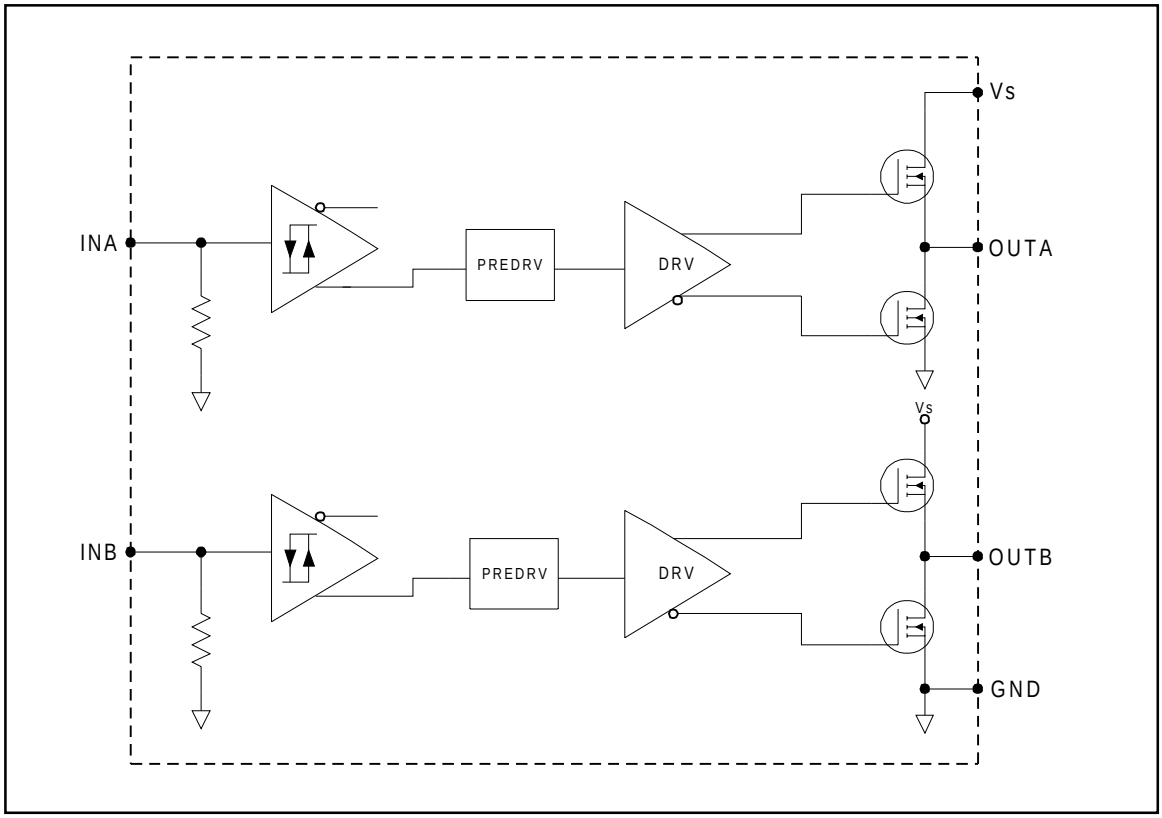
V_{BIAS} (V_S) = 15V, CL = 1000pF, T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation delay characteristics						
t_{d1}	Turn-on propagation delay	—	85	160	ns	figure 4
t_{d2}	Turn-off propagation delay	—	65	150		
t_r	Turn-on rise time	—	15	35		
t_f	Turn-off fall time	—	10	25		

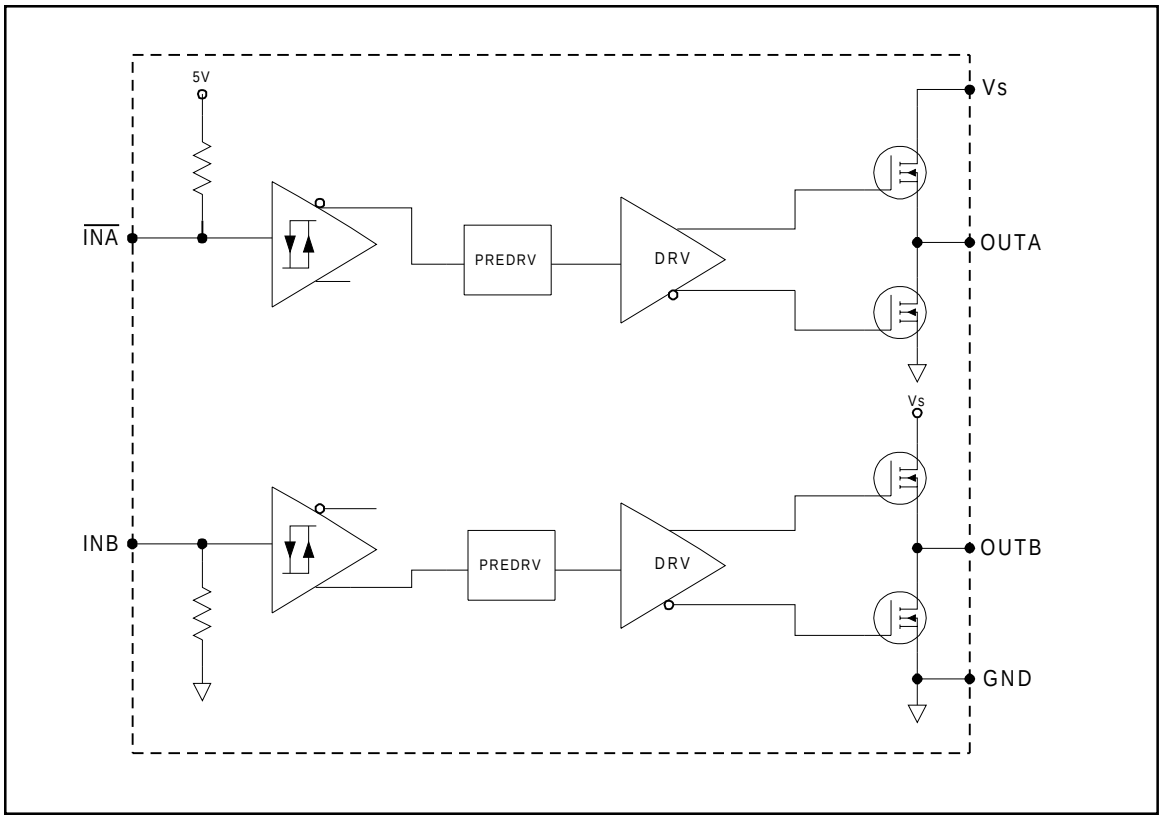
Functional Block Diagram IR4426



Functional Block Diagram IR4427



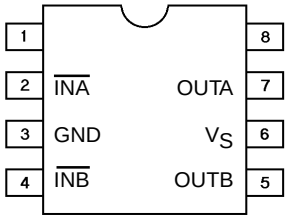
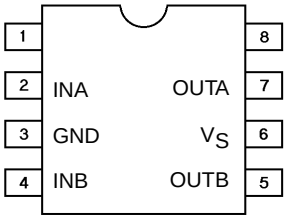
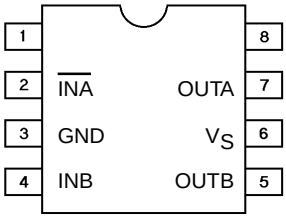
Functional Block Diagram IR4428



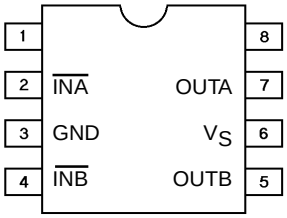
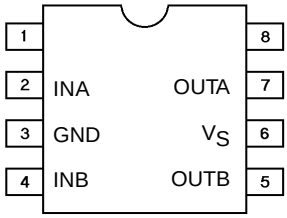
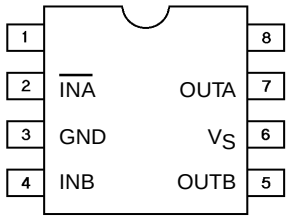
Lead Definitions

Symbol	Description
V_S	Supply voltage
GND	Ground
INA	Logic input for gate driver output (OUTA), out of phase (IR4426, IR4428), in phase (IR4427)
INB	Logic input for gate driver output (OUTB), out of phase (IR4426), in phase (IR4427, IR4428)
OUTA	Gate drive output A
OUTB	Gate drive output B

Lead Assignments

		
8 Lead PDIP	8 Lead PDIP	8 Lead PDIP
IR4426	**IR4427**	**IR4428**
Part Number		

Lead Assignments

		
8 Lead SOIC	8 Lead SOIC	8 Lead SOIC
IR4426S	**IR4427S**	**IR4428S**
Part Number		

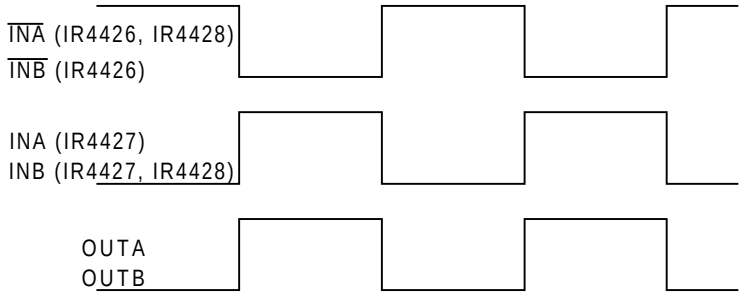


Figure 3. Timing Diagram

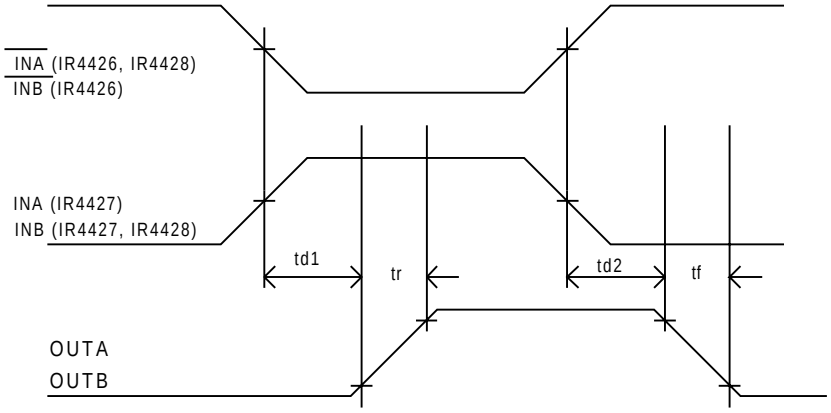


Figure 4. Switching Time Waveforms

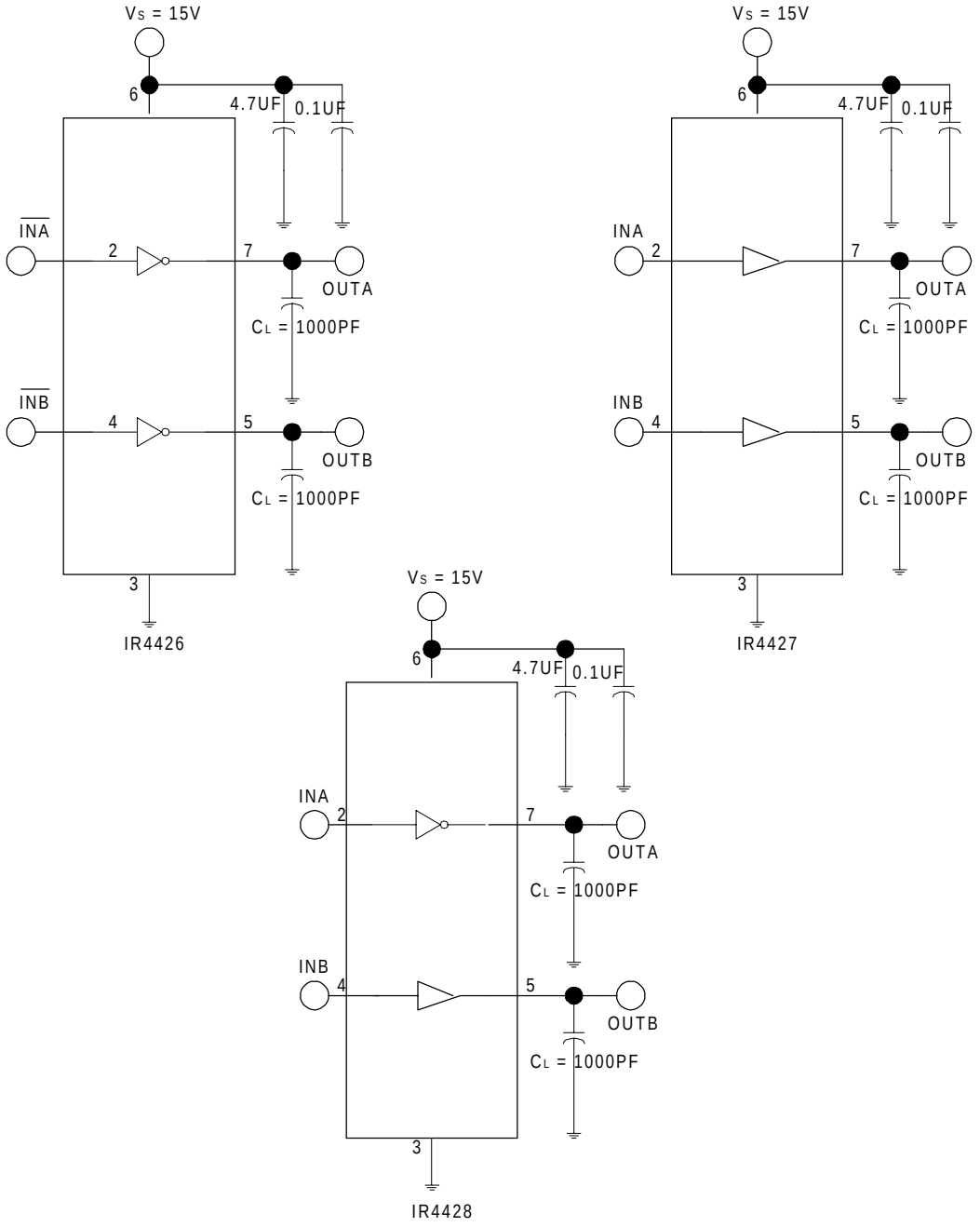
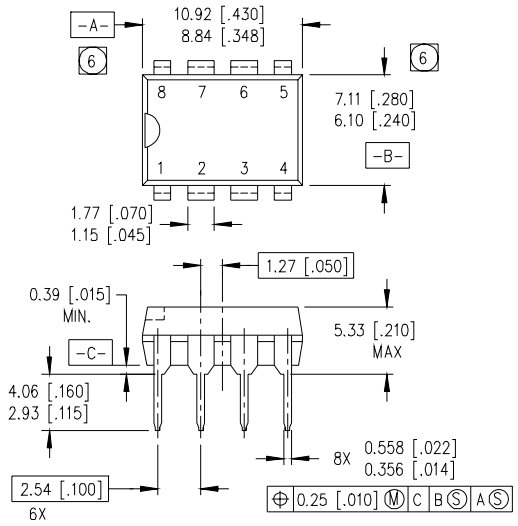
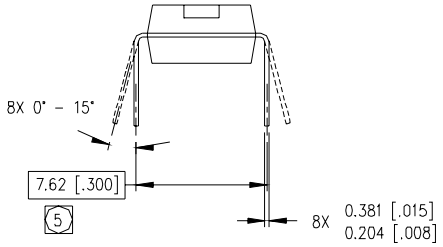


Figure 5. Switching Time Test Circuits

Caseoutline

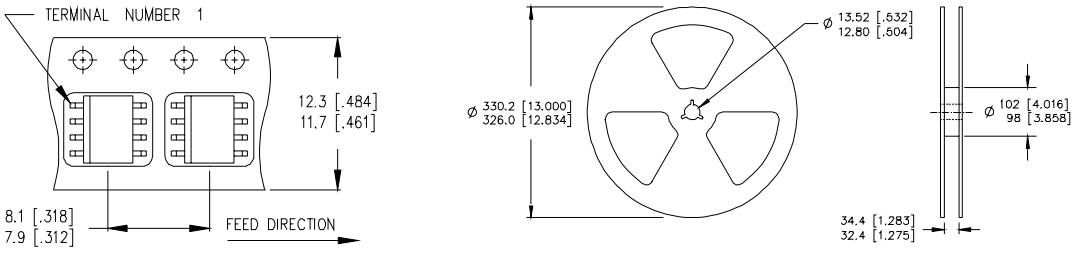


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



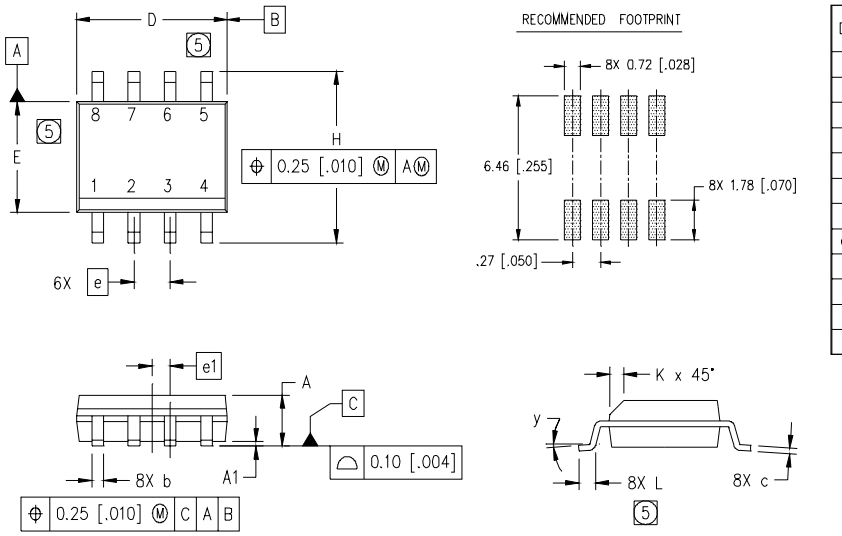
8 Lead PDIP 01-3003 01

Tape & Reel



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Case Outline - 8 Lead SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(MS-012AA) 01-0021 09

International
IOR Rectifier

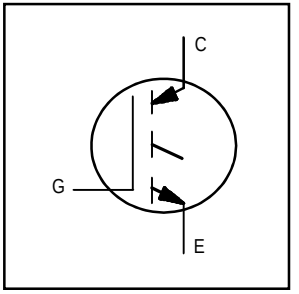
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd., Whyteleafe, Surrey CR3 0BL, United Kingdom
Tel: ++ 44 (0) 20 8645 8000
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171-0021 Tel: 8133 983 0086
IR HONG KONG: Unit 308, #F, New East Ocean Centre, No. 9 Science Museum Road, Tsimshatsui East, Kowloon
Hong Kong Tel: (852) 2803-7380

Data and specifications subject to change without notice. 11/13/2000

International
IOR Rectifier

IRG4CC10KB

IRG4CC10KB IGBT Die in Wafer Form



600 V
Size 1
Ultra-Fast Speed
Short Circuit Rated
6" Wafer

Electrical Characteristics (Wafer Form)

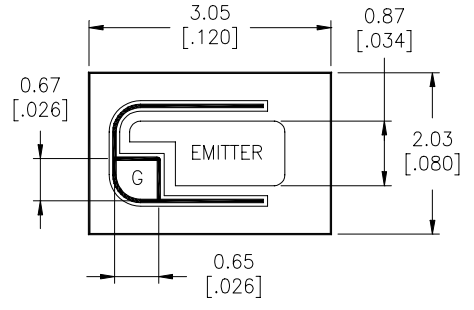
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 1.5A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.5V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	250µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1 kA-2kA-2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	.080" x .120"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5274
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4BC10K

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES:

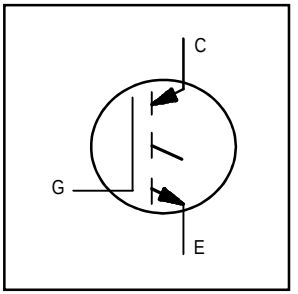
BONDING PADS:	< 0.635 TOLERANCE	= +/− 0.013
WIDTH	< [.0250] TOLERANCE	= +/− [.0005]
&	> 0.635 TOLERANCE	= +/− 0.025
LENGTH	> [.0250] TOLERANCE	= +/− [.0010]
OVERALL DIE:	< 1.270 TOLERANCE	= +/− 0.102
WIDTH	< [.050] TOLERANCE	= +/− [.004]
&	> 1.270 TOLERANCE	= +/− 0.203
LENGTH	> [.050] TOLERANCE	= +/− [.008]

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

IRG4CC10SB

IRG4CC10SB IGBT Die in Wafer Form



600 V
Size 1
Standard Speed
6" Wafer

Electrical Characteristics (Wafer Form)

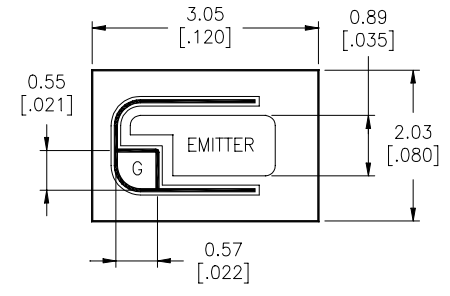
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 1.5A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	250µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NIV-Ag (1 kA-2kA-2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	.080" x .120"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5236
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4BC10S

Die Outline



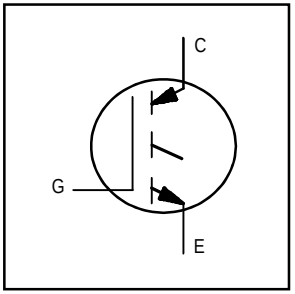
NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES:
   BONDING PADS: < 0.635 TOLERANCE = +/− 0.013
   WIDTH < [.0250] TOLERANCE = +/− [.0005]
   & > 0.635 TOLERANCE = +/− 0.025
   LENGTH > [.0250] TOLERANCE = +/− [.0010]
   OVERALL DIE: < 1.270 TOLERANCE = +/− 0.102
   WIDTH < [.050] TOLERANCE = +/− [.004]
   & > 1.270 TOLERANCE = +/− 0.203
   LENGTH > [.050] TOLERANCE = +/− [.008]
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

IRG4CC10UB

IRG4CC10UB IGBT Die in Wafer Form



600 V
Size 1
Ultra-Fast Speed
6" Wafer

Electrical Characteristics (Wafer Form)

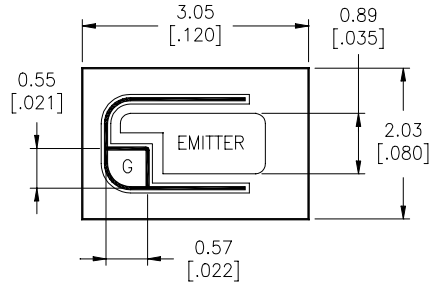
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 1.5A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	250µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1 kA-2kA-2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	.080" x .120"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5236
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4BC10U

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES:

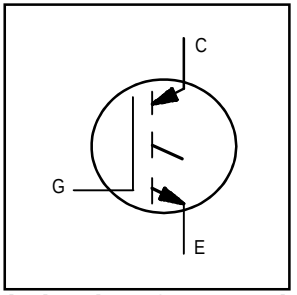
BONDING PADS:	< 0.635 TOLERANCE	= +/- 0.013
WIDTH	< [.0250] TOLERANCE	= +/- [.0005]
&	> 0.635 TOLERANCE	= +/- 0.025
LENGTH	> [.0250] TOLERANCE	= +/- [.0010]
OVERALL DIE:	< 1.270 TOLERANCE	= +/- 0.102
WIDTH	< [.050] TOLERANCE	= +/- [.004]
&	> 1.270 TOLERANCE	= +/- 0.203
LENGTH	> [.050] TOLERANCE	= +/- [.008]

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

IRG4CC20FB

IRG4CC20FB IGBT Die in Wafer Form



600 V
Size 2
Fast Speed
6" Wafer

Electrical Characteristics (Wafer Form)

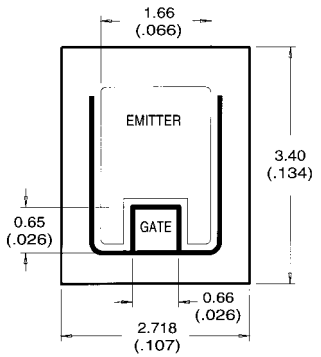
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 3.25A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	250 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1 kA-2kA-2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.107" x 0.134"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5228
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4BC20F

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE	= +/−	0.013
WIDTH	< (.0250) TOLERANCE	= +/−	(.0005)
&	> 0.635 TOLERANCE	= +/−	0.025
LENGTH	> (.0250) TOLERANCE	= +/−	(.0010)
OVERALL DIE:	< 1.270 TOLERANCE	= +/−	0.102
WIDTH	< (.050) TOLERANCE	= +/−	(.004)
&	> 1.270 TOLERANCE	= +/−	0.203
LENGTH	> (.050) TOLERANCE	= +/−	(.008)

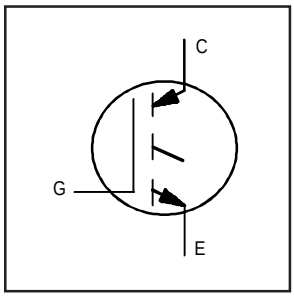
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

PD- 91824

International
IOR Rectifier

IRG4CC20KB

IRG4CC20KB IGBT Die in Wafer Form



600 V
Size 2
Ultra-Fast-Speed,
Short Circuit Rated
Speed
6" Wafer

Electrical Characteristics (Wafer Form)

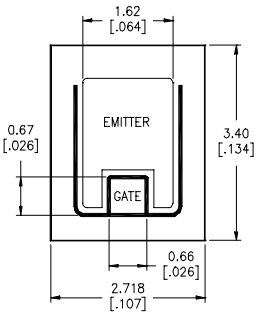
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 3.25A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.5V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	250µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1 kA-2kA-2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	.107" x .134"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5239
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4BC20K

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE	= +/- 0.013
WIDTH	< [.0250] TOLERANCE	= +/- [.0005]
&	> 0.635 TOLERANCE	= +/- 0.025
LENGTH	> [.0250] TOLERANCE	= +/- [.0010]
OVERALL DIE:	< 1.270 TOLERANCE	= +/- 0.102
WIDTH	< [.050] TOLERANCE	= +/- [.004]
&	> 1.270 TOLERANCE	= +/- 0.203
LENGTH	> [.050] TOLERANCE	= +/- [.008]

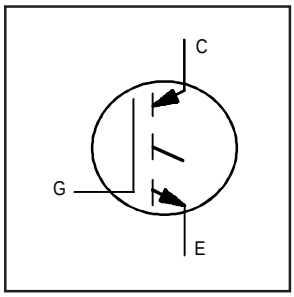
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

PD- 94049

International
IOR Rectifier

IRG4CC20MB

IRG4CC20MB IGBT Die in Wafer Form



600 V
Size 2
Fast-Speed,
Short Circuit Rated
6" Wafer

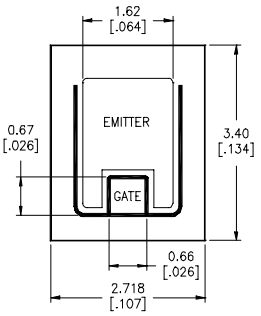
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	1.6V Max.	I_C = 3.25A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.0V Min., 6.5V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	100µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1 kA-2kA-2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	.107" x .134"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5239
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES:

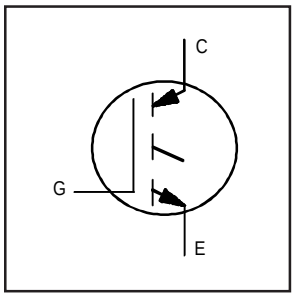
BONDING PADS:	< 0.635 TOLERANCE	= +/- 0.013
WIDTH	< [.0250] TOLERANCE	= +/- [.0005]
&	> 0.635 TOLERANCE	= +/- 0.025
LENGTH	> [.0250] TOLERANCE	= +/- [.0010]
OVERALL DIE:	< 1.270 TOLERANCE	= +/- 0.102
WIDTH	< [.050] TOLERANCE	= +/- [.004]
&	> 1.270 TOLERANCE	= +/- 0.203
LENGTH	> [.050] TOLERANCE	= +/- [.008]

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

IRG4CC20RB

IRG4CC20RB IGBT Die in Wafer Form



600 V
Size 2
Standard-Speed,
Short Circuit Rated
6" Wafer

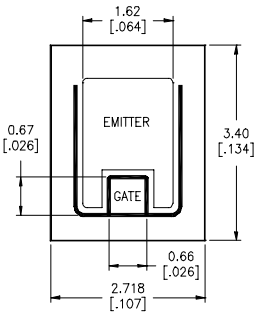
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\,(on)}$	Collector-to-Emitter Saturation Voltage	1.4V Max.	I_C = 3.25A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.0V Min., 6.5V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	100µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1 kA-2kA-2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	.107" x .134"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5239
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE	= +/− 0.013
WIDTH	< [.0250] TOLERANCE	= +/− [.0005]
&	> 0.635 TOLERANCE	= +/− 0.025
LENGTH	> [.0250] TOLERANCE	= +/− [.0010]
OVERALL DIE:	< 1.270 TOLERANCE	= +/− 0.102
WIDTH	< [.050] TOLERANCE	= +/− [.004]
&	> 1.270 TOLERANCE	= +/− 0.203
LENGTH	> [.050] TOLERANCE	= +/− [.008]

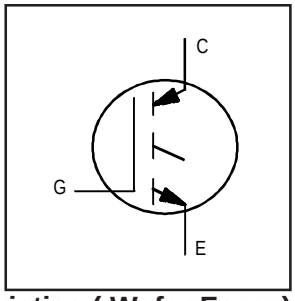
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

PD- 91757

International
IOR Rectifier

IRG4CC20UB

IRG4CC20UB IGBT Die in Wafer Form



600 V
Size 2
Ultra-Fast Speed
6" Wafer

Electrical Characteristics (Wafer Form)

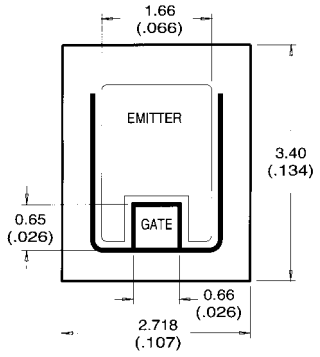
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1 kA-2kA-2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.107" x 0.134"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5228
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4BC20U

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:
   BONDING PADS: < 0.635 TOLERANCE = +/− 0.013
   WIDTH < (.0250) TOLERANCE = +/− (.0005)
   & > 0.635 TOLERANCE = +/− 0.025
   LENGTH > (.0250) TOLERANCE = +/− (.0010)

   OVERALL DIE: < 1.270 TOLERANCE = +/− 0.102
   WIDTH < (.050) TOLERANCE = +/− (.004)
   & > 1.270 TOLERANCE = +/− 0.203
   LENGTH > (.050) TOLERANCE = +/− (.008)
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

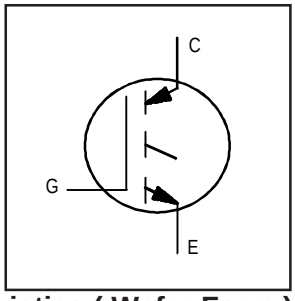
9/24/98

International
IOR Rectifier

PD- 91758

IRG4CC30FB

IRG4CC30FB IGBT Die in Wafer Form



600 V
Size 3
Fast Speed
6" Wafer

Electrical Characteristics (Wafer Form)

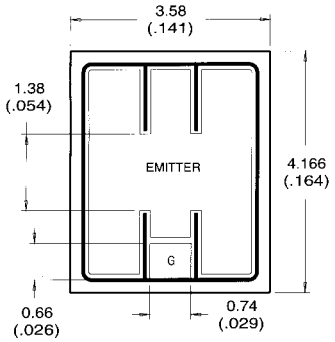
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1 kA-2kA-2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.141" x 0.164"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5225
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4BC30F

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:
   BONDING PADS: < 0.635 TOLERANCE = +/- 0.013
   WIDTH < (.0250) TOLERANCE = +/- (.0005)
   & > 0.635 TOLERANCE = +/- 0.025
   LENGTH > (.0250) TOLERANCE = +/- (.0010)

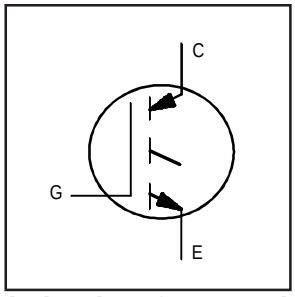
   OVERALL DIE: < 1.270 TOLERANCE = +/- 0.102
   WIDTH < (.050) TOLERANCE = +/- (.004)
   & > 1.270 TOLERANCE = +/- 0.203
   LENGTH > (.050) TOLERANCE = +/- (.008)
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

PD- 91759

IRG4CC30KB

IRG4CC30KB IGBT Die in Wafer Form



600 V
Size 3
Ultra-Fast Speed
6" Wafer

Electrical Characteristics (Wafer Form)

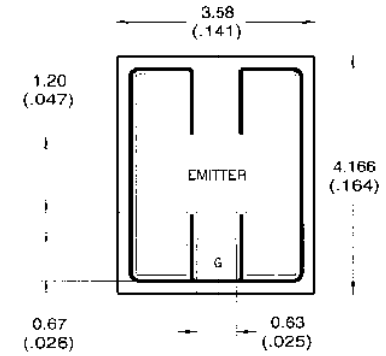
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.141" x 0.164"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5240
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions:	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PC30K

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE =	+/- 0.013
WIDTH	< (.0250)	TOLERANCE =	+/- (.0005)
&	> 0.635	TOLERANCE =	+/- 0.025
LENGTH	> (.0250)	TOLERANCE =	+/- (.0010)
OVERALL DIE:	< 1.270	TOLERANCE =	+/- 0.102
WIDTH	< (.050)	TOLERANCE =	+/- (.004)
&	> 1.270	TOLERANCE =	+/- 0.203
LENGTH	> (.050)	TOLERANCE =	+/- (.008)

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

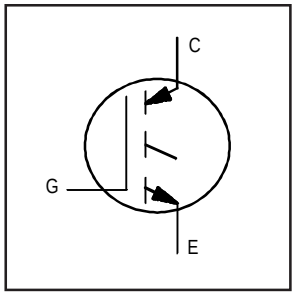
9/24/98

International
IOR Rectifier

PD- 91760

IRG4CC30SB

IRG4CC30SB IGBT Die in Wafer Form



600 V
Size 3
Standard Speed
6" Wafer

Electrical Characteristics (Wafer Form)

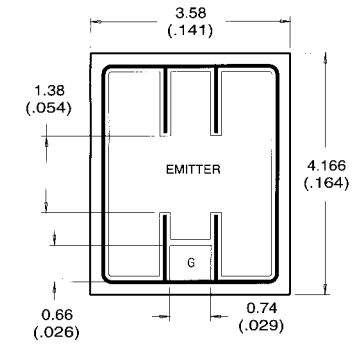
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1 kA-2kA-2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.141" x 0.164"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5225
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4BC30S

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:
   BONDING PADS: < 0.635 TOLERANCE = +/- 0.013
   WIDTH < (.0250) TOLERANCE = +/- (.0005)
   & > 0.635 TOLERANCE = +/- 0.025
   LENGTH > (.0250) TOLERANCE = +/- (.0010)

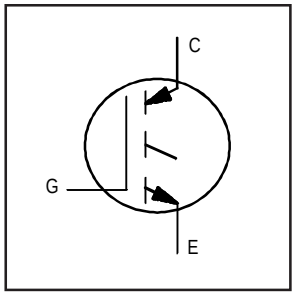
   OVERALL DIE: < 1.270 TOLERANCE = +/- 0.102
   WIDTH < (.050) TOLERANCE = +/- (.004)
   & > 1.270 TOLERANCE = +/- 0.203
   LENGTH > (.050) TOLERANCE = +/- (.008)
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

PD-91771

IRG4CC30UB

IRG4CC30UB IGBT Die in Wafer Form



600 V
Size 3
Ultra-Fast Speed
6" Wafer

Electrical Characteristics (Wafer Form)

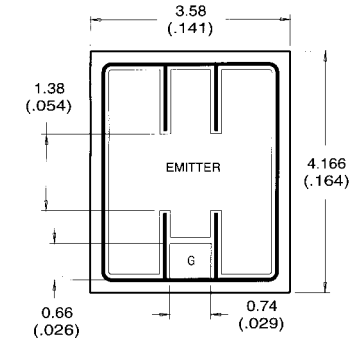
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1 kA-2kA-2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (3 microns)
Dimensions:	0.141" x 0.164"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5225
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : IRG4BC30U

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:
   BONDING PADS: < 0.635 TOLERANCE = +/- 0.013
   WIDTH < (.0250) TOLERANCE = +/- (.0005)
   & > 0.635 TOLERANCE = +/- 0.025
   LENGTH > (.0250) TOLERANCE = +/- (.0010)

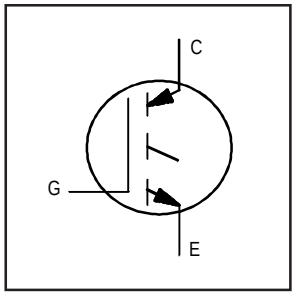
   OVERALL DIE: < 1.270 TOLERANCE = +/- 0.102
   WIDTH < (.050) TOLERANCE = +/- (.004)
   & > 1.270 TOLERANCE = +/- 0.203
   LENGTH > (.050) TOLERANCE = +/- (.008)
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

PD- 91761

IRG4CC40FB

IRG4CC40FB IGBT Die in Wafer Form



600 V
Size 4
Fast Speed
6" Wafer

Electrical Characteristics (Wafer Form)

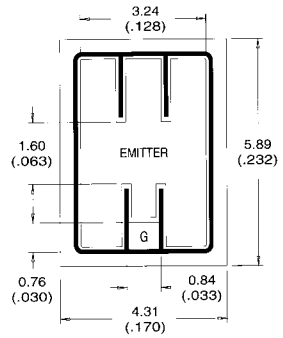
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min.,6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.170" x 0.232"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5219
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PC40F

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE =	+/- 0.013
WIDTH	< (.0250)	TOLERANCE =	+/- (.0005)
&	> 0.635	TOLERANCE =	+/- 0.025
LENGTH	> (.0250)	TOLERANCE =	+/- (.0010)
OVERALL DIE:	< 1.270	TOLERANCE =	+/- 0.102
WIDTH	< (.050)	TOLERANCE =	+/- (.004)
&	> 1.270	TOLERANCE =	+/- 0.203
LENGTH	> (.050)	TOLERANCE =	+/- (.008)

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

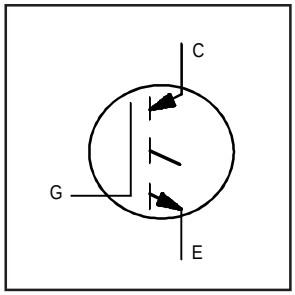
9/24/98

International
IOR Rectifier

PD-91772

IRG4CC40KB

IRG4CC40KB IGBT Die in Wafer Form



600 V
Size 4
Ultra-Fast Speed
6" Wafer

Electrical Characteristics (Wafer Form)

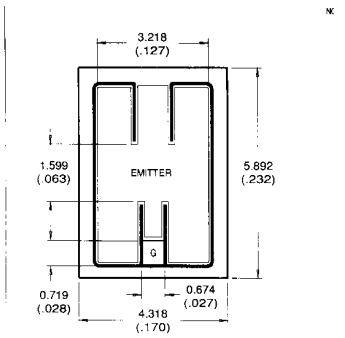
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.127" x 0.232"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5231
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions:	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PC40K

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE = +/− 0.013	
WIDTH	< (.0250) TOLERANCE = +/− (.0005)	
&	> 0.635 TOLERANCE = +/− 0.025	
LENGTH	> (.0250) TOLERANCE = +/− (.0010)	
OVERALL DIE:	< 1.270 TOLERANCE = +/− 0.102	
WIDTH	< (.050) TOLERANCE = +/− (.004)	
&	> 1.270 TOLERANCE = +/− 0.203	
LENGTH	> (.050) TOLERANCE = +/− (.008)	

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

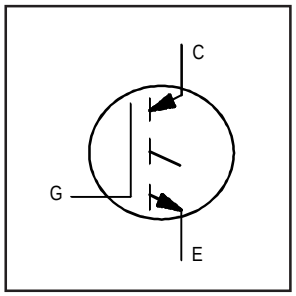
9/24/98

International
IOR Rectifier

PD- 93975

IRG4CC40RB

IRG4CC40RB IGBT Die in Wafer Form



600 V
Size 4
Standard Speed
Short Circuit Rated
6" Wafer

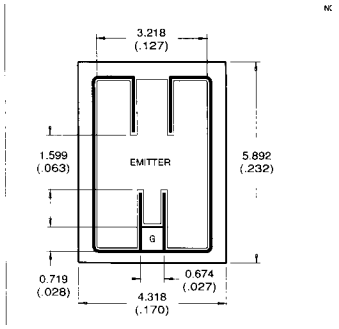
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	1.4V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.0V Min., 6.5V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	100 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.170" x 0.232"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5231
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions:	For optimum electrical results, die attach temperature should not exceed 300C

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

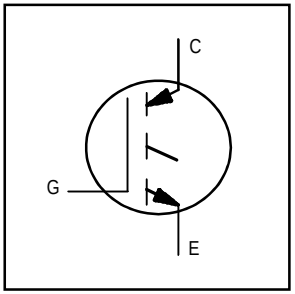
BONDING PADS:	< 0.635 TOLERANCE	= +/-	0.013
WIDTH	< (.0250) TOLERANCE	= +/-	(.0005)
&	> 0.635 TOLERANCE	= +/-	0.025
LENGTH	> (.0250) TOLERANCE	= +/-	(.0010)
OVERALL DIE:	< 1.270 TOLERANCE	= +/-	0.102
WIDTH	< (.050) TOLERANCE	= +/-	(.004)
&	> 1.270 TOLERANCE	= +/-	0.203
LENGTH	> (.050) TOLERANCE	= +/-	(.008)

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

IRG4CC40SB

IRG4CC40SB IGBT Die in Wafer Form



600 V
Size 4
Standard Speed
6" Wafer

Electrical Characteristics (Wafer Form)

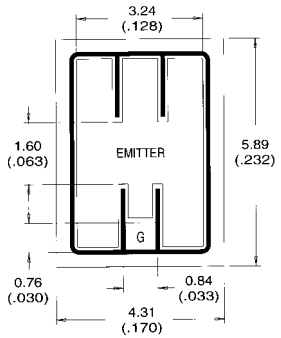
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min.,6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	250 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1kA-2kA-2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.170" x 0.232"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5219
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PC40S

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE	= +/-	0.013
WIDTH	< (.0250) TOLERANCE	= +/-	(.0005)
&	> 0.635 TOLERANCE	= +/-	0.025
LENGTH	> (.0250) TOLERANCE	= +/-	(.0010)
OVERALL DIE:	< 1.270 TOLERANCE	= +/-	0.102
WIDTH	< (.050) TOLERANCE	= +/-	(.004)
&	> 1.270 TOLERANCE	= +/-	0.203
LENGTH	> (.050) TOLERANCE	= +/-	(.008)

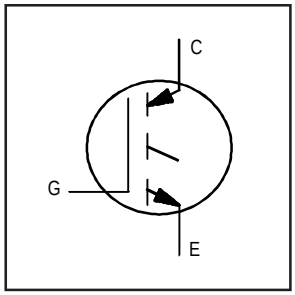
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

PD- 91762

IRG4CC40UB

IRG4CC40UB IGBT Die in Wafer Form



600 V
Size 4
Ultra-Fast Speed
6" Wafer

Electrical Characteristics (Wafer Form)

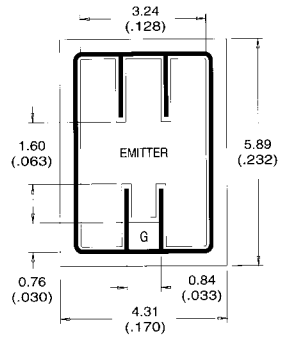
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min.,6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.170" x 0.232"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5219
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PC40U

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE =	+/− 0.013
WIDTH	< (.0250) TOLERANCE =	+/− (.0005)
&	> 0.635 TOLERANCE =	+/− 0.025
LENGTH	> (.0250) TOLERANCE =	+/− (.0010)
OVERALL DIE:	< 1.270 TOLERANCE =	+/− 0.102
WIDTH	< (.050) TOLERANCE =	+/− (.004)
&	> 1.270 TOLERANCE =	+/− 0.203
LENGTH	> (.050) TOLERANCE =	+/− (.008)

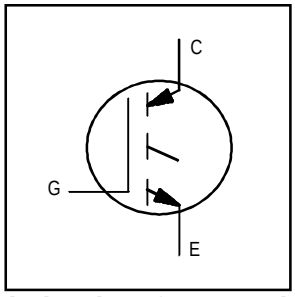
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

PD-94075

IRG4CC40WB

IRG4CC40WB IGBT Die in Wafer Form



600 V
Size 4
WARP Speed
6" Wafer

Electrical Characteristics (Wafer Form)

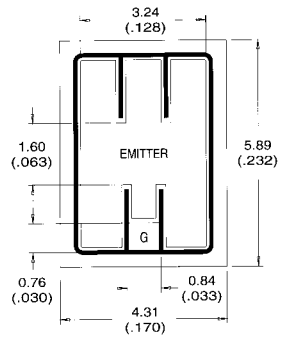
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	2.7V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min.,6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	250 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.170" x 0.232"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5219
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4CC40WB

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

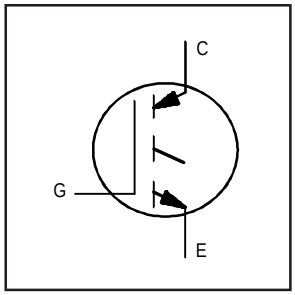
BONDING PADS:	< 0.635 TOLERANCE	= +/- 0.013
WIDTH	< (.0250) TOLERANCE	= +/- (.0005)
&	> 0.635 TOLERANCE	= +/- 0.025
LENGTH	> (.0250) TOLERANCE	= +/- (.0010)
OVERALL DIE:	< 1.270 TOLERANCE	= +/- 0.102
WIDTH	< (.050) TOLERANCE	= +/- (.004)
&	> 1.270 TOLERANCE	= +/- 0.203
LENGTH	> (.050) TOLERANCE	= +/- (.008)

International
IOR Rectifier

PD- 91828

IRG4CC50FB

IRG4CC50FB IGBT Die in Wafer Form



600 V
Size 5
Fast Speed
6" Wafer

Electrical Characteristics (Wafer Form)

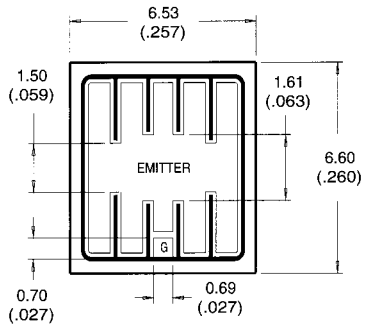
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	250 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1kA-2kA-.2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.257" x 0.260"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5226
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PC50F

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE	= +/-	0.013
WIDTH	< (.0250) TOLERANCE	= +/-	(.0005)
&	> 0.635 TOLERANCE	= +/-	0.025
LENGTH	> (.0250) TOLERANCE	= +/-	(.0010)
OVERALL DIE:	< 1.270 TOLERANCE	= +/-	0.102
WIDTH	< (.050) TOLERANCE	= +/-	(.004)
&	> 1.270 TOLERANCE	= +/-	0.203
LENGTH	> (.050) TOLERANCE	= +/-	(.008)

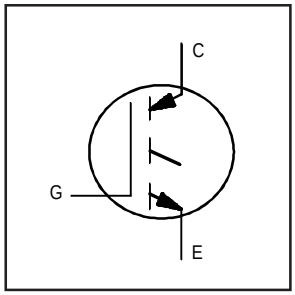
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

PD-91774

IRG4CC50KB

IRG4CC50KB IGBT Die in Wafer Form



600 V
Size 5
Ultra-Fast Speed
6" Wafer

Electrical Characteristics (Wafer Form)

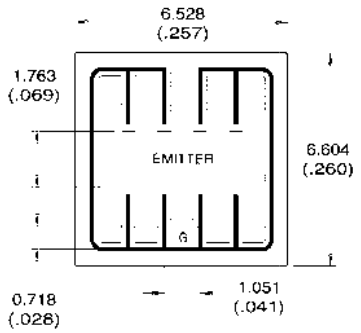
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.257" x 0.260"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5253
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions:	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PC50K

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:
   BONDING PADS: < 0.635 TOLERANCE = +/- 0.013
   WIDTH < (.0250) TOLERANCE = +/- (.0005)
   & > 0.635 TOLERANCE = +/- 0.025
   LENGTH > (.0250) TOLERANCE = +/- (.0010)

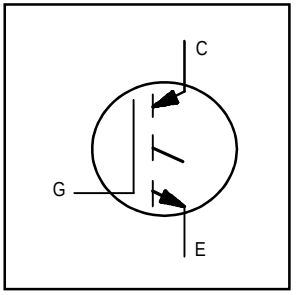
   OVERALL DIE: < 1.270 TOLERANCE = +/- 0.102
   WIDTH < (.050) TOLERANCE = +/- (.004)
   & > 1.270 TOLERANCE = +/- 0.203
   LENGTH > (.050) TOLERANCE = +/- (.008)
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

9/24/98

International
IOR Rectifier

IRG4CC50SB

IRG4CC50SB IGBT Die in Wafer Form



600 V
Size 5
Standard Speed
6" Wafer

Electrical Characteristics (Wafer Form)

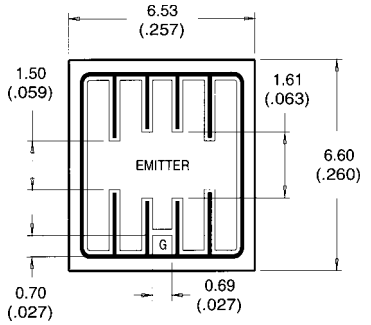
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	250 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1kA-2kA-.2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.257" x 0.260"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5226
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PC50S

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE	= +/−	0.013
WIDTH	< (.0250) TOLERANCE	= +/−	(.0005)
&	> 0.635 TOLERANCE	= +/−	0.025
LENGTH	> (.0250) TOLERANCE	= +/−	(.0010)
OVERALL DIE:	< 1.270 TOLERANCE	= +/−	0.102
WIDTH	< (.050) TOLERANCE	= +/−	(.004)
&	> 1.270 TOLERANCE	= +/−	0.203
LENGTH	> (.050) TOLERANCE	= +/−	(.008)

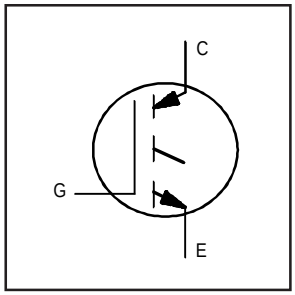
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

PD- 91764

IRG4CC50UB

IRG4CC50UB IGBT Die in Wafer Form



600 V
Size 5
Ultra-Fast Speed
6" Wafer

Electrical Characteristics (Wafer Form)

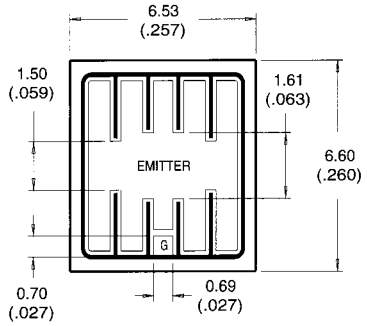
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-.2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.257" x 0.260"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5226
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PC50U

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE	= +/- 0.013
WIDTH	< (.0250) TOLERANCE	= +/- (.0005)
&	> 0.635 TOLERANCE	= +/- 0.025
LENGTH	> (.0250) TOLERANCE	= +/- (.0010)
OVERALL DIE:	< 1.270 TOLERANCE	= +/- 0.102
WIDTH	< (.050) TOLERANCE	= +/- (.004)
&	> 1.270 TOLERANCE	= +/- 0.203
LENGTH	> (.050) TOLERANCE	= +/- (.008)

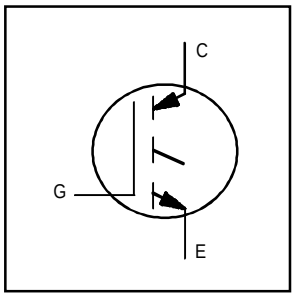
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

PD-91836A

International
IOR Rectifier

IRG4CC50WB

IRG4CC50WB IGBT Die in Wafer Form



600 V
Size 5
WARP Speed
6" Wafer

Electrical Characteristics (Wafer Form)

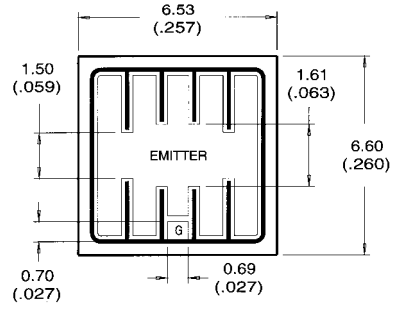
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	2.3V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	250 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1kA-2kA-.2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.257" x 0.260"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5226
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PC50W

Die Outline



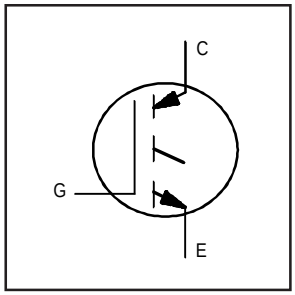
NOTES:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:
   BONDING PADS: < 0.635 TOLERANCE = +/- 0.013
   WIDTH < (.0250) TOLERANCE = +/- (.0005)
   & > 0.635 TOLERANCE = +/- 0.025
   LENGTH > (.0250) TOLERANCE = +/- (.0010)
   OVERALL DIE: < 1.270 TOLERANCE = +/- 0.102
   WIDTH < (.050) TOLERANCE = +/- (.004)
   & > 1.270 TOLERANCE = +/- 0.203
   LENGTH > (.050) TOLERANCE = +/- (.008)

PD-91870

International
IOR Rectifier

IRG4CC58KB

IRG4CC58KB IGBT Die in Wafer Form



600 V
Size 5.8
Ultra-Fast Speed
Short Circuit Rated
6" Wafer

Electrical Characteristics (Wafer Form)

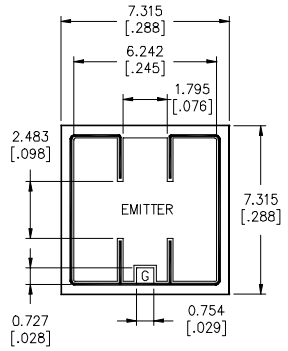
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\,(on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.5V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =1.0mA
I_{CES}	Zero Gate Voltage Collector Current	200 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-Ni V-Ag (1kA°-2kA°-2.5kA°)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	.288" x .288"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5348
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : N/A

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE	= +/- 0.013
WIDTH	< [.0250] TOLERANCE	= +/- [.0005]
&	> 0.635 TOLERANCE	= +/- 0.025
LENGTH	> [.0250] TOLERANCE	= +/- [.0010]
OVERALL DIE:	< 1.270 TOLERANCE	= +/- 0.102
WIDTH	< [.050] TOLERANCE	= +/- [.004]
&	> 1.270 TOLERANCE	= +/- 0.203
LENGTH	> [.050] TOLERANCE	= +/- [.008]

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

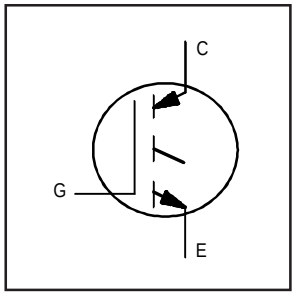
3/25/99

International
IOR Rectifier

PD- 91765

IRG4CC70UB

IRG4CC70UB IGBT Die in Wafer Form



600 V
Size 7
Ultra-Fast Speed
6" Wafer

Electrical Characteristics (Wafer Form)

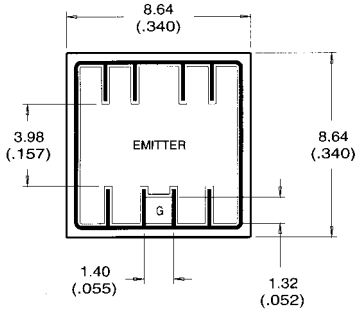
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-.2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.340" x 0.340"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5234
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PSC70U

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

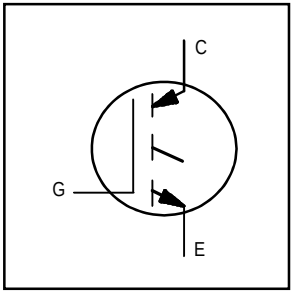
BONDING PADS:	< 0.635 TOLERANCE	= +/−	0.013
WIDTH	< (.0250) TOLERANCE	= +/−	(.0005)
&	> 0.635 TOLERANCE	= +/−	0.025
LENGTH	> (.0250) TOLERANCE	= +/−	(.0010)
OVERALL DIE:	< 1.270 TOLERANCE	= +/−	0.102
WIDTH	< (.050) TOLERANCE	= +/−	(.004)
&	> 1.270 TOLERANCE	= +/−	0.203
LENGTH	> (.050) TOLERANCE	= +/−	(.008)

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

IRG4CC71KB

IRG4CC71KB IGBT Die in Wafer Form



600 V
Size 7.1
Ultra-Fast Speed
Circuit Rated Rated
6" Wafer

Electrical Characteristics (Wafer Form)

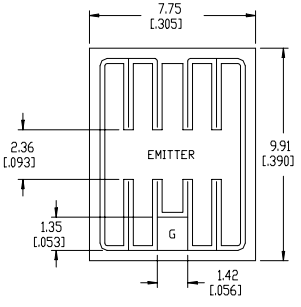
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.5V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1kA-2kA-.2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.305" x 0.390"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5271
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PSC71K

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE	= +/− 0.013
WIDTH	< [.0250] TOLERANCE	= +/− [.0005]
&	> 0.635 TOLERANCE	= +/− 0.025
LENGTH	> [.0250] TOLERANCE	= +/− [.0010]
OVERALL DIE:	< 1.270 TOLERANCE	= +/− 0.102
WIDTH	< [.050] TOLERANCE	= +/− [.004]
&	> 1.270 TOLERANCE	= +/− 0.203
LENGTH	> [.050] TOLERANCE	= +/− [.008]

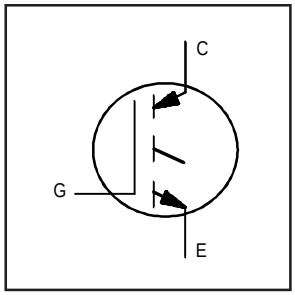
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

PD- 91868

IRG4CC72KB

IRG4CC72KB IGBT Die in Wafer Form



600 V
Size 7.2
Ultra-Fast Speed
Short Circuit Rated
6" Wafer

Electrical Characteristics (Wafer Form)

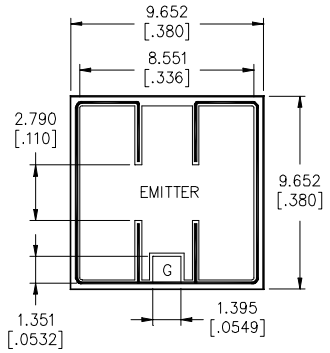
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\,(on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.5V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C = 1.0mA
I_{CES}	Zero Gate Voltage Collector Current	200 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1kA°-2kA°-2.5kA°)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	.380" x .380"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5349
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : N/A

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE =	+/- 0.013
WIDTH	< [.0250] TOLERANCE =	+/- [.0005]
&	> 0.635 TOLERANCE =	+/- 0.025
LENGTH	> [.0250] TOLERANCE =	+/- [.0010]
OVERALL DIE:	< 1.270 TOLERANCE =	+/- 0.102
WIDTH	< [.050] TOLERANCE =	+/- [.004]
&	> 1.270 TOLERANCE =	+/- 0.203
LENGTH	> [.050] TOLERANCE =	+/- [.008]

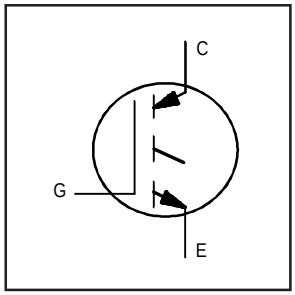
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

PD-91867

International
IOR Rectifier

IRG4CC77KB

IRG4CC77KB IGBT Die in Wafer Form



600 V
Size 7.7
Ultra-Fast Speed
Short Circuit Rated
6" Wafer

Electrical Characteristics (Wafer Form)

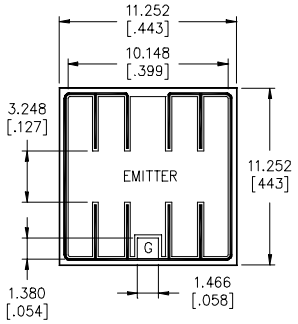
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\,(on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.5V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =1.0mA
I_{CES}	Zero Gate Voltage Collector Current	200 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-Ni V-Ag (1kA-2kA-.2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	.443" x .443"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5248
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : N/A

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/-	0.013
WIDTH	< [.0250]	TOLERANCE = +/-	[.0005]
&	> 0.635	TOLERANCE = +/-	0.025
LENGTH	> [.0250]	TOLERANCE = +/-	[.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/-	0.102
WIDTH	< [.050]	TOLERANCE = +/-	[.004]
&	> 1.270	TOLERANCE = +/-	0.203
LENGTH	> [.050]	TOLERANCE = +/-	[.008]

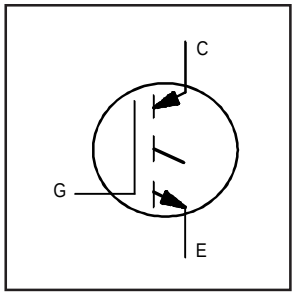
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

PD- 91875

IRG4CC81KB

IRG4CC81KB IGBT Die in Wafer Form



600 V
Size 8.1
Ultra-Fast Speed
Short Circuit Rated
6" Wafer

Electrical Characteristics (Wafer Form)

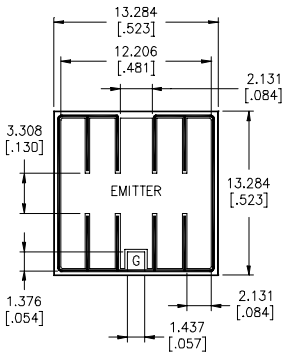
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\,(on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.5V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C = 1.0mA
I_{CES}	Zero Gate Voltage Collector Current	200 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1kA°-2kA°-2.5kA°)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	.523" x .523"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5351
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : N/A

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/−	0.013
WIDTH	< [.0250]	TOLERANCE = +/−	[.0005]
&	> 0.635	TOLERANCE = +/−	0.025
LENGTH	> [.0250]	TOLERANCE = +/−	[.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/−	0.102
WIDTH	< [.050]	TOLERANCE = +/−	[.004]
&	> 1.270	TOLERANCE = +/−	0.203
LENGTH	> [.050]	TOLERANCE = +/−	[.008]

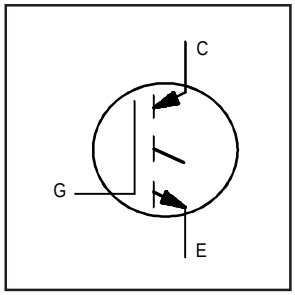
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

PD-91773

IRG4CC81UB

IRG4CC81UB IGBT Die in Wafer Form



600 V
Size 8.1
Ultra-Fast Speed
6" Wafer

Electrical Characteristics (Wafer Form)

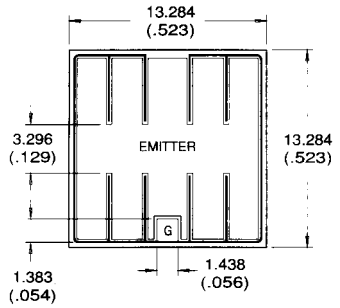
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-.2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.523" x 0.523"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5249
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : GA200TS60U

Die Outline



NOTES:

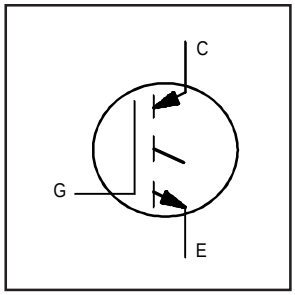
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES:
   BONDING PADS: < 0.635 TOLERANCE = +/- 0.013
   WIDTH < (.0250) TOLERANCE = +/- (.0005)
   & < 0.635 TOLERANCE = +/- 0.025
   LENGTH < (.0250) TOLERANCE = +/- (.0010)
   OVERALL DIE: < 1.270 TOLERANCE = +/- 0.102
   WIDTH < (.050) TOLERANCE = +/- (.004)
   & < 0.635 TOLERANCE = +/- 0.203
   LENGTH < (.050) TOLERANCE = +/- (.008)
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

PD- 91869

IRG4CC88KB

IRG4CC88KB IGBT Die in Wafer Form



600 V
Size 8.8
Ultra-Fast Speed
Short Circuit Rated
6" Wafer

Electrical Characteristics (Wafer Form)

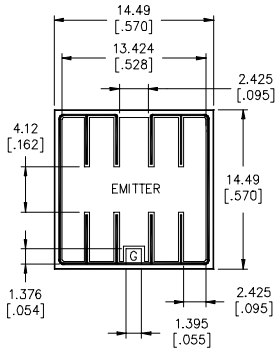
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\,(on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	600V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.5V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C = 1.0mA
I_{CES}	Zero Gate Voltage Collector Current	200 µA Max.	T_J = 25°C, V_{CE} = 600V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1kA°-2kA°-2.5kA°)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	.5705" x .5705"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5347
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : N/A

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE =	+/- 0.013
WIDTH	< [.0250] TOLERANCE =	+/- [.0005]
&	> 0.635 TOLERANCE =	+/- 0.025
LENGTH	> [.0250] TOLERANCE =	+/- [.0010]
OVERALL DIE:	< 1.270 TOLERANCE =	+/- 0.102
WIDTH	< [.050] TOLERANCE =	+/- [.004]
&	> 1.270 TOLERANCE =	+/- 0.203
LENGTH	> [.050] TOLERANCE =	+/- [.008]

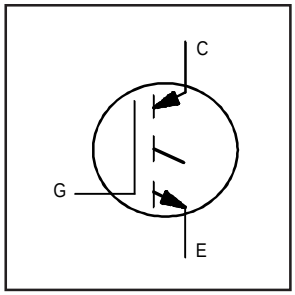
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

PD- 91766

IRG4CH20KB

IRG4CH20KB IGBT Die in Wafer Form



1200 V
Size 2
Ultra Fast Speed
Short Circuit Rated
6" Wafer

Electrical Characteristics (Wafer Form)

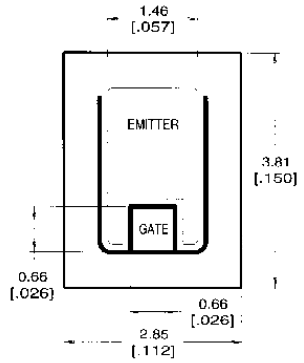
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 5.5A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-.2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.112" x 0.150"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5266
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PH20K (When available)

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE =	+/- 0.013
WIDTH	< (.0250)	TOLERANCE =	+/- (.0005)
&	> 0.635	TOLERANCE =	+/- 0.025
LENGTH	> (.0250)	TOLERANCE =	+/- (.0010)
OVERALL DIE:	< 1.270	TOLERANCE =	+/- 0.102
WIDTH	< (.050)	TOLERANCE =	+/- (.004)
&	> 1.270	TOLERANCE =	+/- 0.203
LENGTH	> (.050)	TOLERANCE =	+/- (.008)

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

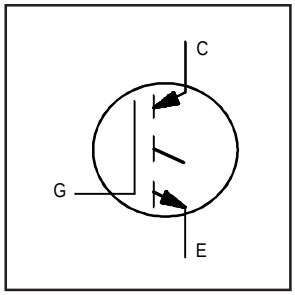
9/24/98

International
IOR Rectifier

PD-91767

IRG4CH30KB

IRG4CH30KB IGBT Die in Wafer Form



1200 V
Size 3
Ultra Fast Speed
Short Circuit Rated
6" Wafer

Electrical Characteristics (Wafer Form)

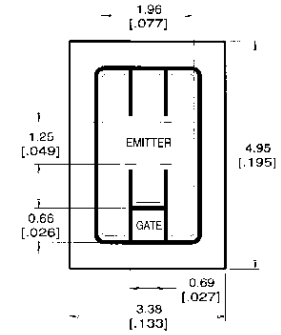
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-.2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.133" x 0.195"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5267
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PH30K (When available)

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

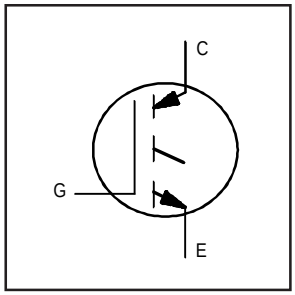
BONDING PADS:	< 0.635 TOLERANCE	= +/-	0.013
WIDTH	< (.0250) TOLERANCE	= +/-	(.0005)
&	> 0.635 TOLERANCE	= +/-	0.025
LENGTH	> (.0250) TOLERANCE	= +/-	(.0010)
OVERALL DIE:	< 1.270 TOLERANCE	= +/-	0.102
WIDTH	< (.050) TOLERANCE	= +/-	(.004)
&	> 1.270 TOLERANCE	= +/-	0.203
LENGTH	> (.050) TOLERANCE	= +/-	(.008)

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

IRG4CH40KB

IRG4CH40KB IGBT Die in Wafer Form



1200 V
Size 4
Ultra Fast Speed
Short Circuit Rated
6" Wafer

Electrical Characteristics (Wafer Form)

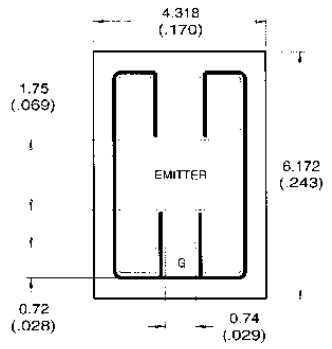
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-.2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.170" x 0.243"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5243
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PH40K (When available)

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

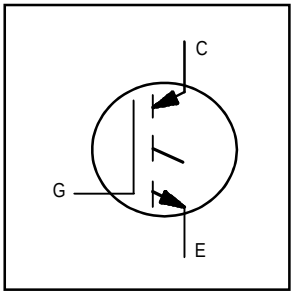
BONDING PADS:	< 0.635 TOLERANCE	= +/−	0.013
WIDTH	< (.0250) TOLERANCE	= +/−	(.0005)
&	> 0.635 TOLERANCE	= +/−	0.025
LENGTH	> (.0250) TOLERANCE	= +/−	(.0010)
OVERALL DIE:	< 1.270 TOLERANCE	= +/−	0.102
WIDTH	< (.050) TOLERANCE	= +/−	(.004)
&	> 1.270 TOLERANCE	= +/−	0.203
LENGTH	> (.050) TOLERANCE	= +/−	(.008)

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

IRG4CH40SB

IRG4CH40SB IGBT Die in Wafer Form



1200 V
Size 4
Standard Speed
6" Wafer

Electrical Characteristics (Wafer Form)

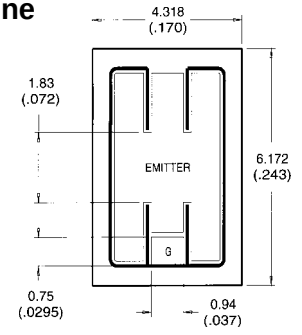
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	1200V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Nominal Backmetal Composition, Thickness:	Cr-NiV-Ag (1kA-2kA-2.5kA)
Nominal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.170" x 0.243"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5242
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PH40S

Die Outline



NOTES:

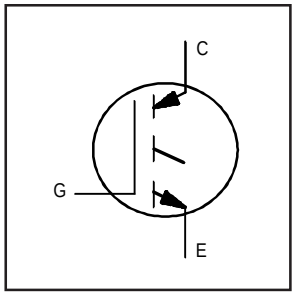
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES:
   BONDING PADS: < 0.635 TOLERANCE = +/- 0.013
   WIDTH < (.0250) TOLERANCE = +/- (.0005)
   & < 0.635 TOLERANCE = +/- 0.025
   LENGTH < (.0250) TOLERANCE = +/- (.0010)
   OVERALL DIE: < 1.270 TOLERANCE = +/- 0.102
   WIDTH < (.050) TOLERANCE = +/- (.004)
   & < 0.635 TOLERANCE = +/- 0.203
   LENGTH < (.050) TOLERANCE = +/- (.008)
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

PD- 91769

IRG4CH40UB

IRG4CH40UB IGBT Die in Wafer Form



1200 V
Size 4
Ultra-Fast Speed
6" Wafer

Electrical Characteristics (Wafer Form)

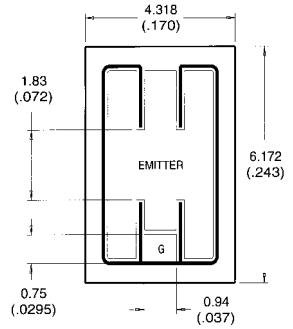
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	1200V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-.2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.170" x 0.243"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5242
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PH40U

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

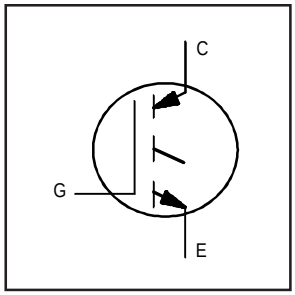
BONDING PADS:	< 0.635 TOLERANCE	= +/- 0.013
WIDTH	< (.0250) TOLERANCE	= +/- (.0005)
&	> 0.635 TOLERANCE	= +/- 0.025
LENGTH	> (.0250) TOLERANCE	= +/- (.0010)
OVERALL DIE:	< 1.270 TOLERANCE	= +/- 0.102
WIDTH	< (.050) TOLERANCE	= +/- (.004)
&	> 1.270 TOLERANCE	= +/- 0.203
LENGTH	> (.050) TOLERANCE	= +/- (.008)

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

IRG4CH50KB

IRG4CH50KB IGBT Die in Wafer Form



1200 V
Size 5
Ultra Fast Speed
Short Circuit Rated
6" Wafer

Electrical Characteristics (Wafer Form)

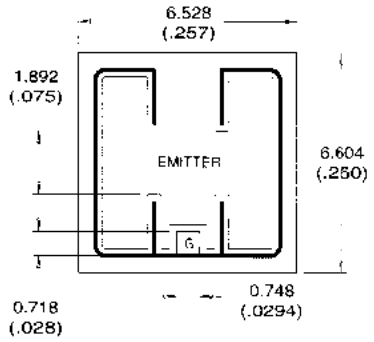
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-.2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.257" x 0.260"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5254
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PH50K (When available)

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE	= +/- 0.013
WIDTH	< (.0250) TOLERANCE	= +/- (.0005)
&	> 0.635 TOLERANCE	= +/- 0.025
LENGTH	> (.0250) TOLERANCE	= +/- (.0010)
OVERALL DIE:	< 1.270 TOLERANCE	= +/- 0.102
WIDTH	< (.050) TOLERANCE	= +/- (.004)
&	> 1.270 TOLERANCE	= +/- 0.203
LENGTH	> (.050) TOLERANCE	= +/- (.008)

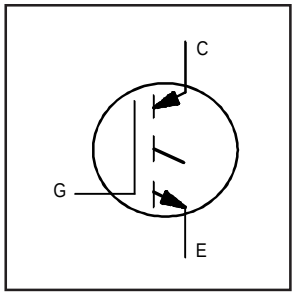
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

PD-91770

IRG4CH50SB

IRG4CH50SB IGBT Die in Wafer Form



1200 V
Size 5
Standard Speed
6" Wafer

Electrical Characteristics (Wafer Form)

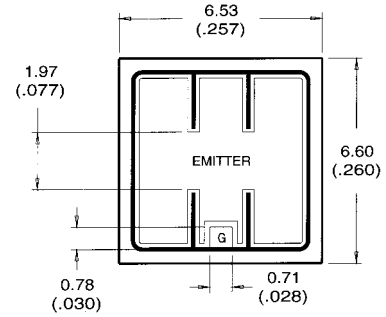
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-.2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.257" x 0.260"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5227
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Reference Standard IR packaged part (for design) : IRG4PH50SB (When available)

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE	= +/- 0.013
WIDTH	< (.0250) TOLERANCE	= +/- (.0005)
&	> 0.635 TOLERANCE	= +/- 0.025
LENGTH	> (.0250) TOLERANCE	= +/- (.0010)
OVERALL DIE:	< 1.270 TOLERANCE	= +/- 0.102
WIDTH	< (.050) TOLERANCE	= +/- (.004)
&	> 1.270 TOLERANCE	= +/- 0.203
LENGTH	> (.050) TOLERANCE	= +/- (.008)

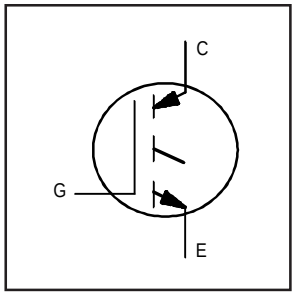
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

International
IOR Rectifier

PD-91775

IRG4CH50UB

IRG4CH50UB IGBT Die in Wafer Form



1200 V
Size 5
Ultra-Fast Speed
6" Wafer

Electrical Characteristics (Wafer Form)

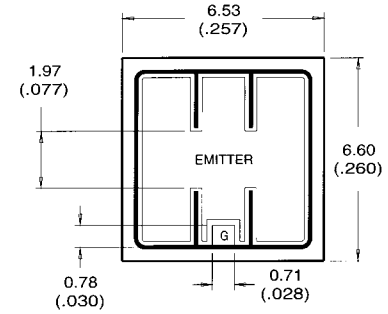
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	4.5V Max.	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	1200V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	300 µA Max.	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 11 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni / V-Ag (1kA-2kA-.2.5kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.257" x 0.260"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5227
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : IRG4PH50U

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: (INCH).
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE =	+/- 0.013
WIDTH	< (.0250) TOLERANCE =	+/- (.0005)
&	> 0.635 TOLERANCE =	+/- 0.025
LENGTH	> (.0250) TOLERANCE =	+/- (.0010)
OVERALL DIE:	< 1.270 TOLERANCE =	+/- 0.102
WIDTH	< (.050) TOLERANCE =	+/- (.004)
&	> 1.270 TOLERANCE =	+/- 0.203
LENGTH	> (.050) TOLERANCE =	+/- (.008)

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

PD - 94314

International
IOR Rectifier

IRGC5B120KB

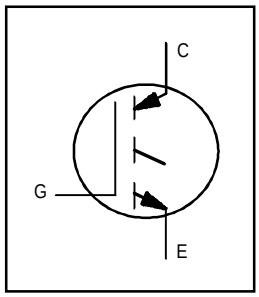
IRGC5B120KB IGBT Die in Wafer Form

Features

- GEN5 Non Punch Through (NPT) Technology
- Low $V_{CE(on)}$
- 10µs Short Circuit Capability
- Square RBSOA
- Positive $V_{CE(on)}$ Temperature Coefficient

Benefits

- Benchmark Efficiency for Motor Control
- Rugged Transient Performance
- Excellent Current Sharing in Parallel Operation
- Qualified for Industrial Market



1200 V
$I_{C(nom)}$ = 5A
VCE(on) typ. = 2.55V @
$I_{C(nom)}$ @ 25°C
Motor Control IGBT
Short Circuit Rated
150mm Wafer

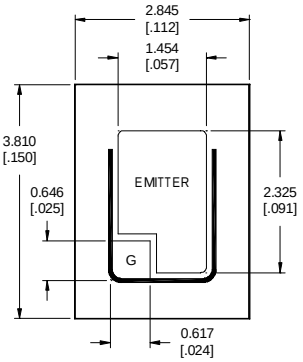
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	1.79V Min., 2.22V Max.	I_C = 2.5A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200V Min.	T_J = 25°C, I_{CES} = 100µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.4V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =125µA
I_{CES}	Zero Gate Voltage Collector Current	5.0 µA Max.	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Al-Ti-NiV-Ag (1kA-1kA-4kA-6kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.112" x 0.150"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	185 +/- 15 Microns
Relevant Die Mechanical Dwg. Number	01-5430
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

PD - 94315

International
IOR Rectifier

IRGC5B120UB

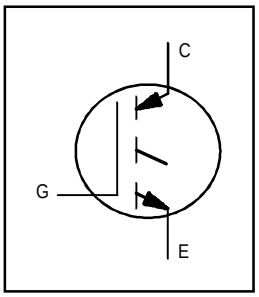
IRGC5B120UB IGBT Die in Wafer Form

Features

- GEN5 Non Punch Through (NPT) Technology
- UltraFast
- 10µs Short Circuit Capability
- Square RBSOA
- Positive $V_{CE(on)}$ Temperature Coefficient

Benefits

- Benchmark Efficiency above 20KHz
- Optimized for Welding, UPS, and Induction Heating
- Rugged with UltraFast Performance
- Excellent Current Sharing in Parallel Operation
- Qualified for Industrial Market



1200 V
$I_{C(nom)}$ = 5A
VCE(on) typ. = 4.01V @
$I_{C(nom)}$ @ 25°C
UltraFast IGBT
Short Circuit Rated
150mm Wafer

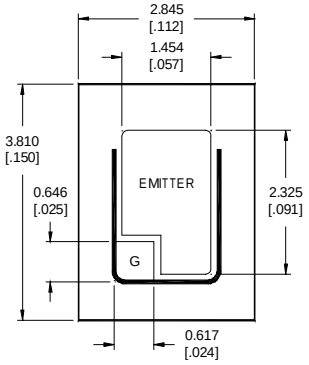
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	2.54V Min., 3.64V Max.	I_C = 2.5A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200V Min.	T_J = 25°C, I_{CES} = 100µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.4V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =125µA
I_{CES}	Zero Gate Voltage Collector Current	5.0 µA Max.	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Al-Ti-NiV-Ag (1kA-1kA-4kA-6kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.112" x 0.150"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	185 +/- 15 Microns
Relevant Die Mechanical Dwg. Number	01-5428
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

International
IOR Rectifier

PD - 94316

IRGC8B120KB

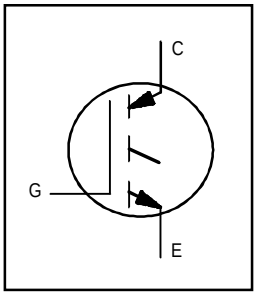
IRGC8B120KB IGBT Die in Wafer Form

Features

- GEN5 Non Punch Through (NPT) Technology
- Low $V_{CE(on)}$
- 10µs Short Circuit Capability
- Square RBSOA
- Positive $V_{CE(on)}$ Temperature Coefficient

Benefits

- Benchmark Efficiency for Motor Control
- Rugged Transient Performance
- Excellent Current Sharing in Parallel Operation
- Qualified for Industrial Market



1200 V
$I_{C(nom)}$ = 8A
VCE(on) typ. = 2.32V @
$I_{C(nom)}$ @ 25°C
Motor Control IGBT
Short Circuit Rated
150mm Wafer

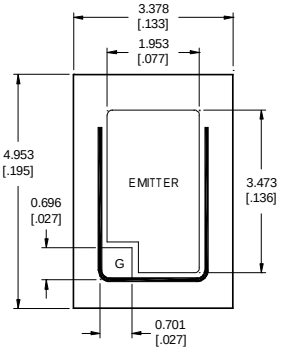
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	1.83V MIn., 2.27V Max.	I_C = 5.0A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200V Min.	T_J = 25°C, I_{CES} = 100µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.4V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =125µA
I_{CES}	Zero Gate Voltage Collector Current	5.0 µA Max.	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Al-Ti-NiV-Ag (1kA-1kA-4kA-6kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.133" x 0.195"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	185 +/- 15 Microns
Relevant Die Mechanical Dwg. Number	01-5429
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

PD-94317

International
IOR Rectifier

IRGC8B120UB

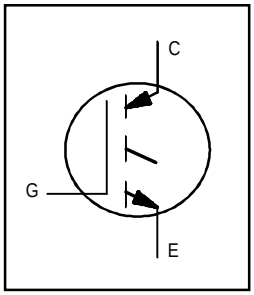
IRGC8B120UB IGBT Die in Wafer Form

Features

- GEN5 Non Punch Through (NPT) Technology
- UltraFast
- 10µs Short Circuit Capability
- Square RBSOA
- Positive $V_{CE(on)}$ Temperature Coefficient

Benefits

- Benchmark Efficiency above 20KHz
- Optimized for Welding, UPS, and Induction Heating
- Rugged with UltraFast Performance
- Excellent Current Sharing in Parallel Operation
- Qualified for Industrial Market



1200 V
$I_{C(nom)}$ = 8A
VCE(on) typ. = 3.63V @
$I_{C(nom)}$ @ 25°C
UltraFast IGBT
Short Circuit Rated
150mm Wafer

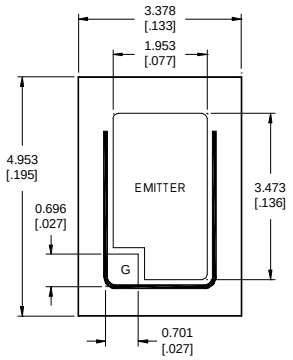
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	2.77V Min., 3.82V Max.	I_C = 5.0A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200V Min.	T_J = 25°C, I_{CES} = 100µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.4V Min., 6.0V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =125µA
I_{CES}	Zero Gate Voltage Collector Current	5.0 µA Max.	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1 µA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Al-Ti-NiV-Ag (1kA-1kA-4kA-6kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (4 microns)
Dimensions:	0.133" x 0.195"
Wafer Diameter:	150mm, with std. < 100 > flat
Wafer thickness:	185 +/- 15 Microns
Relevant Die Mechanical Dwg. Number	01-5427
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300C

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

PD - 93866

International
IOR Rectifier

IRGC15B120KB

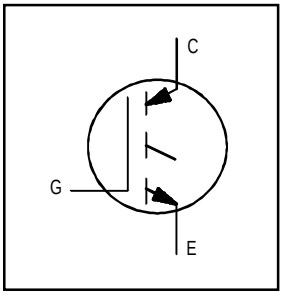
Die in Wafer Form

Features

- GEN5 Non Punch Through (NPT) Technology
- Low $V_{CE(on)}$
- 10µs Short Circuit Capability
- Square RBSOA
- Positive $V_{CE(on)}$ Temperature Coefficient

Benefits

- Benchmark Efficiency for Motor Control Applications
- Rugged Transient Performance
- Excellent Current Sharing in Parallel Operation



1200V
$I_{C(nom)}$=15A
$V_{CE(on)\,typ.}$=2.46V @
$I_{C(nom)}$ @ 25°C
Motor Control IGBT
Short Circuit Rated
150mm Wafer

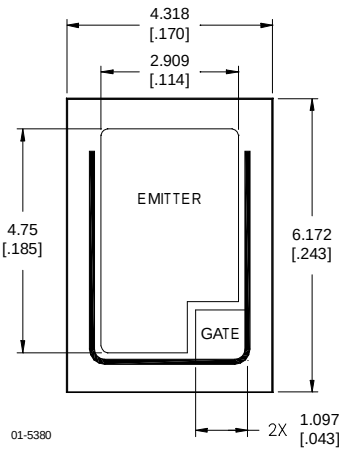
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (min, max)	Test Conditions
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	1.85V min, 2.3V max	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	1200V min	T_J = 25°C, I_{CES} = 125µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.4V min, 6.0V max	V_{GE} = V_{CE} , T_J =25°C, I_C = 125µA
I_{CES}	Zero Gate Voltage Collector Current	7µA max	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1µA max	T_J = 25°C, V_{GE} = +/-20V

Mechanical Data

Nominal Backmetal Composition, (Thickness)	Al - Ti - Ni/V - Ag, (1kA - 1kA - 4kA - 6kA)
Nominal Front Metal Composition, (Thickness)	99% Al/1% Si, (4µm)
Dimensions	0.170" x 0.243"
Wafer Diameter	150mm, with std. < 100 > flat
Wafer Thickness, Tolerance	185µm, +/-15µm
Relevant Die Mechanical Dwg. Number	01-5380
Minimum Street Width	100µm
Reject Ink Dot Size	0.25mm diameter minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300°C

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:
   BONDING PADS: < 0.635 TOLERANCE = +/- 0.013
   WIDTH < [.0250] TOLERANCE = +/- [.0005]
   & > 0.635 TOLERANCE = +/- 0.025
   LENGTH > [.0250] TOLERANCE = +/- [.0010]

   OVERALL DIE: < 1.270 TOLERANCE = +/- 0.102
   WIDTH < [.050] TOLERANCE = +/- [.004]
   & > 1.270 TOLERANCE = +/- 0.203
   LENGTH > [.050] TOLERANCE = +/- [.008]

PD - 93865

International
IOR Rectifier

IRGC15B120UB

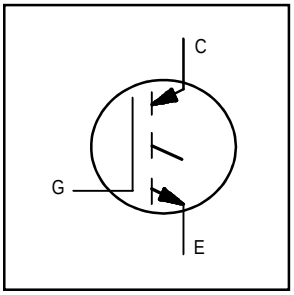
Die in Wafer Form

Features

- GEN5 Non Punch Through (NPT) Technology
- UltraFast
- 10µs Short Circuit Capability
- Square RBSOA
- Positive $V_{CE(on)}$ Temperature Coefficient

Benefits

- Benchmark Efficiency above 20KHz
- Optimized for Welding, UPS, and Induction Heating
- Rugged with UltraFast Performance
- Excellent Current Sharing in Parallel Operation



1200V
$I_{C(nom)}$=15A
$V_{CE(on)\,typ.}$=3.67V @
$I_{C(nom)}$ @ 25°C
UltraFast IGBT
Short Circuit Rated
150mm Wafer

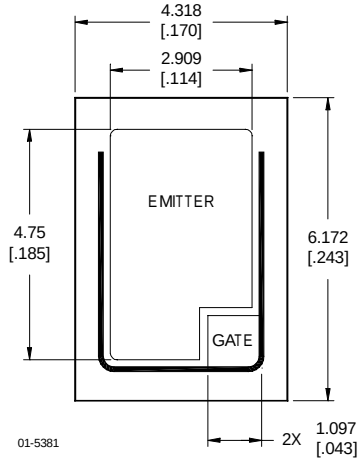
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (min, max)	Test Conditions
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	2.85V min, 3.45V max	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	1200V min	T_J = 25°C, I_{CES} = 125µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.4V min, 6.0V max	V_{GE} = V_{CE} , T_J =25°C, I_C = 125µA
I_{CES}	Zero Gate Voltage Collector Current	7µA max	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1µA max	T_J = 25°C, V_{GE} = +/-20V

Mechanical Data

Nominal Backmetal Composition, (Thickness)	Al - Ti - Ni/V - Ag, (1kA - 1kA - 4kA - 6kA)
Nominal Front Metal Composition, (Thickness)	99% Al/1% Si, (4µm)
Dimensions	0.170" x 0.243"
Wafer Diameter	150mm, with std. < 100 > flat
Wafer Thickness, Tolerance	185µm, +/-15µm
Relevant Die Mechanical Dwg. Number	01-5381
Minimum Street Width	100µm
Reject Ink Dot Size	0.25mm diameter minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300°C

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE =	+/- 0.013
WIDTH	< [.0250] TOLERANCE =	+/- [.0005]
&	> 0.635 TOLERANCE =	+/- 0.025
LENGTH	> [.0250] TOLERANCE =	+/- [.0010]
OVERALL DIE:	< 1.270 TOLERANCE =	+/- 0.102
WIDTH	< [.050] TOLERANCE =	+/- [.004]
&	> 1.270 TOLERANCE =	+/- 0.203
LENGTH	> [.050] TOLERANCE =	+/- [.008]

PD - 93868

International
IOR Rectifier

IRGC25B120KB

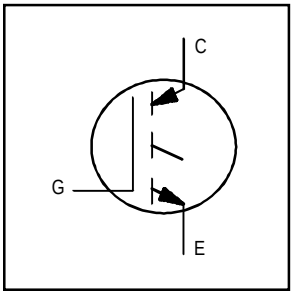
Die in Wafer Form

Features

- GEN5 Non Punch Through (NPT) Technology
- Low $V_{CE(on)}$
- 10µs Short Circuit Capability
- Square RBSOA
- Positive $V_{CE(on)}$ Temperature Coefficient

Benefits

- Benchmark Efficiency for Motor Control Applications
- Rugged Transient Performance
- Excellent Current Sharing in Parallel Operation



1200V
$I_{C(nom)}$=25A
$V_{CE(on)\,typ.}$=2.28V @
$I_{C(nom)}$ @ 25°C
Motor Control IGBT
Short Circuit Rated
150mm Wafer

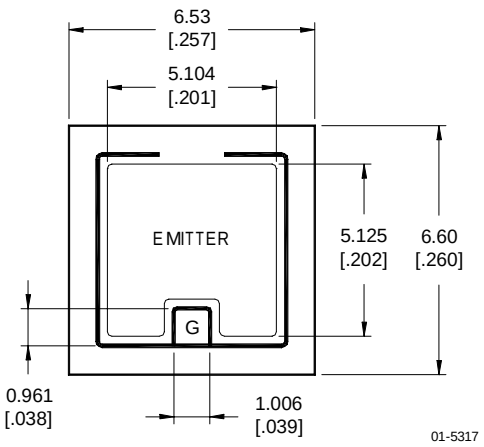
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (min, max)	Test Conditions
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	1.54V min, 1.95V max	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	1200V min	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.4V min, 6.0V max	V_{GE} = V_{CE} , T_J =25°C, I_C = 250µA
I_{CES}	Zero Gate Voltage Collector Current	10µA max	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1µA max	T_J = 25°C, V_{GE} = +/-20V

Mechanical Data

Nominal Backmetal Composition, (Thickness)	Al - Ti - Ni/V - Ag, (1kA - 1kA - 4kA - 6kA)
Nominal Front Metal Composition, (Thickness)	99% Al/1% Si, (4µm)
Dimensions	0.257" x 0.260"
Wafer Diameter	150mm, with std. < 100 > flat
Wafer Thickness, Tolerance	185µm, +/-15µm
Relevant Die Mechanical Dwg. Number	01-5317
Minimum Street Width	100µm
Reject Ink Dot Size	0.25mm diameter minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300°C

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

PD - 93867

International
IOR Rectifier

IRGC25B120UB

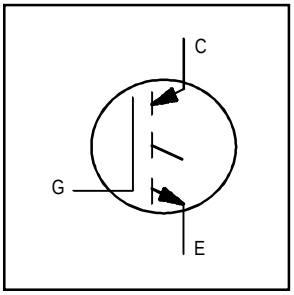
Die in Wafer Form

Features

- GEN5 Non Punch Through (NPT) Technology
- UltraFast
- 10µs Short Circuit Capability
- Square RBSOA
- Positive $V_{CE(on)}$ Temperature Coefficient

Benefits

- Benchmark Efficiency above 20KHz
- Optimized for Welding, UPS, and Induction Heating
- Rugged with UltraFast Performance
- Excellent Current Sharing in Parallel Operation



1200V
$I_{C(nom)}$=25A
$V_{CE(on)\,typ.}$=3.37V @
$I_{C(nom)}$ @ 25°C
UltraFast IGBT
Short Circuit Rated
150mm Wafer

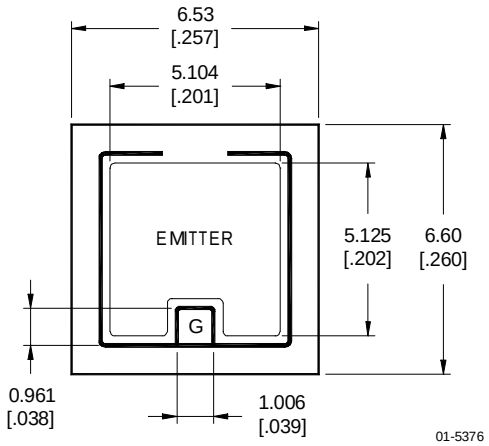
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (min, max)	Test Conditions
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	2.3V min, 2.7V max	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	1200V min	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.4V min, 6.0V max	V_{GE} = V_{CE} , T_J =25°C, I_C = 250µA
I_{CES}	Zero Gate Voltage Collector Current	10µA max	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1µA max	T_J = 25°C, V_{GE} = +/-20V

Mechanical Data

Nominal Backmetal Composition, (Thickness)	Al - Ti - Ni/V - Ag, (1kA - 1kA - 4kA - 6kA)
Nominal Front Metal Composition, (Thickness)	99% Al/1% Si, (4µm)
Dimensions	0.257" x 0.260"
Wafer Diameter	150mm, with std. < 100 > flat
Wafer Thickness, Tolerance	185µm, +/-15µm
Relevant Die Mechanical Dwg. Number	01-5376
Minimum Street Width	100µm
Reject Ink Dot Size	0.25mm diameter minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300°C

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

PD - 93870

International
IOR Rectifier

IRGC50B120KB

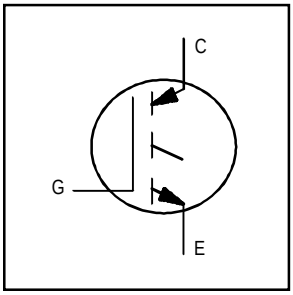
Die in Wafer Form

Features

- GEN5 Non Punch Through (NPT) Technology
- Low $V_{CE(on)}$
- 10µs Short Circuit Capability
- Square RBSOA
- Positive $V_{CE(on)}$ Temperature Coefficient

Benefits

- Benchmark Efficiency for Motor Control Applications
- Rugged Transient Performance
- Excellent Current Sharing in Parallel Operation



1200V
$I_{C(nom)}$=50A
$V_{CE(on)\,typ.}$=2.15V@
$I_{C(nom)}$@25°C
Motor Control IGBT
Short Circuit Rated
150mm Wafer

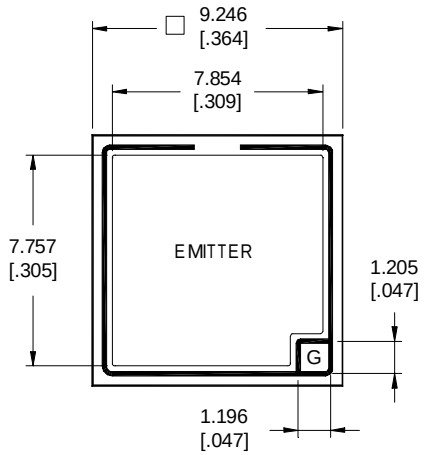
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (min, max)	Test Conditions
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	1.3V min, 1.53V max	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	1200V min	T_J = 25°C, I_{CES} = 500µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.4V min, 6.0V max	V_{GE} = V_{CE} , T_J =25°C, I_C = 500µA
I_{CES}	Zero Gate Voltage Collector Current	20µA max	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1µA max	T_J = 25°C, V_{GE} = +/-20V

Mechanical Data

Nominal Backmetal Composition, (Thickness)	Al - Ti - Ni/V - Ag, (1kA - 1kA - 4kA - 6kA)
Nominal Front Metal Composition, (Thickness)	99% Al/1% Si, (4µm)
Dimensions	0.364" x 0.364"
Wafer Diameter	150mm, with std. < 100 > flat
Wafer Thickness, Tolerance	185µm, +/-15µm
Relevant Die Mechanical Dwg. Number	01-5346
Minimum Street Width	100µm
Reject Ink Dot Size	0.25mm diameter minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300°C

Die Outline



01-5346

NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

PD - 93869

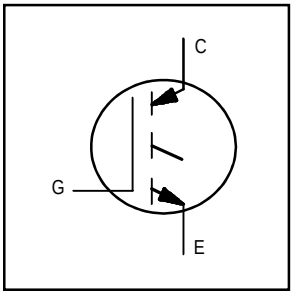
International
IOR Rectifier

IRGC50B120UB

Die in Wafer Form

Features
- GEN5 Non Punch Through (NPT) Technology
- UltraFast
- 10µs Short Circuit Capability
- Square RBSOA
- Positive $V_{CE(on)}$ Temperature Coefficient

Benefits
- Benchmark Efficiency above 20KHz
- Optimized for Welding, UPS, and Induction Heating
- Rugged with UltraFast Performance
- Excellent Current Sharing in Parallel Operation



1200V
$I_{C(nom)}$=50A
$V_{CE(on)\,typ.}$=3.15V @
$I_{C(nom)}$ @ 25°C
UltraFast IGBT
Short Circuit Rated
150mm Wafer

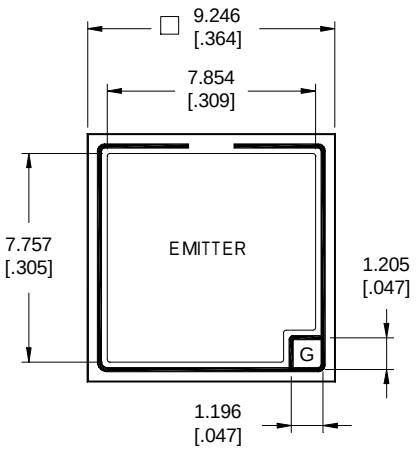
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (min, max)	Test Conditions
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	1.78V min, 2.08V max	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	1200V min	T_J = 25°C, I_{CES} = 500µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.4V min, 6.0V max	V_{GE} = V_{CE} , T_J =25°C, I_C = 500µA
I_{CES}	Zero Gate Voltage Collector Current	20µA max	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 1.1µA max	T_J = 25°C, V_{GE} = +/-20V

Mechanical Data

Nominal Backmetal Composition, (Thickness)	Al - Ti - Ni/V - Ag, (1kA - 1kA - 4kA - 6kA)
Nominal Front Metal Composition, (Thickness)	99% Al/1% Si, (4µm)
Dimensions	0.364" x 0.364"
Wafer Diameter	150mm, with std. < 100 > flat
Wafer Thickness, Tolerance	185µm, +/-15µm
Relevant Die Mechanical Dwg. Number	01-5377
Minimum Street Width	100µm
Reject Ink Dot Size	0.25mm diameter minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300°C

Die Outline



01-5377

NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

PD - 93872

International
IOR Rectifier

IRGC75B120KB

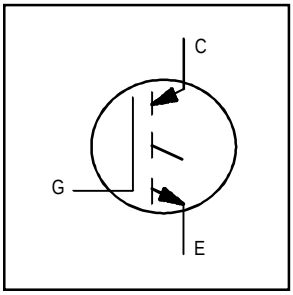
Die in Wafer Form

Features

- GEN5 Non Punch Through (NPT) Technology
- Low $V_{CE(on)}$
- 10µs Short Circuit Capability
- Square RBSOA
- Positive $V_{CE(on)}$ Temperature Coefficient

Benefits

- Benchmark Efficiency for Motor Control Applications
- Rugged Transient Performance
- Excellent Current Sharing in Parallel Operation



1200V
$I_{C(nom)}$ = 75A
$V_{CE(on)\ typ.}$ = 2.1 V @
$I_{C(nom)}$ @ 25°C
Motor Control IGBT
Short Circuit Rated
150mm Wafer

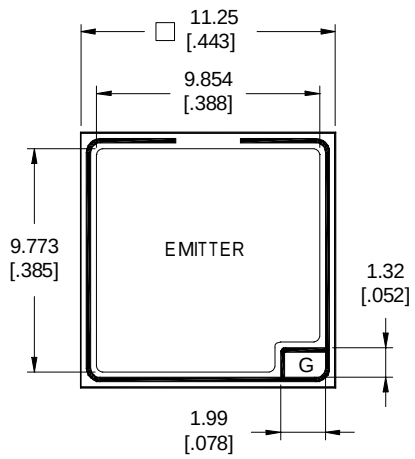
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (min, max)	Test Conditions
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	1.18V min, 1.35V max	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	1200V min	T_J = 25°C, I_{CES} = 750µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.4V min, 6.0V max	V_{GE} = V_{CE} , T_J =25°C, I_C = 750µA
I_{CES}	Zero Gate Voltage Collector Current	30µA max	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 2 µA max	T_J = 25°C, V_{GE} = +/-20V

Mechanical Data

Nominal Backmetal Composition, (Thickness)	Al - Ti - Ni/V - Ag, (1kA - 1kA - 4kA - 6kA)
Nominal Front Metal Composition, (Thickness)	99% Al/1% Si, (4µm)
Dimensions	0.443" x 0.443"
Wafer Diameter	150mm, with std. < 100 > flat
Wafer Thickness, Tolerance	185µm, +/-15µm
Relevant Die Mechanical Dwg. Number	01-5316
Minimum Street Width	100µm
Reject Ink Dot Size	0.25mm diameter minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300°C

Die Outline



01-5316

NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENT SENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE =	+/- 0.013
WIDTH	< [.0250] TOLERANCE =	+/- [.0005]
&	> 0.635 TOLERANCE =	+/- 0.025
LENGTH	> [.0250] TOLERANCE =	+/- [.0010]
OVERALL DIE:	< 1.270 TOLERANCE =	+/- 0.102
WIDTH	< [.050] TOLERANCE =	+/- [.004]
&	> 1.270 TOLERANCE =	+/- 0.203
LENGTH	> [.050] TOLERANCE =	+/- [.008]

PD - 93871

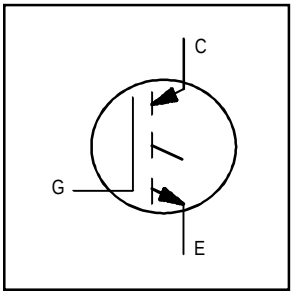
International
IOR Rectifier

IRGC75B120UB

Die in Wafer Form

Features
- GEN5 Non Punch Through (NPT) Technology
- UltraFast
- 10µs Short Circuit Capability
- Square RBSOA
- Positive $V_{CE(on)}$ Temperature Coefficient

Benefits
- Benchmark Efficiency above 20KHz
- Optimized for Welding, UPS, and Induction Heating
- Rugged with UltraFast Performance
- Excellent Current Sharing in Parallel Operation



1200V
$I_{C(nom)}$=75A
$V_{CE(on)\ typ.}$= 3.1V @
$I_{C(nom)}$ @ 25°C
UltraFast IGBT
Short Circuit Rated
150mm Wafer

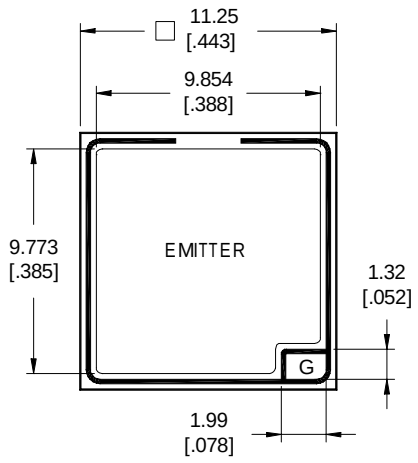
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (min, max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	1.54V min, 1.78V max	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200V min	T_J = 25°C, I_{CES} = 750µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.4V min, 6.0V max	V_{GE} = V_{CE} , T_J =25°C, I_C = 750µA
I_{CES}	Zero Gate Voltage Collector Current	30µA max	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 2 µA max	T_J = 25°C, V_{GE} = +/-20V

Mechanical Data

Nominal Backmetal Composition, (Thickness)	Al - Ti - Ni/V - Ag, (1kA - 1kA - 4kA - 6kA)
Nominal Front Metal Composition, (Thickness)	99% Al/1% Si, (4µm)
Dimensions	0.443" x 0.443"
Wafer Diameter	150mm, with std. < 100 > flat
Wafer Thickness, Tolerance	185µm, +/-15µm
Relevant Die Mechanical Dwg. Number	01-5378
Minimum Street Width	100µm
Reject Ink Dot Size	0.25mm diameter minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300°C

Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

01-5378

PD - 93874

International
IOR Rectifier

IRGC100B120KB

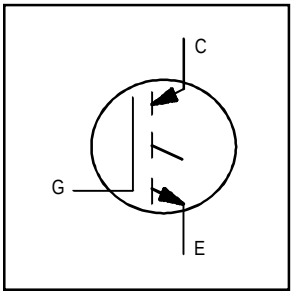
Die in Wafer Form

Features

- GEN5 Non Punch Through (NPT) Technology
- Low $V_{CE(on)}$
- 10µs Short Circuit Capability
- Square RBSOA
- Positive $V_{CE(on)}$ Temperature Coefficient

Benefits

- Benchmark Efficiency for Motor Control Applications
- Rugged Transient Performance
- Excellent Current Sharing in Parallel Operation



1200V
$I_{C(nom)}$ = 100A
$V_{CE(on)\ typ.}$ = 2.2V @
$I_{C(nom)}$ @ 25°C
Motor Control IGBT
Short Circuit Rated
150mm Wafer

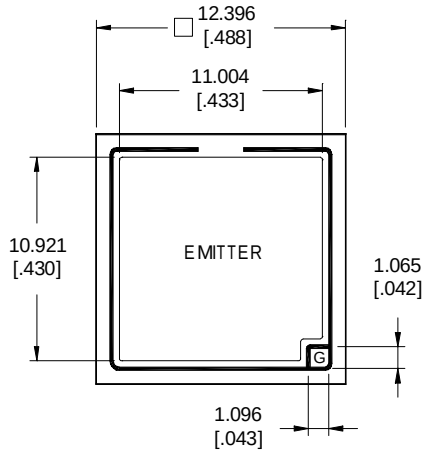
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (min, max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	1.12V min, 1.29V max	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200V min	T_J = 25°C, I_{CES} = 1mA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.4V min, 6.0V max	V_{GE} = V_{CE} , T_J =25°C, I_C = 1mA
I_{CES}	Zero Gate Voltage Collector Current	40µA max	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 3 µA max	T_J = 25°C, V_{GE} = +/-20V

Mechanical Data

Nominal Backmetal Composition, (Thickness)	Al - Ti - Ni/V - Ag, (1kA - 1kA - 4kA - 6kA)
Nominal Front Metal Composition, (Thickness)	99% Al/1% Si, (4µm)
Dimensions	0.488" x 0.488"
Wafer Diameter	150mm, with std. < 100 > flat
Wafer Thickness, Tolerance	185µm, +/-15µm
Relevant Die Mechanical Dwg. Number	01-5318
Minimum Street Width	100µm
Reject Ink Dot Size	0.25mm diameter minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300°C

Die Outline



01-5318

NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

International
IOR Rectifier

PD - 93873A

IRGC100B120UB

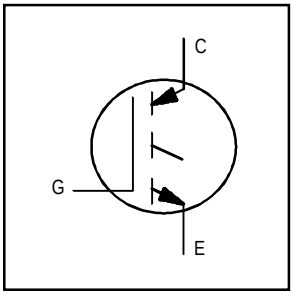
Die in Wafer Form

Features

- GEN5 Non Punch Through (NPT) Technology
- Low $V_{CE(on)}$
- 10µs Short Circuit Capability
- Square RBSOA
- Positive $V_{CE(on)}$ Temperature Coefficient

Benefits

- Benchmark Efficiency above 20KHz
- Optimized for Welding, UPS, and Induction Heating
- Rugged with Ultra Fast Performance
- Excellent Current Sharing in Parallel Operation



1200V
$I_{C(nom)}$ = 100A
$V_{CE(on)\ typ.}$ = 3.1V @
$I_{C(nom)}$ @ 25°C
UltraFast IGBT
Short Circuit Rated
150mm Wafer

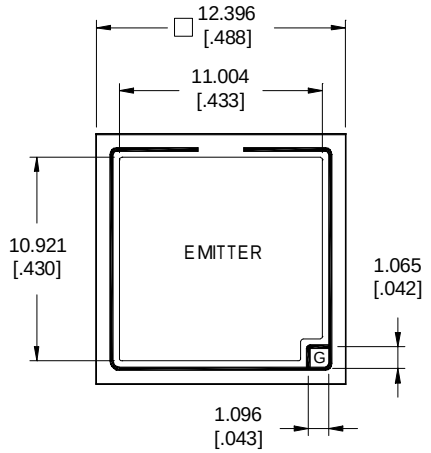
Electrical Characteristics (Wafer Form)

Parameter	Description	Guaranteed (min, max)	Test Conditions
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	1.43V min, 1.64V max	I_C = 10A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	1200V min	T_J = 25°C, I_{CES} = 1mA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	4.4V min, 6.0V max	V_{GE} = V_{CE} , T_J =25°C, I_C = 1mA
I_{CES}	Zero Gate Voltage Collector Current	40µA max	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 3 µA max	T_J = 25°C, V_{GE} = +/-20V

Mechanical Data

Nominal Backmetal Composition, (Thickness)	Al - Ti - Ni/V - Ag, (1kA - 1kA - 4kA - 6kA)
Nominal Front Metal Composition, (Thickness)	99% Al/1% Si, (4µm)
Dimensions	0.488" x 0.488"
Wafer Diameter	150mm, with std. < 100 > flat
Wafer Thickness, Tolerance	185µm, +/-15µm
Relevant Die Mechanical Dwg. Number	01-5318
Minimum Street Width	100µm
Reject Ink Dot Size	0.25mm diameter minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300°C

Die Outline



01-5318

NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
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3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE =	+/- 0.013
WIDTH	< [.0250] TOLERANCE =	+/- [.0005]
&	> 0.635 TOLERANCE =	+/- 0.025
LENGTH	> [.0250] TOLERANCE =	+/- [.0010]
OVERALL DIE:	< 1.270 TOLERANCE =	+/- 0.102
WIDTH	< [.050] TOLERANCE =	+/- [.004]
&	> 1.270 TOLERANCE =	+/- 0.203
LENGTH	> [.050] TOLERANCE =	+/- [.008]

International
IOR Rectifier

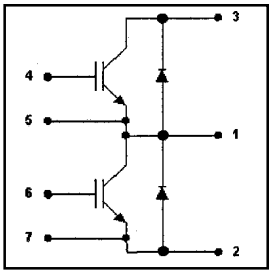
GA75TS60U

"HALF-BRIDGE" IGBT INT-A-PAK

Ultra-Fast™ Speed IGBT

Features

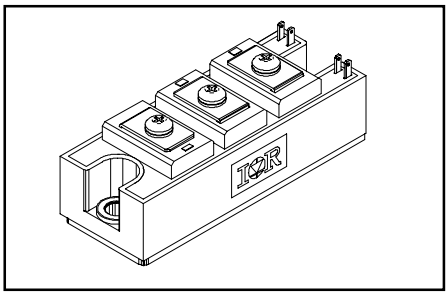
- Generation 4 IGBT technology
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL approved



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.7V

@V_{GE} = 15V, I_C = 75A



Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	75	A
I_{CM}	Pulsed Collector Current•	150	
I_{LM}	Peak Switching Current,	150	
I_{FM}	Peak Diode Forward Current	150	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	285	W
P_D @ T_C = 85°C	Maximum Power Dissipation	150	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.44	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.70	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3ƒ	—	3.0	
	Weight of Module	200	—	g

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	1.7	2.2		V_{GE} = 15V, I_C = 75A
		—	1.76	—		V_{GE} = 15V, I_C = 75A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		I_C = 0.5mA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 500µA
g_{fe}	Forward Transconductance „	—	83	—	S	V_{CE} = 25V, I_C = 75A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	1.0	mA	V_{GE} = 0V, V_{CE} = 600V
		—	—	10		V_{GE} = 0V, V_{CE} = 600V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	3.3	—	V	I_F = 75A, V_{GE} = 0V
		—	3.1	—		I_F = 75A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	250	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	340	510	nC	V_{CC} = 400V, V_{GE} = 15V
Q_{ge}	Gate - Emitter Charge (turn-on)	—	48	72		I_C = 75A
Q_{gc}	Gate - Collector Charge (turn-on)	—	120	170		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	110	—	ns	R_{G1} = 27Ω, R_{G2} = 0Ω,
t_r	Rise Time	—	94	—		I_C = 75A
$t_{d(off)}$	Turn-Off Delay Time	—	250	—		V_{CC} = 360V
t_f	Fall Time	—	180	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	1.95	—	mJ	
$E_{off\ (1)}$	Turn-Off Switching Energy	—	4.4	—		
$E_{ts\ (1)}$	Total Switching Energy	—	6.35	12.6		
C_{ies}	Input Capacitance	—	7880	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	770	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	98	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	133	—	ns	I_C = 75A
I_{rr}	Diode Peak ReverseCurrent	—	94	—	A	R_{G1} = 27Ω
Q_{rr}	Diode Recovery Charge	—	6274	—	nC	R_{G2} = 0Ω
$di_{(rec)}M_{/dt}$	Diode Peak Rate of Fall of Recovery During t_b	—	2061	—	A/µs	V_{CC} = 360V di/dt =1300A/µs

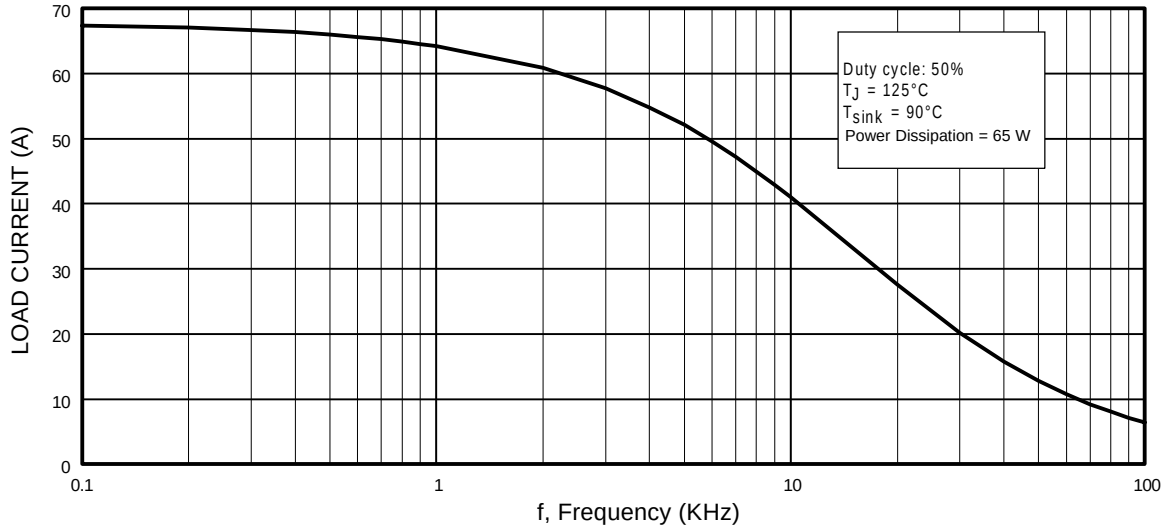


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

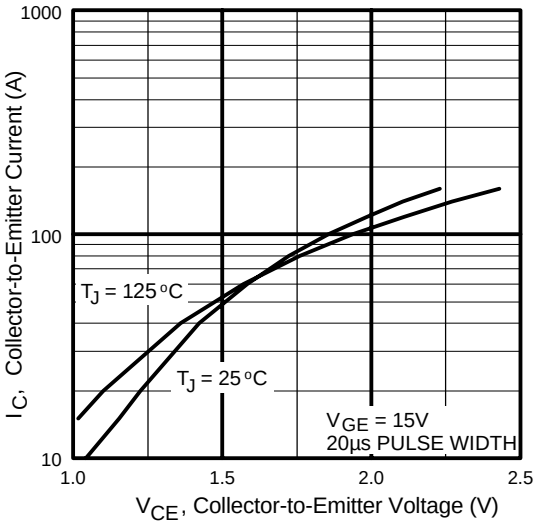


Fig. 2 - Typical Output Characteristics

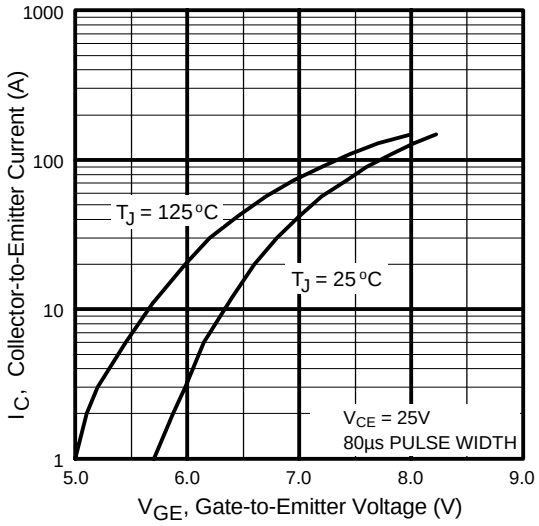


Fig. 3 - Typical Transfer Characteristics

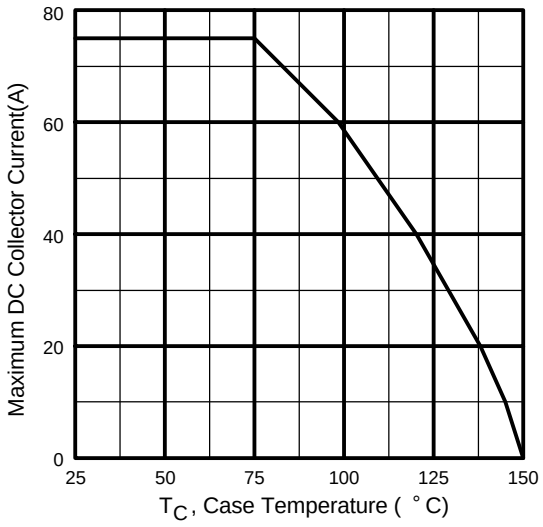


Fig. 4 - Maximum Collector Current vs. Case Temperature

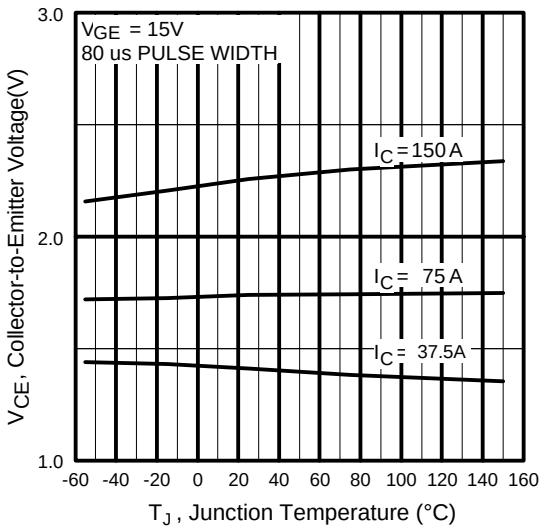


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

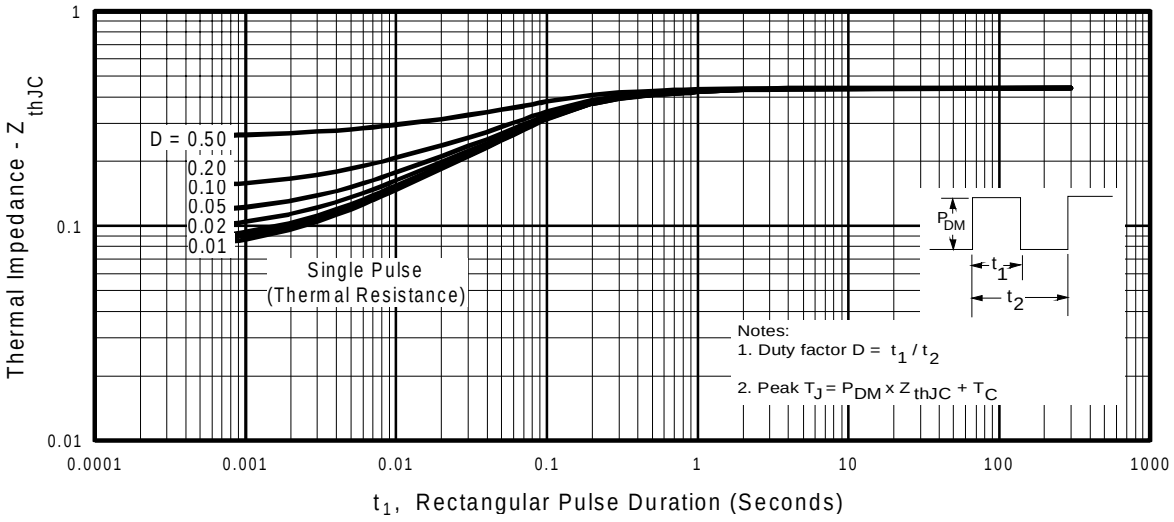


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

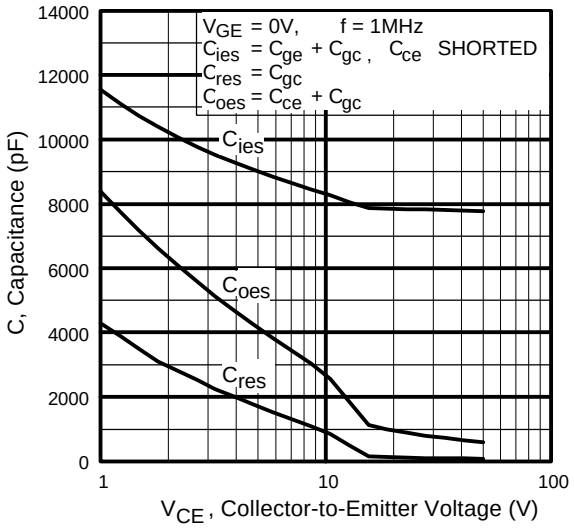


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

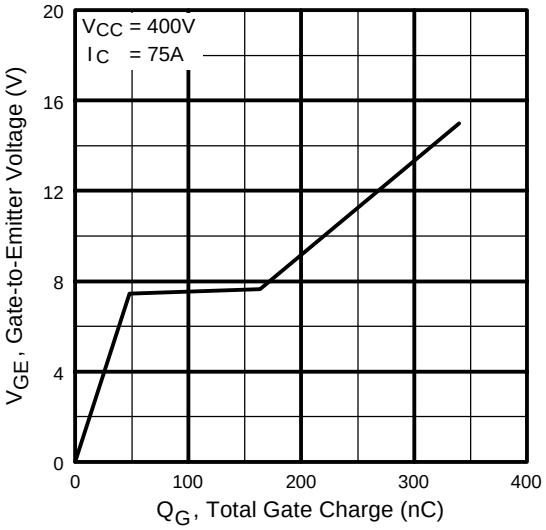


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

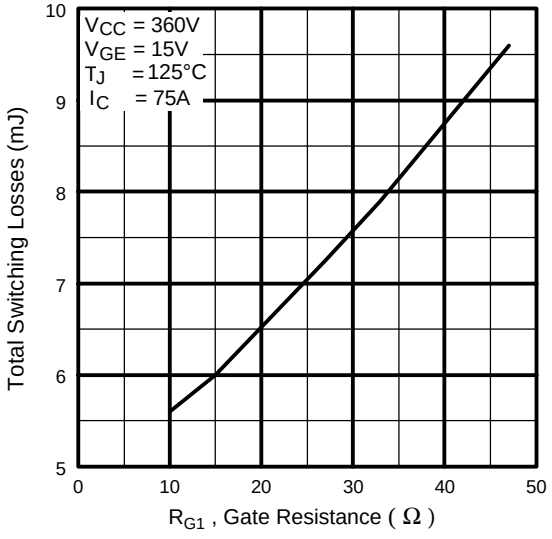


Fig. 9 - Typical Switching Losses vs. Gate Resistance

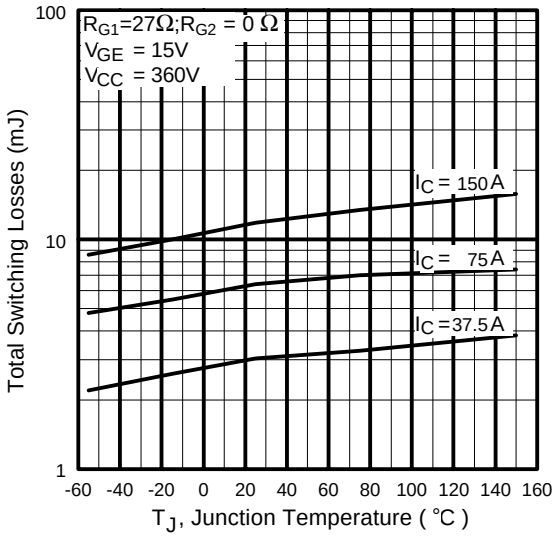


Fig. 10 - Typical Switching Losses vs. Junction Temperature

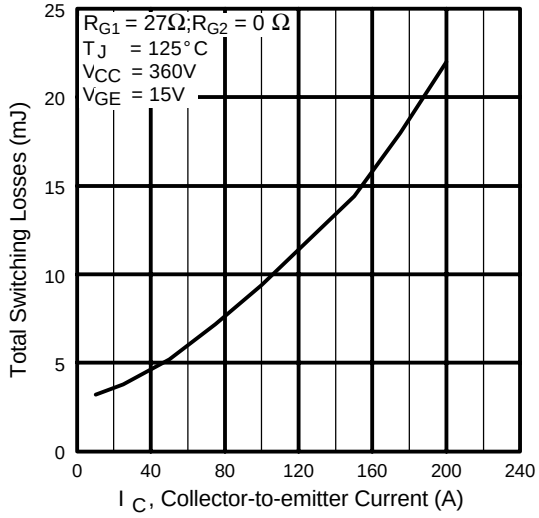


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

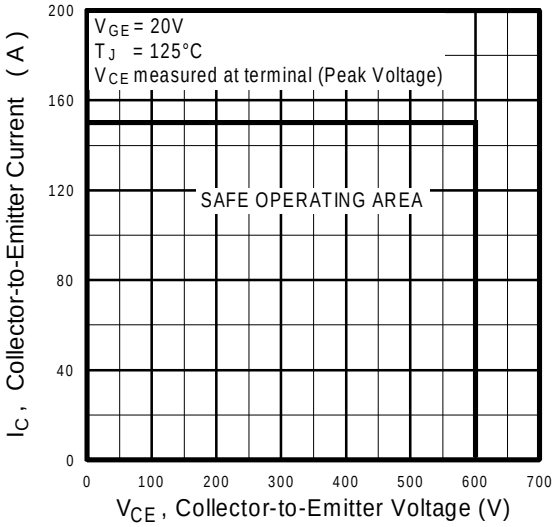


Fig. 12 - Reverse Bias SOA

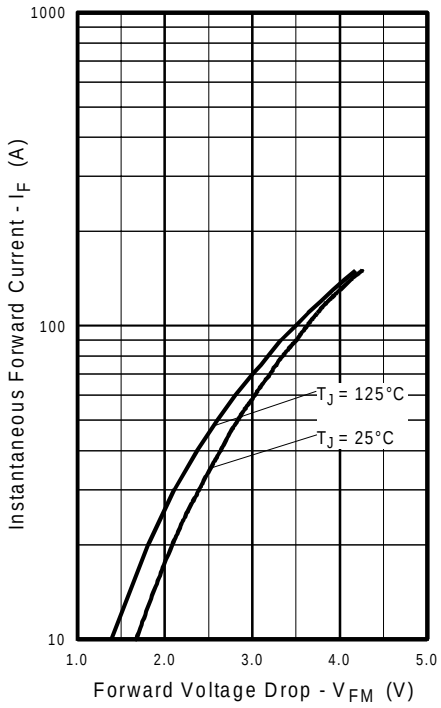


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

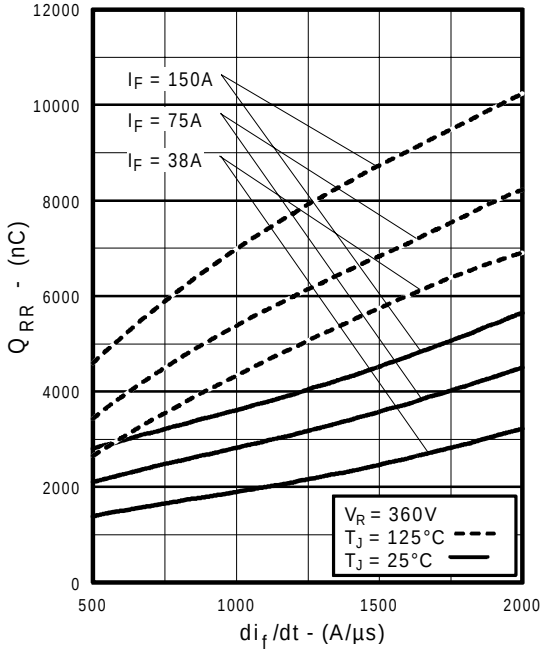


Fig. 14 - Typical Stored Charge vs. di_f/dt

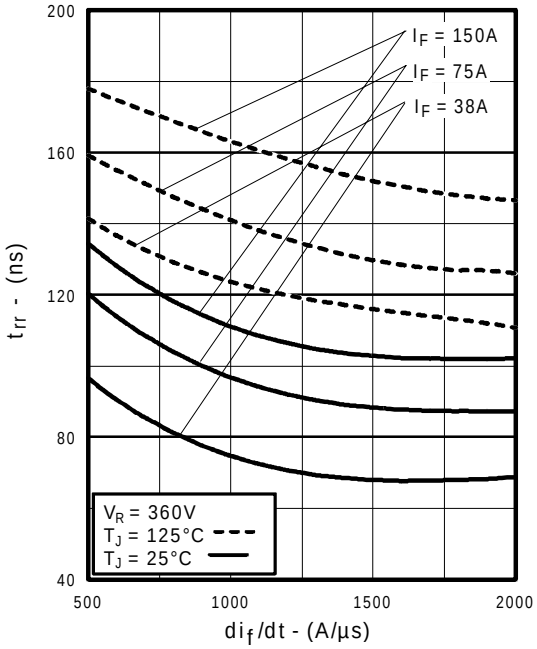


Fig. 15 - Typical Reverse Recovery vs. di_f/dt

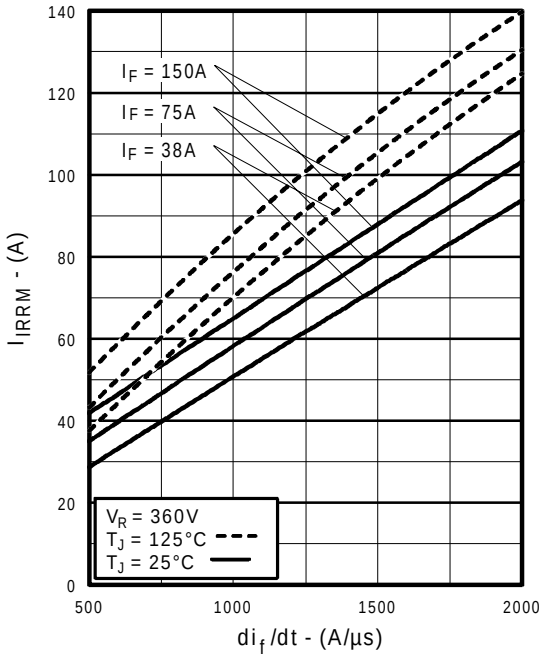


Fig. 16 - Typical Recovery Current vs. di_f/dt

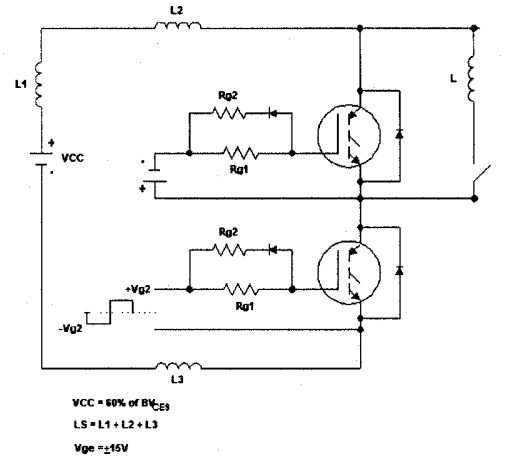


Fig. 17 - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

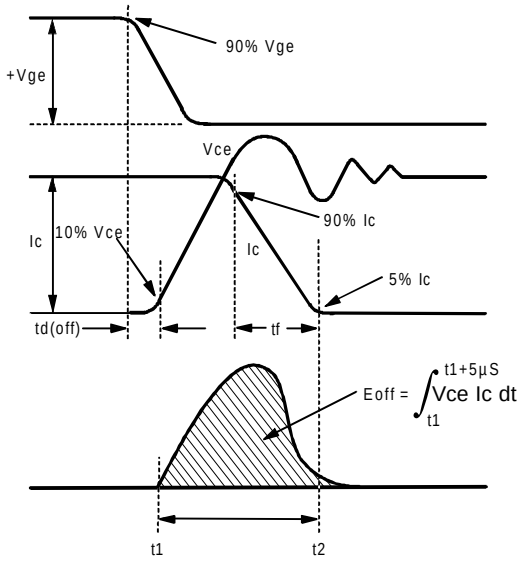


Fig. 18 - Test Waveforms for Circuit of Fig. 17, Defining E_{off}, $t_{d(off)}$, t_f

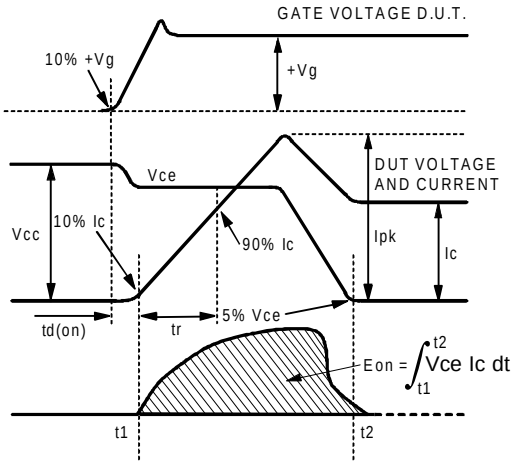


Fig. 19 - Test Waveforms for Circuit of Fig. 17, Defining E_{on}, $t_{d(on)}$, t_r

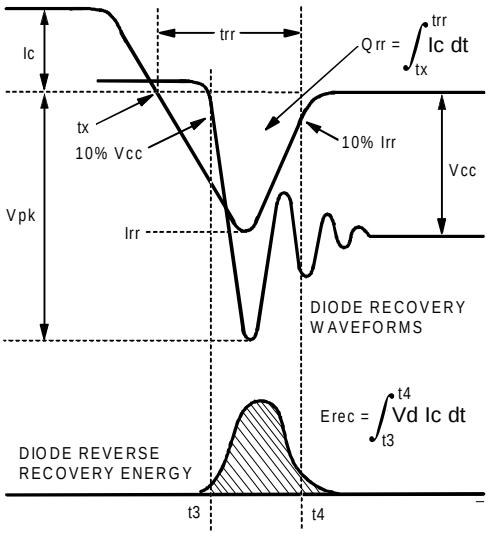


Fig. 20 - Test Waveforms for Circuit of Fig. 17, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

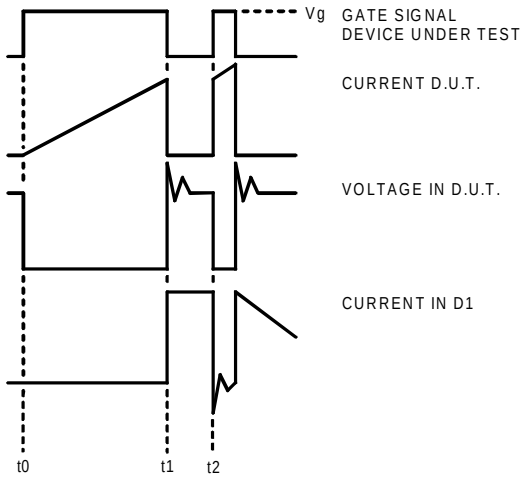


Figure 21. Macro Waveforms for Figure 17's Test Circuit

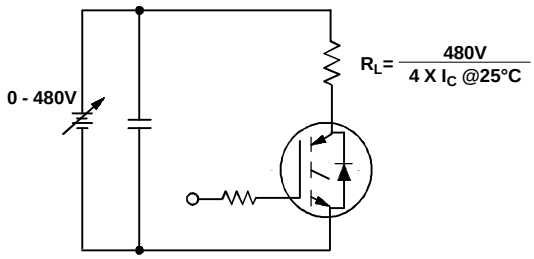


Figure 22. Pulsed Collector Current
Test Circuit

Notes:

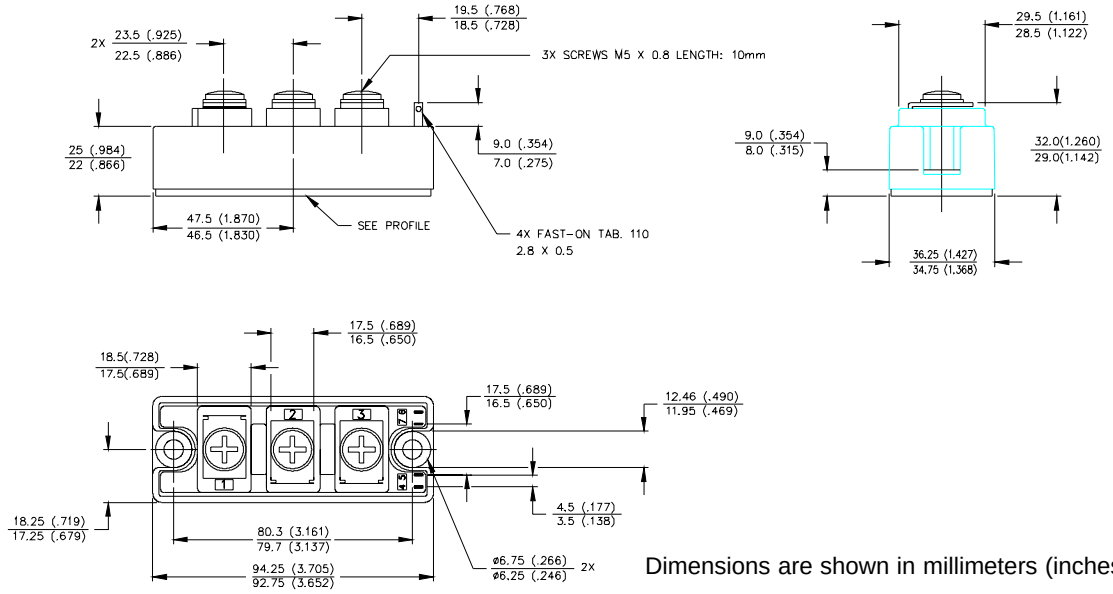
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 17

③ For screws M5x0.8

④ Pulse width 80µs; single shot.

Case Outline — INT-A-PAK



Dimensions are shown in millimeters (inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
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IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
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International
IOR Rectifier

PD -50055B

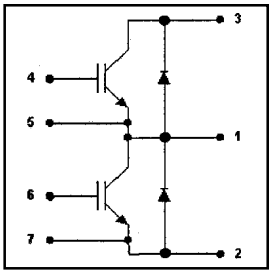
GA100TS60U

"HALF-BRIDGE" IGBT INT-A-PAK

Ultra-Fast™ Speed IGBT

Features

- Generation 4 IGBT technology
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL recognition pending



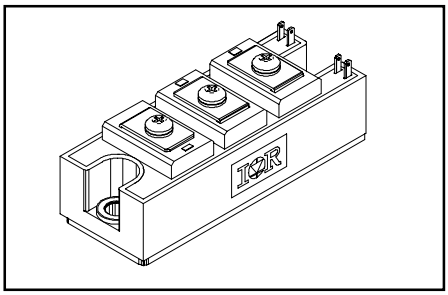
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.6V

@V_{GE} = 15V, I_C = 100A

Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	100	A
I_{CM}	Pulsed Collector Current•	200	
I_{LM}	Peak Switching Current,	200	
I_{FM}	Peak Diode Forward Current	200	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	320	W
P_D @ T_C = 85°C	Maximum Power Dissipation	170	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.38	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.70	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3③	—	3.0	
	Weight of Module	200	—	g

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	1.6	2.1		V_{GE} = 15V, I_C = 100A
		—	1.6	—		V_{GE} = 15V, I_C = 100A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		I_C = 500µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 500µA
g_{fe}	Forward Transconductance „	—	107	—	S	V_{CE} = 25V, I_C = 100A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	1.0	mA	V_{GE} = 0V, V_{CE} = 600V
		—	—	10		V_{GE} = 0V, V_{CE} = 600V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	3.6	—	V	I_F = 100A, V_{GE} = 0V
		—	3.5	—		I_F = 100A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	100	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	443	664	nC	V_{CC} = 400V
Q_{ge}	Gate - Emitter Charge (turn-on)	—	86	129		I_C = 66A
Q_{gc}	Gate - Collector Charge (turn-on)	—	150	225		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	168	—	ns	R_{G1} = 27Ω, R_{G2} = 0Ω
t_r	Rise Time	—	145	—		I_C = 100A
$t_{d(off)}$	Turn-Off Delay Time	—	320	—		V_{CC} = 360V
t_f	Fall Time	—	242	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	4.0	—	mJ	
$E_{off\ (1)}$	Turn-Off Switching Energy	—	7.0	—		
$E_{ts\ (1)}$	Total Switching Energy	—	11	17		
C_{ies}	Input Capacitance	—	9837	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	615	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	128	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	143	—	ns	I_C = 100A
I_{rr}	Diode Peak ReverseCurrent	—	95	—	A	R_{G1} = 27Ω
Q_{rr}	Diode Recovery Charge	—	6813	—	nC	R_{G2} = 0Ω
$di_{(rec)}M_{/dt}$	Diode Peak Rate of Fall of Recovery During t_b	—	1883	—	A/µs	V_{CC} = 360V di/dt»1300A/µs

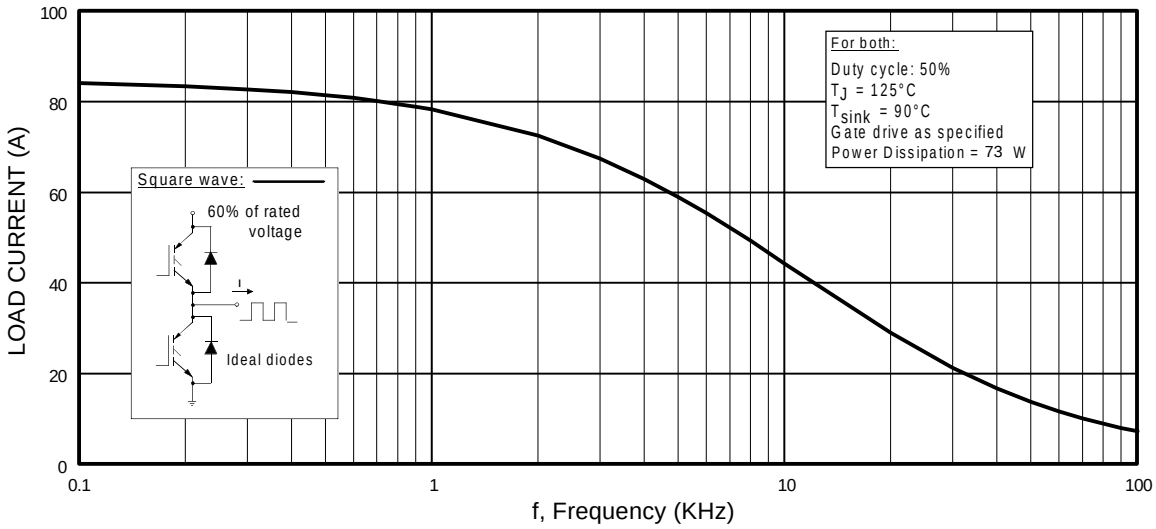


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

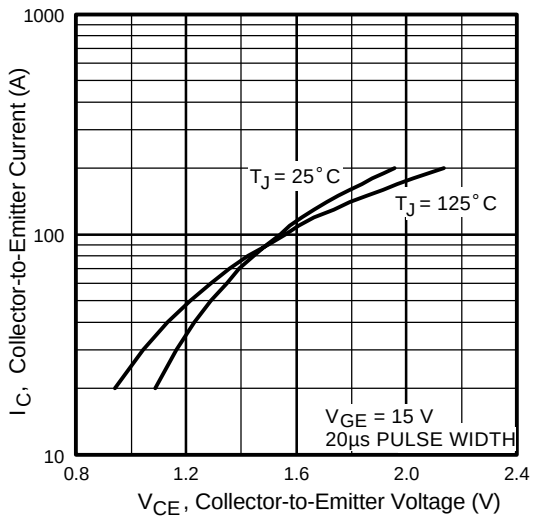


Fig. 2 - Typical Output Characteristics

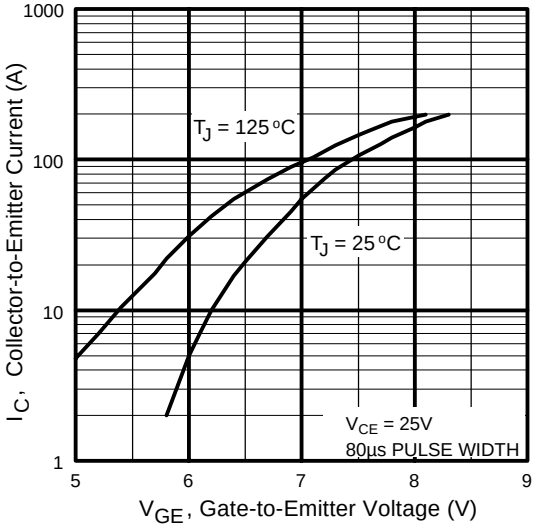


Fig. 3 - Typical Transfer Characteristics

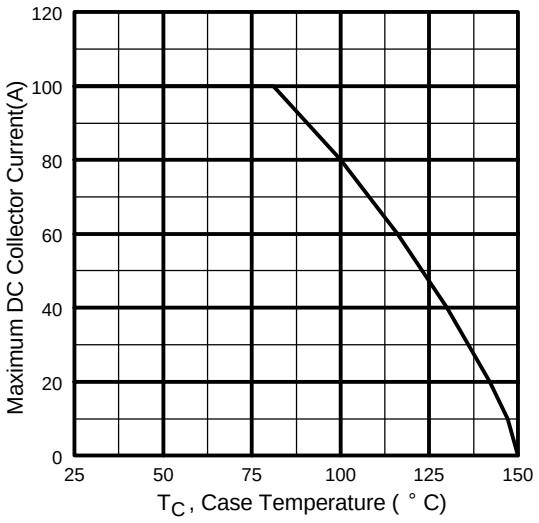


Fig. 4 - Maximum Collector Current vs. Case Temperature

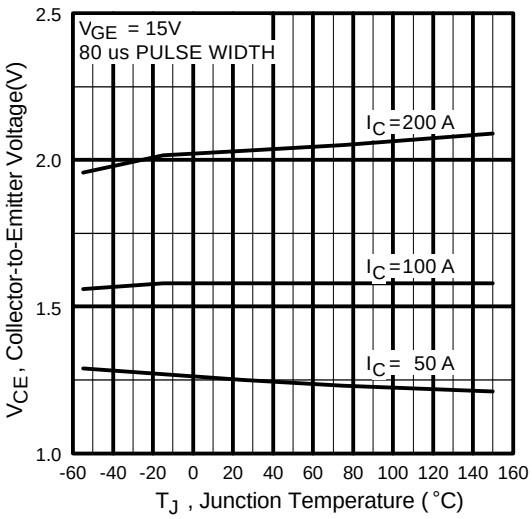


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

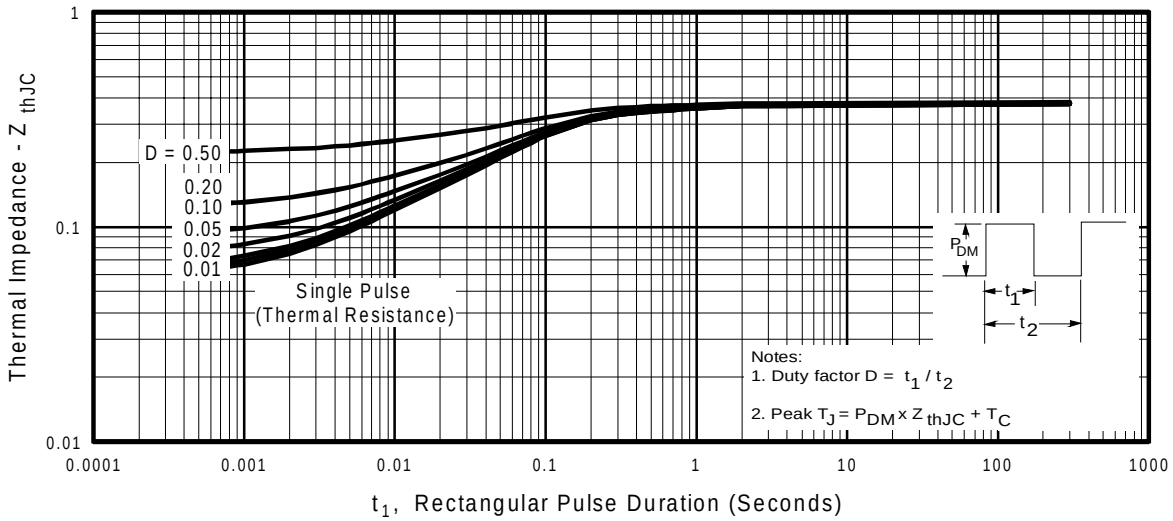


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

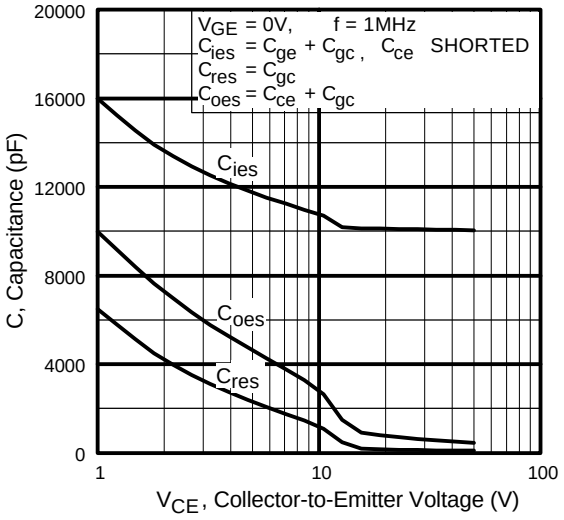


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

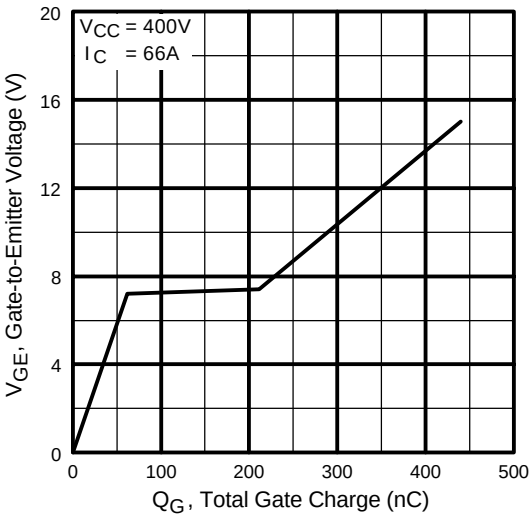


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

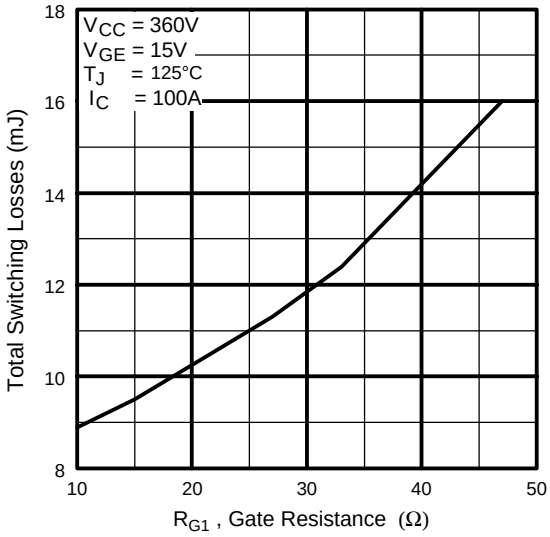


Fig. 9 - Typical Switching Losses vs. Gate Resistance

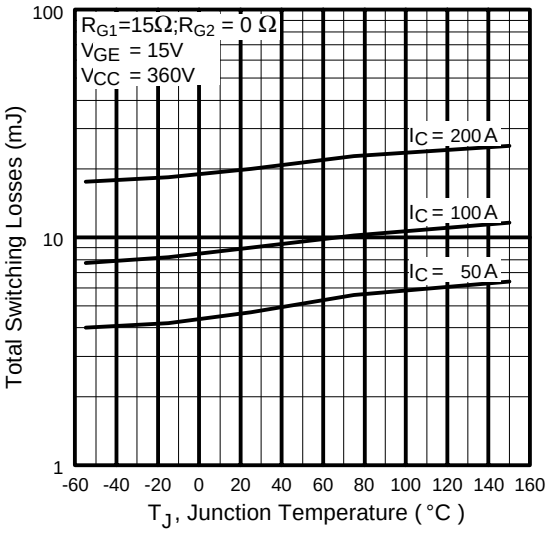


Fig. 10 - Typical Switching Losses vs. Junction Temperature

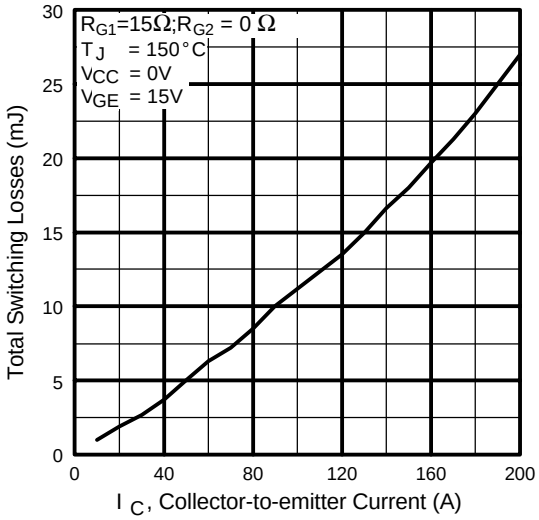


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

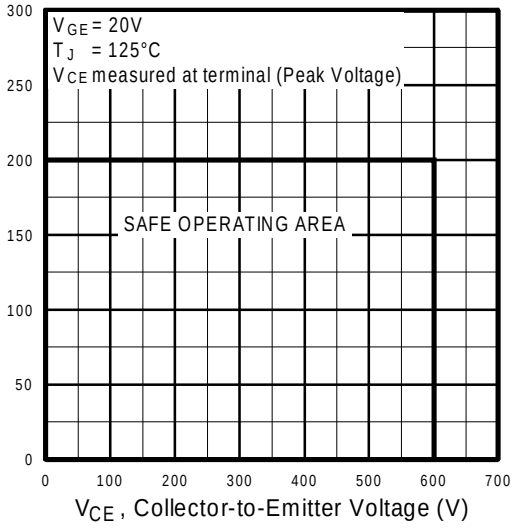


Fig. 12 - Reverse Bias SOA

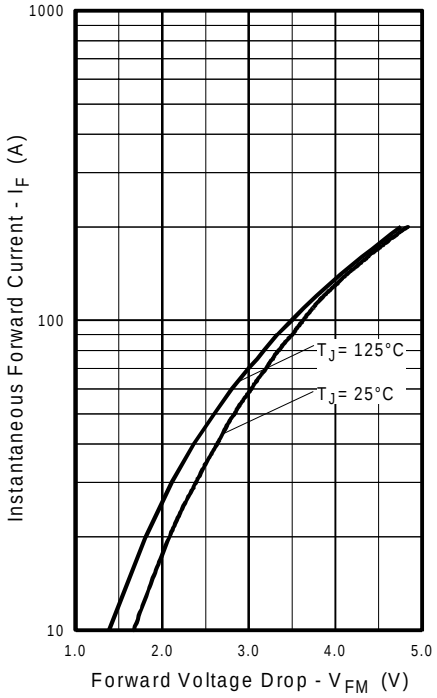


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

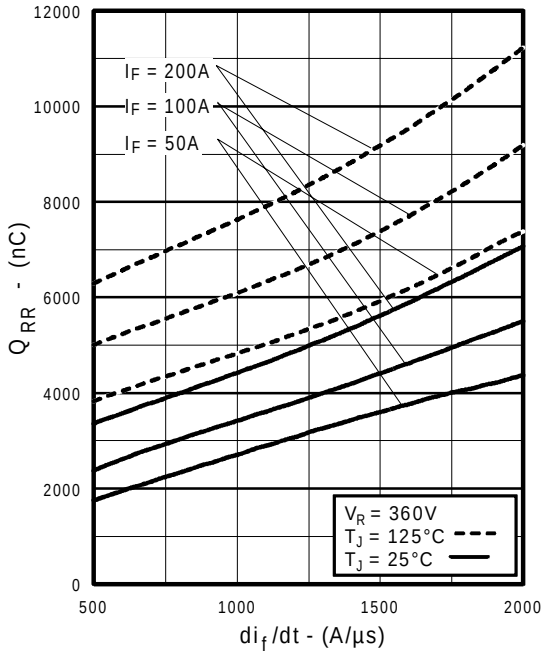


Fig. 14 - Typical Stored Charge vs. di_f/dt

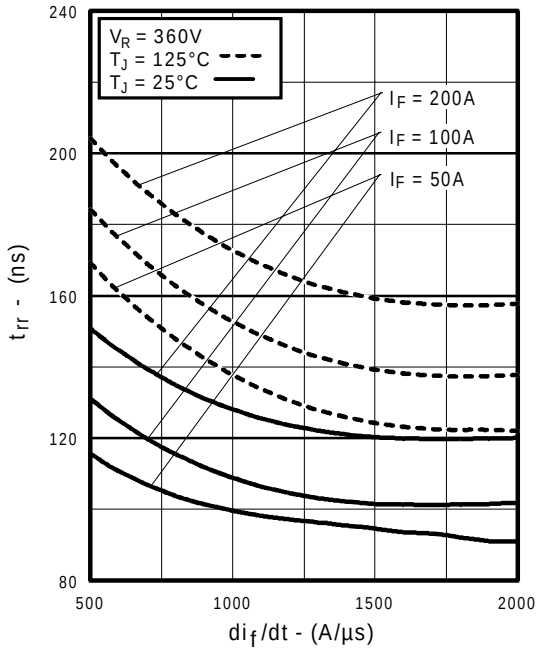


Fig. 15 - Typical Reverse Recovery vs. di_f/dt

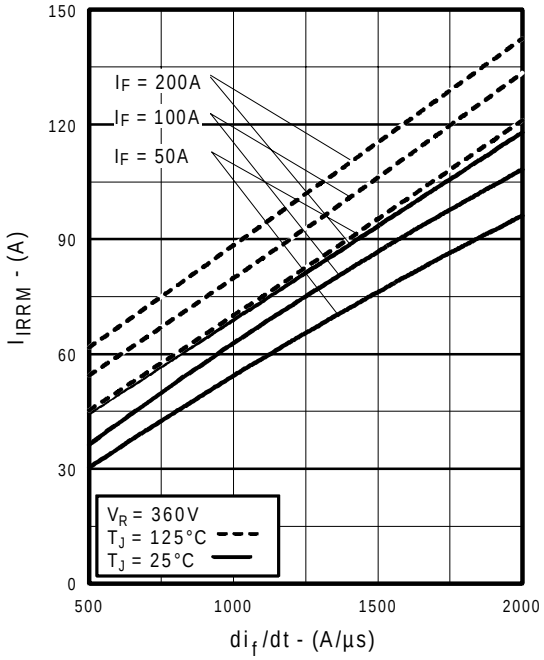


Fig. 16 - Typical Recovery Current vs. di_f/dt

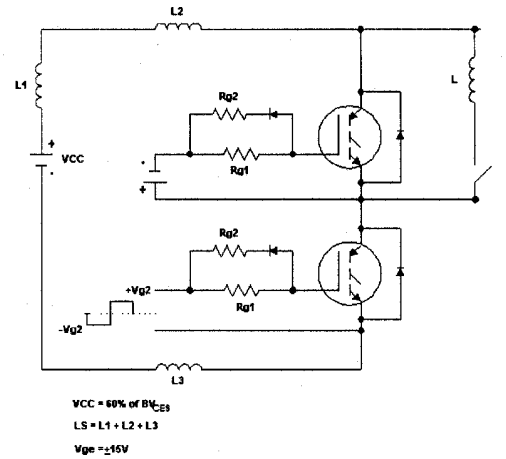


Fig. 17 - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

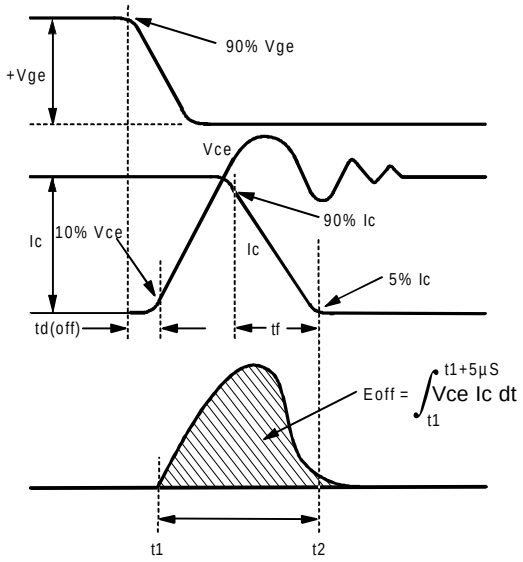


Fig. 18 - Test Waveforms for Circuit of Fig. 17, Defining E_{off}, $t_{d(off)}$, t_f

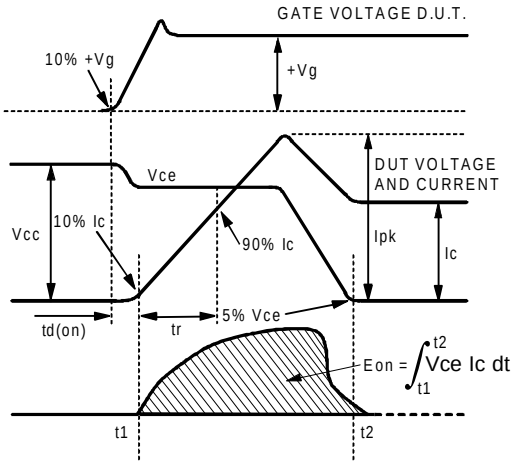


Fig. 19 - Test Waveforms for Circuit of Fig. 17, Defining E_{on}, $t_{d(on)}$, t_r

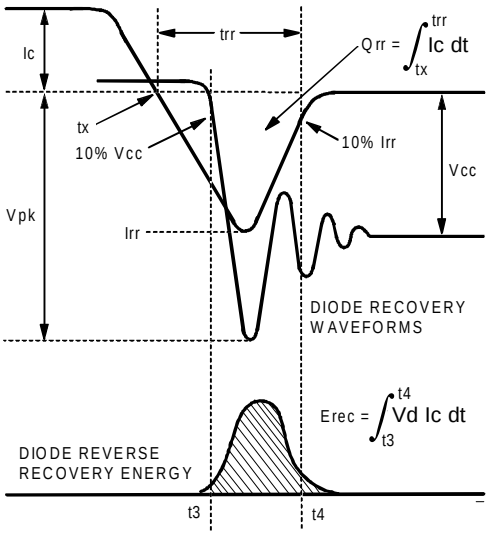


Fig. 20 - Test Waveforms for Circuit of Fig. 17, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

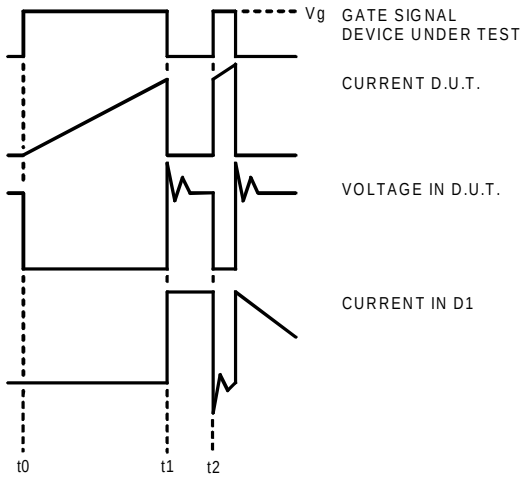


Figure 21. Macro Waveforms for Figure 17's Test Circuit

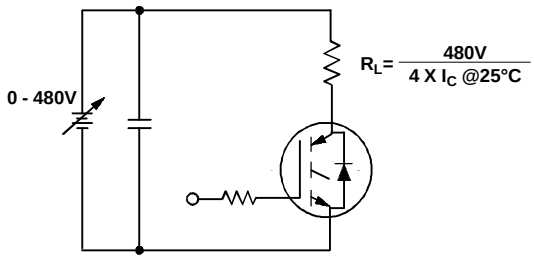


Figure 22. Pulsed Collector Current
Test Circuit

Notes:

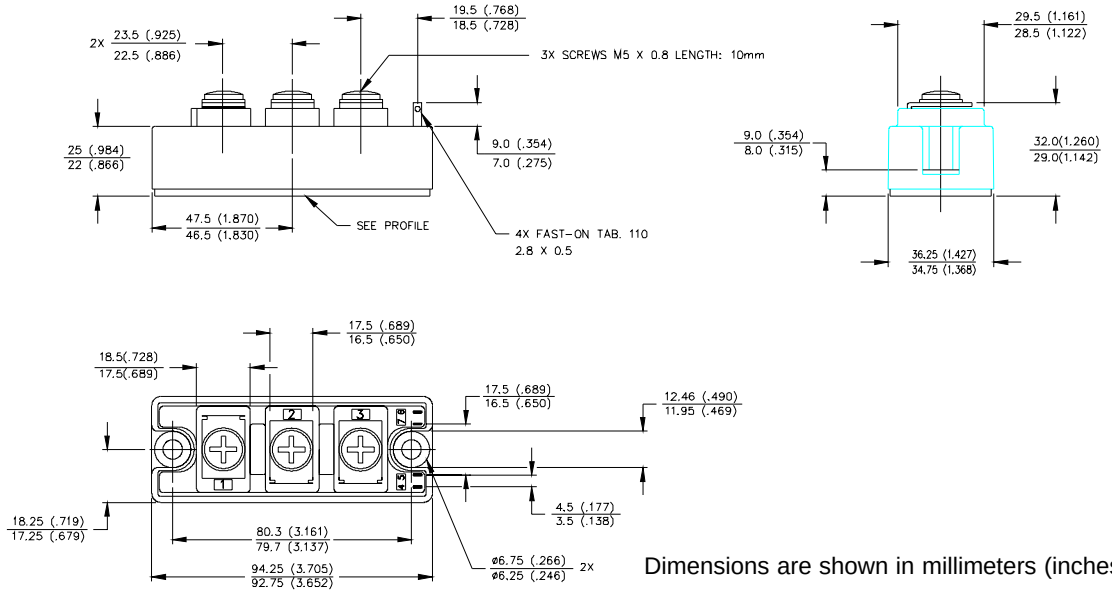
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 17

③ For screws M5x0.8

④ Pulse width 80µs; single shot.

Case Outline — INT-A-PAK



Dimensions are shown in millimeters (inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
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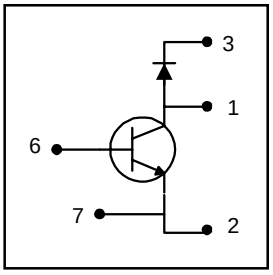
PD -94346

International
IOR Rectifier

GA150KS61U

IGBT INT-A-PAK

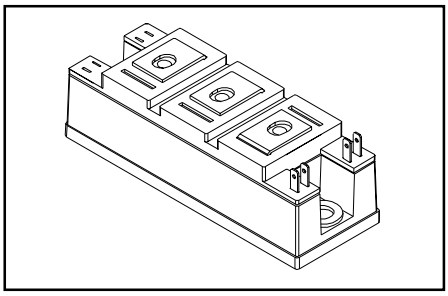
Low Side Switch Chopper Module
Ultra-Fast™ Speed IGBT



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.7V

@V_{GE} = 15V, I_C = 150A



Features

- Generation 4 IGBT technology
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL approved

Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	150	A
I_{CM}	Pulsed Collector Current①	300	
I_{LM}	Peak Switching Current②	300	
I_{FM}	Peak Diode Forward Current	300	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	440	W
P_D @ T_C = 85°C	Maximum Power Dissipation	230	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.28	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.35	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3③	—	3.0	
	Weight of Module	200	—	g

11/06/01

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	1.7	2.3		V_{GE} = 15V, I_C = 150A
		—	1.7	—		V_{GE} = 15V, I_C = 150A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		I_C = 750µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 750µA
g_{fe}	Forward Transconductance ④	—	152	—	S	V_{CE} = 25V, I_C = 150A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	1.0	mA	V_{GE} = 0V, V_{CE} = 600V
		—	—	10		V_{GE} = 0V, V_{CE} = 600V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	1.4	2.0	V	I_F = 150A, V_{GE} = 0V
		—	1.4	—		I_F = 150A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	250	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	624	937	nC	V_{CC} = 400V
Q_{ge}	Gate - Emitter Charge (turn-on)	—	121	182		I_C = 94A
Q_{gc}	Gate - Collector Charge (turn-on)	—	212	317		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	241	—	ns	R_{G1} = 27Ω, R_{G2} = 0Ω,
t_r	Rise Time	—	145	—		I_C = 150A
$t_{d(off)}$	Turn-Off Delay Time	—	336	—		V_{CC} = 360V
t_f	Fall Time	—	227	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	6.0	—	mJ	
$E_{off\ (1)}$	Turn-Off Switching Energy	—	12	—		
$E_{ts\ (1)}$	Total Switching Energy	—	19	33		
C_{ies}	Input Capacitance	—	13878	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	867	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	181	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	139	—	ns	I_C = 150A
I_{rr}	Diode Peak ReverseCurrent	—	100	—	A	R_{G1} = 27Ω
Q_{rr}	Diode Recovery Charge	—	6938	—	nC	R_{G2} = 0Ω
$di_{(rec)}M_{/dt}$	Diode Peak Rate of Fall of Recovery During t_b	—	4682	—	A/µs	V_{CC} = 360V di/dt =1400A/µs

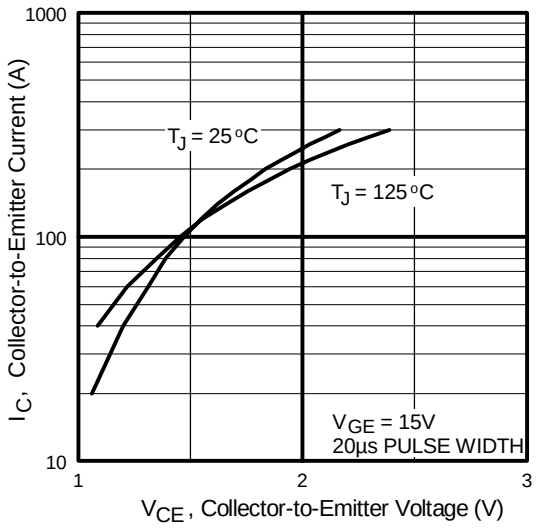


Fig. 1 - Typical Output Characteristics

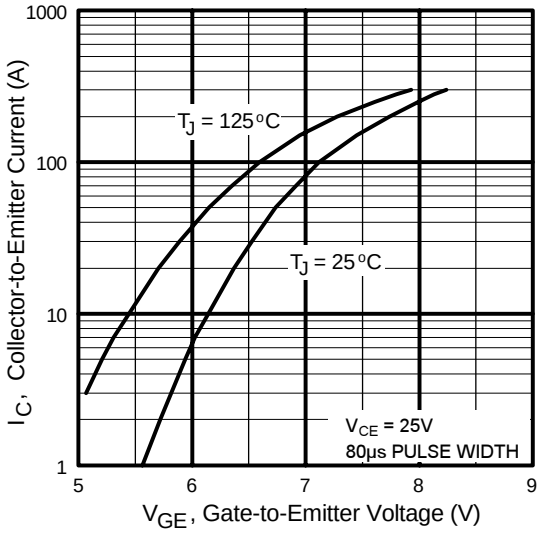


Fig. 2 - Typical Transfer Characteristics

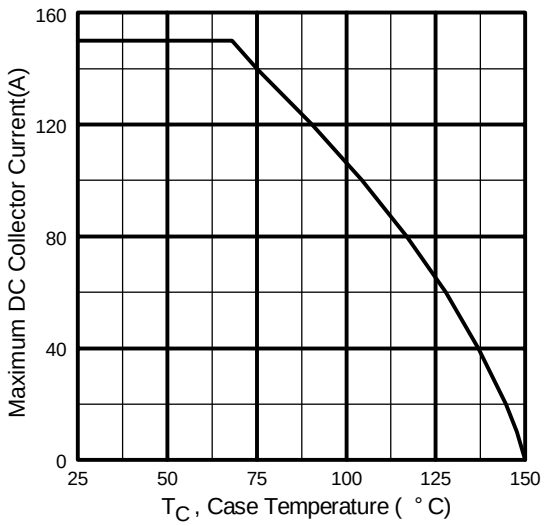


Fig. 3 - Maximum Collector Current vs. Case Temperature

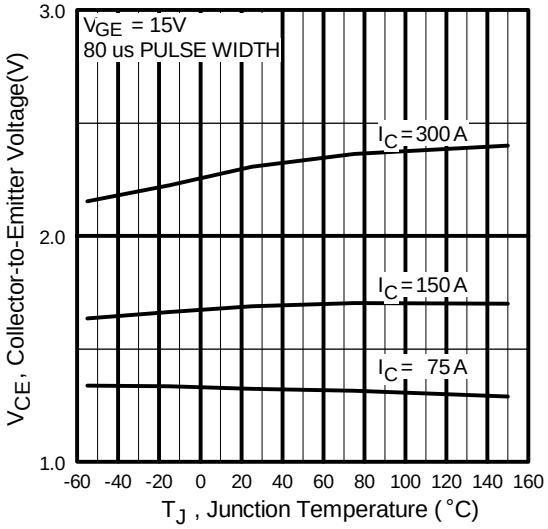


Fig. 4 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

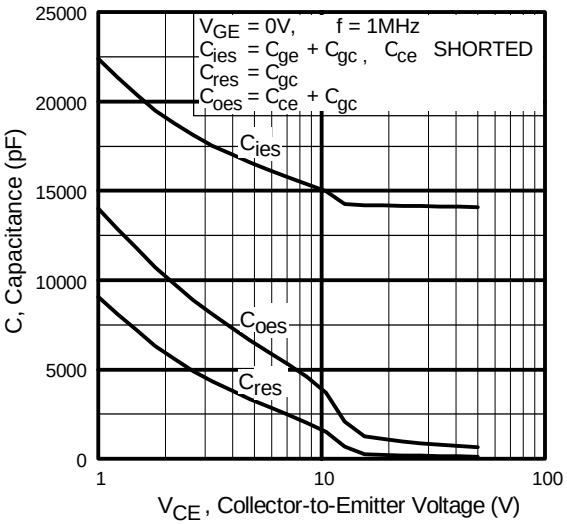


Fig. 5 - Typical Capacitance vs. Collector-to-Emitter Voltage

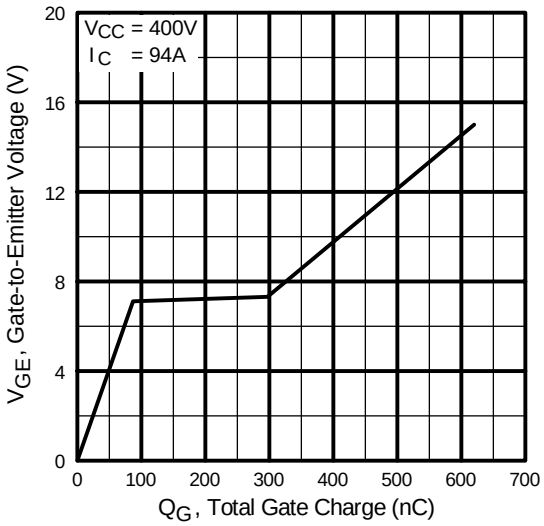


Fig. 6 - Typical Gate Charge vs. Gate-to-Emitter Voltage

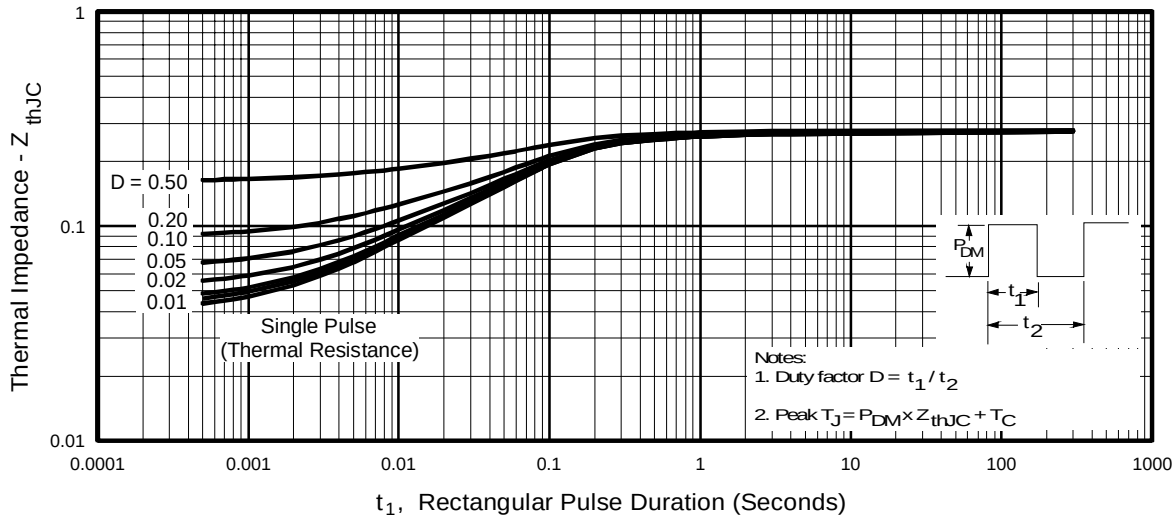


Fig. 7 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

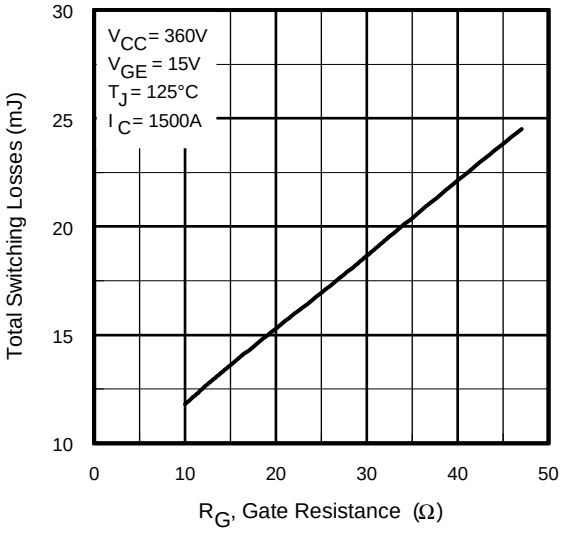


Fig. 8 - Typical Switching Losses vs. Gate Resistance

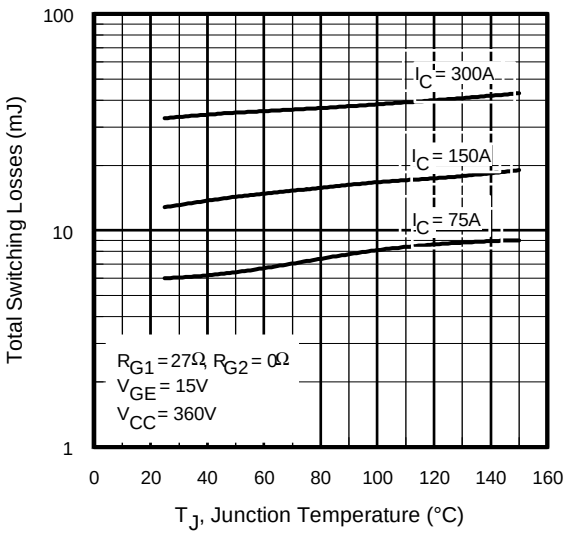


Fig. 9 - Typical Switching Losses vs. Junction Temperature

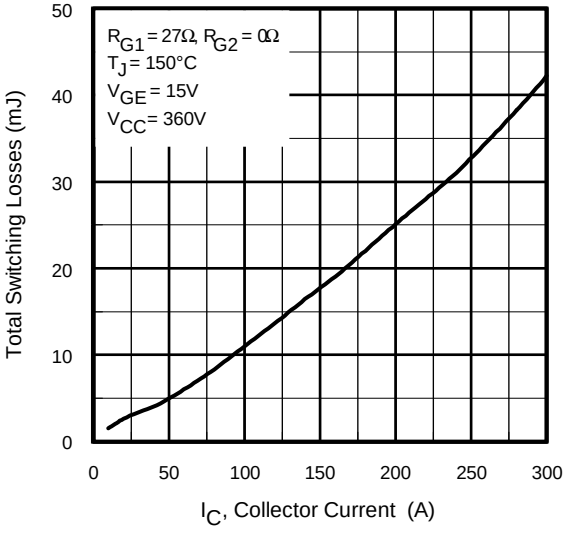


Fig. 10 - Typical Switching Losses vs. Collector-to-Emitter Current

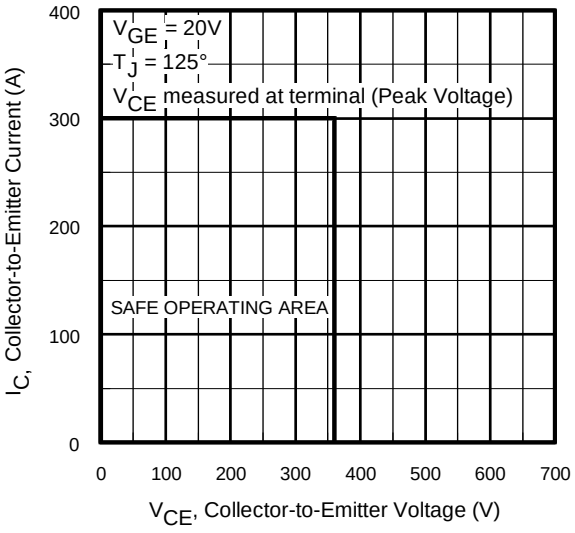


Fig. 11 - Reverse Bias SOA

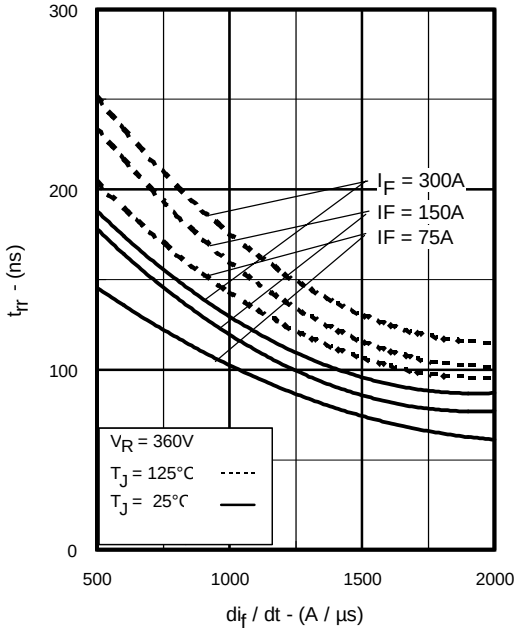


Fig. 12 - Typical Reverse Recovery vs. di_f/dt

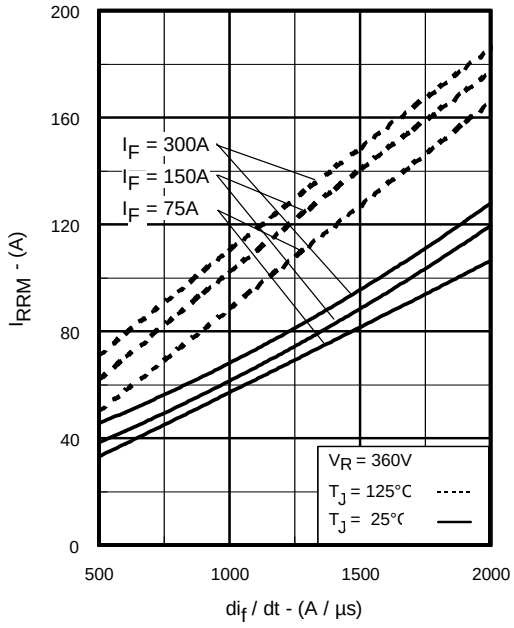


Fig. 13 - Typical Recovery Current vs. di_f/dt

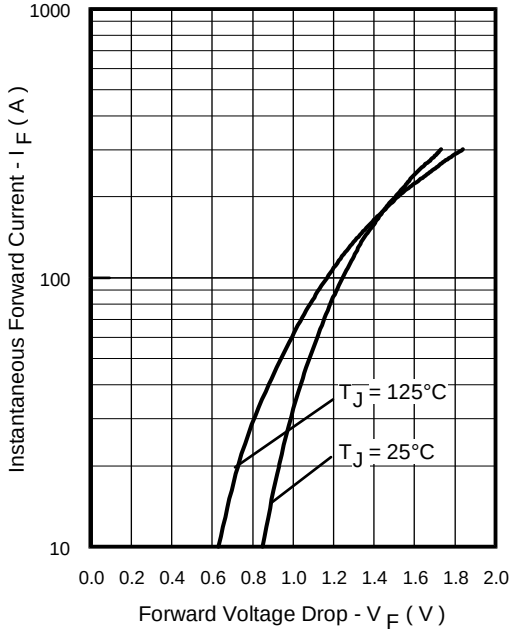


Fig. 14 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

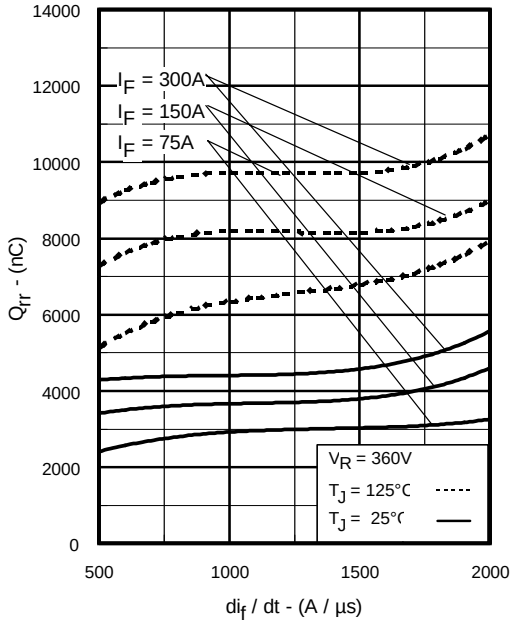
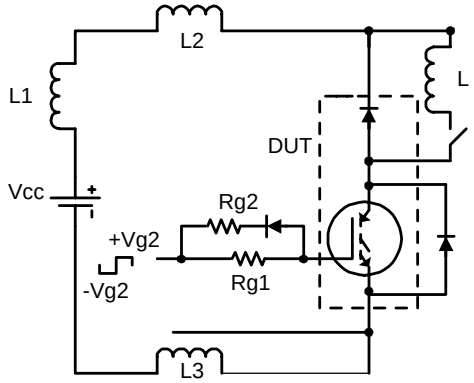


Fig. 15 - Typical Stored Charge vs. di_f/dt



Vcc=60% of BVces
Ls= L1+L2+L3
Vge=15V

Fig. 16a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

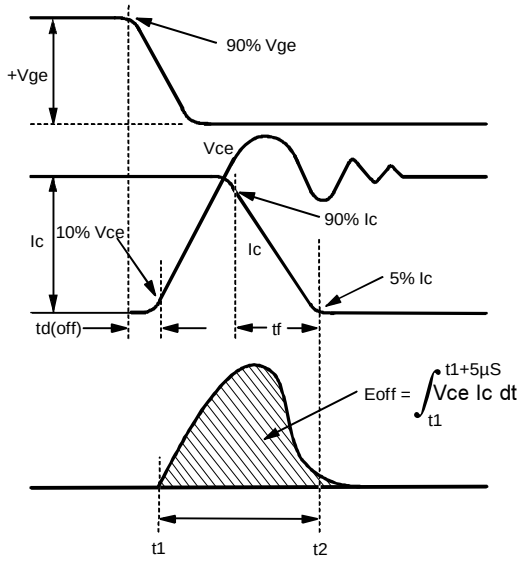


Fig. 16b - Test Waveforms for Circuit of Fig. 16a, Defining E_{off}, $t_{d(off)}$, t_f

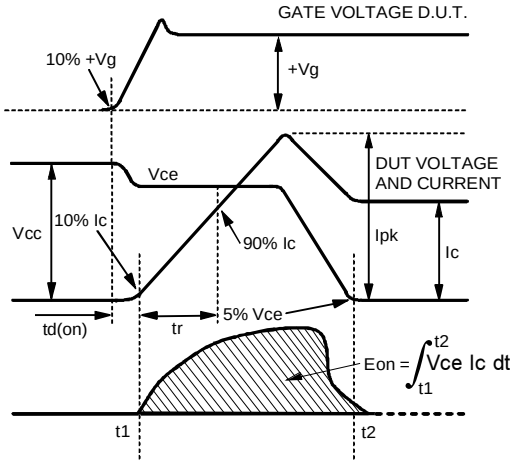


Fig. 16c - Test Waveforms for Circuit of Fig. 16a, Defining E_{on}, $t_{d(on)}$, t_r

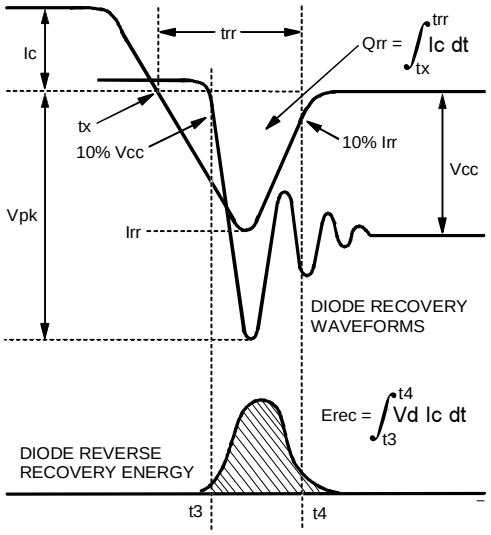


Fig. 16d - Test Waveforms for Circuit of Fig. 16a Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

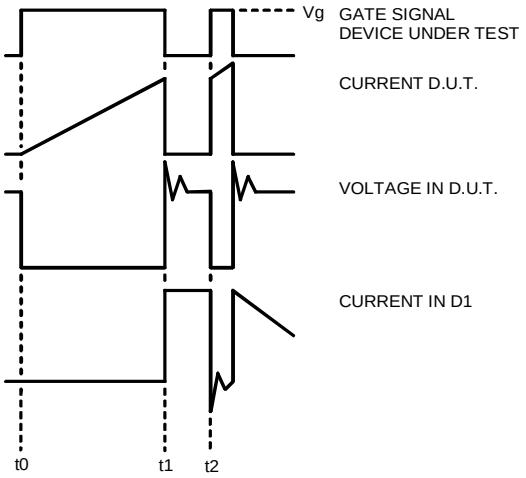


Figure 16e. Macro Waveforms for Figure 17's Test Circuit

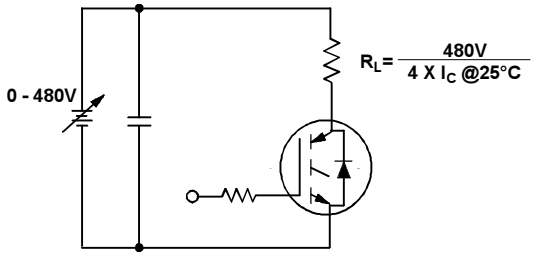


Figure 17. Pulsed Collector Current
Test Circuit

Notes:

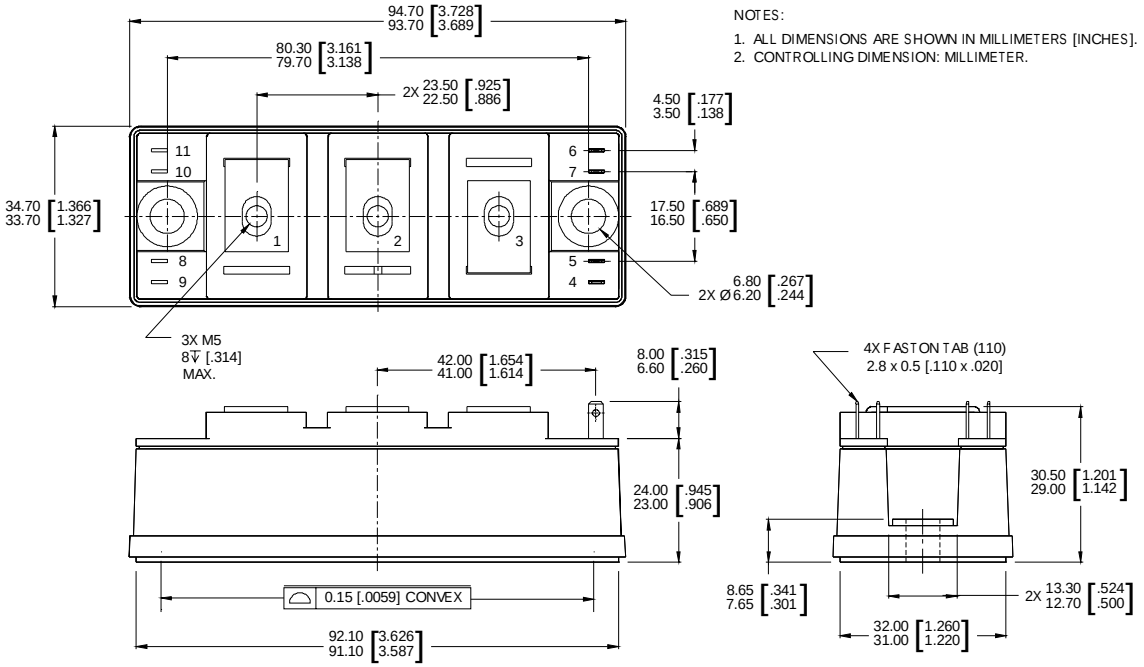
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 16

③ For screws M5x0.8

④ Pulse width 80µs; single shot.

Case Outline — INT-A-PAK



Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.11/01

International
IOR Rectifier

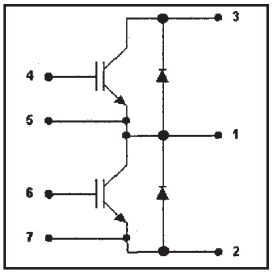
GA150TS60U

"HALF-BRIDGE" IGBT INT-A-PAK

Ultra-Fast™ Speed IGBT

Features

- Generation 4 IGBT technology
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL approved



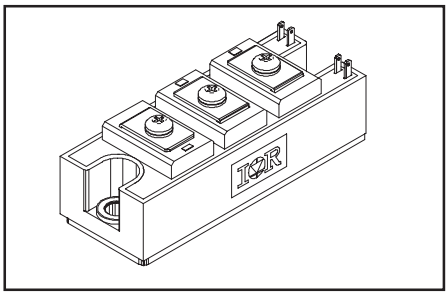
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.7V

@V_{GE} = 15V, I_C = 150A

Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	150	A
I_{CM}	Pulsed Collector Current①	300	
I_{LM}	Peak Switching Current②	300	
I_{FM}	Peak Diode Forward Current	300	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	440	W
P_D @ T_C = 85°C	Maximum Power Dissipation	230	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.28	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.35	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3③	—	3.0	
	Weight of Module	200	—	g

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	1.7	2.3		V_{GE} = 15V, I_C = 150A
		—	1.7	—		V_{GE} = 15V, I_C = 150A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		I_C = 750µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 750µA
g_{fe}	Forward Transconductance ④	—	152	—	S	V_{CE} = 25V, I_C = 150A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	1.0	mA	V_{GE} = 0V, V_{CE} = 600V
		—	—	10		V_{GE} = 0V, V_{CE} = 600V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	3.3	—	V	I_F = 150A, V_{GE} = 0V
		—	3.2	—		I_F = 150A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	250	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	624	937	nC	V_{CC} = 400V
Q_{ge}	Gate - Emitter Charge (turn-on)	—	87	130		I_C = 94A
Q_{gc}	Gate - Collector Charge (turn-on)	—	212	317		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	241	—	ns	R_{G1} = 27Ω, R_{G2} = 0Ω,
t_r	Rise Time	—	145	—		I_C = 150A
$t_{d(off)}$	Turn-Off Delay Time	—	336	—		V_{CC} = 360V
t_f	Fall Time	—	227	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	6.0	—	mJ	
$E_{off\ (1)}$	Turn-Off Switching Energy	—	12	—		
$E_{ts\ (1)}$	Total Switching Energy	—	19	33		
C_{ies}	Input Capacitance	—	14000	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	860	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	180	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	172	—	ns	I_C = 150A
I_{rr}	Diode Peak ReverseCurrent	—	113	—	A	R_{G1} = 27Ω
Q_{rr}	Diode Recovery Charge	—	9696	—	nC	R_{G2} = 0Ω
$di_{(rec)}M_{/dt}$	Diode Peak Rate of Fall of Recovery During t_b	—	2000	—	A/µs	V_{CC} = 360V di/dt =1300A/µs

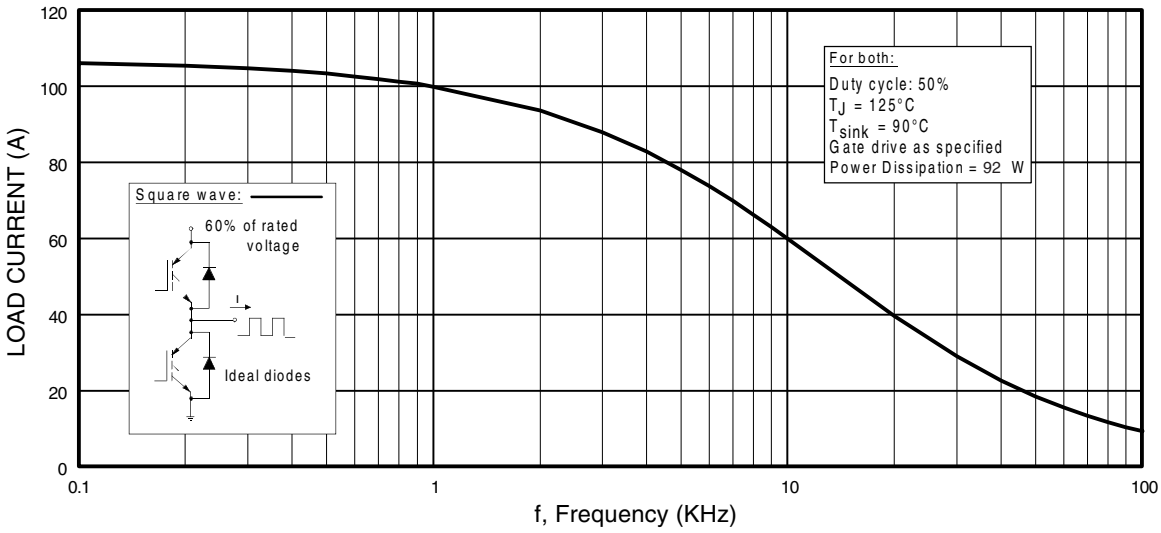


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

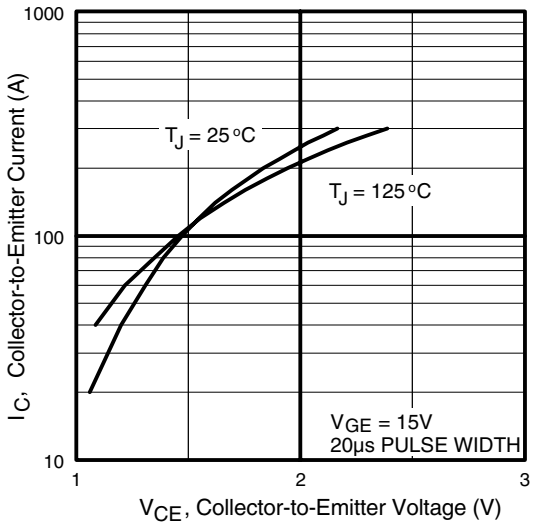


Fig. 2 - Typical Output Characteristics

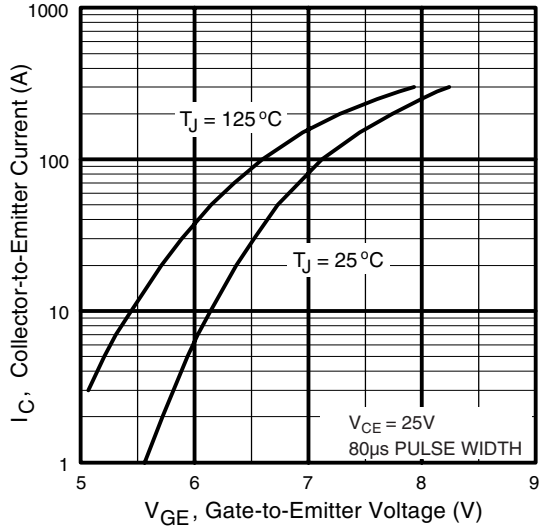


Fig. 3 - Typical Transfer Characteristics

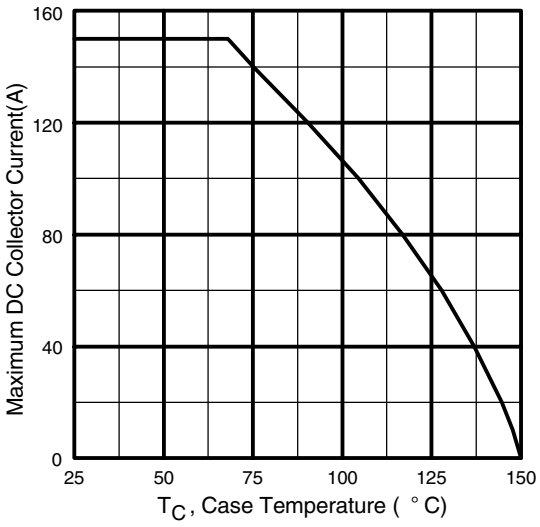


Fig. 4 - Maximum Collector Current vs. Case Temperature

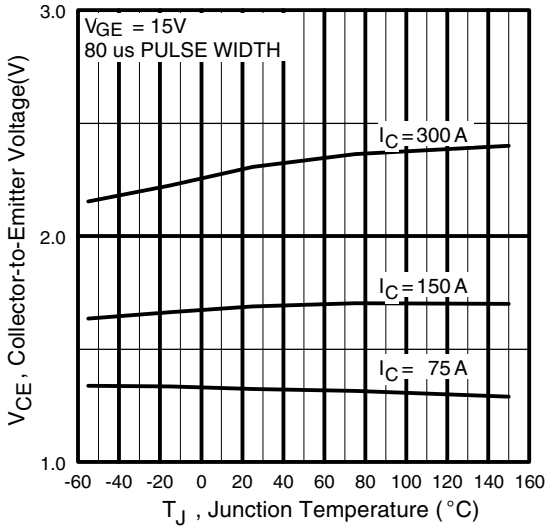


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

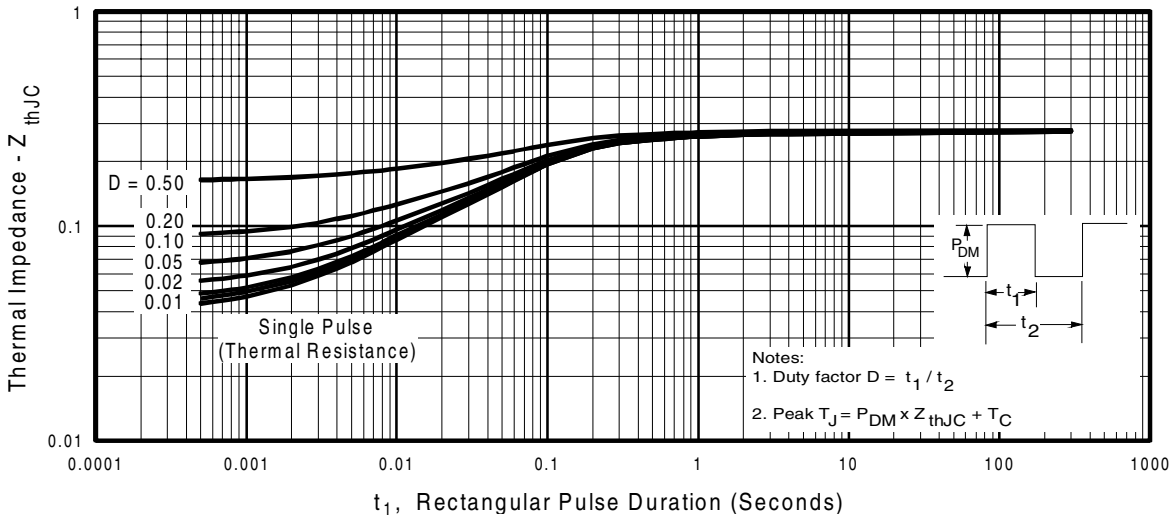


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

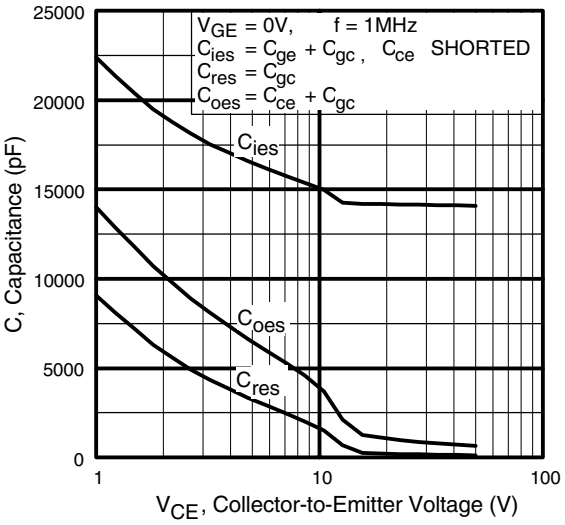


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

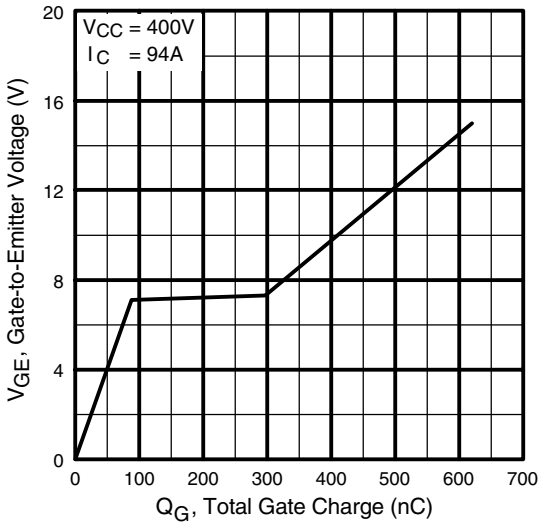


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

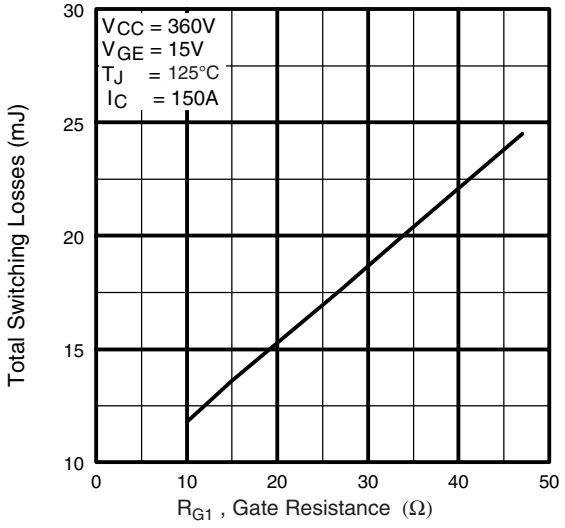


Fig. 9 - Typical Switching Losses vs. Gate Resistance

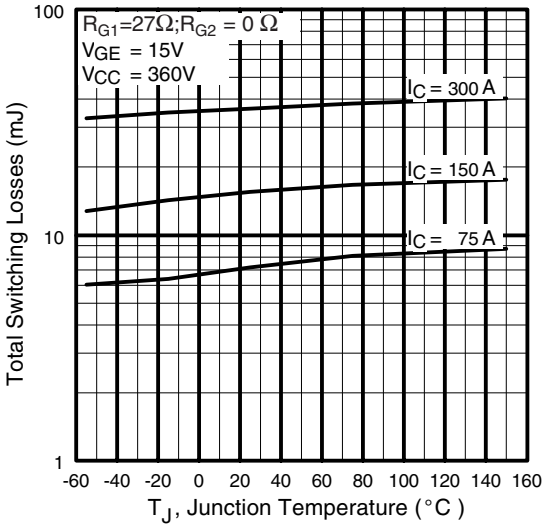


Fig. 10 - Typical Switching Losses vs. Junction Temperature

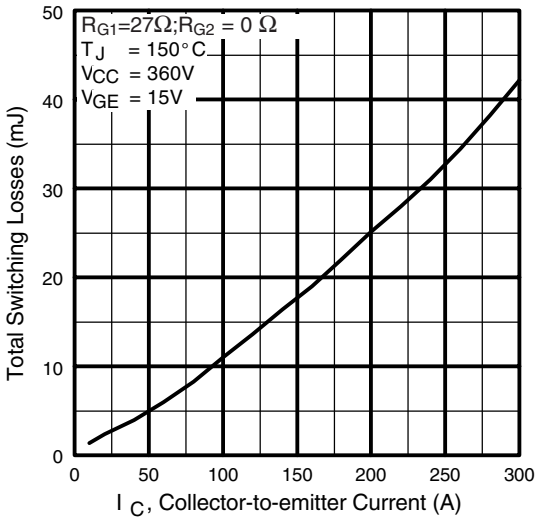


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

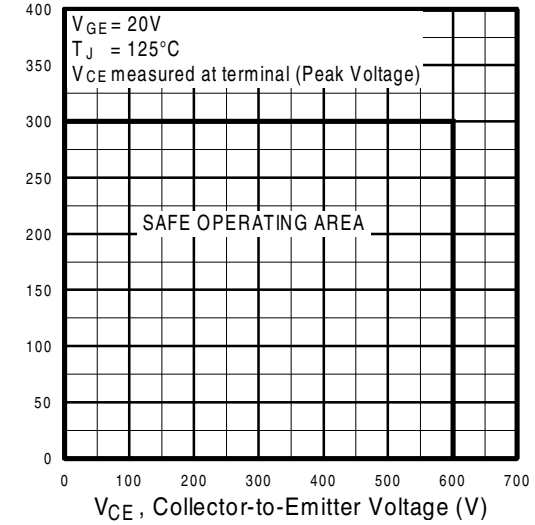


Fig. 12 - Reverse Bias SOA

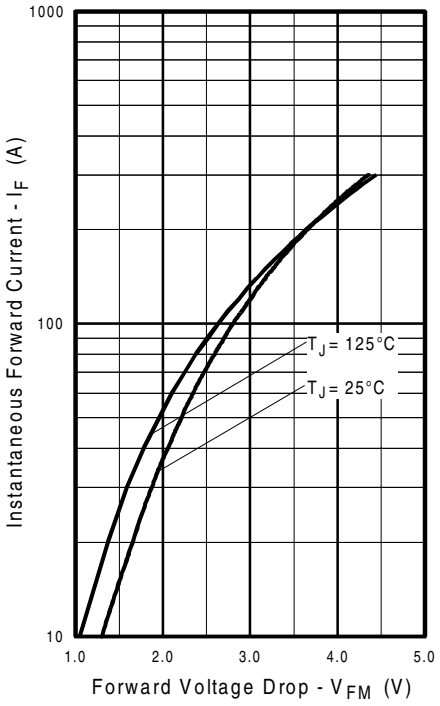


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

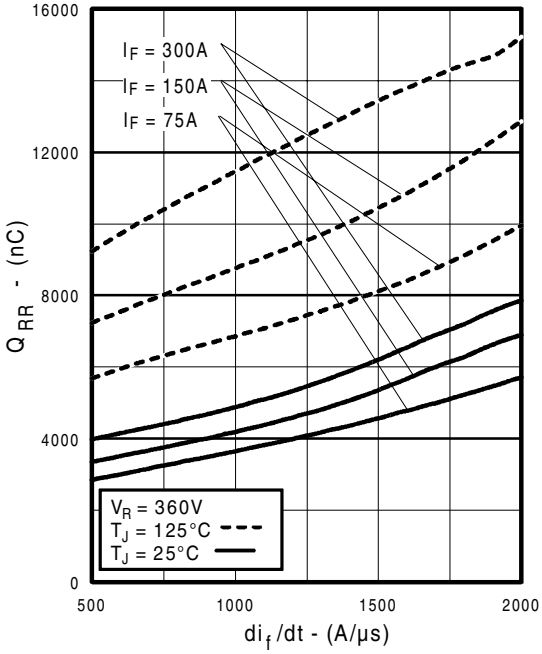


Fig. 14 - Typical Stored Charge vs. di_f/dt

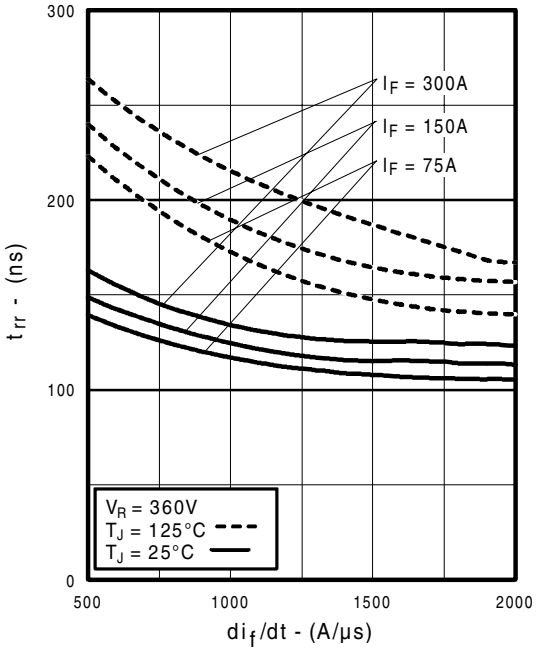


Fig. 15 - Typical Reverse Recovery vs. di_f/dt

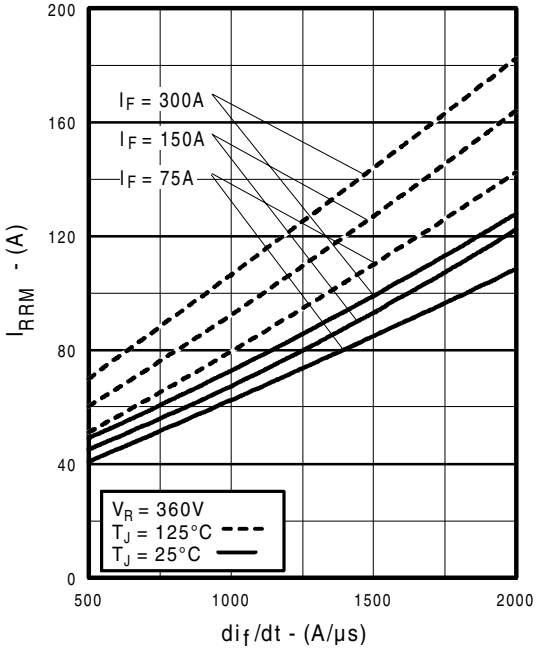


Fig. 16 - Typical Recovery Current vs. di_f/dt

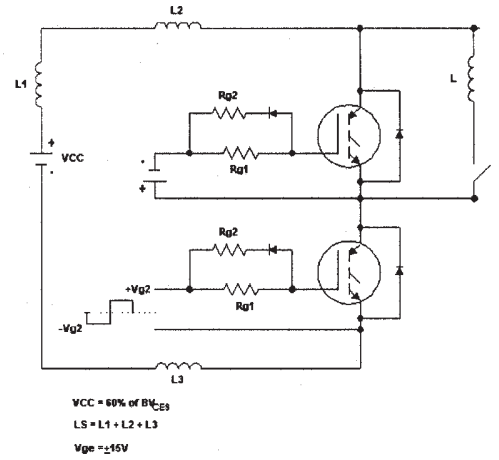


Fig. 17 - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

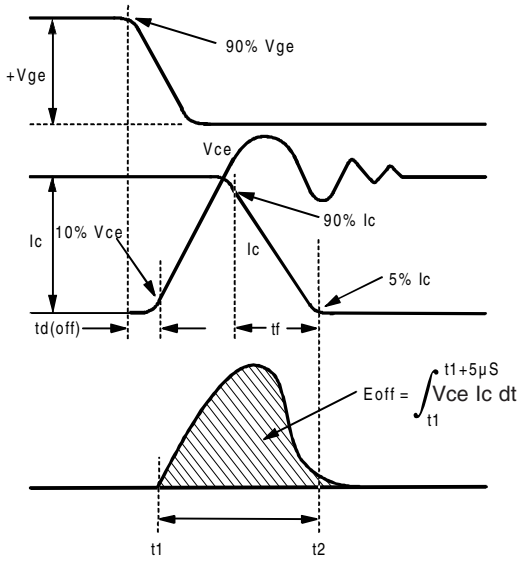


Fig. 18 - Test Waveforms for Circuit of Fig. 17, Defining E_{off}, $t_{d(off)}$, t_f

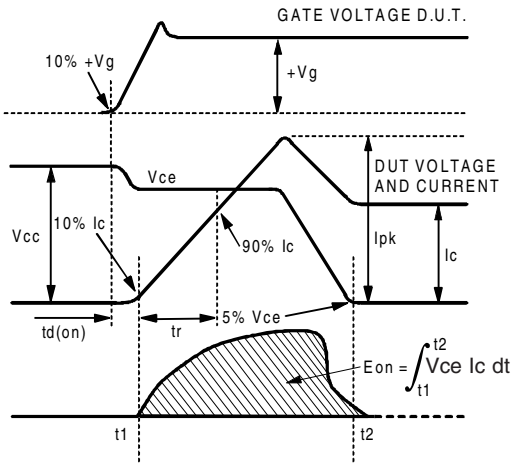


Fig. 19 - Test Waveforms for Circuit of Fig. 17, Defining E_{on}, $t_{d(on)}$, t_r

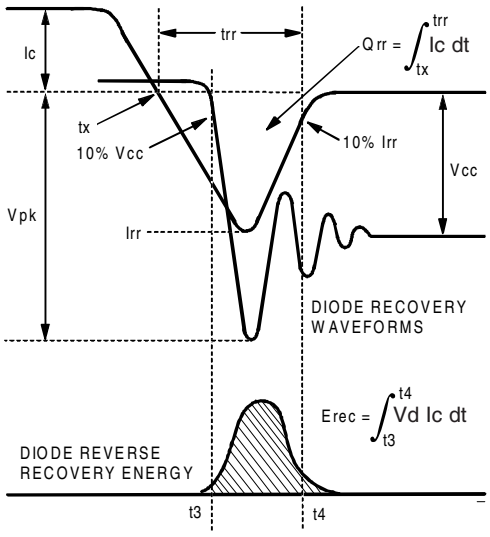


Fig. 20 - Test Waveforms for Circuit of Fig. 17, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

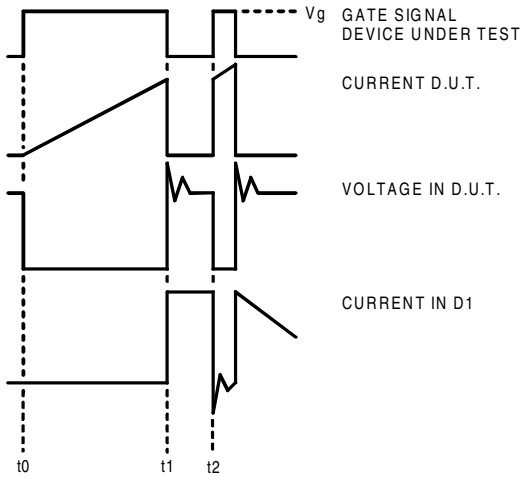


Figure 21. Macro Waveforms for Figure 17's Test Circuit

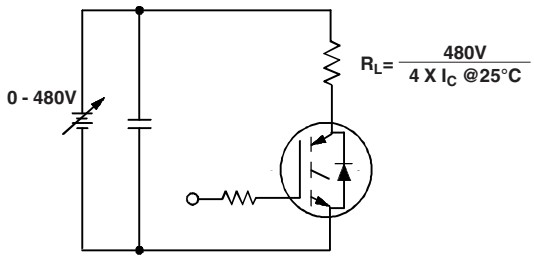


Figure 22. Pulsed Collector Current
Test Circuit

Notes:

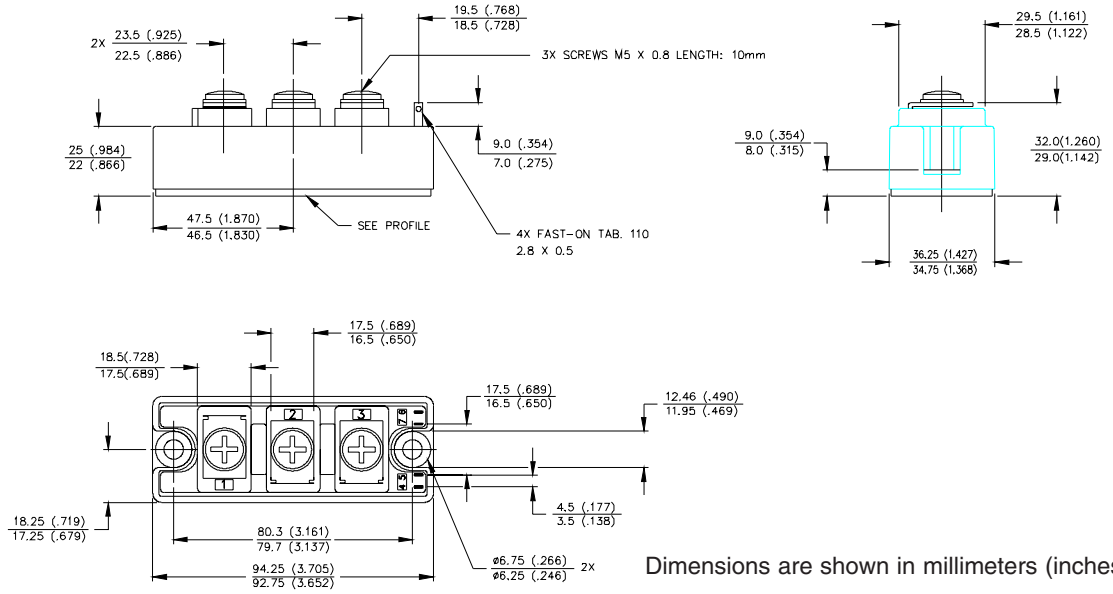
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 17

③ For screws M5x0.8

④ Pulse width 80µs; single shot.

Case Outline — INT-A-PAK



Dimensions are shown in millimeters (inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD -94347

International
IOR Rectifier

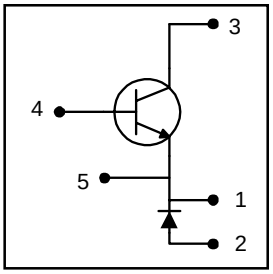
GA200NS61U

IGBT INT-A-PAK

High Side Switch Chopper Module
Ultra-Fast™ Speed IGBT

Features

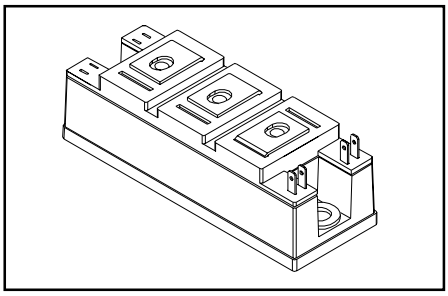
- Generation 4 IGBT technology
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL approved



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.8V

@V_{GE} = 15V, I_C = 200A



Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	200	A
I_{CM}	Pulsed Collector Current①	400	
I_{LM}	Peak Switching Current②	400	
I_{FM}	Peak Diode Forward Current	400	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	625	W
P_D @ T_C = 85°C	Maximum Power Dissipation	325	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.20	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.35	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3③	—	3.0	
	Weight of Module	200	—	g

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	1.8	2.2		V_{GE} = 15V, I_C = 200A
		—	1.9	—		V_{GE} = 15V, I_C = 200A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		I_C = 1.25mA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.25mA
g_{fe}	Forward Transconductance ④	—	175	—	S	V_{CE} = 25V, I_C = 200A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	1.0	mA	V_{GE} = 0V, V_{CE} = 600V
		—	—	10		V_{GE} = 0V, V_{CE} = 600V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	1.6	2.2	V	I_F = 200A, V_{GE} = 0V
		—	1.7	—		I_F = 200A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	250	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	903	1355	nC	V_{CC} = 400V, V_{GE} = 15V
Q_{ge}	Gate - Emitter Charge (turn-on)	—	125	188		I_C = 135A
Q_{gc}	Gate - Collector Charge (turn-on)	—	306	459		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	342	—	ns	R_{G1} = 27Ω, R_{G2} = 0Ω,
t_r	Rise Time	—	194	—		I_C = 200A
$t_{d(off)}$	Turn-Off Delay Time	—	366	—		V_{CC} = 360V
t_f	Fall Time	—	213	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	12	—	mJ	Inductive load
$E_{off\ (1)}$	Turn-Off Switching Energy	—	16	—		
$E_{ts\ (1)}$	Total Switching Energy	—	28	39		
C_{ies}	Input Capacitance	—	20068	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	1254	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	261	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	137	—	ns	I_C = 200A
I_{rr}	Diode Peak ReverseCurrent	—	96	—	A	R_{G1} = 27Ω
Q_{rr}	Diode Recovery Charge	—	6731	—	µC	R_{G2} = 0Ω
$di_{(rec)}M/dt$	Diode Peak Rate of Fall of Recovery During t_b	—	5705	—	A/µs	V_{CC} = 360V di/dt=1227A/µs

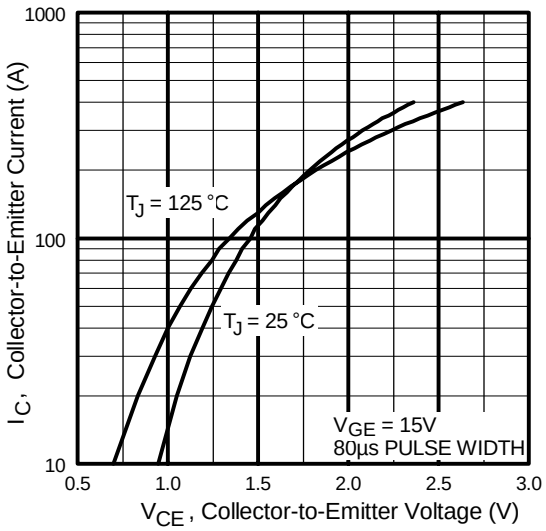


Fig. 1 - Typical Output Characteristics

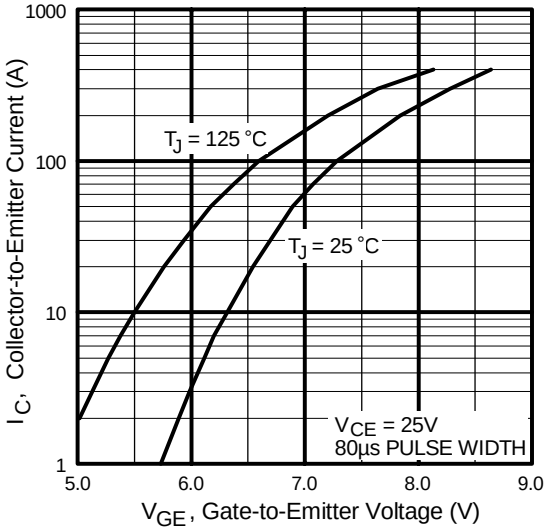


Fig. 2 - Typical Transfer Characteristics

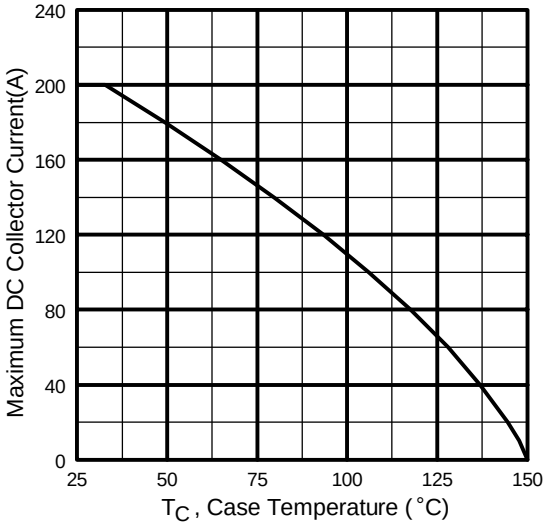


Fig. 3 - Maximum Collector Current vs. Case Temperature

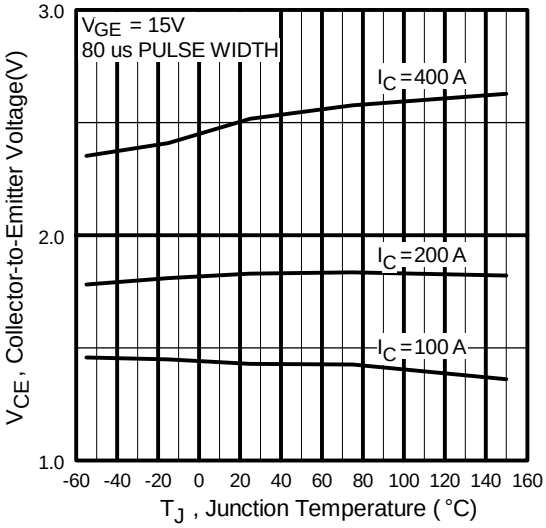


Fig. 4- Typical Collector-to-Emitter Voltage vs. Junction Temperature

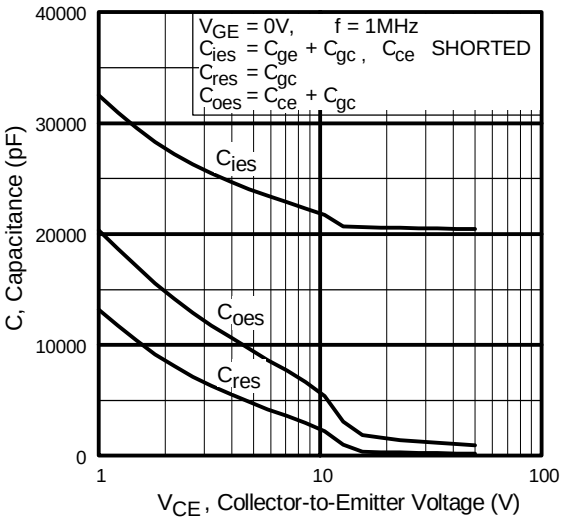


Fig. 5 - Typical Capacitance vs. Collector-to-Emitter Voltage

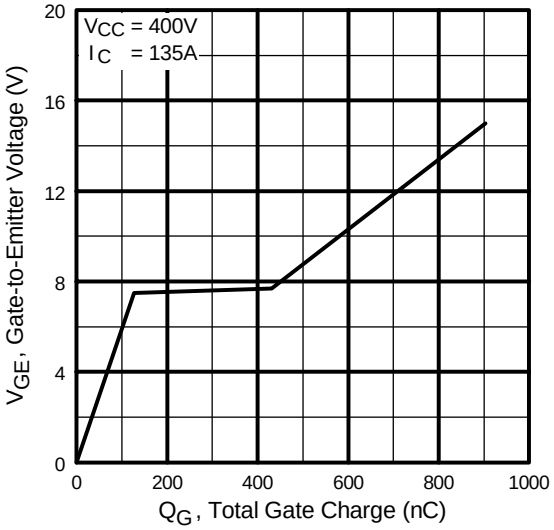


Fig. 6 - Typical Gate Charge vs. Gate-to-Emitter Voltage

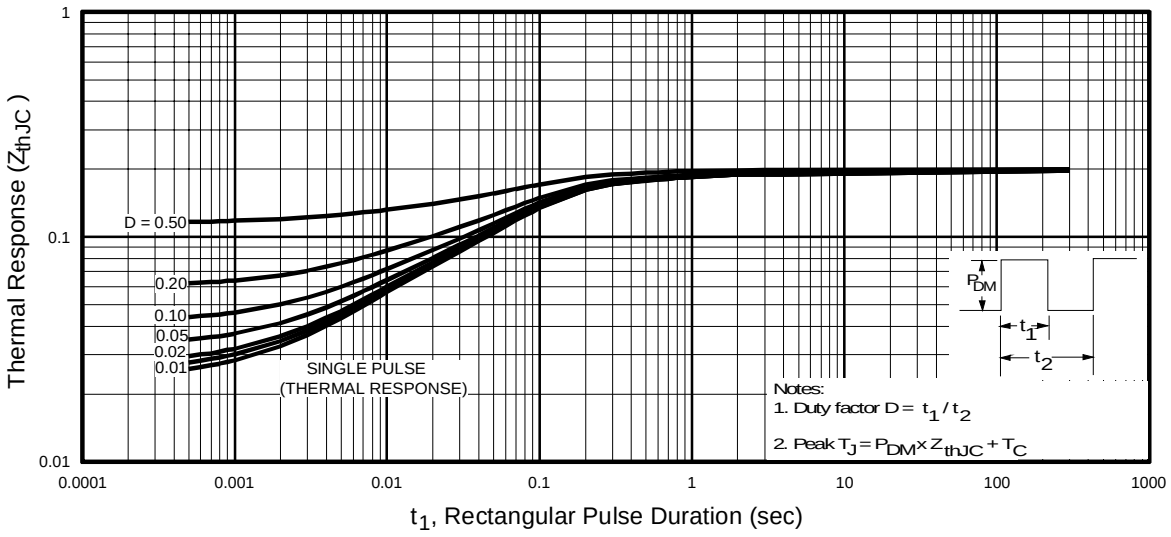


Fig. 7 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

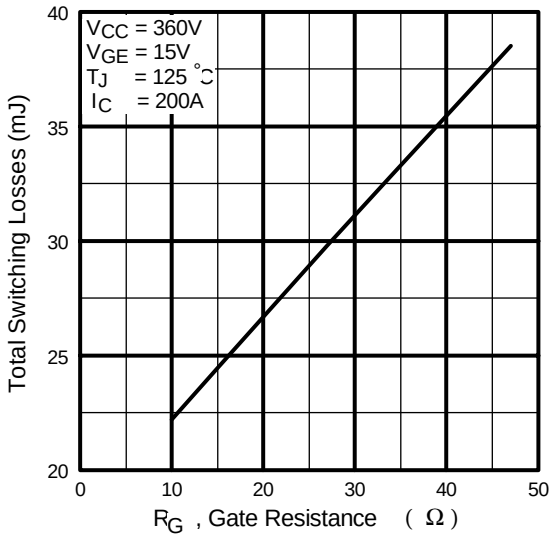


Fig. 8 - Typical Switching Losses vs. Gate Resistance

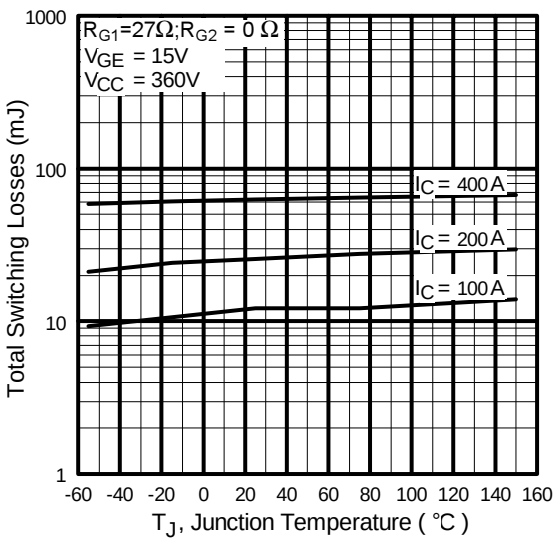


Fig. 9 - Typical Switching Losses vs. Junction Temperature

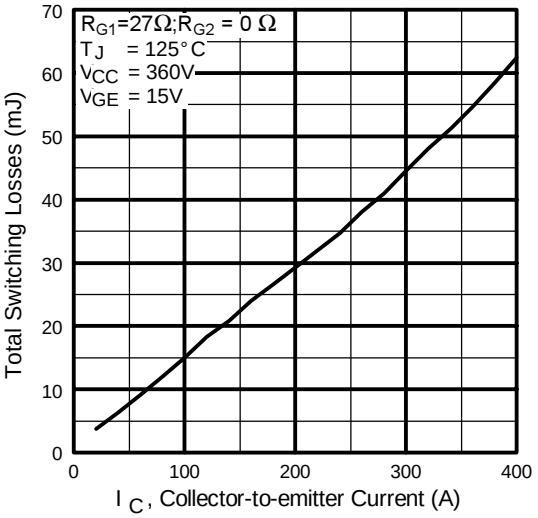


Fig. 10 - Typical Switching Losses vs. Collector-to-Emitter Current

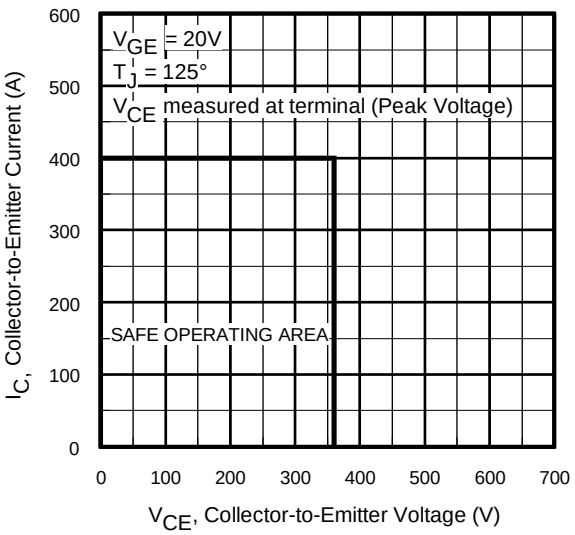


Fig. 11 - Reverse Bias SOA

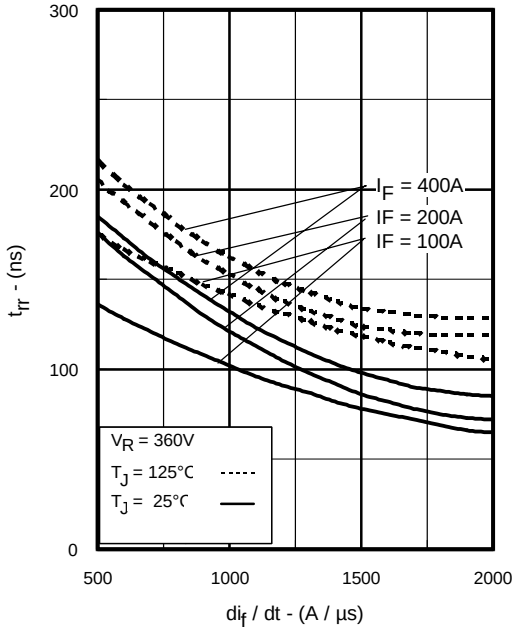


Fig. 12 - Typical Reverse Recovery vs. di_f/dt

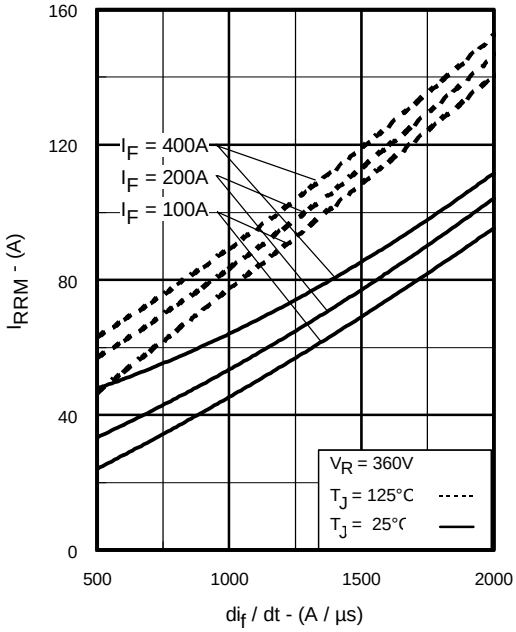


Fig. 13 - Typical Recovery Current vs. di_f/dt

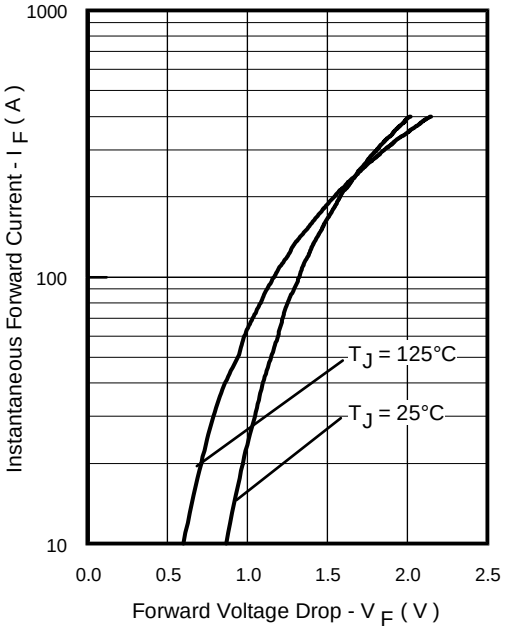


Fig. 14 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

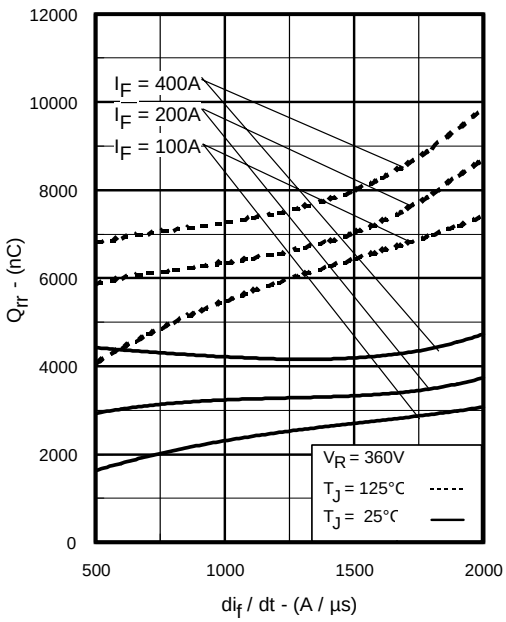


Fig. 15 - Typical Stored Charge vs. di_f/dt

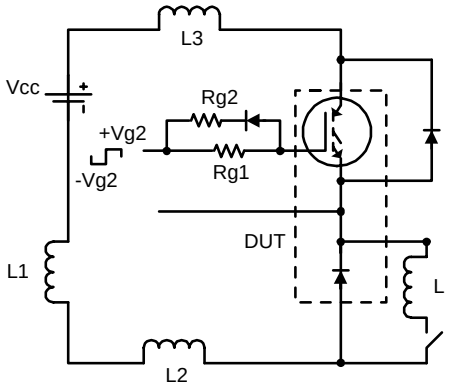


Fig. 16a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

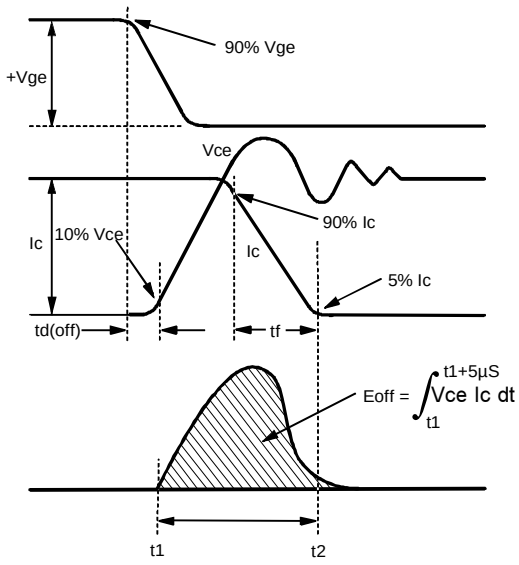


Fig. 16b - Test Waveforms for Circuit of Fig. 16a, Defining E_{off}, $t_{d(off)}$, t_f

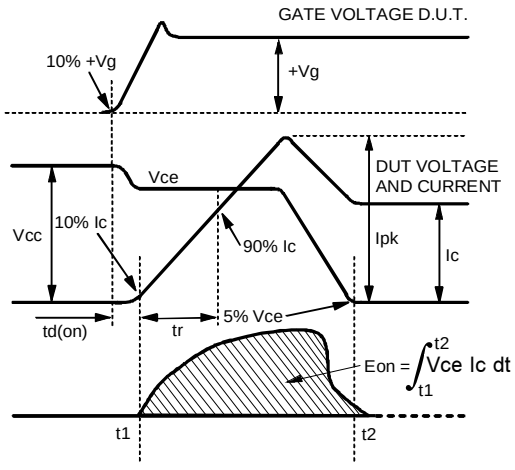


Fig. 16c - Test Waveforms for Circuit of Fig. 16a, Defining E_{on}, $t_{d(on)}$, t_r

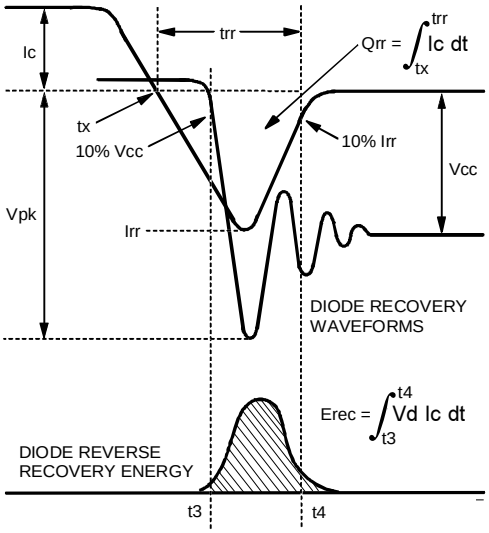


Fig. 16d - Test Waveforms for Circuit of Fig. 16a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

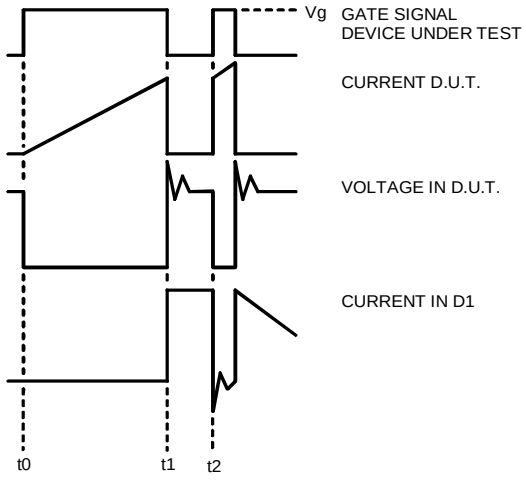


Figure 16e. Macro Waveforms for Figure 18a's Test Circuit

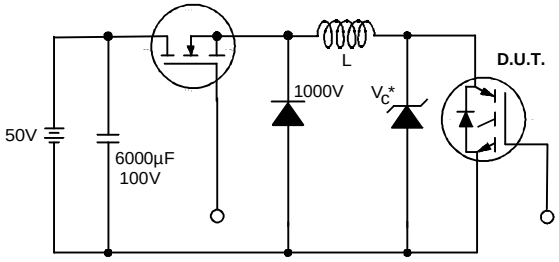


Figure 17. Clamped Inductive Load Test Circuit

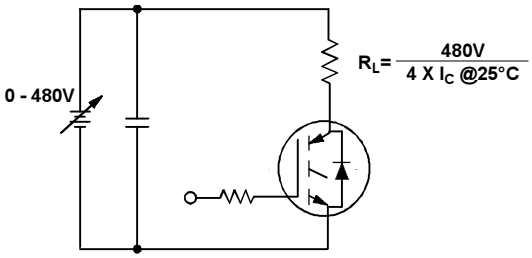


Figure 18. Pulsed Collector Current Test Circuit

Notes:

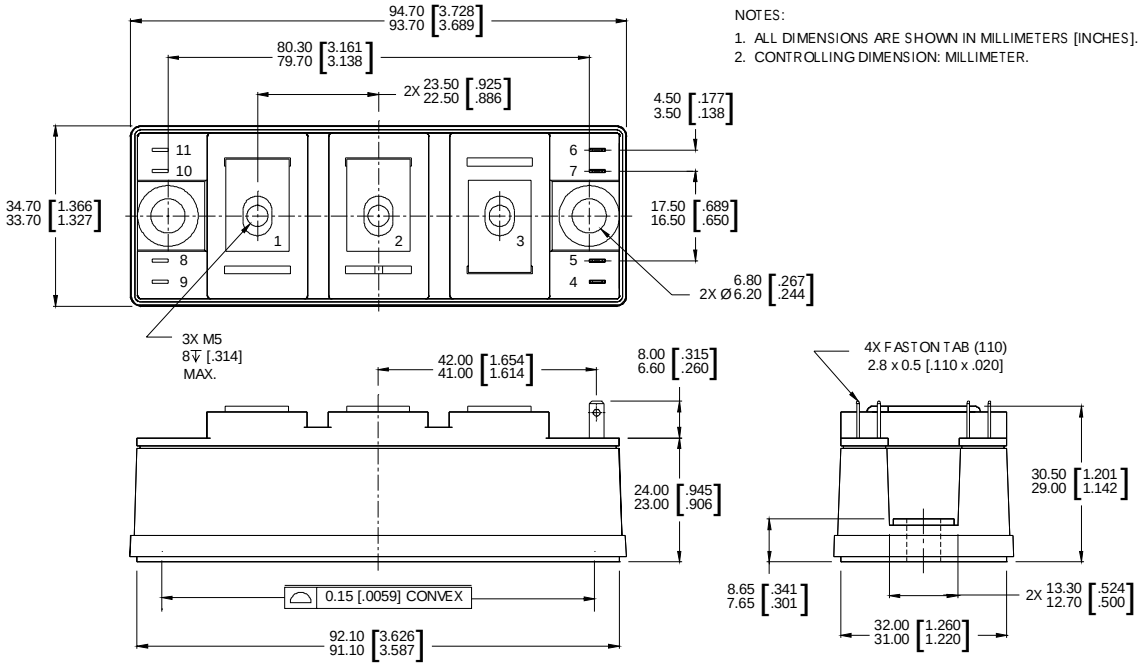
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 16

③ For screws M5x0.8

④ Pulse width 50µs; single shot.

Case Outline — INT-A-PAK



Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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TAC Fax: (310) 252-7903
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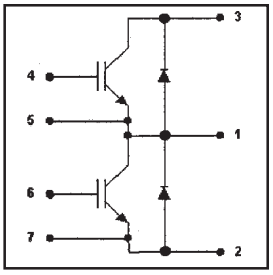
GA200TS60U

"HALF-BRIDGE" IGBT INT-A-PAK

Ultra-Fast™ Speed IGBT

Features

- Generation 4 IGBT technology
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL approved



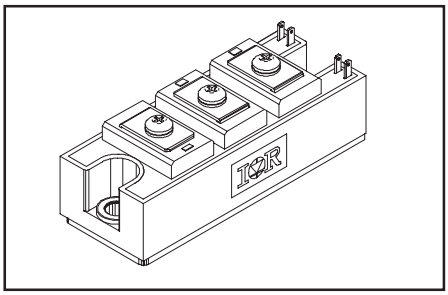
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.8V

@V_{GE} = 15V, I_C = 200A

Benefits

- Increased operating efficiency
- Direct mounting to heatsink
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- Lower EMI, requires less snubbing



Absolute Maximum Ratings

	Parameter	Max.	Units
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I_C @ T_C = 25°C	Continuous Collector Current	200	A
I_{CM}	Pulsed Collector Current①	400	
I_{LM}	Peak Switching Current②	400	
I_{FM}	Peak Diode Forward Current	400	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	625	W
P_D @ T_C = 85°C	Maximum Power Dissipation	325	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.20	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.35	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3③	—	3.0	
	Weight of Module	200	—	g

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	1.8	2.2		V_{GE} = 15V, I_C = 200A
		—	1.9	—		V_{GE} = 15V, I_C = 200A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		I_C = 1.25mA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.25mA
g_{fe}	Forward Transconductance ④	—	175	—	S	V_{CE} = 25V, I_C = 200A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	1.0	mA	V_{GE} = 0V, V_{CE} = 600V
		—	—	10		V_{GE} = 0V, V_{CE} = 600V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	3.7	—	V	I_F = 200A, V_{GE} = 0V
		—	3.7	—		I_F = 200A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	250	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	903	1355	nC	V_{CC} = 400V, V_{GE} = 15V
Q_{ge}	Gate - Emitter Charge (turn-on)	—	125	188		I_C = 135A
Q_{gc}	Gate - Collector Charge (turn-on)	—	306	459		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	342	—	ns	R_{G1} = 27Ω, R_{G2} = 0Ω,
t_r	Rise Time	—	194	—		I_C = 200A
$t_{d(off)}$	Turn-Off Delay Time	—	366	—		V_{CC} = 360V
t_f	Fall Time	—	213	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	12	—	mJ	
$E_{off\,(1)}$	Turn-Off Switching Energy	—	16	—		
$E_{ts\,(1)}$	Total Switching Energy	—	28	39		
C_{ies}	Input Capacitance	—	20068	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	1254	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	261	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	179	—	ns	I_C = 200A
I_{rr}	Diode Peak ReverseCurrent	—	120	—	A	R_{G1} = 27Ω
Q_{rr}	Diode Recovery Charge	—	10714	—	µC	R_{G2} = 0Ω
$di_{(rec)}M/dt$	Diode Peak Rate of Fall of Recovery During t_b	—	1922	—	A/µs	V_{CC} = 360V di/dt=1300A/µs

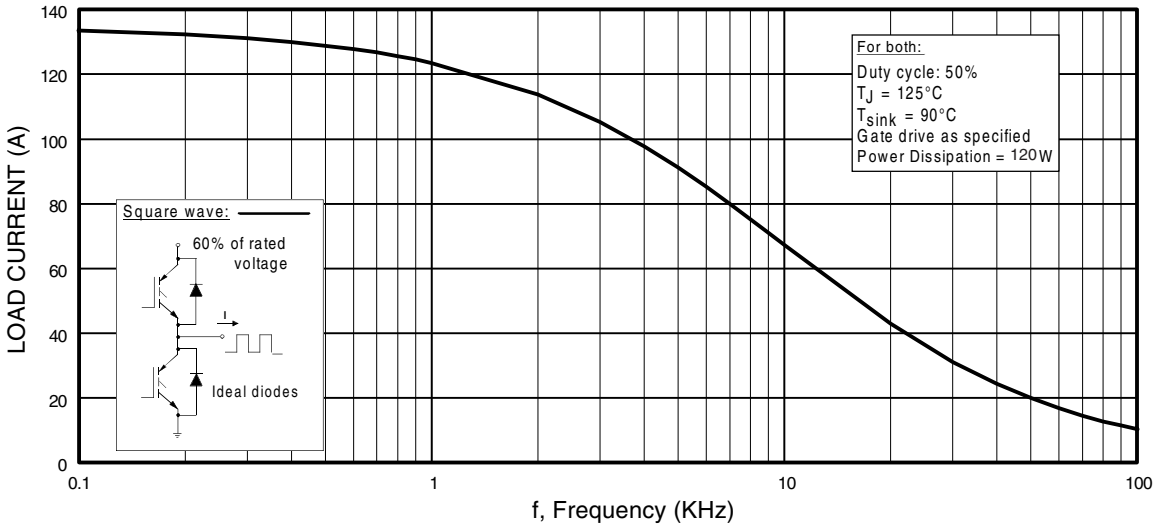


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

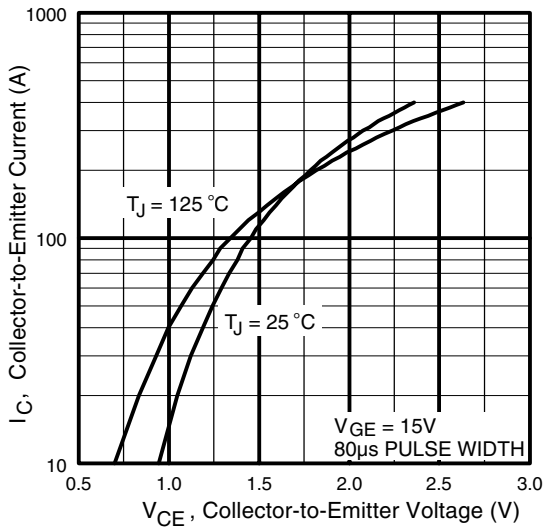


Fig. 2 - Typical Output Characteristics

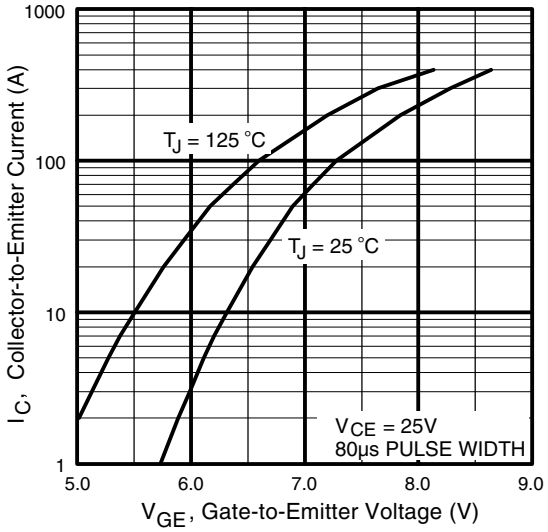


Fig. 3 - Typical Transfer Characteristics

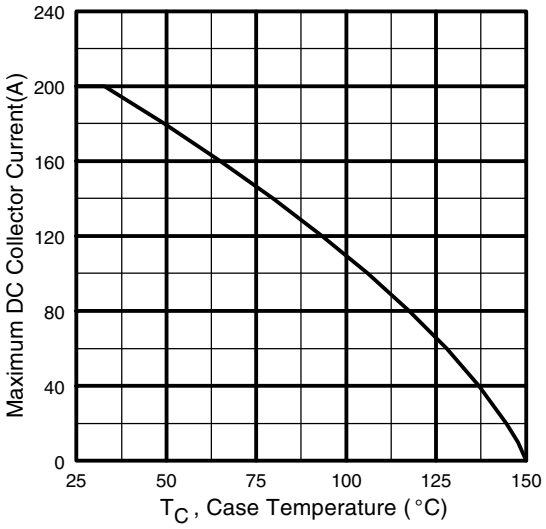


Fig. 4 - Maximum Collector Current vs. Case Temperature

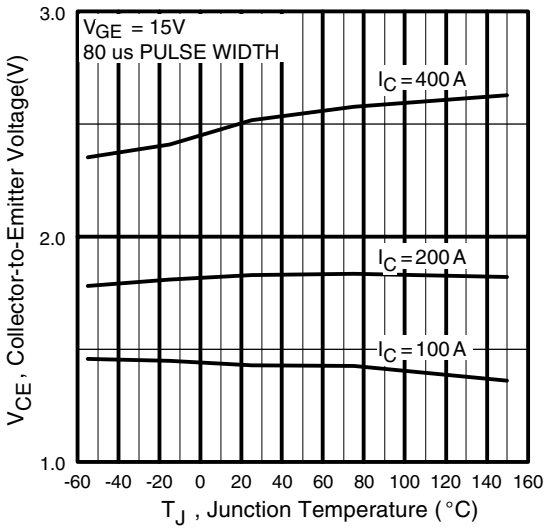


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

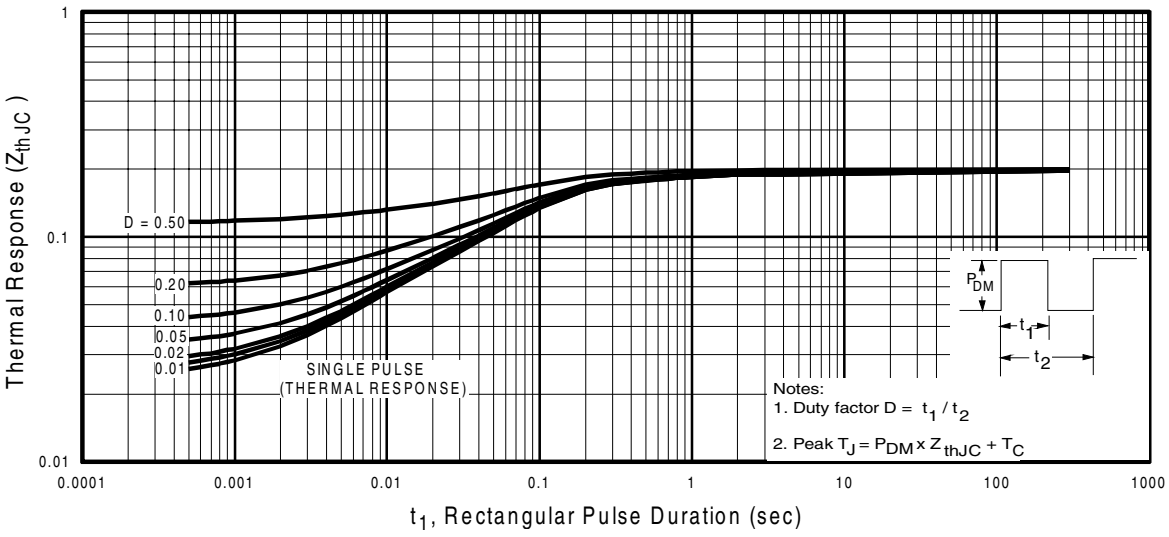


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

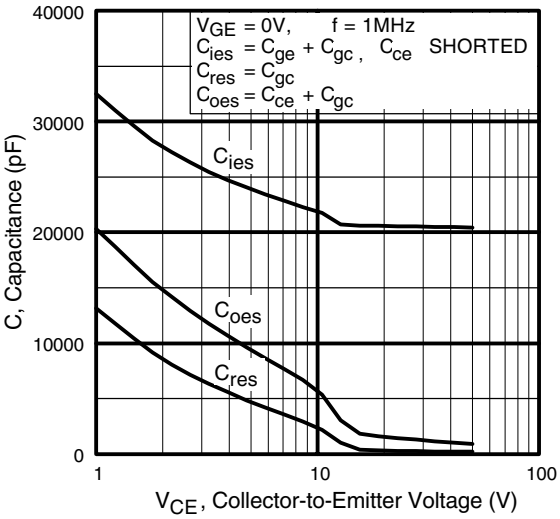


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

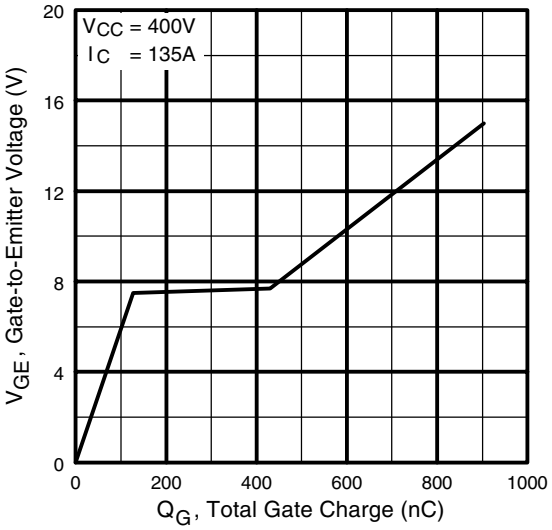


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

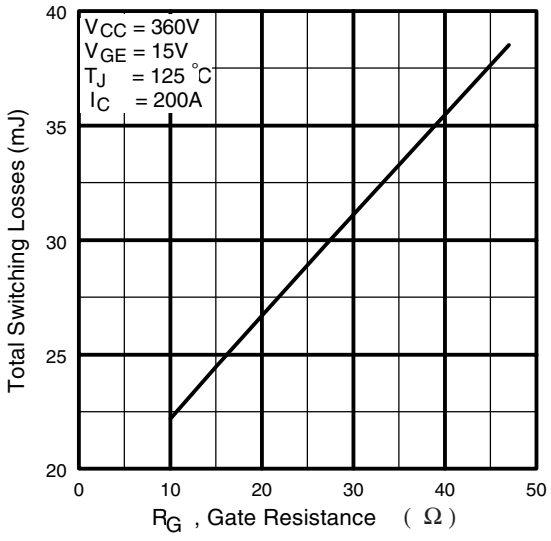


Fig. 9 - Typical Switching Losses vs. Gate Resistance

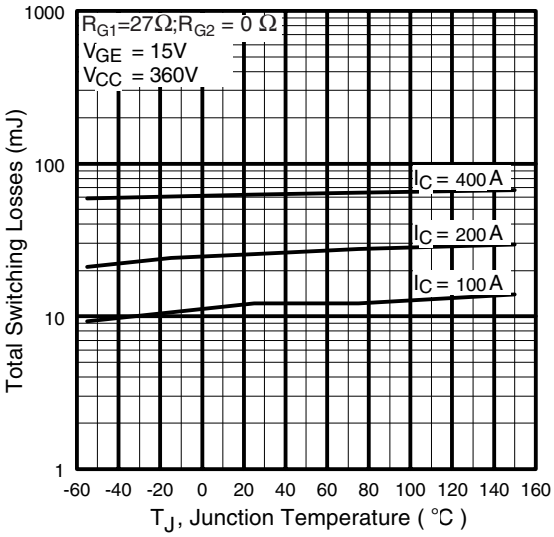


Fig. 10 - Typical Switching Losses vs. Junction Temperature

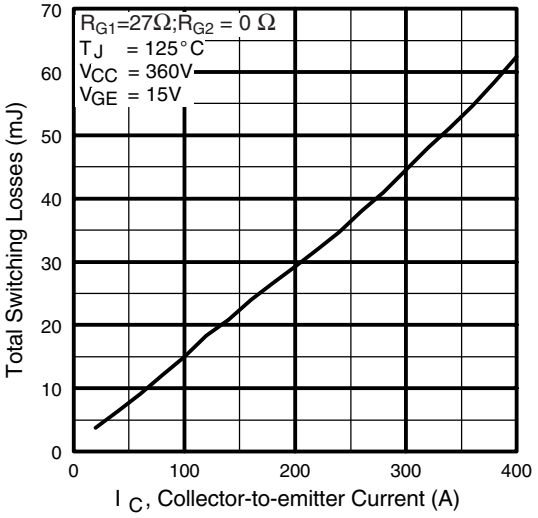


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

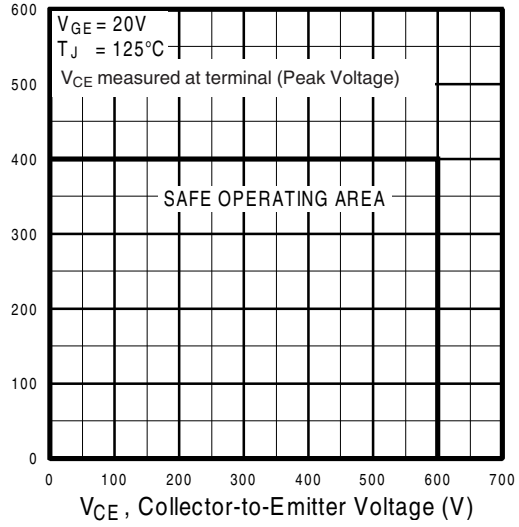


Fig. 12 - Reverse Bias SOA

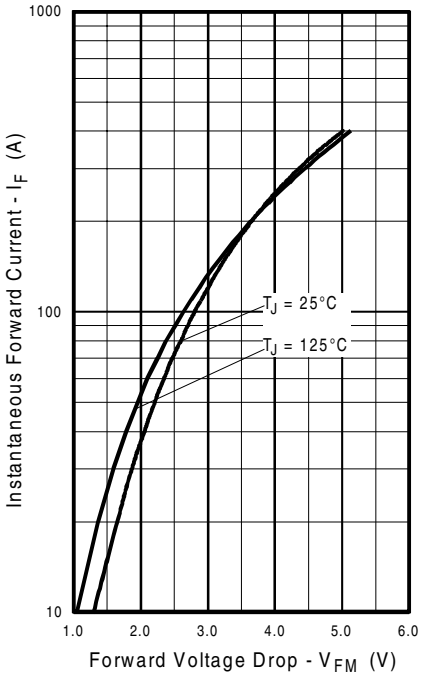


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

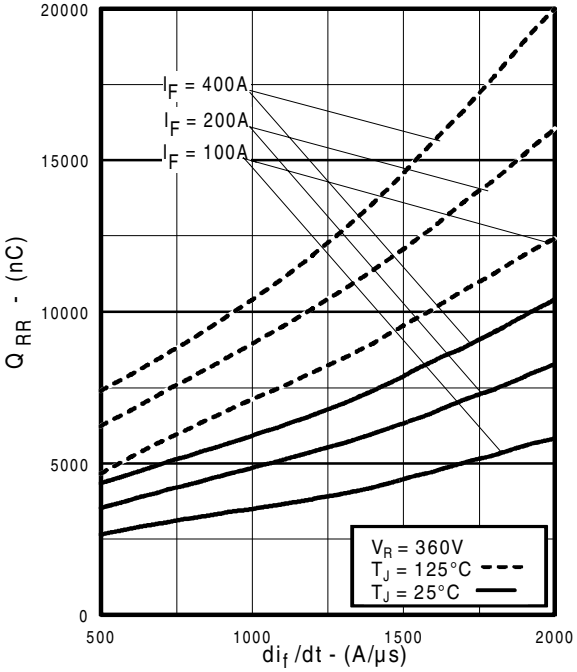


Fig. 14 - Typical Stored Charge vs. di_f/dt

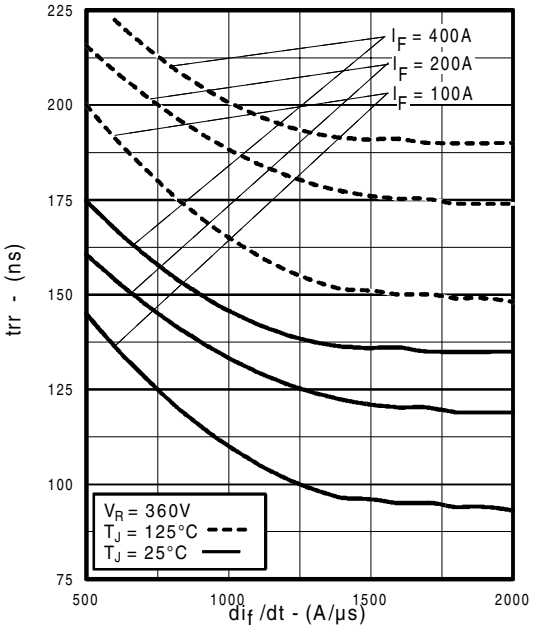


Fig. 15 - Typical Reverse Recovery vs. di_f/dt

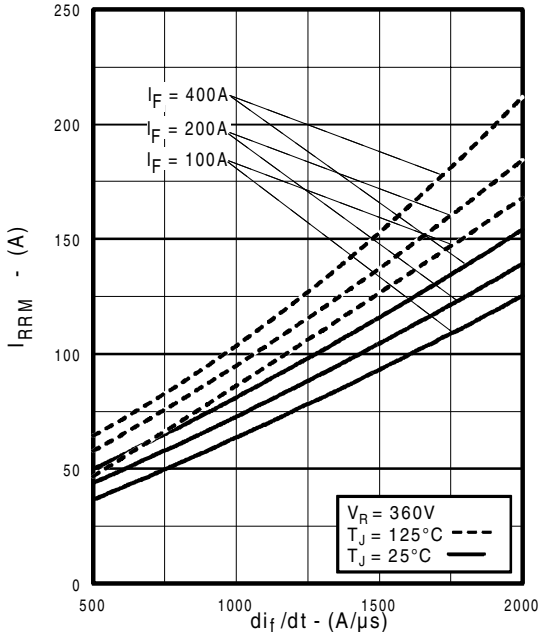


Fig. 16 - Typical Recovery Current vs. di_f/dt

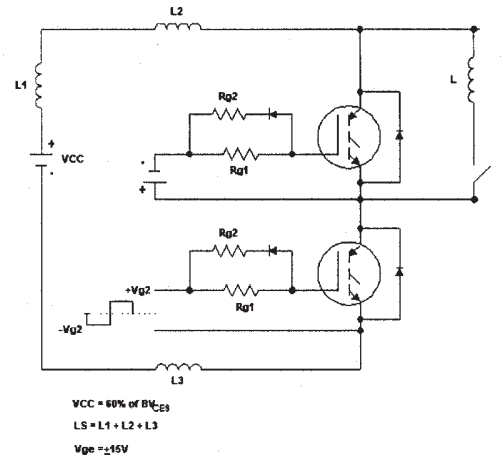


Fig. 17a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

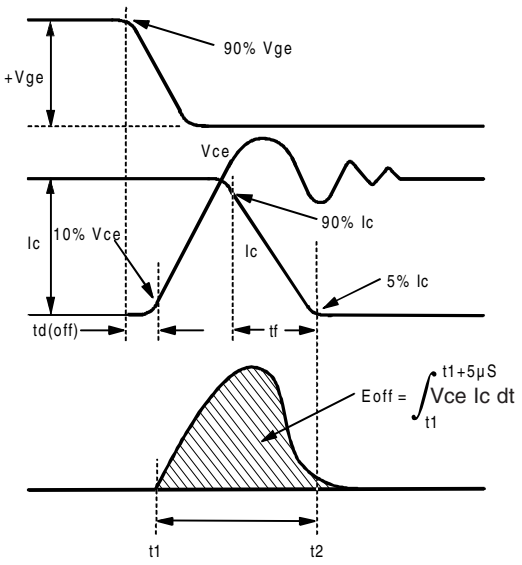


Fig. 17b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

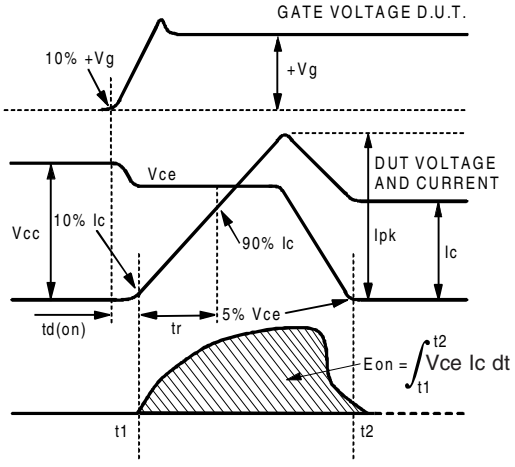


Fig. 17c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

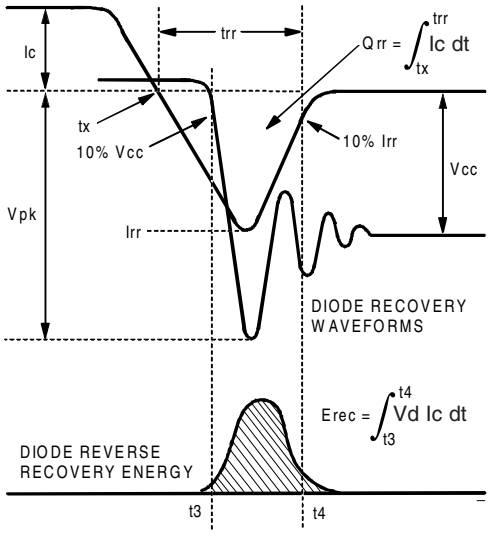


Fig. 17d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

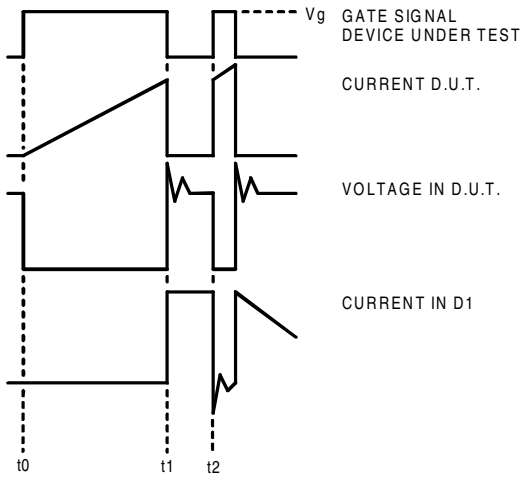


Figure 17e. Macro Waveforms for Figure 18a's Test Circuit

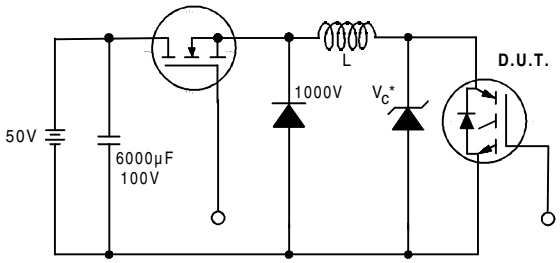


Figure 18. Clamped Inductive Load Test Circuit

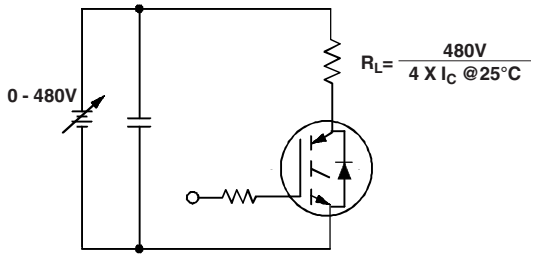


Figure 19. Pulsed Collector Current Test Circuit

Notes:

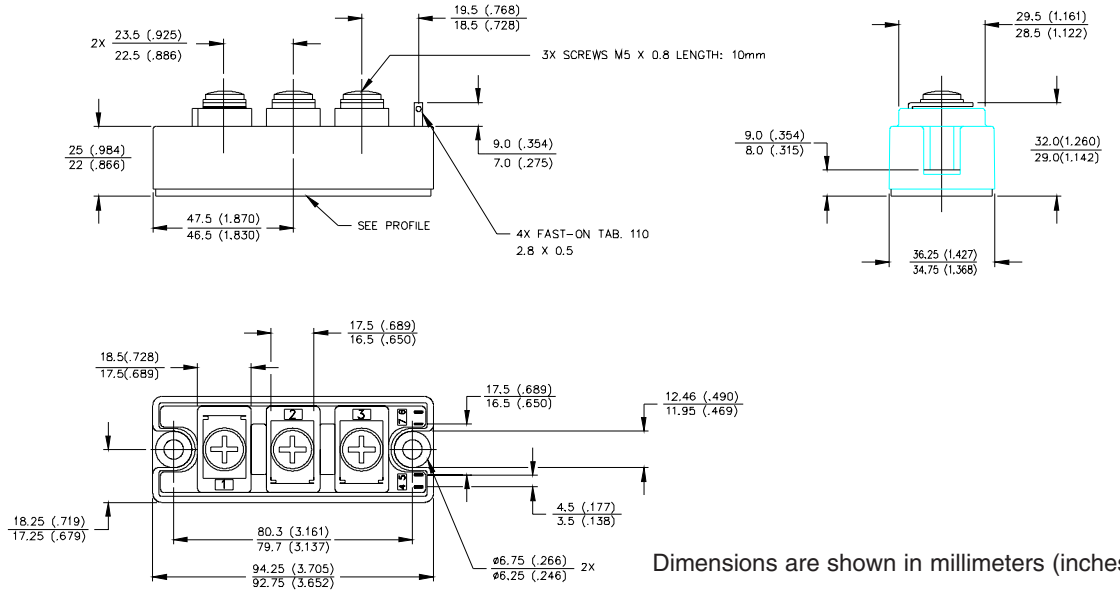
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 17

③ For screws M5x0.8

④ Pulse width 50µs; single shot.

Case Outline — INT-A-PAK



Dimensions are shown in millimeters (inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD- 50070A

International
IOR Rectifier

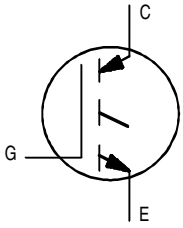
GA200SA60S

INSULATED GATE BIPOLAR TRANSISTOR

Standard Speed IGBT

Features

- Standard : Optimized for minimum saturation voltage and low operating frequencies up to 1kHz
- Lowest conduction losses available
- Fully isolated package (2,500 volt AC)
- Very low internal inductance (5 nH typ.)
- Industry standard outline



n-channel

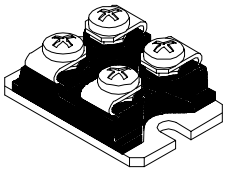
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.10V

@V_{GE} = 15V, I_C = 100A

Benefits

- Designed for increased operating efficiency in power conversion: UPS, SMPS, Welding, Induction heating
- Easy to assemble and parallel
- Direct mounting to heatsink
- Plug-in compatible with other SOT-227 packages



SOT-227

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	200	A
I_C @ T_C = 100°C	Continuous Collector Current	100	
I_{CM}	Pulsed Collector Current ①	400	
I_{LM}	Clamped Inductive Load Current ②	400	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	155	mJ
V_{ISOL}	RMS Isolation Voltage, Any Terminal to Case, t=1 min	2500	V
P_D @ T_C = 25°C	Maximum Power Dissipation	630	W
P_D @ T_C = 100°C	Maximum Power Dissipation	250	
T_J	Operating Junction	-55 to + 150	°C
T_{STG}	Storage Temperature Range	-55 to + 150	
	Mounting Torque, 6-32 or M3 Screw	12 lbf •in(1.3N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.20	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.05	——	
Wt	Weight of Module	30	——	gm

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.62	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.10	1.3	V	I_C = 100A V_{GE} = 15V
		—	1.33	—		I_C = 200A See Fig.2, 5
		—	1.02	—		I_C = 100A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 2 mA
g_{fe}	Forward Transconductance ⑤	90	150	—	S	V_{CE} = 100V, I_C = 100A
I_{CES}	Zero Gate Voltage Collector Current	—	—	1.0	mA	V_{GE} = 0V, V_{CE} = 600V
		—	—	10		V_{GE} = 0V, V_{CE} = 10V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±250	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	770	1200	nC	I_C = 100A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	100	150		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	260	380		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	78	—	ns	T_J = 25°C
t_r	Rise Time	—	56	—		I_C = 100A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	890	1300		V_{GE} = 15V, R_G = 2.0Ω
t_f	Fall Time	—	390	580		Energy losses include "tail"
E_{on}	Turn-On Switching Loss	—	0.98	—	mJ	See Fig. 9, 10, 13
E_{off}	Turn-Off Switching Loss	—	17.4	—		
E_{ts}	Total Switching Loss	—	18.4	25.5		
$t_{d(on)}$	Turn-On Delay Time	—	72	—	ns	T_J = 150°C,
t_r	Rise Time	—	60	—		I_C = 100A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	1500	—		V_{GE} = 15V, R_G = 2.0Ω
t_f	Fall Time	—	660	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	35.7	—	mJ	See Fig. 10,11, 13
L_E	Internal Emitter Inductance	—	5.0	—	nH	Between lead, and center of the die contact
C_{ies}	Input Capacitance	—	16250	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	1040	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	190	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 15)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 2.0Ω, (See fig. 14)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

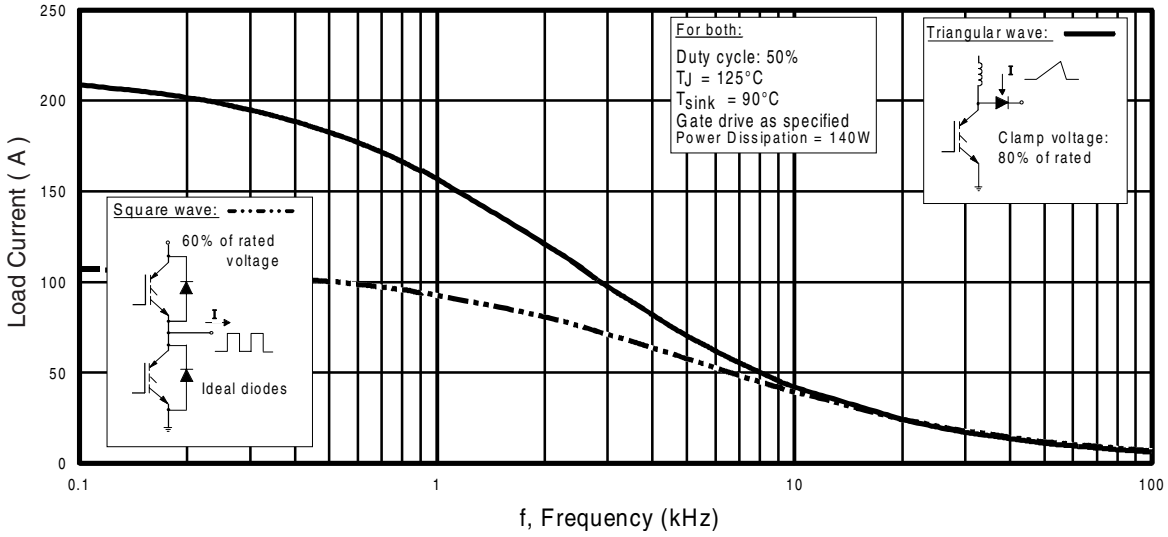


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

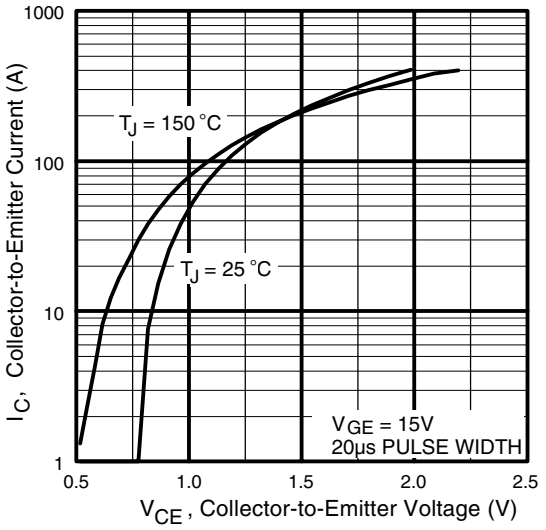


Fig. 2 - Typical Output Characteristics

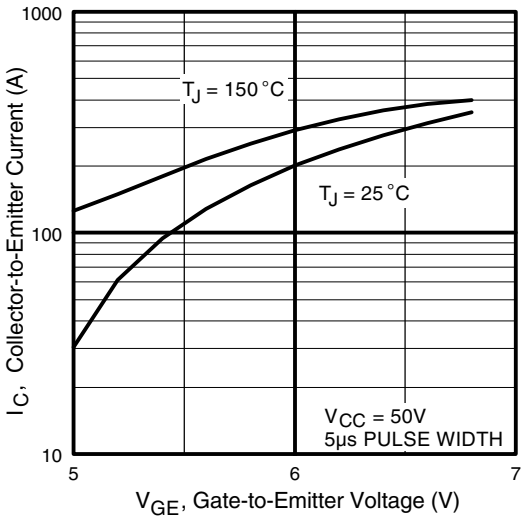


Fig. 3 - Typical Transfer Characteristics

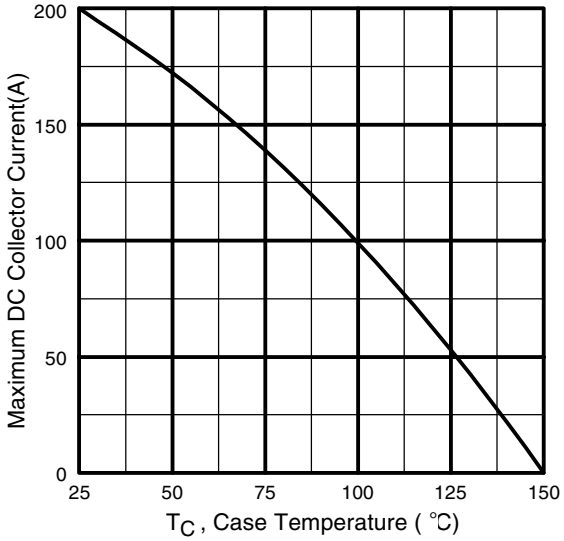


Fig. 4 - Maximum Collector Current vs. Case Temperature

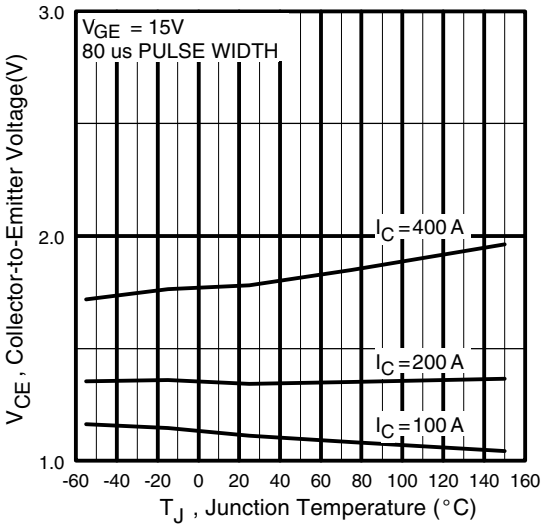


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

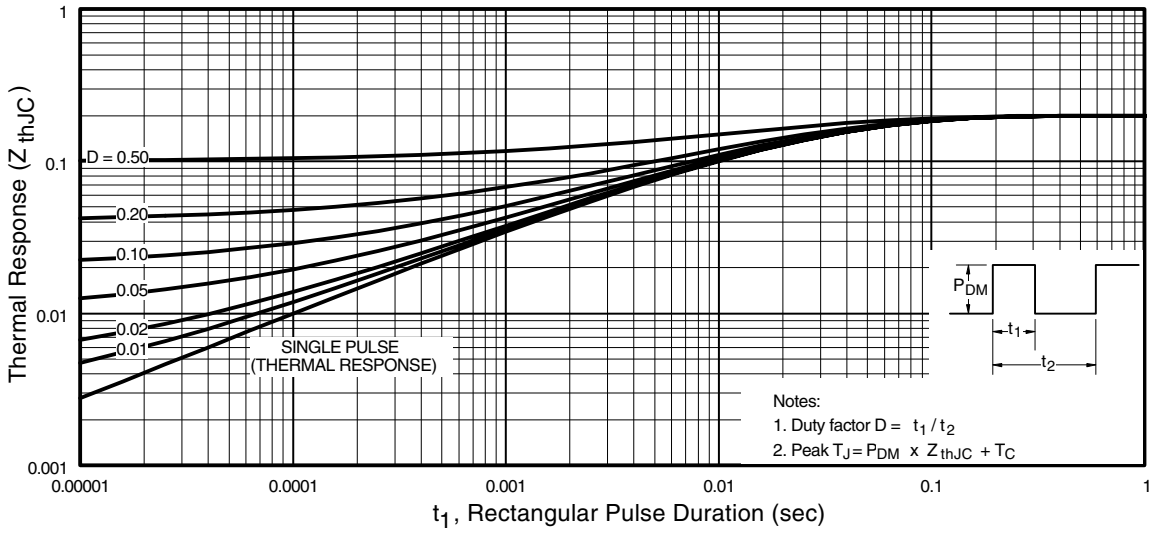


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

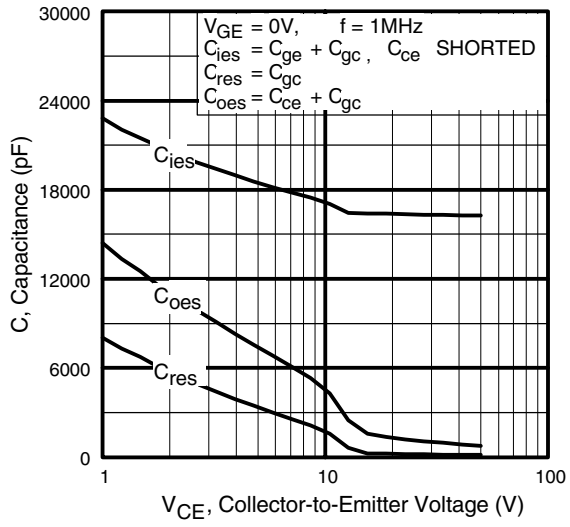


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

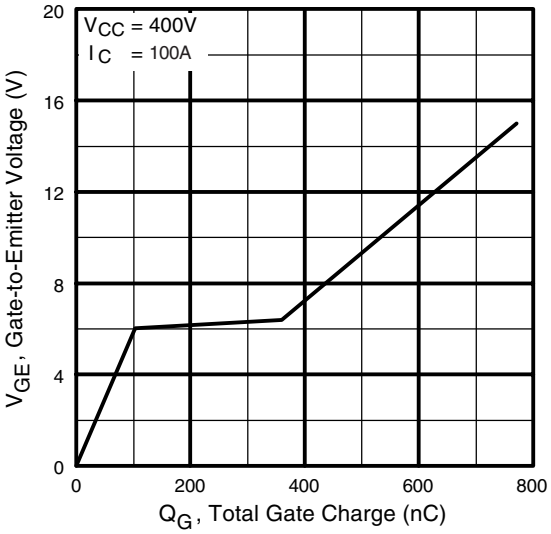


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

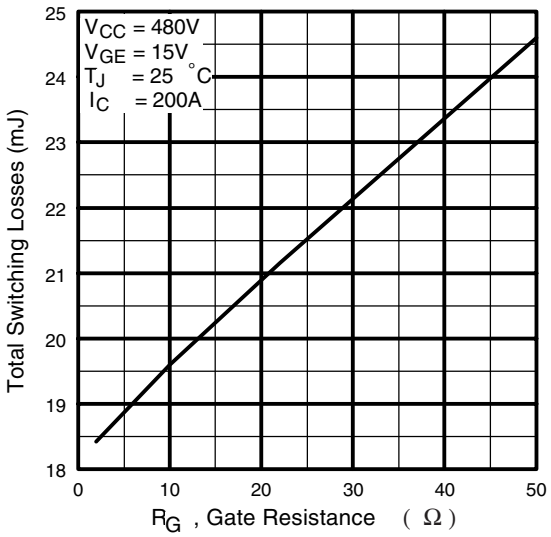


Fig. 9 - Typical Switching Losses vs. Gate Resistance

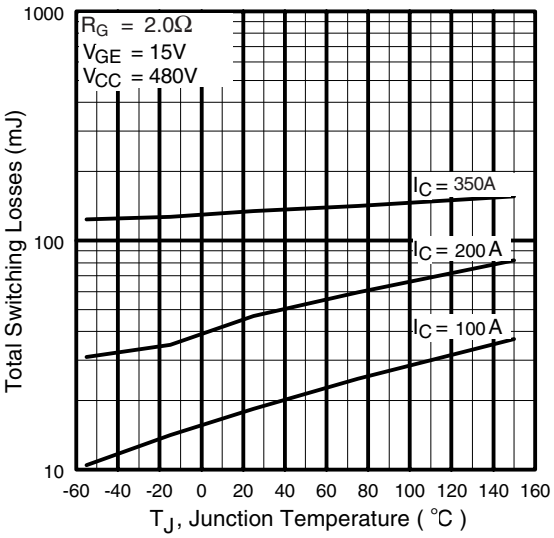


Fig. 10 - Typical Switching Losses vs. Junction Temperature

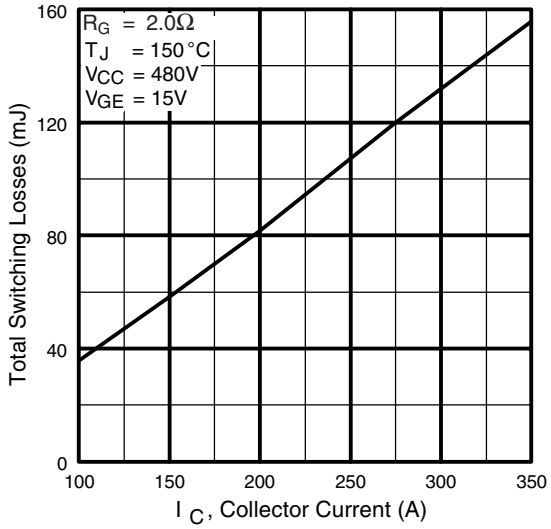


Fig. 11 - Typical Switching Losses vs. Collector Current

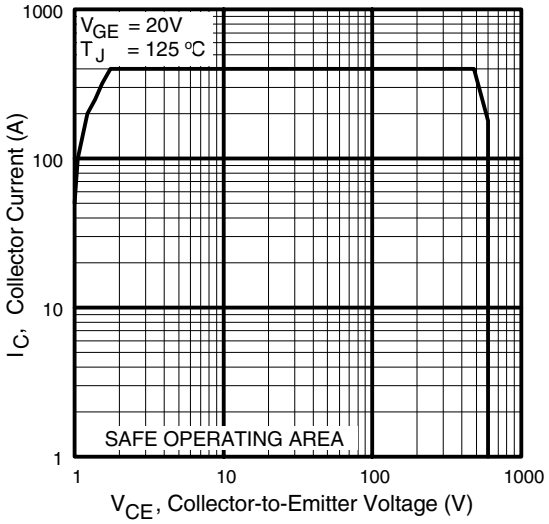


Fig. 12 - Turn-Off SOA

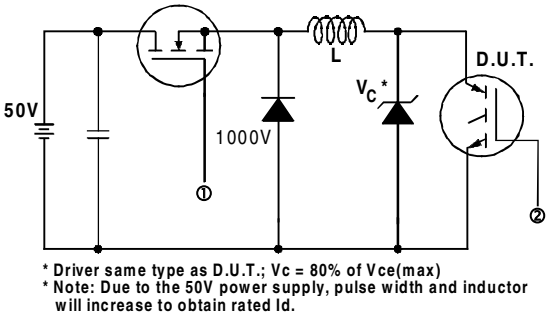


Fig. 13a - Clamped Inductive Load Test Circuit

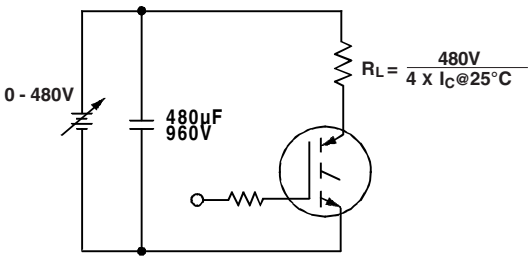


Fig. 13b - Pulsed Collector Current Test Circuit

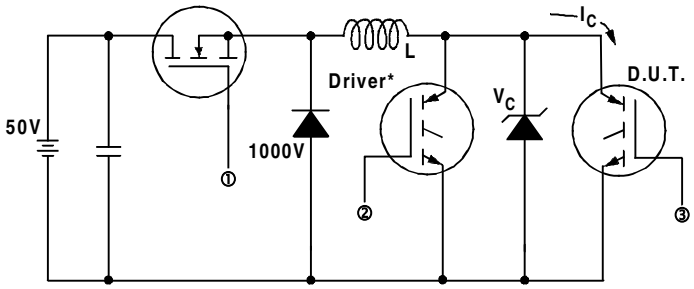


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

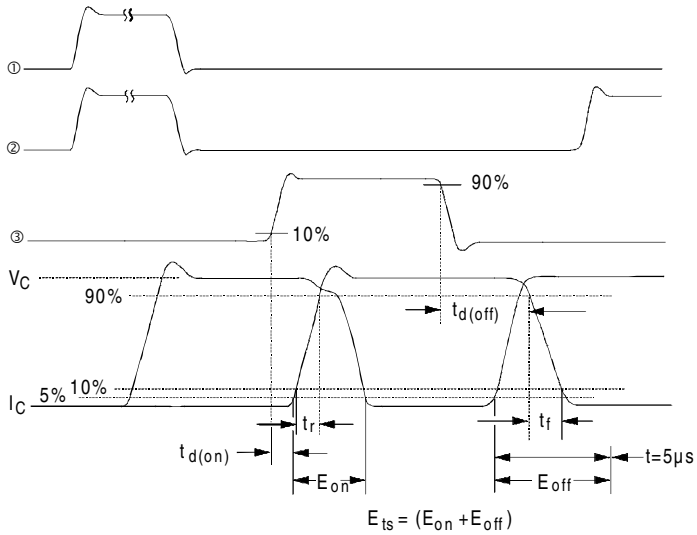
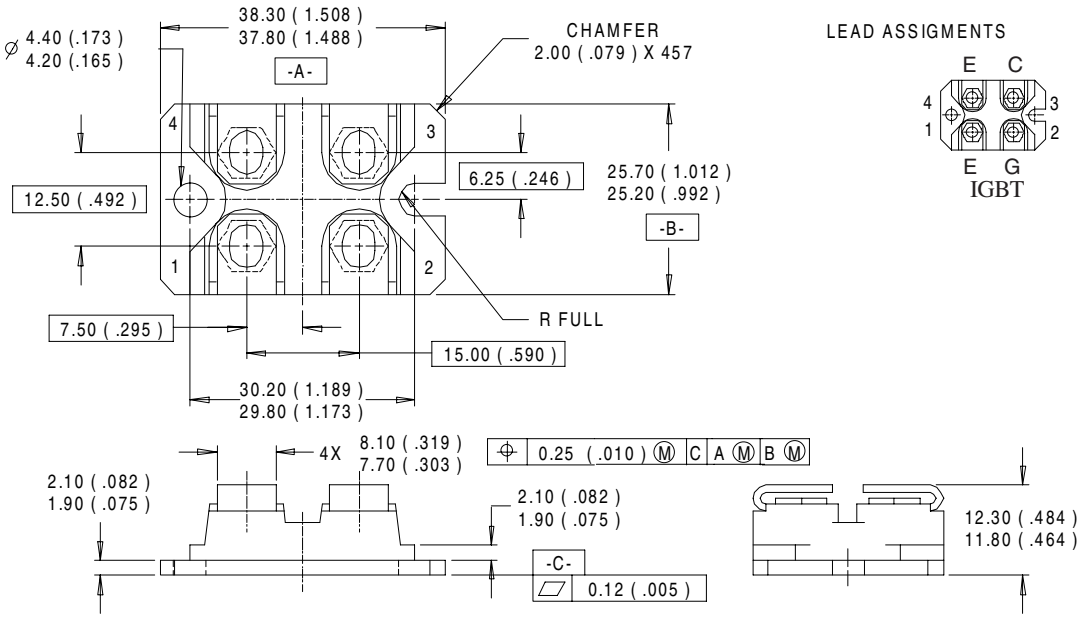


Fig. 14b - Switching Loss Waveforms

GA200SA60S

SOT-227 Package Details

Dimensions are shown in millimeters (inches)

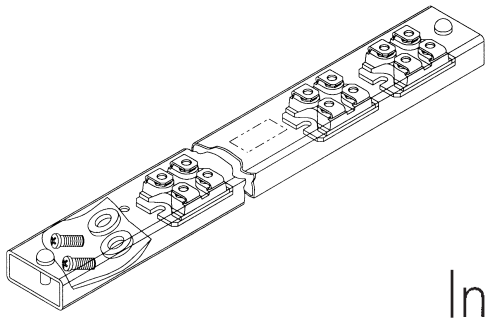


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QUANTITIES PER TUBE IS 10
M4 SREW AND WASHER INCLUDED



International
IOR Rectifier

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IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
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IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

Data and specifications subject to change without notice. 4/00

PD -50066A

International
IOR Rectifier

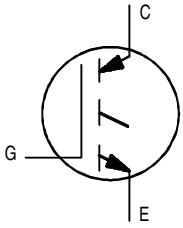
GA200SA60U

INSULATED GATE BIPOLAR TRANSISTOR

Ultra-Fast™ Speed IGBT

Features

- UltraFast: Optimized for minimum saturation voltage and operating frequencies up to 40 kHz in hard switching, > 200 kHz in resonant mode
- Very low conduction and switching losses
- Fully isolate package (2,500 Volt AC/RMS)
- Very low internal inductance (≤ 5 nH typ.)
- Industry standard outline



n-channel

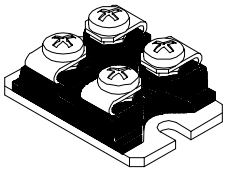
$V_{CES} = 600V$

$V_{CE(on)\ typ.} = 1.60V$

$@V_{GE} = 15V, I_C = 100A$

Benefits

- Designed for increased operating efficiency in power conversion: UPS, SMPS, Welding, Induction heating
- Lower overall losses available at frequencies ≥ 20kHz
- Easy to assemble and parallel
- Direct mounting to heatsink
- Lower EMI, requires less snubbing
- Plug-in compatible with other SOT-227 packages



SOT-227

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	200	A
I_C @ T_C = 100°C	Continuous Collector Current	100	
I_{CM}	Pulsed Collector Current	400	
I_{LM}	Clamped Inductive Load Current②	400	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	160	mJ
V_{ISOL}	RMS Isolation Voltage, Any Terminal to Case, t=1 min	2500	V
P_D @ T_C = 25°C	Maximum Power Dissipation	500	W
P_D @ T_C = 100°C	Maximum Power Dissipation	200	
T_J	Operating Junction	-55 to + 150	°C
T_{STG}	Storage Temperature Range	-55 to + 150	
	Mounting Torque, 6-32 or M3 Screw	12 lbf •in(1.3N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.25	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.05	—	
Wt	Weight of Module	30	—	gm

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$DV_{(BR)CES}/DT_J$	Temperature Coeff. of Breakdown Voltage	—	0.38	—	V/°C	V_{GE} = 0V, I_C = 10 mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.60	1.9	V	I_C = 100A; V_{GE} = 15V
		—	1.92	—		I_C = 200A; See Fig.2, 5
		—	1.54	—		I_C = 100A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 2.0 mA
g_{fe}	Forward Transconductance ⑤	79		—	S	V_{CE} = 100V, I_C = 100A
I_{CES}	Zero Gate Voltage Collector Current	—	—	1.0	mA	V_{GE} = 0V, V_{CE} = 600V
		—	—	10		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±250	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	770	1200	nC	I_C = 100A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	100	150		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	260	380		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	54	—	ns	T_J = 25°C
t_r	Rise Time	—	79	—		I_C = 100A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	130	200		V_{GE} = 15V, R_G = 2.0Ω
t_f	Fall Time	—	300	450		Energy losses include "tail"
E_{on}	Turn-On Switching Loss	—	0.98	—	mJ	See Fig. 9, 10, 14
E_{off}	Turn-Off Switching Loss	—	3.48	—		
E_{ts}	Total Switching Loss	—	4.46	7.6		
$t_{d(on)}$	Turn-On Delay Time	—	56	—	ns	T_J = 150°C,
t_r	Rise Time	—	75	—		I_C = 100A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	160	—		V_{GE} = 15V, R_G = 2.0Ω
t_f	Fall Time	—	460	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	7.24	—	mJ	See Fig. 10, 11, 14
L_E	Internal Emitter Inductance	—	5.0	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	16500	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	1000	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	200	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 2.0Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

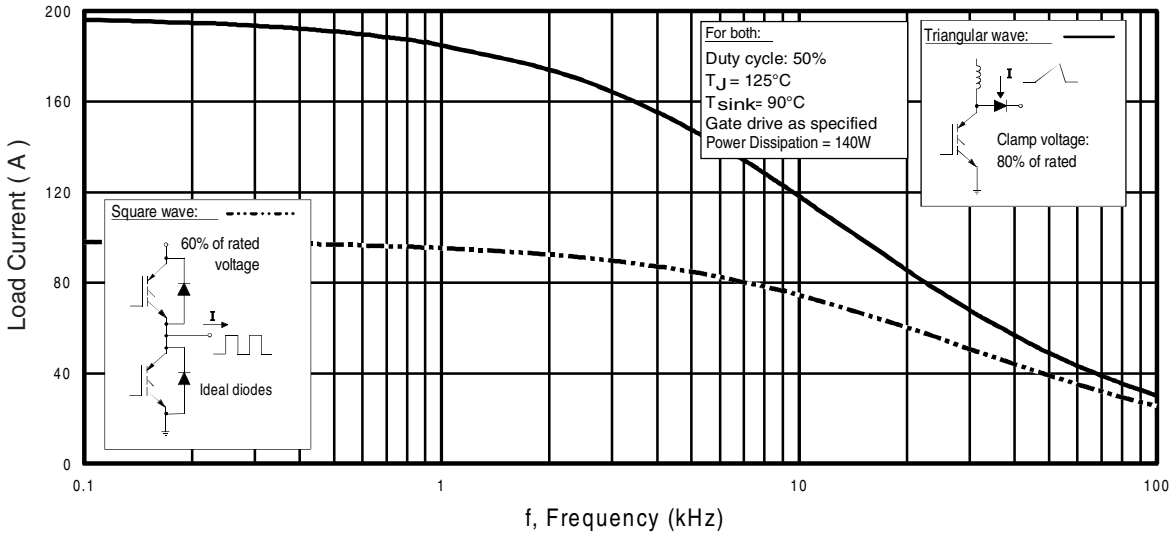


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

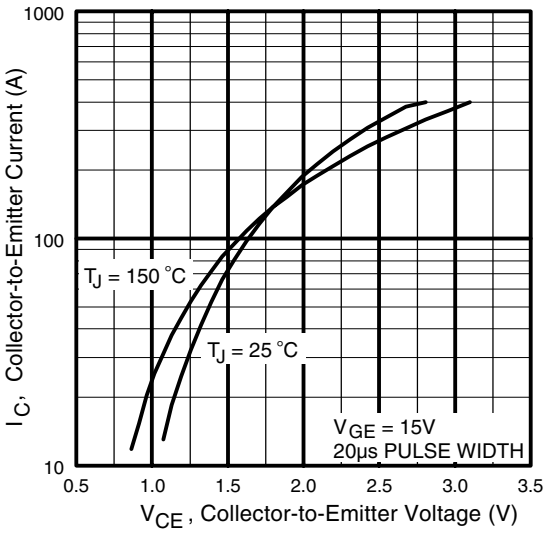


Fig. 2 - Typical Output Characteristics

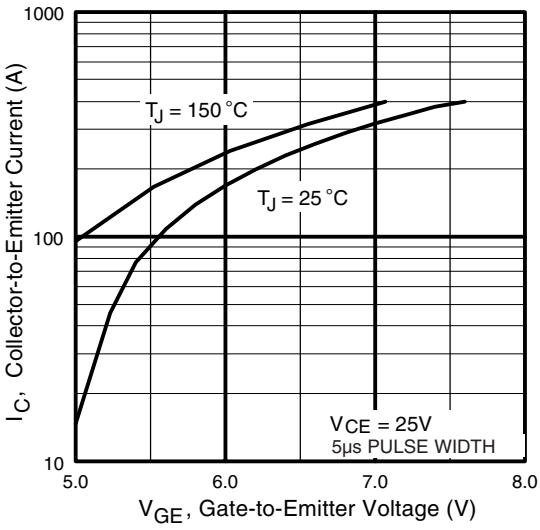


Fig. 3 - Typical Transfer Characteristics

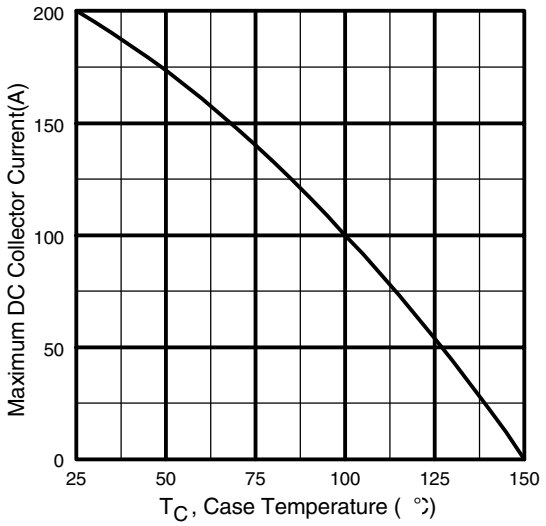


Fig. 4 - Maximum Collector Current vs. Case Temperature

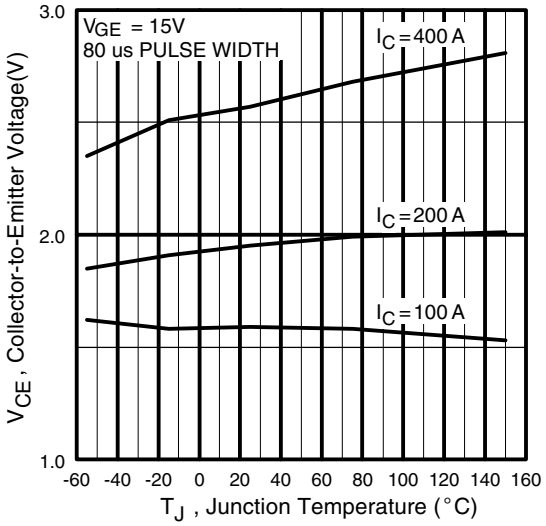


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

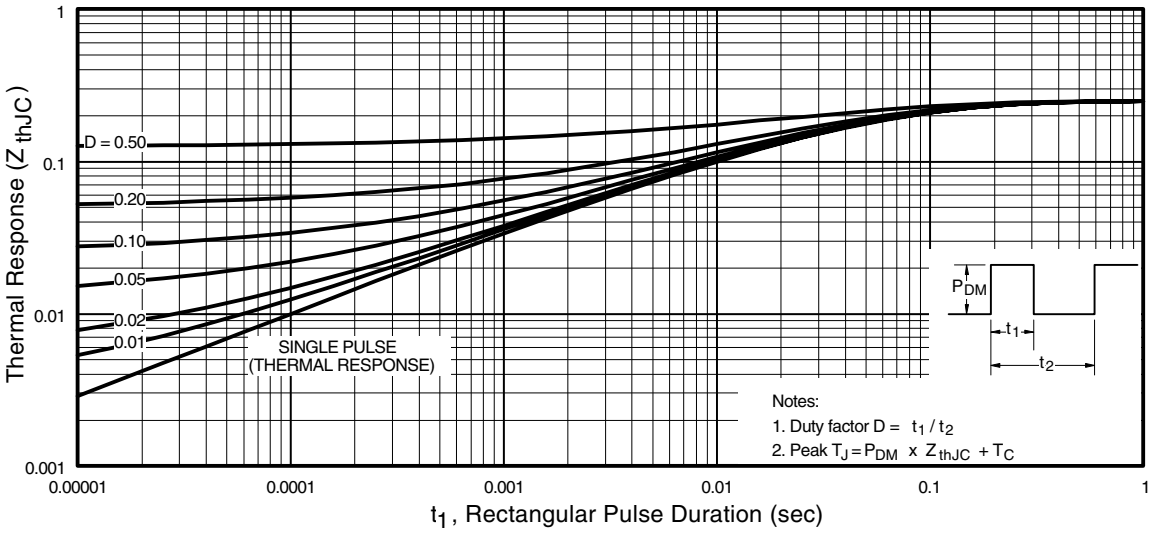


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

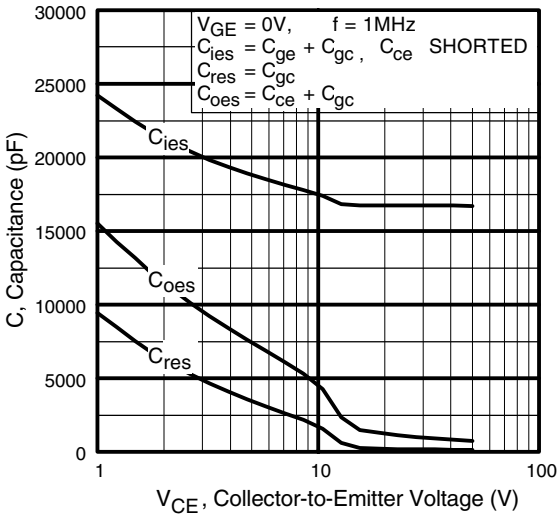


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

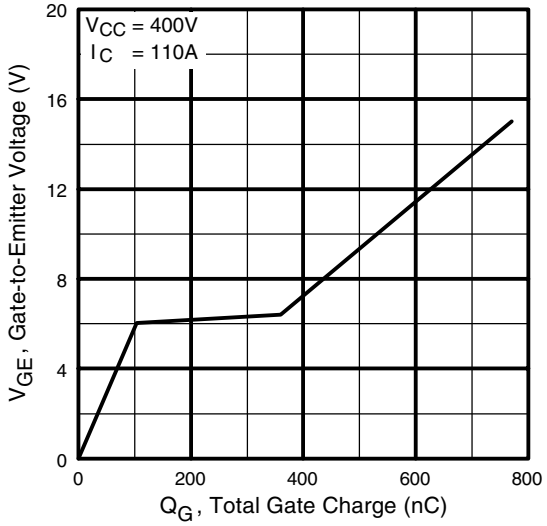


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

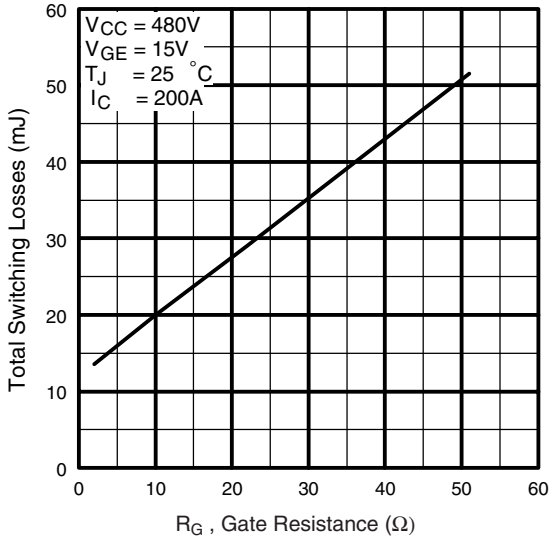


Fig. 9 - Typical Switching Losses vs. Gate Resistance

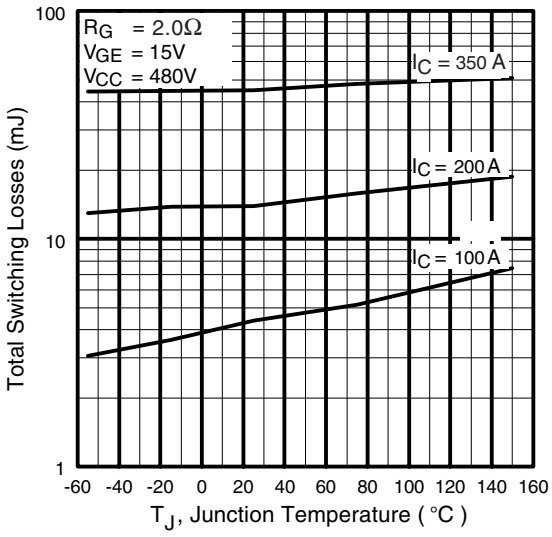


Fig. 10 - Typical Switching Losses vs. Junction Temperature

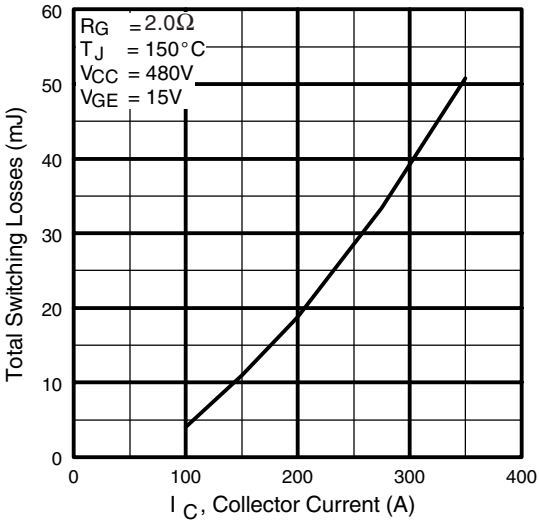


Fig. 11 - Typical Switching Losses vs. Collector Current

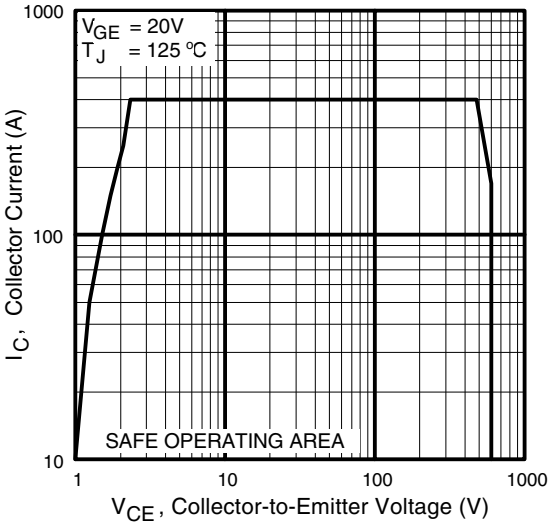


Fig. 12 - Turn-Off SOA

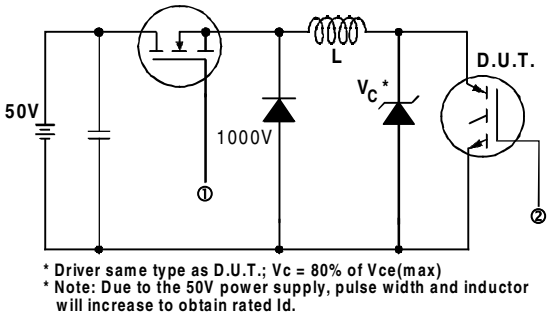


Fig. 13a - Clamped Inductive Load Test Circuit

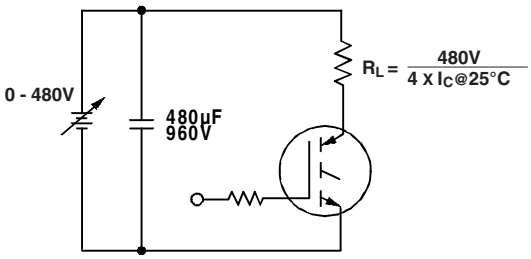


Fig. 13b - Pulsed Collector Current Test Circuit

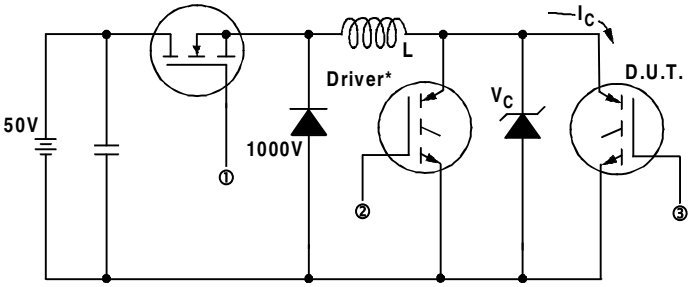


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

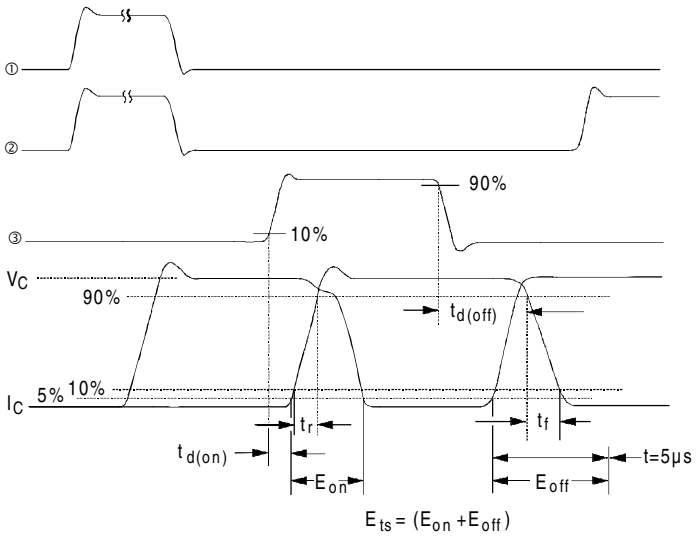
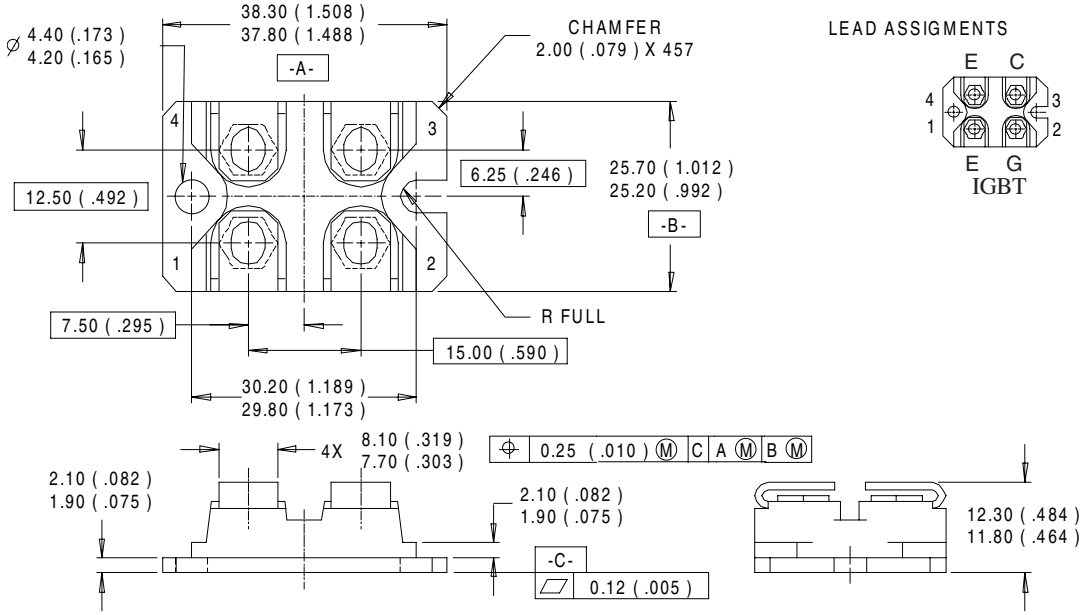


Fig. 14b - Switching Loss Waveforms

GA200SA60U

SOT-227 Package Details

Dimensions are shown in millimeters (inches)

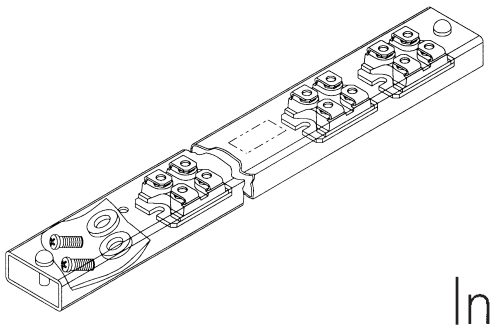


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IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

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International
IOR Rectifier

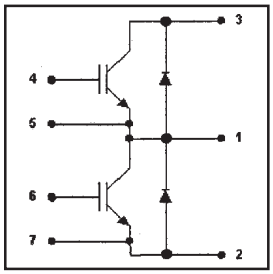
GA250TS60U

"HALF-BRIDGE" IGBT INT-A-PAK

Ultra-Fast™ Speed IGBT

Features

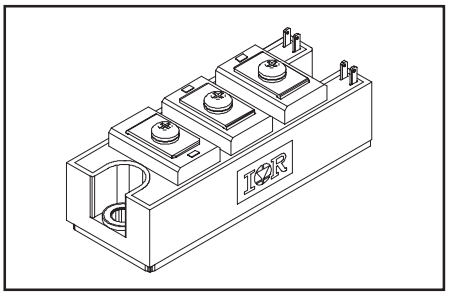
- Generation 4 IGBT technology
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL approved



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.9V

@V_{GE} = 15V, I_C = 250A



Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	250	A
I_{CM}	Pulsed Collector Current①	500	
I_{LM}	Peak Switching Current②	500	
I_{FM}	Peak Diode Forward Current	500	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	780	W
P_D @ T_C = 85°C	Maximum Power Dissipation	400	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.16	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.35	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3③	—	3.0	
	Weight of Module	200	—	g

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	1.9	2.3		V_{GE} = 15V, I_C = 250A
		—	2.0	—		V_{GE} = 15V, I_C = 250A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		I_C = 1.5mA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.5mA
g_{fe}	Forward Transconductance ④	—	204	—	S	V_{CE} = 25V, I_C = 250A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	1.0	mA	V_{GE} = 0V, V_{CE} = 600V
		—	—	10		V_{GE} = 0V, V_{CE} = 600V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	4.0	—	V	I_F = 250A, V_{GE} = 0V
		—	4.1	—		I_F = 250A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	250	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	1050	1600	nC	V_{CC} = 400V
Qge	Gate - Emitter Charge (turn-on)	—	146	220		I_C = 250A
Q_{gc}	Gate - Collector Charge (turn-on)	—	525	790		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	173	—	ns	R_{G1} = 15Ω, R_{G2} = 0Ω,
t_r	Rise Time	—	242	—		I_C = 250A
$t_{d(off)}$	Turn-Off Delay Time	—	1020	—		V_{CC} = 360V
t_f	Fall Time	—	190	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	10.5	—	mJ	
$E_{off\,(1)}$	Turn-Off Switching Energy	—	20.0	—		
$E_{ts\,(1)}$	Total Switching Energy	—	30.5	45		
C_{ies}	Input Capacitance	—	23400	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	1460	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	300	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	183	—	ns	I_C = 250A
I_{rr}	Diode Peak ReverseCurrent	—	124	—	A	R_{G1} = 15Ω
Q_{rr}	Diode Recovery Charge	—	11275	—	µC	R_{G2} = 0Ω
$di_{(rec)}M_{/dt}$	Diode Peak Rate of Fall of Recovery During t_b	—	1700	—	A/µs	V_{CC} = 360V di/dt=1300A/µs

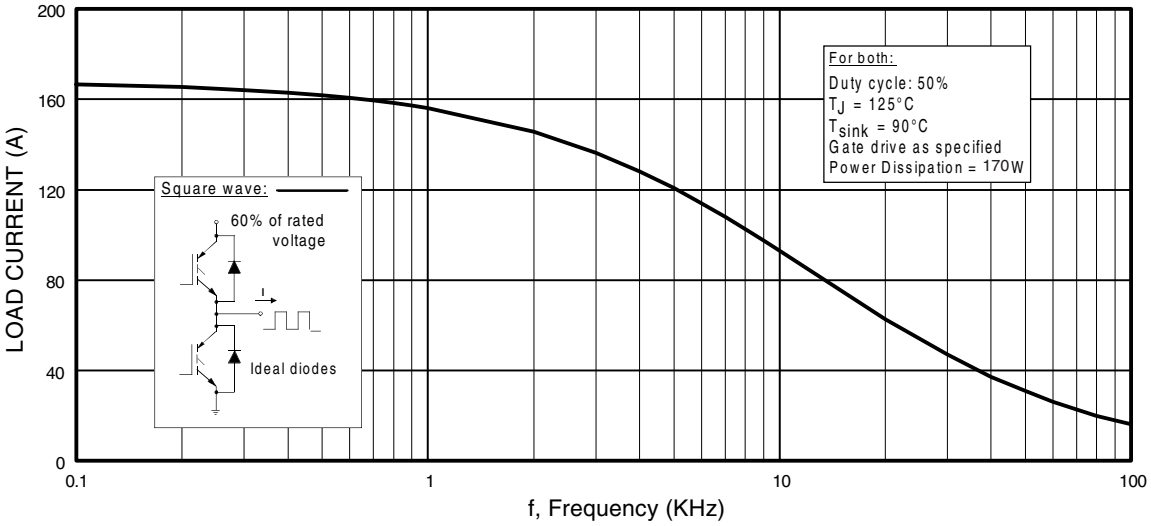


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

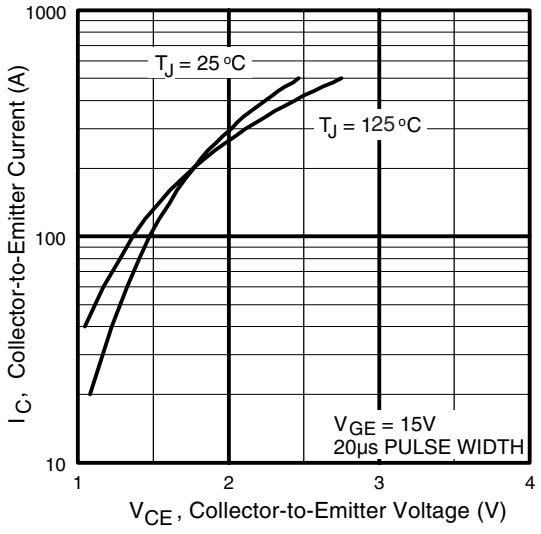


Fig. 2 - Typical Output Characteristics

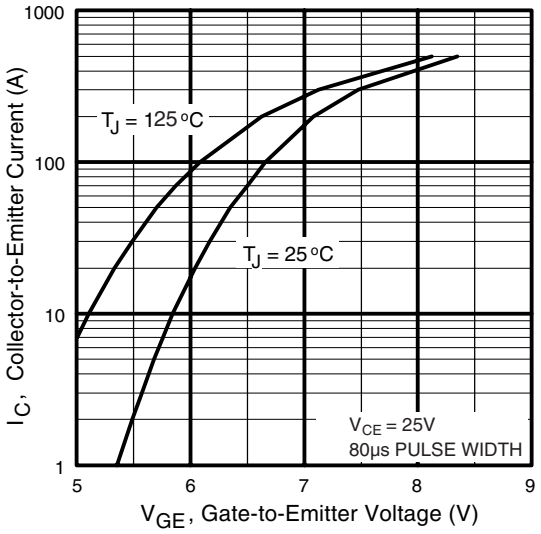


Fig. 3 - Typical Transfer Characteristics

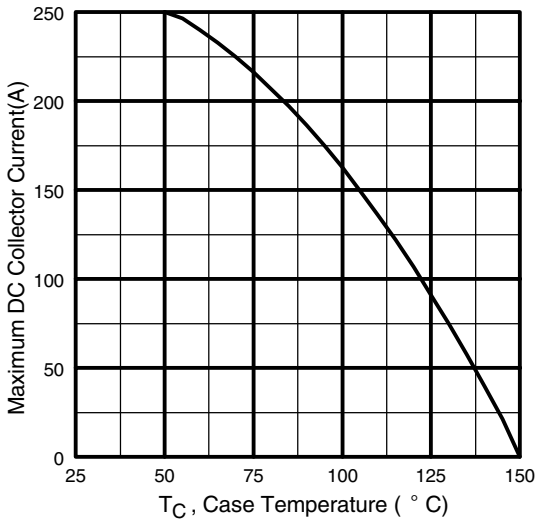


Fig. 4 - Maximum Collector Current vs. Case Temperature

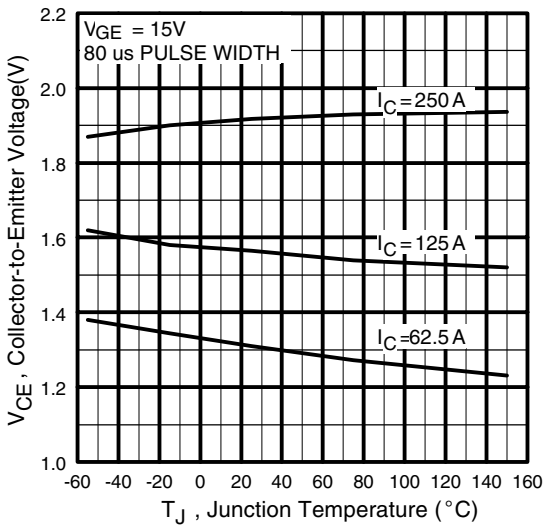


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

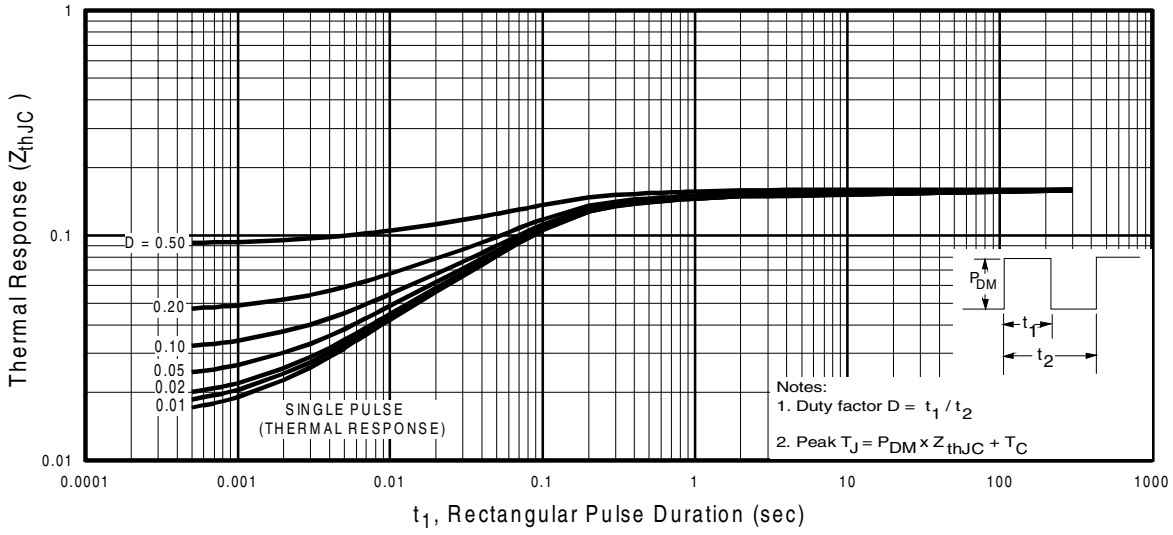


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

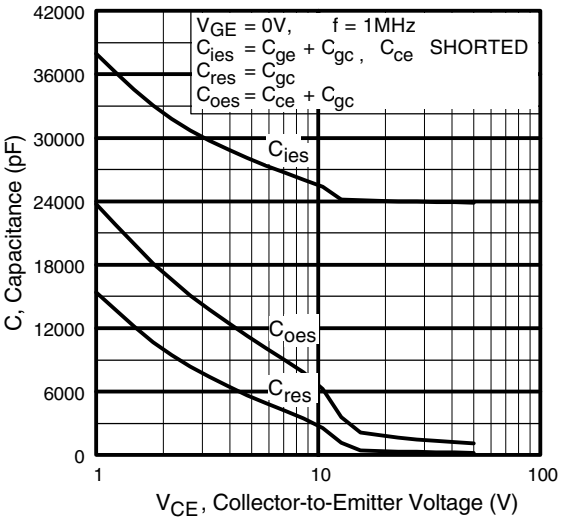


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

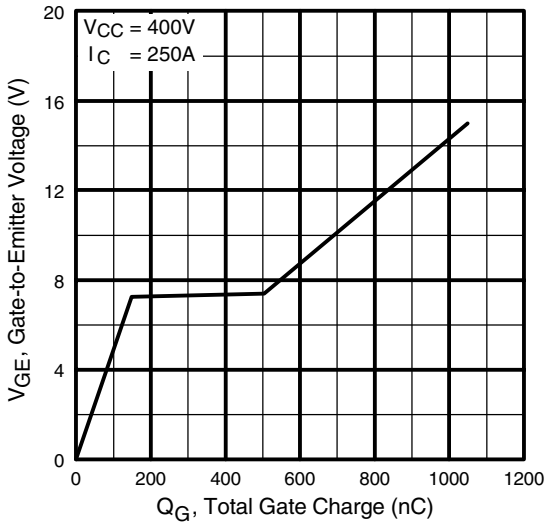


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

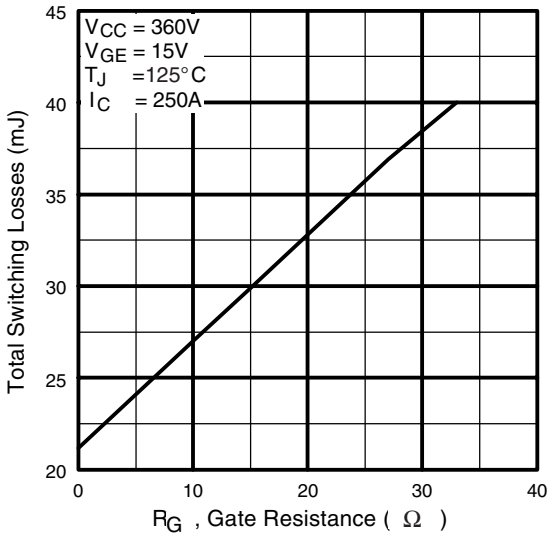


Fig. 9 - Typical Switching Losses vs. Gate Resistance

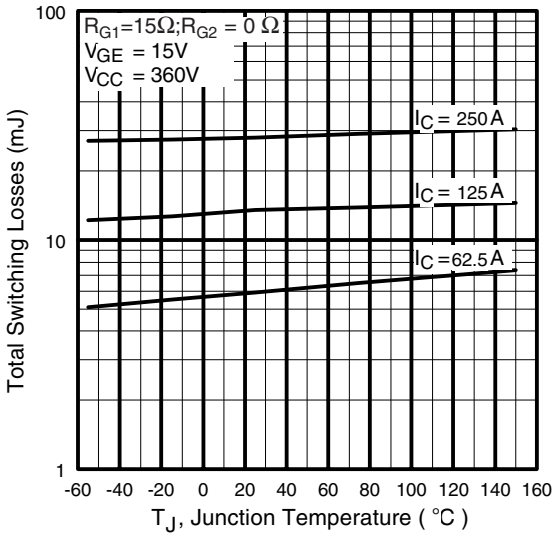


Fig. 10 - Typical Switching Losses vs. Junction Temperature

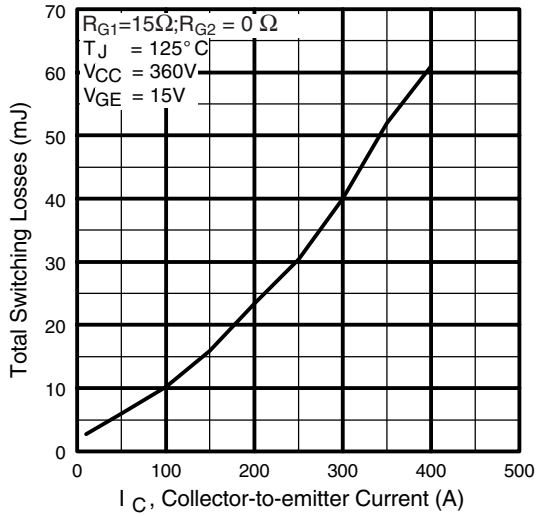


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

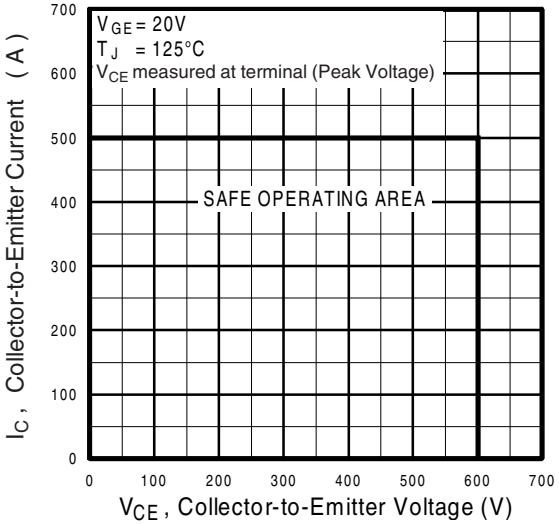


Fig. 12 - Reverse Bias SOA

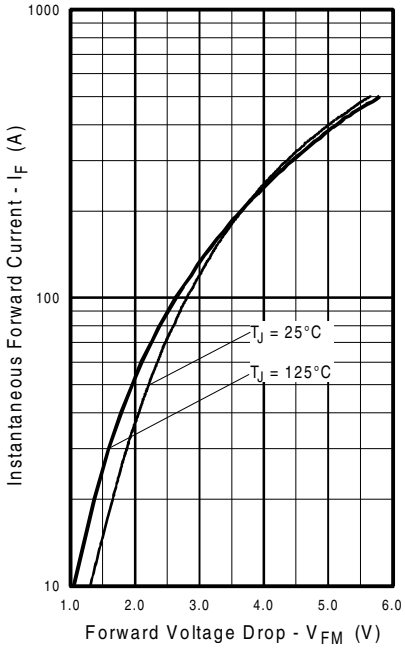


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

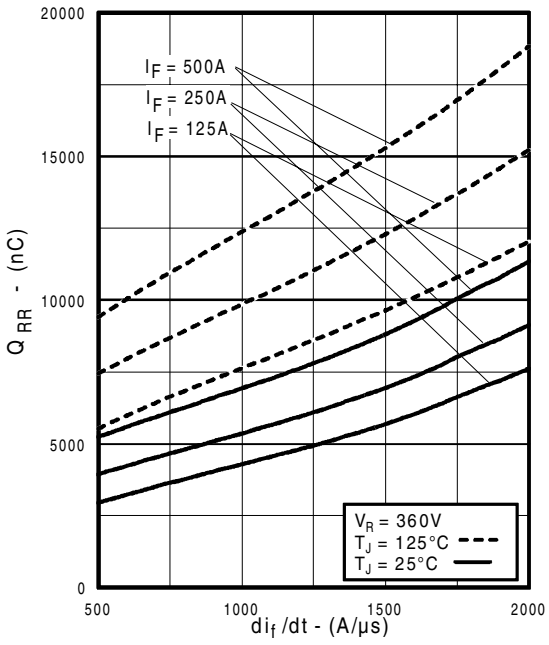


Fig. 14 - Typical Stored Charge vs. di_f/dt

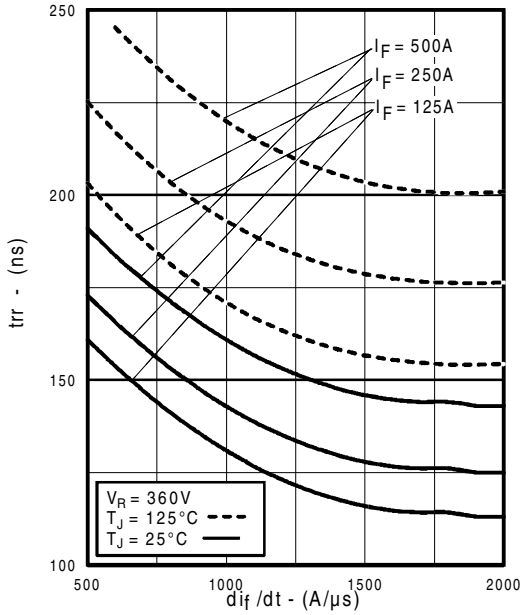


Fig. 15 - Typical Reverse Recovery vs. di_f/dt

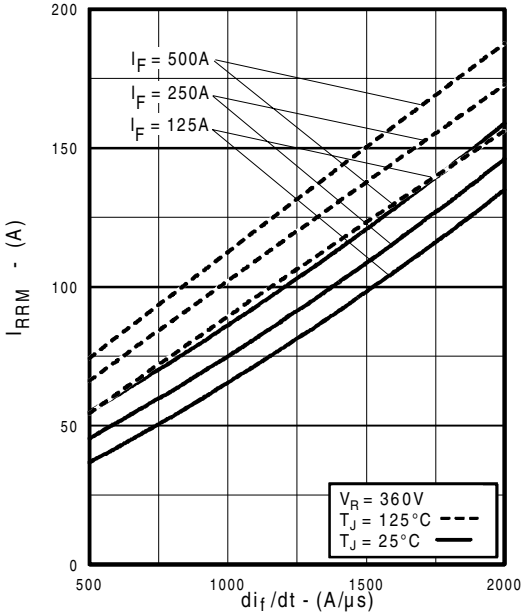


Fig. 16 - Typical Recovery Current vs. di_f/dt

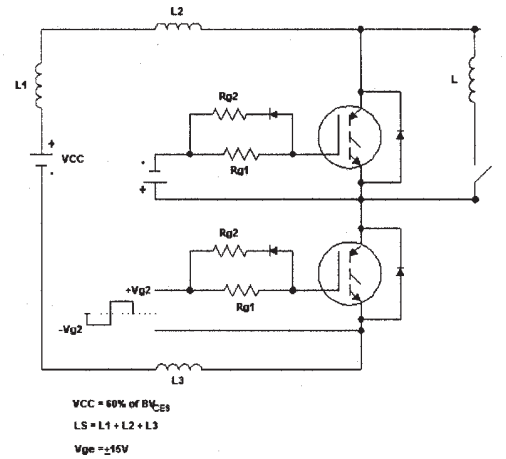


Fig. 17a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

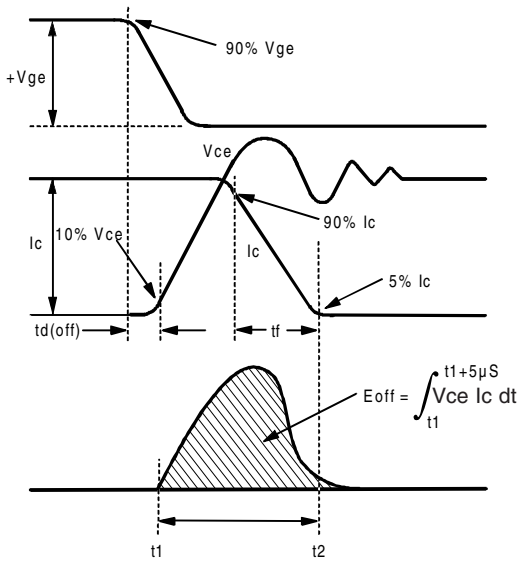


Fig. 17b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

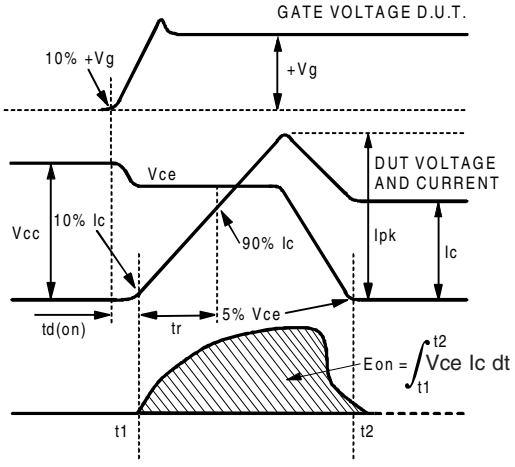


Fig. 17c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

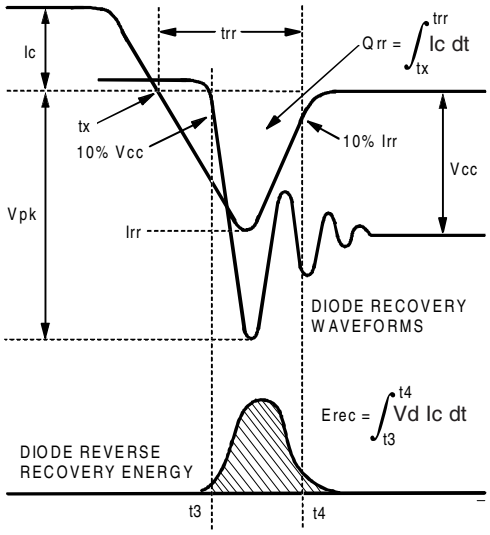


Fig. 17d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

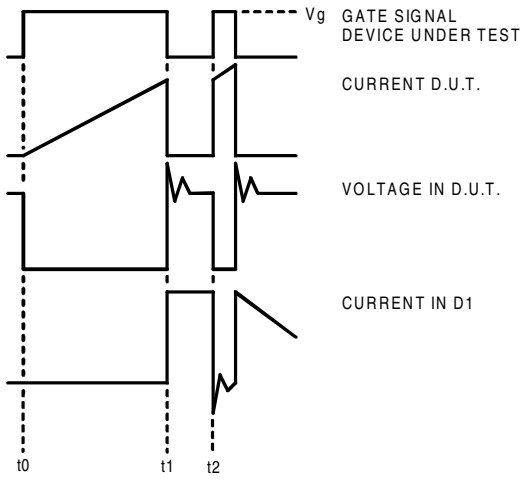


Figure 17e. Macro Waveforms for Figure 18a's Test Circuit

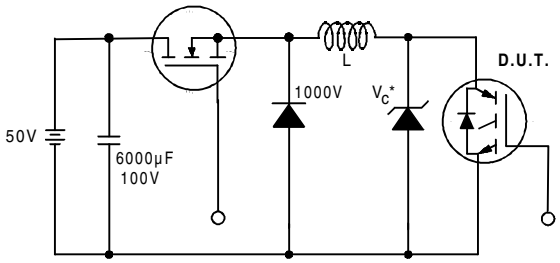


Figure 18. Clamped Inductive Load Test Circuit

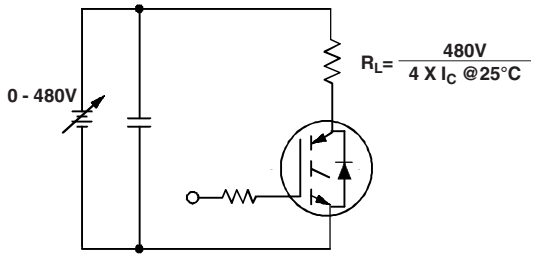


Figure 19. Pulsed Collector Current Test Circuit

Notes:

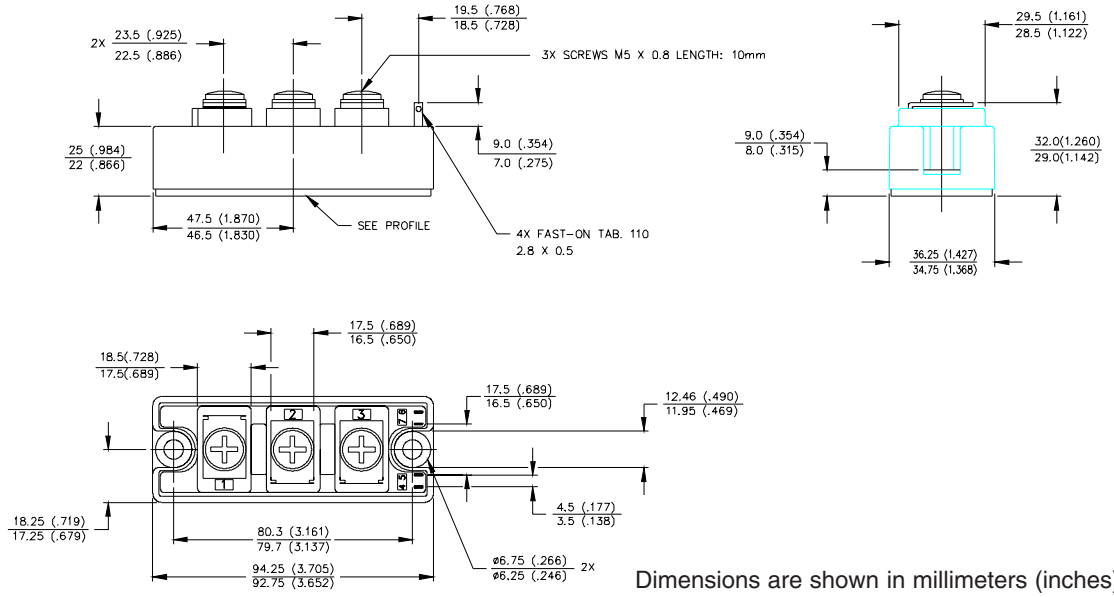
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 17

③ For screws M5x0.8

④ Pulse width 50µs; single shot.

Case Outline — INT-A-PAK



Dimensions are shown in millimeters (inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
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International
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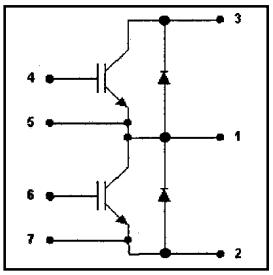
GA300TD60U

"HALF-BRIDGE" IGBT DOUBLE INT-A-PAK

Ultra-Fast™ Speed IGBT

Features

- Generation 4 IGBT technology
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL approved



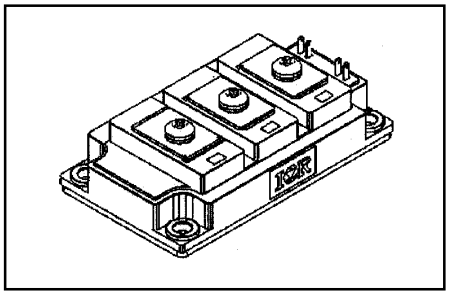
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.80V

@V_{GE} = 15V, I_C = 300A

Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	300	A
I_{CM}	Pulsed Collector Current•	600	
I_{LM}	Peak Switching Current,	600	
I_{FM}	Peak Diode Forward Current	600	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	880	W
P_D @ T_C = 85°C	Maximum Power Dissipation	460	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.14	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.20	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3③	—	3.0	
	Weight of Module	400	—	g

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	1.8	2.3		V_{GE} = 15V, I_C = 300A
		—	1.9	—		V_{GE} = 15V, I_C = 300A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		I_C = 1.75mA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.75mA
g_{fe}	Forward Transconductance „	—	269	—	S	V_{CE} = 25V, I_C = 300A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	1.0	mA	V_{GE} = 0V, V_{CE} = 600V
		—	—	10		V_{GE} = 0V, V_{CE} = 600V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	3.3	—	V	I_F = 300A, V_{GE} = 0V
		—	3.2	—		I_F = 300A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	400	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	1249	1873	nC	V_{CC} = 400V
Q_{ge}	Gate - Emitter Charge (turn-on)	—	173	260		I_C = 187A
Q_{gc}	Gate - Collector Charge (turn-on)	—	423	635		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	645	—	ns	R_{G1} = 27Ω, R_{G2} = 0Ω,
t_r	Rise Time	—	282	—		I_C = 300A
$t_{d(off)}$	Turn-Off Delay Time	—	418	—		V_{CC} = 360V
t_f	Fall Time	—	220	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	22	—	mJ	See Fig.17 through Fig.19
E_{off}	Turn-Off Switching Energy	—	25	—		
E_{ts}	Total Switching Energy	—	47	60		
C_{ies}	Input Capacitance	—	27755	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	1735	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	361	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	200	—	ns	I_C = 300A
I_{rr}	Diode Peak ReverseCurrent	—	128	—	A	R_{G1} = 27Ω
Q_{rr}	Diode Recovery Charge	—	12771	—	nC	R_{G2} = 0Ω
$di_{(rec)}M_{/dt}$	Diode Peak Rate of Fall of Recovery During t_b	—	1691	—	A/µs	V_{CC} = 360V di/dt =1300A/µs

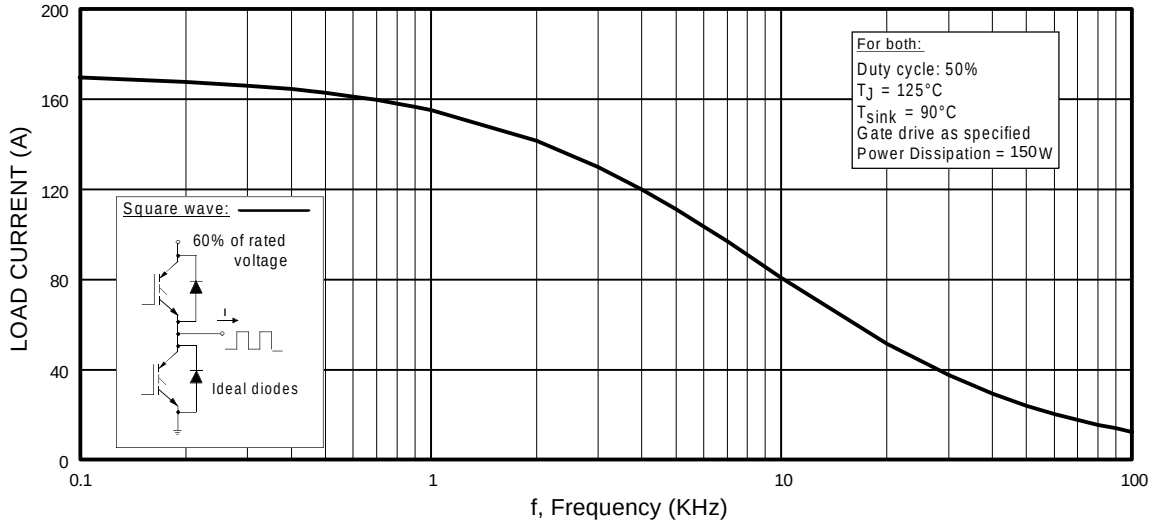


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

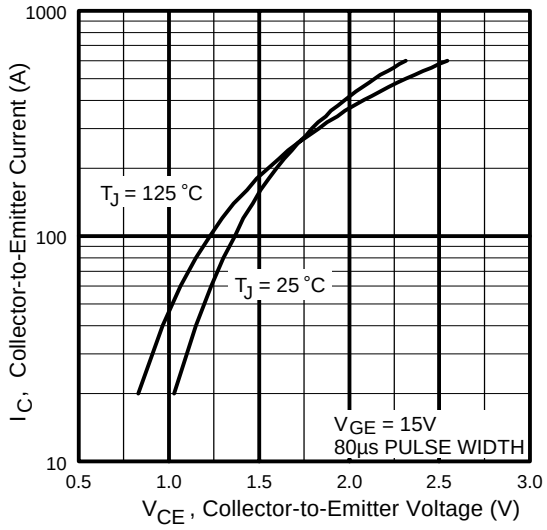


Fig. 2 - Typical Output Characteristics

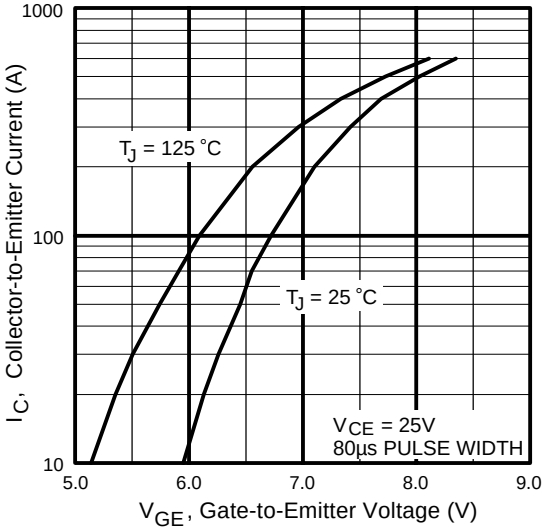


Fig. 3 - Typical Transfer Characteristics

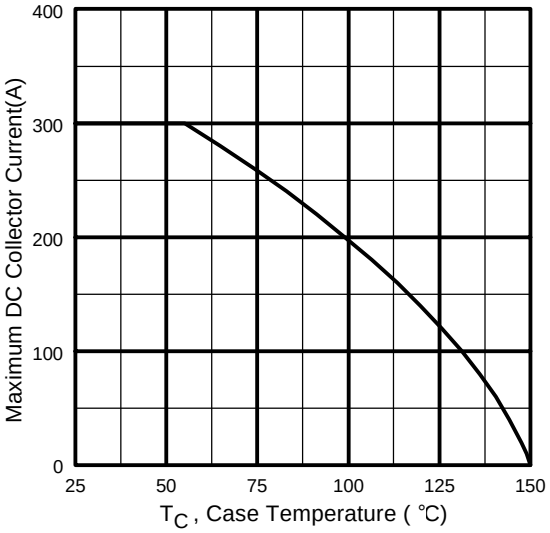


Fig. 4 - Maximum Collector Current vs. Case Temperature

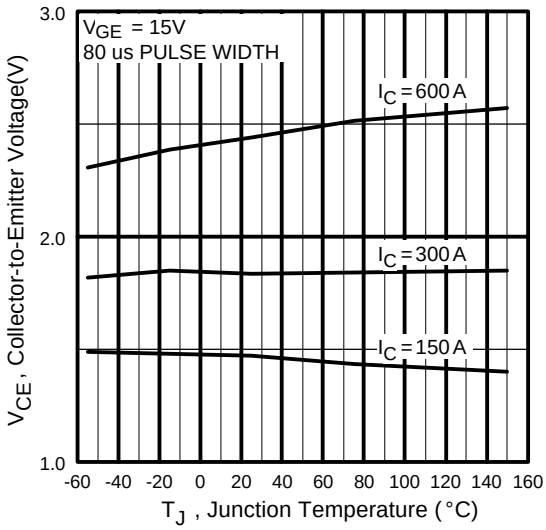


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

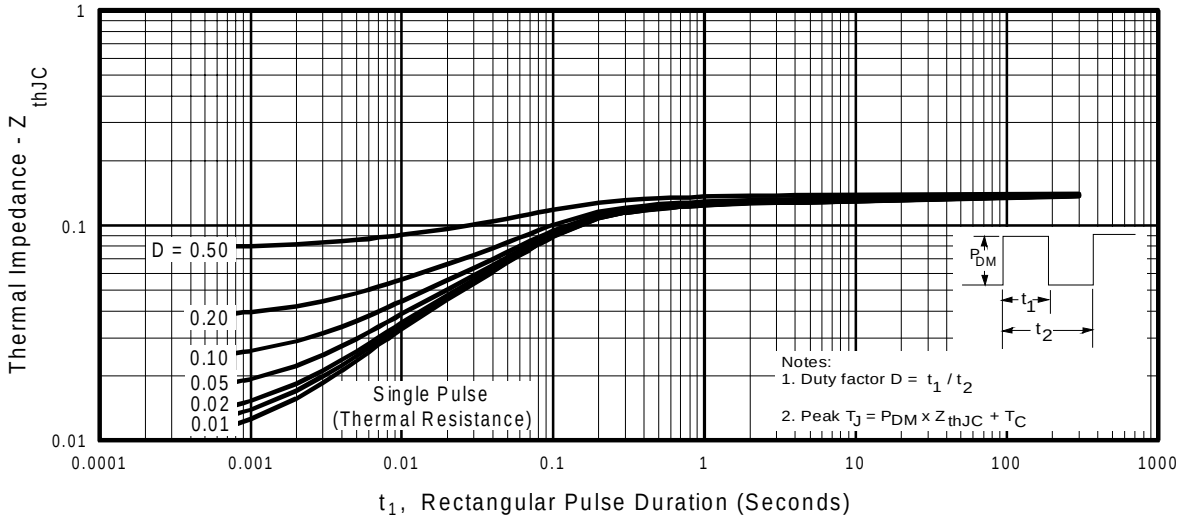


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

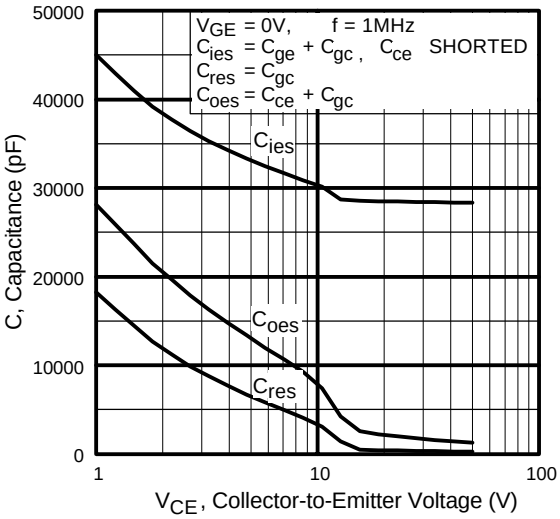


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

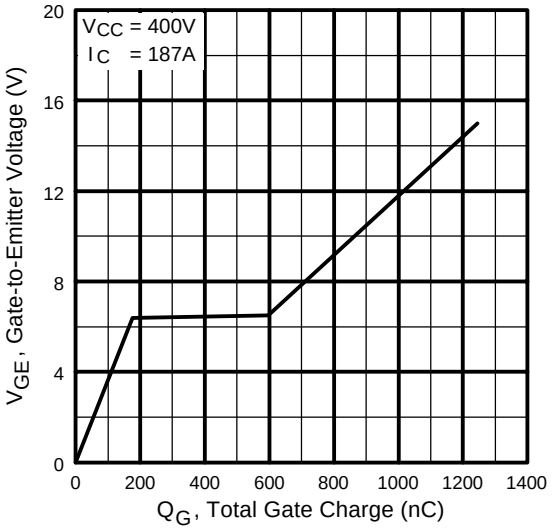


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

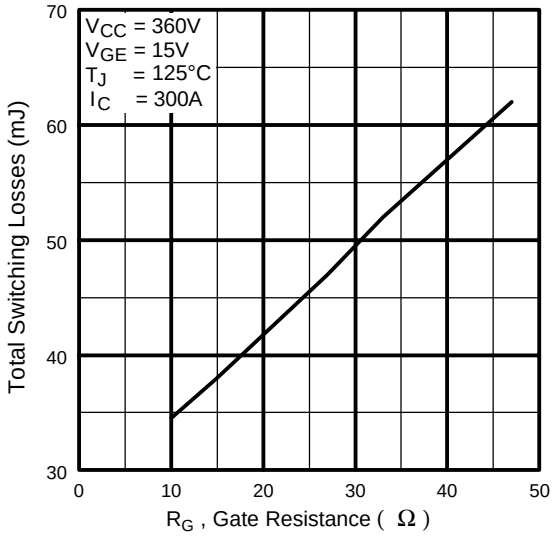


Fig. 9 - Typical Switching Losses vs. Gate Resistance

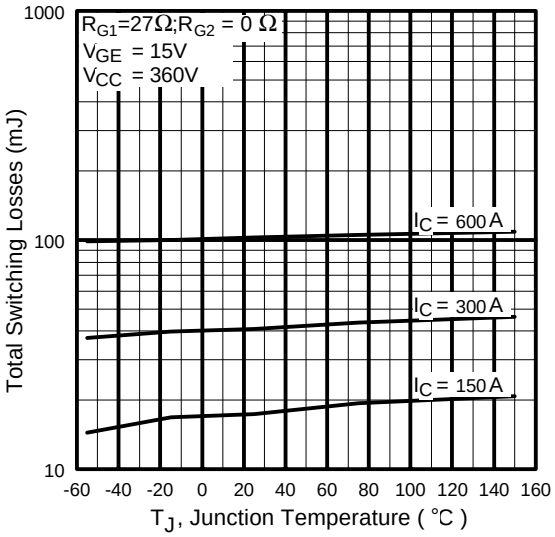


Fig. 10 - Typical Switching Losses vs. Junction Temperature

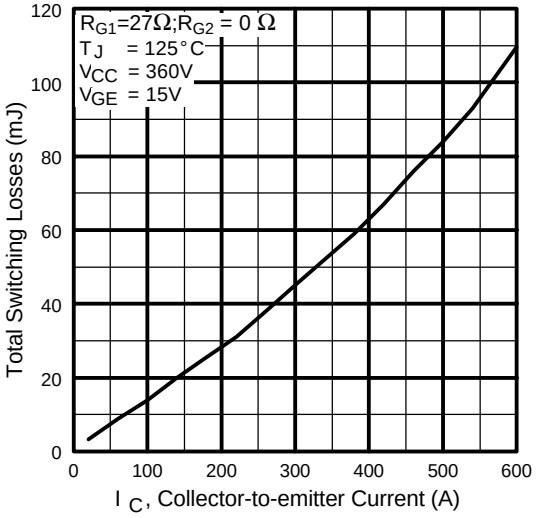


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

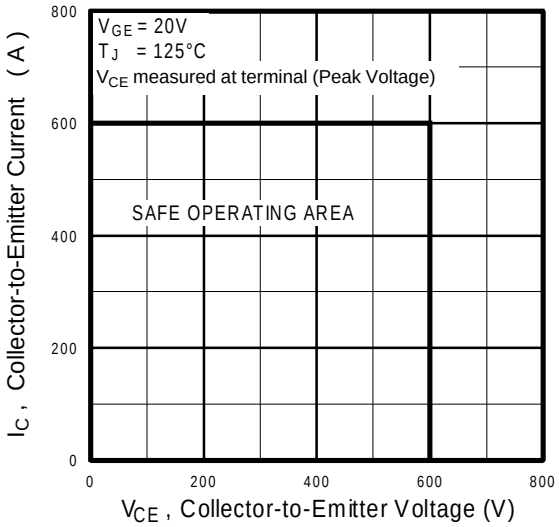


Fig. 12 - Reverse Bias SOA

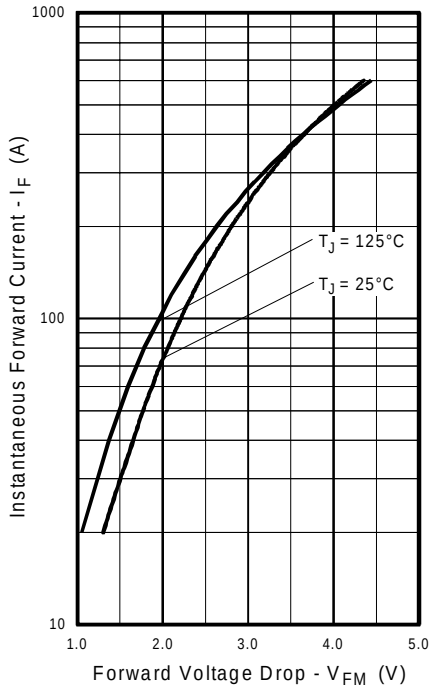


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

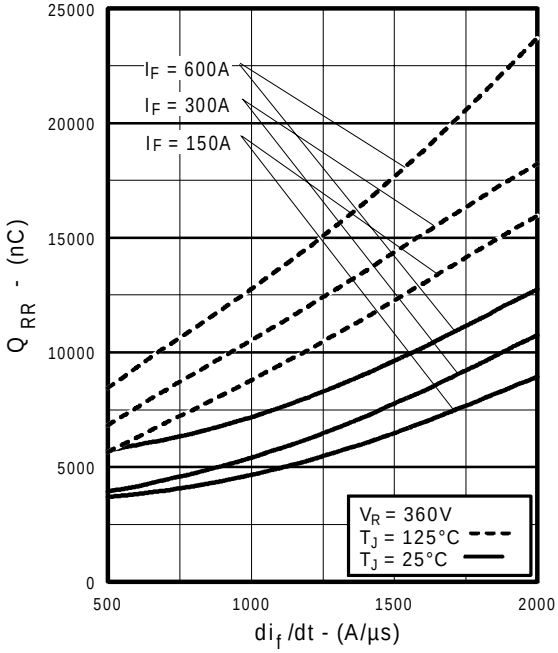


Fig. 14 - Typical Stored Charge vs. di_f/dt

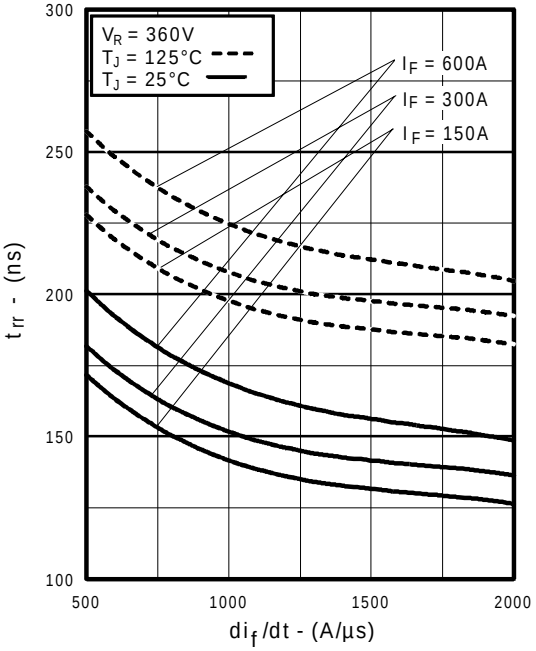


Fig. 15 - Typical Reverse Recovery vs. di_f/dt

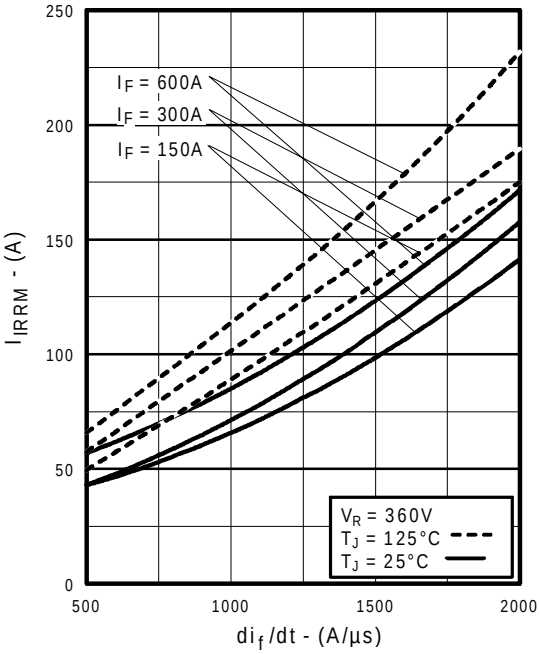


Fig. 16 - Typical Recovery Current vs. di_f/dt

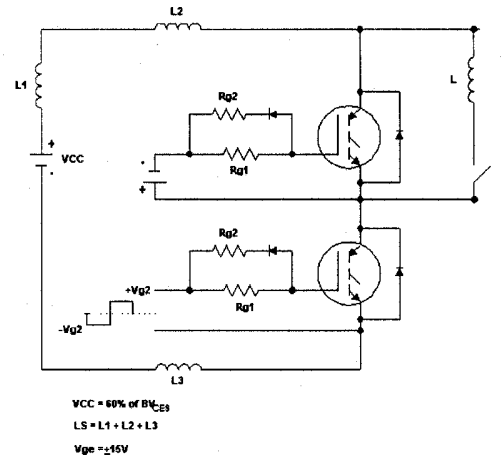


Fig. 17a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

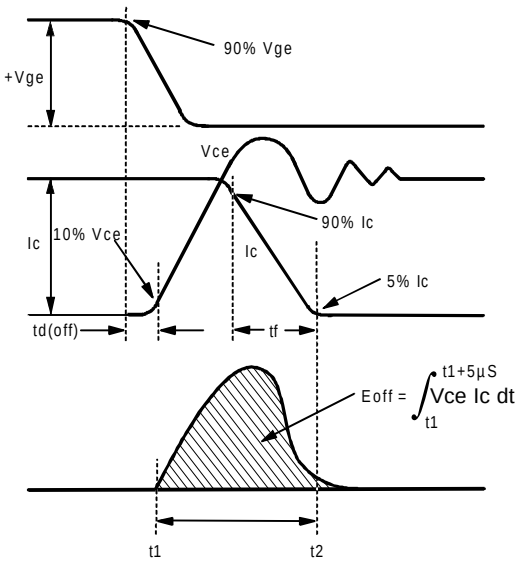


Fig. 17b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

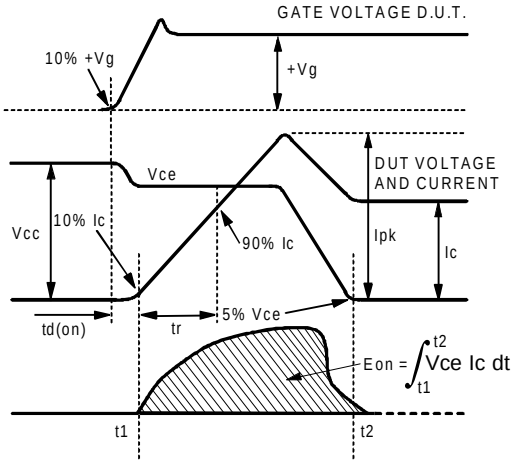


Fig. 17c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

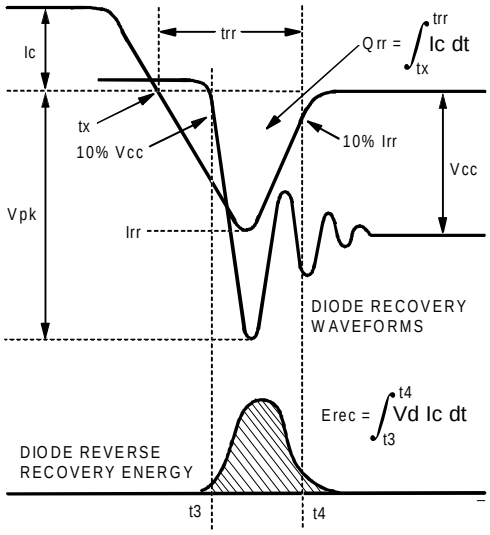


Fig. 17d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

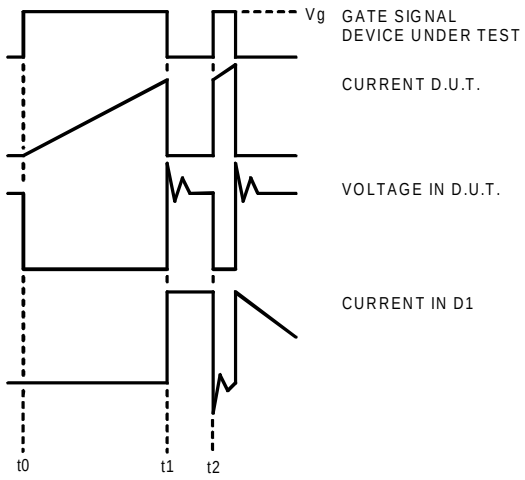


Figure 17e. Macro Waveforms for Figure 17a's Test Circuit

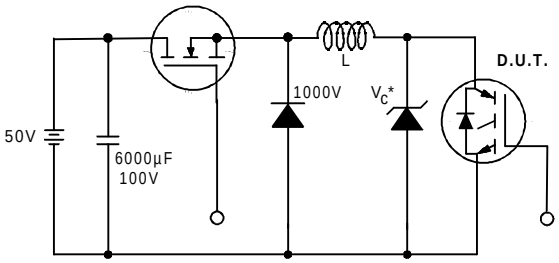


Figure 18. Clamped Inductive Load Test Circuit

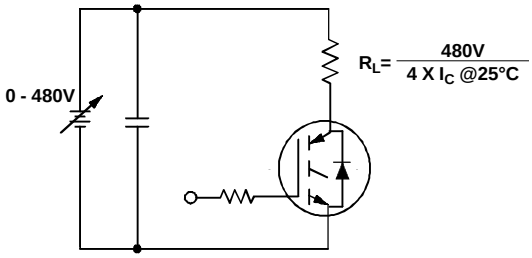


Figure 19. Pulsed Collector Current Test Circuit

Notes:

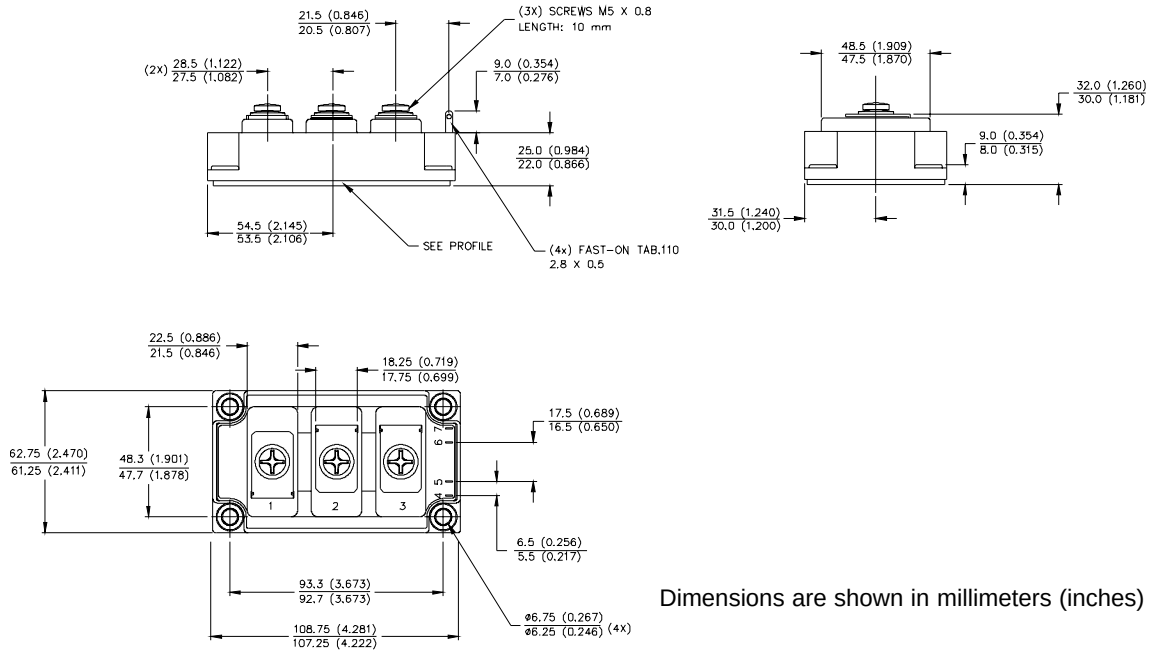
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 17

③ For screws M5x0.8

④ Pulse width 80µs; single shot.

Case Outline — DOUBLE INT-A-PAK



Dimensions are shown in millimeters (inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

International
IOR Rectifier

PD - 50059C

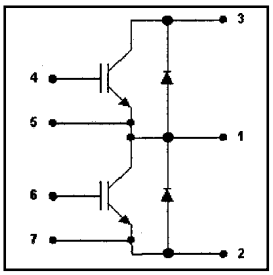
GA400TD60U

"HALF-BRIDGE" IGBT DOUBLE INT-A-PAK

Ultra-Fast™ Speed IGBT

Features

- Generation 4 IGBT technology
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL approved



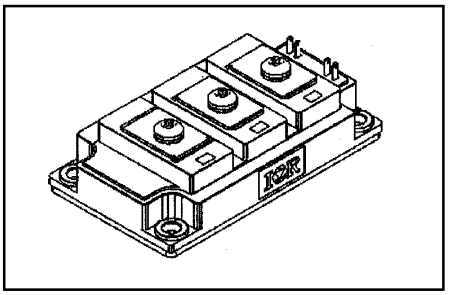
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.70V

@V_{GE} = 15V, I_C = 400A

Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	400	A
I_{CM}	Pulsed Collector Current①	800	
I_{LM}	Peak Switching Current②	800	
I_{FM}	Peak Diode Forward Current	800	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	1250	W
P_D @ T_C = 85°C	Maximum Power Dissipation	650	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.10	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.20	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3③	—	3.0	
	Weight of Module	400	—	g

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	1.7	2.4		V_{GE} = 15V, I_C = 400A
		—	1.8	—		V_{GE} = 15V, I_C = 400A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		I_C = 2.5mA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 2.5mA
g_{fe}	Forward Transconductance ④	—	481	—	S	V_{CE} = 25V, I_C = 400A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	2.0	mA	V_{GE} = 0V, V_{CE} = 600V
		—	—	20		V_{GE} = 0V, V_{CE} = 600V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	3.7	—	V	I_F = 400A, V_{GE} = 0V
		—	3.6	—		I_F = 400A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	500	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	1806	2709	nC	V_{CC} = 400V
Qge	Gate - Emitter Charge (turn-on)	—	251	376		I_C = 270A ,V_{GE} = 15V
Q_{gc}	Gate - Collector Charge (turn-on)	—	612	918		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	1033	—	ns	R_{G1} = 15Ω, R_{G2} = 0Ω,
t_r	Rise Time	—	335	—		I_C = 400A
$t_{d(off)}$	Turn-Off Delay Time	—	688	—		V_{CC} = 360V
t_f	Fall Time	—	225	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	26	—	mJ	
$E_{off\ (1)}$	Turn-Off Switching Energy	—	48	—		
$E_{ts\ (1)}$	Total Switching Energy	—	74	89		
C_{ies}	Input Capacitance	—	40136	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	2509	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	522	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	232	—	ns	I_C = 400A
I_{rr}	Diode Peak ReverseCurrent	—	141	—	A	R_{G1} = 15Ω
Q_{rr}	Diode Recovery Charge	—	16292	—	nC	R_{G2} = 0Ω
$di_{(rec)}M_{/dt}$	Diode Peak Rate of Fall of Recovery During t_b	—	1641	—	A/µs	V_{CC} = 360V di/dt=1300A/µs

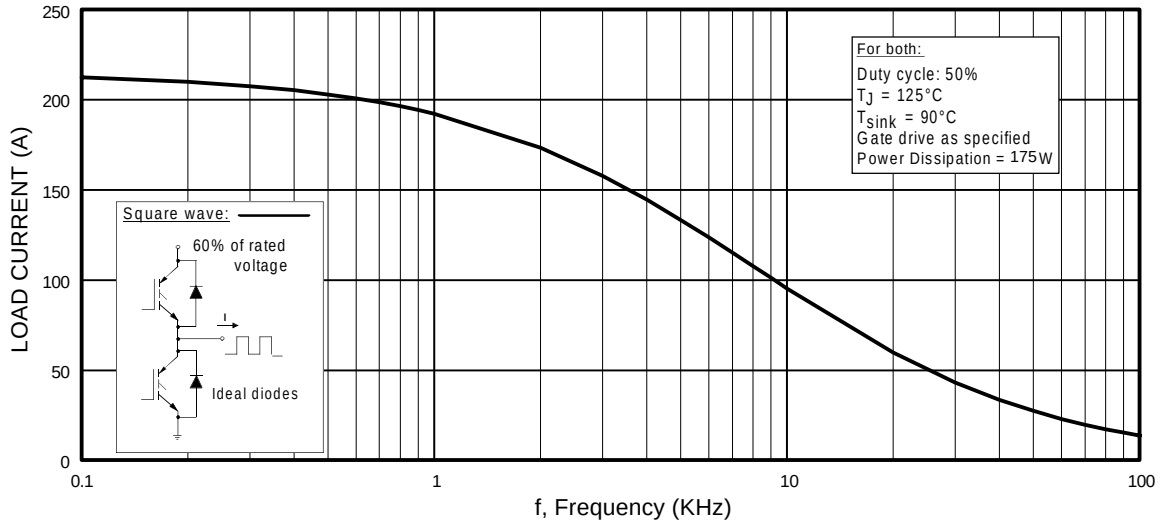


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

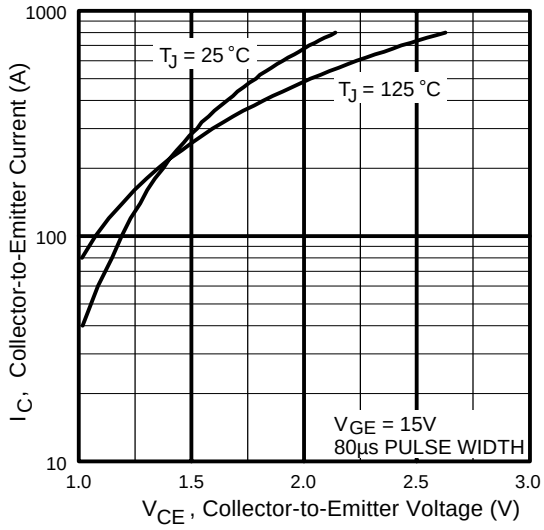


Fig. 2 - Typical Output Characteristics

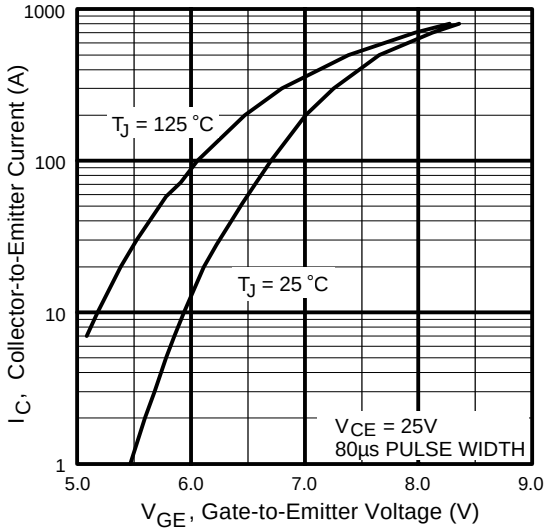


Fig. 3 - Typical Transfer Characteristics

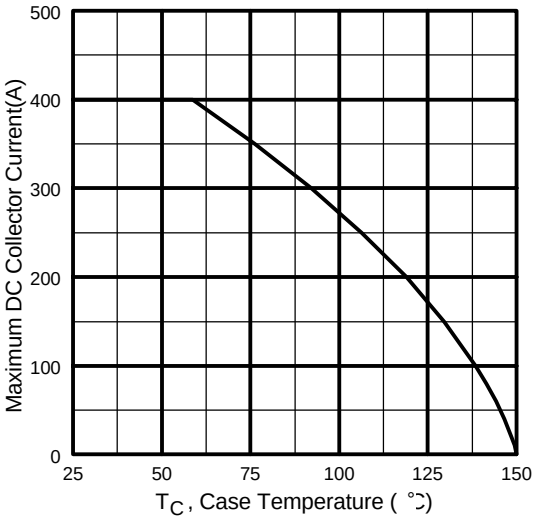


Fig. 4 - Maximum Collector Current vs. Case Temperature

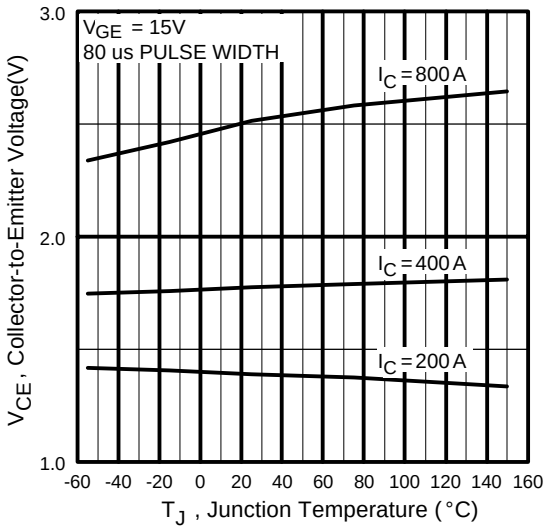


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

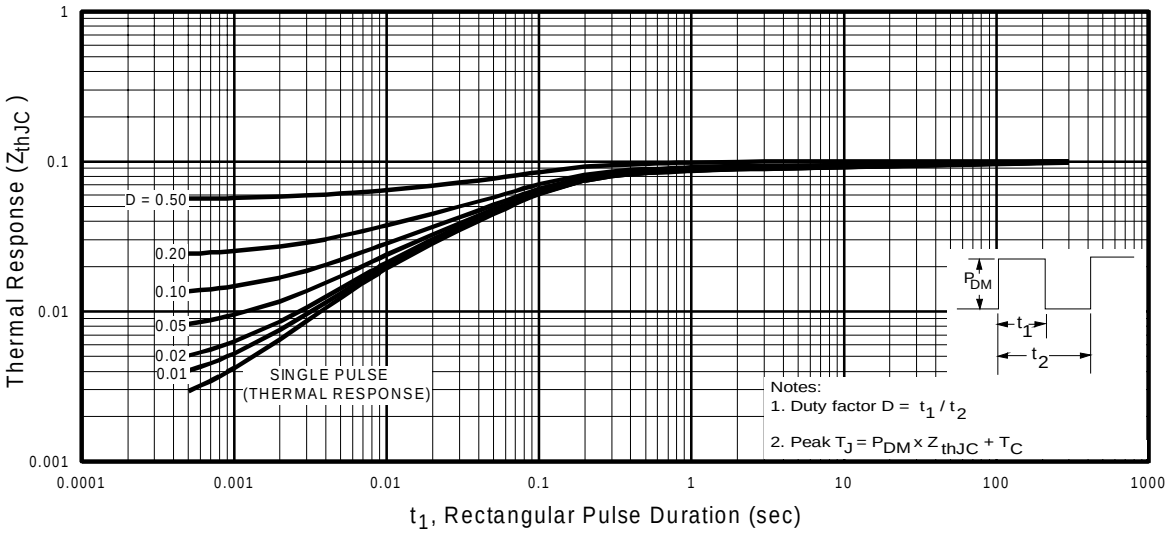


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

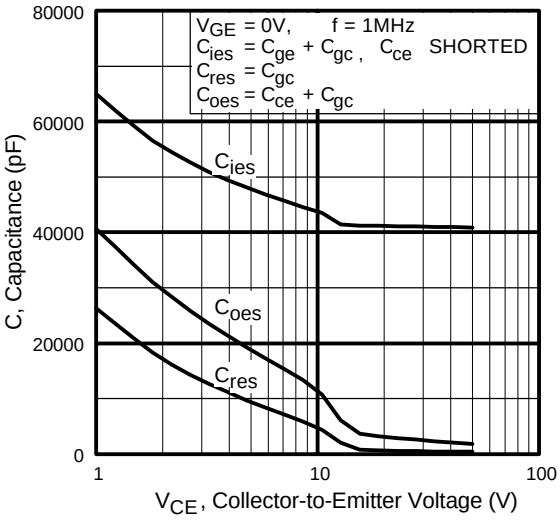


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

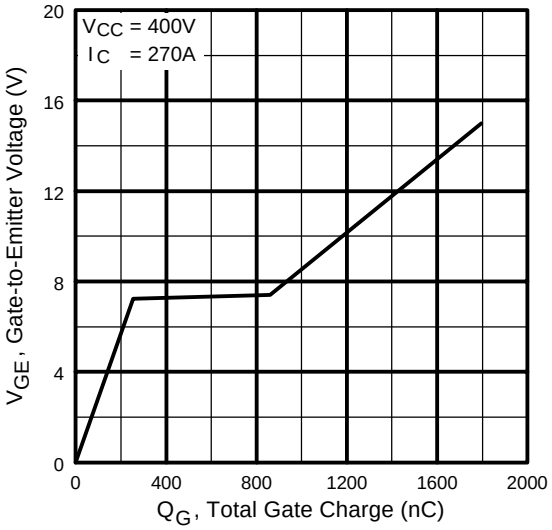


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

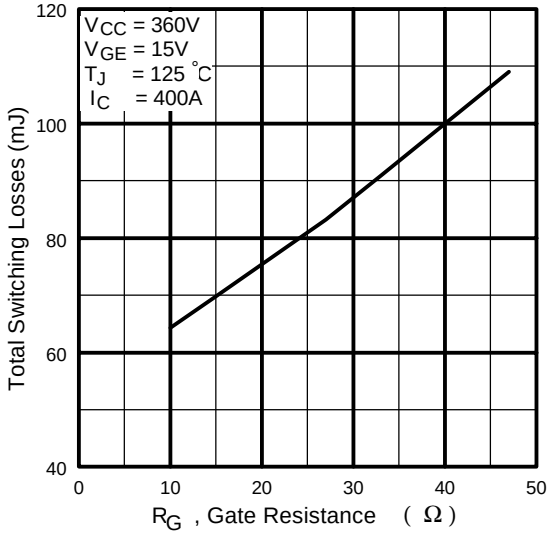


Fig. 9 - Typical Switching Losses vs. Gate Resistance

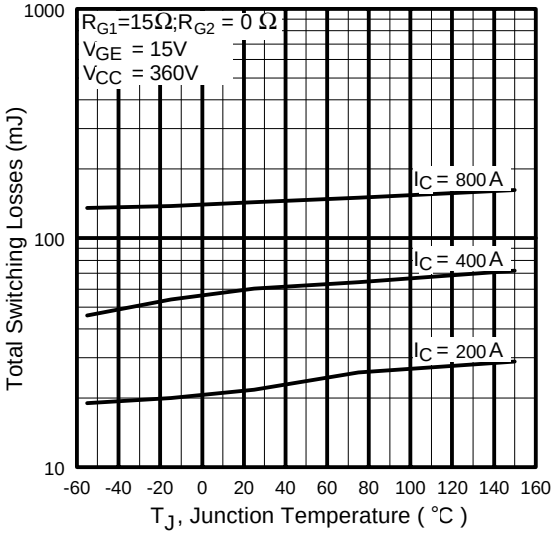


Fig. 10 - Typical Switching Losses vs. Junction Temperature

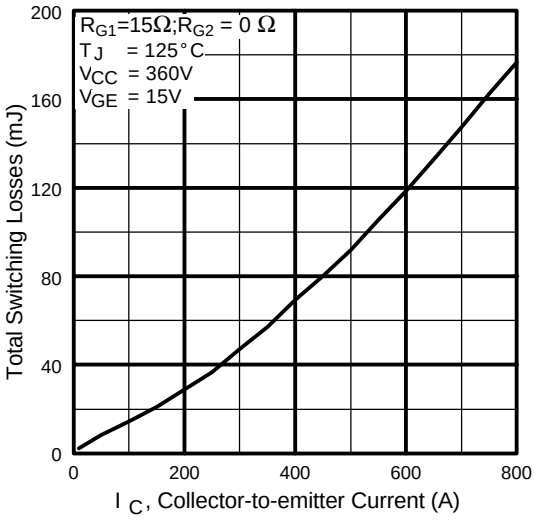


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

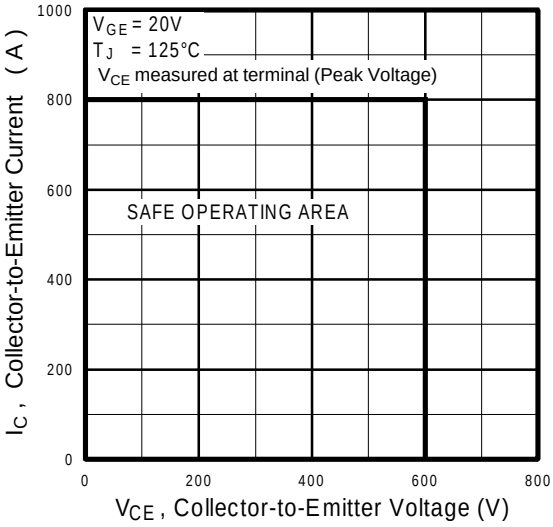


Fig. 12 - Reverse Bias SOA

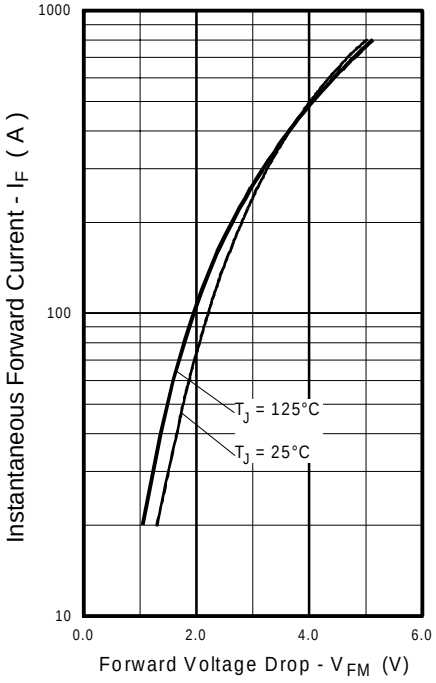


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

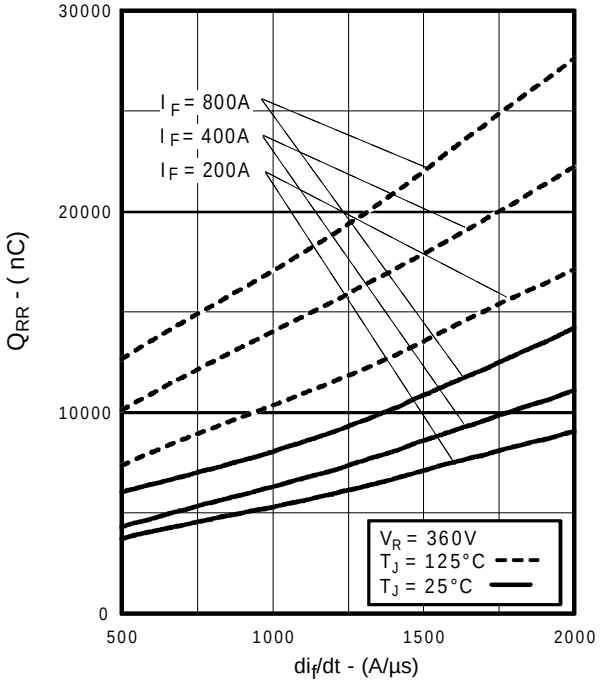


Fig. 14 - Typical Stored Charge vs. di_f/dt

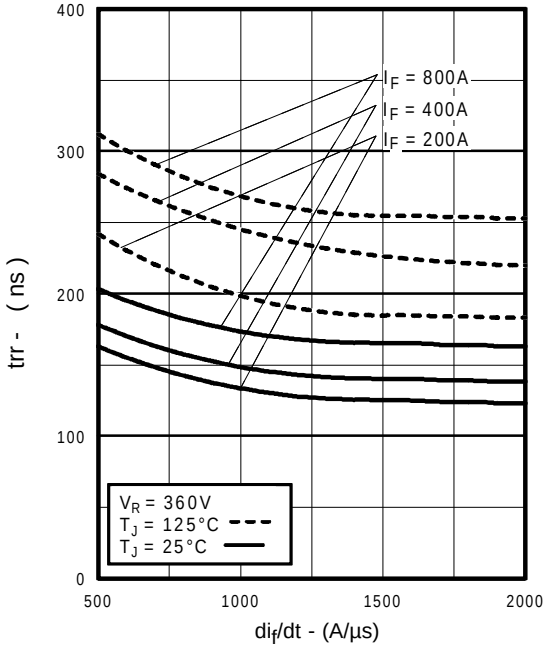


Fig. 15 - Typical Reverse Recovery vs. di_f/dt

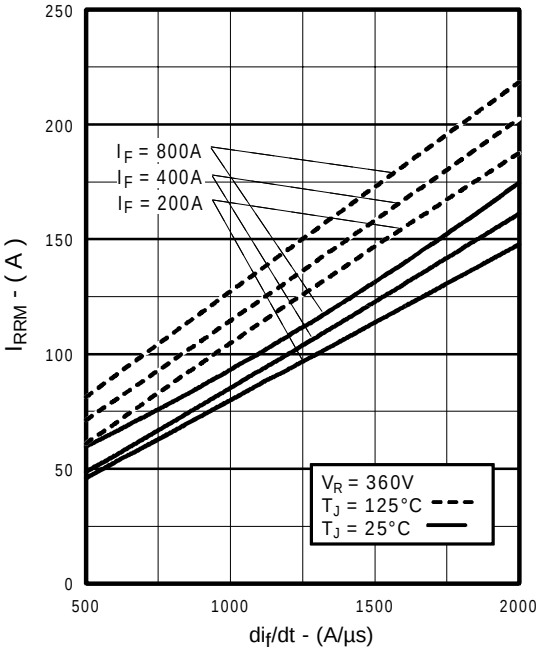


Fig. 16 - Typical Recovery Current vs. di_f/dt

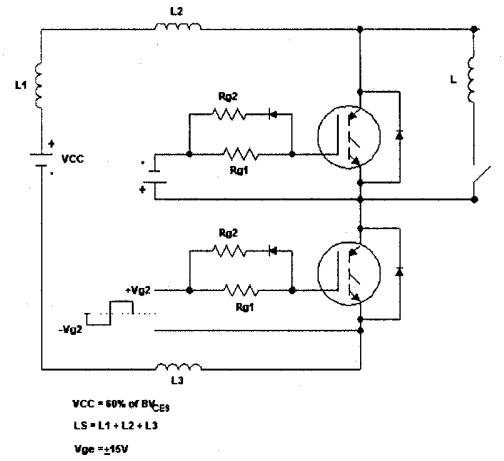


Fig. 17a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

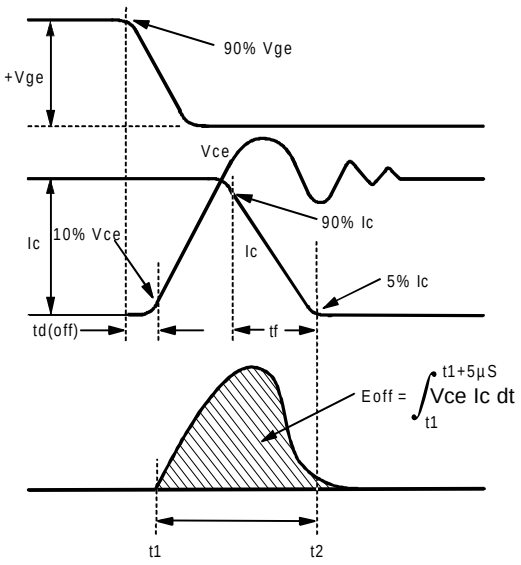


Fig. 17b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

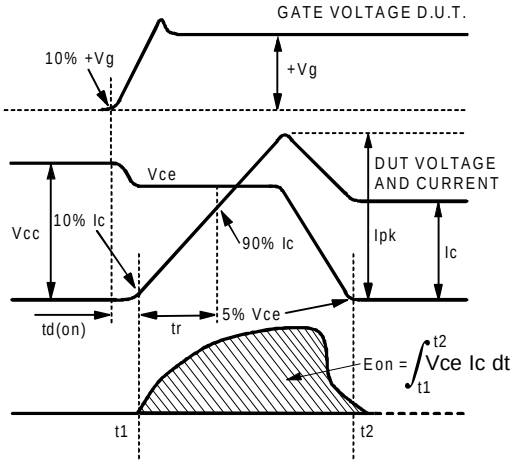


Fig. 17c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

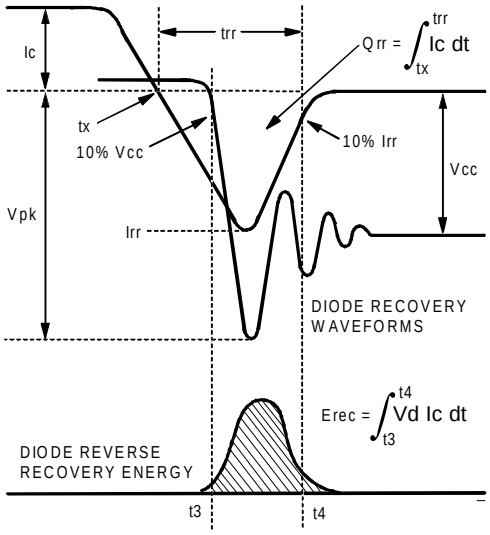


Fig. 17d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

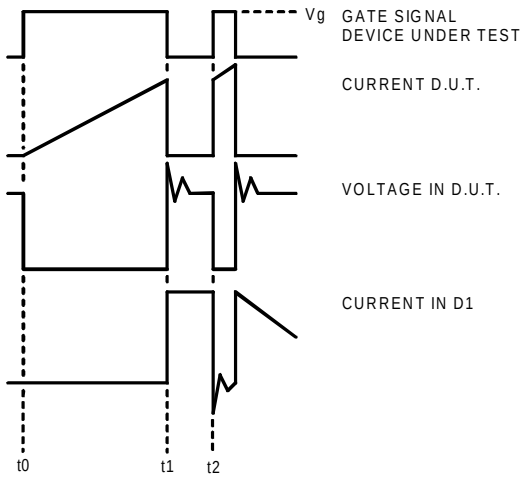


Figure 17e. Macro Waveforms for Figure 18a's Test Circuit

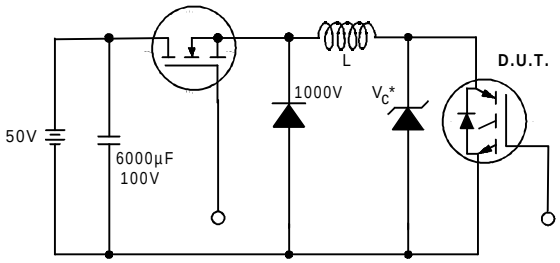


Figure 18. Clamped Inductive Load Test Circuit

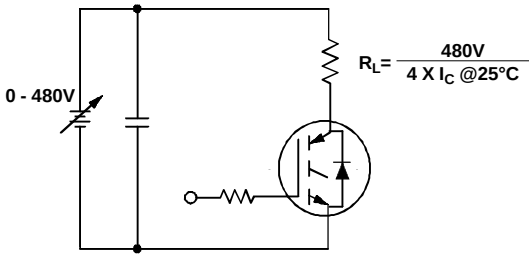


Figure 19. Pulsed Collector Current Test Circuit

Notes:

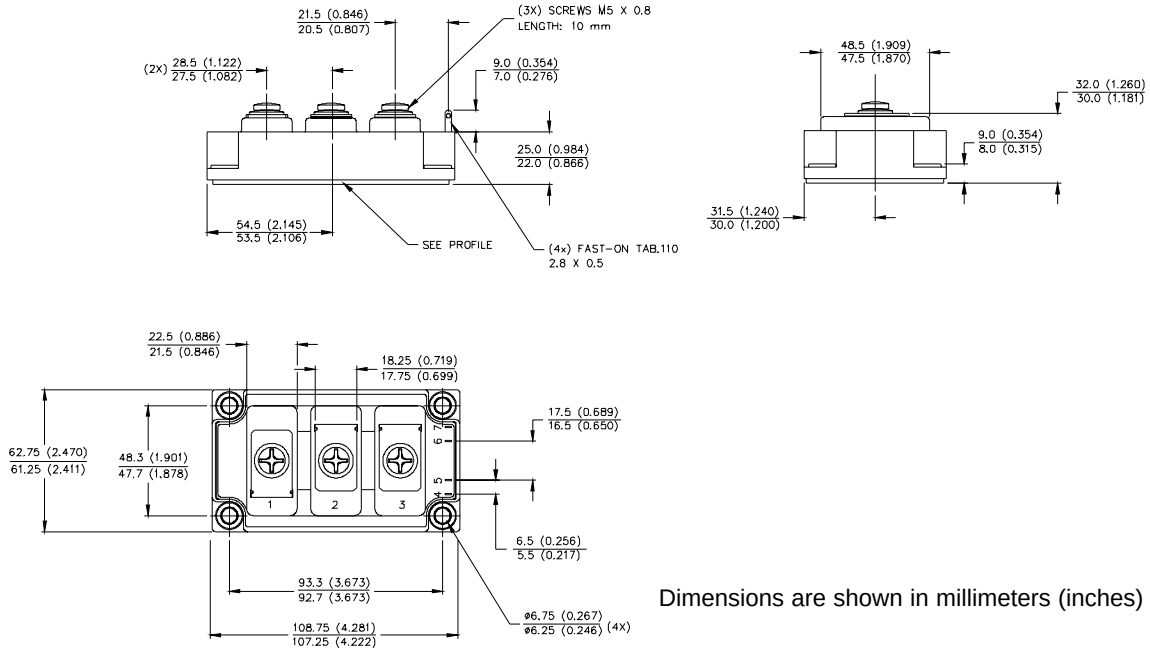
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 17

③ For screws M5x0.8

④ Pulse width 50µs; single shot.

Case Outline — DOUBLE INT-A-PAK



Dimensions are shown in millimeters (inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

International
IOR Rectifier

PD - 50048C

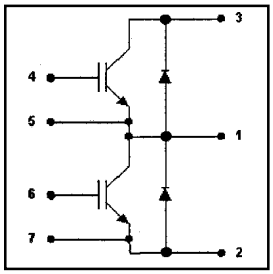
GA500TD60U

"HALF-BRIDGE" IGBT DOUBLE INT-A-PAK

Ultra-Fast™ Speed IGBT

Features

- Generation 4 IGBT technology
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL approved



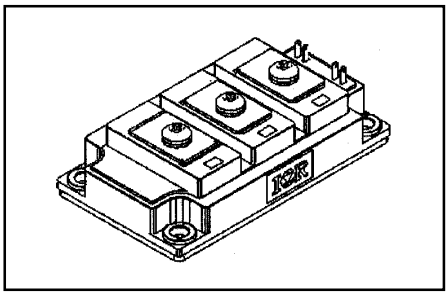
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.9V

@V_{GE} = 15V, I_C = 500A

Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	500	A
I_{CM}	Pulsed Collector Current①	1000	
I_{LM}	Peak Switching Current②	1000	
I_{FM}	Peak Diode Forward Current	500	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	1550	W
P_D @ T_C = 85°C	Maximum Power Dissipation	800	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.08	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.20	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3ƒ	—	3.0	
	Weight of Module	400	—	g

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	1.9	2.4		V_{GE} = 15V, I_C = 500A
		—	2.0	—		V_{GE} = 15V, I_C = 500A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		I_C = 3.0mA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 3.0mA
g_{fe}	Forward Transconductance ④	—	244	—	S	V_{CE} = 25V, I_C = 500A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	2.0	mA	V_{GE} = 0V, V_{CE} = 600V
		—	—	20		V_{GE} = 0V, V_{CE} = 600V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	4.0	—	V	I_F = 500A, V_{GE} = 0V
		—	4.1	—		I_F = 500A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	250	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	2100	3200	nC	V_{CC} = 400V
Q_{ge}	Gate - Emitter Charge (turn-on)	—	292	440		I_C = 500A
Q_{gc}	Gate - Collector Charge (turn-on)	—	1050	1580		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	1900	—	ns	R_{G1} = 15Ω, R_{G2} = 0Ω,
t_r	Rise Time	—	430	—		I_C = 500A
$t_{d(off)}$	Turn-Off Delay Time	—	800	—		V_{CC} = 360V
t_f	Fall Time	—	190	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	41	—	mJ	See Fig.17 through Fig.21
E_{off}	Turn-Off Switching Energy	—	56	—		
E_{ts}	Total Switching Energy	—	97	110		
C_{ies}	Input Capacitance	—	46800	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	2920	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	600	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	246	—	ns	I_C = 500A
I_{rr}	Diode Peak ReverseCurrent	—	144	—	A	R_{G1} = 15Ω
Q_{rr}	Diode Recovery Charge	—	17655	—	µC	R_{G2} = 0Ω
$di_{(rec)}M_{/dt}$	Diode Peak Rate of Fall of Recovery During t_b	—	1386	—	A/µs	V_{CC} = 360V di/dt=1300A/µs

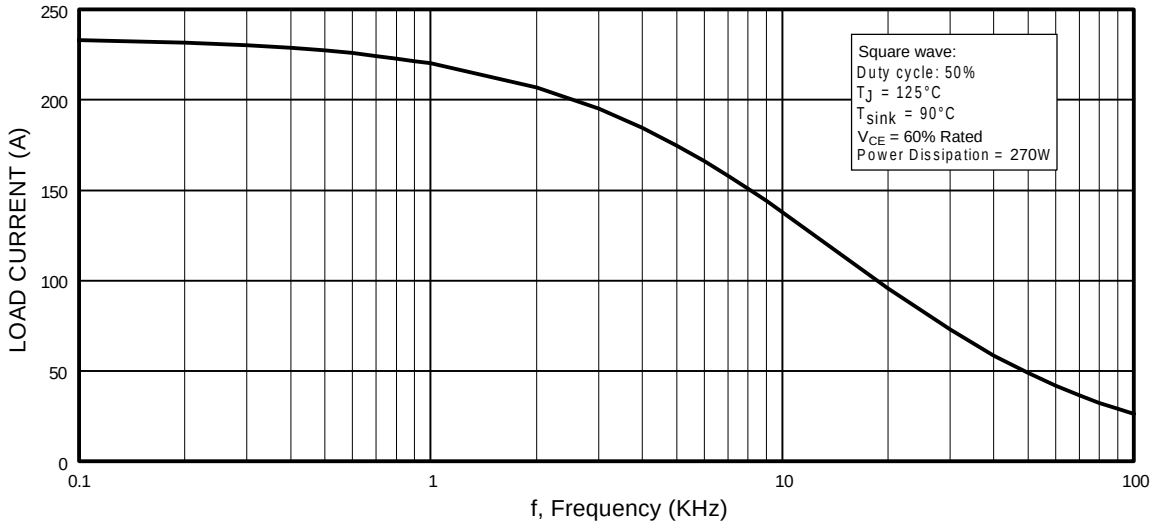


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

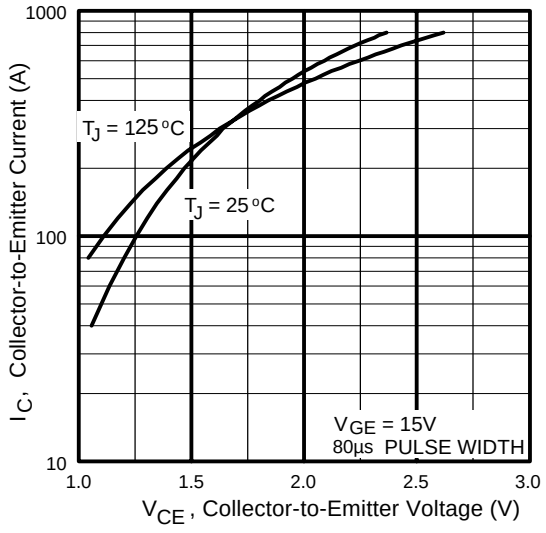


Fig. 2 - Typical Output Characteristics

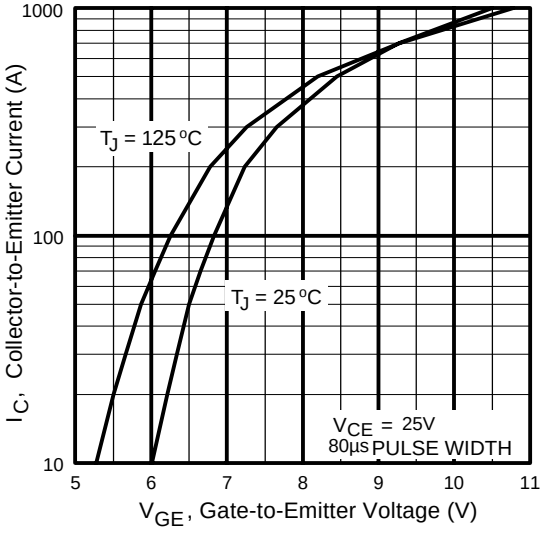


Fig. 3 - Typical Transfer Characteristics

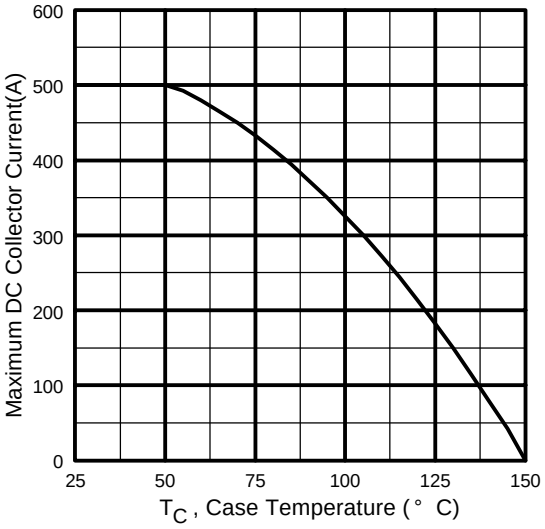


Fig. 4 - Maximum Collector Current vs. Case Temperature

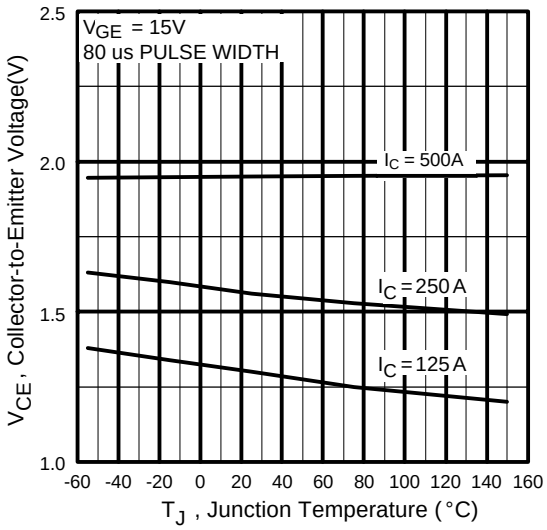


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

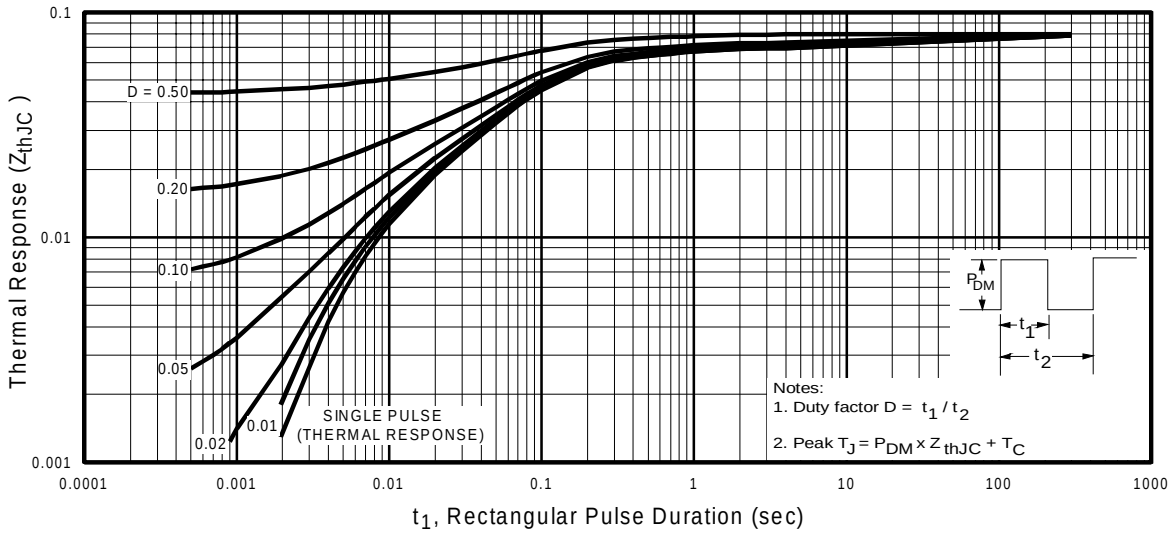


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

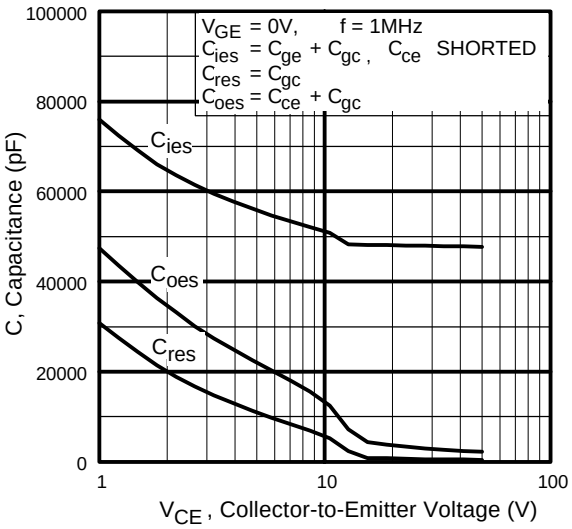


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

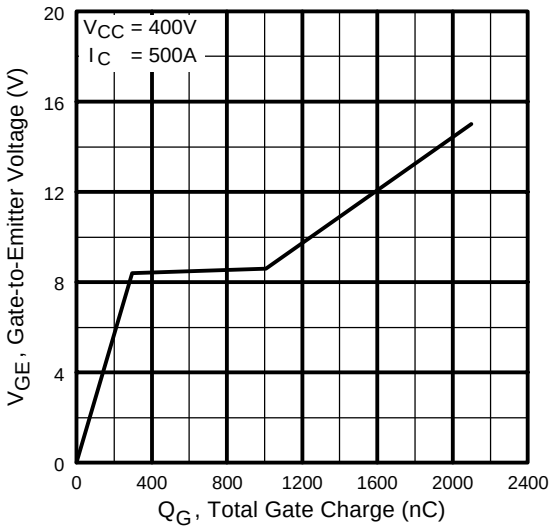


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

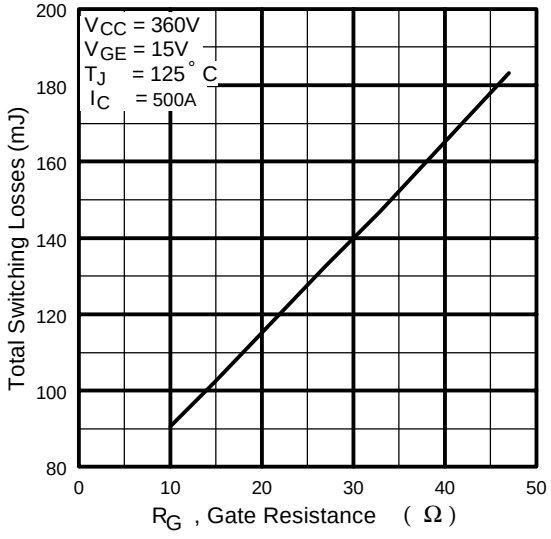


Fig. 9 - Typical Switching Losses vs. Gate Resistance

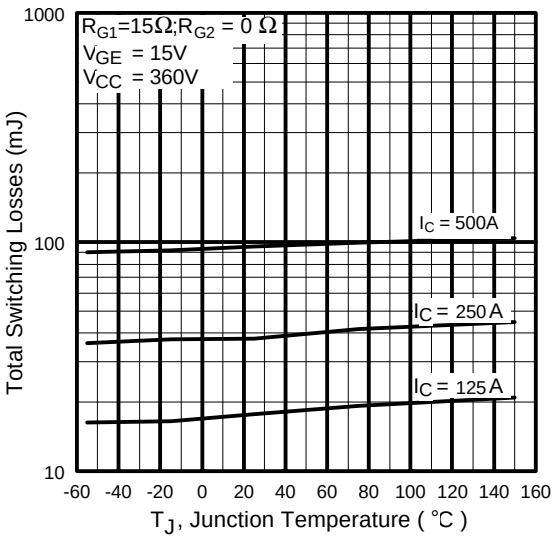


Fig. 10 - Typical Switching Losses vs. Junction Temperature

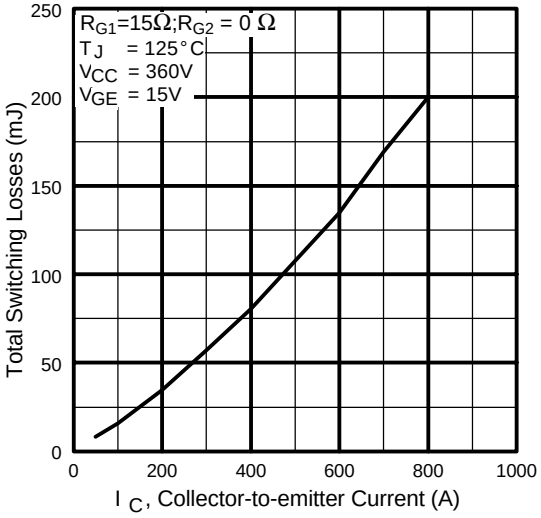


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

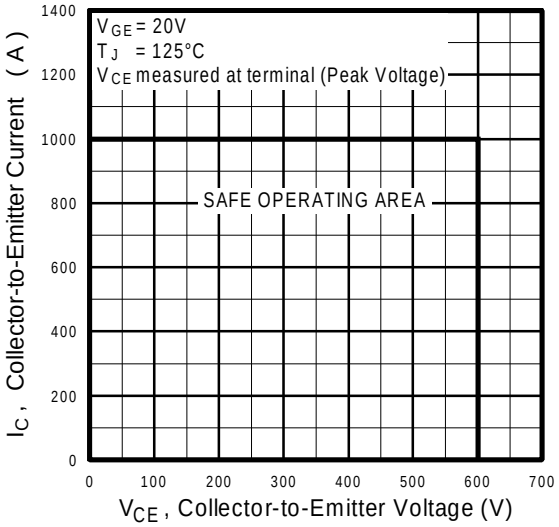


Fig. 12 - Reverse Bias SOA

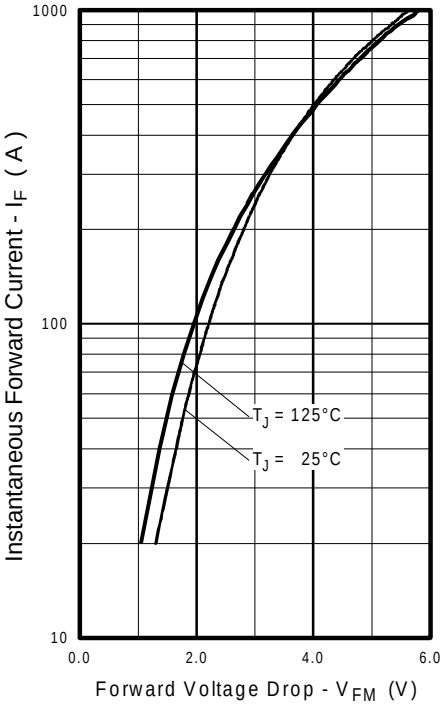


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

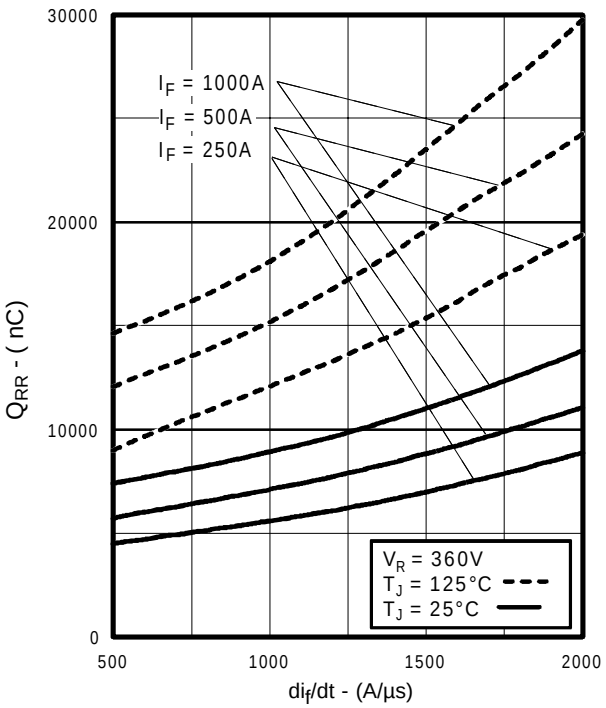


Fig. 14 - Typical Stored Charge vs. di_f/dt

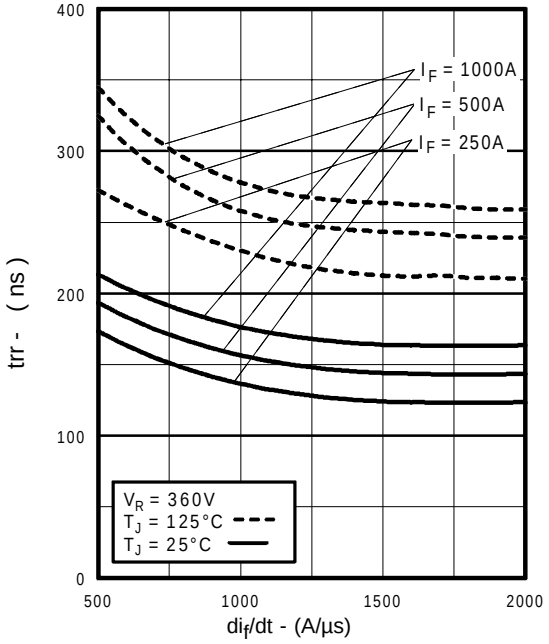


Fig. 15 - Typical Reverse Recovery vs. di_f/dt

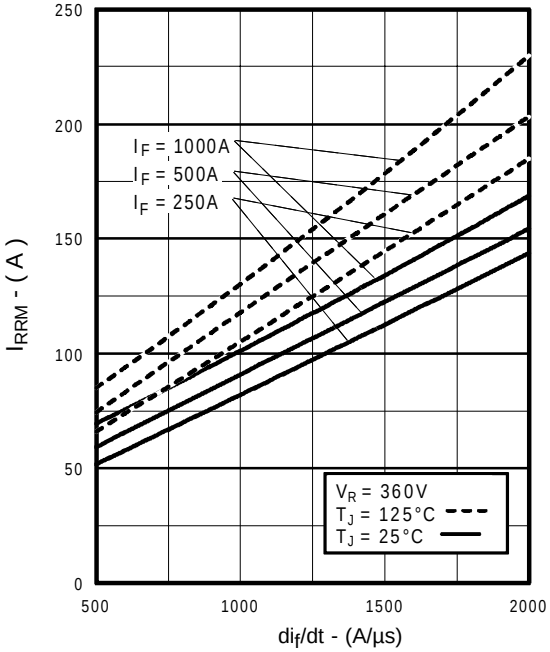


Fig. 16 - Typical Recovery Current vs. di_f/dt

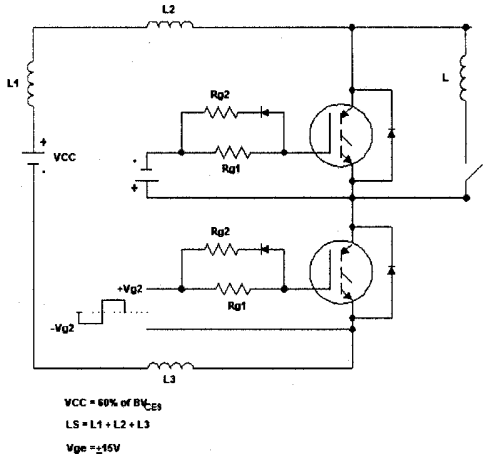


Fig. 17 - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

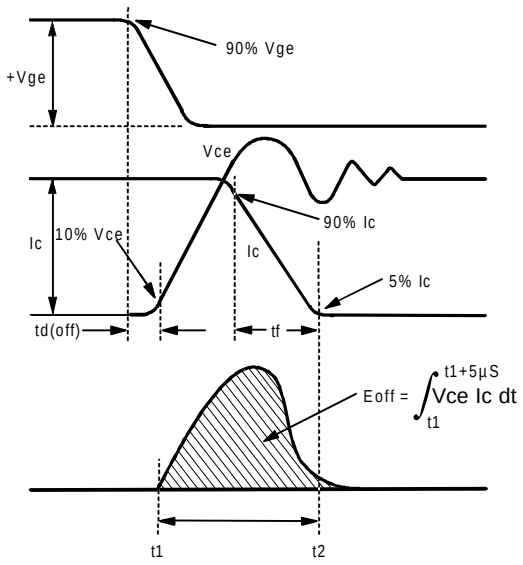


Fig. 18 - Test Waveforms for Circuit of Fig. 17, Defining E_{off}, $t_{d(off)}$, t_f

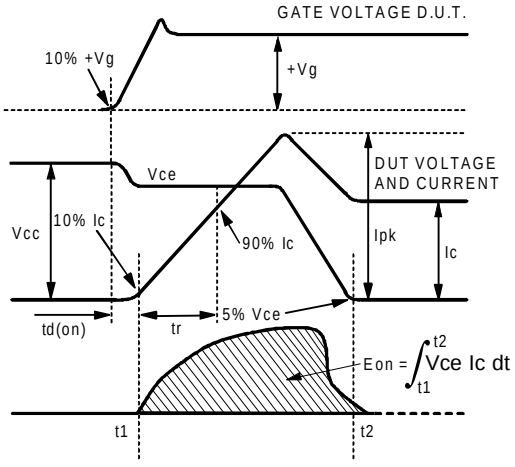


Fig. 19 - Test Waveforms for Circuit of Fig. 17, Defining E_{on}, $t_{d(on)}$, t_r

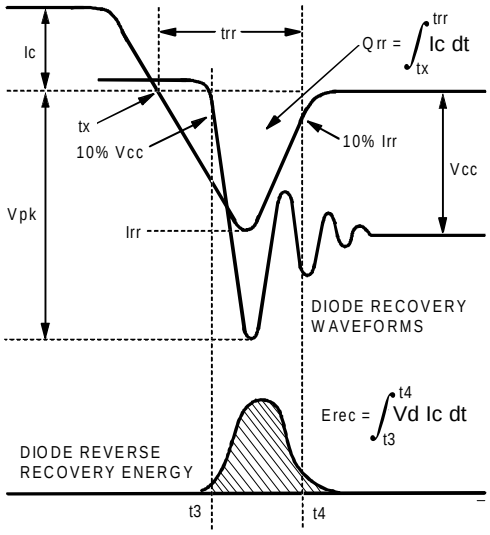


Fig. 20 - Test Waveforms for Circuit of Fig. 17, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

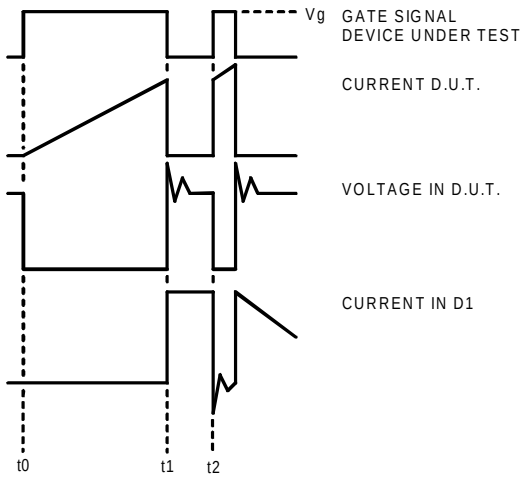


Figure 21. Macro Waveforms for Figure 17's Test Circuit

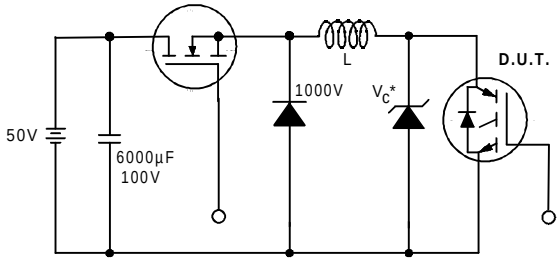


Figure 22. Clamped Inductive Load Test Circuit

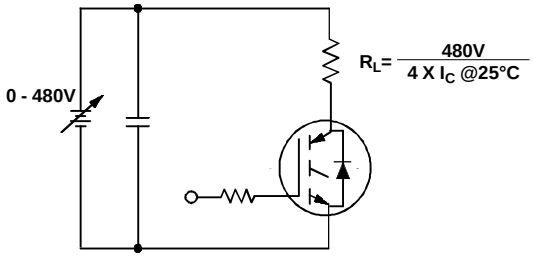


Figure 23. Pulsed Collector Current Test Circuit

Notes:

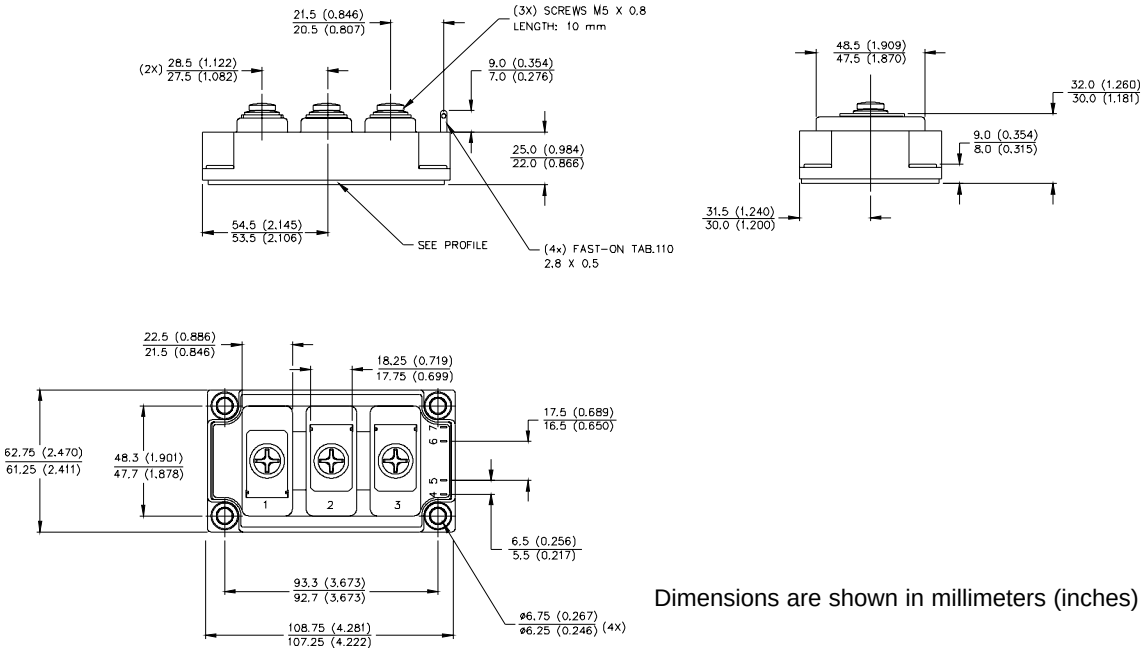
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 17

③ For screws M5x0.8

④ Pulse width 80µs; single shot.

Case Outline — DOUBLE INT-A-PAK



Dimensions are shown in millimeters (inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 10/00

PD - 50064A

International
IOR Rectifier

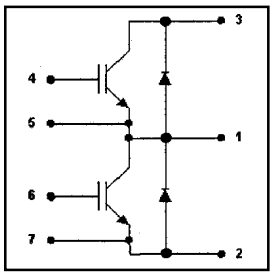
GA50TS120U

"HALF-BRIDGE" IGBT INT-A-PAK

Ultra-Fast™ Speed IGBT

Features

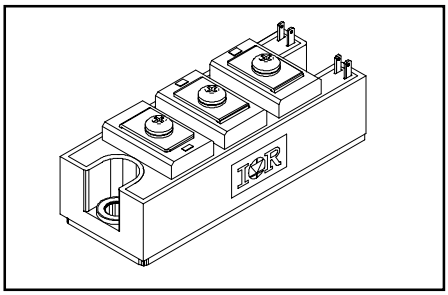
- Generation 4 IGBT technology
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL approved



V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.4V

@V_{GE} = 15V, I_C = 50A



Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	50	A
I_{CM}	Pulsed Collector Current ①	100	
I_{LM}	Peak Switching Current ②	100	
I_{FM}	Peak Diode Forward Current	100	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	280	W
P_D @ T_C = 85°C	Maximum Power Dissipation	145	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.44	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.70	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3 ③	—	3.0	
	Weight of Module	200	—	g

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	2.4	3.0		V_{GE} = 15V, I_C = 50A
		—	2.2	—		V_{GE} = 15V, I_C = 50A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = 6.0V, I_C = 500µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = 6.0V, I_C = 500µA
g_{fe}	Forward Transconductance ④	—	72	—	S	V_{CE} = 25V, I_C = 50A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	1.0	mA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	10		V_{GE} = 0V, V_{CE} = 1200V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	2.9	4.1	V	I_F = 50A, V_{GE} = 0V
		—	2.7	—		I_F = 50A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	250	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	397	596	nC	V_{CC} = 400V
Qge	Gate - Emitter Charge (turn-on)	—	67	100		I_C = 60A
Q_{gc}	Gate - Collector Charge (turn-on)	—	132	197		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	74	—	ns	R_{G1} = 15Ω, R_{G2} = 0Ω,
t_r	Rise Time	—	82	—		I_C = 50A
$t_{d(off)}$	Turn-Off Delay Time	—	313	—		V_{CC} = 720V
t_f	Fall Time	—	327	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	6.0	—	mJ	Inductor load
$E_{off\ (1)}$	Turn-Off Switching Energy	—	10	—		
$E_{ts\ (1)}$	Total Switching Energy	—	16	24		
C_{ies}	Input Capacitance	—	8933	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	397	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	77	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	141	—	ns	I_C = 50A
I_{rr}	Diode Peak ReverseCurrent	—	66	—	A	R_{G1} = 15Ω
Q_{rr}	Diode Recovery Charge	—	4616	—	nC	R_{G2} = 0Ω
$di_{(rec)}M_{/dt}$	Diode Peak Rate of Fall of Recovery During t_b	—	999	—	A/µs	V_{CC} = 720V di/dt = 1200A/µs

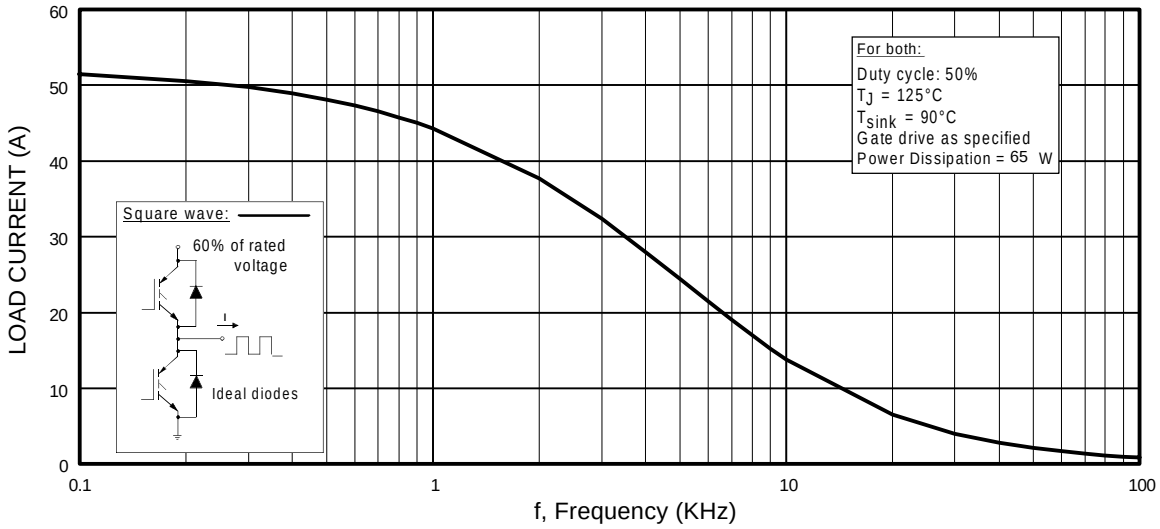


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

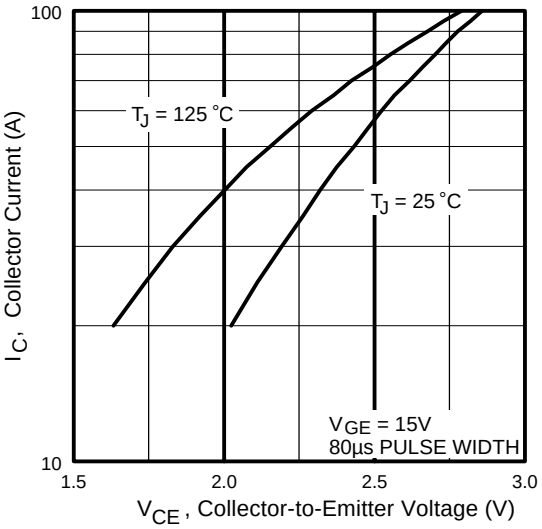


Fig. 2 - Typical Output Characteristics

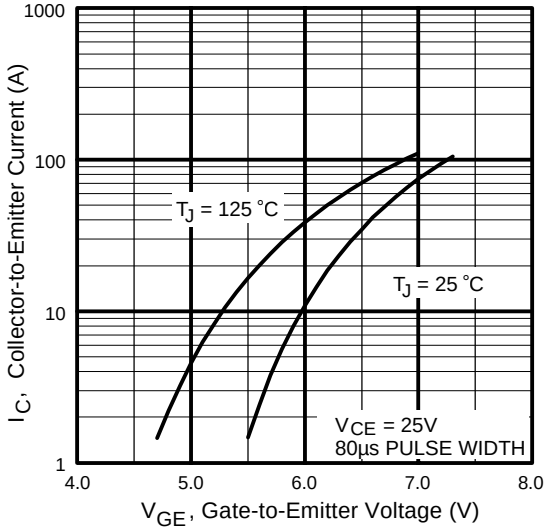


Fig. 3 - Typical Transfer Characteristics

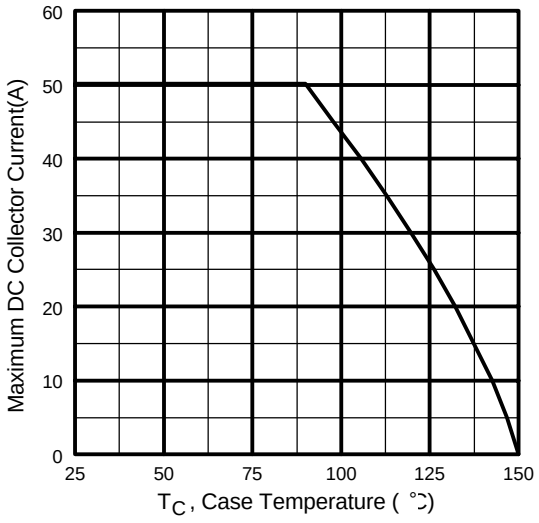


Fig. 4 - Maximum Collector Current vs. Case Temperature

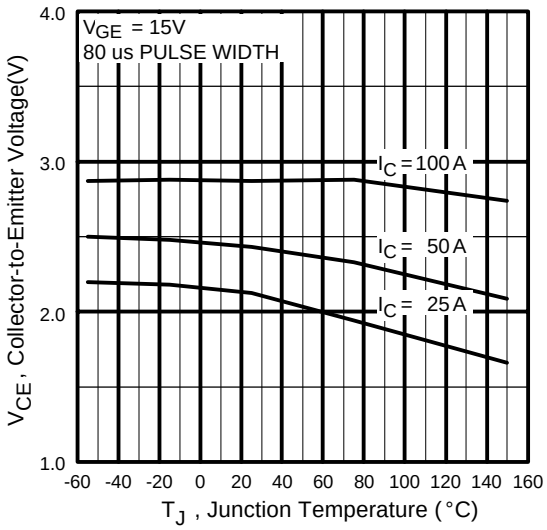


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

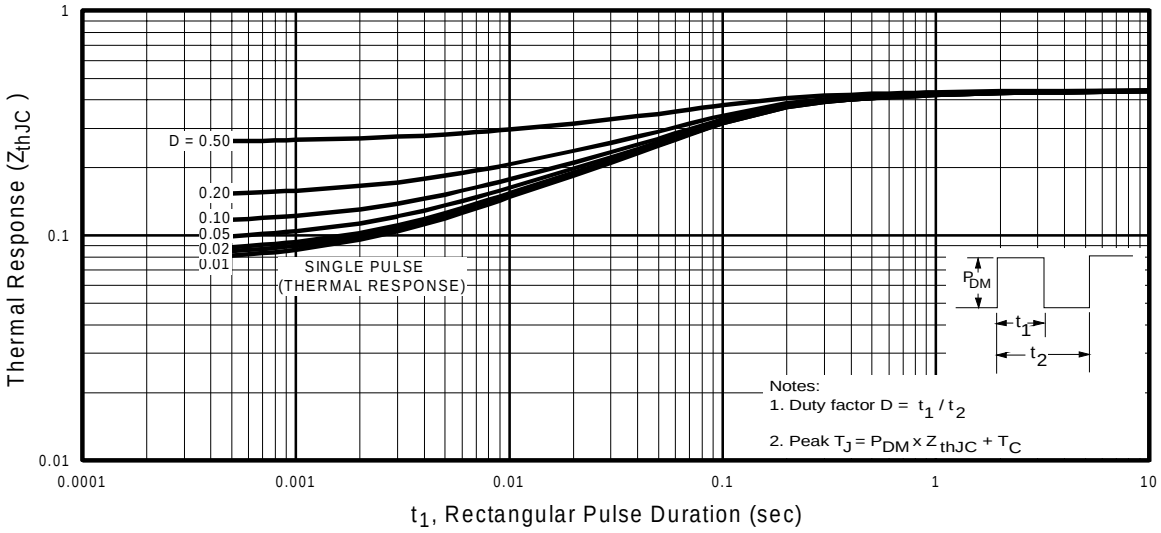


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

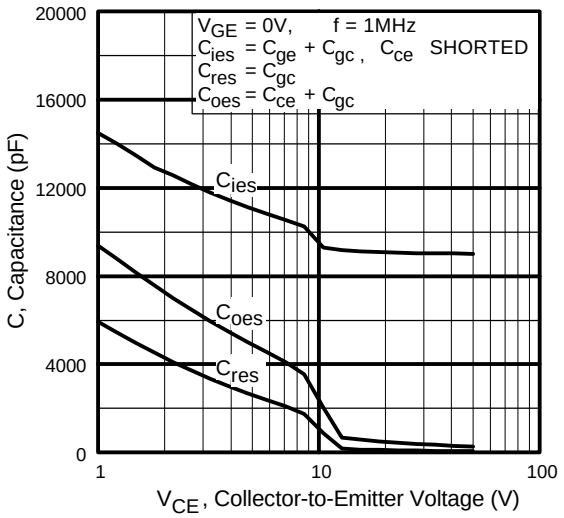


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

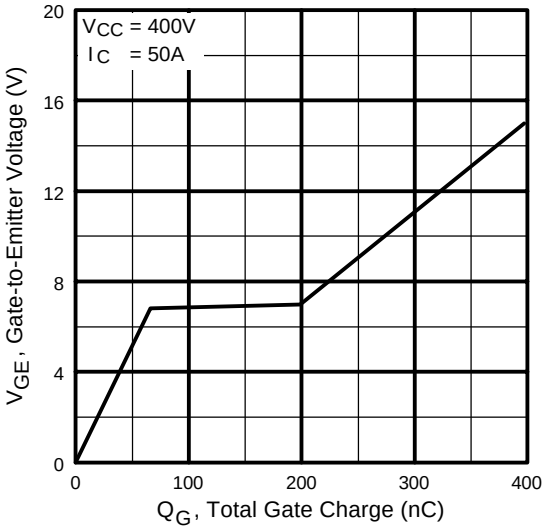


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

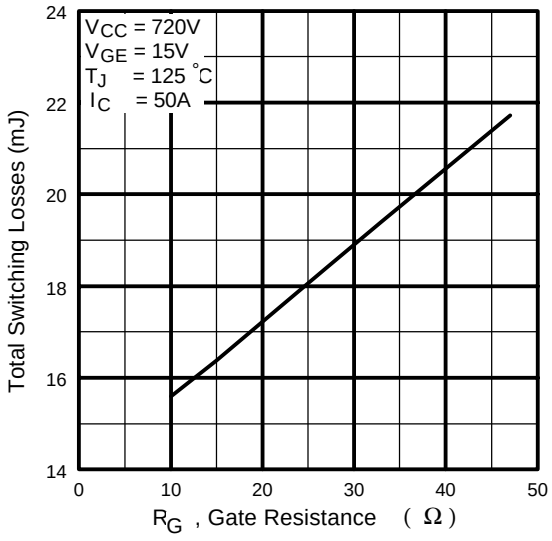


Fig. 9 - Typical Switching Losses vs. Gate Resistance

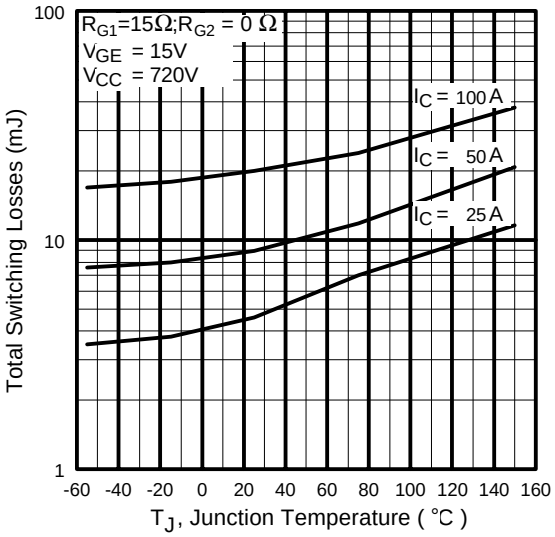


Fig. 10 - Typical Switching Losses vs. Junction Temperature

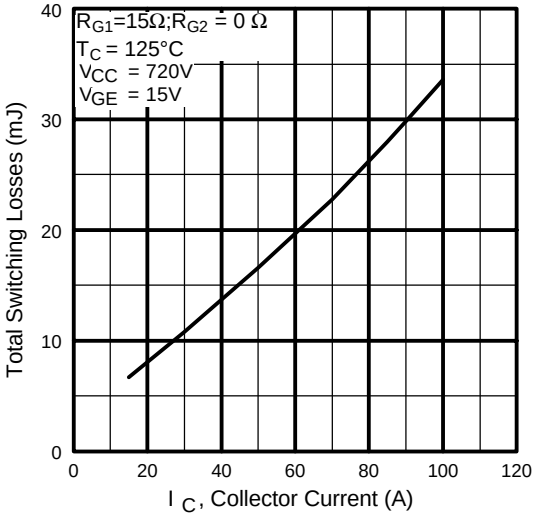


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

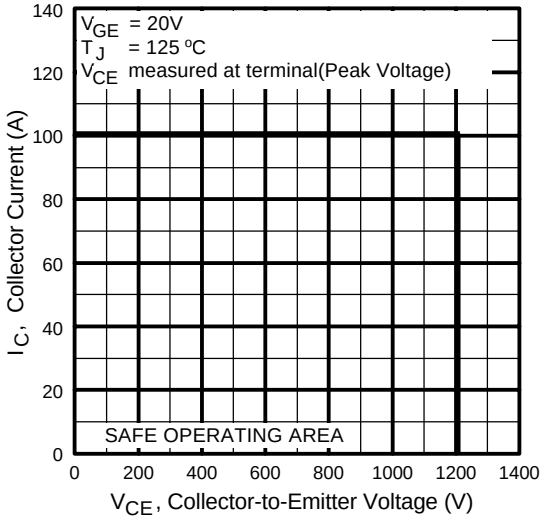


Fig. 12 - Reverse Bias SOA

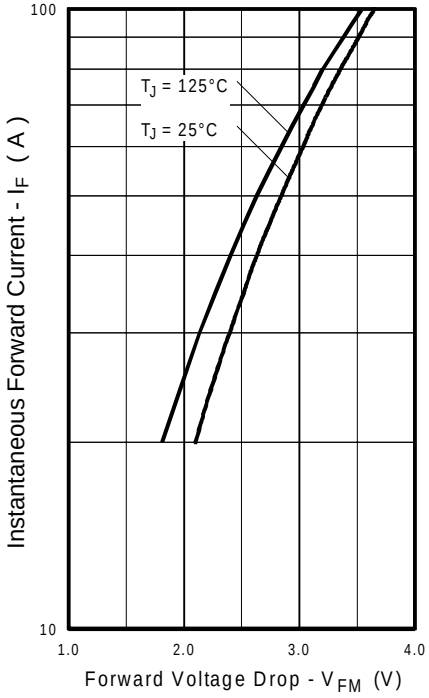


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

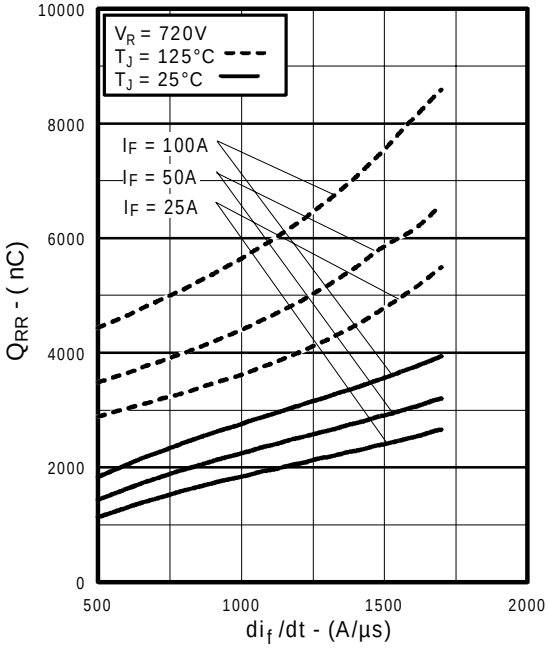


Fig. 14 - Typical Stored Charge vs. di_f/dt

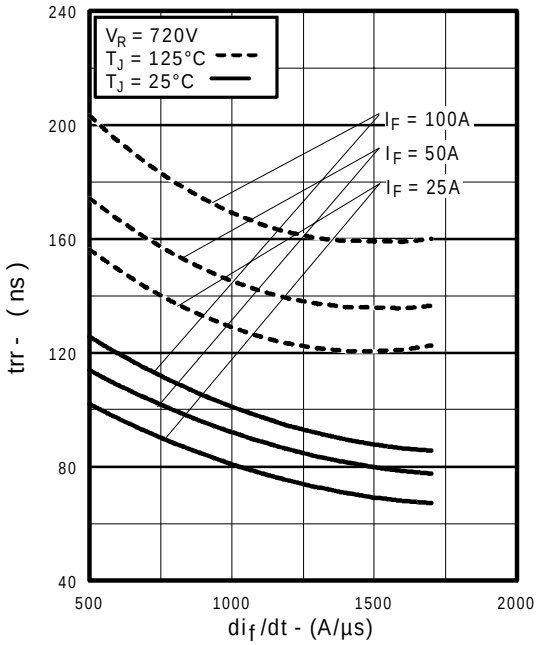


Fig. 15 - Typical Reverse Recovery vs. di_f/dt

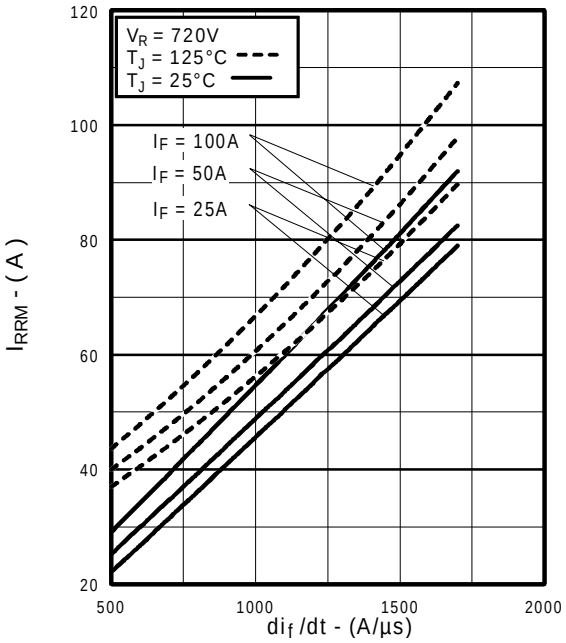


Fig. 16 - Typical Recovery Current vs. di_f/dt

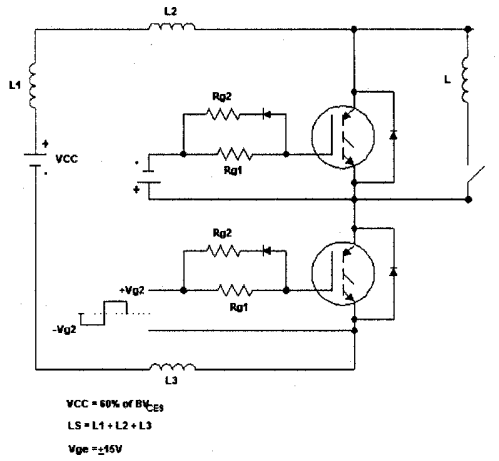


Fig. 17a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

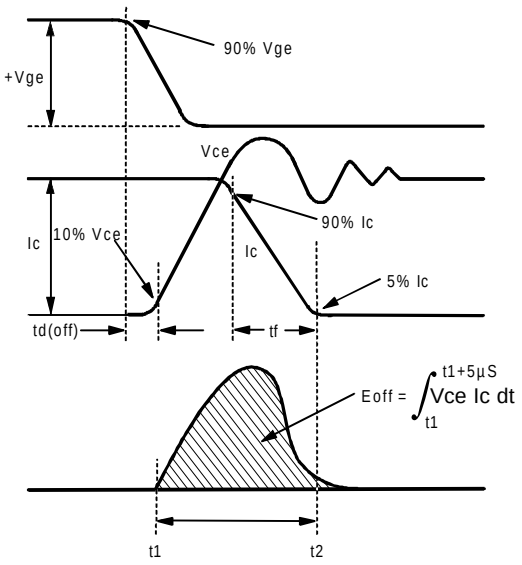


Fig. 17b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

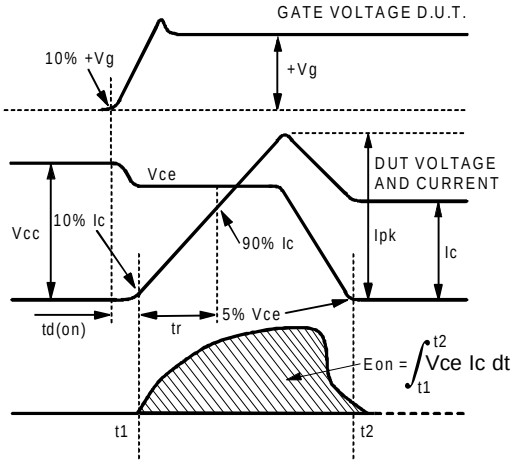


Fig. 17c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

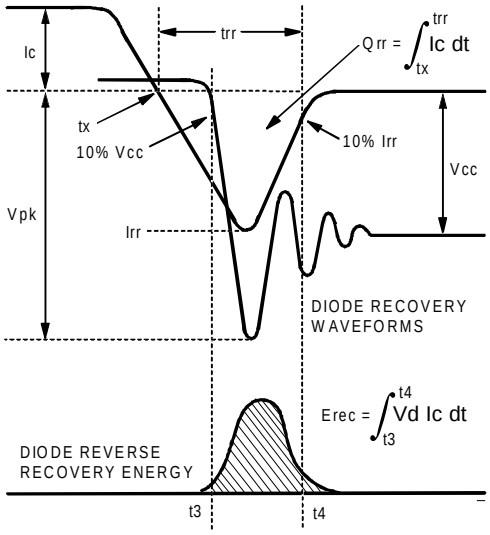


Fig. 17d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

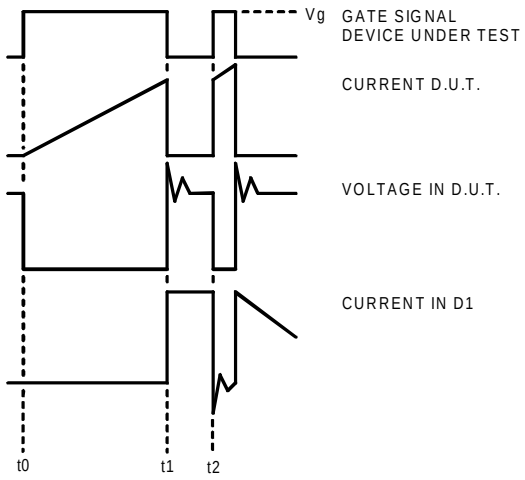


Figure 17e. Macro Waveforms for Figure 18a's Test Circuit

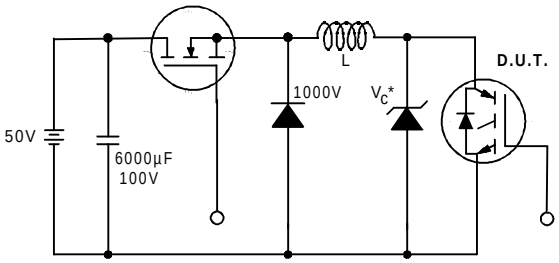


Figure 18. Clamped Inductive Load Test Circuit

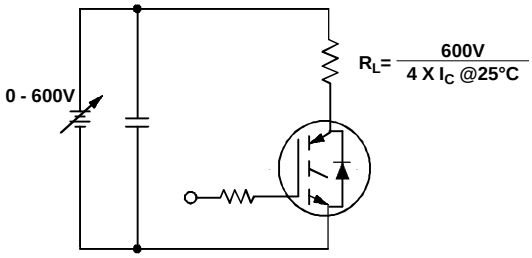


Figure 19. Pulsed Collector Current Test Circuit

Notes:

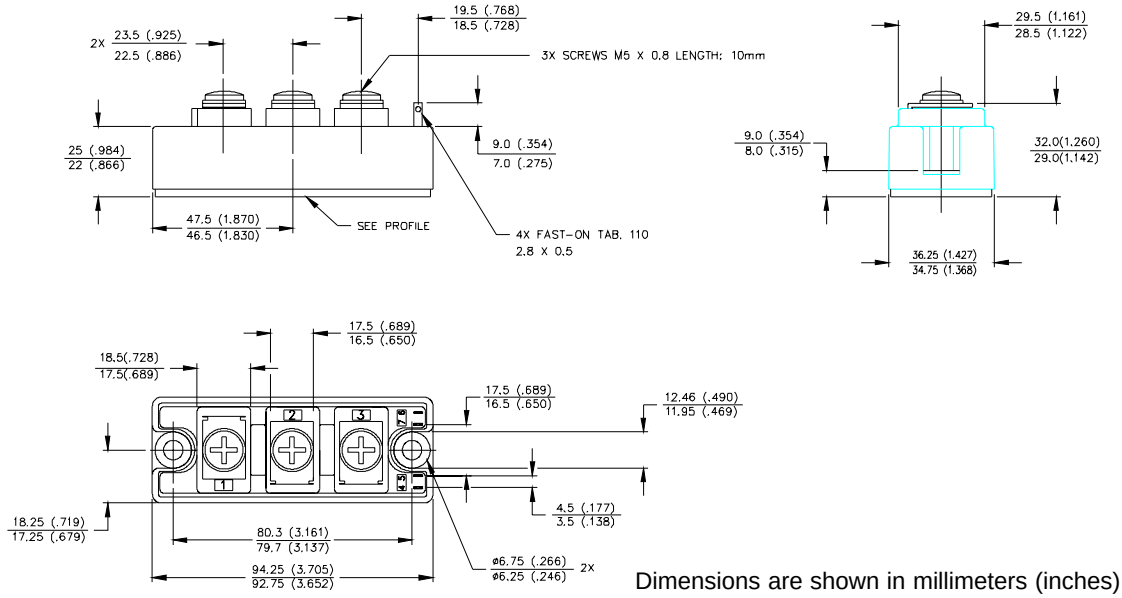
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 17

③ For screws M5x0.8

④ Pulse width 50µs; single shot.

Case Outline — INT-A-PAK



Dimensions are shown in millimeters (inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 10/00

International
IOR Rectifier

PD - 50062A

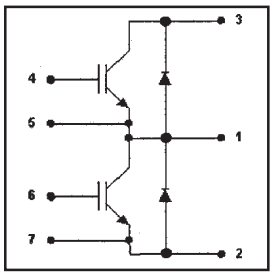
GA75TS120U

"HALF-BRIDGE" IGBT INT-A-PAK

Ultra-Fast™ Speed IGBT

Features

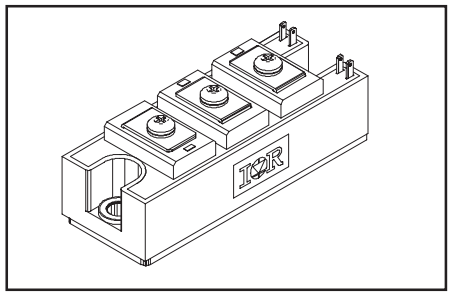
- Generation 4 IGBT technology
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL approved



V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.1V

@V_{GE} = 15V, I_C = 75A



Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	75	A
I_{CM}	Pulsed Collector Current ①	150	
I_{LM}	Peak Switching Current ②	150	
I_{FM}	Peak Diode Forward Current	150	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	390	W
P_D @ T_C = 85°C	Maximum Power Dissipation	200	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.32	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.35	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3 ③	—	3.0	
	Weight of Module	200	—	g

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	2.1	3.1		V_{GE} = 15V, I_C = 75A
		—	1.9	—		V_{GE} = 15V, I_C = 75A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = 6.0V, I_C = 750µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = 6.0V, I_C = 750µA
g_{fe}	Forward Transconductance ④	—	107	—	S	V_{CE} = 25V, I_C = 75A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	1.0	mA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	10		V_{GE} = 0V, V_{CE} = 1200V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	2.3	3.3	V	I_F = 75A, V_{GE} = 0V
		—	2.1	—		I_F = 75A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	250	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	570	854	nC	V_{CC} = 400V
Qge	Gate - Emitter Charge (turn-on)	—	96	144		I_C = 85A
Q_{gc}	Gate - Collector Charge (turn-on)	—	189	283		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	109	—	ns	R_{G1} = 15Ω, R_{G2} = 0Ω,
t_r	Rise Time	—	119	—		I_C = 75A
$t_{d(off)}$	Turn-Off Delay Time	—	392	—		V_{CC} = 720V
t_f	Fall Time	—	402	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	11	—	mJ	Inductor load
$E_{off(1)}$	Turn-Off Switching Energy	—	20	—		
$E_{ts(1)}$	Total Switching Energy	—	31	45		
C_{ies}	Input Capacitance	—	12815	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	570	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	110	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	174	—	ns	I_C = 75A
I_{rr}	Diode Peak ReverseCurrent	—	107	—	A	R_{G1} = 15Ω
Q_{rr}	Diode Recovery Charge	—	9367	—	nC	R_{G2} = 0Ω
$di_{(rec)}M_{/dt}$	Diode Peak Rate of Fall of Recovery During t_b	—	1491	—	A/µs	V_{CC} = 720V di/dt = 1300A/µs

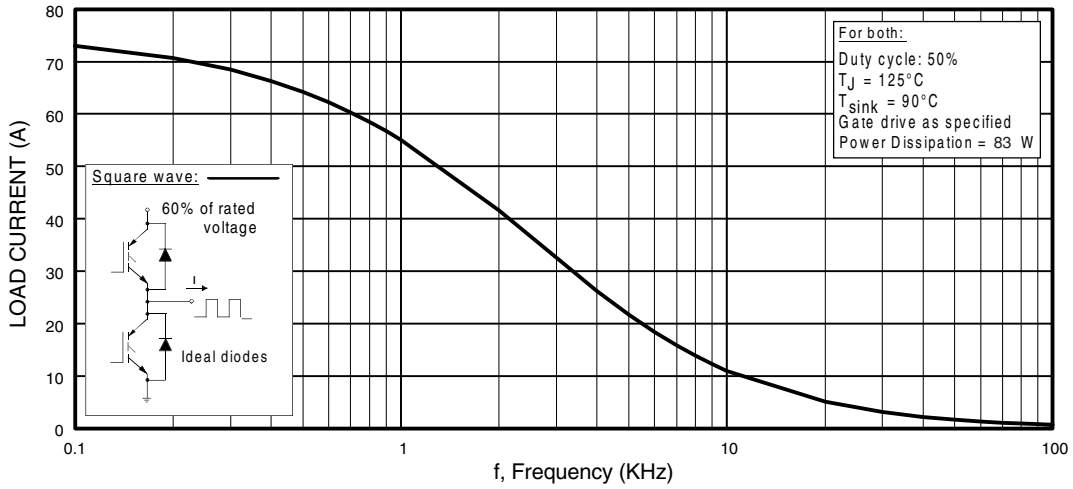


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

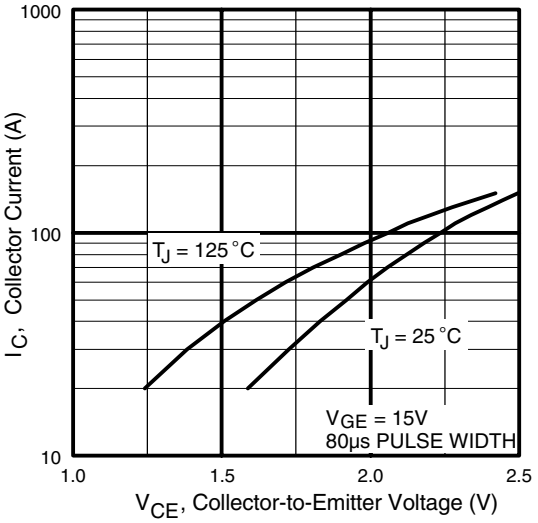


Fig. 2 - Typical Output Characteristics

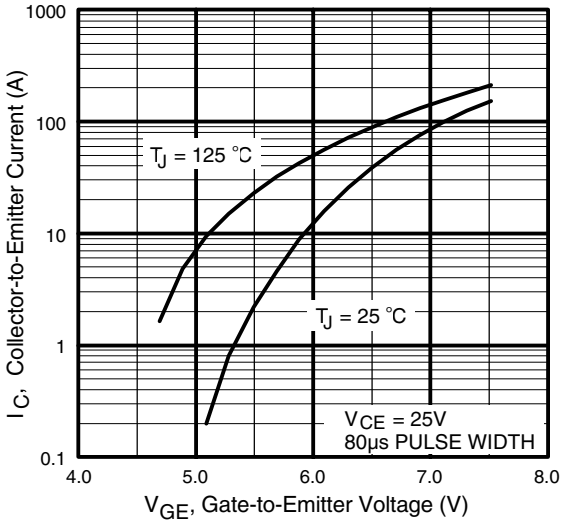


Fig. 3 - Typical Transfer Characteristics

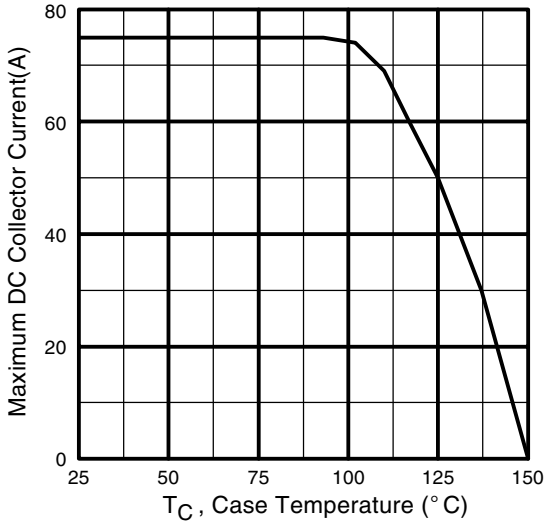


Fig. 4 - Maximum Collector Current vs. Case Temperature

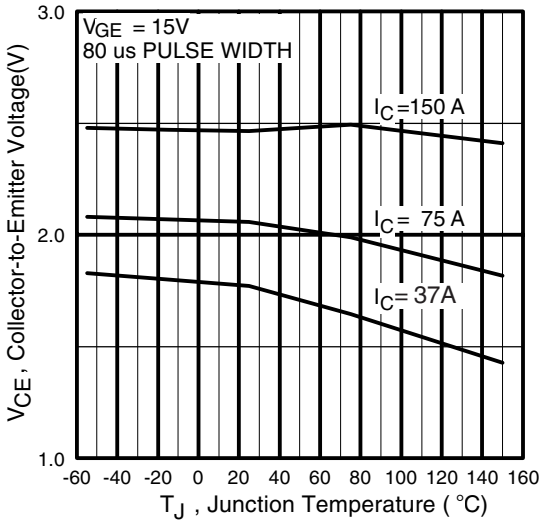


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

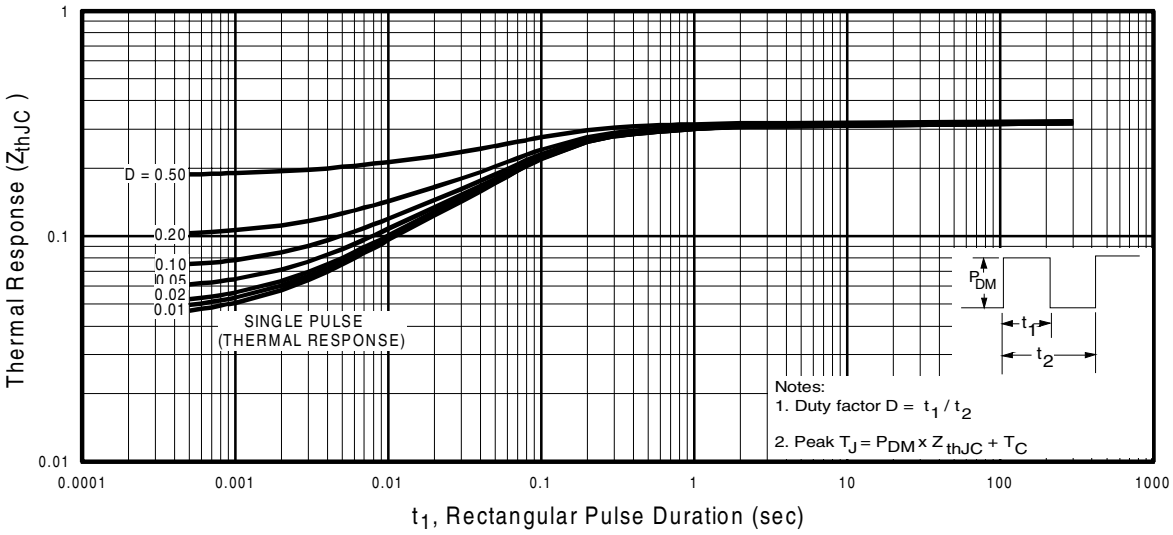


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

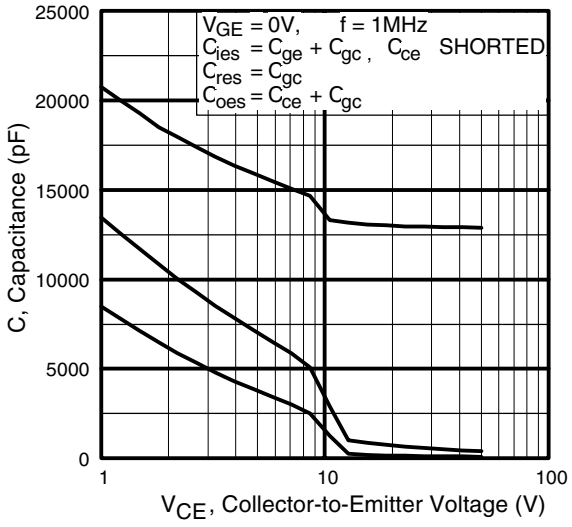


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

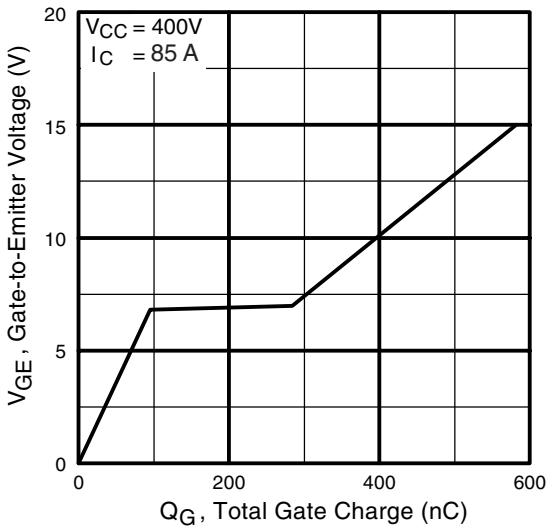


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

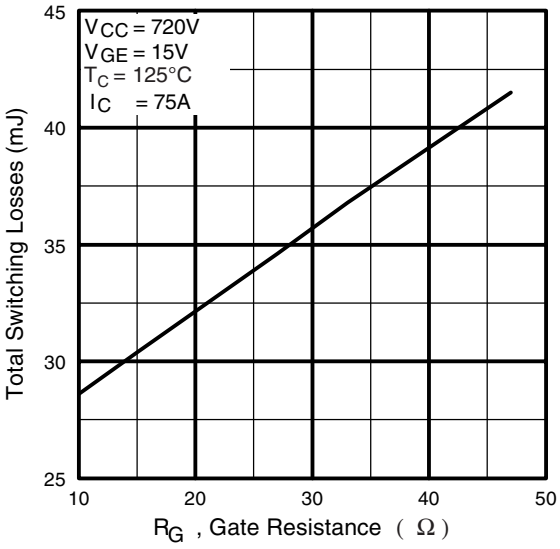


Fig. 9 - Typical Switching Losses vs. Gate Resistance

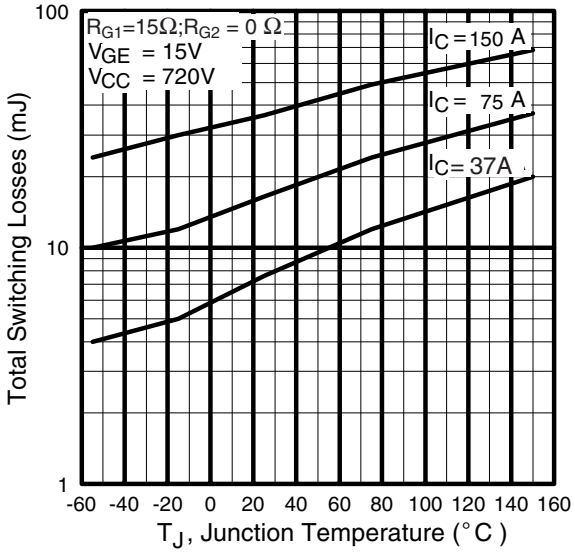


Fig. 10 - Typical Switching Losses vs. Junction Temperature

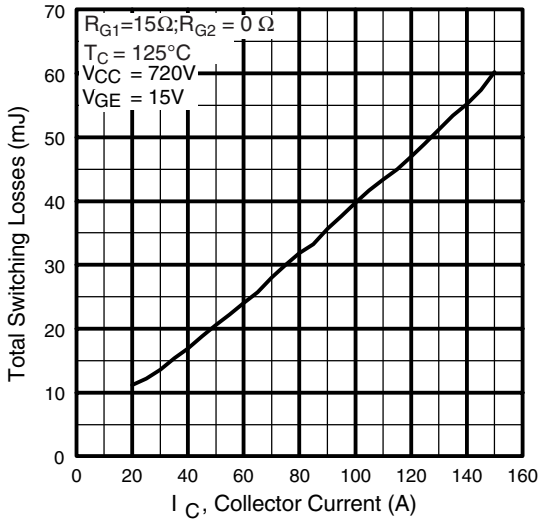


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

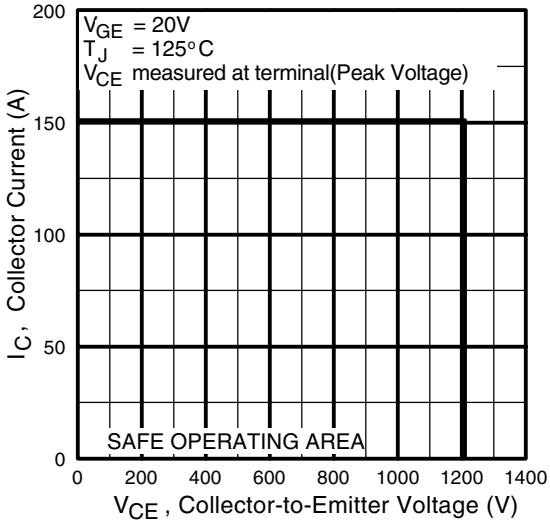


Fig. 12 - Reverse Bias SOA

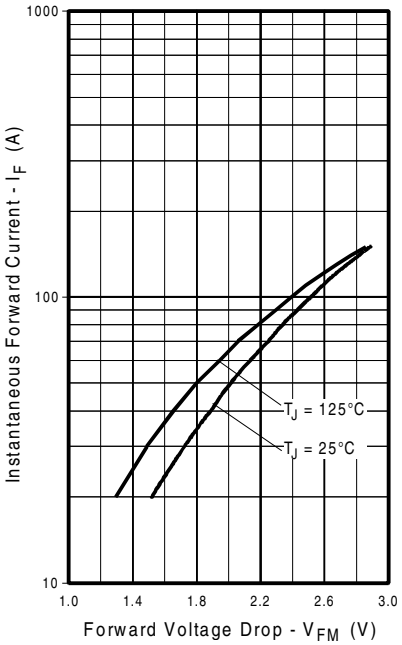


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

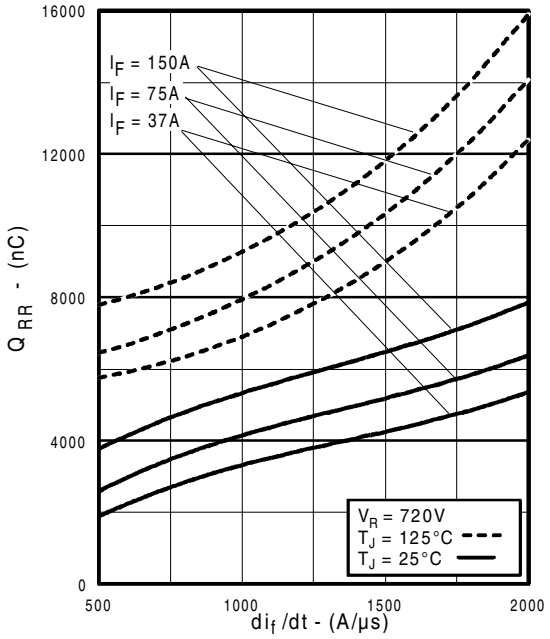


Fig. 14 - Typical Stored Charge vs. di_f/dt

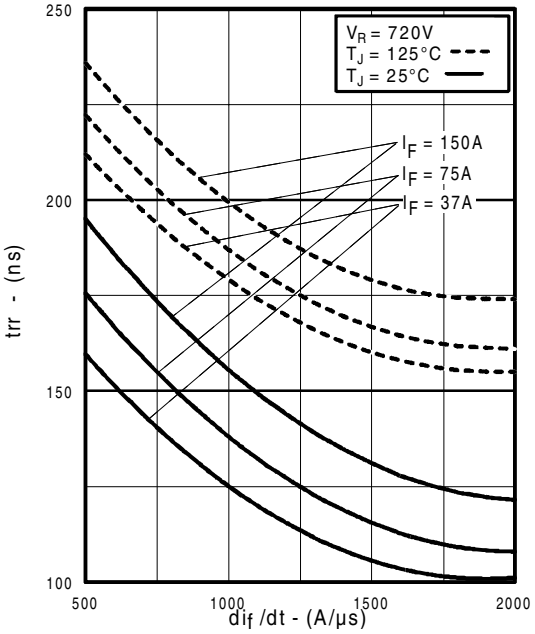


Fig. 15 - Typical Reverse Recovery vs. di_f/dt

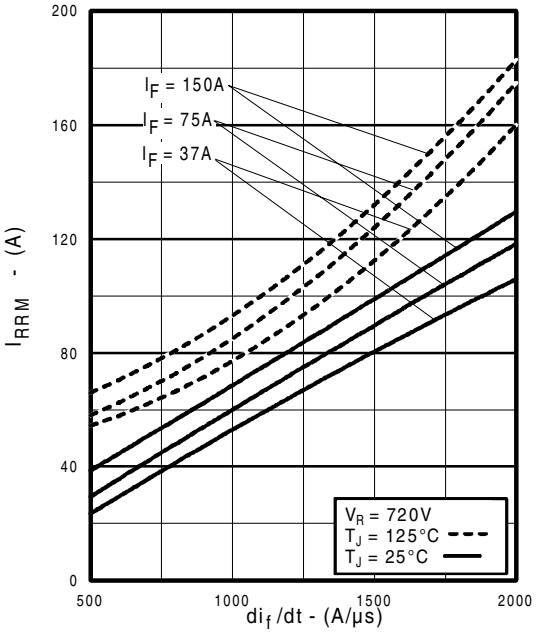


Fig. 16 - Typical Recovery Current vs. di_f/dt

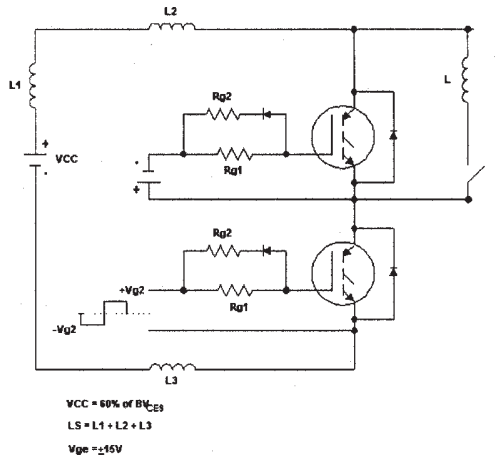


Fig. 17a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

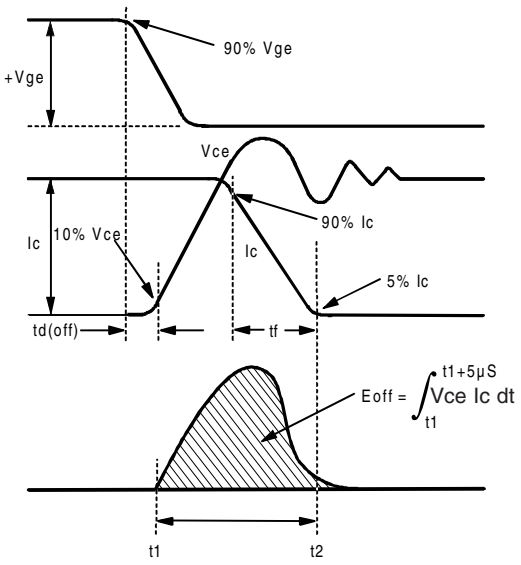


Fig. 17b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

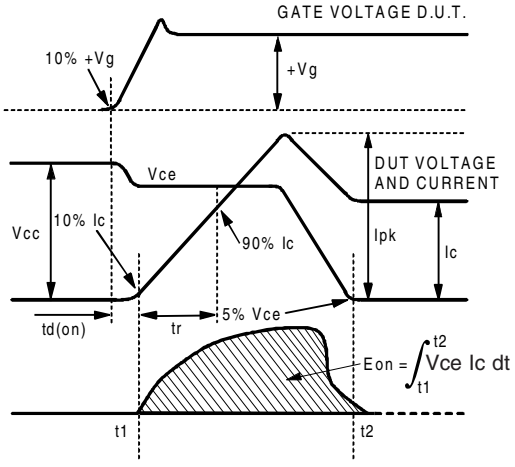


Fig. 17c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

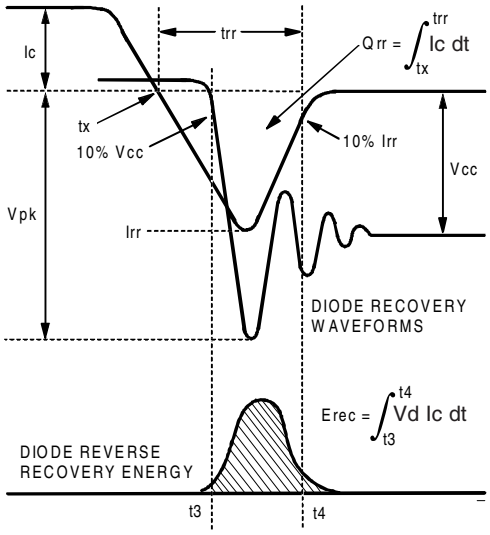


Fig. 17d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

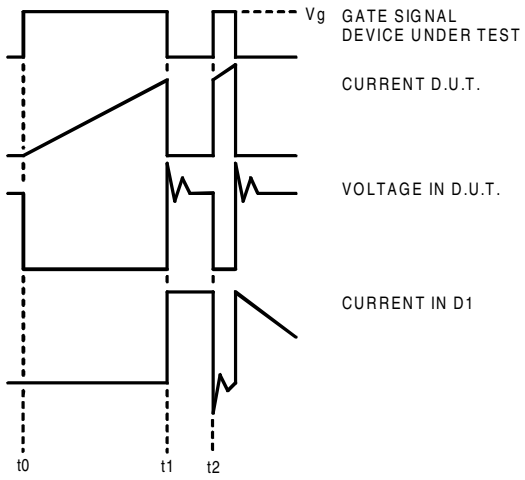


Figure 17e. Macro Waveforms for Figure 18a's Test Circuit

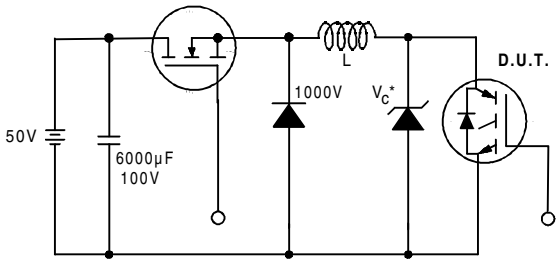


Figure 18. Clamped Inductive Load Test Circuit

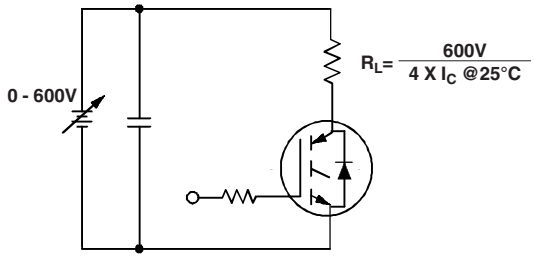


Figure 19. Pulsed Collector Current Test Circuit

Notes:

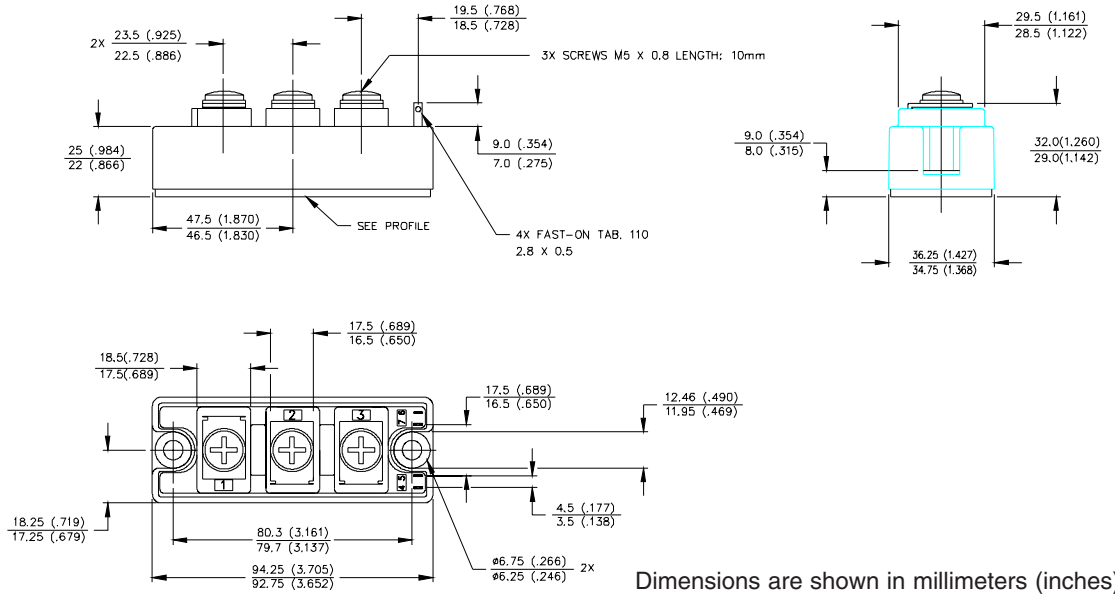
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 17

③ For screws M5x0.8

④ Pulse width 50µs; single shot.

Case Outline — INT-A-PAK



Dimensions are shown in millimeters (inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

International
IOR Rectifier

PD - 50060B

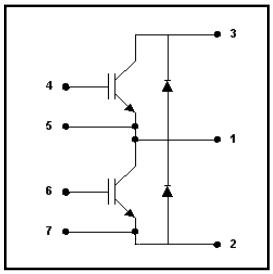
GA100TS120U

"HALF-BRIDGE" IGBT INT-A-PAK

Ultra-Fast™ Speed IGBT

Features

- Generation 4 IGBT technology
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL approved



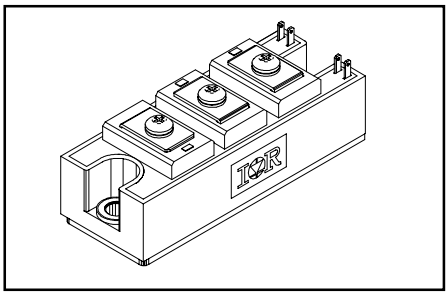
V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.4V

@V_{GE} = 15V, I_C = 100A

Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	100	A
I_{CM}	Pulsed Collector Current ①	200	
I_{LM}	Peak Switching Current ②	200	
I_{FM}	Peak Diode Forward Current	200	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	520	W
P_D @ T_C = 85°C	Maximum Power Dissipation	270	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.24	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.35	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3 ③	—	3.0	
	Weight of Module	200	—	g

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	2.4	2.9		V_{GE} = 15V, I_C = 100A
		—	2.2	—		V_{GE} = 15V, I_C = 100A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		I_C = 1.25mA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.25mA
g_{fe}	Forward Transconductance ④	—	136	—	S	V_{CE} = 25V, I_C = 100A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	1.0	mA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	10		V_{GE} = 0V, V_{CE} = 1200V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	3.3	4.0	V	I_F = 100A, V_{GE} = 0V
		—	3.2	—		I_F = 100A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	250	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	830	1245	nC	V_{CC} = 400V
Qge	Gate - Emitter Charge (turn-on)	—	140	210		I_C = 124A
Q_{gc}	Gate - Collector Charge (turn-on)	—	275	412		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	172	—	ns	R_{G1} = 15Ω, R_{G2} = 0Ω,
t_r	Rise Time	—	141	—		I_C = 100A
$t_{d(off)}$	Turn-Off Delay Time	—	435	—		V_{CC} = 720V
t_f	Fall Time	—	343	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	14	—	mJ	
$E_{off\ (1)}$	Turn-Off Switching Energy	—	21	—		
$E_{ts\ (1)}$	Total Switching Energy	—	35	52		
C_{ies}	Input Capacitance	—	18672	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	830	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	161	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	149	—	ns	I_C = 100A
I_{rr}	Diode Peak ReverseCurrent	—	104	—	A	R_{G1} = 15Ω
Q_{rr}	Diode Recovery Charge	—	7664	—	µC	R_{G2} = 0Ω
$di_{(rec)}M_{/dt}$	Diode Peak Rate of Fall of Recovery During t_b	—	1916	—	A/µs	V_{CC} = 720V di/dt»1300A/µs

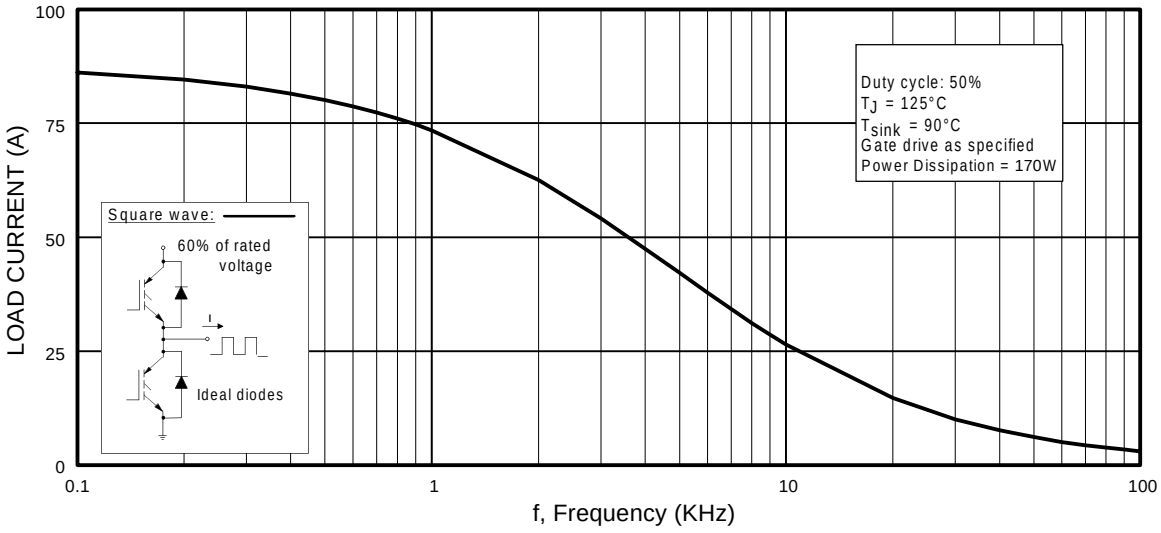


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

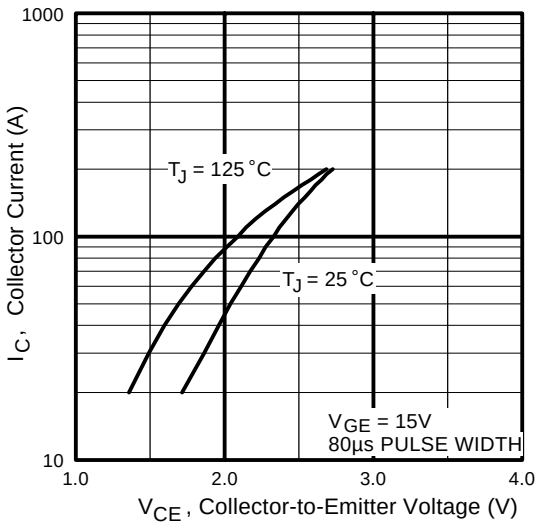


Fig. 2 - Typical Output Characteristics

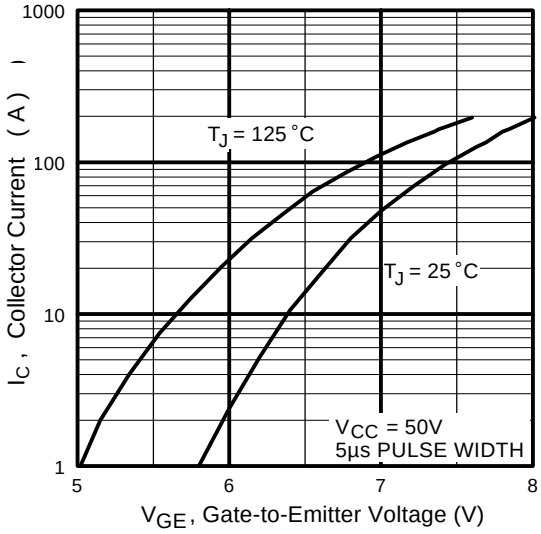


Fig. 3 - Typical Transfer Characteristics

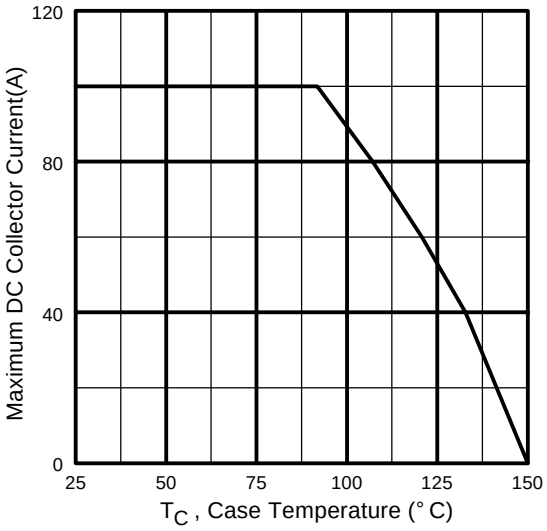


Fig. 4 - Maximum Collector Current vs. Case Temperature

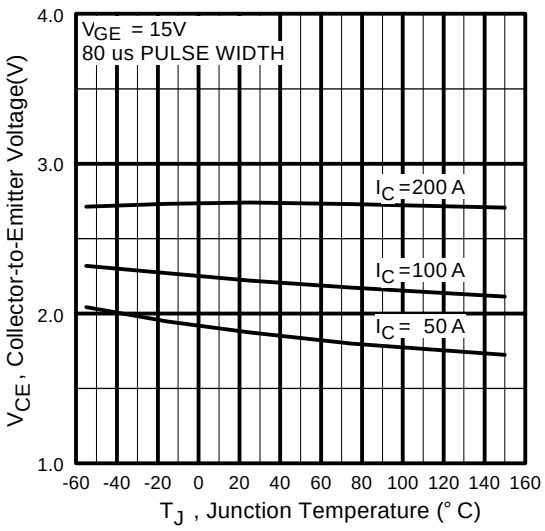


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

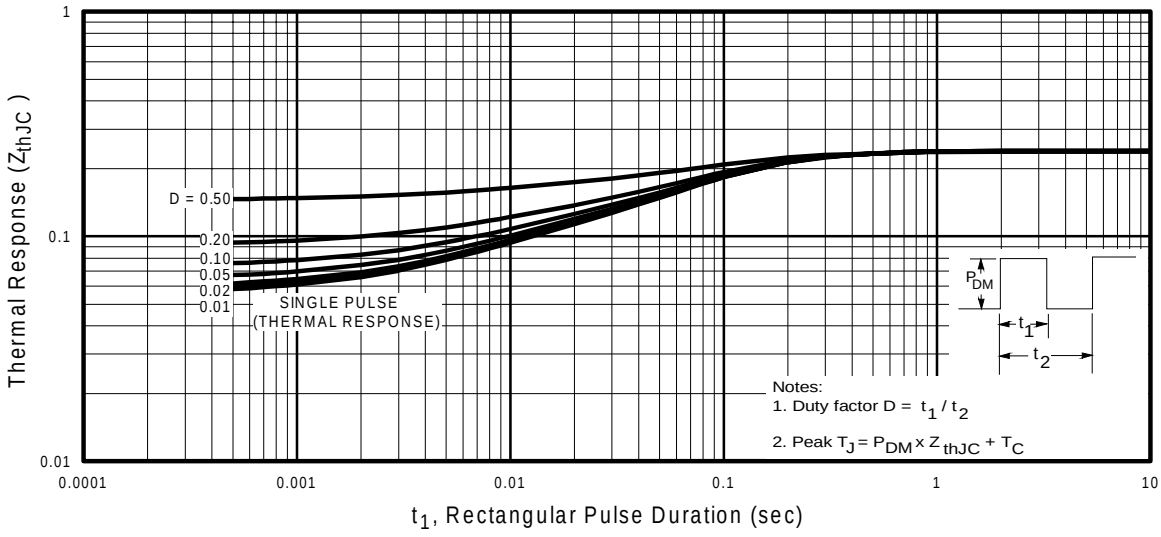


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

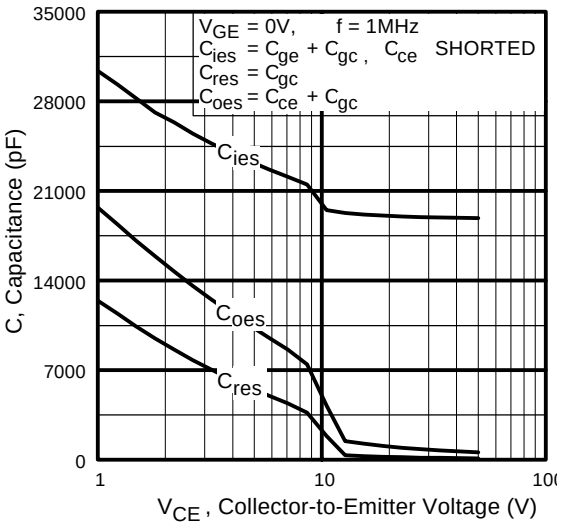


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

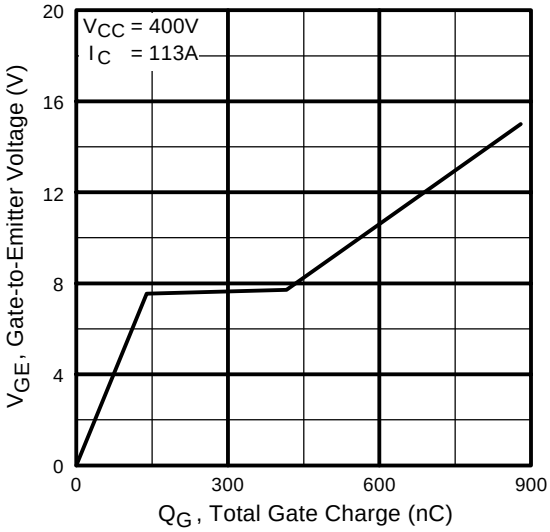


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

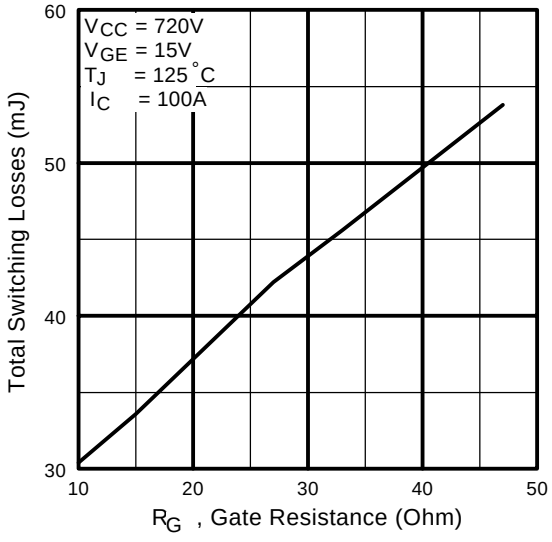


Fig. 9 - Typical Switching Losses vs. Gate Resistance

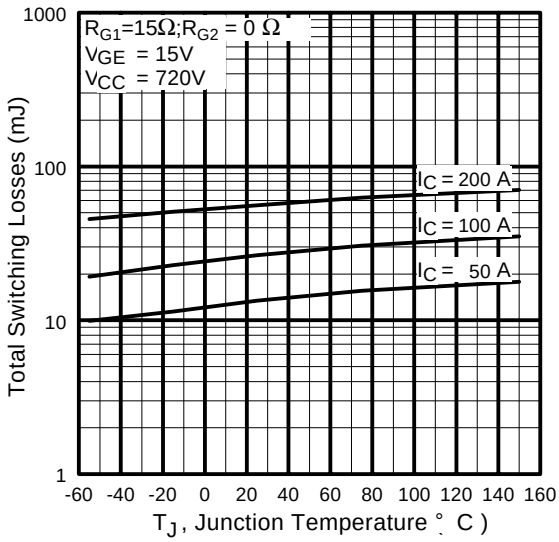


Fig. 10 - Typical Switching Losses vs. Junction Temperature

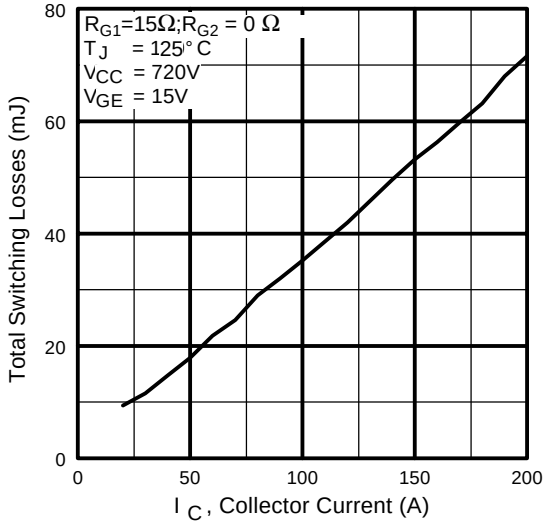


Fig. 11 - Typical Switching Losses vs. Collector Current

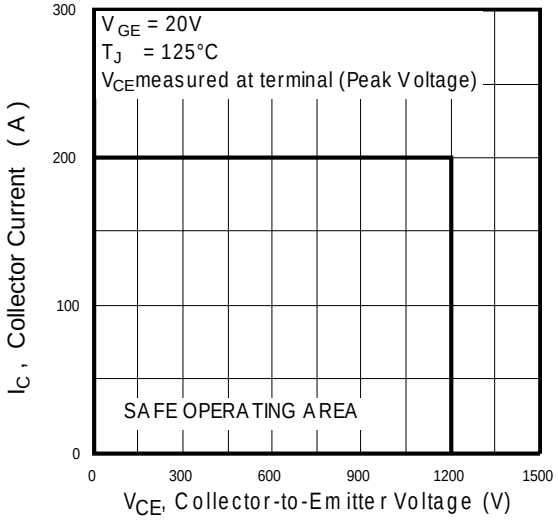


Fig. 12 - Reverse Bias SOA

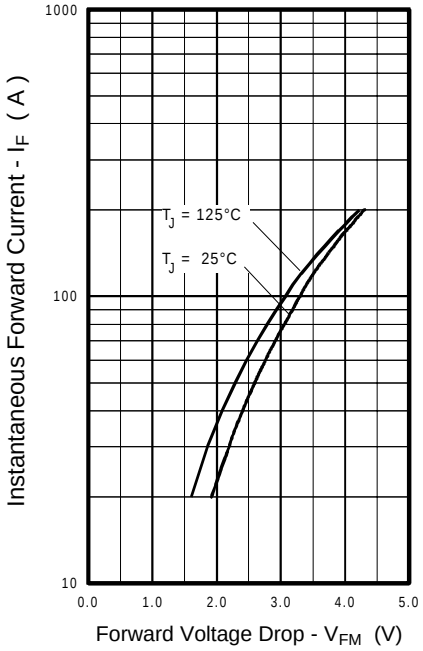


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

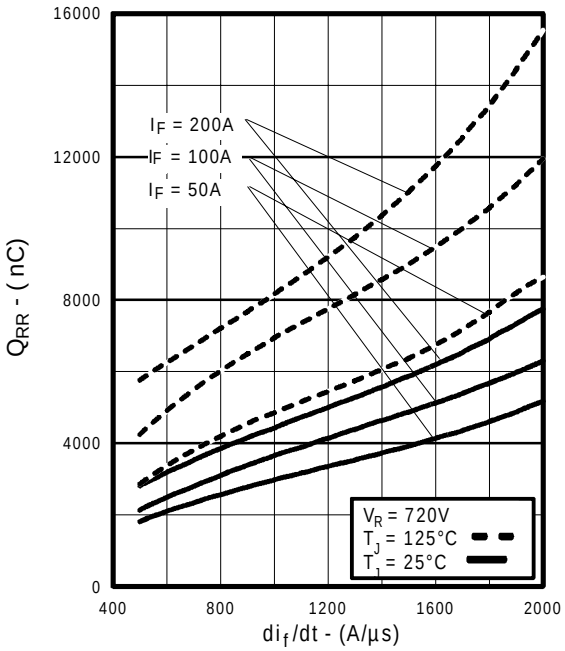


Fig. 14 - Typical Stored Charge vs. di_f/dt

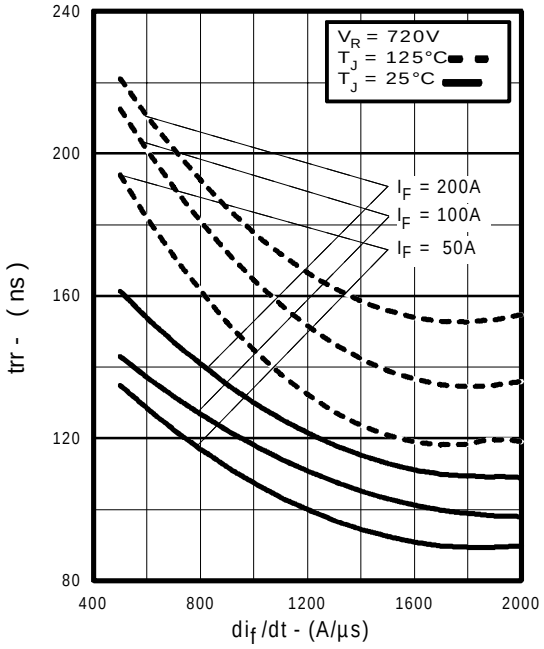


Fig. 15 - Typical Reverse Recovery vs. di_f/dt

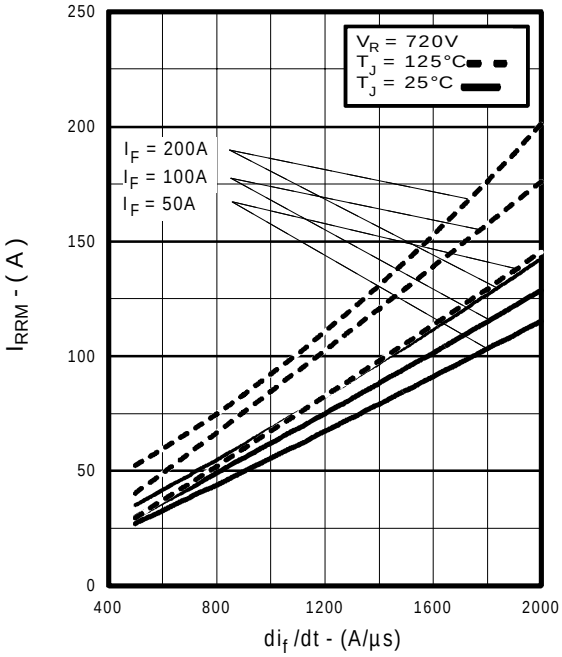


Fig. 16 - Typical Recovery Current vs. di_f/dt

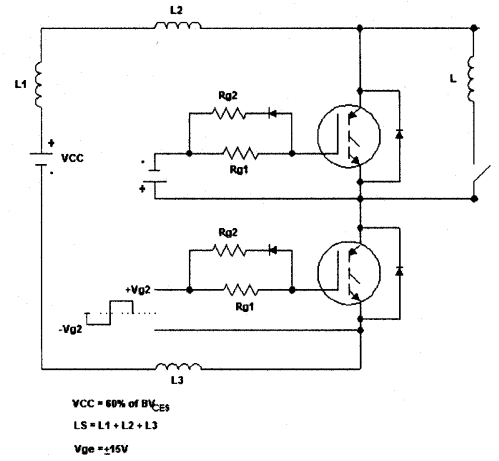


Fig. 17a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

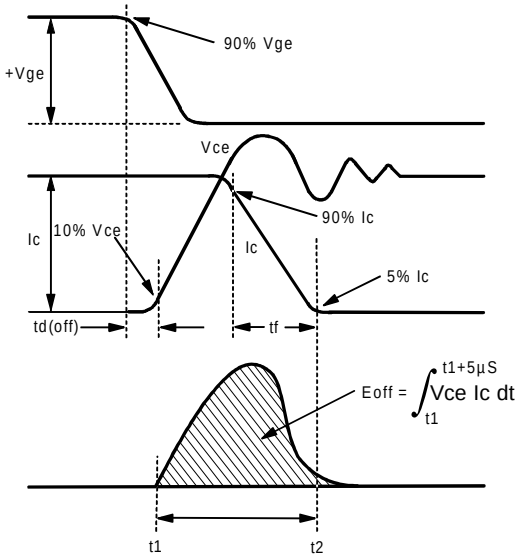


Fig. 17b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

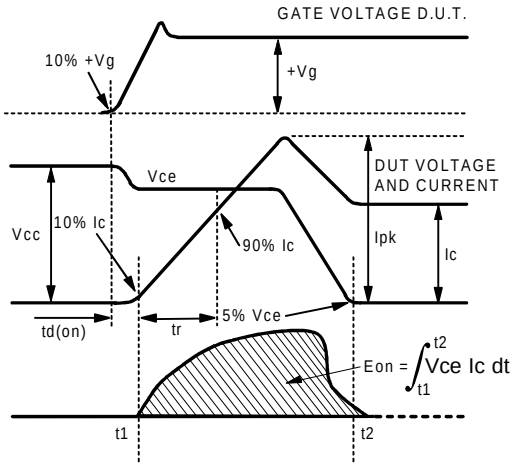


Fig. 17c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

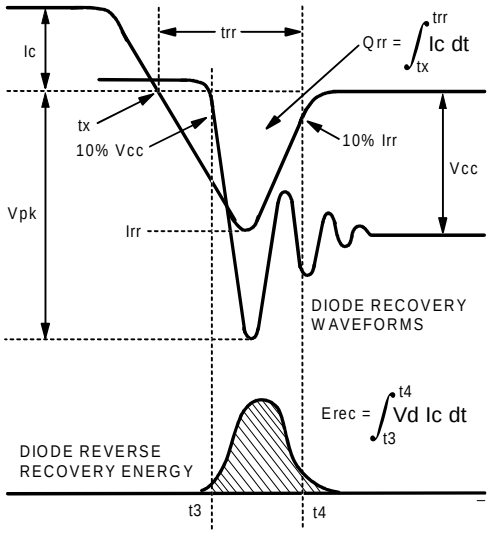


Fig. 17d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

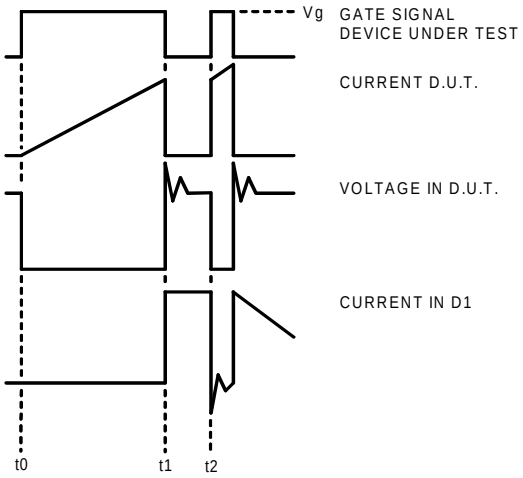


Figure 17e. Macro Waveforms for Figure 18a's Test Circuit

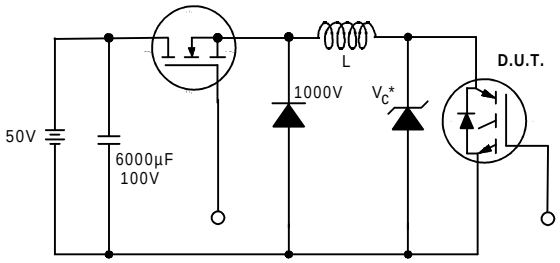


Figure 18. Clamped Inductive Load Test Circuit

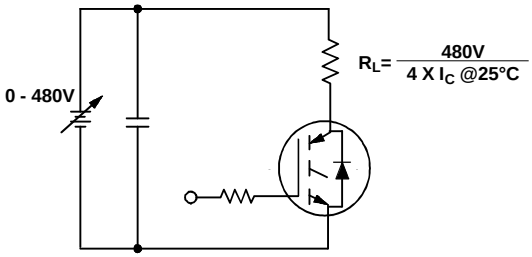


Figure 19. Pulsed Collector Current Test Circuit

Notes:

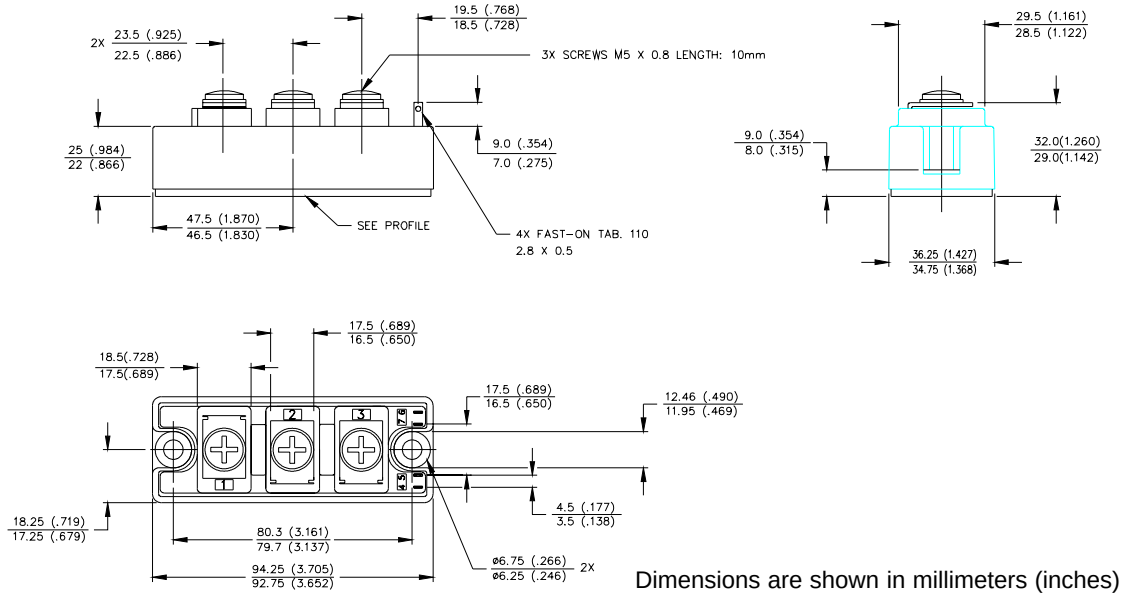
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 17

③ For screws M5x0.8

④ Pulse width 50µs; single shot.

Case Outline — INT-A-PAK



Dimensions are shown in millimeters (inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

International
IOR Rectifier

PD - 50053B

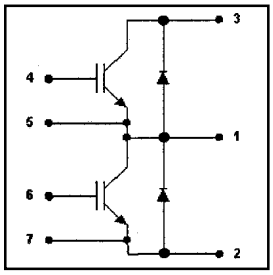
GA125TS120U

"HALF-BRIDGE" IGBT INT-A-PAK

Ultra-Fast™ Speed IGBT

Features

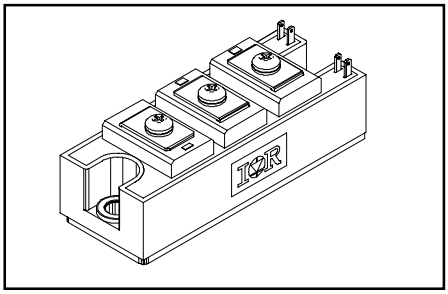
- Generation 4 IGBT technology
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL approved



V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.2V

@V_{GE} = 15V, I_C = 125A



Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	125	A
I_{CM}	Pulsed Collector Current ①	250	
I_{LM}	Peak Switching Current ②	250	
I_{FM}	Peak Diode Forward Current	250	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	625	W
P_D @ T_C = 85°C	Maximum Power Dissipation	325	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.20	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.35	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3 ③	—	3.0	
	Weight of Module	200	—	g

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	2.2	3.0		V_{GE} = 15V, I_C = 125A
		—	2.1	—		V_{GE} = 15V, I_C = 125A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = 6.0V, I_C = 1.5mA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = 6.0V, I_C = 1.5mA
g_{fe}	Forward Transconductance ④	—	170	—	S	V_{CE} = 25V, I_C = 125A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	1.0	mA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	10		V_{GE} = 0V, V_{CE} = 1200V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	2.7	4.2	V	I_F = 125A, V_{GE} = 0V
		—	2.6	—		I_F = 125A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	250	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	989	1484	nC	V_{CC} = 400V
Qge	Gate - Emitter Charge (turn-on)	—	167	250		I_C = 148A
Q_{gc}	Gate - Collector Charge (turn-on)	—	328	492		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	186	—	ns	R_{G1} = 15Ω, R_{G2} = 0Ω,
t_r	Rise Time	—	159	—		I_C = 125A
$t_{d(off)}$	Turn-Off Delay Time	—	459	—		V_{CC} = 720V
t_f	Fall Time	—	404	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	19	—	mJ	Inductor load
$E_{off\ (1)}$	Turn-Off Switching Energy	—	31	—		
$E_{ts\ (1)}$	Total Switching Energy	—	49	75		
C_{ies}	Input Capacitance	—	22258	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	989	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	192	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	181	—	ns	I_C = 125A
I_{rr}	Diode Peak ReverseCurrent	—	126	—	A	R_{G1} = 15Ω
Q_{rr}	Diode Recovery Charge	—	11360	—	nC	R_{G2} = 0Ω
$di_{(rec)}M/dt$	Diode Peak Rate of Fall of Recovery	—	1875	—	A/µs	V_{CC} = 720V
	During t_b					di/dt =1448A/µs

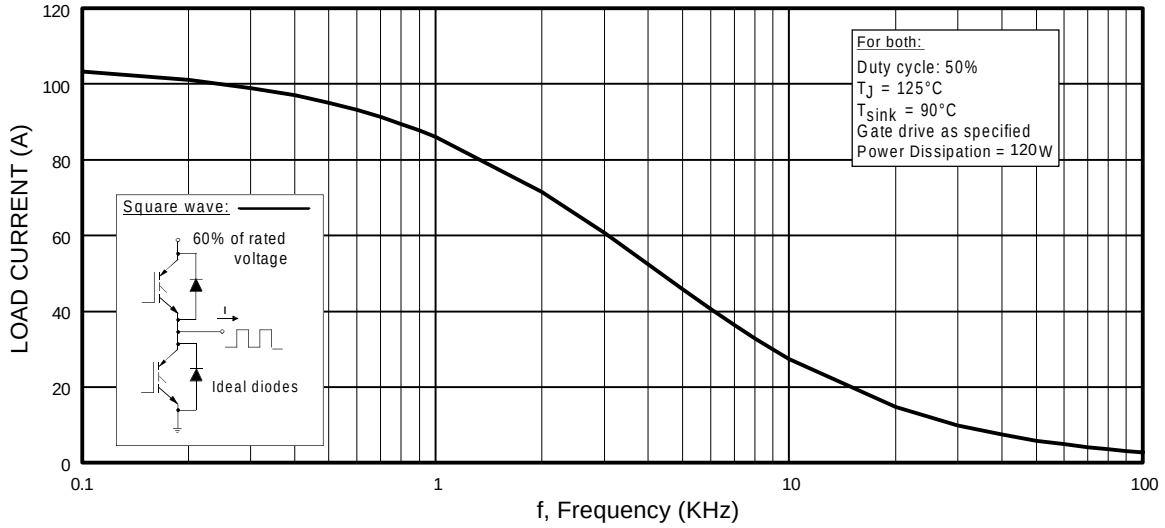


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

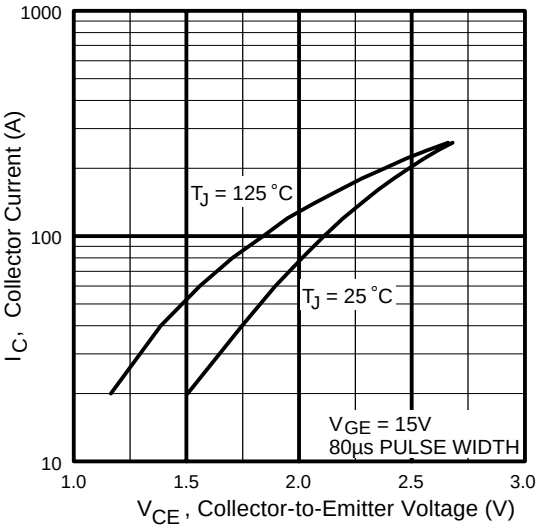


Fig. 2 - Typical Output Characteristics

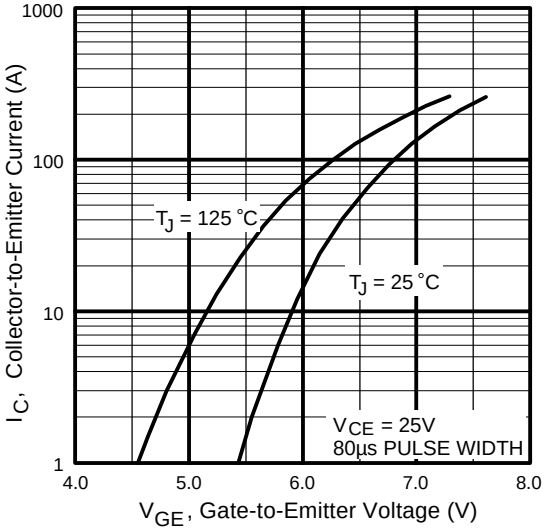


Fig. 3 - Typical Transfer Characteristics

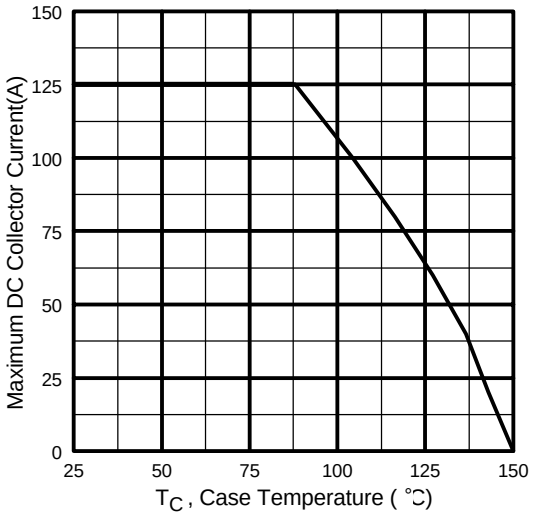


Fig. 4 - Maximum Collector Current vs. Case Temperature

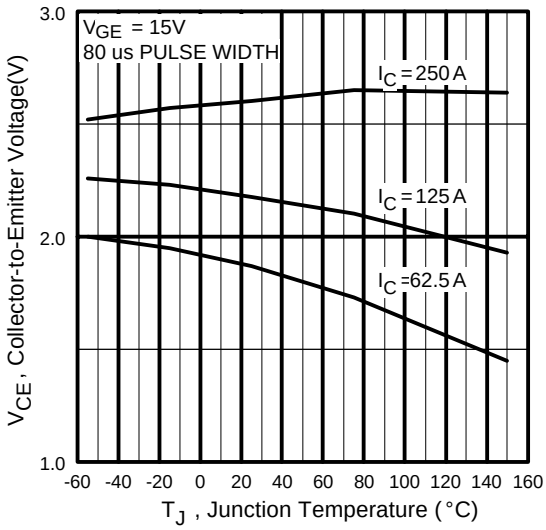


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

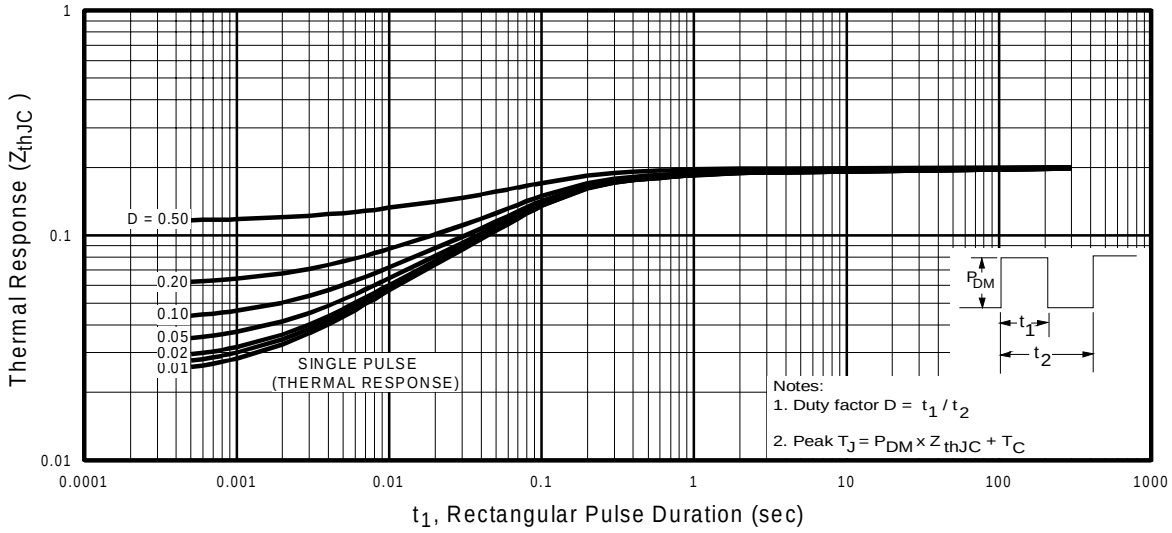


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

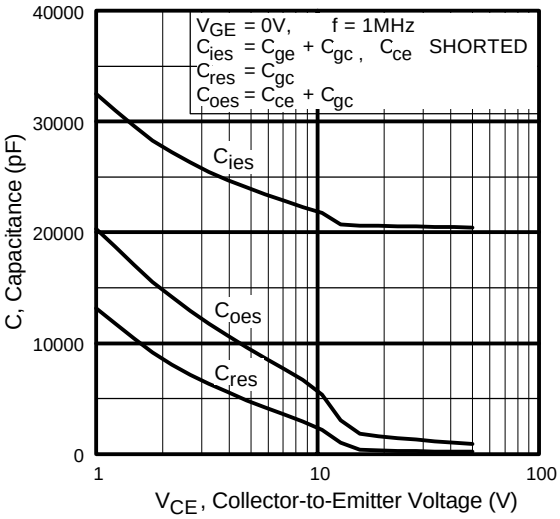


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

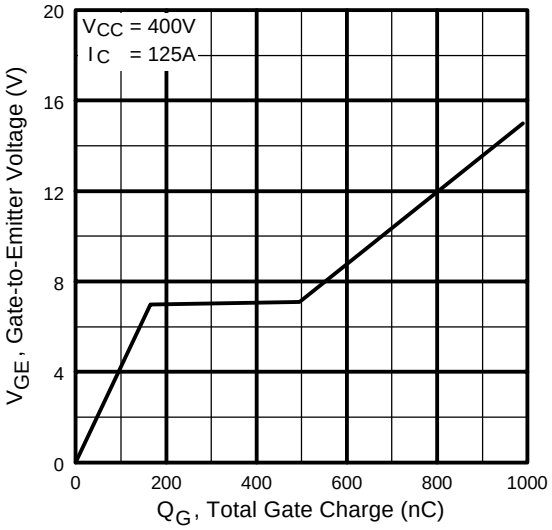


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

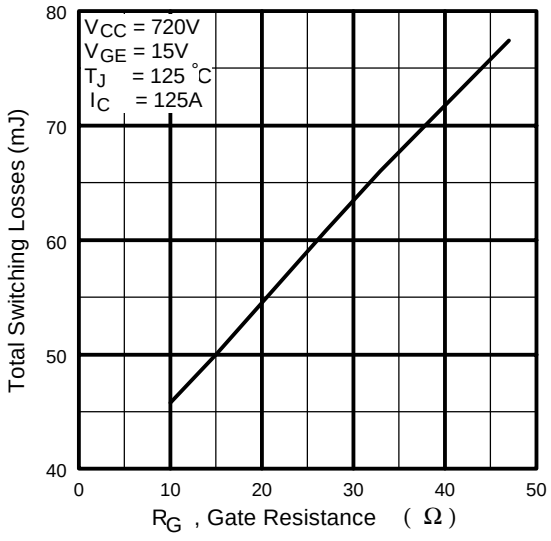


Fig. 9 - Typical Switching Losses vs. Gate Resistance

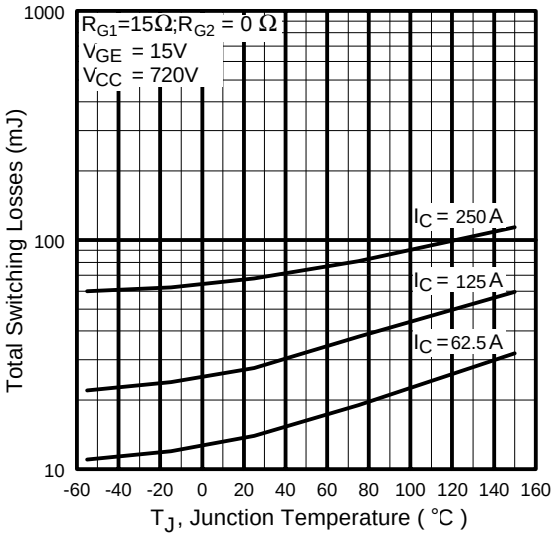


Fig. 10 - Typical Switching Losses vs. Junction Temperature

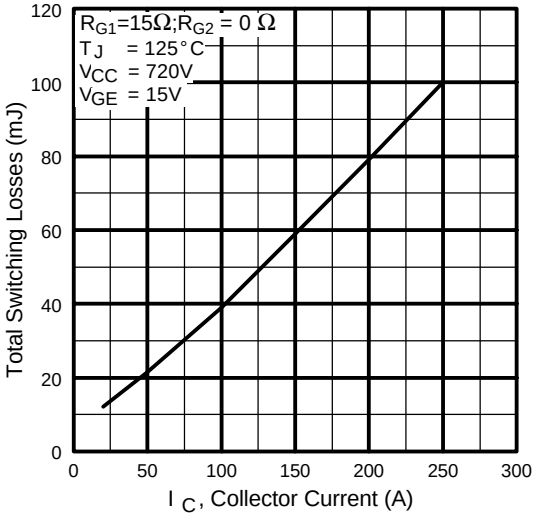


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

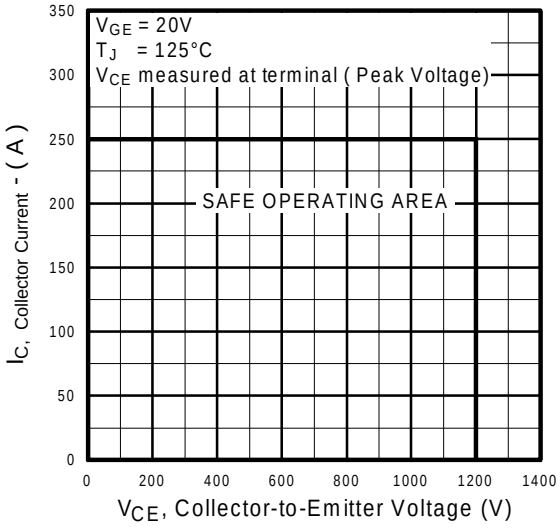


Fig. 12 - Reverse Bias SOA

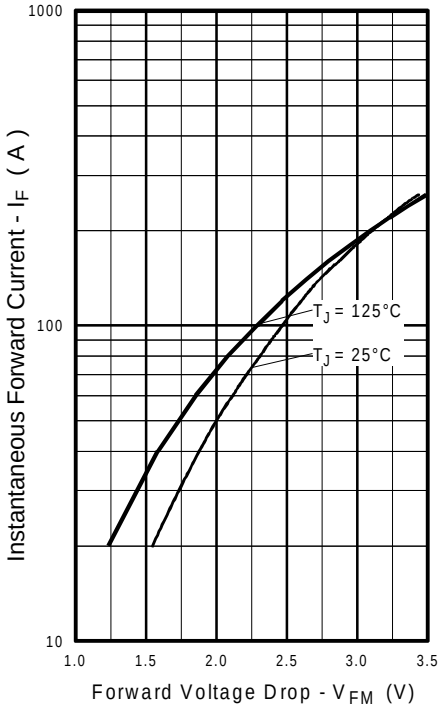


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

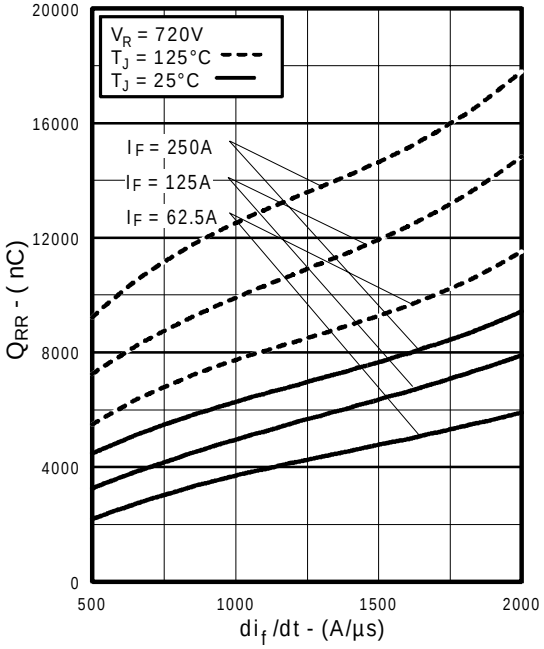


Fig. 14 - Typical Stored Charge vs. di_f/dt

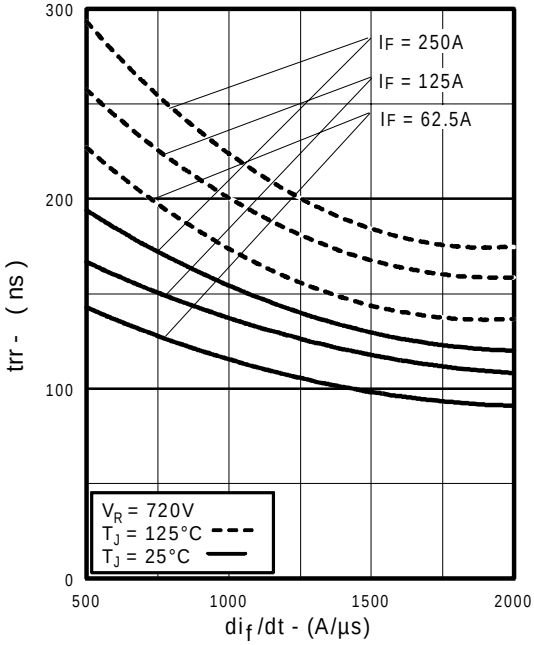


Fig. 15 - Typical Reverse Recovery vs. di_f/dt

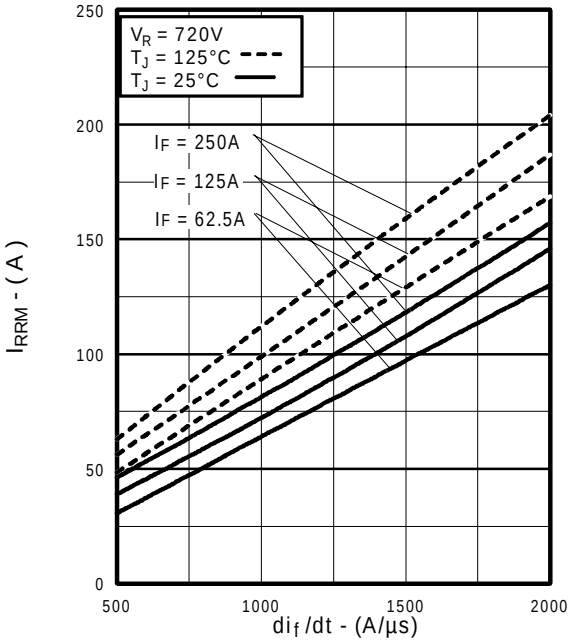


Fig. 16 - Typical Recovery Current vs. di_f/dt

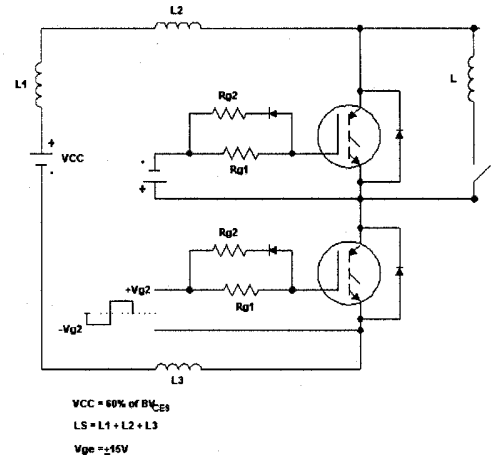


Fig. 17a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

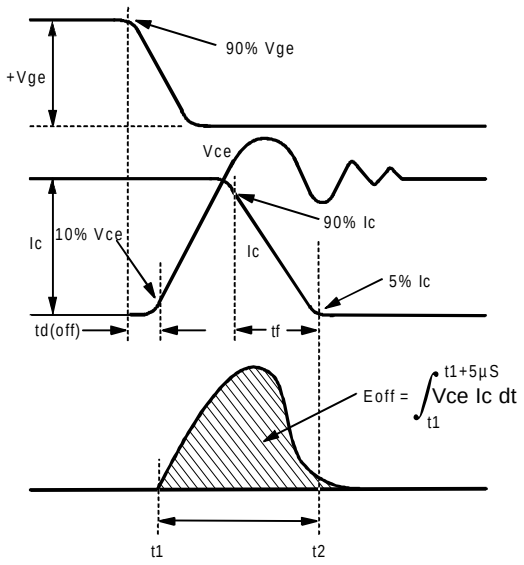


Fig. 17b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

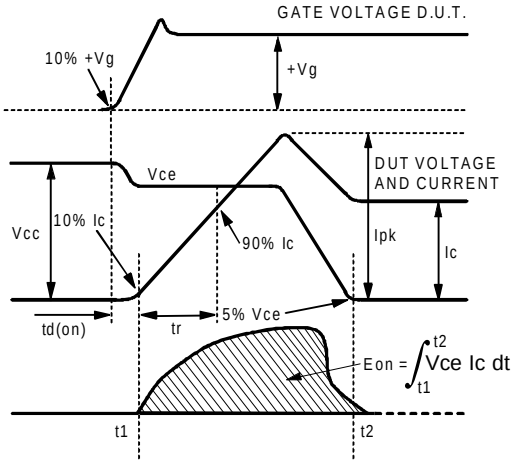


Fig. 17c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

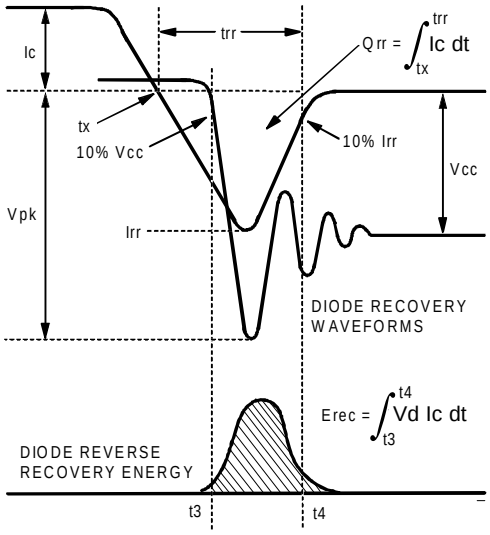


Fig. 17d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

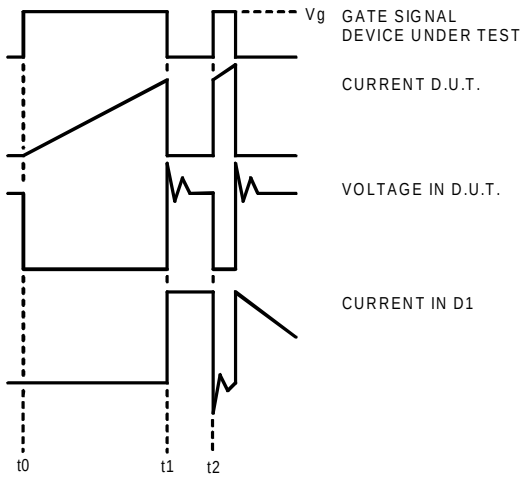


Figure 17e. Macro Waveforms for Figure 18a's Test Circuit

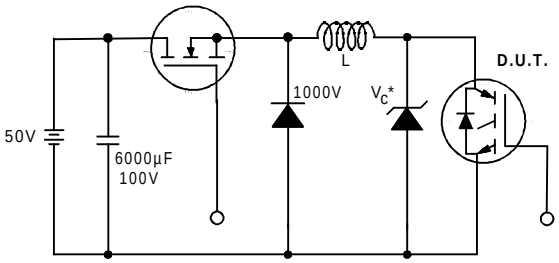


Figure 18. Clamped Inductive Load Test Circuit

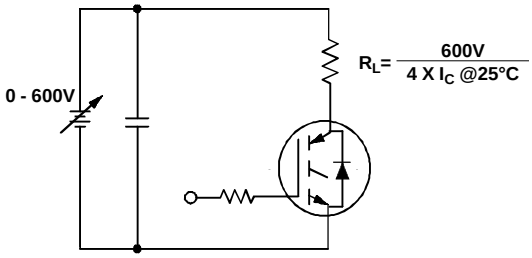


Figure 19. Pulsed Collector Current Test Circuit

Notes:

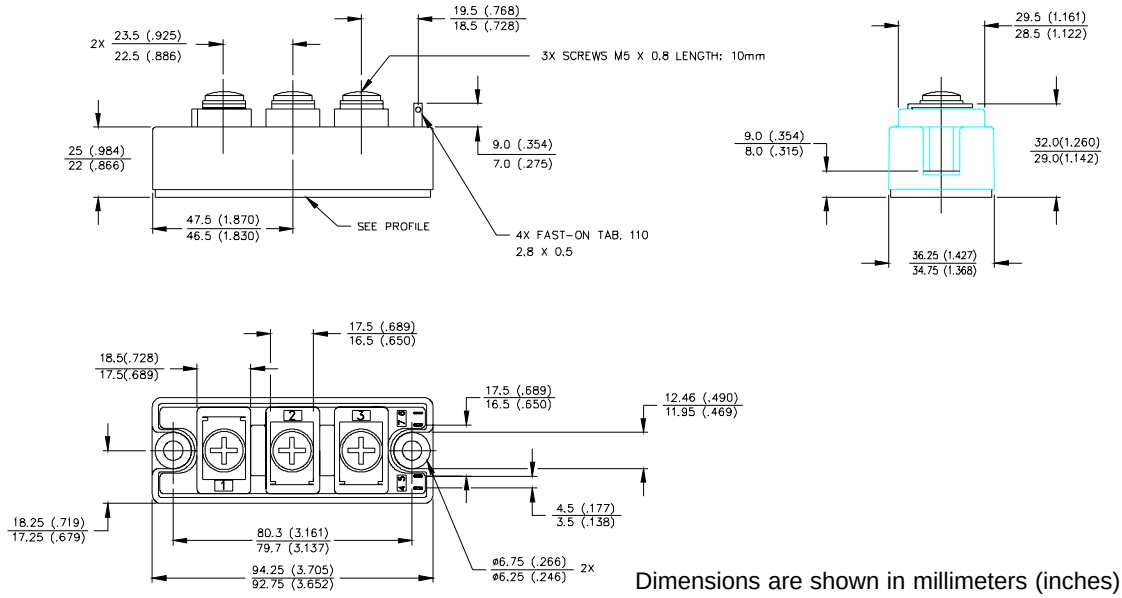
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 17

③ For screws M5x0.8

④ Pulse width 50µs; single shot.

Case Outline — INT-A-PAK



Dimensions are shown in millimeters (inches)

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IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
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PD - 5.067A

PRELIMINARY

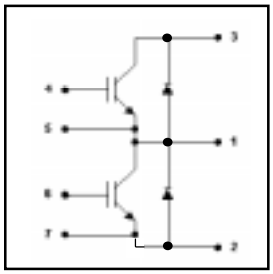
GA150TD120U

"HALF-BRIDGE" IGBT DOUBLE INT-A-PAK

Ultra-Fast™ Speed IGBT

Features

- Generation 4 IGBT technology
- Standard: Optimized for minimum saturation voltage and operating frequencies up to 10kHz
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL approved



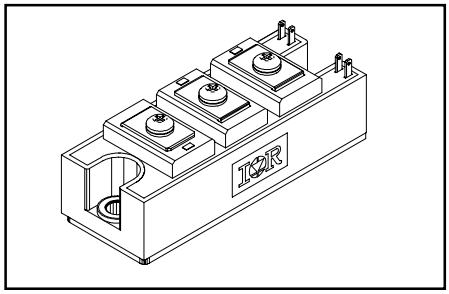
V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.4V

@V_{GE} = 15V, I_C = 150A

Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	150	A
I_{CM}	Pulsed Collector Current①	300	
I_{LM}	Peak Switching Current②	300	
I_{FM}	Peak Diode Forward Current	300	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	780	W
P_D @ T_C = 85°C	Maximum Power Dissipation	406	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.16	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.20	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3③	—	3.0	
	Weight of Module	400	—	g

3/20/98

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	2.4	2.9		V_{GE} = 15V, I_C = 150A
		—	2.2	—		V_{GE} = 15V, I_C = 150A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		I_C = 1.75 mA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.75mA
g_{fe}	Forward Transconductance ④	—	201	—	S	V_{CE} = 25V, I_C = 150A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	2	mA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	20		V_{GE} = 0V, V_{CE} = 1200V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	2.7	3.5	V	I_F = 150A, V_{GE} = 0V
		—	2.6	—		I_F = 150A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	500	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	1139	1709	nC	V_{CC} = 400V, V_{GE} = 15V
Q_{ge}	Gate - Emitter Charge (turn-on)	—	192	288		I_C = 171A
Q_{gc}	Gate - Collector Charge (turn-on)	—	377	566		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	414	—	ns	R_{G1} = 15Ω, R_{G2} = 0Ω
t_r	Rise Time	—	208	—		I_C = 150A
$t_{d(off)}$	Turn-Off Delay Time	—	552	—		V_{CC} = 720V
t_f	Fall Time	—	342	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	29	—	mJ	See Fig.17 through Fig.21
E_{off}	Turn-Off Switching Energy	—	32	—		
E_{ts}	Total Switching Energy	—	61	90		
C_{ies}	Input Capacitance	—	25630	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	1139	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	221	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	186	—	ns	I_C = 150A
I_{rr}	Diode Peak ReverseCurrent	—	133	—	A	R_{G1}= 15 Ω
Q_{rr}	Diode Recovery Charge	—	12381	—	nC	R_{G2} = 0 Ω
$di_{(rec)}M/dt$	Diode Peak Rate of Fall of Recovery During t_b	—	2524	—	A/µs	V_{CC} = 720V di/dt=1260A/µs

Details of note ① through ④ are on the last page

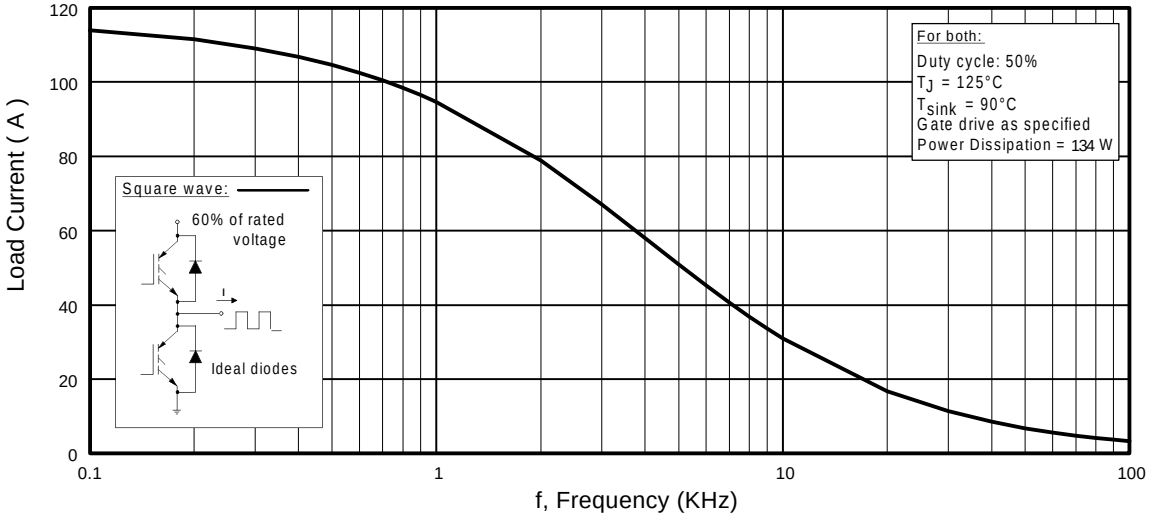


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

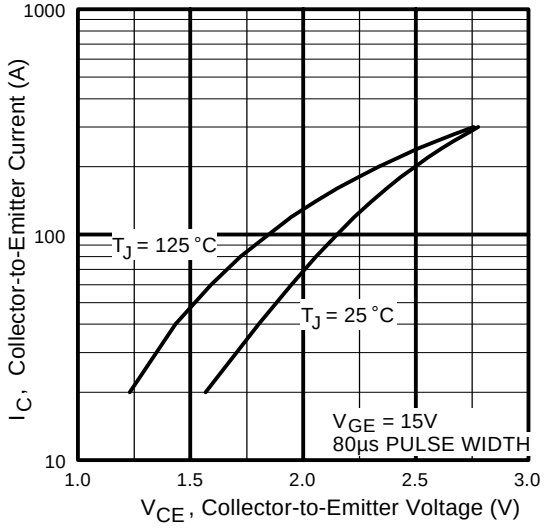


Fig. 2 - Typical Output Characteristics

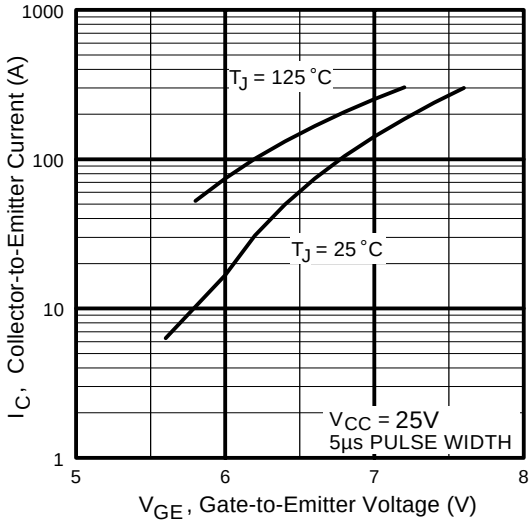


Fig. 3 - Typical Transfer Characteristics

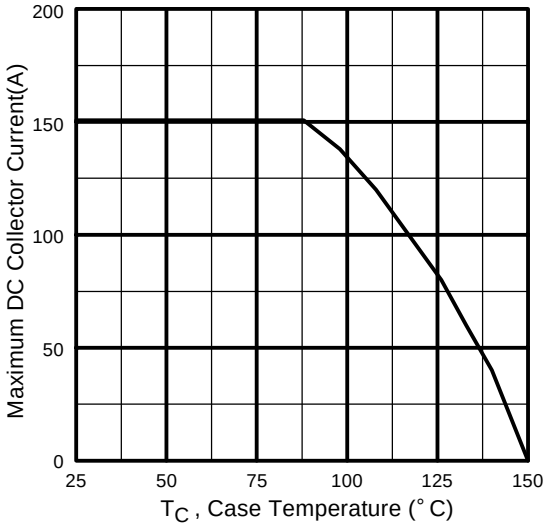


Fig. 4 - Maximum Collector Current vs. Case Temperature

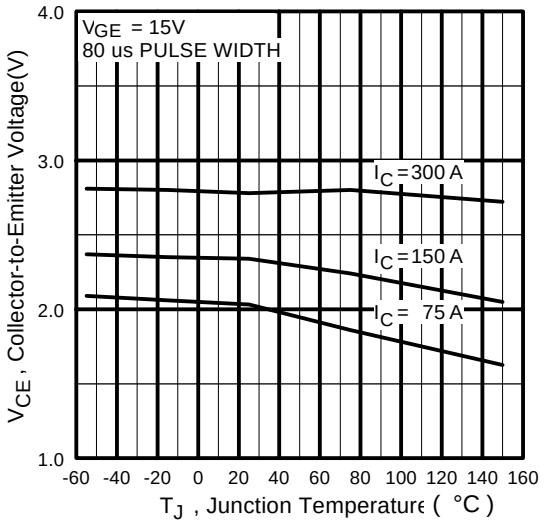


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

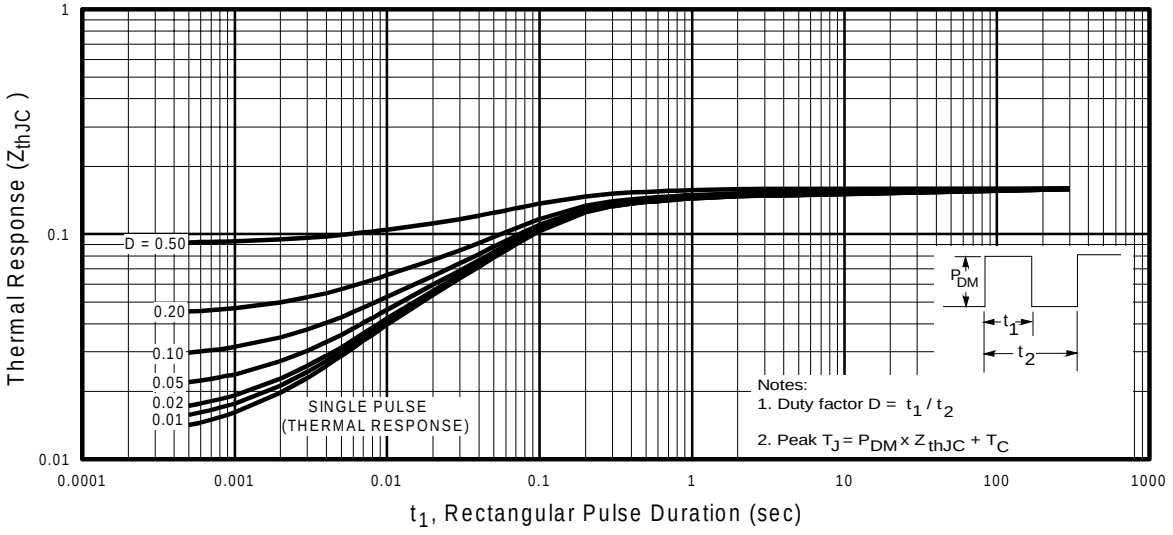


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

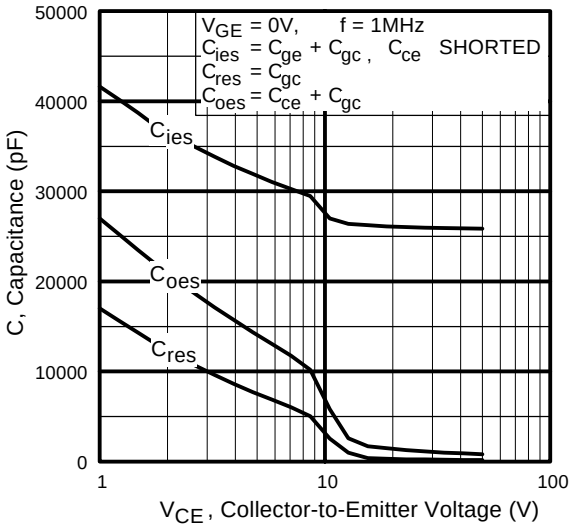


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

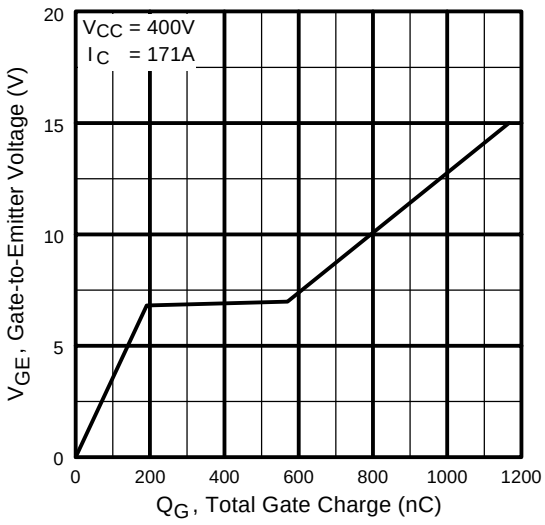


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

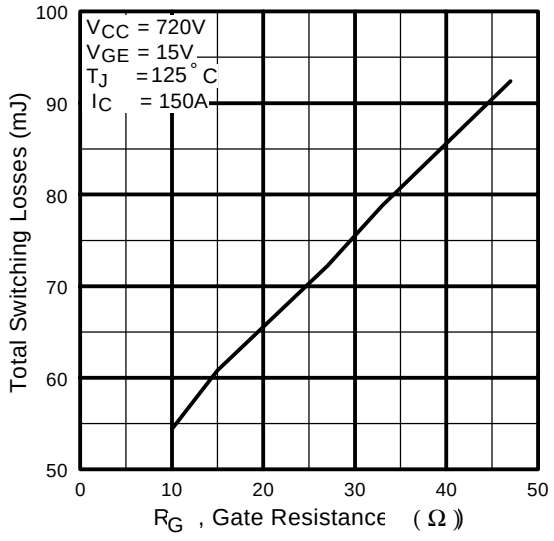


Fig. 9 - Typical Switching Losses vs. Gate Resistance

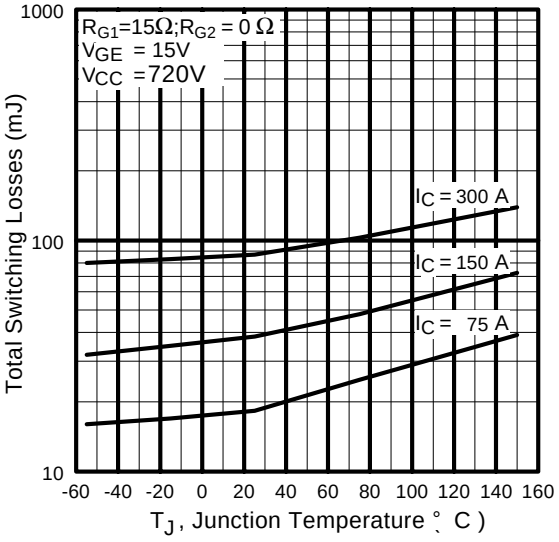


Fig. 10 - Typical Switching Losses vs. Junction Temperature

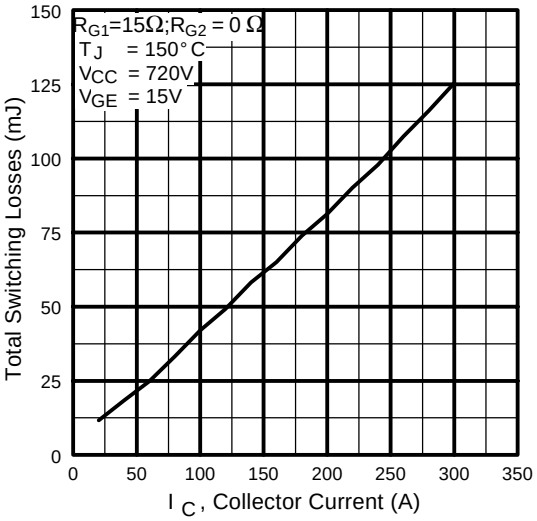


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

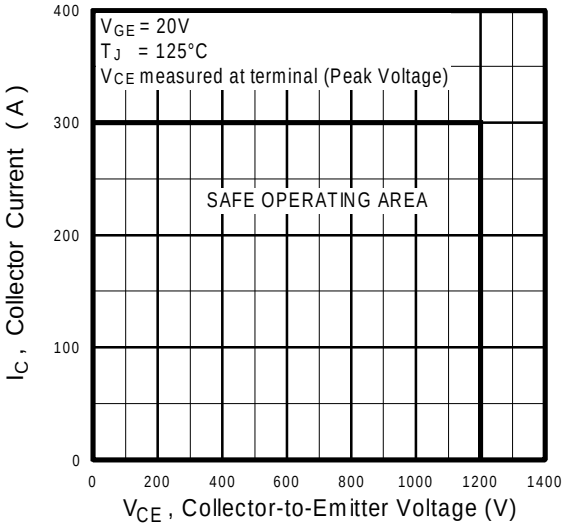


Fig. 12 - Reverse Bias SOA

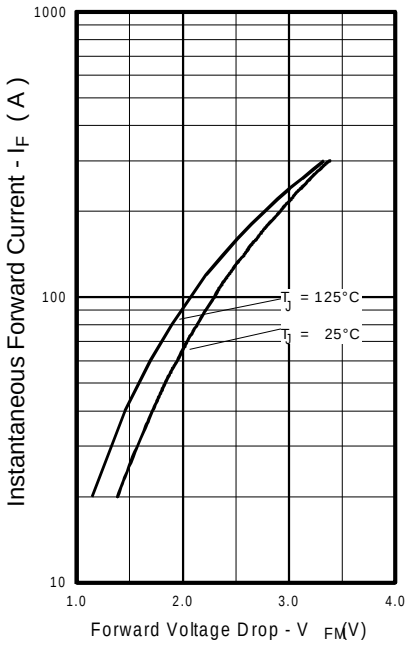


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

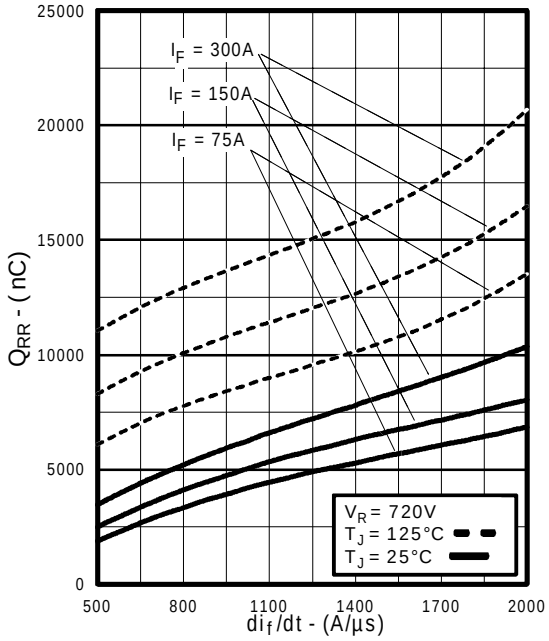


Fig. 14 - Typical Stored Charge vs. di_f/dt

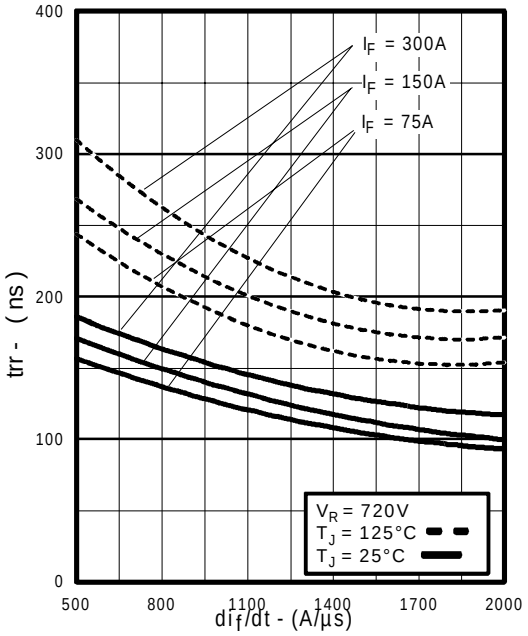


Fig. 15 - Typical Reverse Recovery vs. di_f/dt

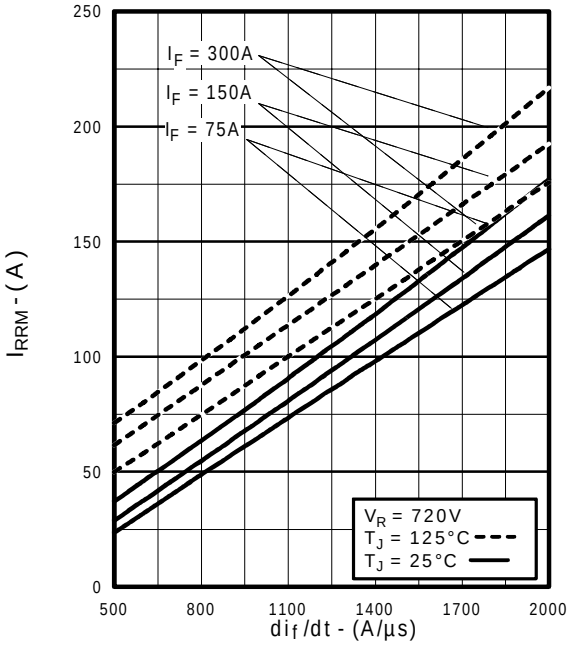


Fig. 16 - Typical Recovery Current vs. di_f/dt

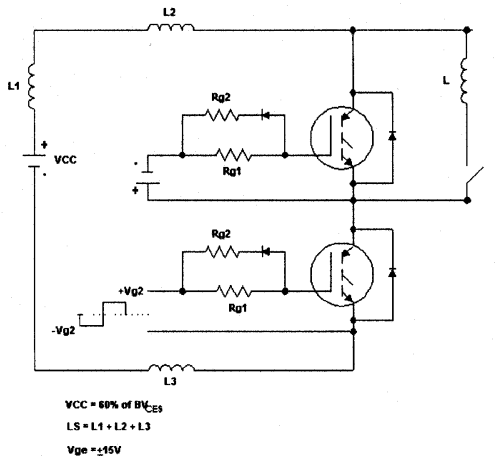


Fig. 17 - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

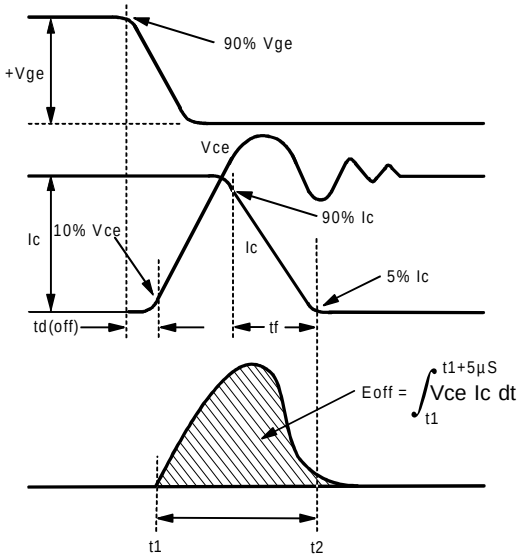


Fig. 18 - Test Waveforms for Circuit of Fig. 17, Defining E_{off}, $t_{d(off)}$, t_f

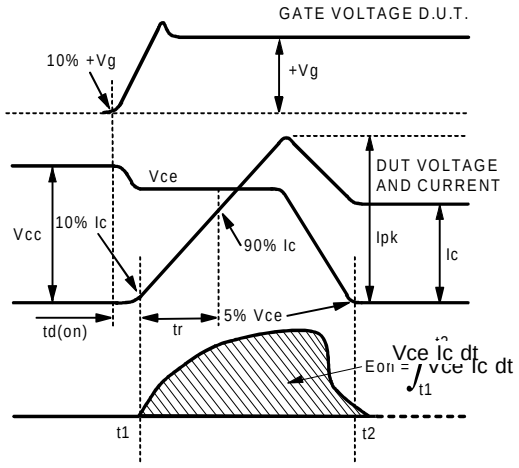


Fig. 19 - Test Waveforms for Circuit of Fig. 17, Defining E_{on}, $t_{d(on)}$, t_r

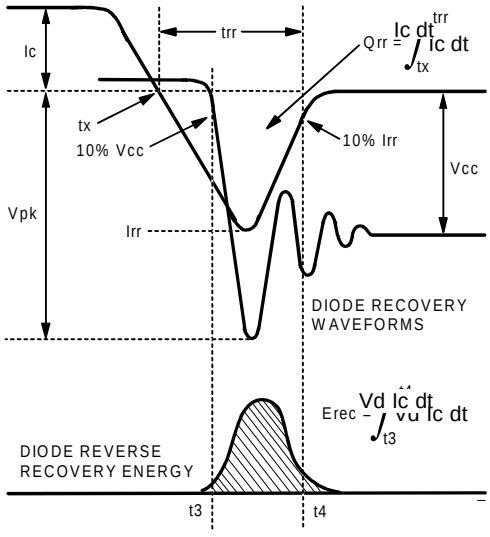


Fig. 20 - Test Waveforms for Circuit of Fig. 17, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

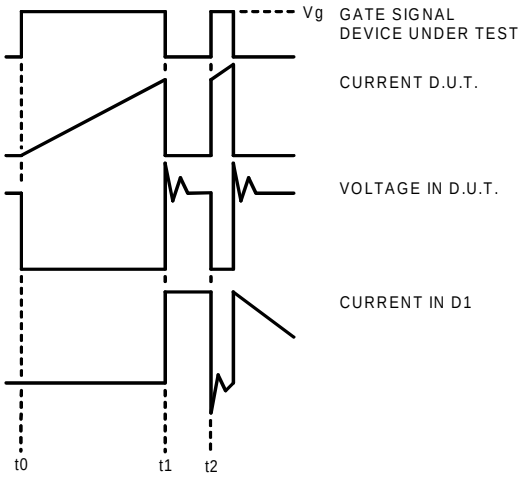


Figure 21. Macro Waveforms for Figure 17's Test Circuit

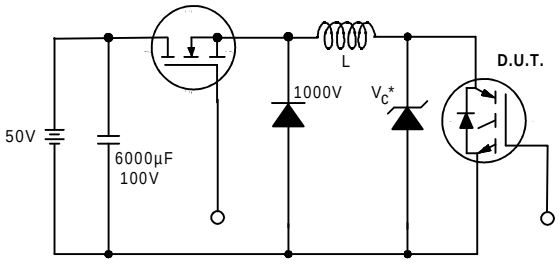


Figure 18. Clamped Inductive Load Test Circuit

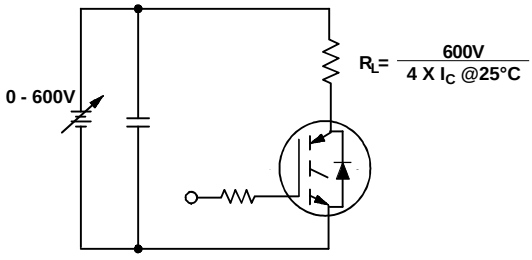


Figure 22. Pulsed Collector Current Test Circuit

Notes:

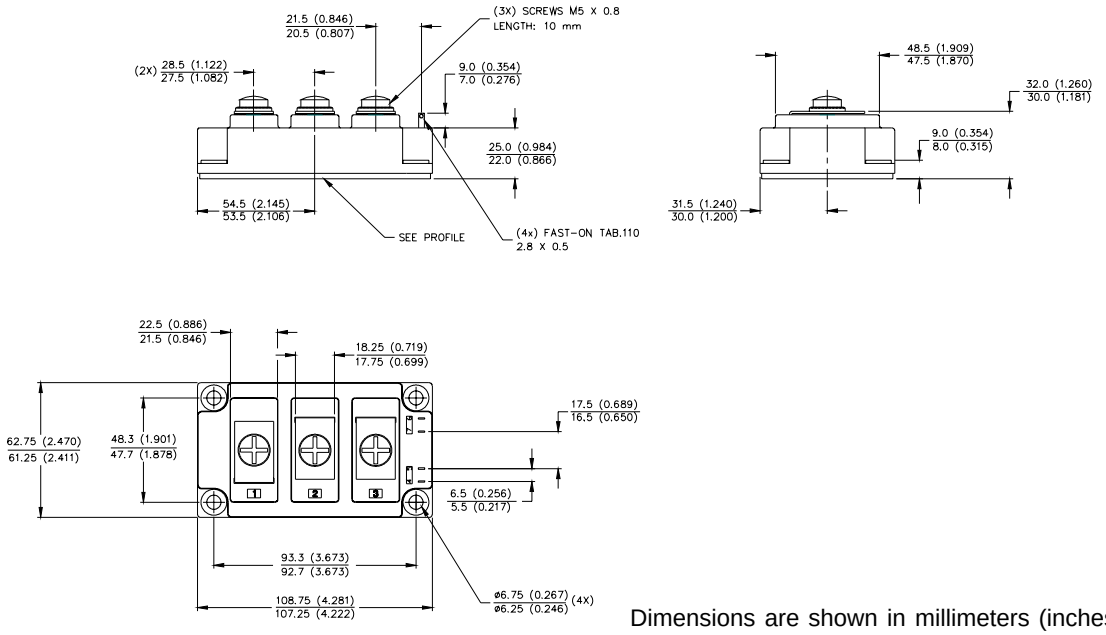
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 17

③ For screws M5x0.8

④ Pulse width 80µs; single shot.

Case Outline — DOUBLE INT-A-PAK



Dimensions are shown in millimeters (inches)

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371
http://www.irf.com/ Data and specifications subject to change without notice. 3/98

International
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PD - 50061C

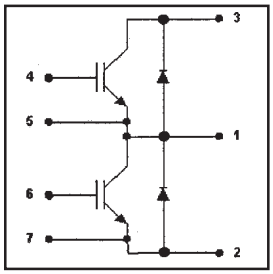
GA200TD120U

"HALF-BRIDGE" IGBT DOUBLE INT-A-PAK

Ultra-Fast™ Speed IGBT

Features

- Generation 4 IGBT technology
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL approved



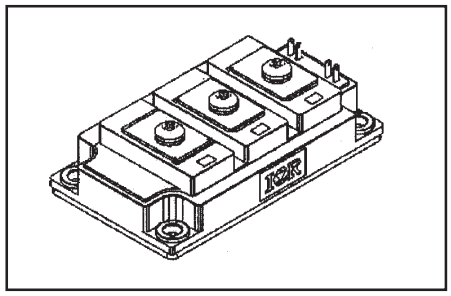
V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.3V

@V_{GE} = 15V, I_C = 200A

Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	200	A
I_{CM}	Pulsed Collector Current①	400	
I_{LM}	Peak Switching Current,	400	
I_{FM}	Peak Diode Forward Current	400	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	1040	W
P_D @ T_C = 85°C	Maximum Power Dissipation	540	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.12	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.20	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3③	—	3.0	
	Weight of Module	400	—	g

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	2.3	2.8		V_{GE} = 15V, I_C = 200A
		—	2.1	—		V_{GE} = 15V, I_C = 200A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		I_C = 2.5mA
$DV_{GE(th)}/DT_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 2.5mA
g_{fe}	Forward Transconductance ④	—	261	—	S	V_{CE} = 25V, I_C = 200A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	2.0	mA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	20		V_{GE} = 0V, V_{CE} = 1200V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	3.2	4.1	V	I_F = 200A, V_{GE} = 0V
		—	3.1	—		I_F = 200A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	500	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	1660	2490	nC	V_{CC} = 400V V_{GE} = 15V
Qge	Gate - Emitter Charge (turn-on)	—	280	420		I_C = 249A
Q_{gc}	Gate - Collector Charge (turn-on)	—	550	825		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	636	—	ns	R_{G1} = 15Ω, R_{G2} = 0Ω,
t_r	Rise Time	—	201	—		I_C = 200A
$t_{d(off)}$	Turn-Off Delay Time	—	650	—		V_{CC} = 720V
t_f	Fall Time	—	341	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	44	—	mJ	
$E_{off\ (1)}$	Turn-Off Switching Energy	—	44	—		
$E_{ts\ (1)}$	Total Switching Energy	—	88	130		
C_{ies}	Input Capacitance	—	37343	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	1660	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	322	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	196	—	ns	I_C = 200A
I_{rr}	Diode Peak ReverseCurrent	—	131	—	A	R_{G1} = 15Ω
Q_{rr}	Diode Recovery Charge	—	12833	—	nC	R_{G2} = 0Ω
$di_{(rec)}M_{/dt}$	Diode Peak Rate of Fall of Recovery During t_b	—	1740	—	A/µs	V_{CC} = 720V di/dt»1294A/µs

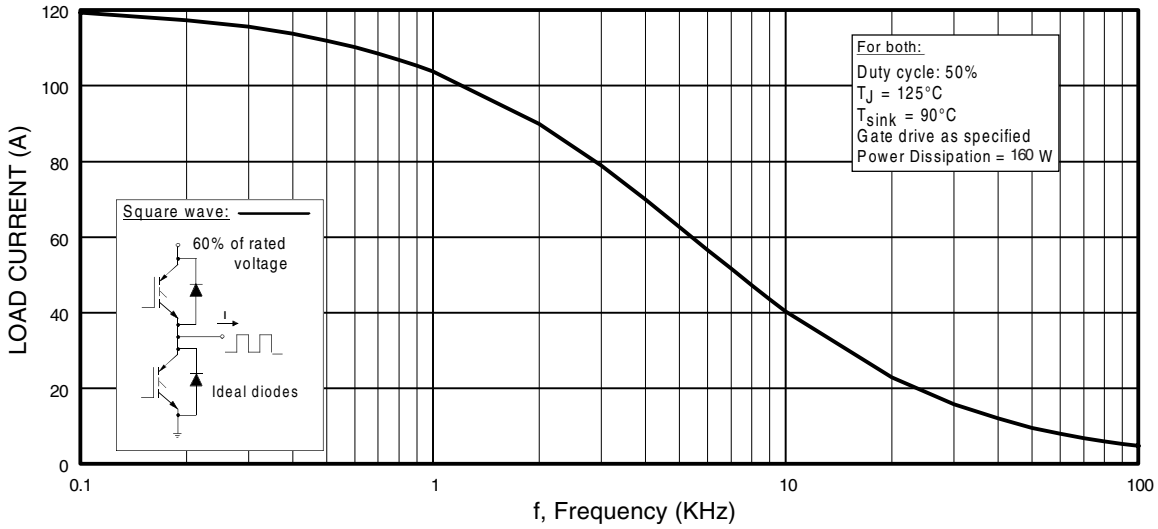


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

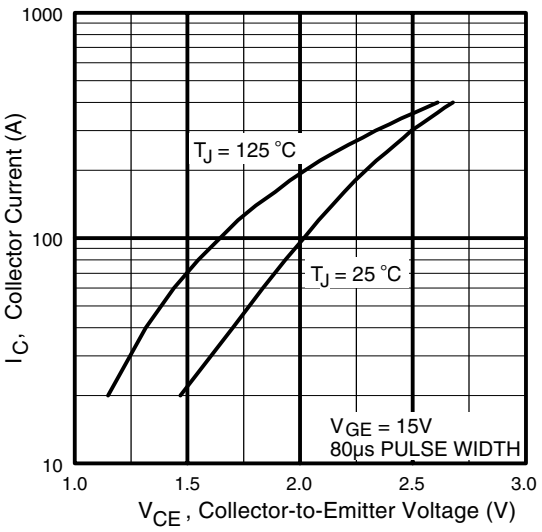


Fig. 2 - Typical Output Characteristics

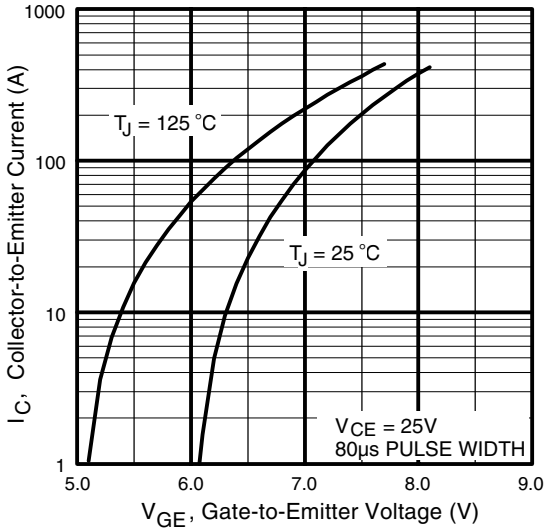


Fig. 3 - Typical Transfer Characteristics

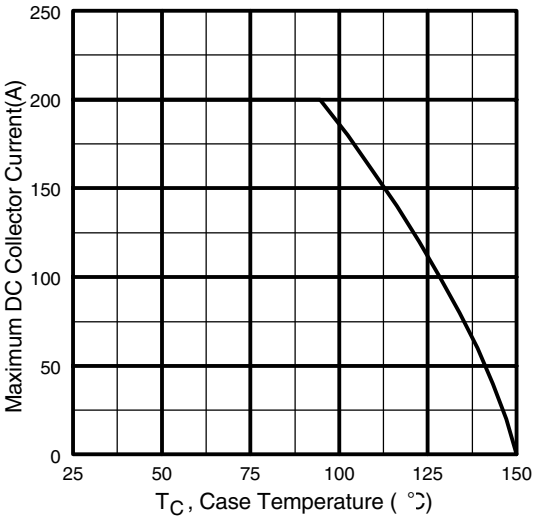


Fig. 4 - Maximum Collector Current vs. Case Temperature

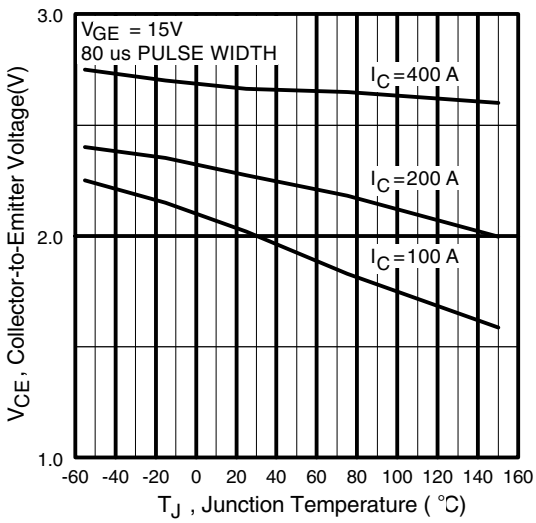


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

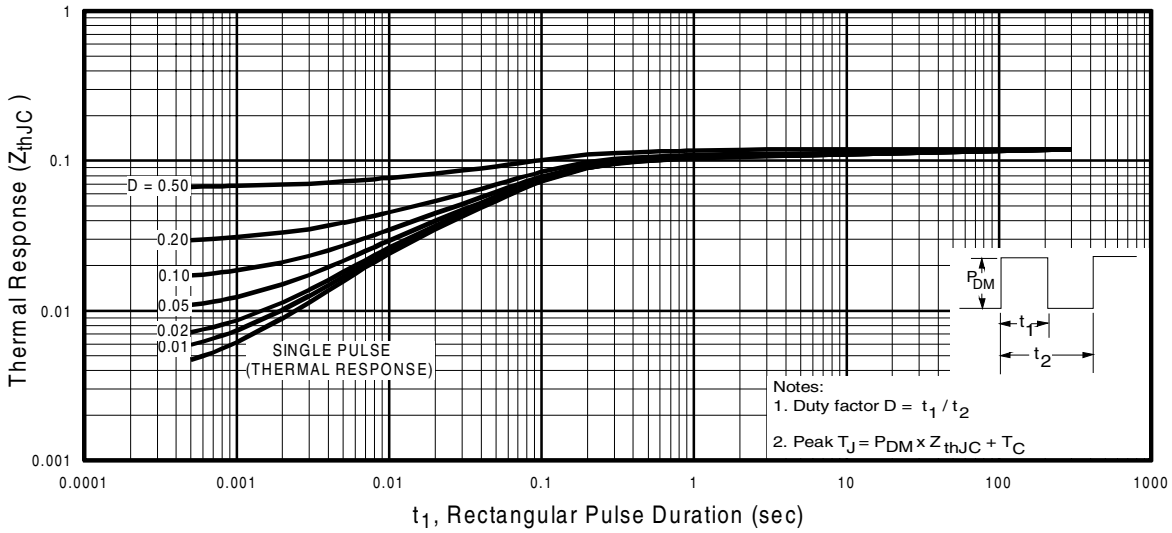


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

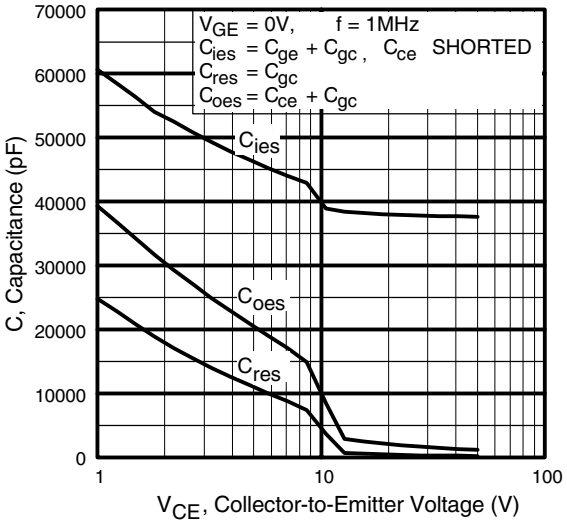


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

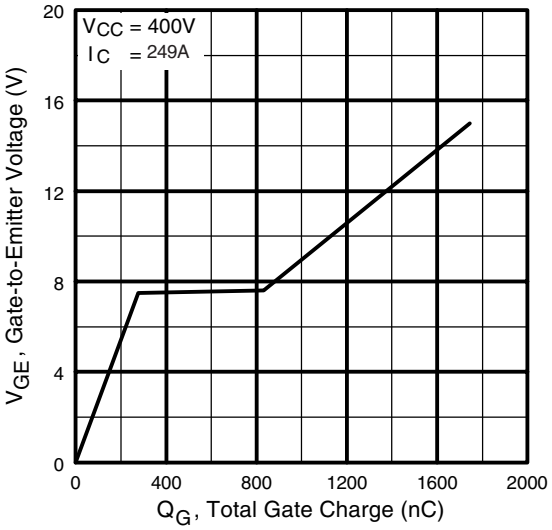


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

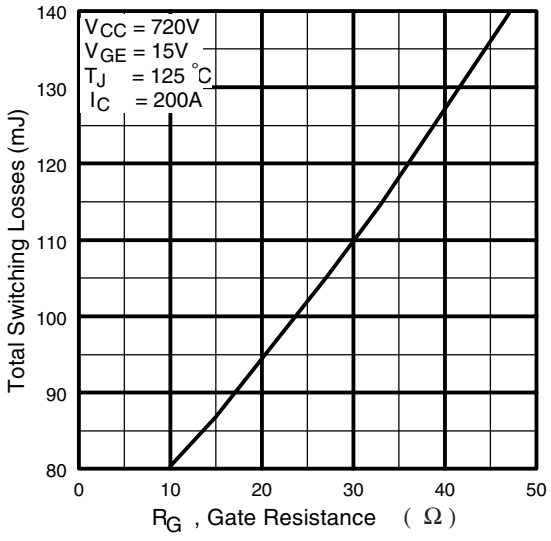


Fig. 9 - Typical Switching Losses vs. Gate Resistance

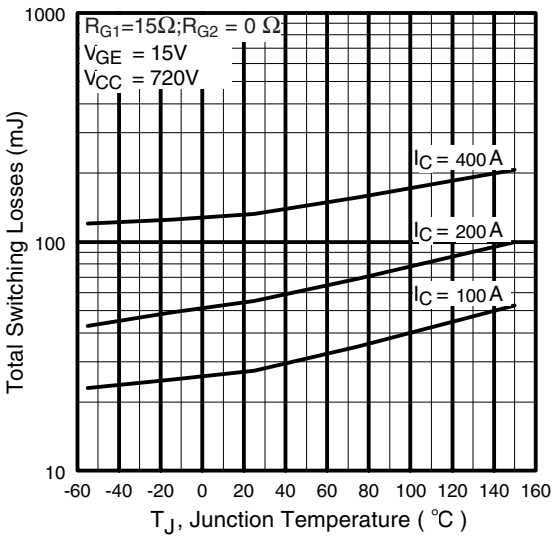


Fig. 10 - Typical Switching Losses vs. Junction Temperature

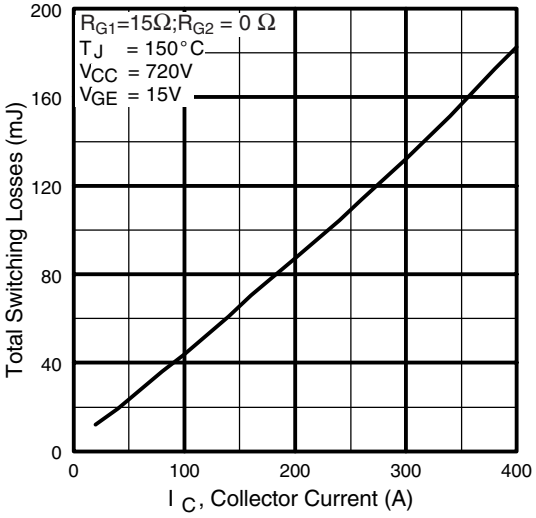


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

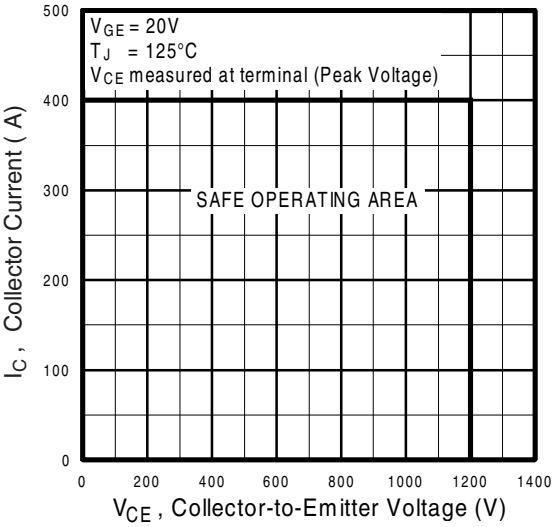


Fig. 12 - Reverse Bias SOA

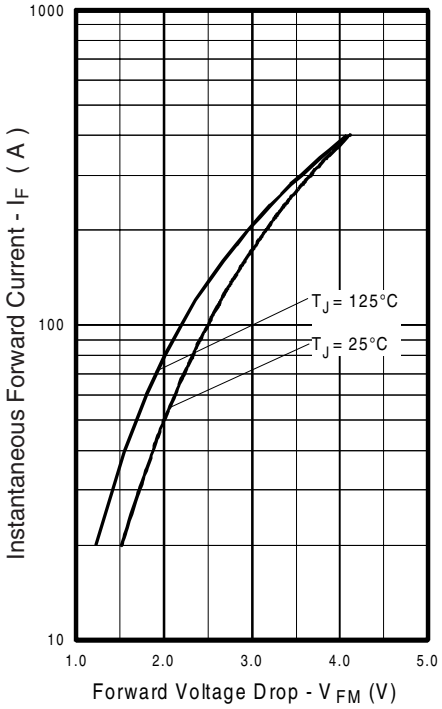


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

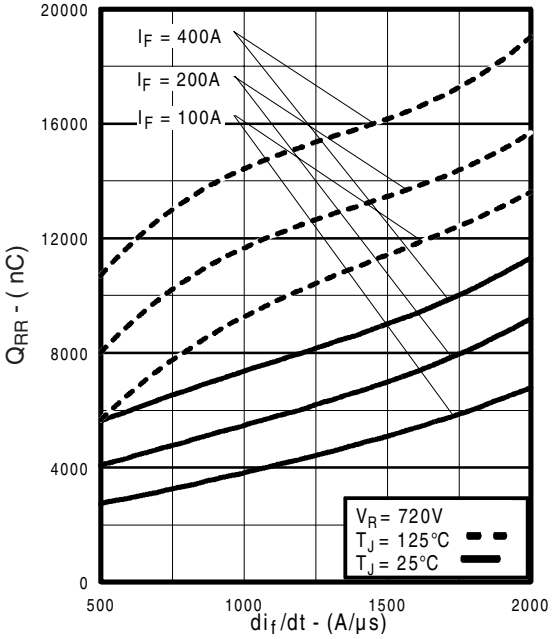


Fig. 14 - Typical Stored Charge vs. di_f/dt

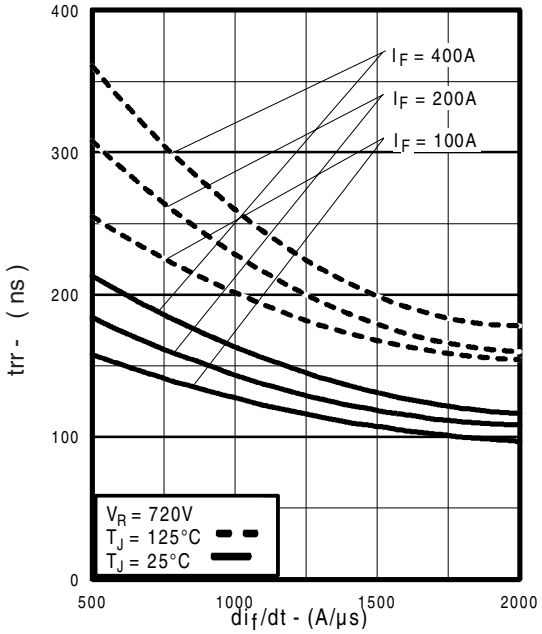


Fig. 15 - Typical Reverse Recovery vs. di_f/dt

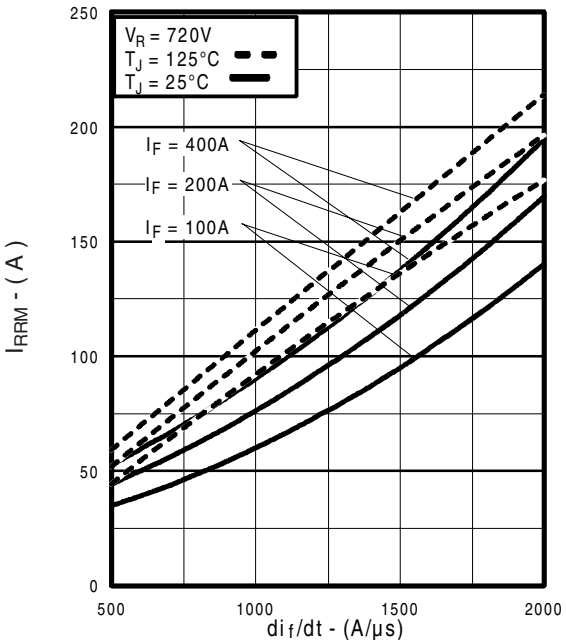


Fig. 16 - Typical Recovery Current vs. di_f/dt

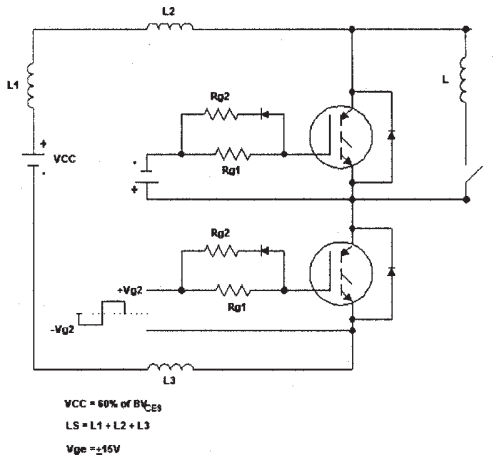


Fig. 17a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

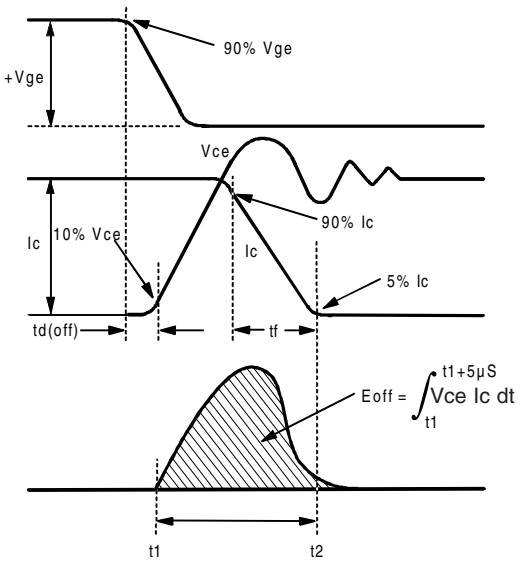


Fig. 17b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

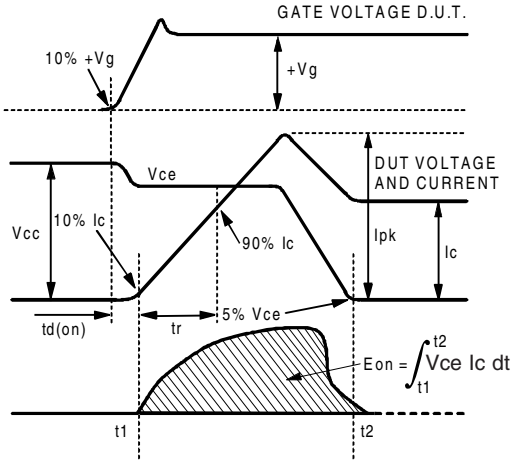


Fig. 17c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

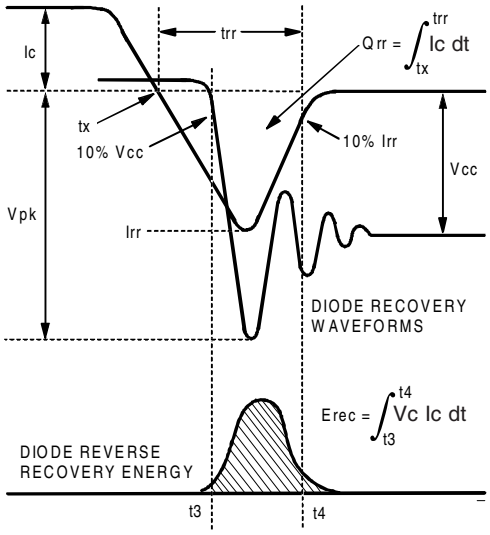


Fig. 17d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

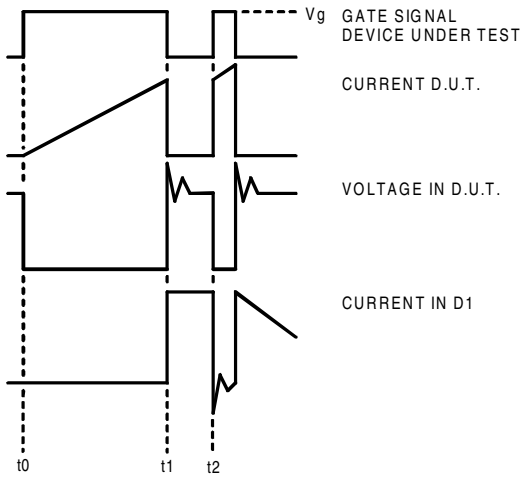


Figure 17e. Macro Waveforms for Figure 18a's Test Circuit

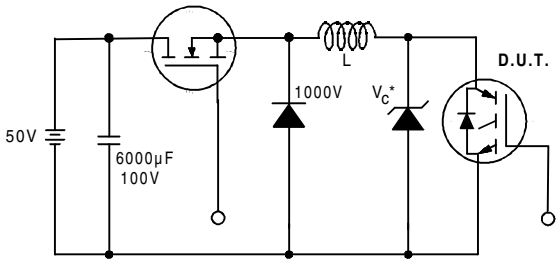


Figure 18. Clamped Inductive Load Test Circuit

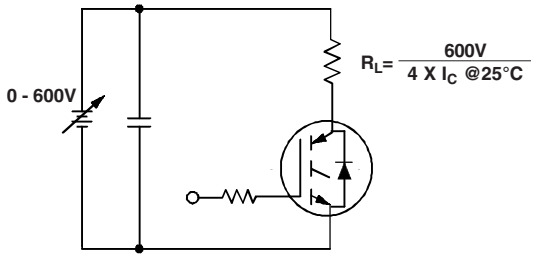


Figure 19. Pulsed Collector Current Test Circuit

Notes:

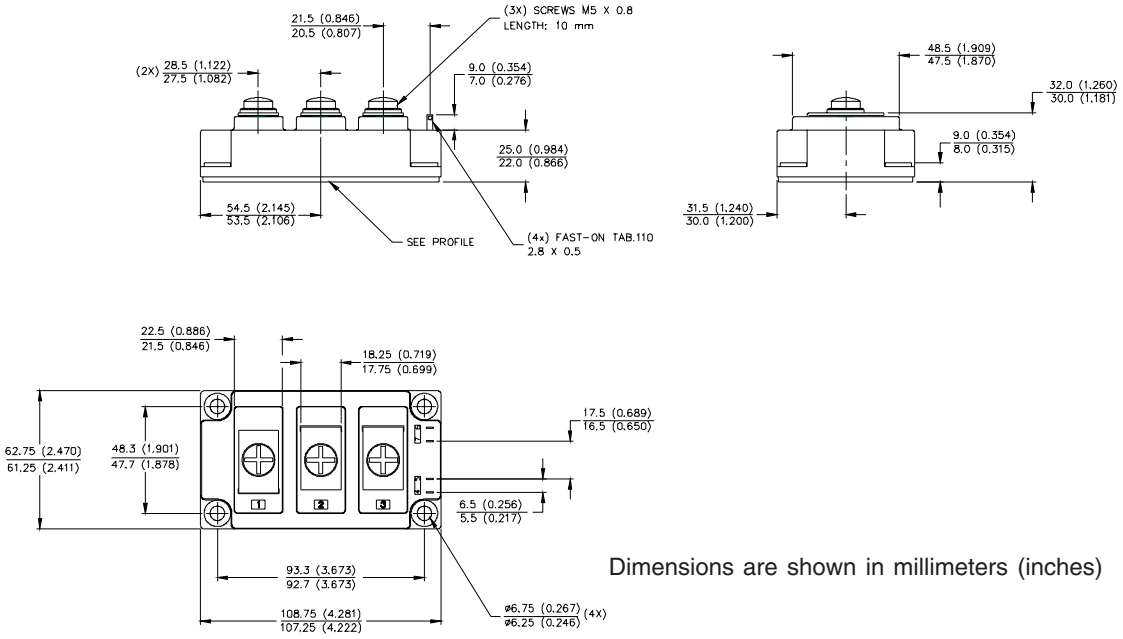
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 17

③ For screws M5x0.8

④ Pulse width 50µs; single shot.

Case Outline — DOUBLE INT-A-PAK



Dimensions are shown in millimeters (inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

International
IOR Rectifier

PD - 50054A

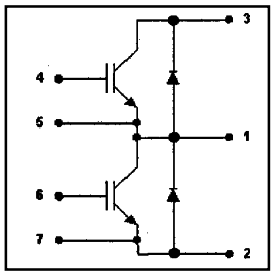
GA250TD120U

"HALF-BRIDGE" IGBT DOUBLE INT-A-PAK

Ultra-Fast™ Speed IGBT

Features

- Generation 4 IGBT technology
- Standard: Optimized for minimum saturation voltage and operating frequencies up to 10kHz
- Very low conduction and switching losses
- HEXFRED™ antiparallel diodes with ultra- soft recovery
- Industry standard package
- UL approved



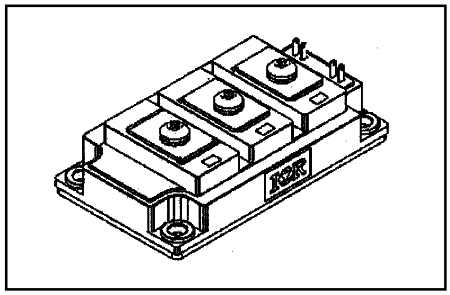
V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.4V

@V_{GE} = 15V, I_C = 250A

Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	250	A
I_{CM}	Pulsed Collector Current①	500	
I_{LM}	Peak Switching Current②	500	
I_{FM}	Peak Diode Forward Current	500	
V_{GE}	Gate-to-Emitter Voltage	±20	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	1250	W
P_D @ T_C = 85°C	Maximum Power Dissipation	650	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.10	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.20	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.1	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2 & 3③	—	3.0	
	Weight of Module	400	—	g

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	2.4	2.9		V_{GE} = 15V, I_C = 250A
		—	2.1	—		V_{GE} = 15V, I_C = 250A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = 6V, I_C = 3 mA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = 6V, I_C = 3mA
g_{fe}	Forward Transconductance ④	—	323	—	S	V_{CE} = 25V, I_C = 250A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	2.0	mA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	20		V_{GE} = 0V, V_{CE} = 1200V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	3.0	4.0	V	I_F = 250A, V_{GE} = 0V
		—	2.9	—		I_F = 250A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	500	nA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	1979	2968	nC	V_{CC} = 400V, V_{GE} = 15V
Q_{ge}	Gate - Emitter Charge (turn-on)	—	334	501		I_C = 297A
Q_{gc}	Gate - Collector Charge (turn-on)	—	655	983		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	731	—	ns	R_{G1} = 15Ω, R_{G2} = 0Ω
t_r	Rise Time	—	227	—		I_C = 250A
$t_{d(off)}$	Turn-Off Delay Time	—	653	—		V_{CC} = 720V
t_f	Fall Time	—	343	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	54	—	mJ	See Fig.17 through Fig.21
E_{off}	Turn-Off Switching Energy	—	54	—		
E_{ts}	Total Switching Energy	—	108	162		
C_{ies}	Input Capacitance	—	44517	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	1979	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	383	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	214	—	ns	I_C = 250A
I_{rr}	Diode Peak ReverseCurrent	—	155	—	A	R_{G1}= 15 Ω
Q_{rr}	Diode Recovery Charge	—	16540	—	nC	R_{G2} = 0 Ω
$di_{(rec)}M/dt$	Diode Peak Rate of Fall of Recovery During t_b	—	1970	—	A/µs	V_{CC} = 720V di/dt=1368A/µs

Details of note ① through ④ are on the last page

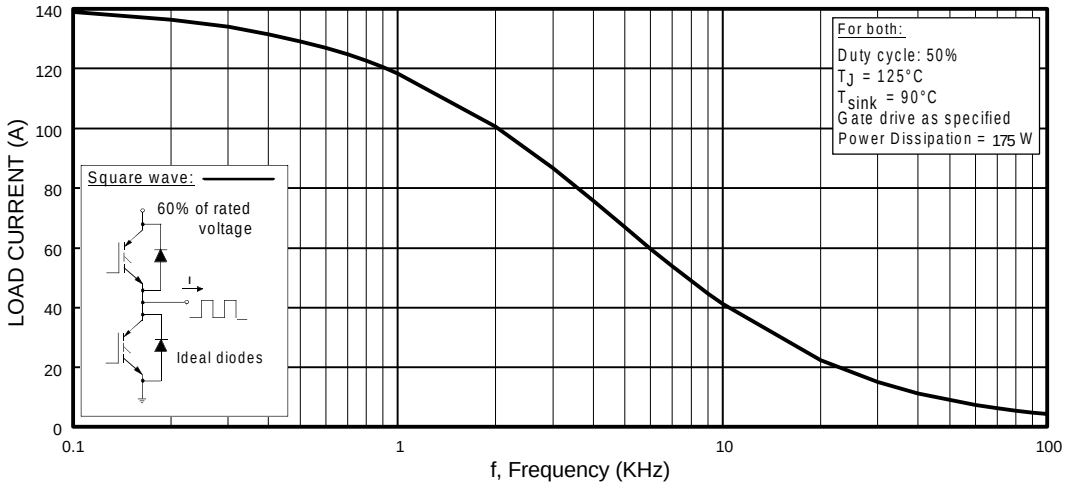


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

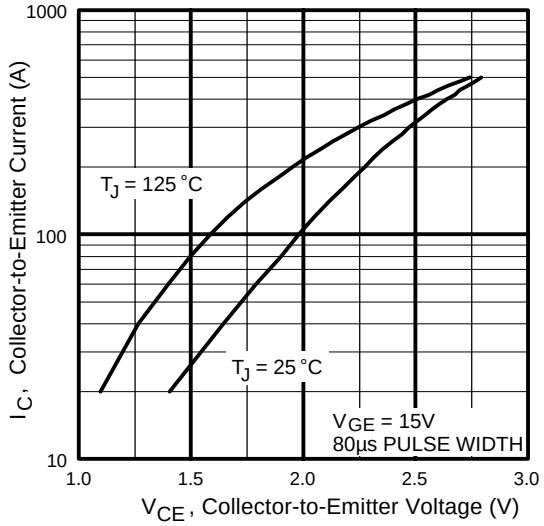


Fig. 2 - Typical Output Characteristics

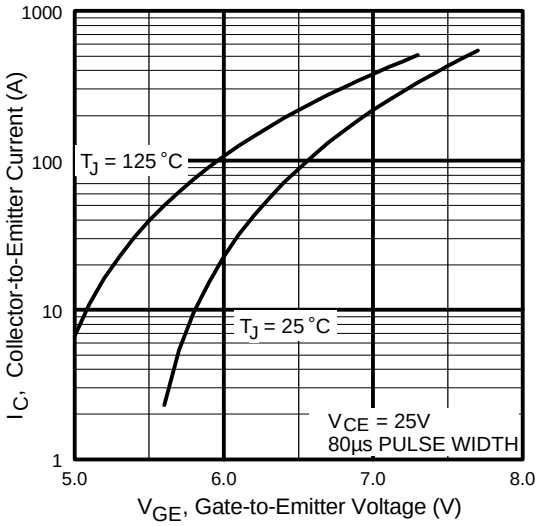


Fig. 3 - Typical Transfer Characteristics

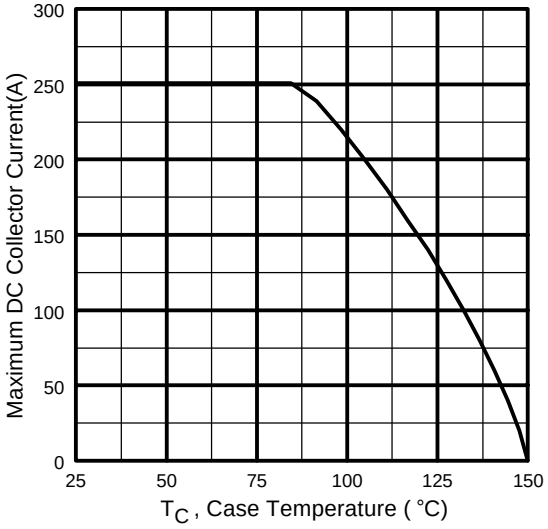


Fig. 4 - Maximum Collector Current vs. Case Temperature

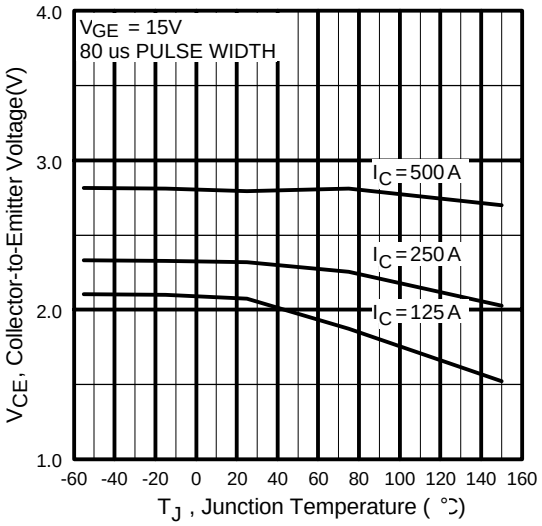


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

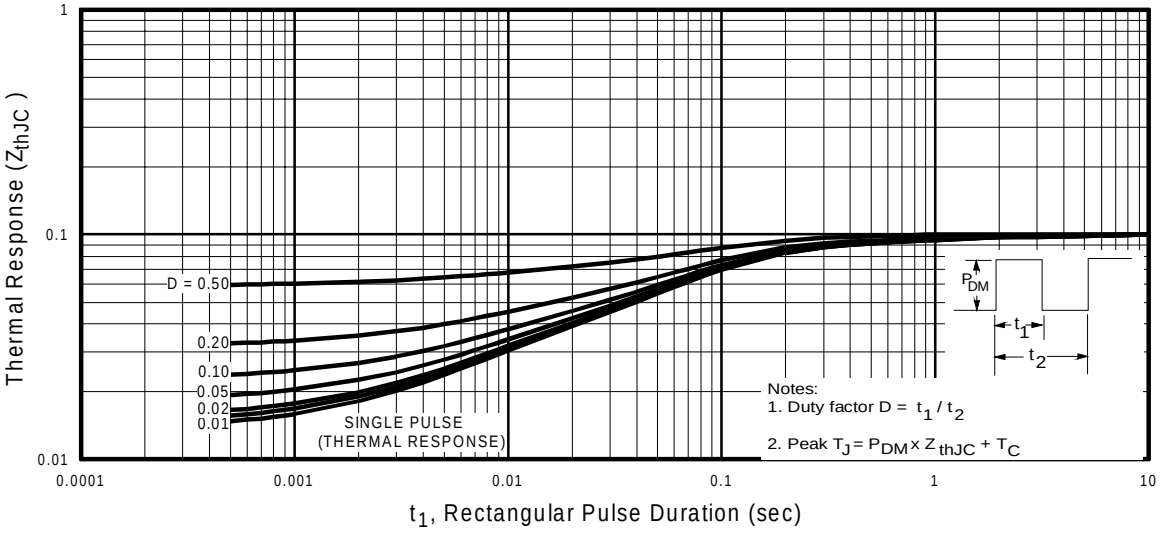
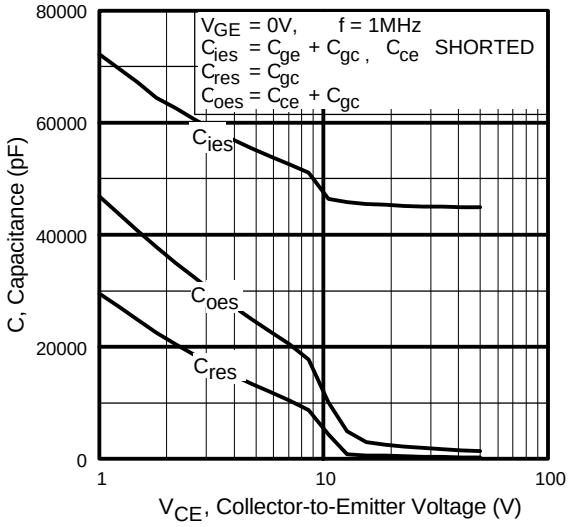


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



(° C)

Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

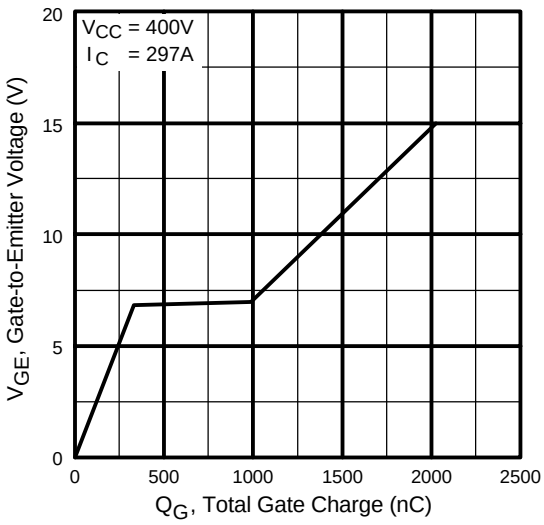


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

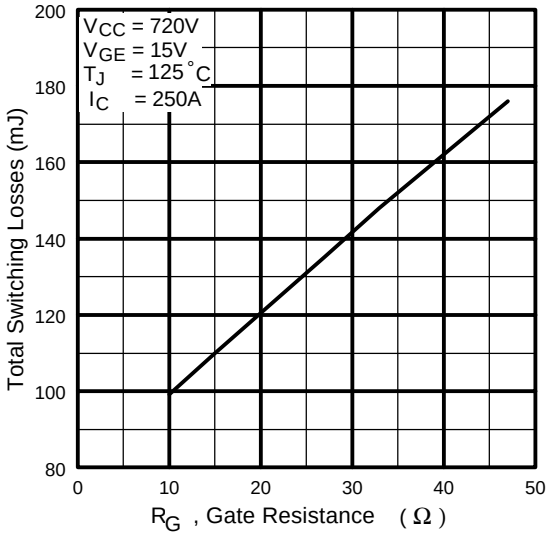


Fig. 9 - Typical Switching Losses vs. Gate Resistance

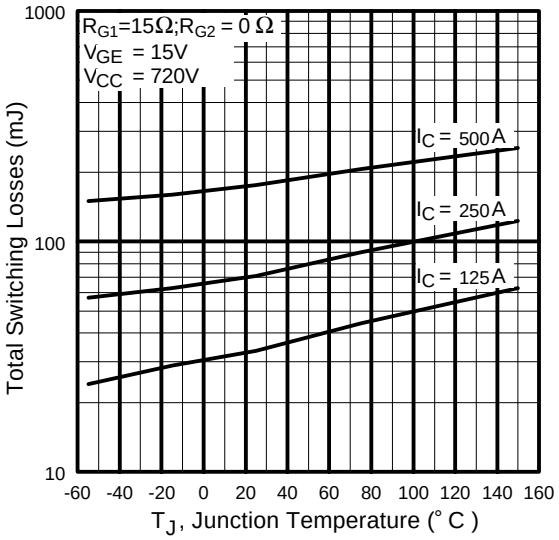


Fig. 10 - Typical Switching Losses vs. Junction Temperature

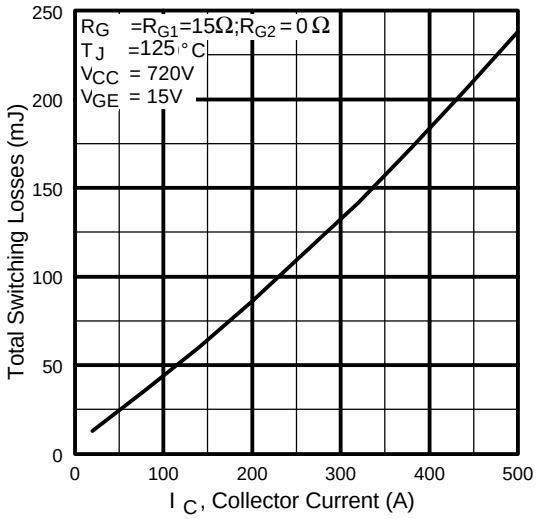


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

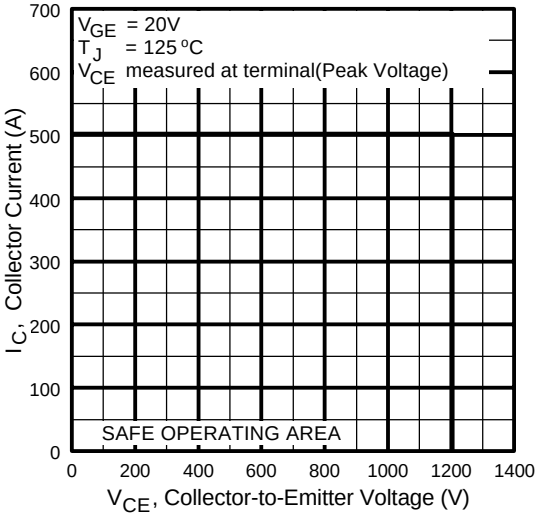


Fig. 12 - Reverse Bias SOA

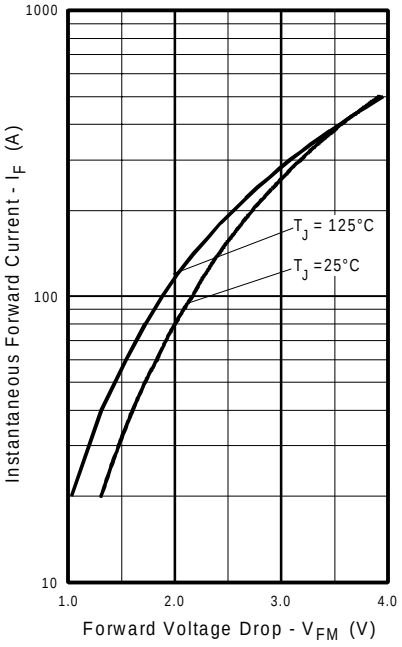


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

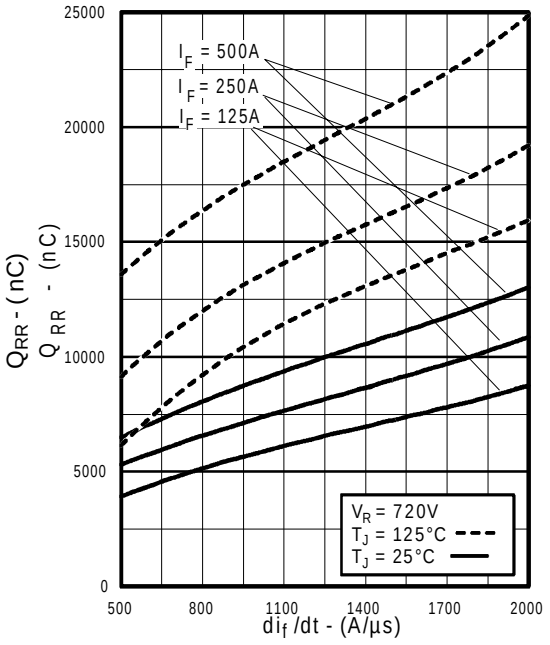


Fig. 14 - Typical Stored Charge vs. di_f/dt

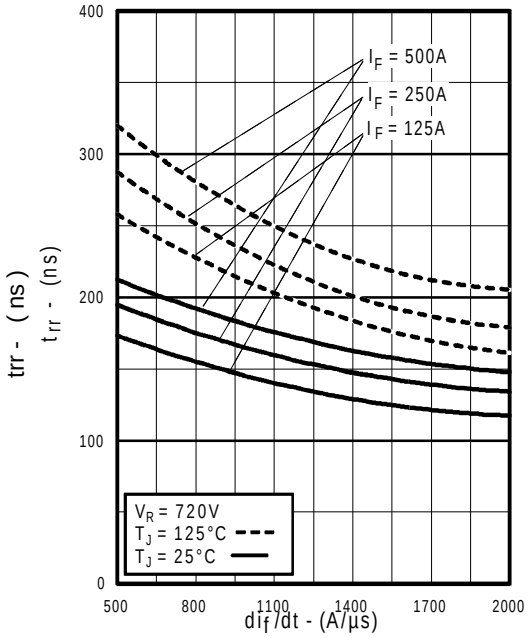


Fig. 15 - Typical Reverse Recovery vs. di_f/dt

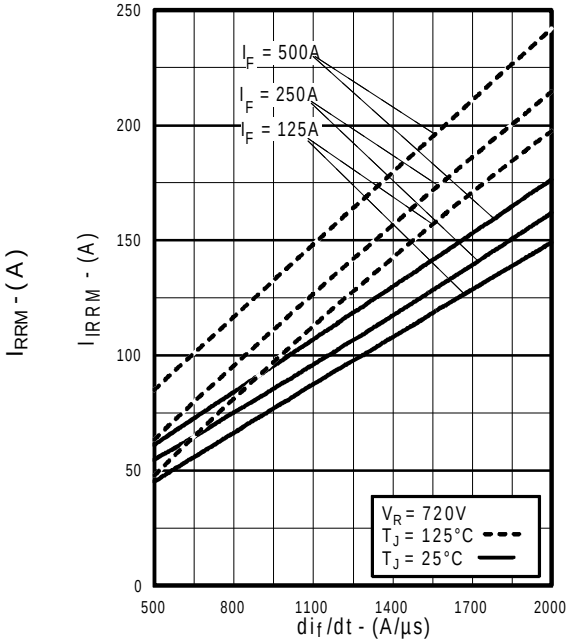


Fig. 16 - Typical Recovery Current vs. di_f/dt

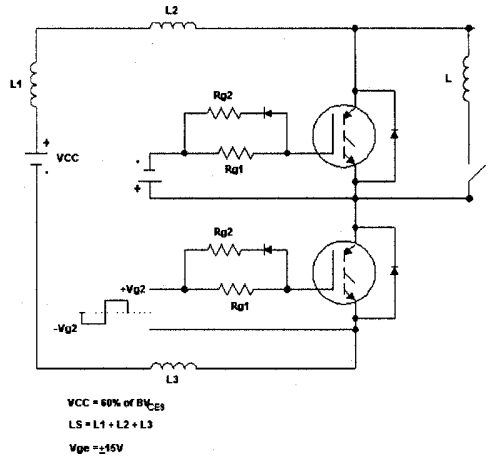


Fig. 17 - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

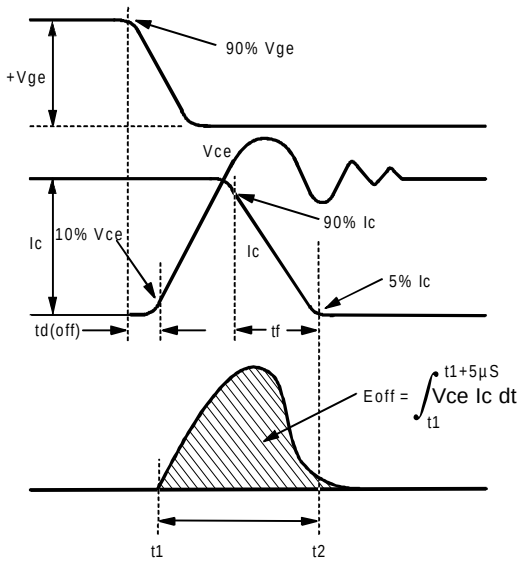


Fig. 18 - Test Waveforms for Circuit of Fig. 17, Defining E_{off}, $t_{d(off)}$, t_f

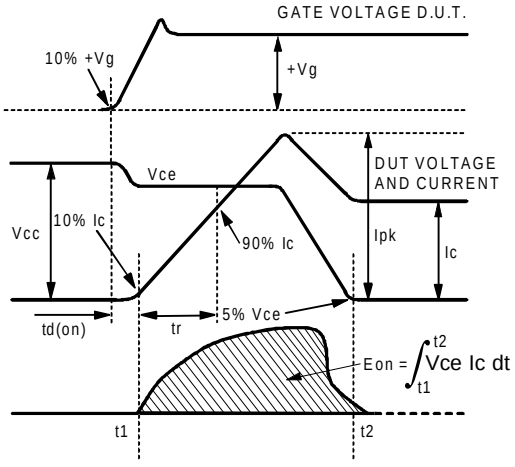


Fig. 19 - Test Waveforms for Circuit of Fig. 17, Defining E_{on}, $t_{d(on)}$, t_r

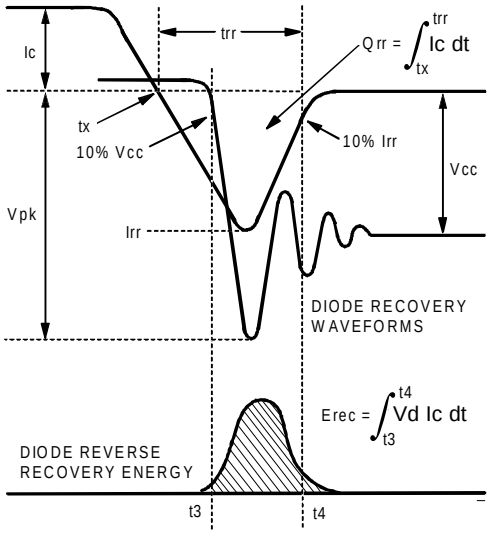


Fig. 20 - Test Waveforms for Circuit of Fig. 17, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

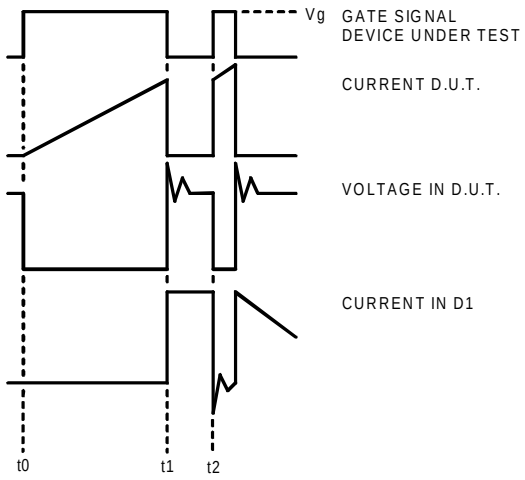


Figure 21. Macro Waveforms for Figure 17's Test Circuit

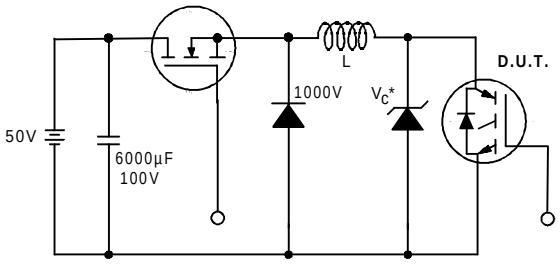


Figure 22. Clamped Inductive Load Test Circuit

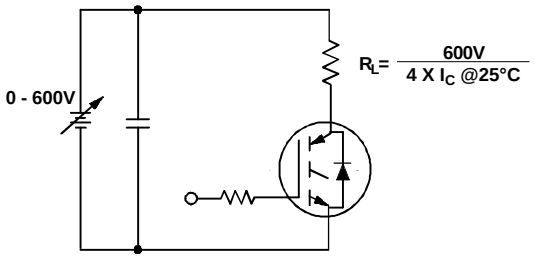


Figure 23. Pulsed Collector Current Test Circuit

Notes:

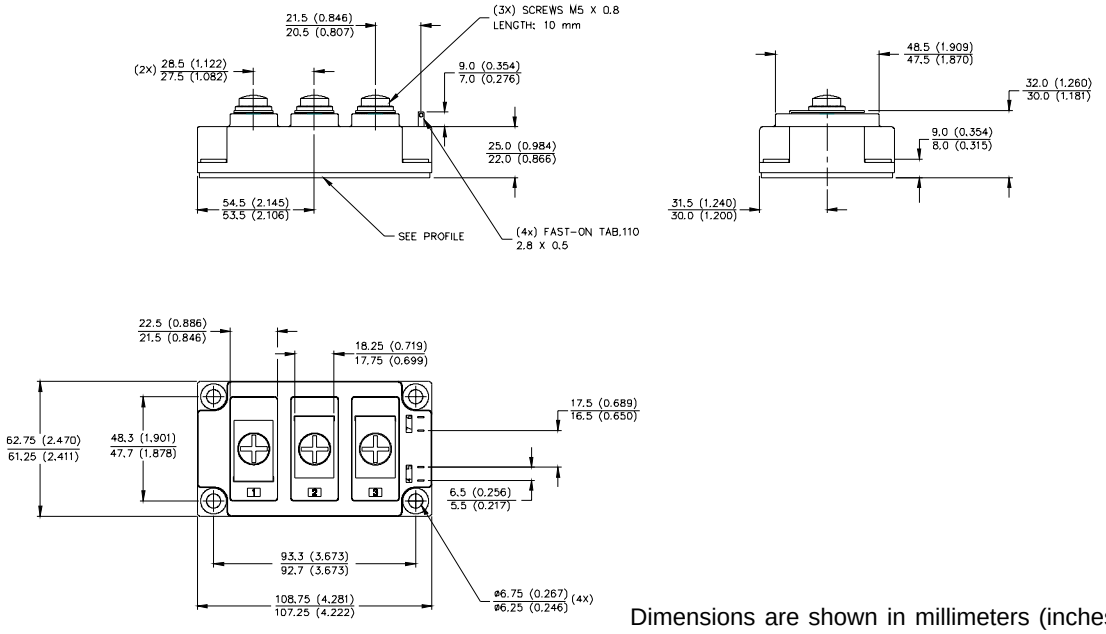
① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature.

② See fig. 17

③ For screws M5x0.8

④ Pulse width 80µs; single shot.

Case Outline — DOUBLE INT-A-PAK



Dimensions are shown in millimeters (inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

International
IOR Rectifier

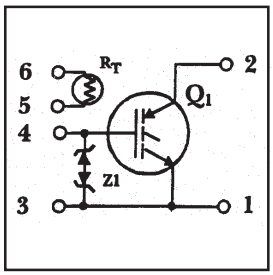
GA600GD25S

SINGLE SWITCH IGBT DOUBLE INT-A-PAK

Standard™ Speed IGBT

Features

- Standard speed, optimized for battery powered application
- Very low conduction losses
- HEXFRED™ antiparallel diodes with ultra-soft recovery
- Industry standard package
- UL recognition pending
- Internal thermistor



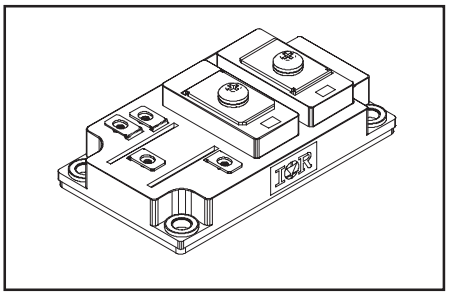
V_{CES} = 250V

$V_{CE(on)\ typ.}$ = 1.25V

@V_{GE} = 15V, I_C = 600A

Benefits

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, Welding
- Lower EMI, requires less snubbing



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	250	V
I_C @ T_C = 25°C	Continuous Collector Current	600	A
I_{CM}	Pulsed Collector Current①	1200	
I_{LM}	Peak Switching Current②	1200	
I_{FM}	Peak Diode Forward Current	1200	
V_{GE}	Gate-to-Emitter Voltage	±17	V
V_{ISOL}	RMS Isolation Voltage, Any Terminal To Case, t = 1 min	2500	
P_D @ T_C = 25°C	Maximum Power Dissipation	1920	W
P_D @ T_C = 85°C	Maximum Power Dissipation	1000	
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +125	

Thermal / Mechanical Characteristics

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - IGBT	—	0.065	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case - Diode	—	0.20	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink - Module	0.04	—	
	Mounting Torque, Case-to-Heatsink	—	4.0	N·m
	Mounting Torque, Case-to-Terminal 1, 2	—	5.0	
	Mounting Torque, Case-to-Terminal 3,4,5,6	—	1.5	
	Weight of Module	365	—	g

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	250	—	—	V	V_{GE} = 0V, I_C = 1mA
$V_{CE(on)}$	Collector-to-Emitter Voltage	—	1.25	1.4		V_{GE} = 15V, I_C = 600A
		—	1.25	—		V_{GE} = 15V, I_C = 600A, T_J = 125°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		I_C = 5.0mA, V_{CE} = 6.0V
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = 6.0V, I_C = 5.0mA,T_C= 25/125°C
g_{fe}	Forward Transconductance ③	—	720	—	S	V_{CE} = 25V, I_C = 600A
I_{CES}	Collector-to-Emitter Leaking Current	—	—	2.0	mA	V_{GE} = 0V, V_{CE} = 250V
		—	—	20		V_{GE} = 0V, V_{CE} = 250V, T_J = 125°C
V_{FM}	Diode Forward Voltage - Maximum	—	1.5	1.8	V	I_F = 300A, V_{GE} = 0V
		—	1.5	—		I_F = 300A, V_{GE} = 0V, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	1.0	µA	V_{GE} = ±14V (18V zeners gate-emitter)
ΔT_{DP}	Pulse Diode Temp Rise	—	—	80	°C	I_C = 300A, t = 150msec, Tc =70°C
R-T_{25}	Thermistor, Positive Temp Coefficient	738	820	902	Ω	I = 100mA,P = 2.5mW/°C (see note 1)

Dynamic Characteristics - T_J = 125°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	3825	5738	nC	V_{CC} = 200V, V_{GE} = 15V
Qge	Gate - Emitter Charge (turn-on)	—	555	832		I_C = 600A
Q_{gc}	Gate - Collector Charge (turn-on)	—	1262	1893		T_J = 25°C
$t_{d(on)}$	Turn-On Delay Time	—	1060	—	ns	R_{G1} = 15Ω, R_{G2} = 0Ω,
t_r	Rise Time	—	950	—		I_C = 600A
$t_{d(off)}$	Turn-Off Delay Time	—	846	—		V_{CC} = 150V, Inductor load
t_f	Fall Time	—	934	—		V_{GE} = ±15V
E_{on}	Turn-On Switching Energy	—	17	—	mJ	See Fig. 17, 19
$E_{off\ (1)}$	Turn-Off Switching Energy	—	105	—		
$E_{ts\ (1)}$	Total Switching Energy	—	122	250		
C_{ies}	Input Capacitance	—	86063	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	9754	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	1913	—		f = 1 MHz
t_{rr}	Diode Reverse Recovery Time	—	314	—	ns	I_C = 600A
I_{rr}	Diode Peak ReverseCurrent	—	80	—	A	R_{G1} = 15Ω
Q_{rr}	Diode Recovery Charge	—	12513	—	µC	R_{G2} = 0Ω
$di_{(rec)}M_{/dt}$	Diode Peak Rate of Fall of Recovery During t_b	—	632	—	A/µs	V_{CC} = 150V di/dt = 500A/µs

Notes:

1. The thermistor has an average rate of change of 7Ω /°C between 20°C and 125°C.
   Consult U.S. Sensor data sheet for P821GS1K for details

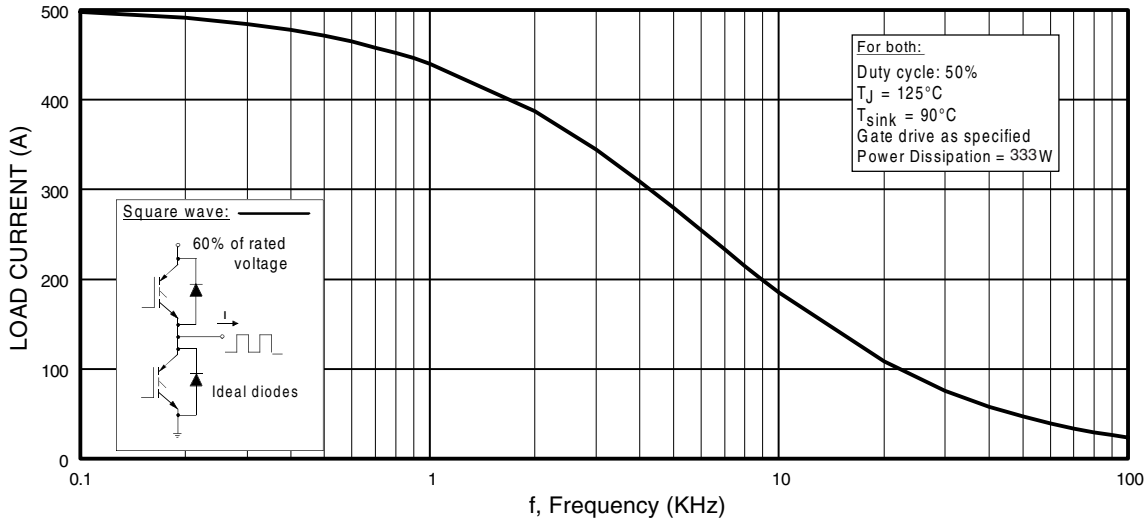


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

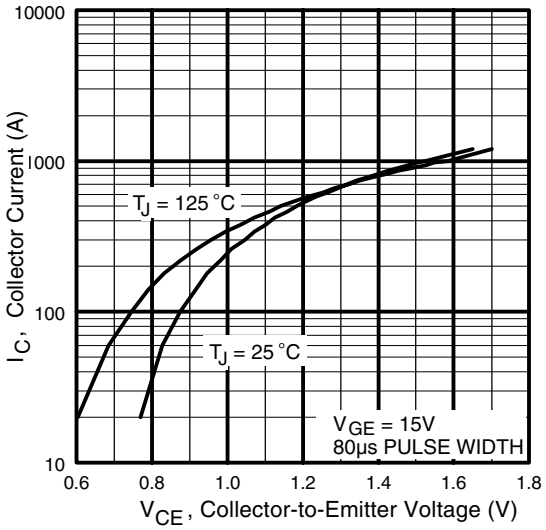


Fig. 2 - Typical Output Characteristics

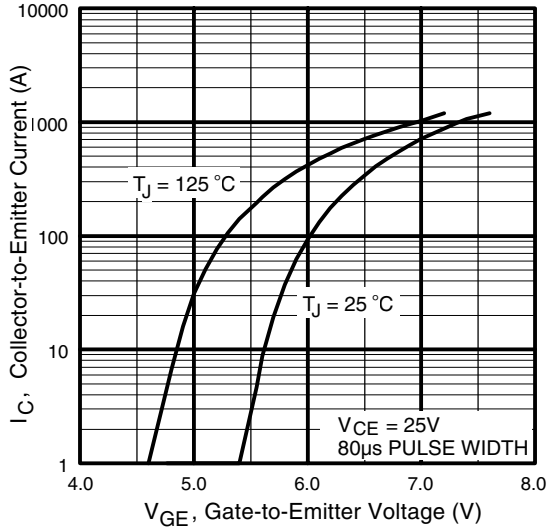


Fig. 3 - Typical Transfer Characteristics

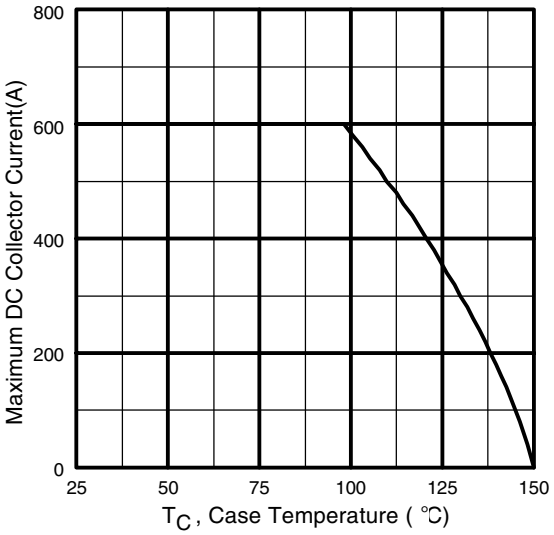


Fig. 4 - Maximum Collector Current vs. Case Temperature

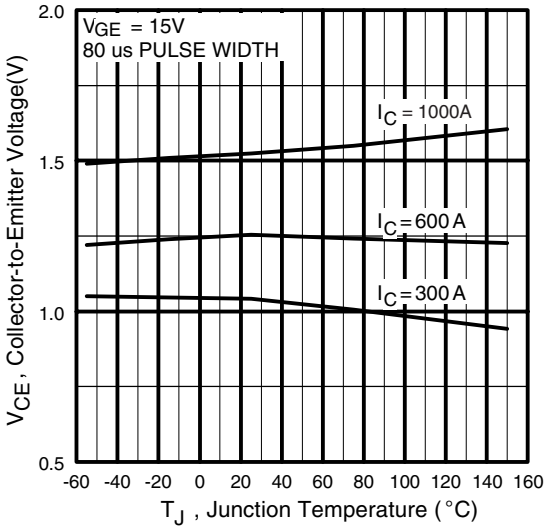


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

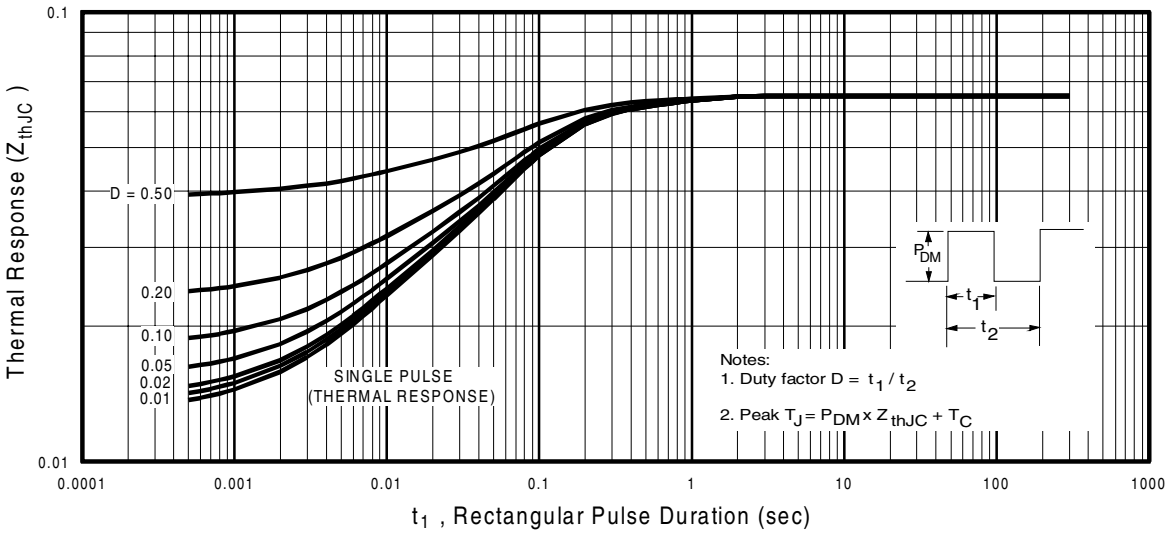


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

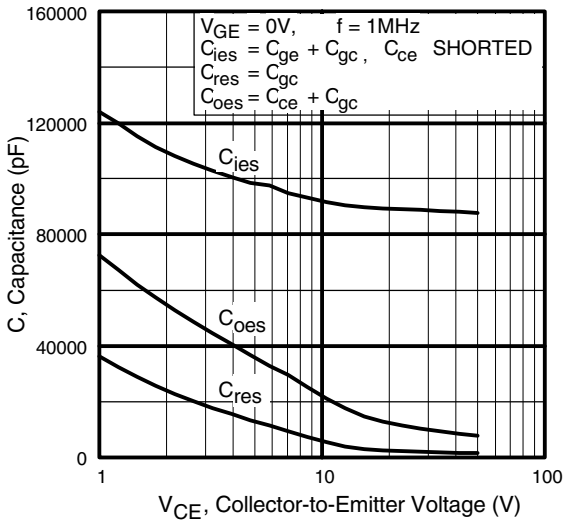


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

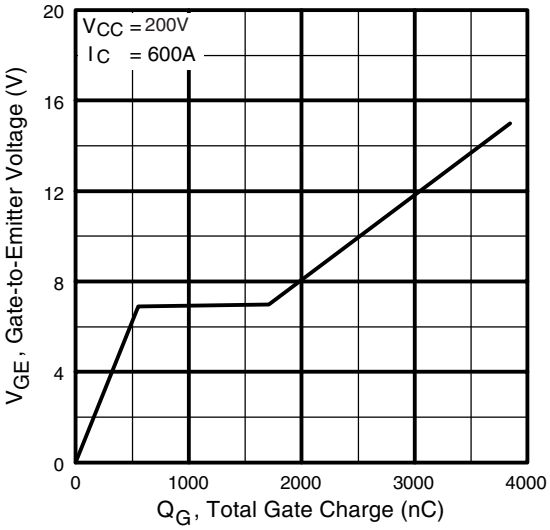


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

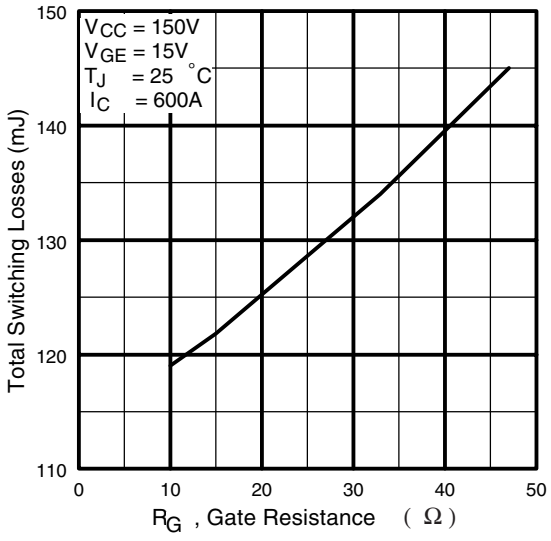


Fig. 9 - Typical Switching Losses vs. Gate Resistance

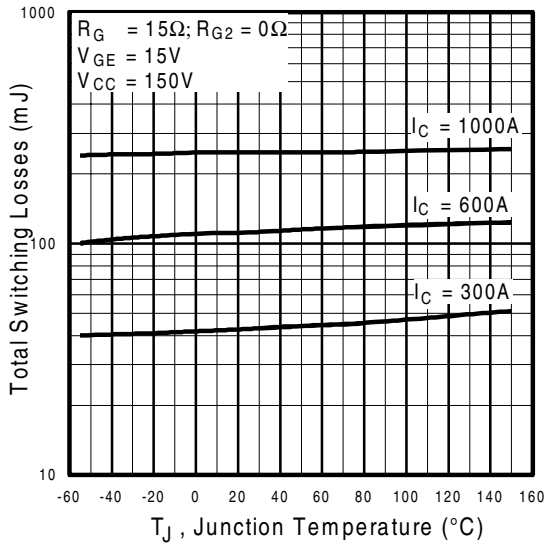


Fig. 10 - Typical Switching Losses vs. Junction Temperature

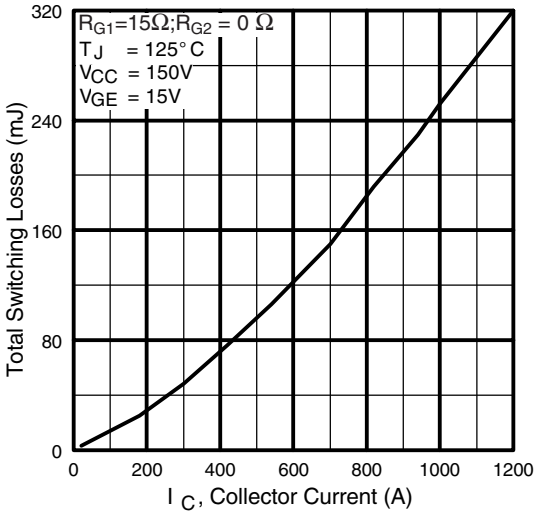


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

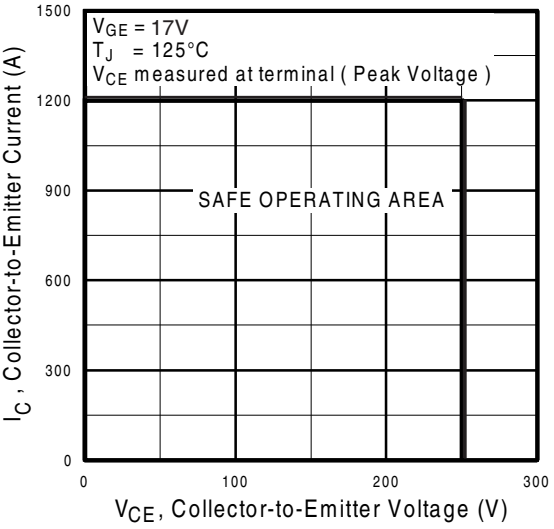


Fig. 12 - Reverse Bias SOA

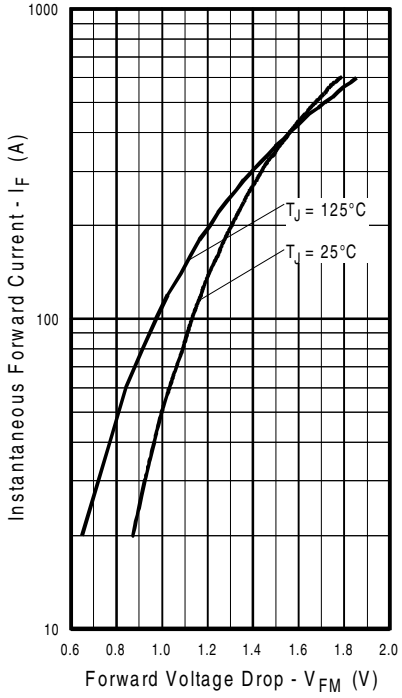


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

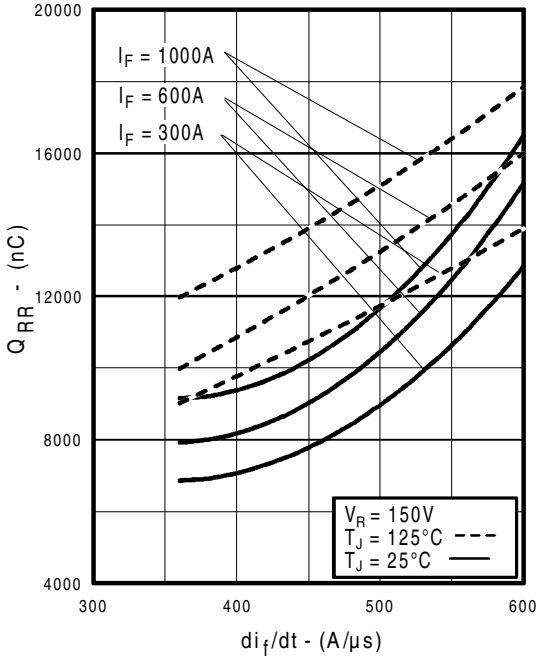


Fig. 14 - Typical Stored Charge vs. di_f/dt

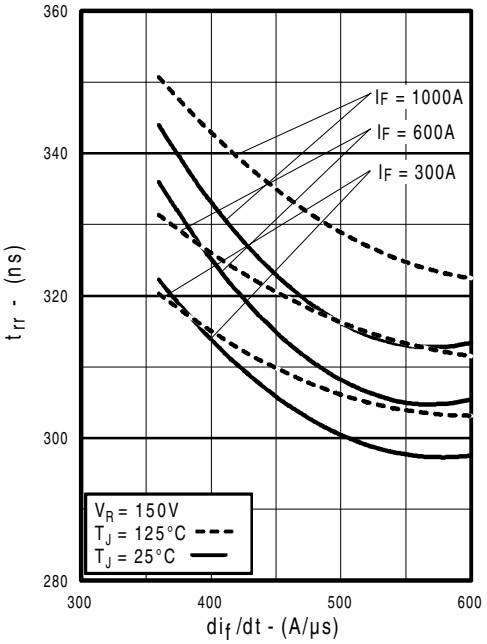


Fig. 15 - Typical Reverse Recovery vs. di_f/dt

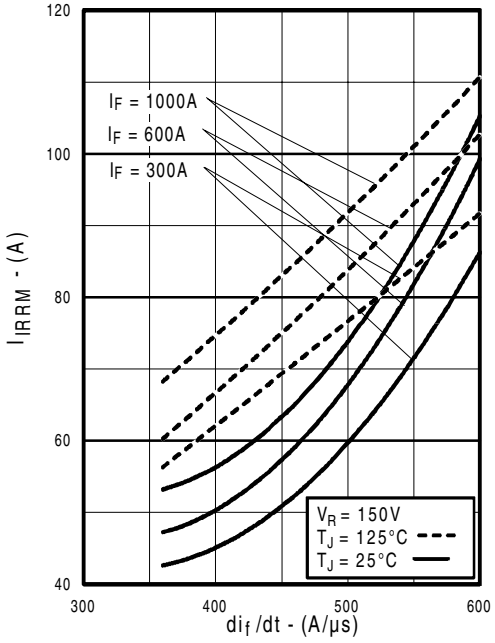


Fig. 16 - Typical Recovery Current vs. di_f/dt

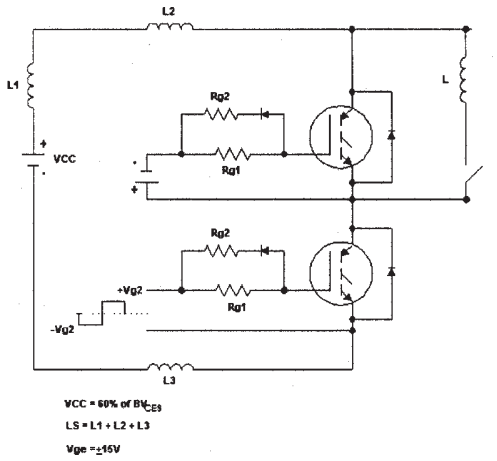


Fig. 17a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

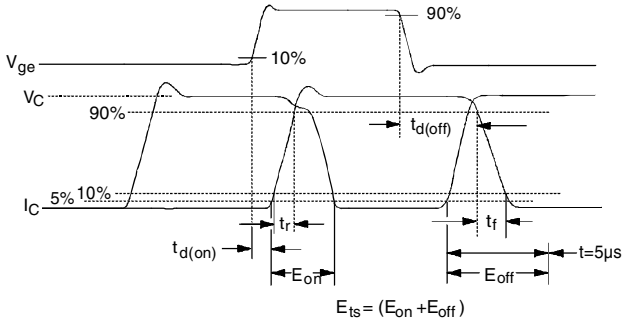


Fig. 17b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

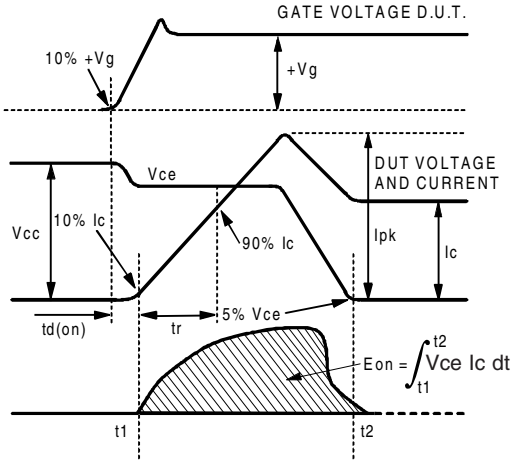


Fig. 17c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

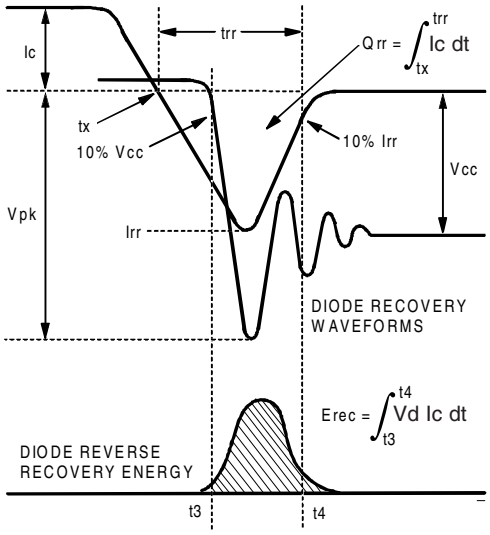


Fig. 17d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

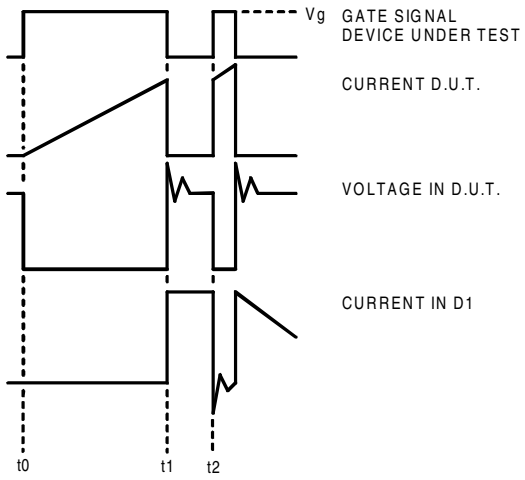


Figure 17e. Macro Waveforms for Figure 18a's Test Circuit

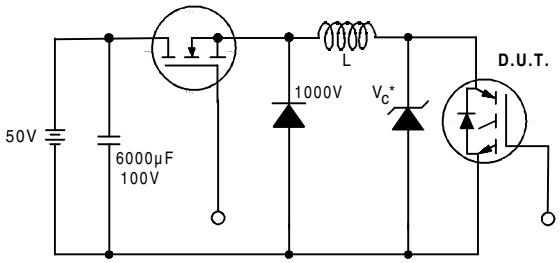


Figure 18. Clamped Inductive Load Test Circuit

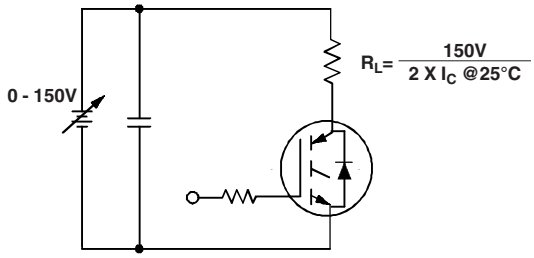


Figure 19. Pulsed Collector Current Test Circuit

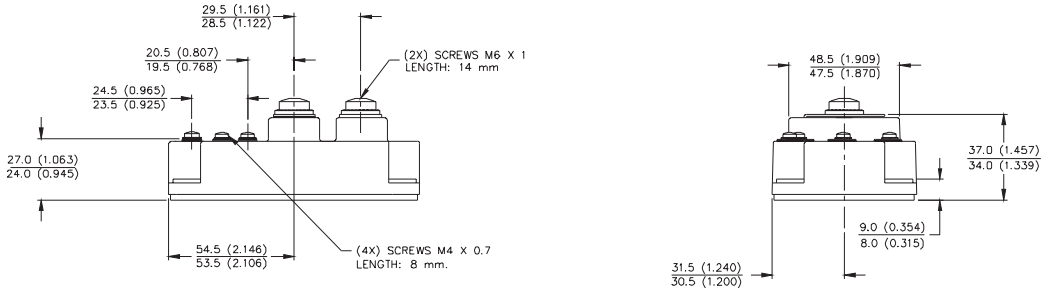
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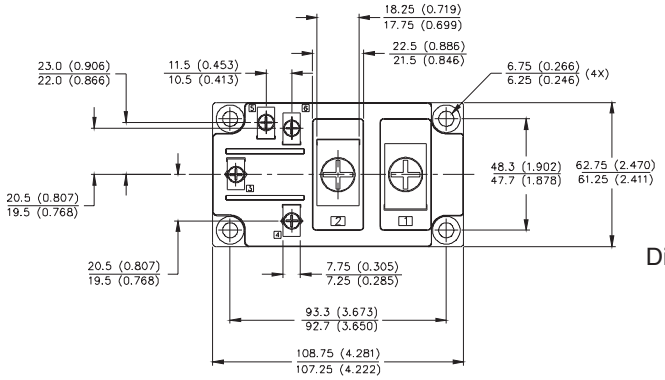
① Repetitive rating; V_{GE} = 17V, pulse width limited by max. junction temperature.

② See fig. 17

③ Pulse width 50µs; single shot.

Case Outline — DOUBLE INT-A-PAK





Dimensions are shown in millimeters (inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD - 91581A

International
IOR Rectifier

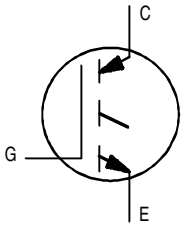
IRG4PC50S

INSULATED GATE BIPOLAR TRANSISTOR

Standard Speed IGBT

Features

- Standard: Optimized for minimum saturation voltage and low operating frequencies (< 1kHz)
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-247AC package



n-channel

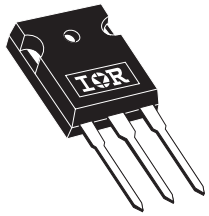
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.28V

@V_{GE} = 15V, I_C = 41A

Benefits

- Generation 4 IGBT's offer highest efficiency available
- IGBT's optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	70	A
I_C @ T_C = 100°C	Continuous Collector Current	41	
I_{CM}	Pulsed Collector Current ①	140	
I_{LM}	Clamped Inductive Load Current ②	140	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	20	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.64	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6.0 (0.21)	—	g (oz)

2/7/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.75	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.28	1.36	V	I_C = 41A V_{GE} = 15V
		—	1.62	—		I_C = 80A See Fig.2, 5
		—	1.28	—		I_C = 41A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-9.3	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	17	34	—	S	V_{CE} = 100V, I_C = 41A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	180	280	nC	I_C = 41A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	24	37		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	61	92		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	33	—	ns	
t_r	Rise Time	—	30	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	650	980		I_C = 41A, V_{CC} = 480V
t_f	Fall Time	—	400	600		V_{GE} = 15V, R_G = 5.0Ω
E_{on}	Turn-On Switching Loss	—	0.72	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	8.27	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	8.99	13		
$t_{d(on)}$	Turn-On Delay Time	—	31	—	ns	T_J = 150°C,
t_r	Rise Time	—	31	—		I_C = 41A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	1080	—		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	620	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	15	—	mJ	See Fig. 11, 14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	4100	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	250	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	48	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 5.0Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

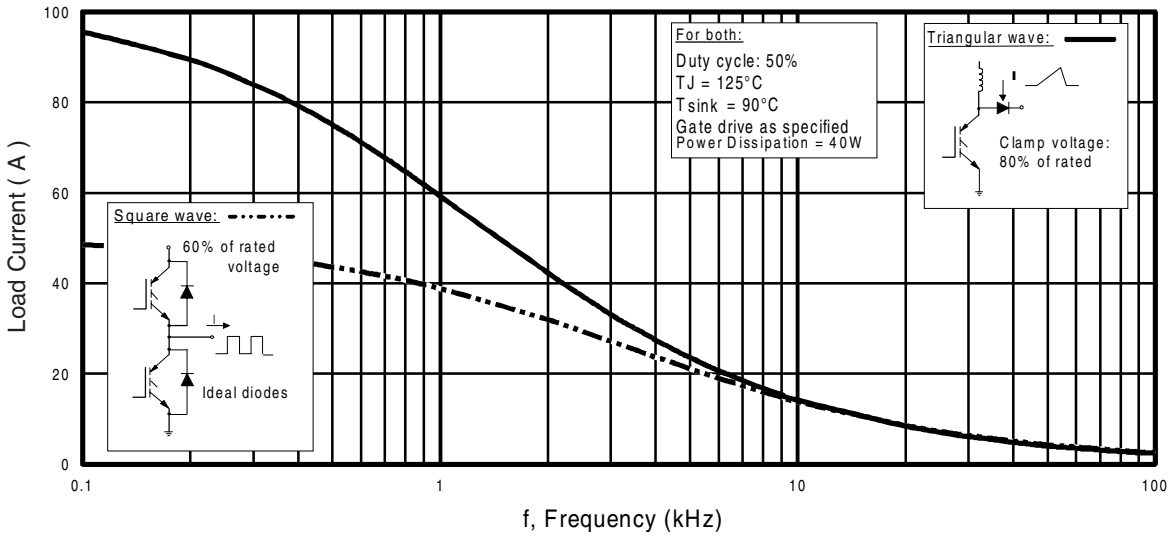


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

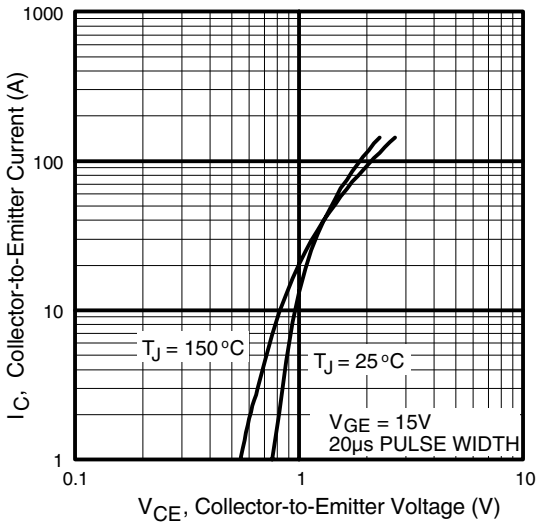


Fig. 2 - Typical Output Characteristics

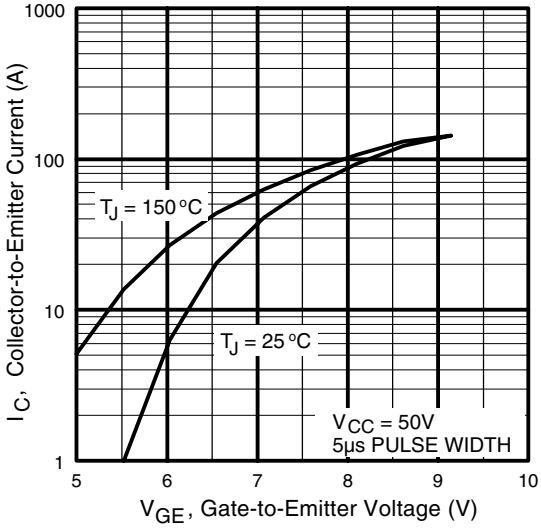


Fig. 3 - Typical Transfer Characteristics

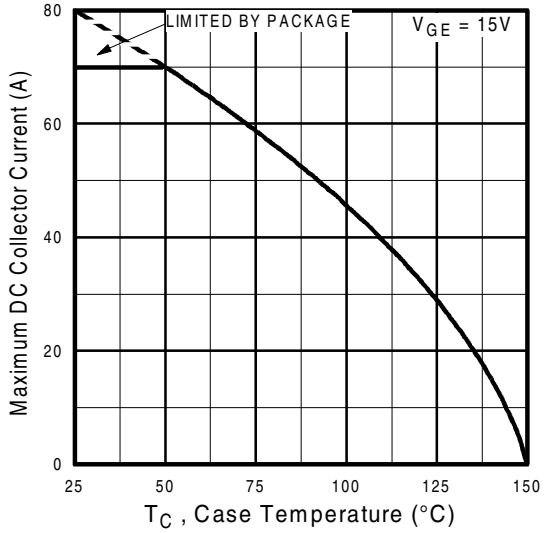


Fig. 4 - Maximum Collector Current vs. Case Temperature

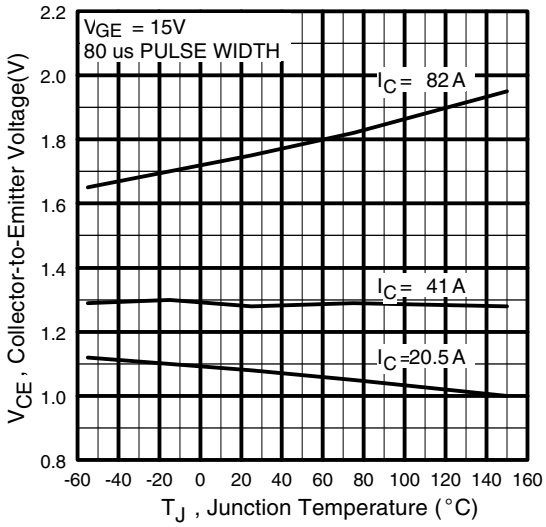


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

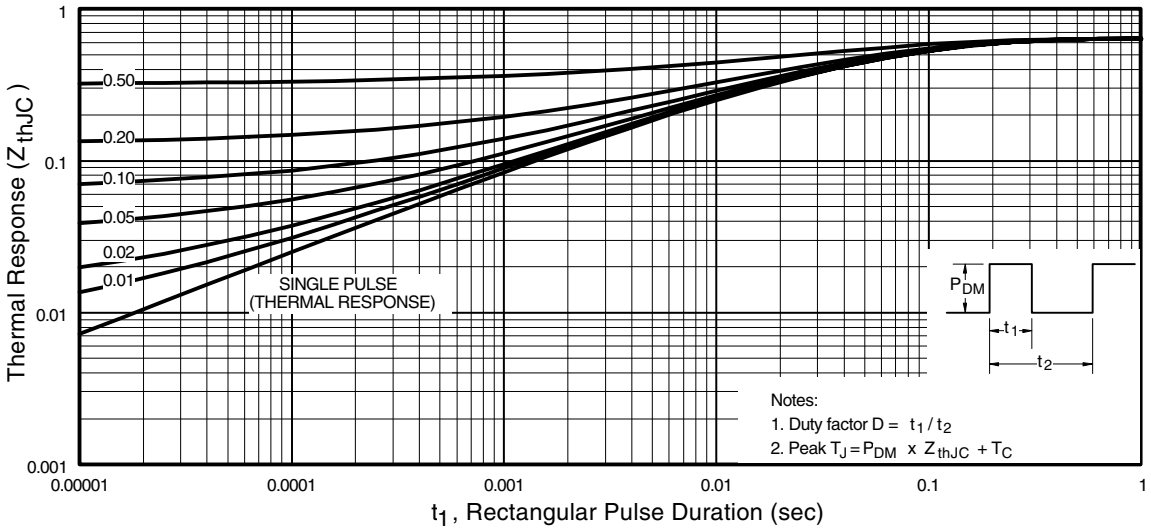


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

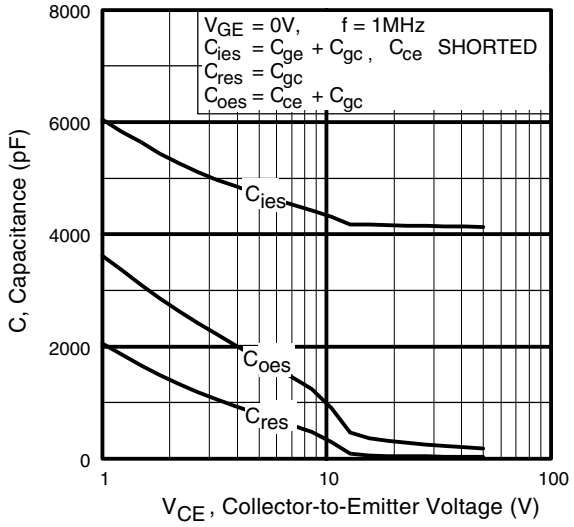


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

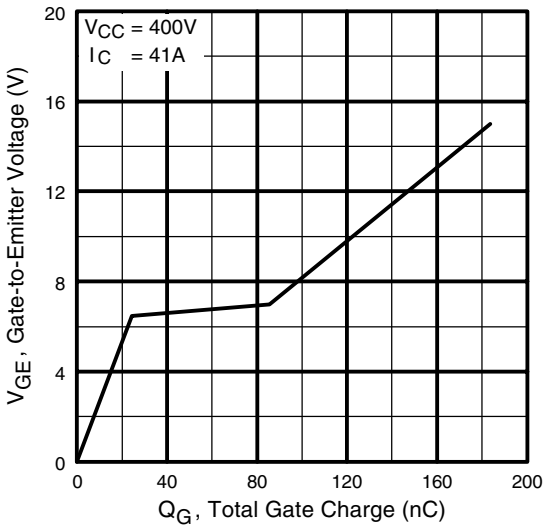


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

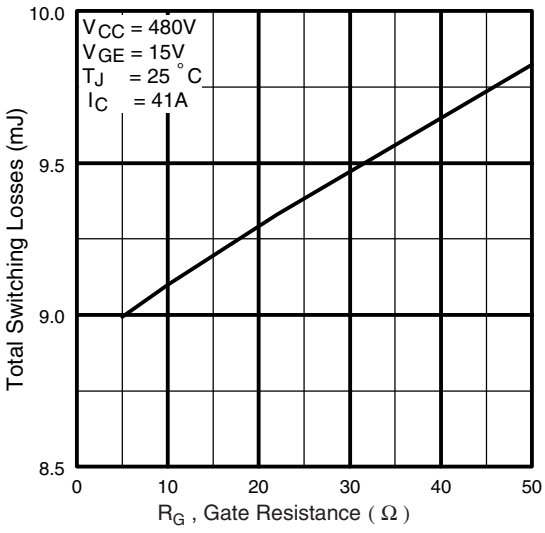


Fig. 9 - Typical Switching Losses vs. Gate Resistance

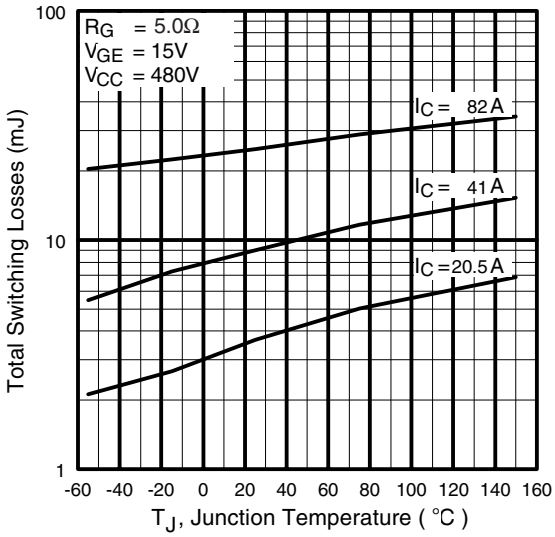


Fig. 10 - Typical Switching Losses vs. Junction Temperature

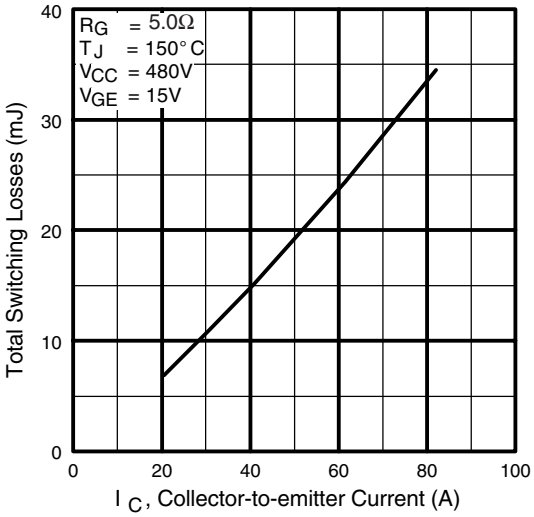


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

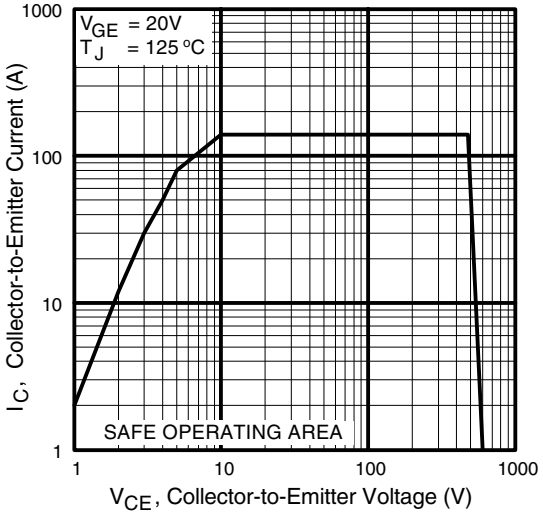


Fig. 12 - Turn-Off SOA

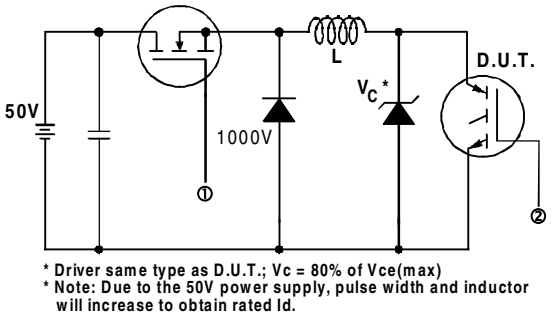


Fig. 13a - Clamped Inductive Load Test Circuit

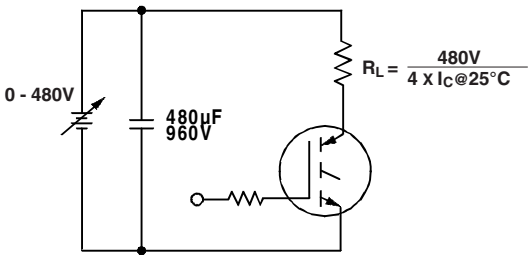


Fig. 13b - Pulsed Collector Current Test Circuit

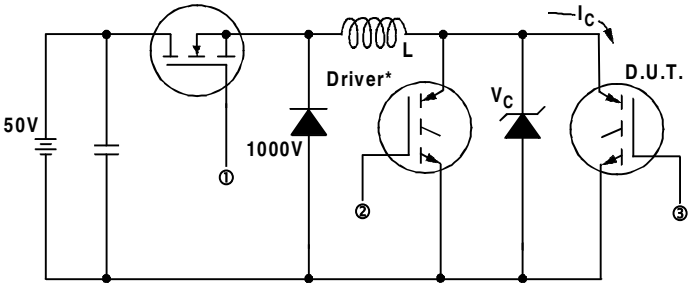


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

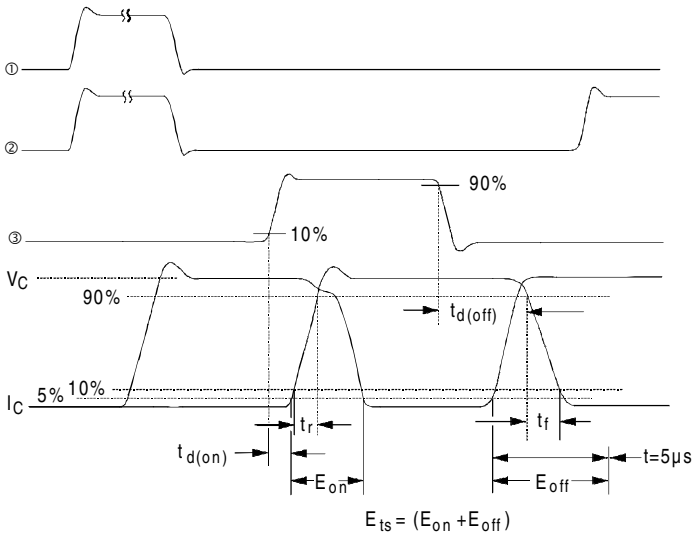
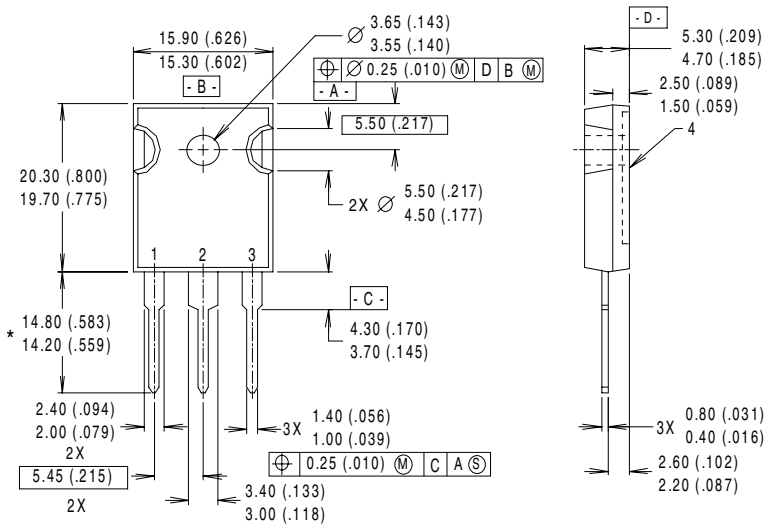


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 6/00

PD 91468C

International
IOR Rectifier

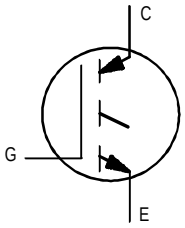
IRG4PC50F

INSULATED GATE BIPOLAR TRANSISTOR

Fast Speed IGBT

Features

- Optimized for medium operating frequencies (1-5 kHz in hard switching, >20 kHz in resonant mode).
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-247AC package



n-channel

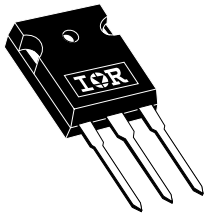
$V_{CES} = 600V$

$V_{CE(on)\ typ.} = 1.45V$

$@V_{GE} = 15V, I_C = 39A$

Benefits

- Generation 4 IGBT's offer highest efficiency available
- IGBT's optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	70	A
I_C @ T_C = 100°C	Continuous Collector Current	39	
I_{CM}	Pulsed Collector Current ①	280	
I_{LM}	Clamped Inductive Load Current ②	280	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	20	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.64	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

12/30/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.62	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.45	1.6	V	I_C = 39A V_{GE} = 15V
		—	1.79	—		I_C = 70A See Fig.2, 5
		—	1.53	—		I_C = 39A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-14	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	21	30	—	S	V_{CE} = 100V, I_C = 39A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	2000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	190	290	nC	I_C = 39A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	28	42		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	65	97		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	31	—	ns	
t_r	Rise Time	—	25	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	240	350		I_C = 39A, V_{CC} = 480V
t_f	Fall Time	—	130	190		V_{GE} = 15V, R_G = 5.0Ω
E_{on}	Turn-On Switching Loss	—	0.37	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	2.1	—		See Fig. 10, 11, 13, 14
E_{ts}	Total Switching Loss	—	2.47	3.0		
$t_{d(on)}$	Turn-On Delay Time	—	28	—	ns	T_J = 150°C,
t_r	Rise Time	—	24	—		I_C = 39A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	390	—		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	230	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	5.0	—	mJ	See Fig. 13, 14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	4100	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	250	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	49	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 5.0Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

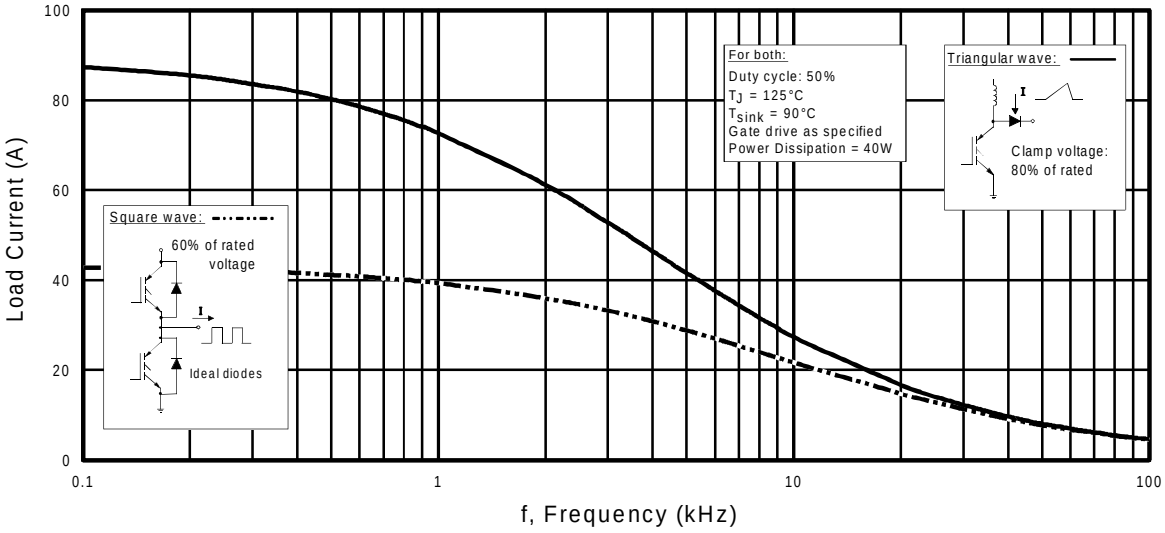


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

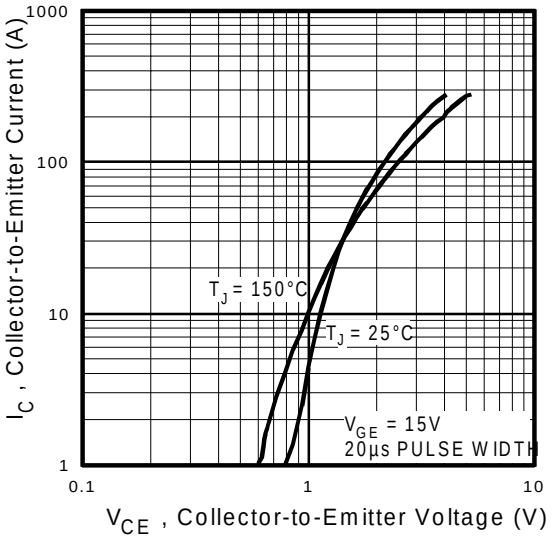


Fig. 2 - Typical Output Characteristics

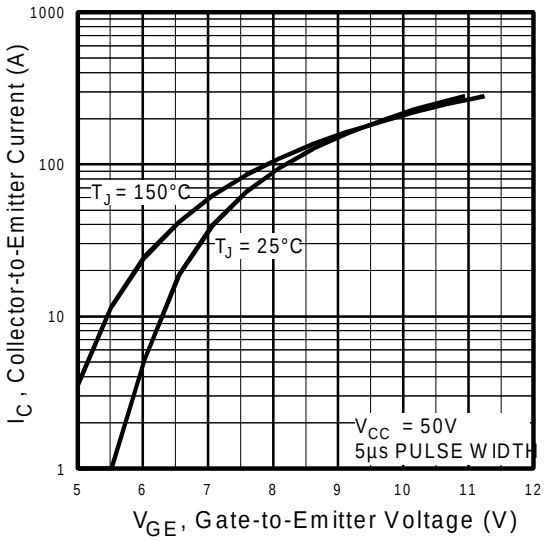


Fig. 3 - Typical Transfer Characteristics

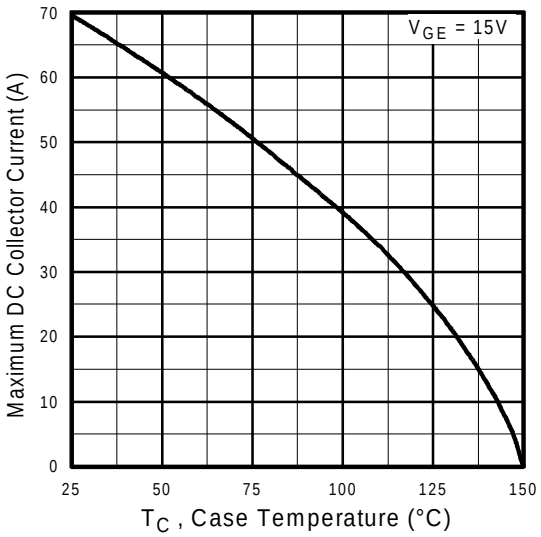


Fig. 4 - Maximum Collector Current vs. Case Temperature

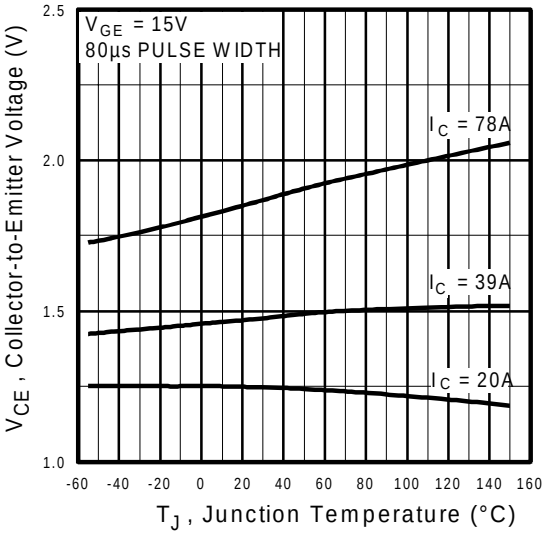


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

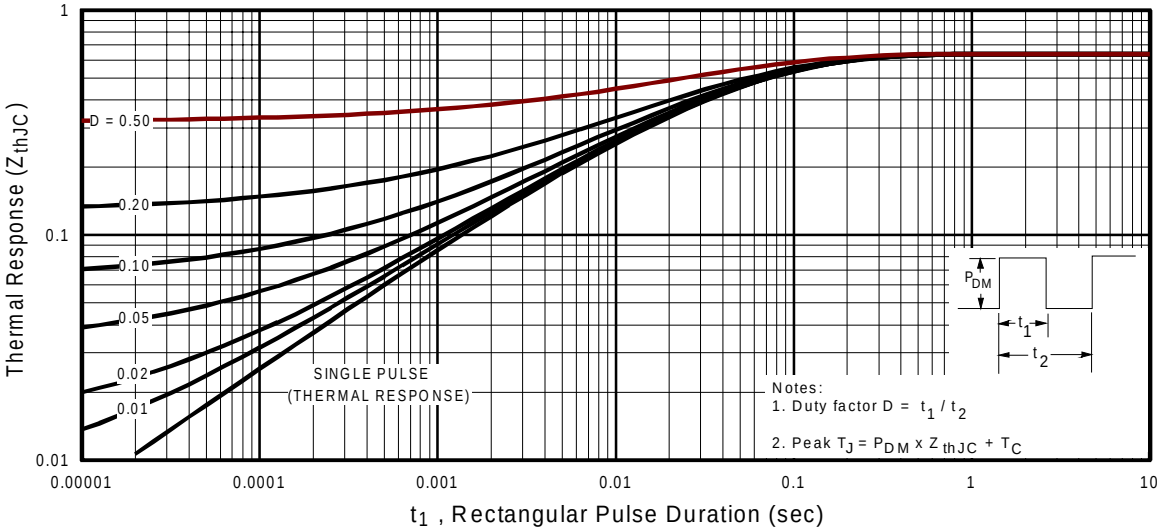


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

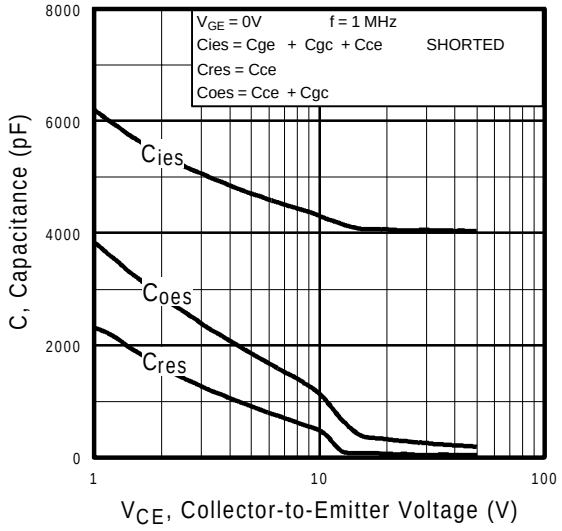


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

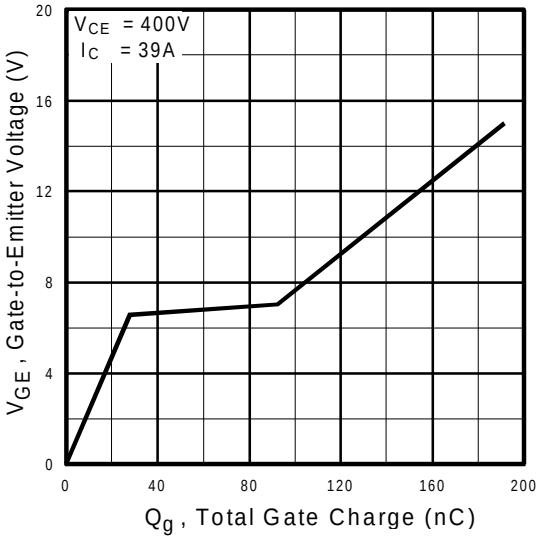


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

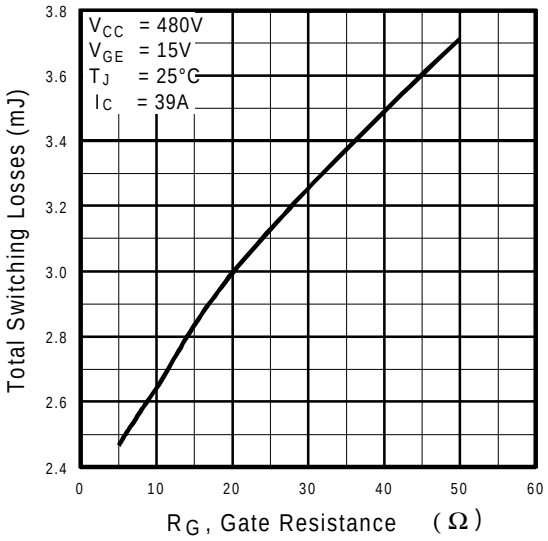


Fig. 9 - Typical Switching Losses vs. Gate Resistance

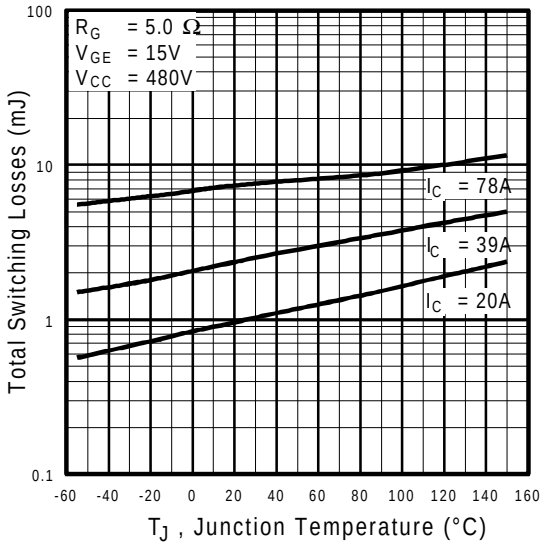


Fig. 10 - Typical Switching Losses vs. Junction Temperature

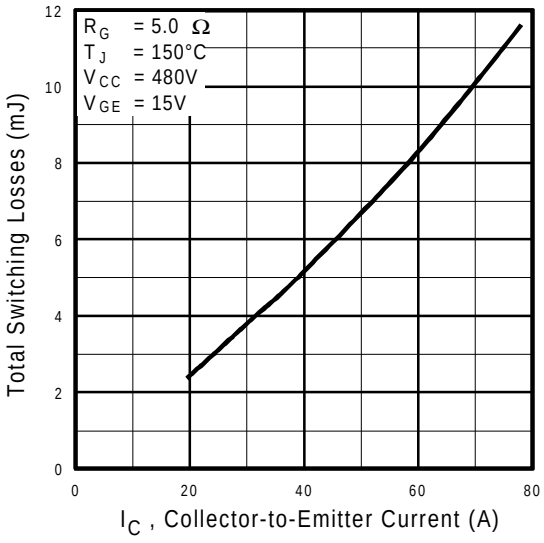


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

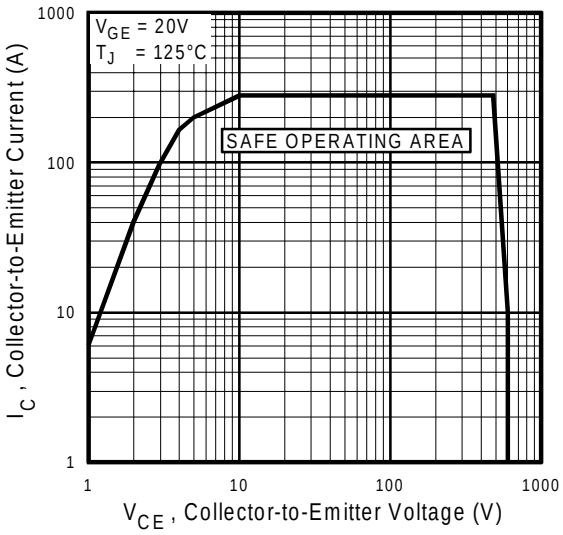


Fig. 12 - Turn-Off SOA

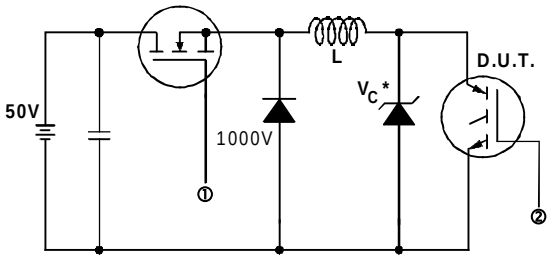


Fig. 13a - Clamped Inductive Load Test Circuit

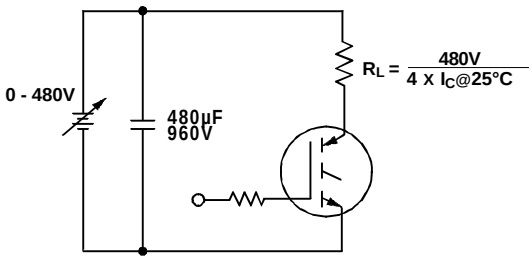


Fig. 13b - Pulsed Collector Current Test Circuit

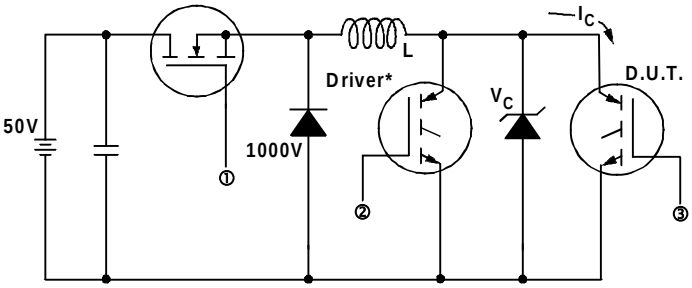


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

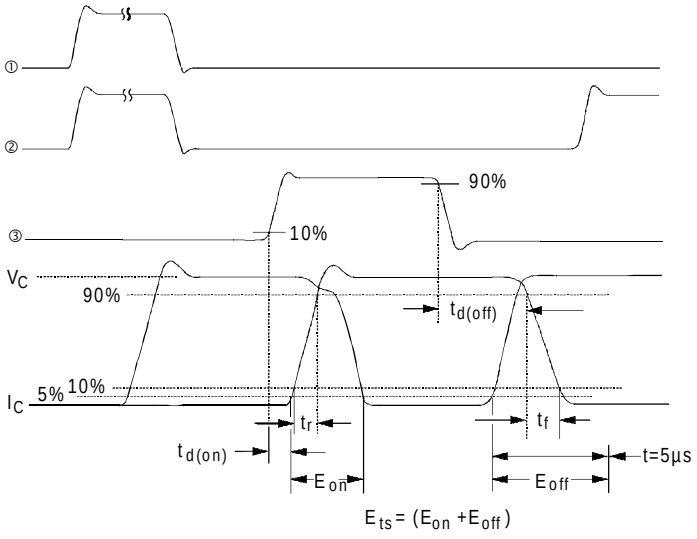
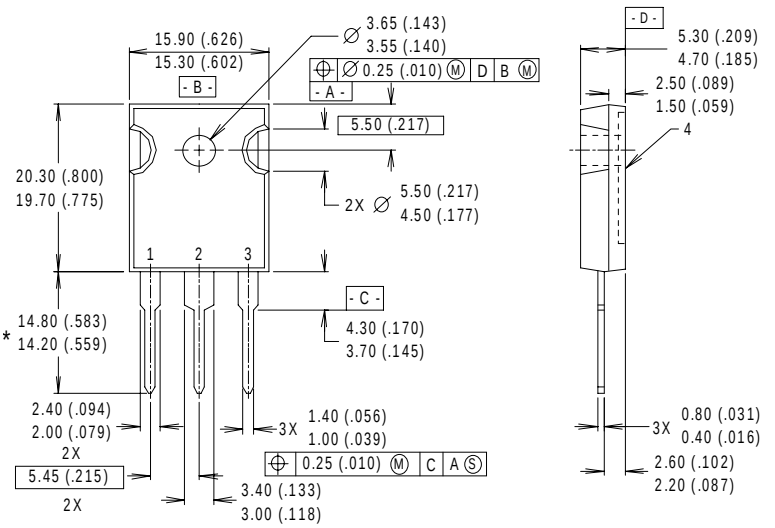


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
Data and specifications subject to change without notice. 12/00

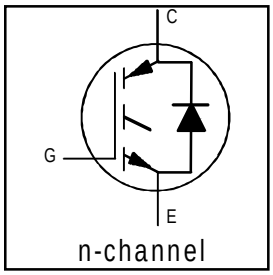
PD 91469B

International
IOR Rectifier

IRG4PC50FD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Fast CoPack IGBT



n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.45V

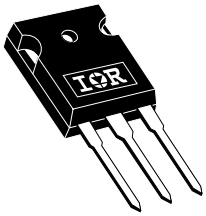
@V_{GE} = 15V, I_C = 39A

Features

- Fast: Optimized for medium operating frequencies (1-5 kHz in hard switching, >20 kHz in resonant mode).
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-247AC package

Benefits

- Generation -4 IGBT's offer highest efficiencies available
- IGBT's optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBT's . Minimized recovery characteristics require less/no snubbing
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	70	A
I_C @ T_C = 100°C	Continuous Collector Current	39	
I_{CM}	Pulsed Collector Current ①	280	
I_{LM}	Clamped Inductive Load Current ②	280	
I_F @ T_C = 100°C	Diode Continuous Forward Current	25	
I_{FM}	Diode Maximum Forward Current	280	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	------	------	0.64	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	------	------	0.83	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	------	0.24	------	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	-----	-----	40	
Wt	Weight	------	6 (0.21)	------	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	----	----	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	----	0.62	----	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	----	1.45	1.6	V	I_C = 39A V_{GE} = 15V
		----	1.79	----		I_C = 70A See Fig. 2, 5
		----	1.53	----		I_C = 39A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	----	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	----	-14	----	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	21	30	----	S	V_{CE} = 100V, I_C = 39A
I_{CES}	Zero Gate Voltage Collector Current	----	----	250	µA	V_{GE} = 0V, V_{CE} = 600V
		----	----	6500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	----	1.3	1.7	V	I_C = 25A See Fig. 13
		----	1.2	1.5		I_C = 25A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	----	----	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	----	190	290		I_C = 39A
Qge	Gate - Emitter Charge (turn-on)	----	28	42	nC	V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	----	65	97		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	----	55	----		T_J = 25°C
t_r	Rise Time	----	25	----	ns	I_C = 39A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	240	360		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	----	140	210		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	----	1.5	----		diode reverse recovery.
E_{off}	Turn-Off Switching Loss	----	2.4	----	mJ	See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	----	3.9	5.0		
$t_{d(on)}$	Turn-On Delay Time	----	59	----		T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	----	27	----	ns	I_C = 39A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	400	----		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	----	260	----		Energy losses include "tail" and
E_{ts}	Total Switching Loss	----	6.5	----	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	----	13	----	nH	Measured 5mm from package
C_{ies}	Input Capacitance	----	4100	----		V_{GE} = 0V
C_{oes}	Output Capacitance	----	250	----	pF	V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	----	49	----		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	----	50	75	ns	T_J = 25°C See Fig.
		----	105	160		T_J = 125°C 14 I_F = 25A
I_{rr}	Diode Peak Reverse Recovery Current	----	4.5	10	A	T_J = 25°C See Fig.
		----	8.0	15		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	----	112	375	nC	T_J = 25°C See Fig.
		----	420	1200		T_J = 125°C 16 di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	----	250	----	A/µs	T_J = 25°C See Fig.
	During t_b	----	160	----		T_J = 125°C 17

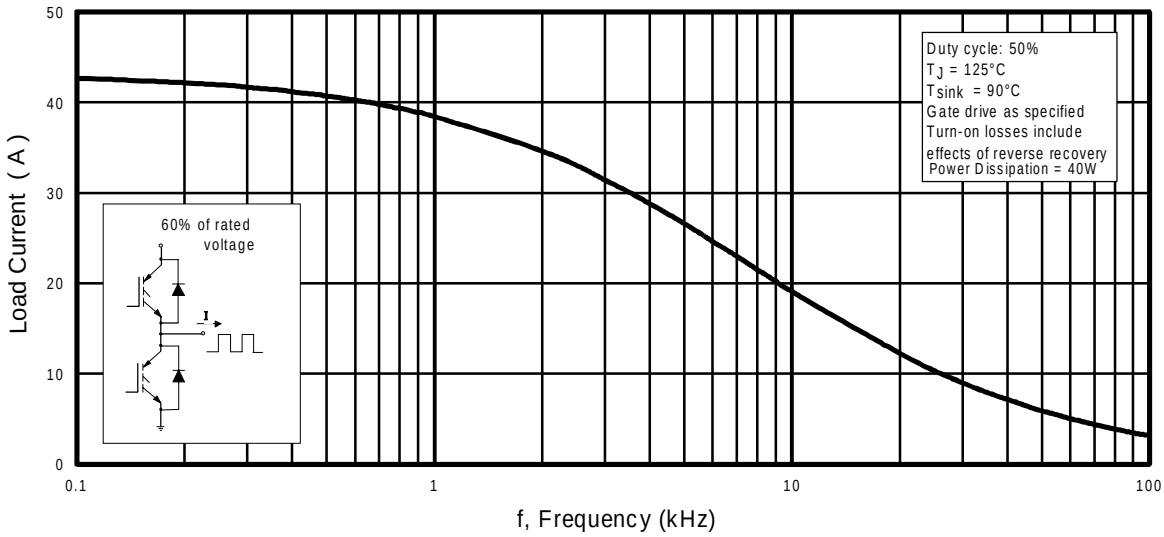


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

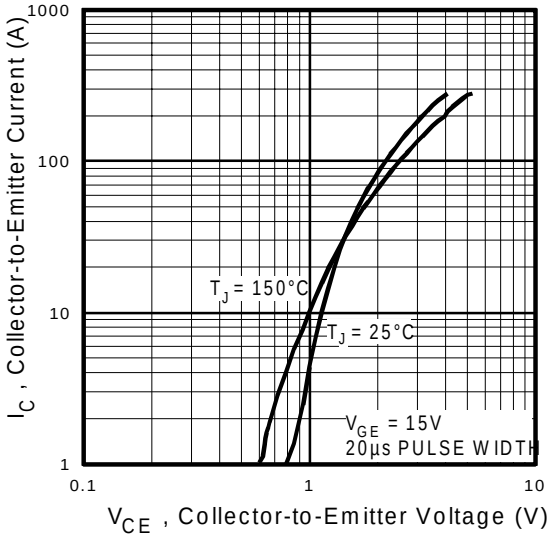


Fig. 2 - Typical Output Characteristics

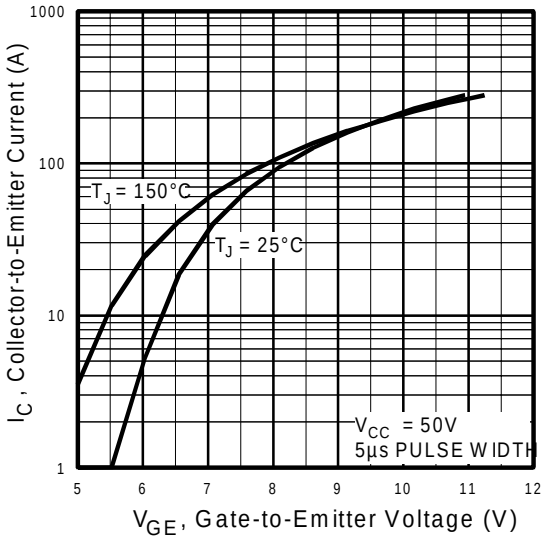


Fig. 3 - Typical Transfer Characteristics

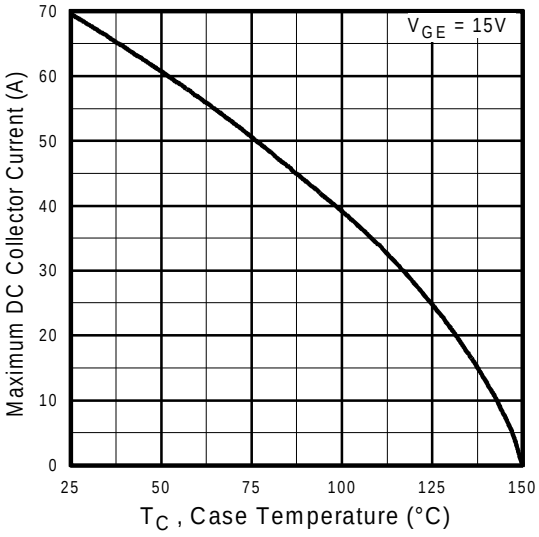


Fig. 4 - Maximum Collector Current vs. Case Temperature

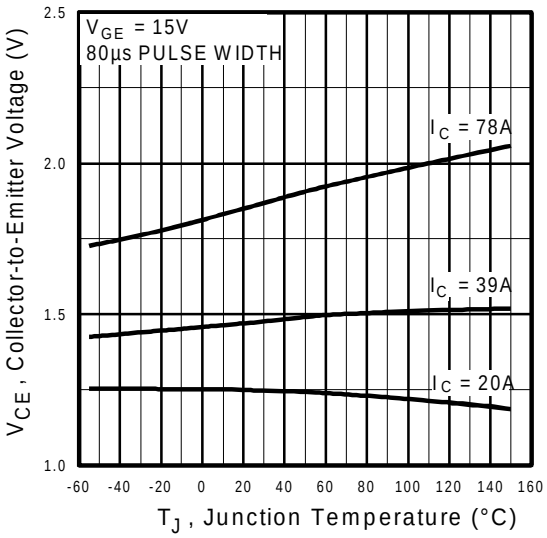


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

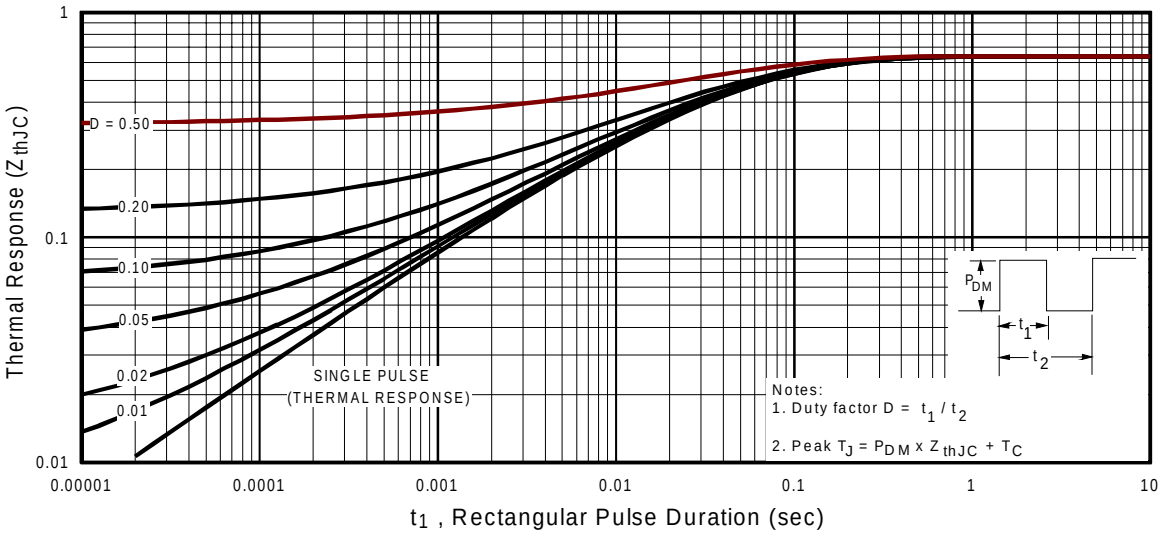


Fig. 6 - Maximum IGBT Effective Transient Thermal Impedance, Junction-to-Case

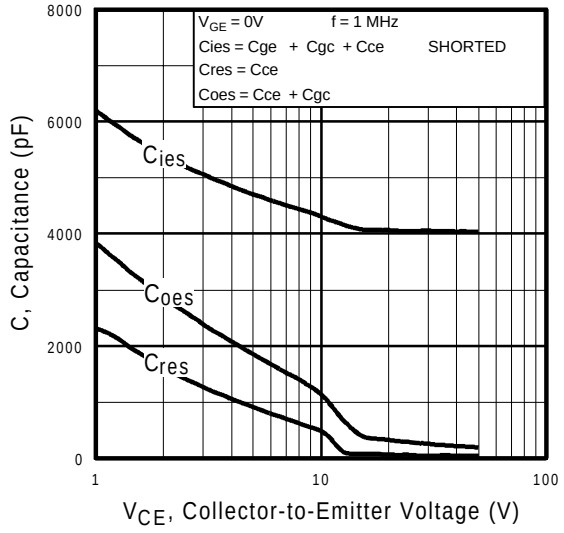


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

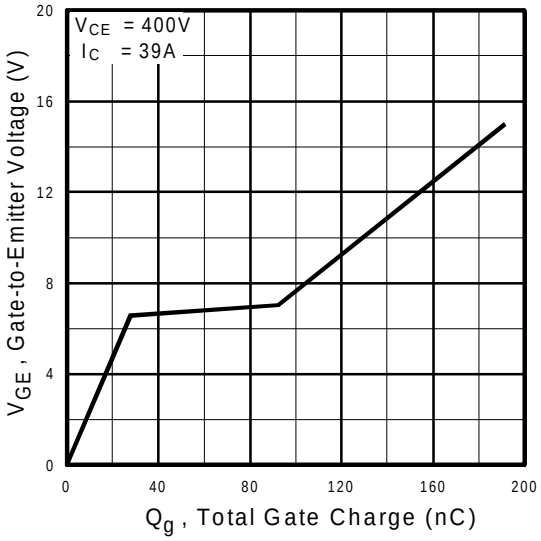


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

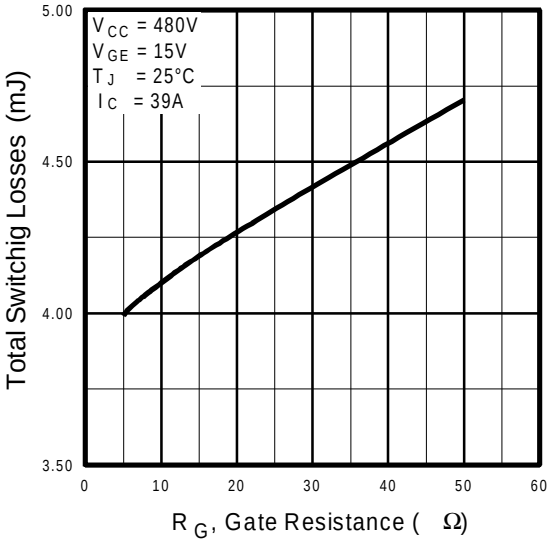


Fig. 9 - Typical Switching Losses vs. Gate Resistance

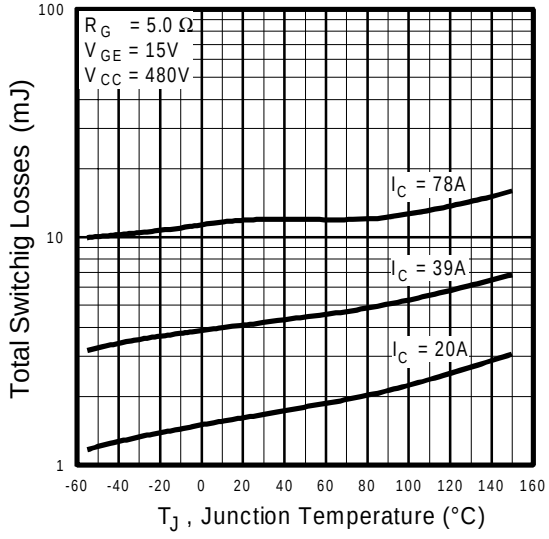


Fig. 10 - Typical Switching Losses vs. Junction Temperature

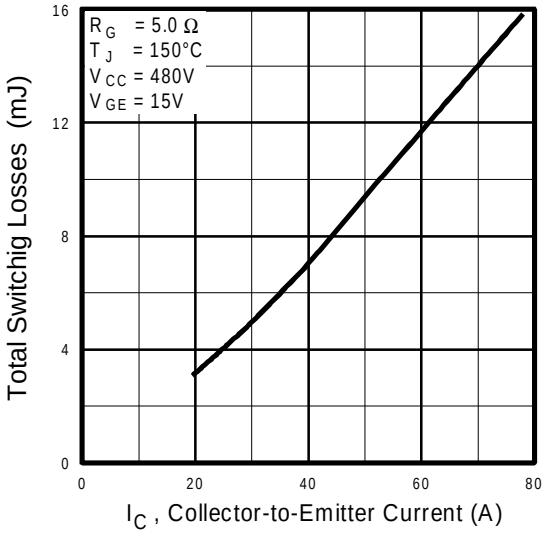


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

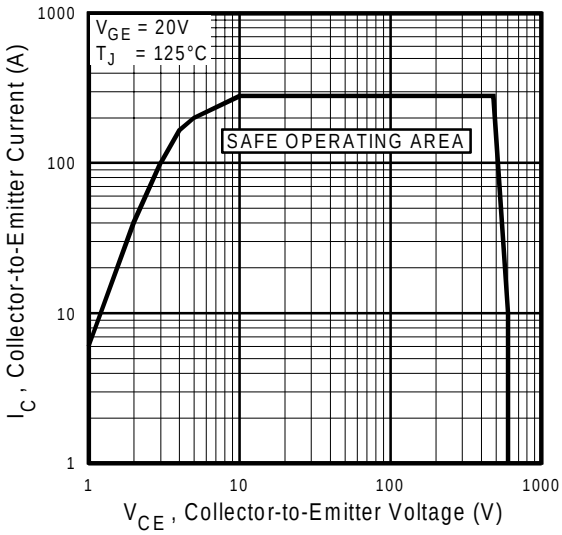


Fig. 12 - Turn-Off SOA

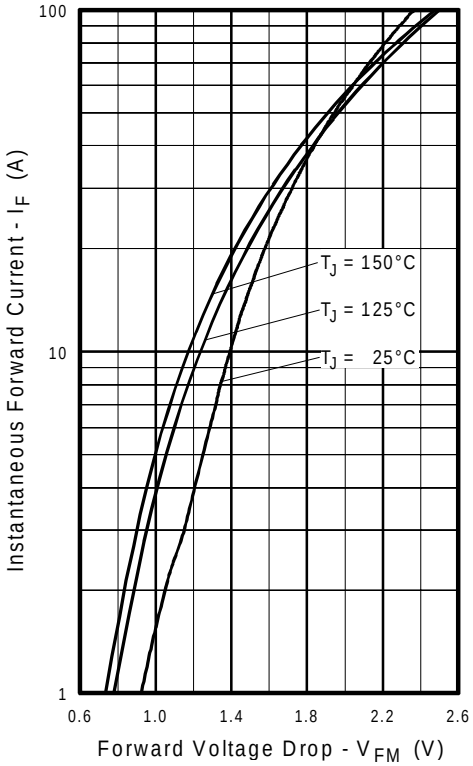


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

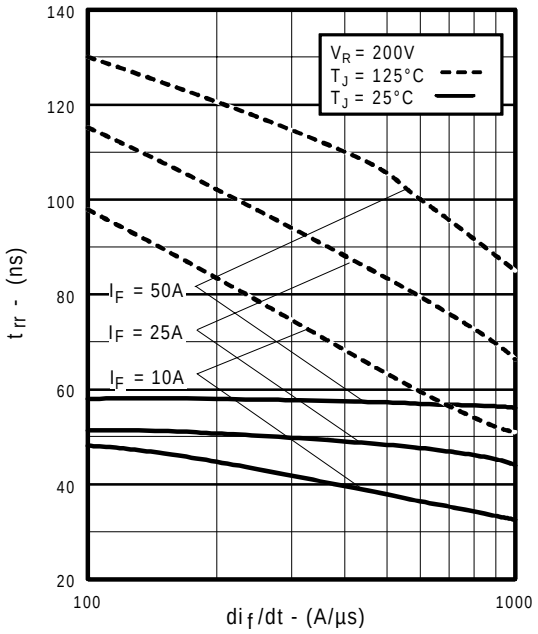


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

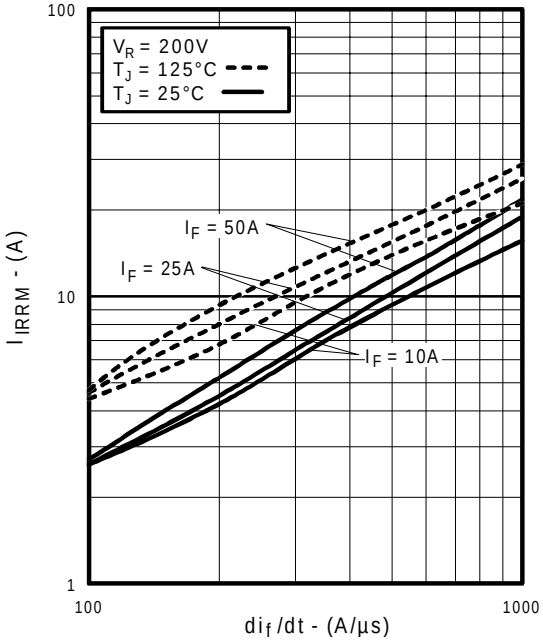


Fig. 15 - Typical Recovery Current vs. di_f/dt

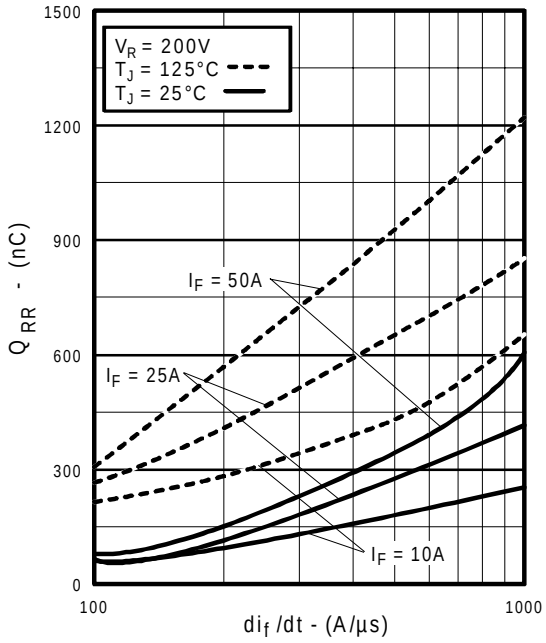


Fig. 16 - Typical Stored Charge vs. di_f/dt

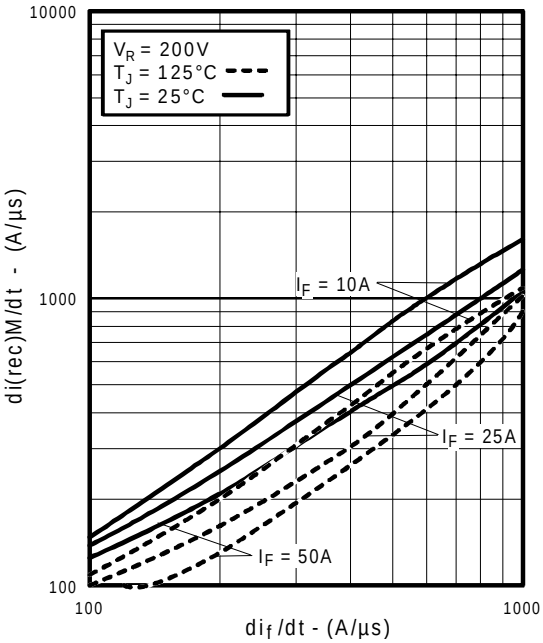


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

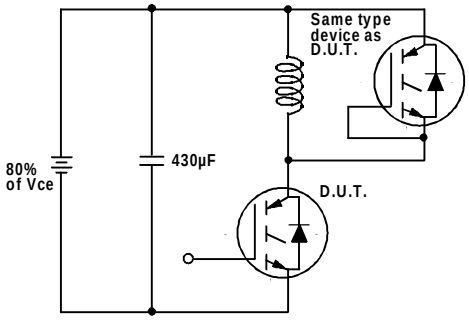


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

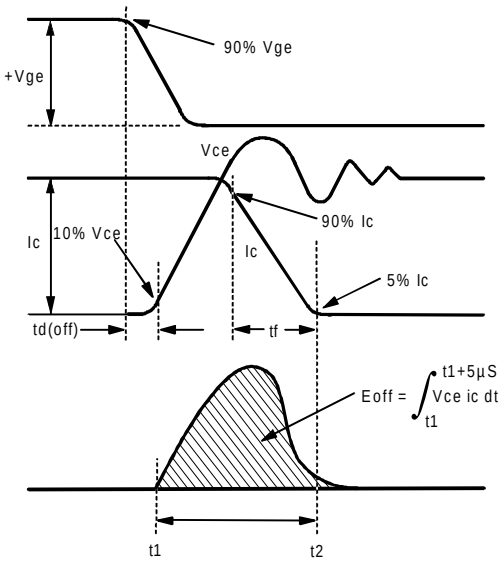


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

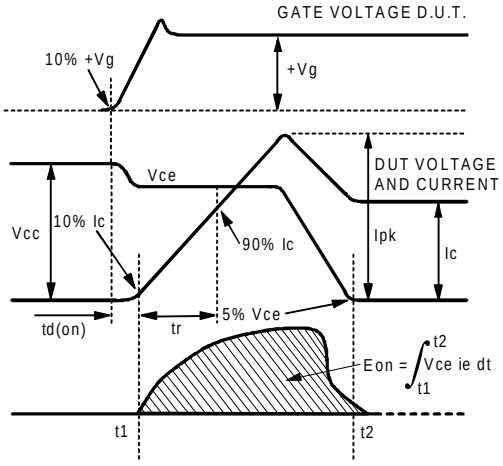


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

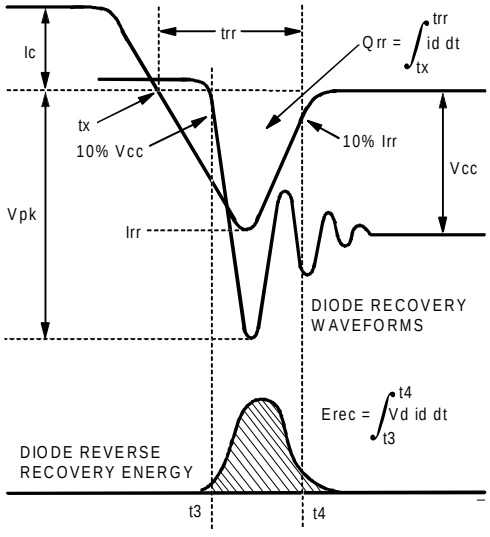


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

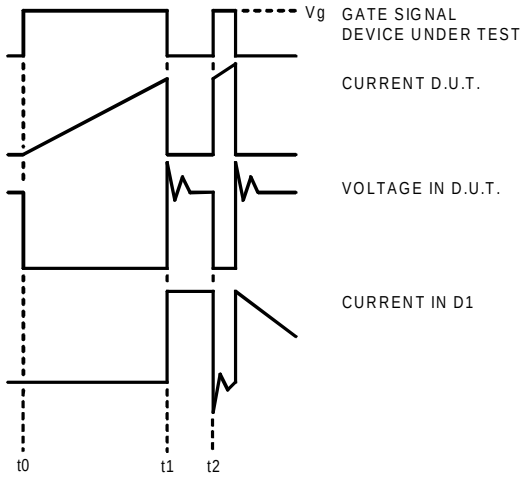


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

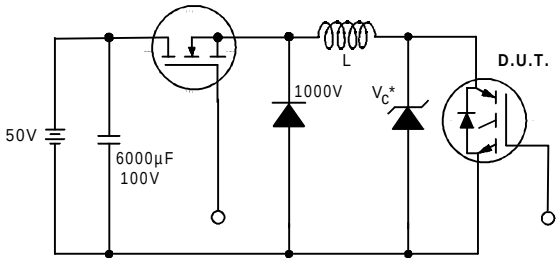


Figure 19. Clamped Inductive Load Test Circuit

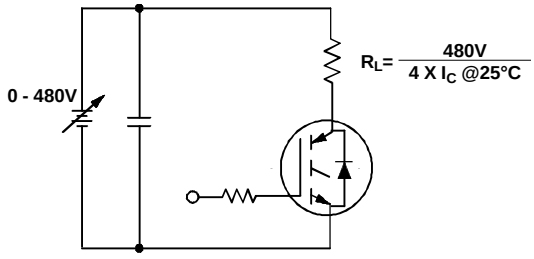


Figure 20. Pulsed Collector Current Test Circuit

Notes:

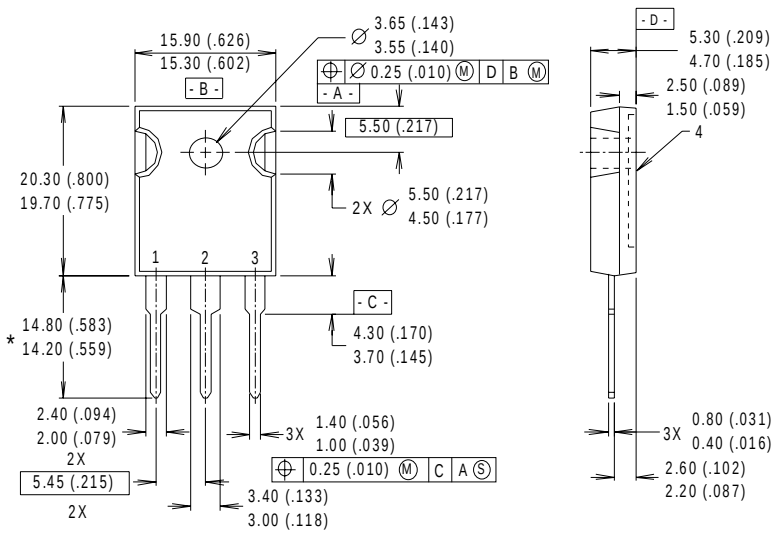
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 5.0Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
Data and specifications subject to change without notice. 12/00

PD - 91683A

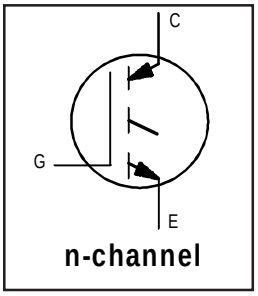
International
IOR Rectifier

PRELIMINARY

IRG4PSC71K

Short Circuit Rated
UltraFast IGBT

INSULATED GATE BIPOLAR TRANSISTOR



n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.83V

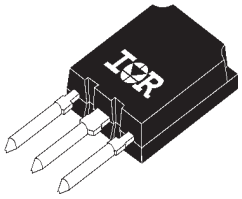
@V_{GE} = 15V, I_C = 60A

Features

- Hole-less clip/pressure mount package compatible with TO-247 and TO-264, with reinforced pins
- High abort circuit rating IGBTs, optimized for motorcontrol
- Minimum switching losses combined with low conduction losses
- Tightest parameter distribution
- Creepage distance increased to 5.35mm

Benefits

- Highest current rating IGBT
- Maximum power density, twice the power handling of the TO-247, less space than TO-264



SUPER - 247

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	85⑥	A
I_C @ T_C = 100°C	Continuous Collector Current	60	
I_{CM}	Pulsed Collector Current ①	200	
I_{LM}	Clamped Inductive Load Current ②	200	
t_{SC}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	180	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	350	W
P_D @ T_C = 100°C	Maximum Power Dissipation	140	
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	

Thermal Resistance\ Mechanical

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.36	°C/W
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	38	
	Recommended Clip Force	20.0(2.0)	—	—	N (kgf)
	Weight	—	6 (0.21)	—	g (oz)

5/11/99

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.5	—	V/°C	V_{GE} = 0V, I_C = 10mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.83	2.3	V	I_C = 60A V_{GE} = 15V
		—	2.20	—		I_C = 100A See Fig.2, 5
		—	1.81	—		I_C = 60A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-8.0	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.5mA
g_{fe}	Forward Transconductance ⑤	31	46	—	S	V_{CE} = 50V, I_C = 60A
I_{CES}	Zero Gate Voltage Collector Current	—	—	500	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	5.0	mA	V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	340	510	nC	I_C = 60A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	44	66		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	160	240		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	34	—	ns	
t_r	Rise Time	—	54	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	251	377		I_C = 60A, V_{CC} = 480V
t_f	Fall Time	—	89	133		V_{GE} = 15V, R_G = 5.0Ω
E_{on}	Turn-On Switching Loss	—	0.79	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	1.98	—		and diode reverse recovery
E_{ts}	Total Switching Loss	—	2.77	3.1		See Fig. 9,10,18
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 360V, T_J = 125°C
						V_{GE} = 15V, R_G = 5.0Ω
$t_{d(on)}$	Turn-On Delay Time	—	37	—	ns	T_J = 150°C, See Fig. 10,11,18
t_r	Rise Time	—	56	—		I_C = 60A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	356	—		V_{GE} = 15V, R_G = 5.0Ω,
t_f	Fall Time	—	177	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	5.5	—	mJ	and diode reverse recovery
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	6900	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	730	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	190	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 5.0Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

⑥ Current limited by the package, (Die current = 100A)

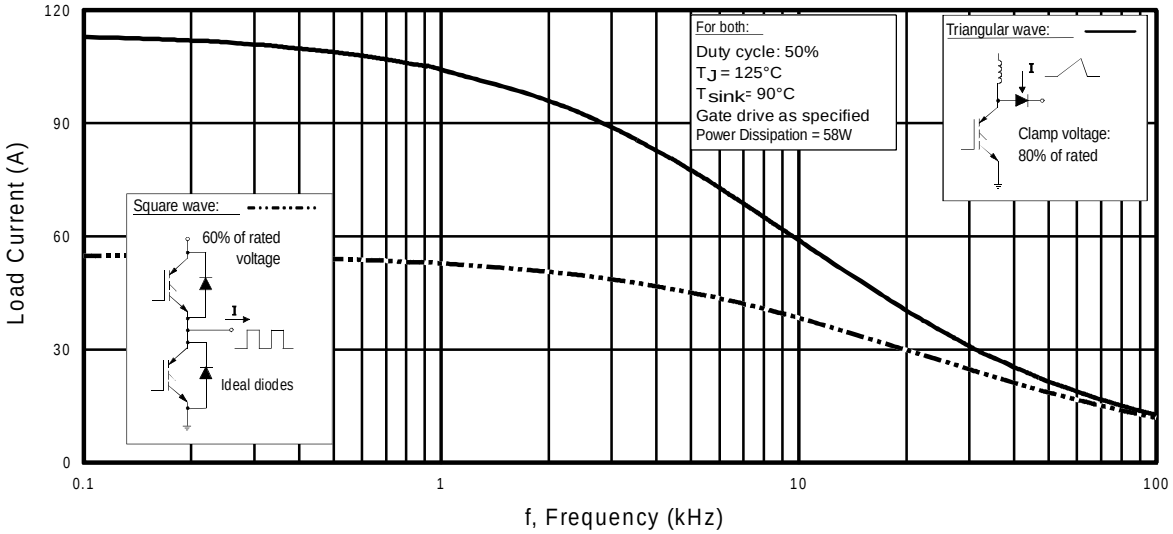


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

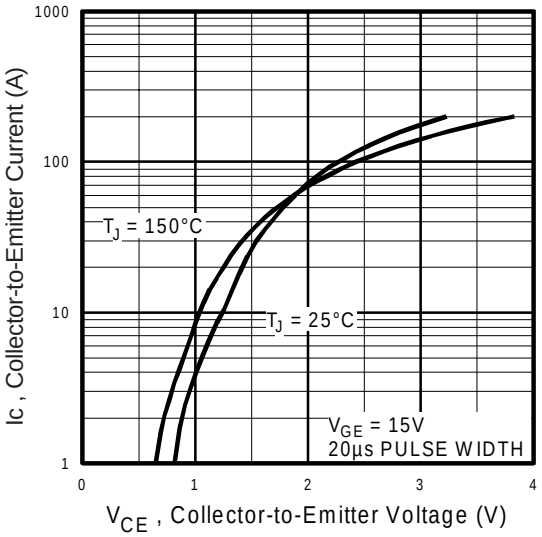


Fig. 2 - Typical Output Characteristics

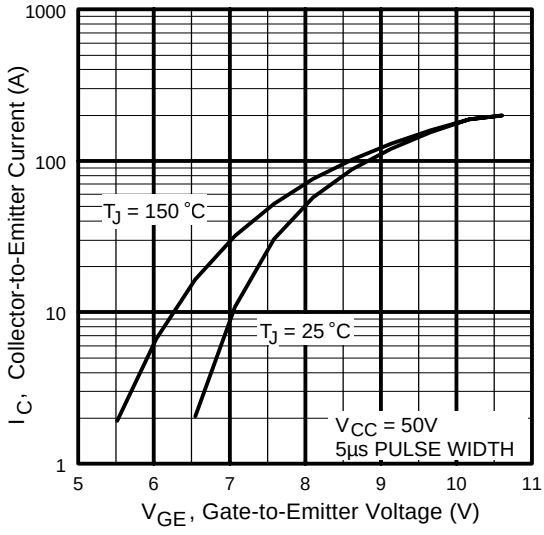


Fig. 3 - Typical Transfer Characteristics

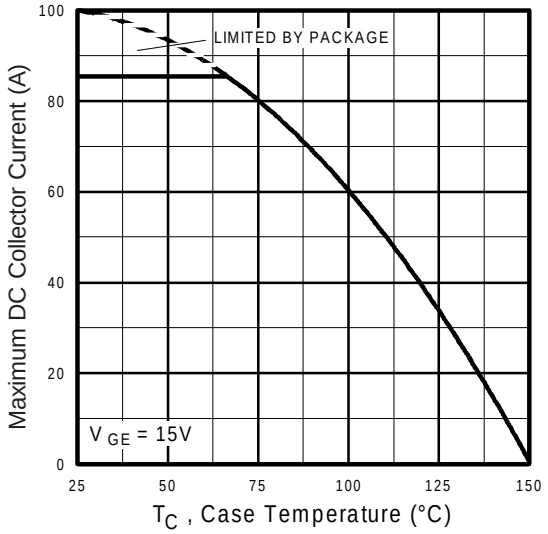


Fig. 4 - Maximum Collector Current vs. Case Temperature

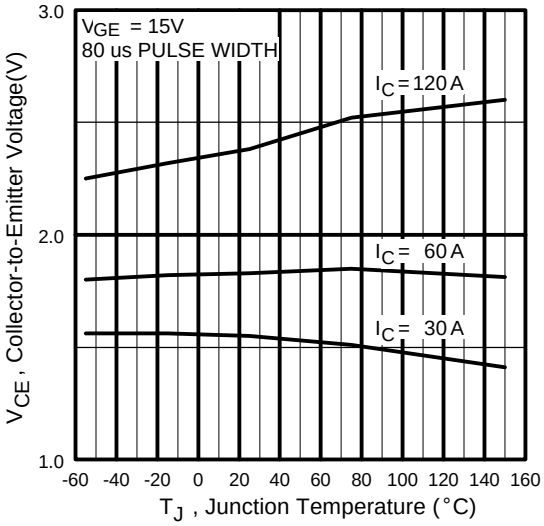


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

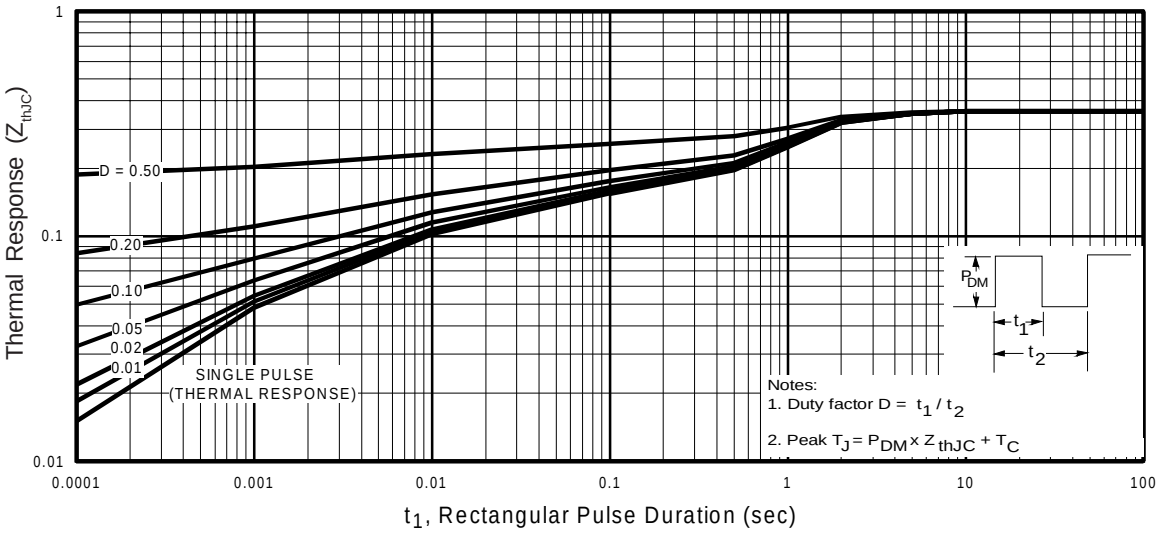


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

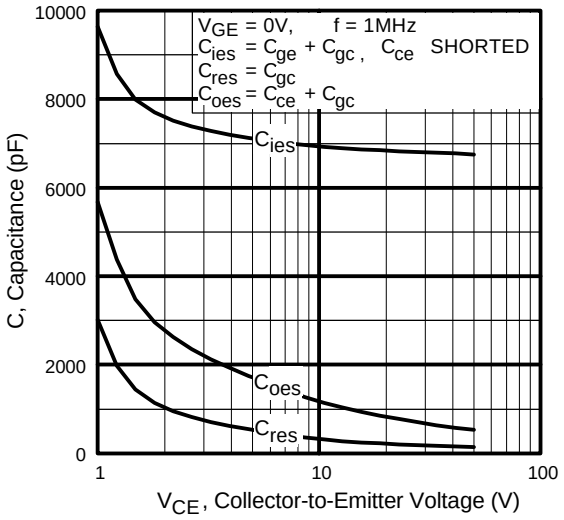


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

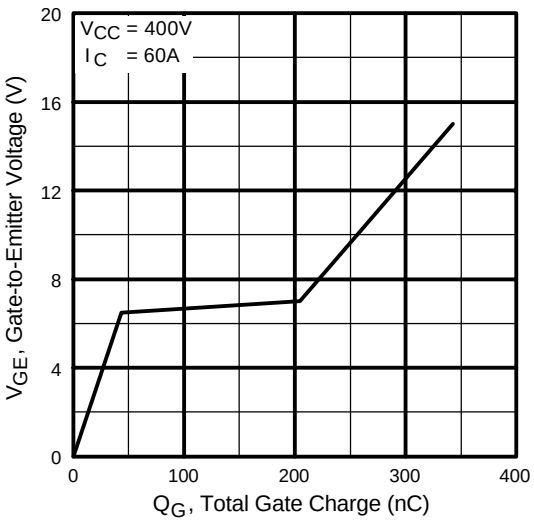


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

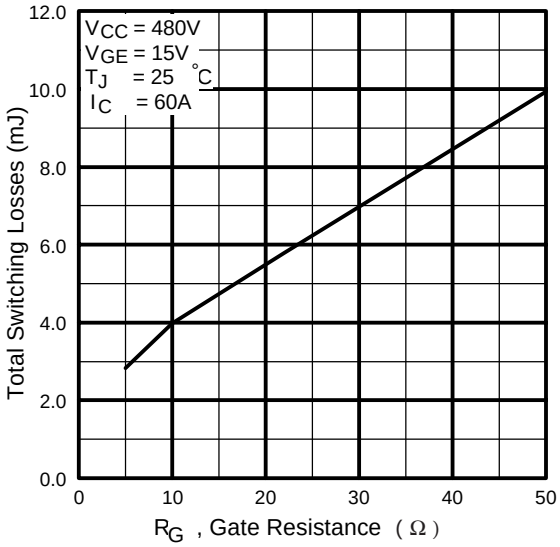


Fig. 9 - Typical Switching Losses vs. Gate Resistance

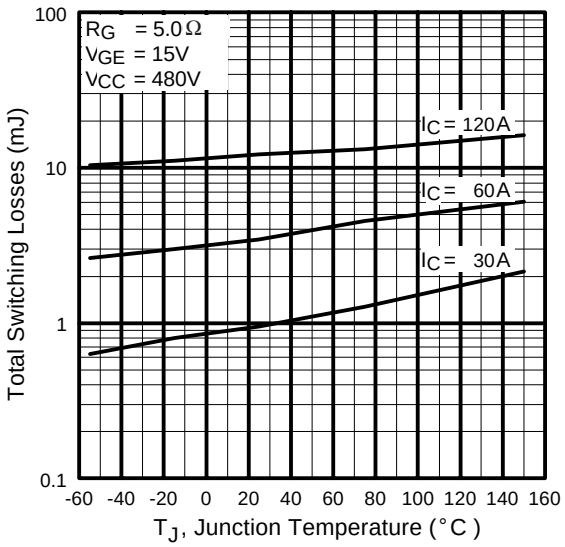


Fig. 10 - Typical Switching Losses vs. Junction Temperature

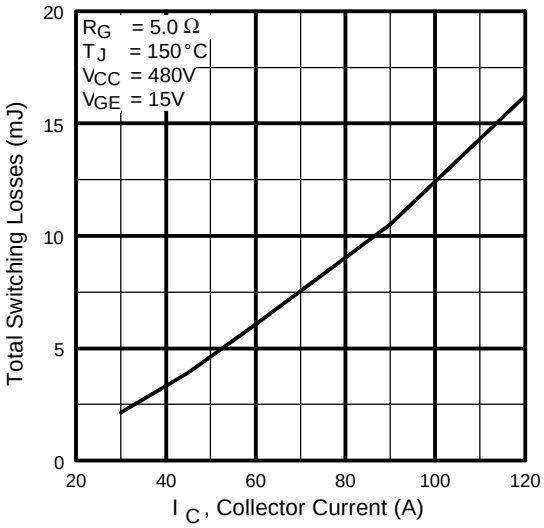


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

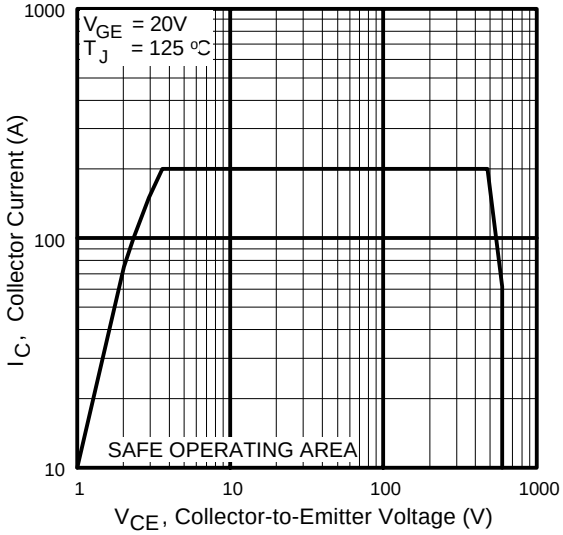


Fig. 12 - Turn-Off SOA

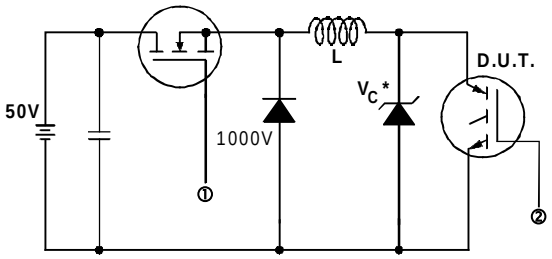


Fig. 13a - Clamped Inductive Load Test Circuit

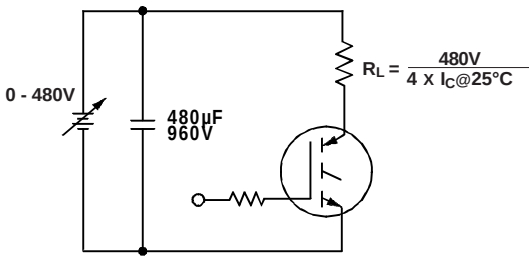


Fig. 13b - Pulsed Collector Current Test Circuit

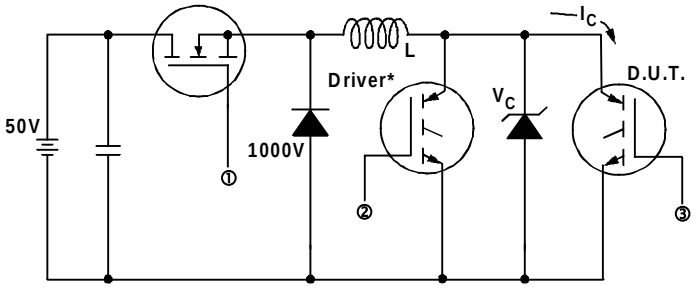


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

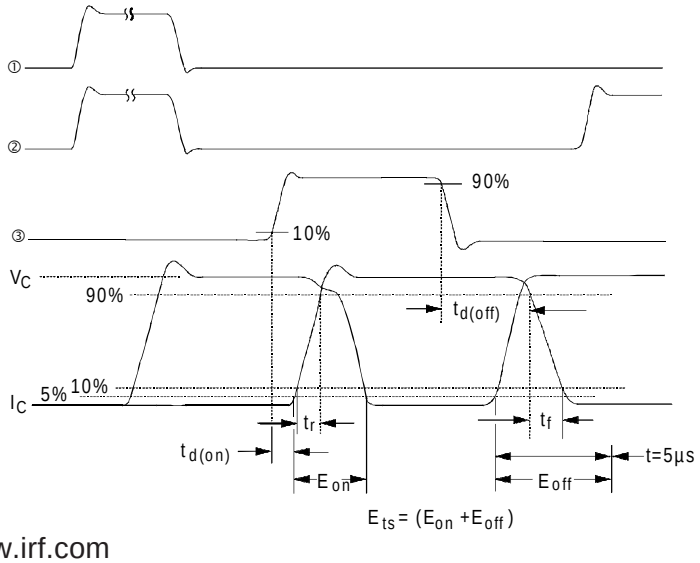
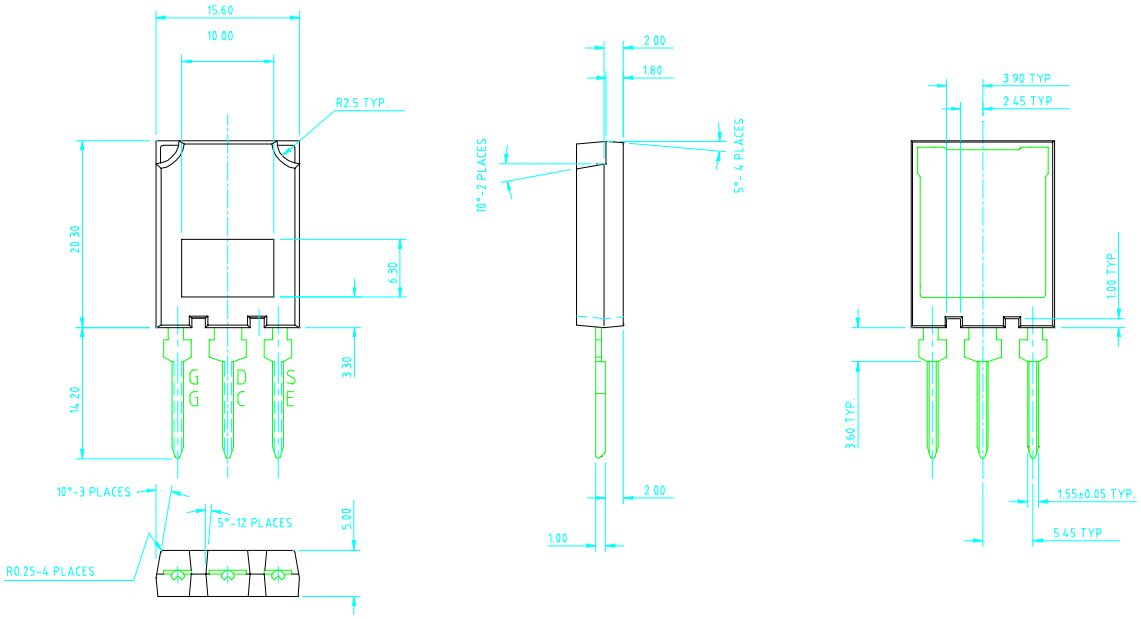


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — Super-247

Dimensions are shown in millimeters



International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
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International
IOR Rectifier

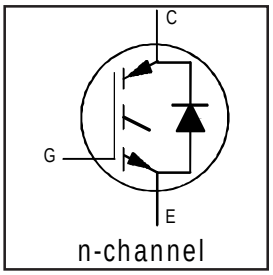
PD - 91684A

PRELIMINARY

IRG4PSC71KD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
UltraFast IGBT



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.83V

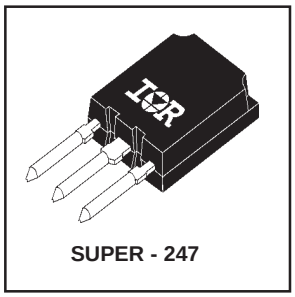
@V_{GE} = 15V, I_C = 60A

Features

- Hole-less clip/pressure mount package compatible with TO-247 and TO-264, with reinforced pins
- High abort circuit rating IGBTs, optimized for motorcontrol
- Minimum switching losses combined with low conduction losses
- Tightest parameter distribution
- IGBT co-packaged with ultrafast soft recovery antiparallel diode
- Creepage distance increased to 5.35mm

Benefits

- Highest current rating copack IGBT
- Maximum power density, twice the power handling of the TO-247, less space than TO-264
- HEXFRED™ diode optimized for operation with IGBT, to minimize EMI, noise and switching losses



SUPER - 247

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	85⑤	A
I_C @ T_C = 100°C	Continuous Collector Current	60	
I_{CM}	Pulsed Collector Current ①	200	
I_{LM}	Clamped Inductive Load Current ②	200	
I_F @ T_C = 100°C	Diode Continuous Forward Current	50	
I_{FM}	Diode Maximum Forward Current	200	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	350	W
P_D @ T_C = 100°C	Maximum Power Dissipation	140	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	

Thermal Resistance\ Mechanical

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	0.36	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	0.69	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	38	
	Recommended Clip Force	20.0(2.0)	—	—	N (kgf)
	Weight	—	6 (0.21)	—	g (oz)

5/11/99

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.5	—	V/°C	V_{GE} = 0V, I_C = 10mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.83	2.3	V	I_C = 60A V_{GE} = 15V
		—	2.20	—		I_C = 100A See Fig. 2, 5
		—	1.81	—		I_C = 60A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-8.0	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.5mA
g_{fe}	Forward Transconductance ④	31	46	—	S	V_{CE} = 50V, I_C = 60A
I_{CES}	Zero Gate Voltage Collector Current	—	—	500	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	13	mA	V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 60A See Fig. 13
		—	1.3	—		I_C = 60A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	340	510	nC	I_C = 60A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	44	66		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	160	240		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	82	—	ns	
t_r	Rise Time	—	107	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	282	423		I_C = 60A, V_{CC} = 480V
t_f	Fall Time	—	97	146		V_{GE} = 15V, R_G = 5.0Ω
E_{on}	Turn-On Switching Loss	—	3.95	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	2.33	—		and diode reverse recovery
E_{ts}	Total Switching Loss	—	6.28	7.7		See Fig. 9,10,18
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 360V, T_J = 125°C
						V_{GE} = 15V, R_G = 5.0Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	87	—	ns	T_J = 150°C, See Fig. 11,18
t_r	Rise Time	—	104	—		I_C = 60A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	374	—		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	143	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	8.5	—	mJ	and diode reverse recovery
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	6900	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	730	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	190	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	82	120	ns	T_J = 25°C See Fig.
		—	140	210		T_J = 125°C 14 I_F = 60A
I_{rr}	Diode Peak Reverse Recovery Current	—	8.2	12	A	T_J = 25°C See Fig.
		—	13	20		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	364	546	nC	T_J = 25°C See Fig.
		—	1084	1625		T_J = 125°C 16 di/dt = 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	328	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	266	—		T_J = 125°C 17

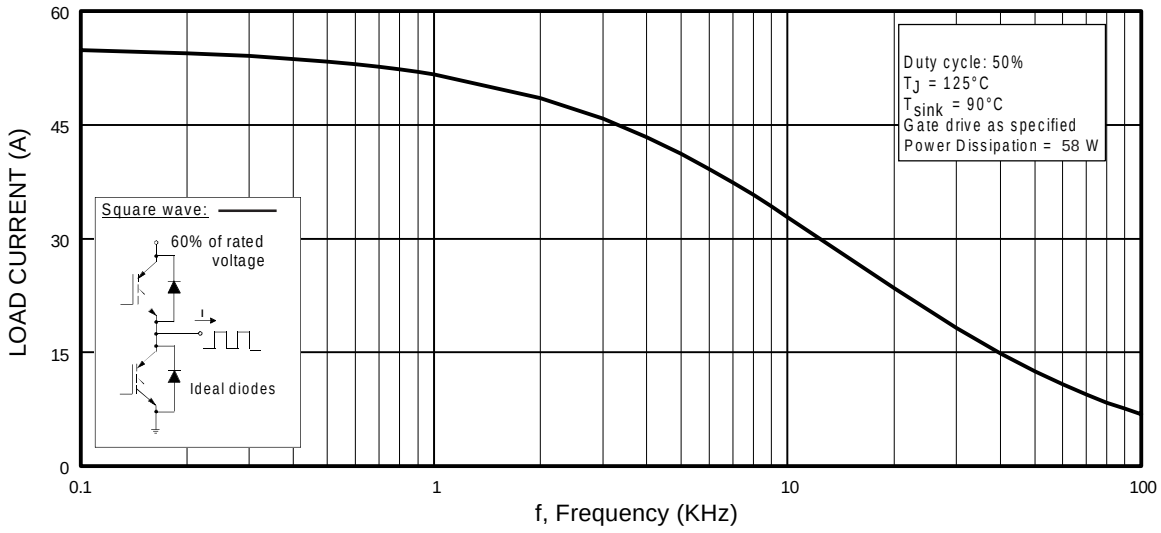


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

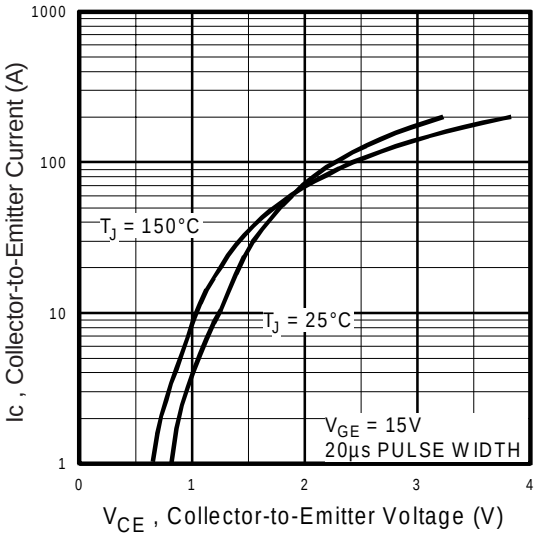


Fig. 2 - Typical Output Characteristics

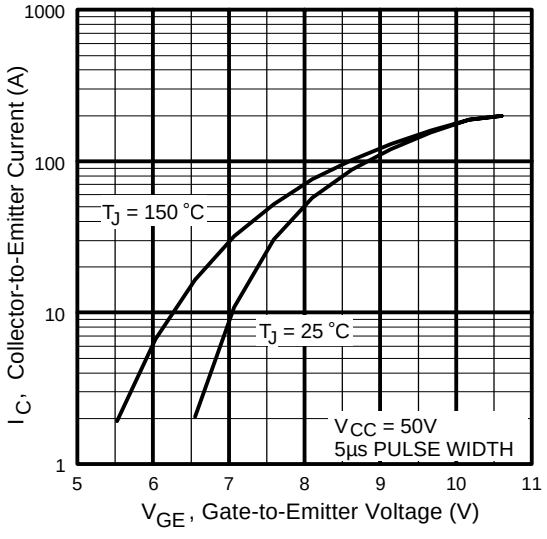


Fig. 3 - Typical Transfer Characteristics

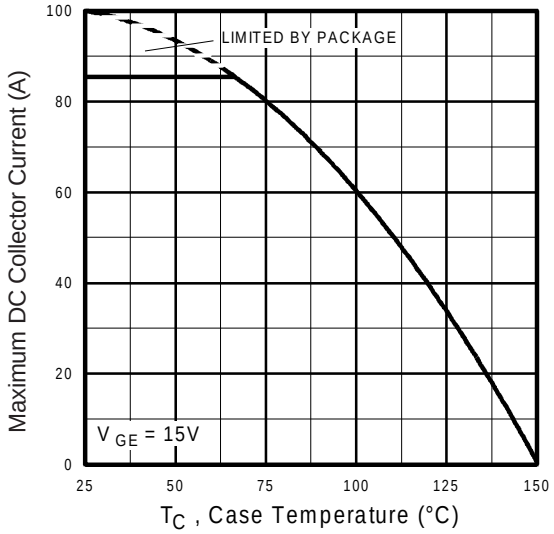


Fig. 4 - Maximum Collector Current vs. Case Temperature

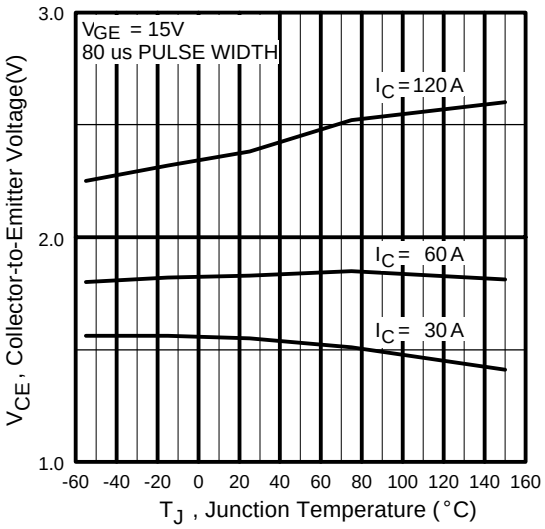


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

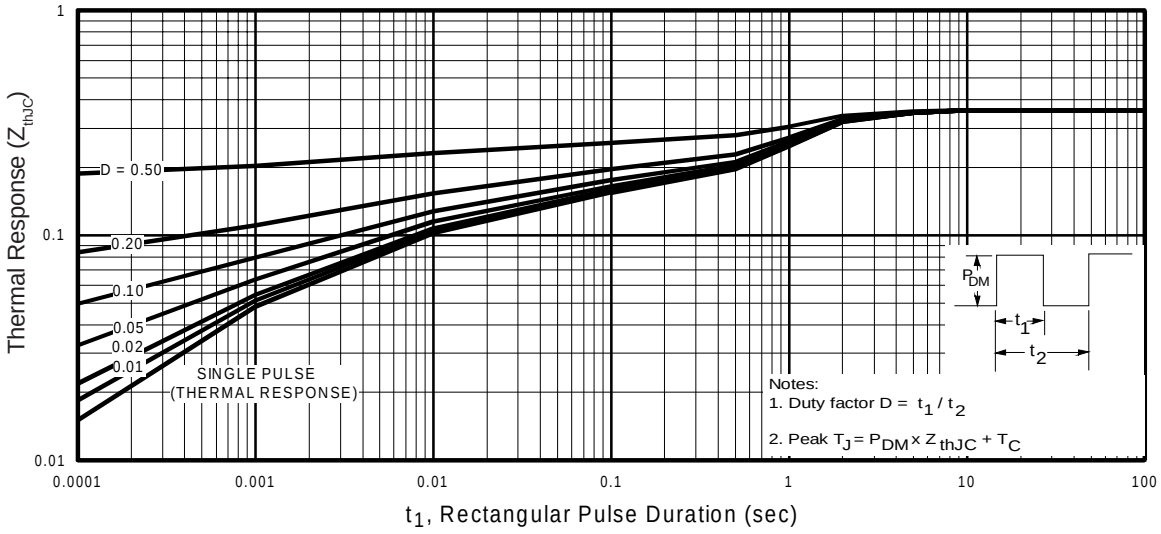


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

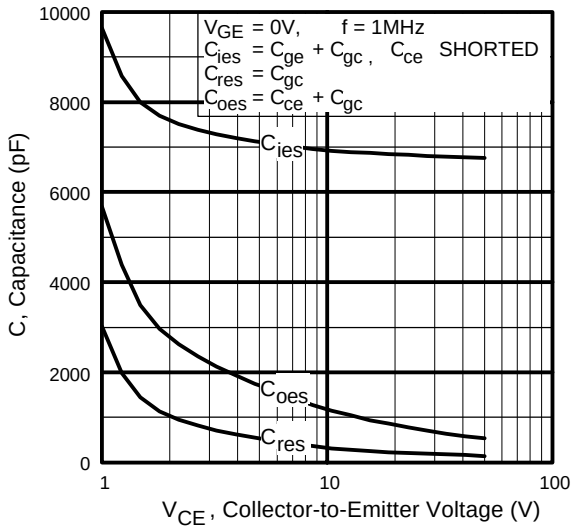


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

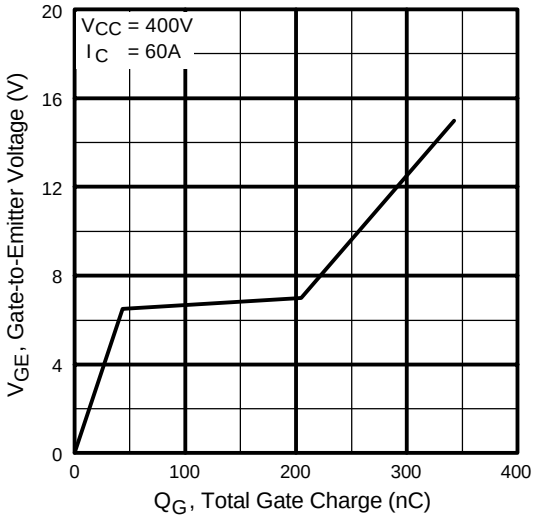


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

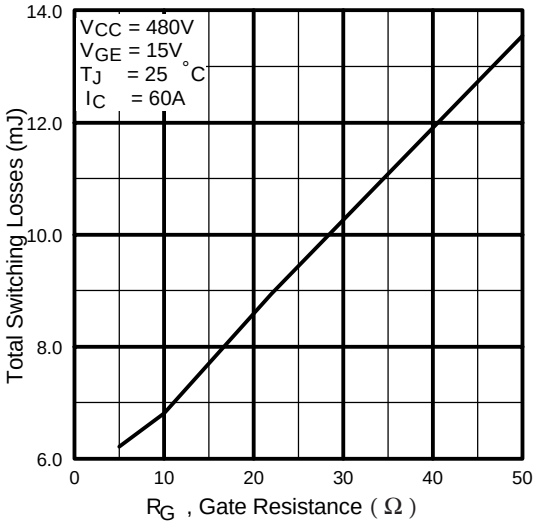


Fig. 9 - Typical Switching Losses vs. Gate Resistance

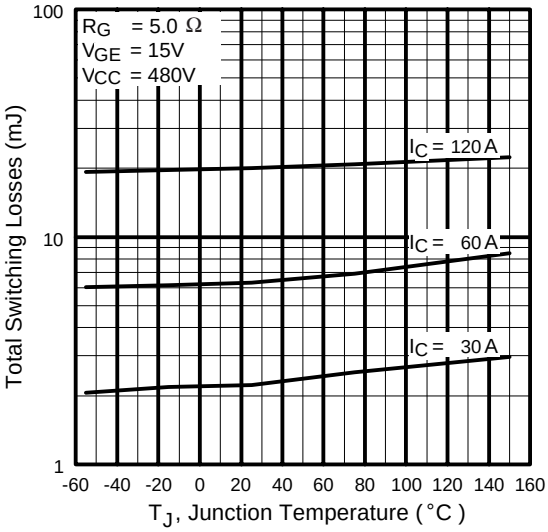


Fig. 10 - Typical Switching Losses vs. Junction Temperature

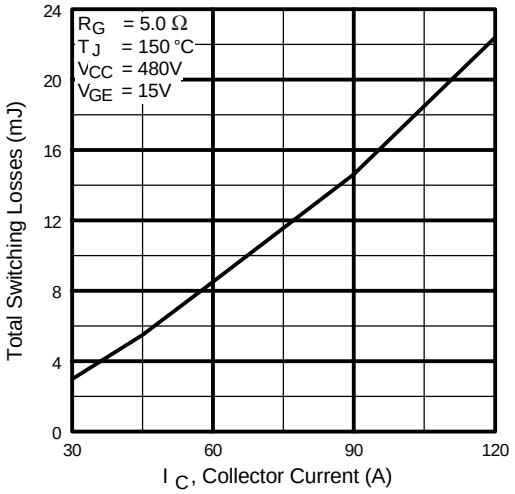


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

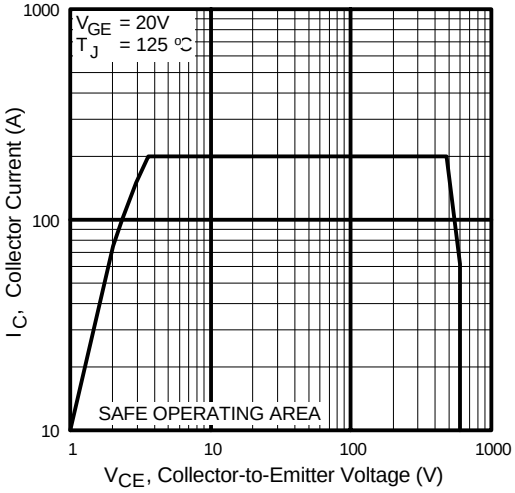


Fig. 12 - Turn-Off SOA

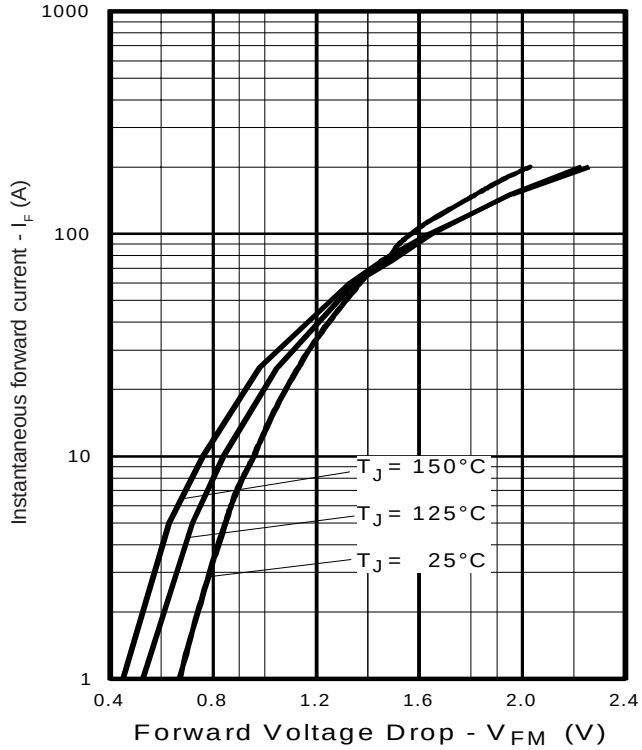


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

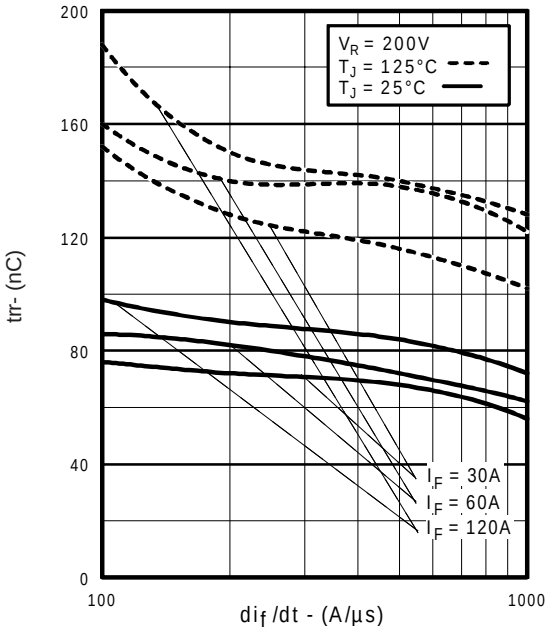


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

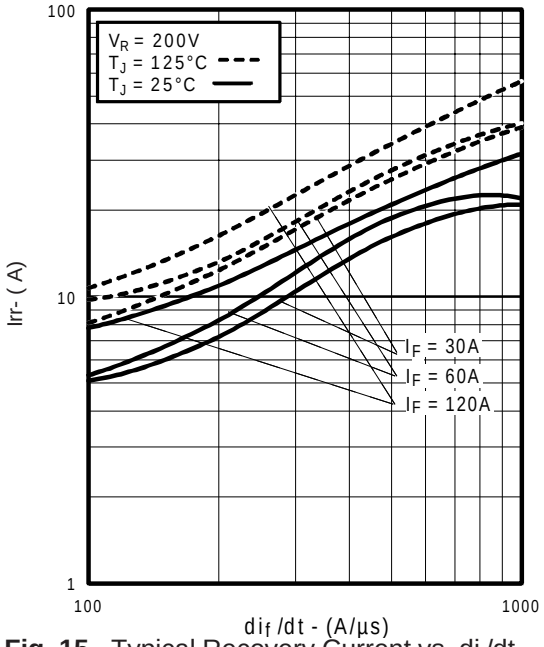


Fig. 15 - Typical Recovery Current vs. di_f/dt

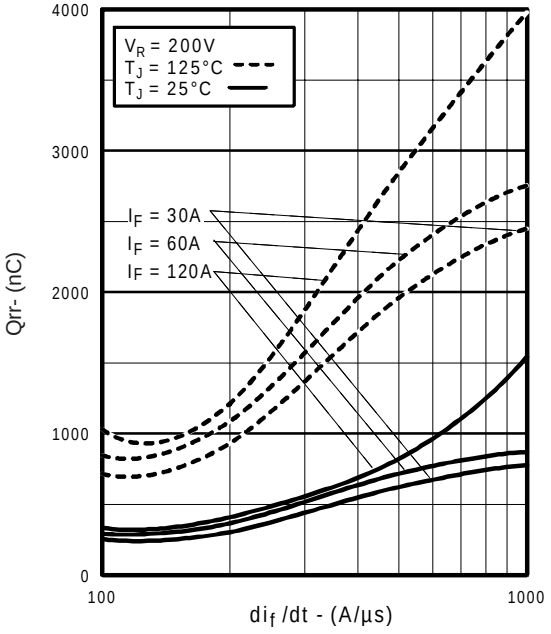


Fig. 16 - Typical Stored Charge vs. di_f/dt

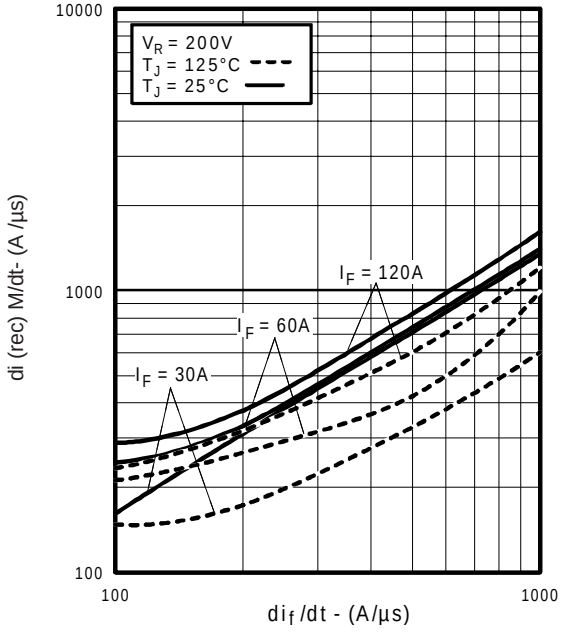


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

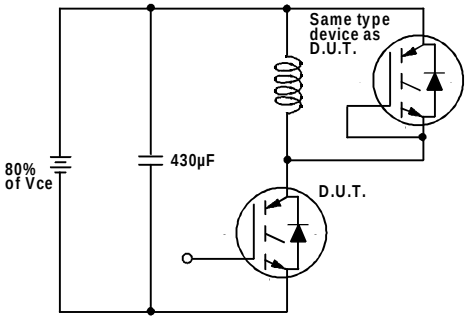


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

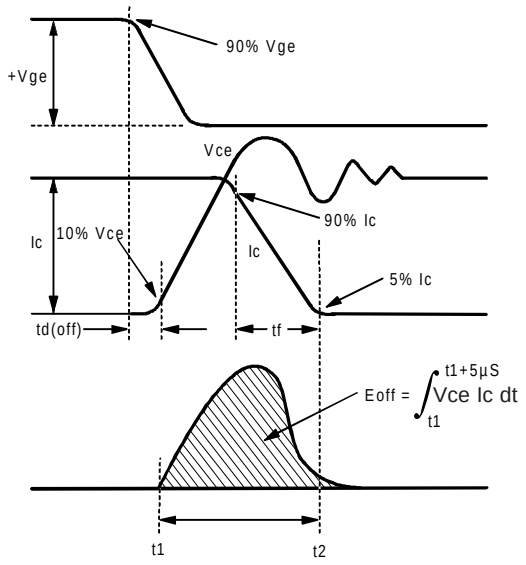


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

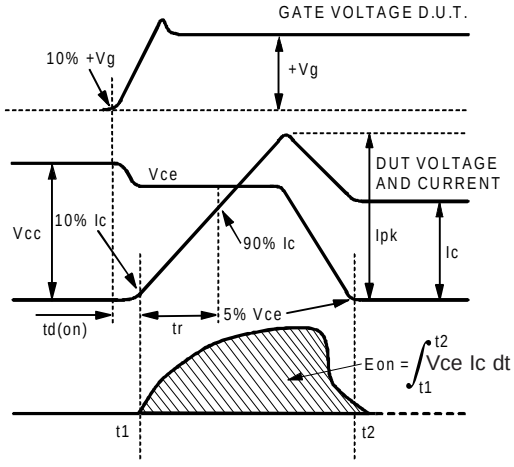


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

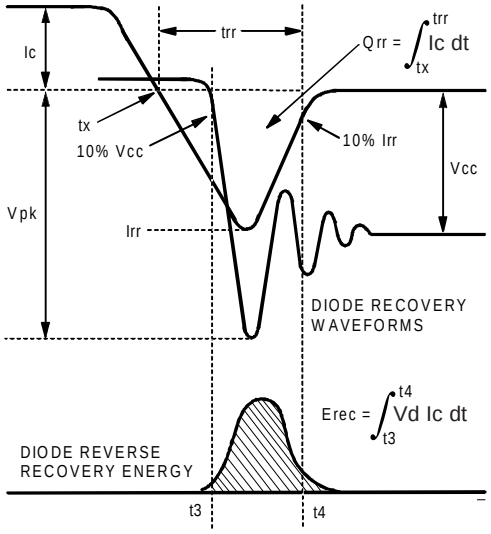


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

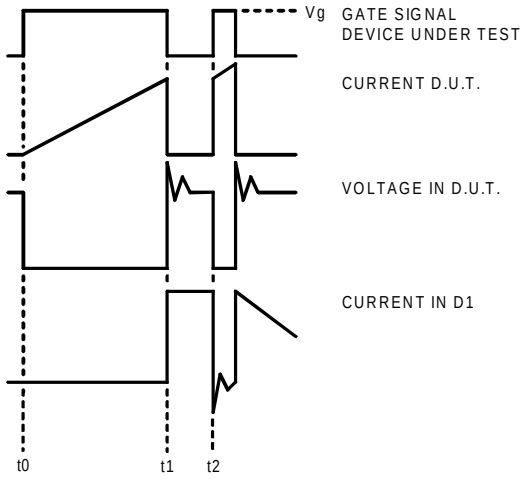


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

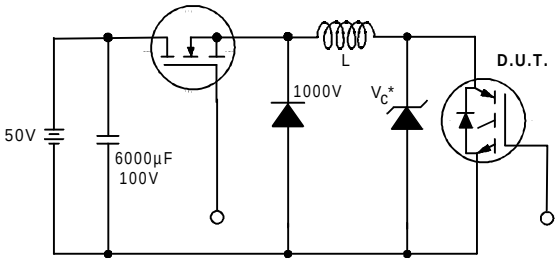


Figure 19. Clamped Inductive Load Test Circuit

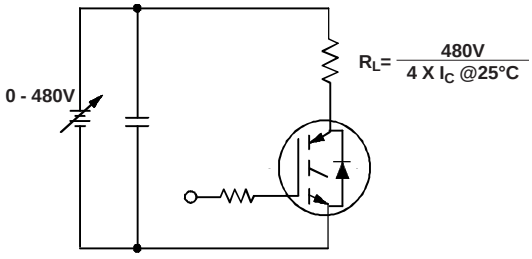


Figure 20. Pulsed Collector Current Test Circuit

Notes:

① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 5.0Ω (figure 19)

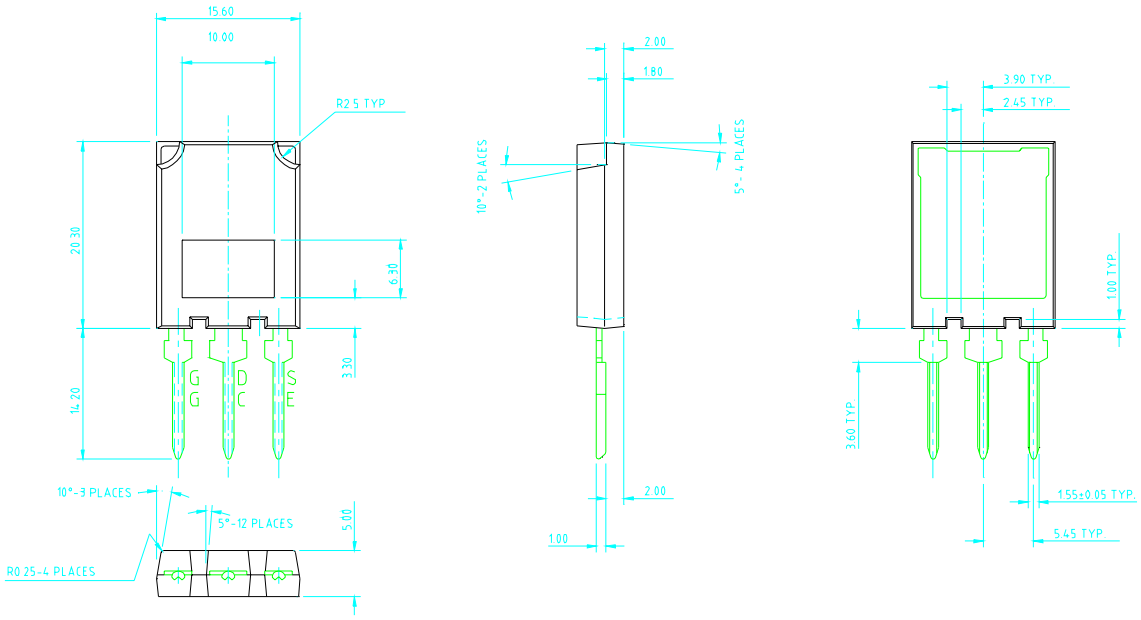
③ Pulse width ≤ 80µs; duty factor ≤ 0.1%

④ Pulse width 5.0µs, single shot

⑤ Current limited by the package, (Die current = 100A)

Case Outline and Dimensions — Super-247

Dimensions are shown in millimeters



International
IOR Rectifier

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IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
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PD - 91681A

International
IOR Rectifier

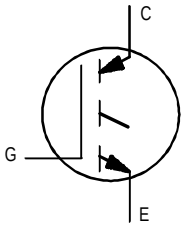
IRG4PSC71U

INSULATED GATE BIPOLAR TRANSISTOR

UltraFast Speed IGBT

Features

- UltraFast switching speed optimized for operating frequencies 8 to 40kHz in hard switching, 200kHz in resonant mode soft switching
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency (minimum switching and conduction losses) than prior generations
- Industry-benchmark Super-247 package with higher power handling capability compared to same footprint TO-247
- Creepage distance increased to 5.35mm



n-channel

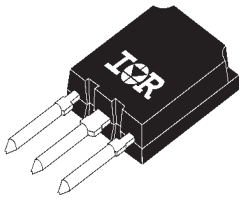
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.67V

@V_{GE} = 15V, I_C = 60A

Benefits

- Generation 4 IGBT's offer highest efficiencies available
- Maximum power density, twice the power handling of the TO-247, less space than TO-264
- IGBTs optimized for specific application conditions
- Cost and space saving in designs that require multiple, paralleled IGBTs



SUPER - 247

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	85⑥	A
I_C @ T_C = 100°C	Continuous Collector Current	60	
I_{CM}	Pulsed Collector Current ①	200	
I_{LM}	Clamped Inductive Load Current ②	200	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	180	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	350	W
P_D @ T_C = 100°C	Maximum Power Dissipation	140	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	

Thermal Resistance\ Mechanical

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	——	0.36	°C/W
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	——	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	——	38	
	Recommended Clip Force	20.0(2.0)	——	——	N (kgf)
	Weight	——	6 (0.21)	——	g (oz)

5/12/99

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.45	—	V/°C	V_{GE} = 0V, I_C = 5.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.67	2.0	V	I_C = 60A V_{GE} = 15V
		—	1.95	—		I_C = 100A See Fig.2, 5
		—	1.71	—		I_C = 60A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.0mA
g_{fe}	Forward Transconductance ⑤	47	70	—	S	V_{CE} = 50V, I_C = 60A
I_{CES}	Zero Gate Voltage Collector Current	—	—	500	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	5.0	mA	V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	340	520	nC	I_C = 60A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	44	66		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	160	240		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	34	—	ns	T_J = 25°C
t_r	Rise Time	—	50	—		I_C = 60A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	56	84		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	86	130		Energy losses include "tail"
E_{on}	Turn-On Switching Loss	—	0.42	—	mJ	See Fig. 10, 11, 13, 14
E_{off}	Turn-Off Switching Loss	—	1.99	—		
E_{ts}	Total Switching Loss	—	2.41	3.2		
$t_{d(on)}$	Turn-On Delay Time	—	30	—	ns	T_J = 150°C,
t_r	Rise Time	—	49	—		I_C = 60A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	129	—		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	175	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	4.5	—	mJ	See Fig. 13, 14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	7500	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	720	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	93	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 5.0Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

⑥ Current limited by the package, (Die current = 100A)

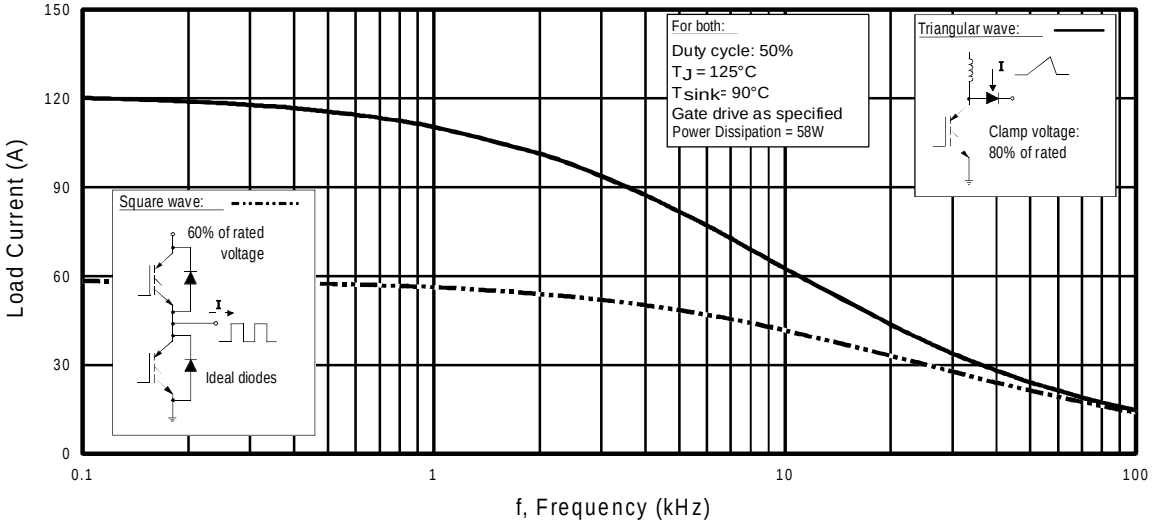


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

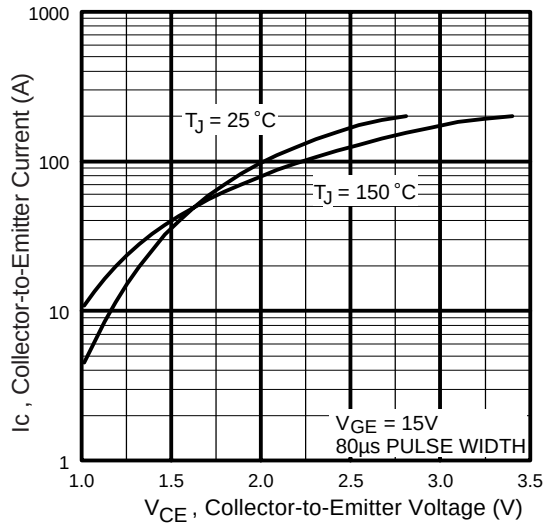


Fig. 2 - Typical Output Characteristics

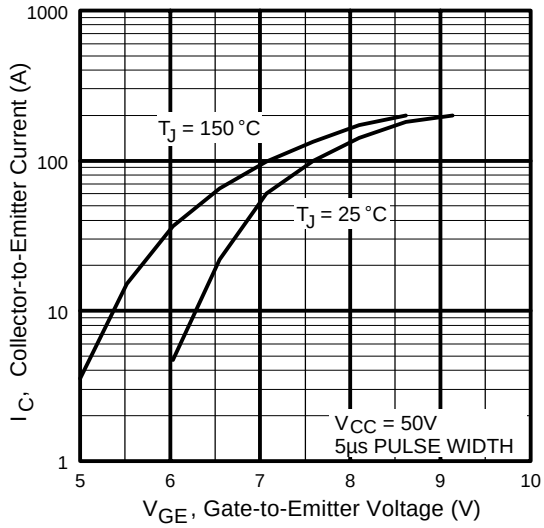


Fig. 3 - Typical Transfer Characteristics

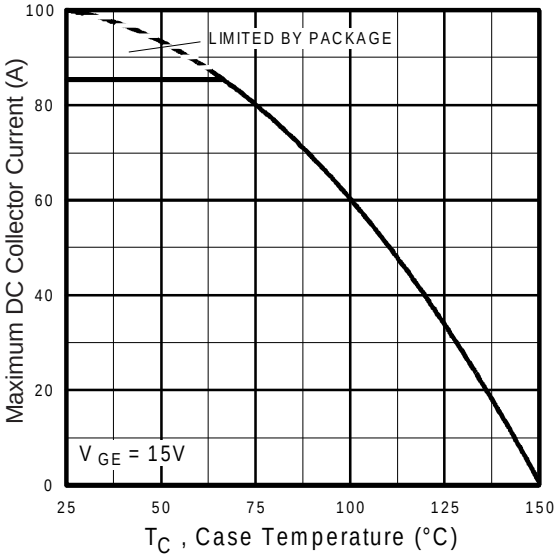


Fig. 4 - Maximum Collector Current vs. Case Temperature

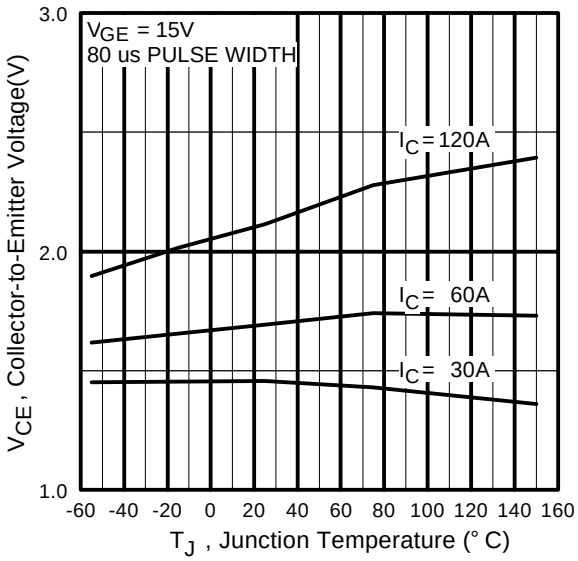


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

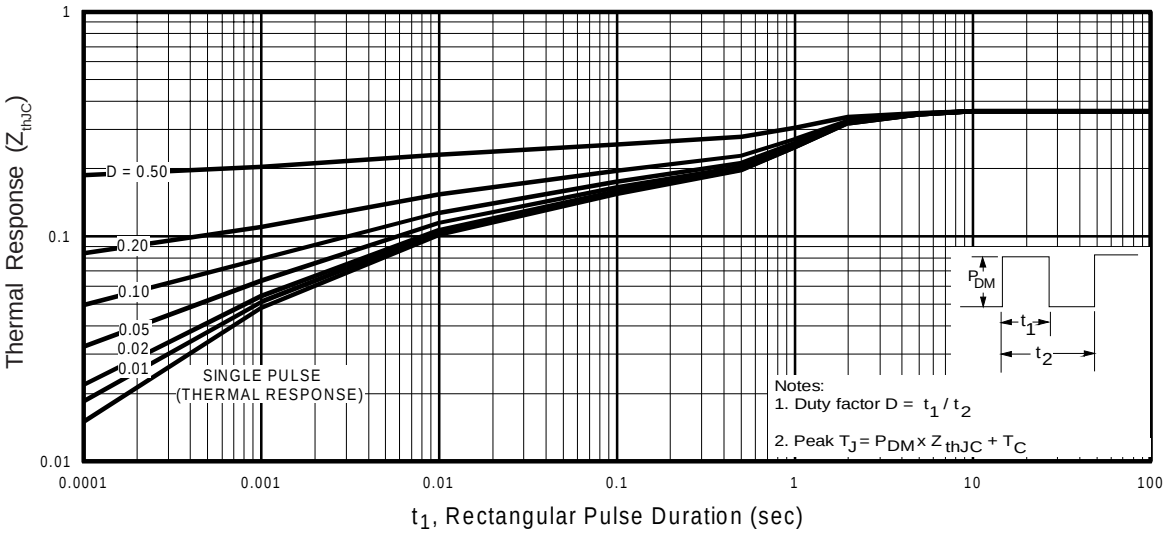


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

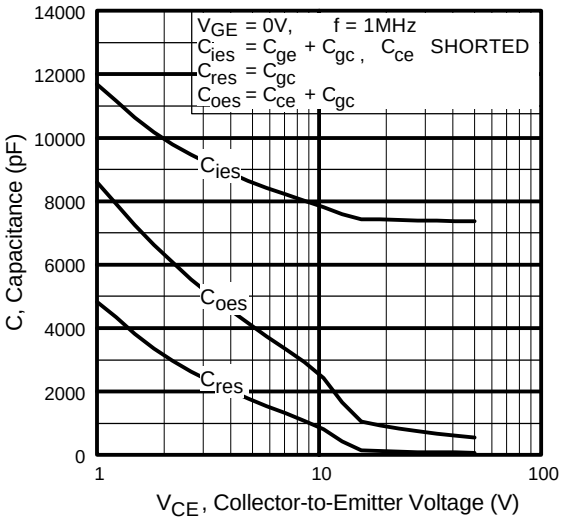


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

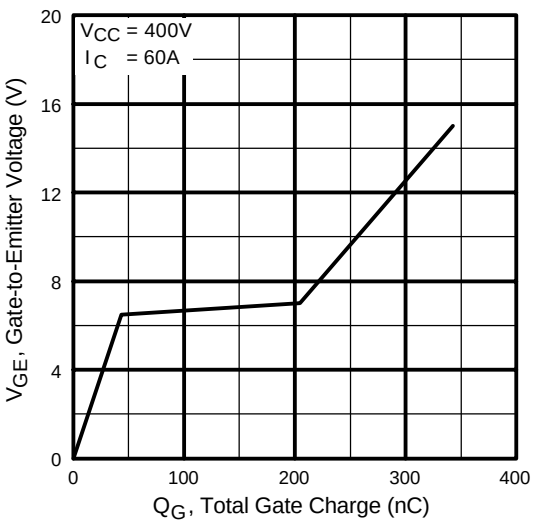


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

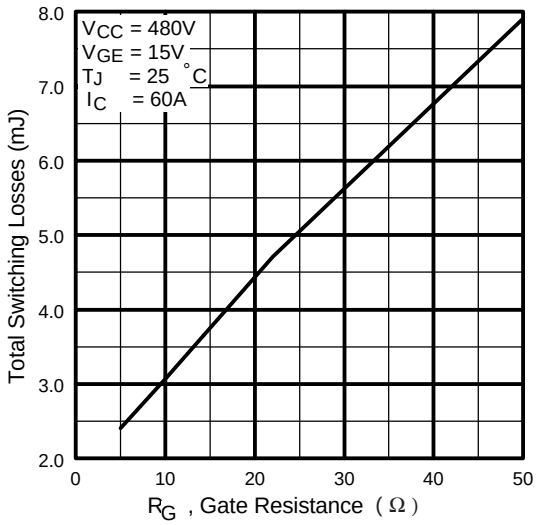


Fig. 9 - Typical Switching Losses vs. Gate Resistance

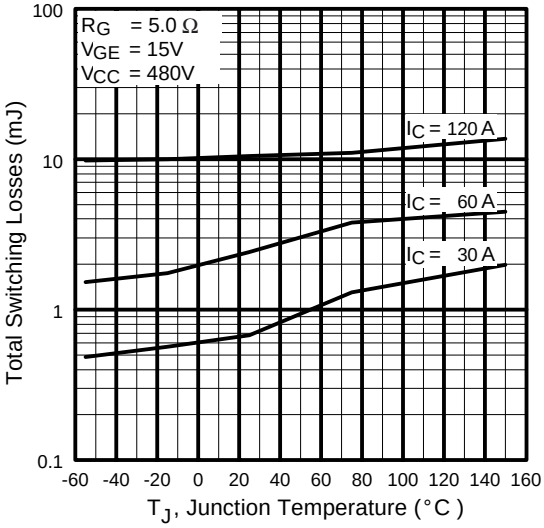


Fig. 10 - Typical Switching Losses vs. Junction Temperature

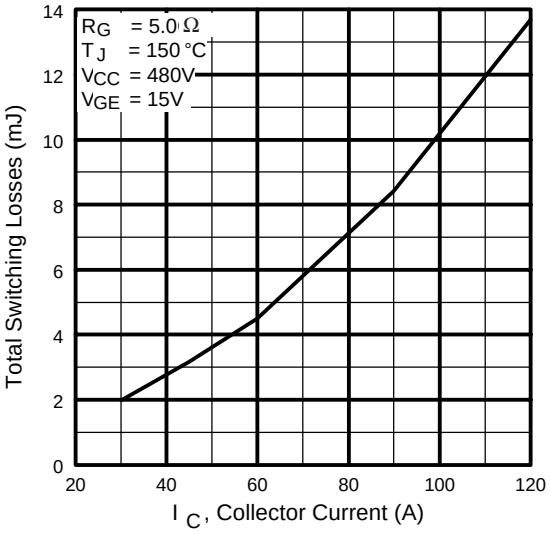


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

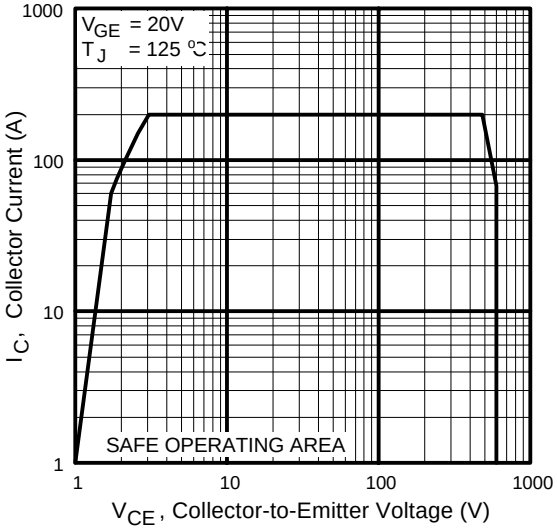


Fig. 12 - Turn-Off SOA

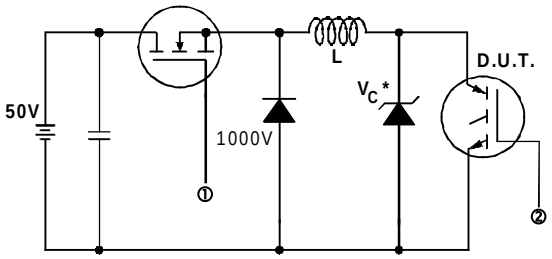


Fig. 13a - Clamped Inductive Load Test Circuit

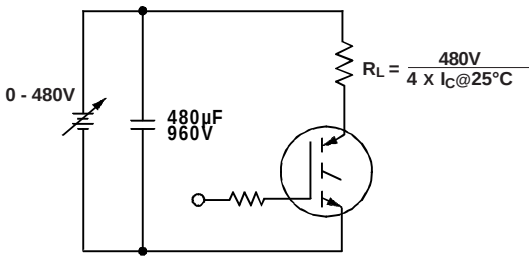


Fig. 13b - Pulsed Collector Current Test Circuit

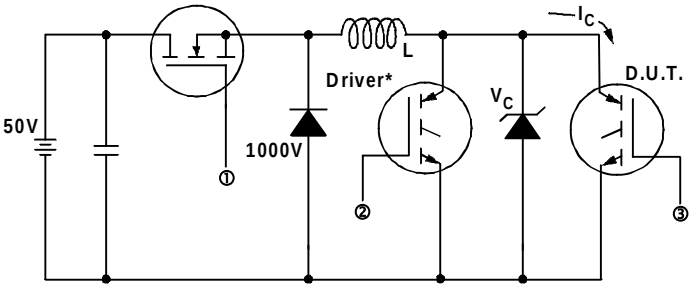


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

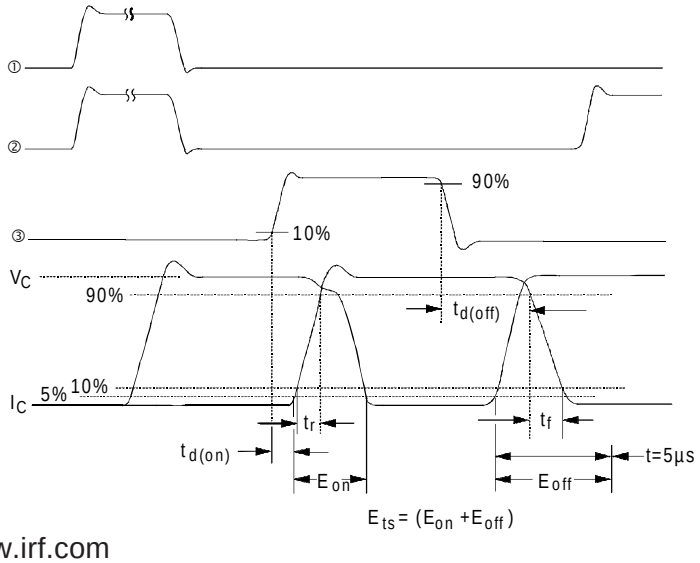
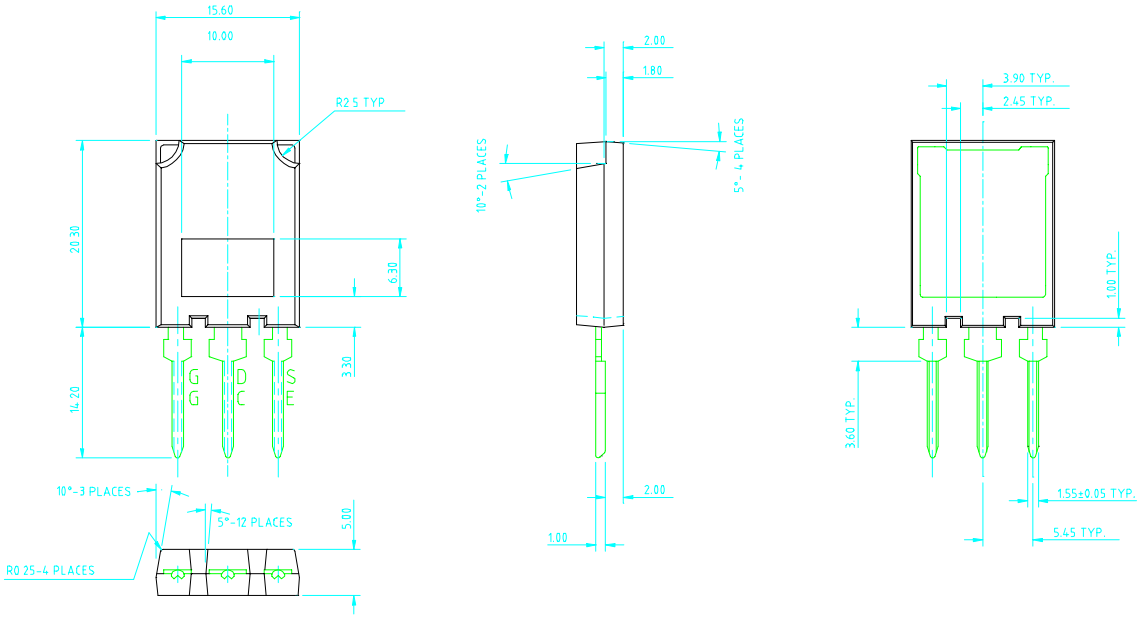


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — Super-247

Dimensions are shown in millimeters



International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936
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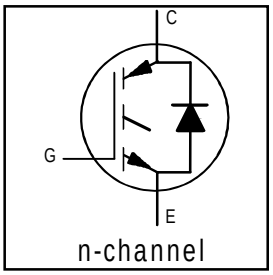
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PD - 91682A

IRG4PSC71UD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

UltraFast CoPack IGBT



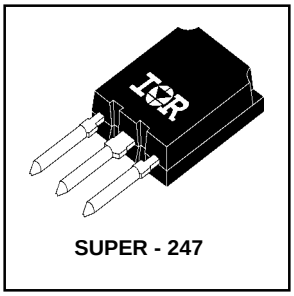
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.67V

@V_{GE} = 15V, I_C = 60A

Features

- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency (minimum switching and conduction losses) than prior generations
- IGBT co-packaged with HEXFRED ultrafast, ultrasoft recovery anti-parallel diodes for use in bridge configurations
- Industry-benchmark Super-247 package with higher power handling capability compared to same footprint TO-247
- Creepage distance increased to 5.35mm



SUPER - 247

Benefits

- Generation 4 IGBT's offer highest efficiencies available
- Maximum power density, twice the power handling of TO-247, less space than TO-264
- IGBTs optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBTs
- Cost and space saving in designs that require multiple, paralleled IGBTs

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	85⑤	A
I_C @ T_C = 100°C	Continuous Collector Current	60	
I_{CM}	Pulsed Collector Current ①	200	
I_{LM}	Clamped Inductive Load Current ②	200	
I_F @ T_C = 100°C	Diode Continuous Forward Current	60	
I_{FM}	Diode Maximum Forward Current	350	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	350	W
P_D @ T_C = 100°C	Maximum Power Dissipation	140	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	

Thermal Resistance\ Mechanical

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	0.36	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	0.69	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	38	
	Recommended Clip Force	20.0(2.0)	—	—	N (kgf)
	Weight	—	6 (0.21)	—	g (oz)

5/12/99

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.39	—	V/°C	V_{GE} = 0V, I_C = 10mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.67	2.0	V	I_C = 60A V_{GE} = 15V
		—	1.95	—		I_C = 100A See Fig. 2, 5
		—	1.71	—		I_C = 60A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-13	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.5mA
g_{fe}	Forward Transconductance ④	47	70	—	S	V_{CE} = 50V, I_C = 60A
I_{CES}	Zero Gate Voltage Collector Current	—	—	500	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	13	mA	V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 60A See Fig. 13
		—	1.3	—		I_C = 60A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	340	520		I_C = 60A
Qge	Gate - Emitter Charge (turn-on)	—	44	66	nC	V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	160	240		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	90	—		T_J = 25°C
t_r	Rise Time	—	94	—	ns	I_C = 60A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	245	368		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	110	167		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	3.26	—		diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	2.27	—	mJ	See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	—	5.53	7.2		
$t_{d(on)}$	Turn-On Delay Time	—	91	—		T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	—	88	—	ns	I_C = 60A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	353	—		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	150	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	7.1	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	7500	—		V_{GE} = 0V
C_{oes}	Output Capacitance	—	720	—	pF	V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	93	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	82	120	ns	T_J = 25°C See Fig.
		—	140	210		T_J = 125°C 14 I_F = 60A
I_{rr}	Diode Peak Reverse Recovery Current	—	8.2	12	A	T_J = 25°C See Fig.
		—	13	20		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	364	546	nC	T_J = 25°C See Fig.
		—	1084	1625		T_J = 125°C 16 di/dt = 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	328	—	A/µs	T_J = 25°C See Fig.
During t_b		—	266	—		T_J = 125°C 17

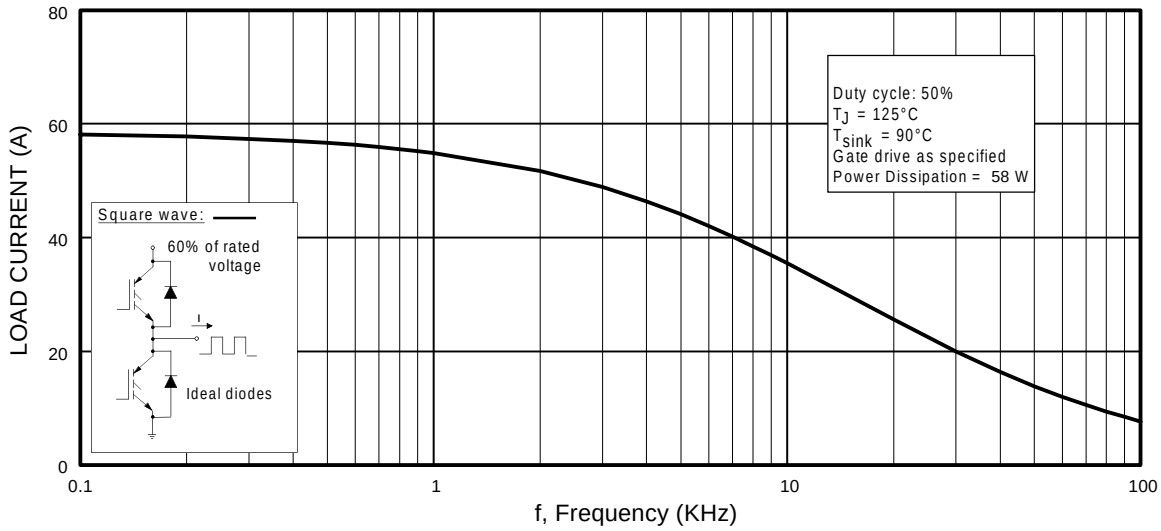


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

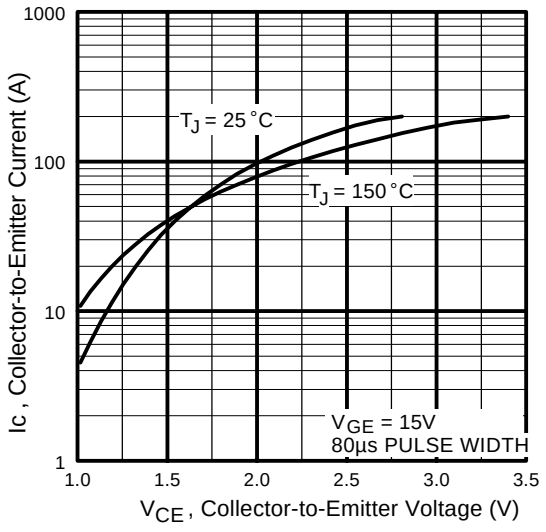


Fig. 2 - Typical Output Characteristics

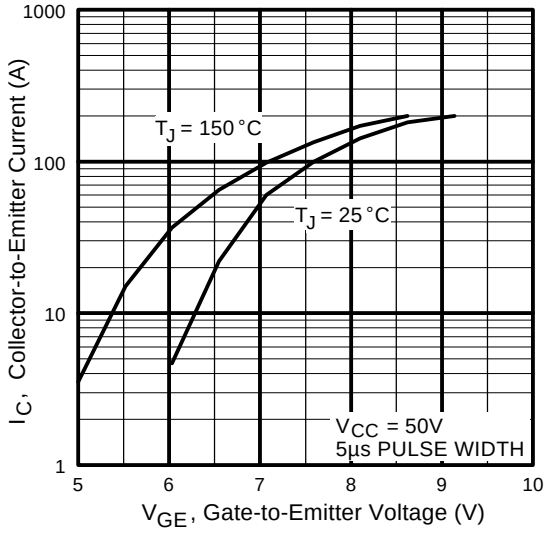


Fig. 3 - Typical Transfer Characteristics

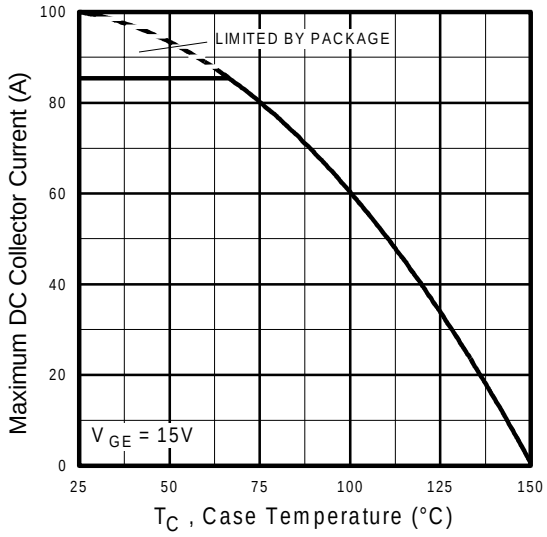


Fig. 4 - Maximum Collector Current vs. Case Temperature

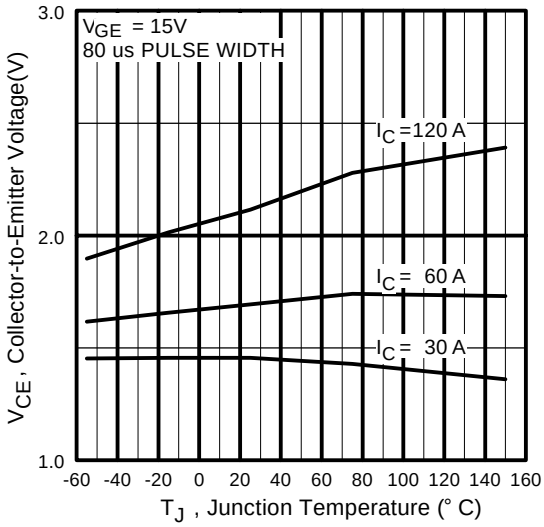


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

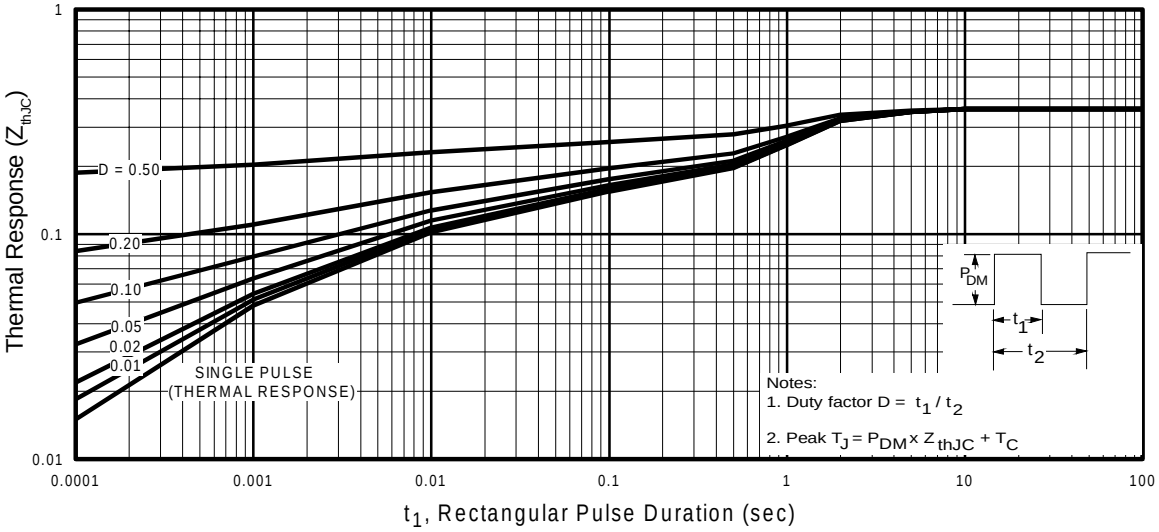


Fig. 6 - Maximum IGBT Effective Transient Thermal Impedance, Junction-to-Case

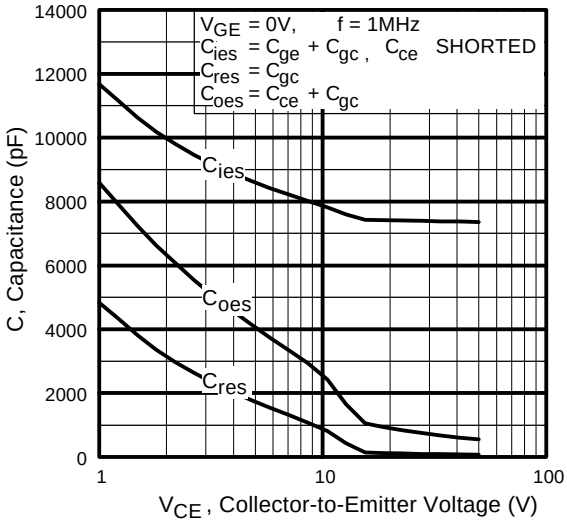


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

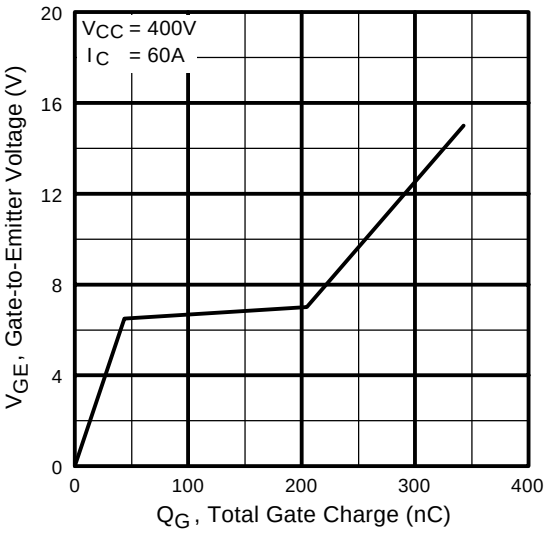


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

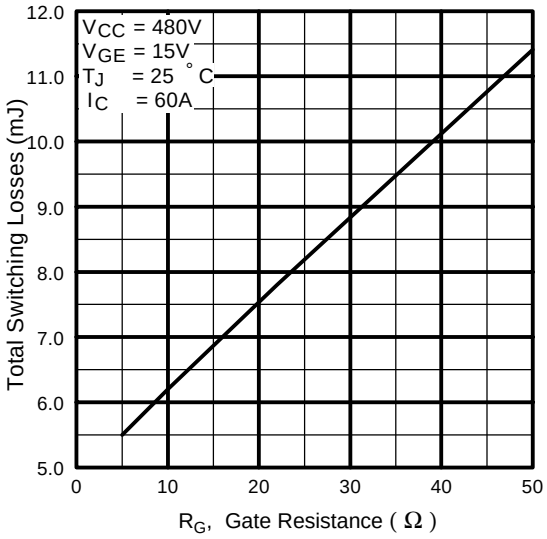


Fig. 9 - Typical Switching Losses vs. Gate Resistance

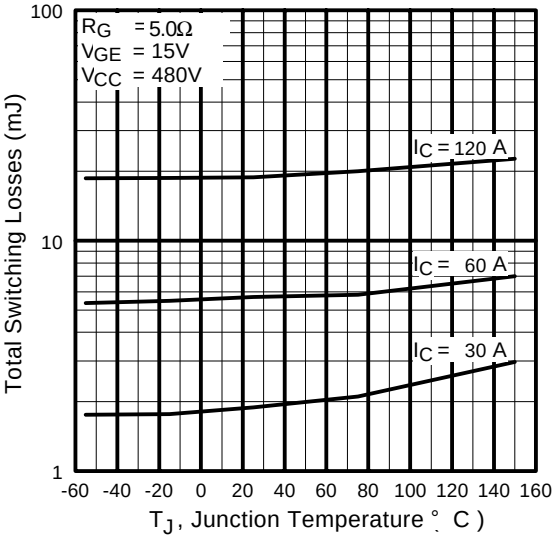


Fig. 10 - Typical Switching Losses vs. Junction Temperature

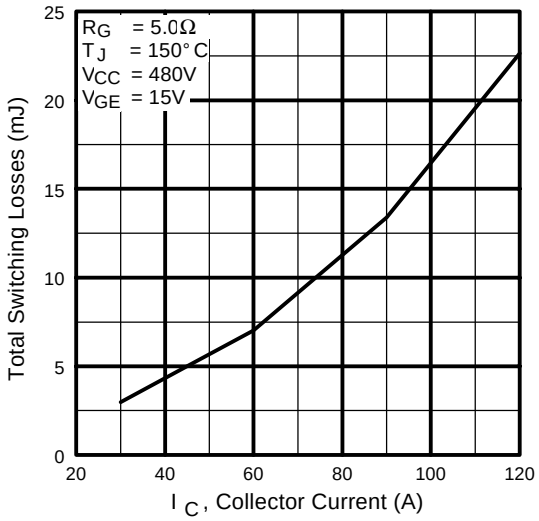


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

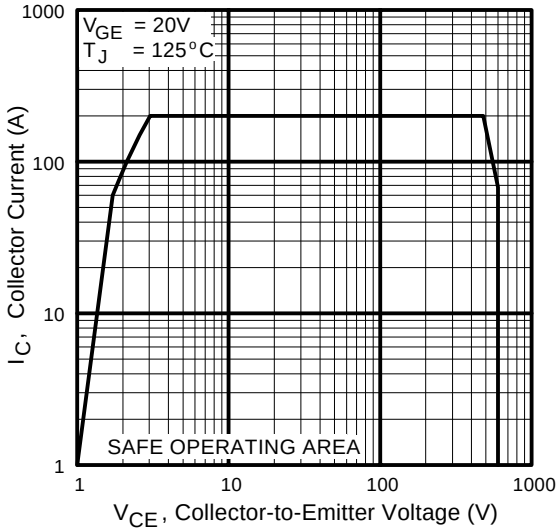


Fig. 12 - Turn-Off SOA

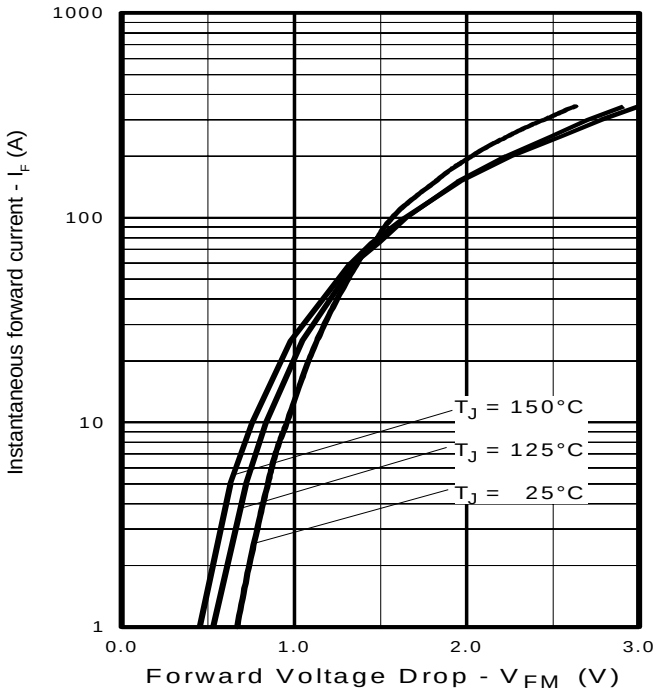


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

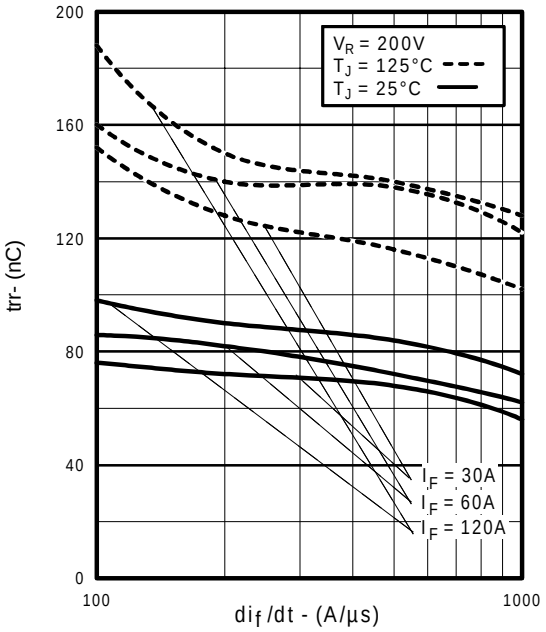


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

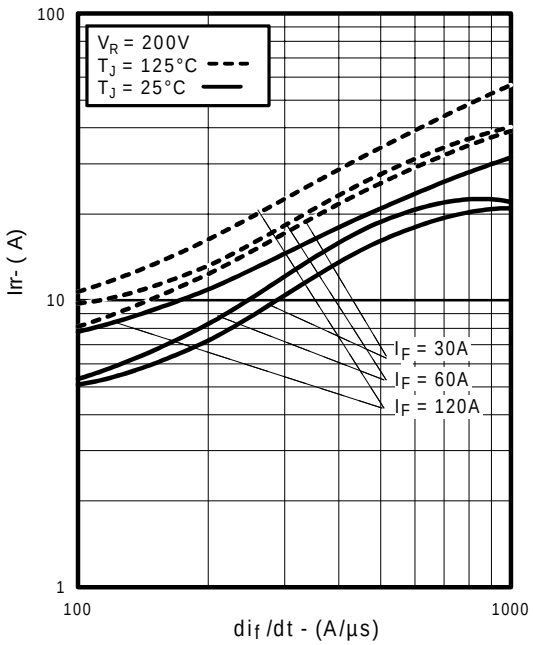


Fig. 15 - Typical Recovery Current vs. di_f/dt

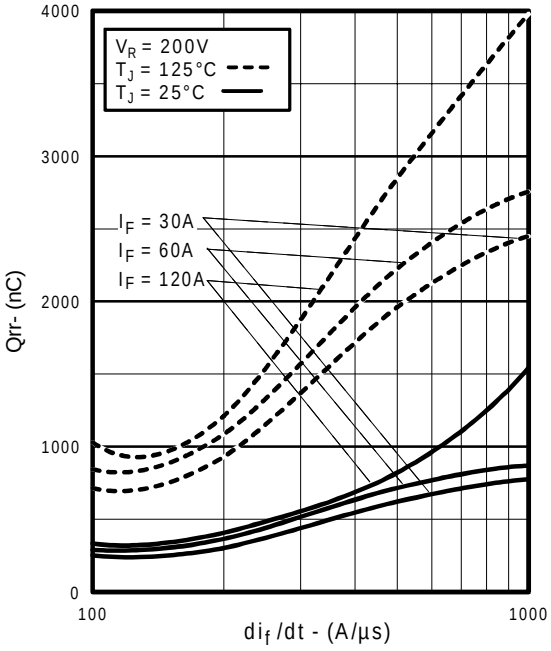


Fig. 16 - Typical Stored Charge vs. di_f/dt

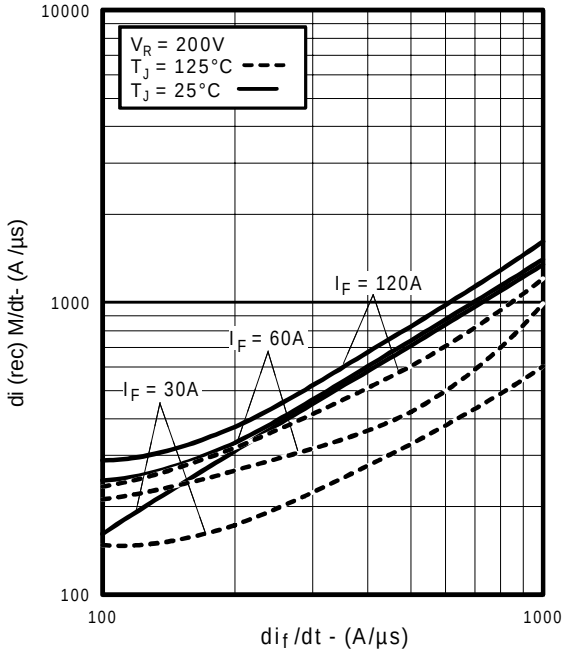


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

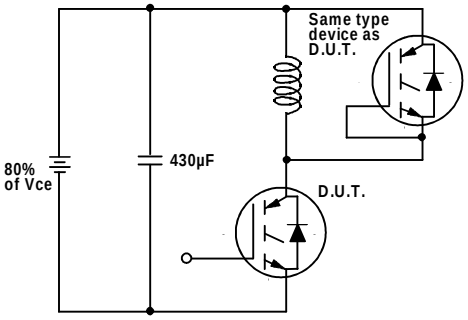


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

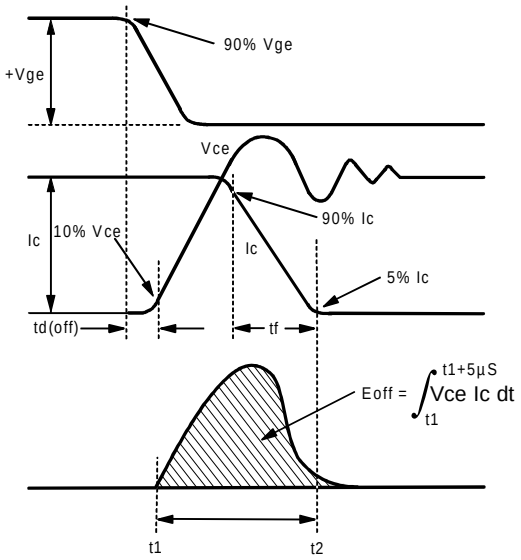


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

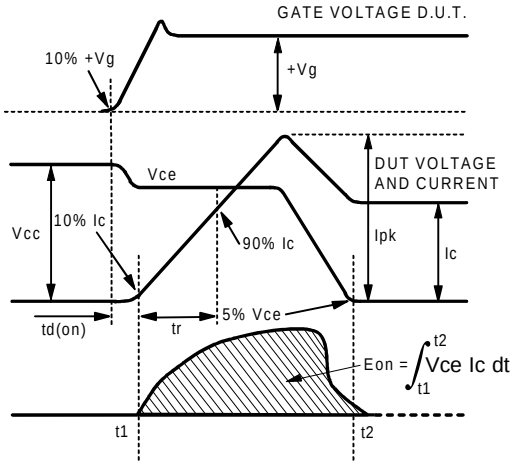


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

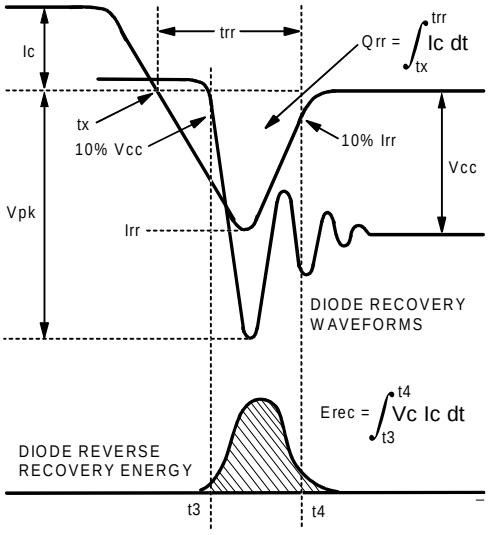


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

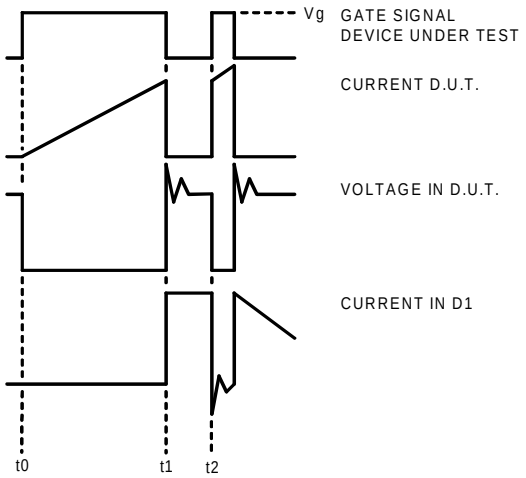


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

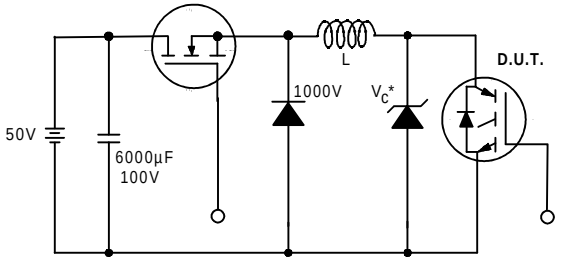


Figure 19. Clamped Inductive Load Test Circuit

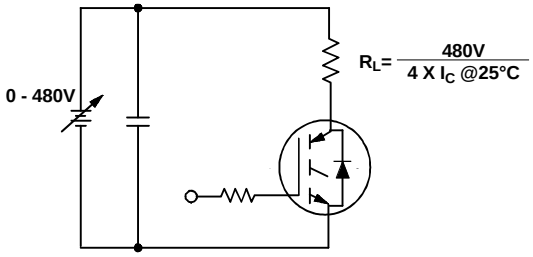


Figure 20. Pulsed Collector Current Test Circuit

Notes:

① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 5.0Ω (figure 19)

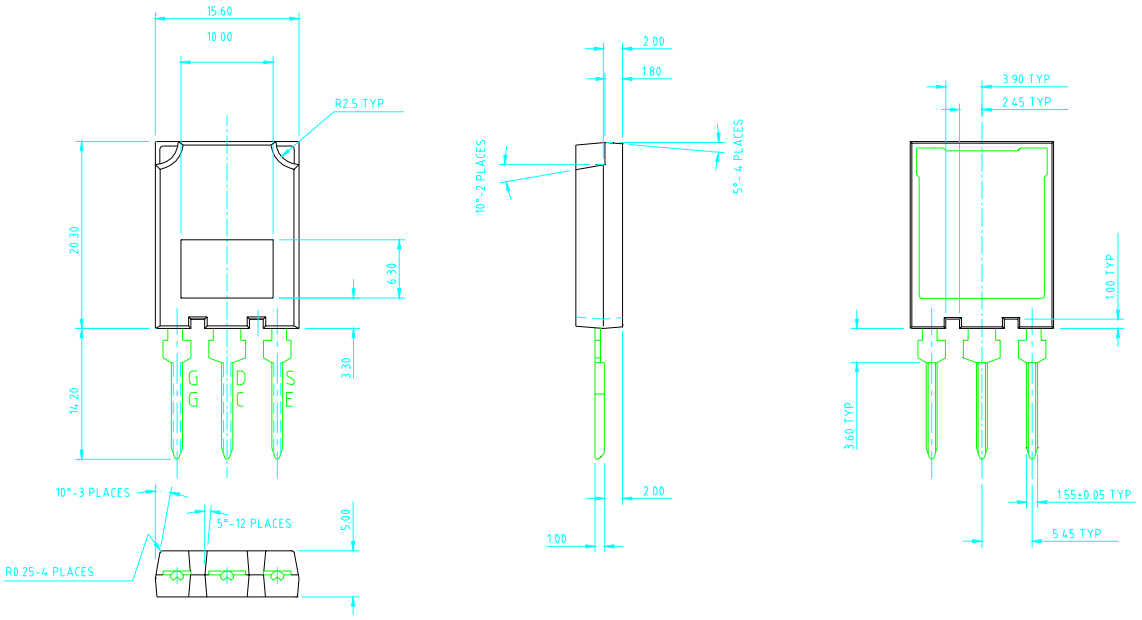
③ Pulse width ≤ 80µs; duty factor ≤ 0.1%

④ Pulse width 5.0µs, single shot

⑤ Current limited by the package, (Die current = 100A)

Case Outline and Dimensions — Super-247

Dimensions are shown in millimeters



International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936
http://www.irf.com/ Data and specifications subject to change without notice. 5/99

International
IOR Rectifier

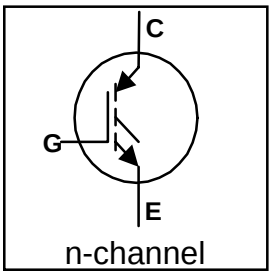
IRGP20B120U-E

INSULATED GATE BIPOLAR TRANSISTOR

UltraFast IGBT

Features

- UltraFast Non Punch Through (NPT) Technology
- 10 µs Short Circuit capability
- Square RBSOA
- Positive V_{CE}(on) Temperature Coefficient
- Extended lead TO-247 package



n-channel

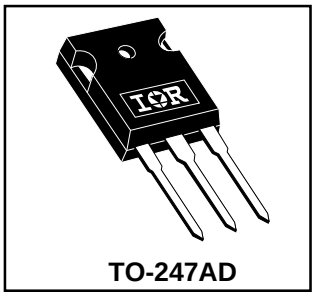
V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 3.05V

V_{GE} = 15V, I_C = 20A, 25°C

Benefits

- Benchmark efficiency above 20KHz
- Optimized for Welding, UPS, and Induction Heating applications
- Rugged with UltraFast performance
- Low EMI
- Significantly Less Snubber required
- Excellent Current sharing in Parallel operation
- Longer leads for easier mounting



TO-247AD

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current (Fig.1)	40	A
I_C @ T_C = 100°C	Continuous Collector Current (Fig.1)	20	
I_{CM}	Pulsed Collector Current (Fig.3, Fig. CT.5)	120	
I_{LM}	Clamped Inductive Load Current(Fig.4, Fig. CT.2)	120	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{AS} @ T_C =25°C	Avalanche Energy, single pulse I_C = 25A, V_{CC} = 50V, R_{GE} = 25ohm L = 200µH (Fig. CT.6)	65	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation (Fig.2)	300	W
P_D @ T_C = 100°C	Maximum Power Dissipation (Fig.2)	120	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300, (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	0.42	°C/W
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	40	
Wt	Weight	—	6 (0.21)	—	g (oz)
$Z_{\theta JC}$	Transient Thermal Impedance Junction-to-Case (Fig.18)				

Electrical Characteristics @ TJ = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	Fig.
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200			V	V_{GE} = 0V, I_c =250 µA	
$\Delta V_{(BR)CES}$ / ΔTj	Temperature Coeff. of Breakdown Voltage		+1.2		V/°C	V_{GE} = 0V, I_c = 1 mA (25 -125 °C)	
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage		3.05	3.45	V	I_C = 20A, V_{GE} = 15V	5, 6
			3.37	3.80		I_C = 25A, V_{GE} = 15V	7, 8
			4.23	4.85		I_C = 40A, V_{GE} = 15V	9
			3.89	4.50		I_C = 20A, V_{GE} = 15V, T_J = 125°C	10
			4.31	5.06		I_C = 25A, V_{GE} = 15V, T_J = 125°C	
$V_{GE(th)}$	Gate Threshold Voltage	4.0	5.0	6.0	V	V_{CE} = V_{GE}, I_C = 250 µA	8,9,10,11
$\Delta V_{GE(th)}$ / ΔTj	Temperature Coeff. of Threshold Voltage		- 1.2		mV/°C	V_{CE} = V_{GE}, I_C = 1 mA (25 -125 °C)	
g_{fe}	Forward Transconductance	13.6	15.7	17.8	S	V_{CE} = 50V, I_C = 20A, PW=80µs	
I_{CES}	Zero Gate Voltage Collector Current			250	µA	V_{GE} = 0V, V_{CE} = 1200V	
			420	750		V_{GE} = 0V, V_{CE} = 1200V, T_J =125°C	
			1482	2200		V_{GE} = 0V, V_{CE} = 1200V, T_J =150°C	
I_{GES}	Gate-to-Emitter Leakage Current			±100	nA	V_{GE} = ±20V	

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	Fig.
Q_g	Total Gate charge (turn-on)		169	254	nC	I_C = 20A	17
Q_{ge}	Gate - Emitter Charge (turn-on)		24	36		V_{CC} = 600V	CT1
Q_{gc}	Gate - Collector Charge (turn-on)		82	126		V_{GE} = 15V	
E_{on}	Turn-On Switching Loss *		850	1050	µJ	I_C = 20A, V_{CC} = 600V	CT4
E_{off}	Turn-Off Switching Loss *		425	650		V_{GE} = 15V, Rg = 5Ω, L = 200µH	WF1
E_{tot}	Total Switching Loss *		1275	1800		T_J = 25°C, Energy losses include tail and diode reverse recovery	WF2
E_{on}	Turn-on Switching Loss *		1350	1550	µJ	Ic = 20A, V_{CC} = 600V	12, 14
E_{off}	Turn-off Switching Loss *		610	875		V_{GE} = 15V, Rg = 5Ω, L = 200µH	CT4
E_{tot}	Total Switching Loss *		1960	2425		T_J = 125°C, Energy losses include tail and diode reverse recovery	WF1 & 2
td(on)	Turn - on delay time		50	65	ns	Ic = 20A, V_{CC} = 600V	13, 15
tr	Rise time		20	30		V_{GE} = 15V, Rg = 5Ω, L = 200µH	CT4
td(off)	Turn - off delay time		204	230		T_J = 125°C	WF1
tf	Fall time		24	35			WF2
C_{ies}	Input Capacitance		2200		pF	V_{GE} = 0V	
C_{oes}	Output Capacitance		210			V_{CC} = 30V	16
C_{res}	Reverse Transfer Capacitance		85			f = 1.0 MHz	
RBSOA	Reverse bias safe operating area	FULL SQUARE				T_J = 150°C, Ic = 120A V_{CC} = 1000V, V_P = 1200V Rg = 5Ω, V_{GE} = +15V to 0V	4 CT2
SCSOA	Short Circuit Safe Operating Area	10	----	----	µs	T_J = 150°C V_{CC} = 900V, V_P = 1200V Rg = 5Ω, V_{GE} = +15V to 0V	CT3 WF3
Le	Internal Emitter Inductance		13		nH	Measured 5 mm from the package.	

* Used Diode HF40D120ACE

Fig.1 - Maximum DC Collector Current vs. Case Temperature

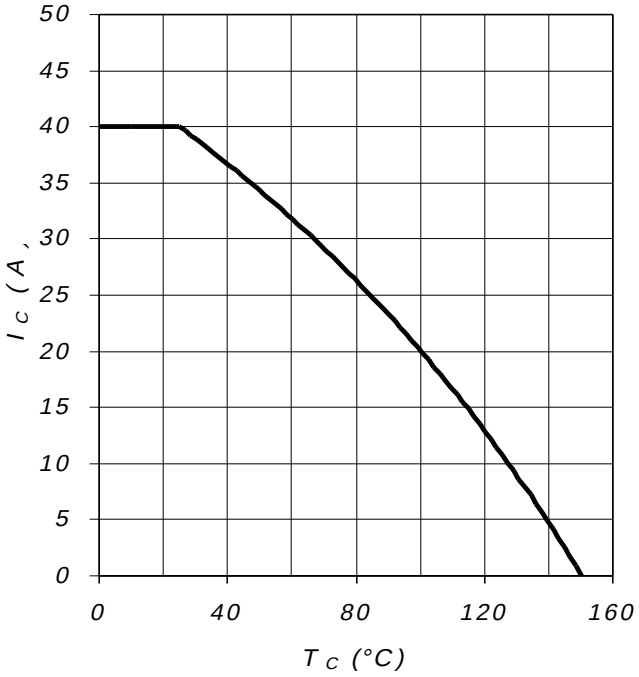


Fig.2 - Power Dissipation vs. Case Temperature

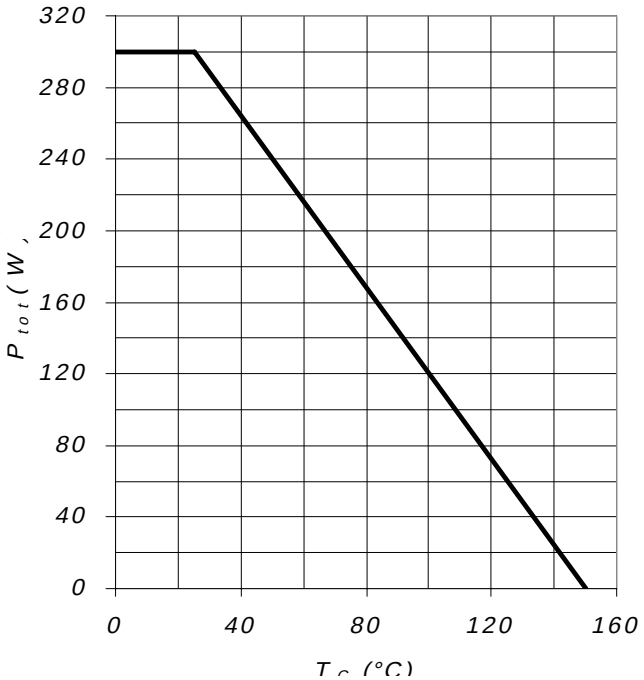


Fig.3 - Forward SOA
T_C=25°C; Tj≤150°C

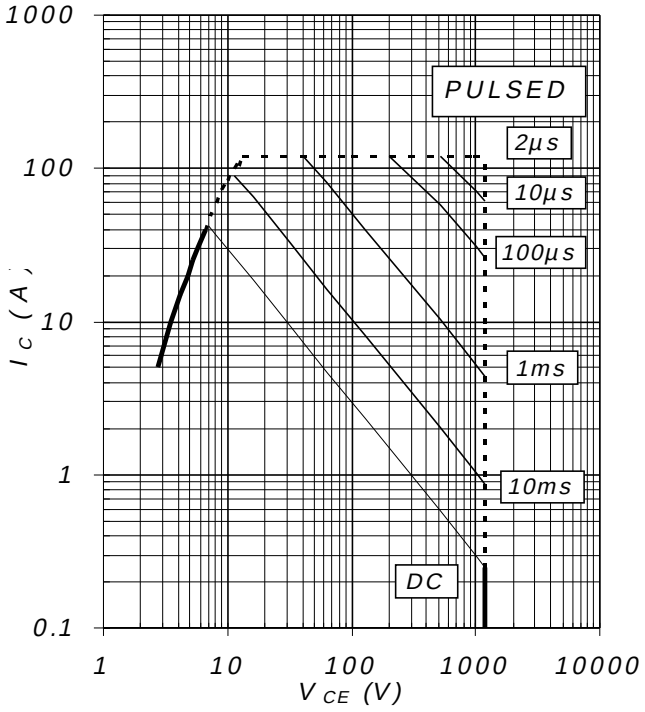


Fig.4 - Reverse Bias SOA
Tj = 150°C, V_{GE} = 15V

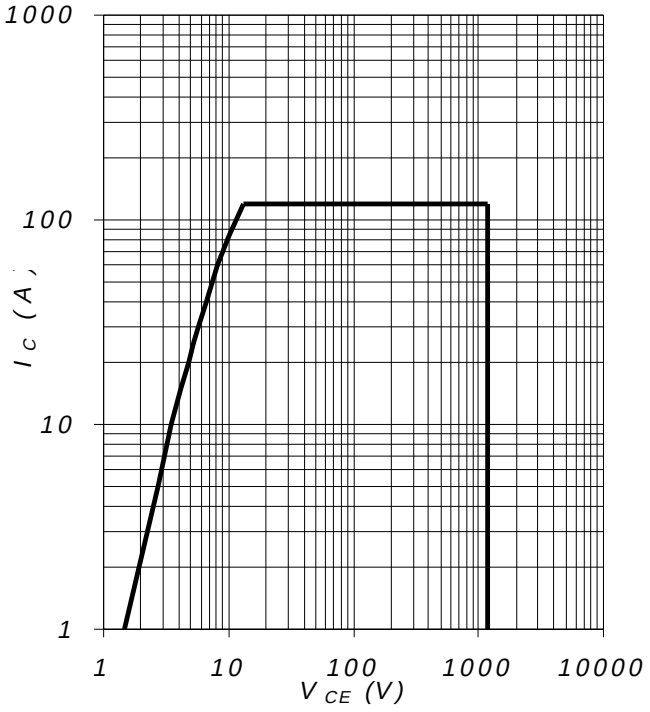


Fig.5 - Typical IGBT Output Characteristics
Tj= -40°C; tp=300µs

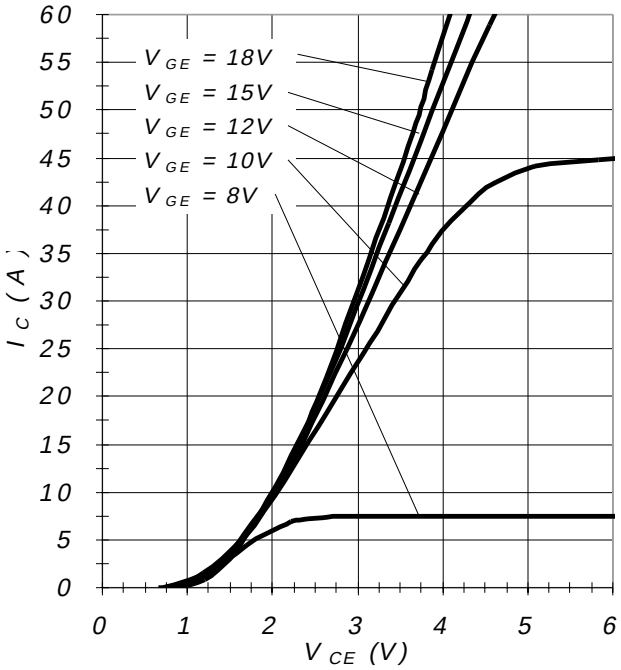


Fig.6 - Typical IGBT Output Characteristics
Tj=25°C; tp=300µs

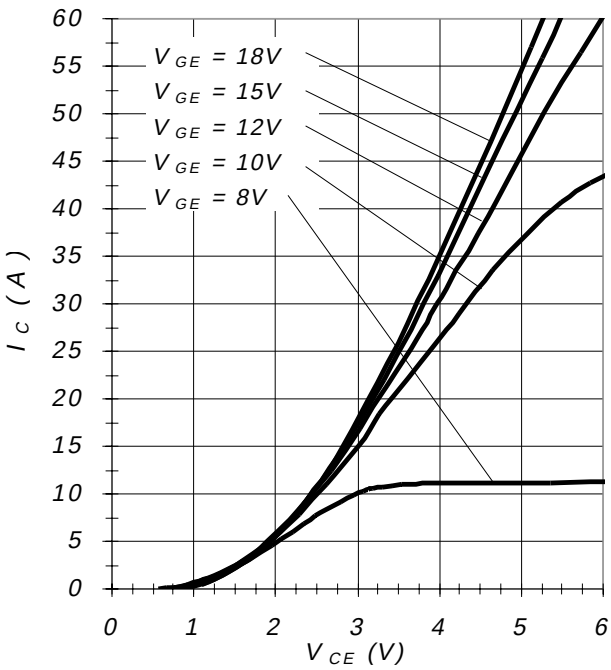


Fig.7 - Typical IGBT Output Characteristics
Tj=125°C; tp=300µs

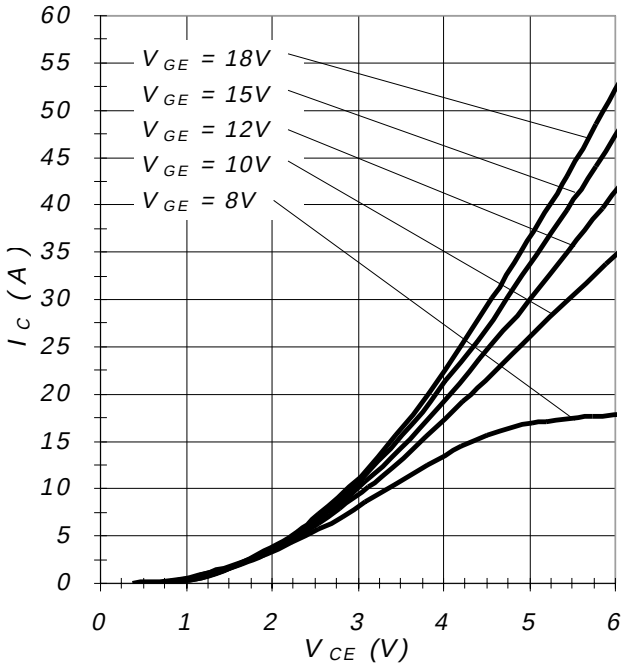


Fig. 8 - Typical V_{CE} vs V_{GE}
Tj= -40°C

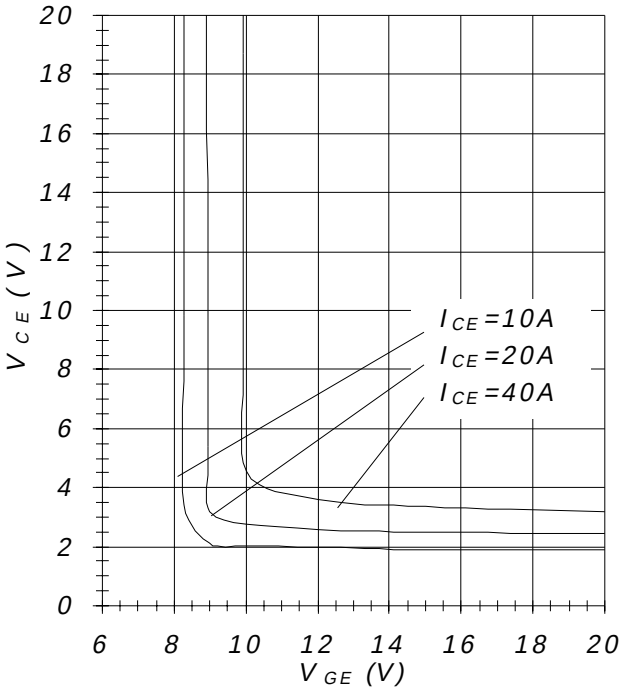


Fig. 9 - Typical V_{CE} vs V_{GE}
Tj= 25°C

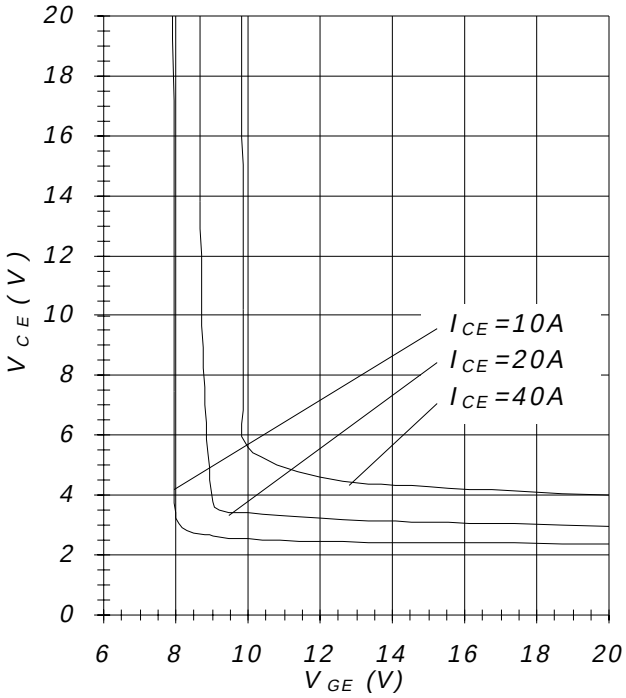


Fig. 10 - Typical V_{CE} vs V_{GE}
Tj= 125°C

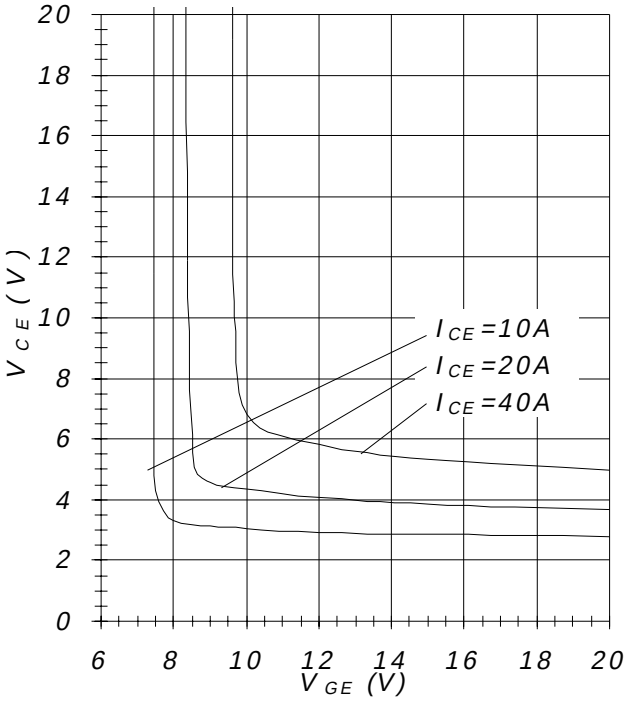


Fig. 11 - Typ. Transfer Characteristics
V_{CE}=20V; tp=20µs

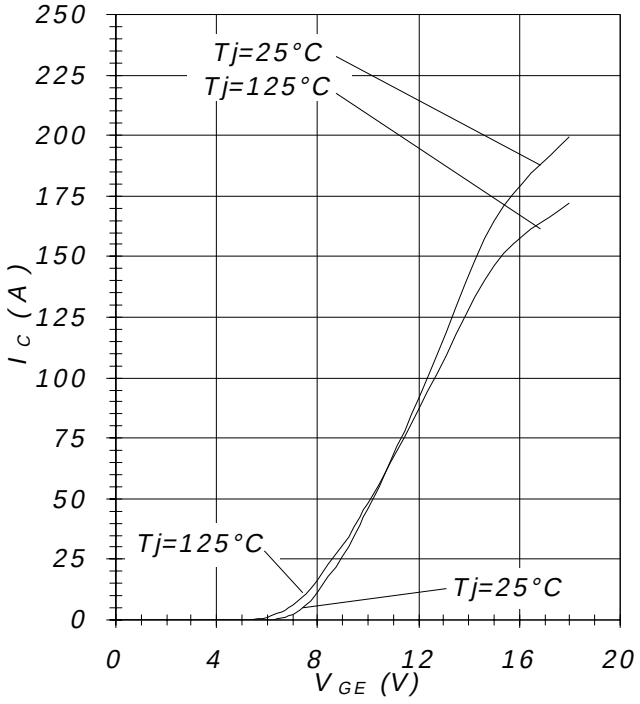


Fig.12 - Typical Energy Loss vs Ic
Tj=125°C; L=200µH; V_{CE}=600V;
Rg=22 Ω; V_{GE}=15V

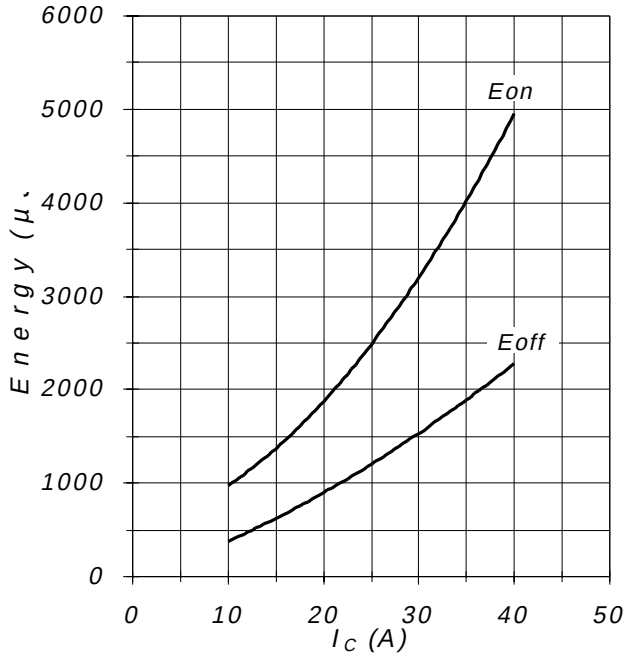


Fig.13 - Typical Switching Time vs Ic
Tj=125°C; L=200µH; V_{CE}=600V;
Rg=22 Ω; V_{GE}=15V

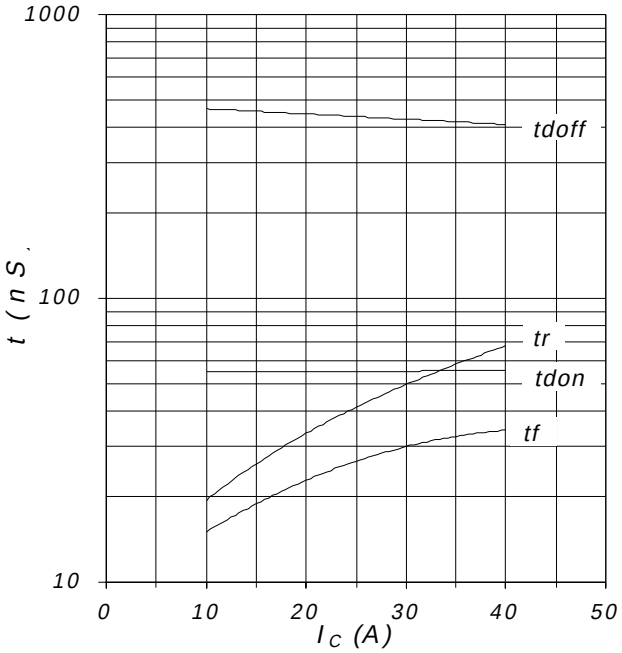


Fig.14 - Typical Energy Loss vs Rg
Tj=125°C; L=200µH; V_{CE}=600V;
I_{CE}=20A; V_{GE}=15V

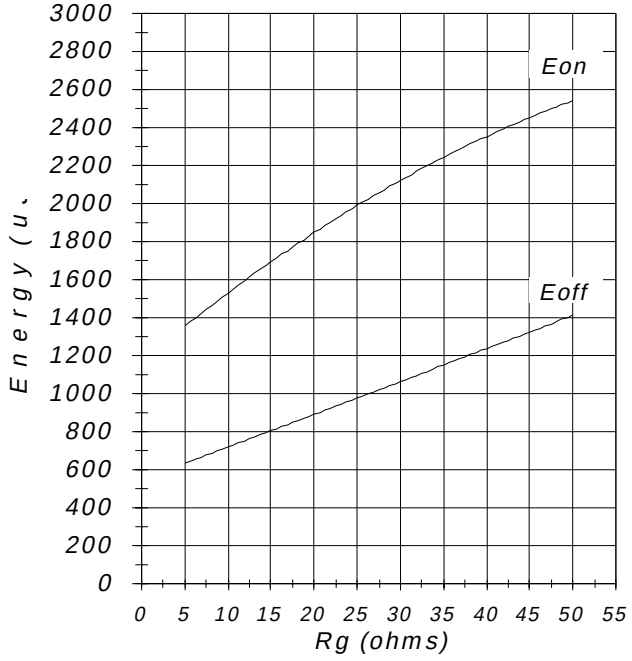


Fig.15 - Typical Switching Time vs Rg
Tj=125°C; L=200µH; V_{CE}=600V;
I_{CE}=20A; V_{GE}=15V

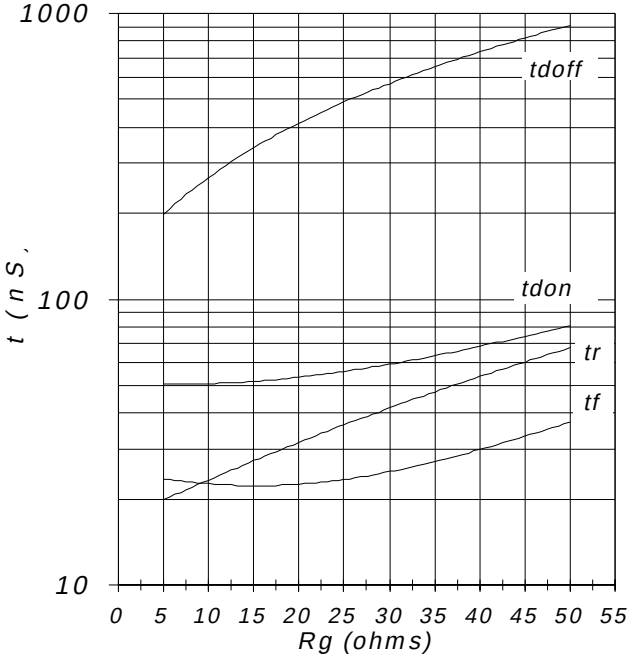


Fig.16 - Typical Capacitance vs V_{CE}
V_{GE}=0V; f=1MHz

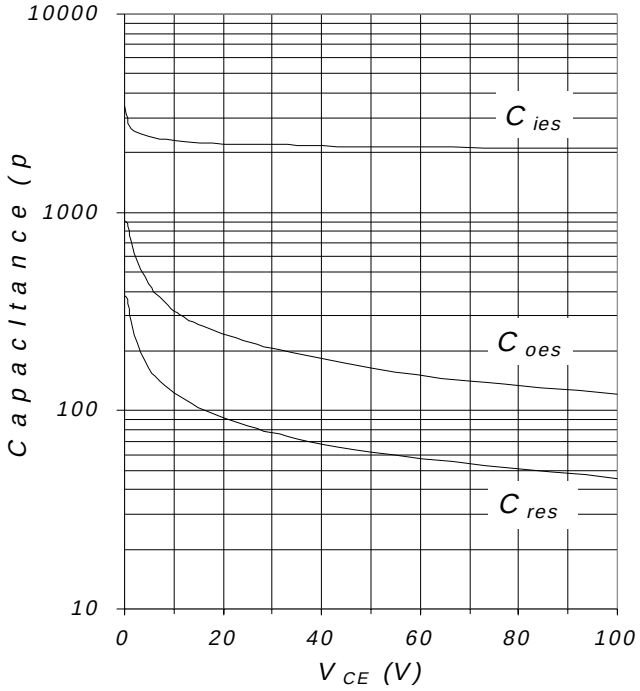


Fig.17 - Typ. Gate Charge vs. V_{GE}
I_C=20A; L=600µH

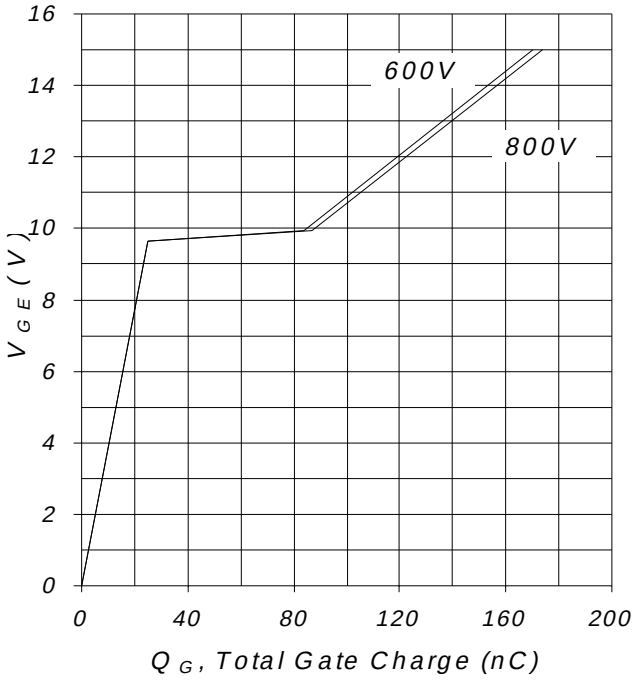


Fig. 18 - Normalized Transient Thermal Impedance, Junction-to-Case

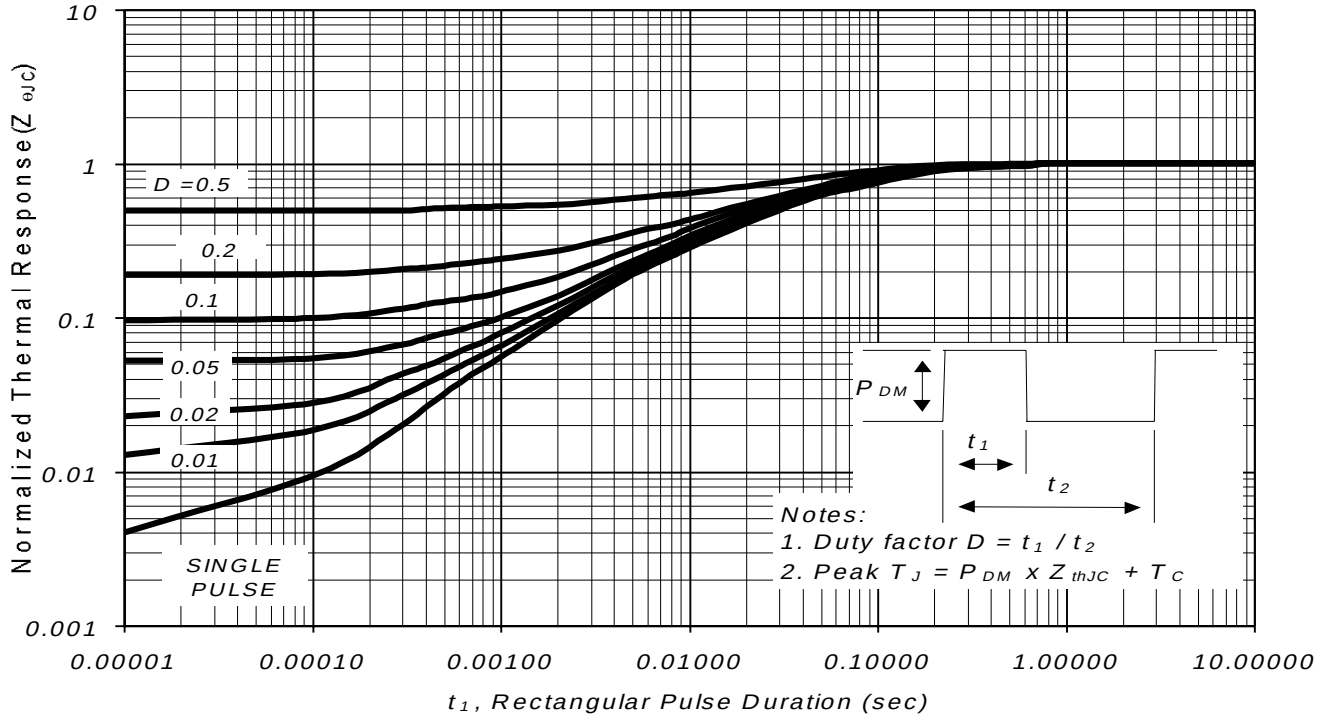


Fig. CT.1 - Gate Charge Circuit (turn-off)

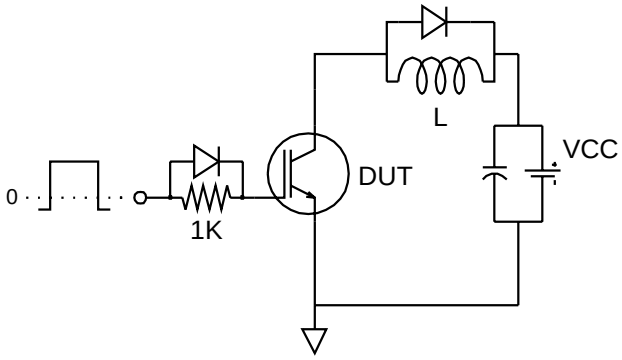


Fig. CT.2 - RBSOA Circuit

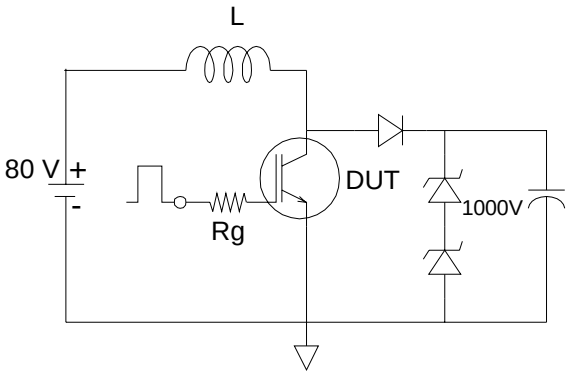


Fig. CT.3 - S.C. SOA Circuit

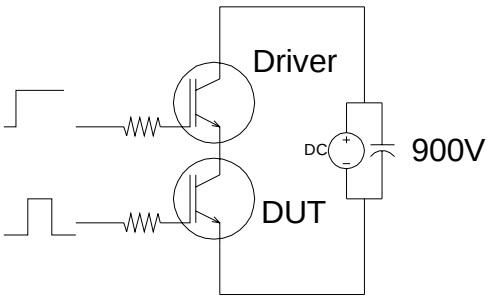


Fig. CT.4 - Switching Loss Circuit

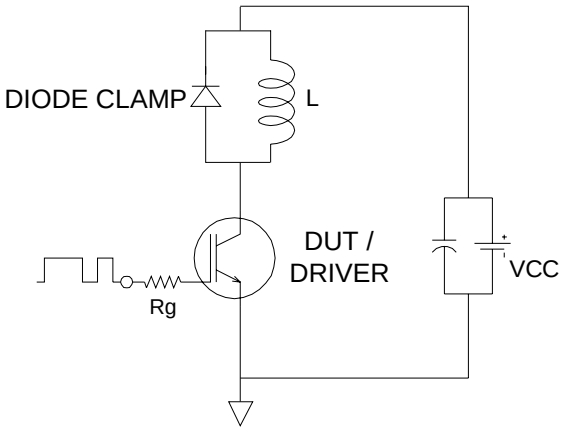


Fig. CT.5 - Resistive Load Circuit

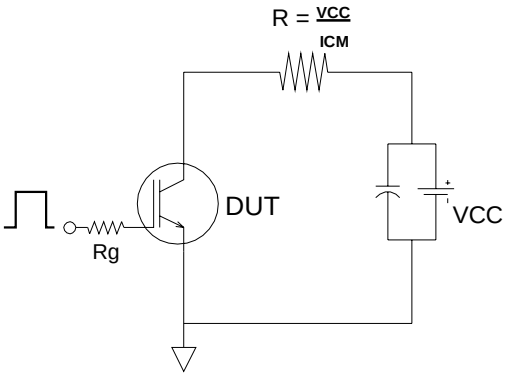


Fig. CT.6 - Unclamped Inductive Load Circuit

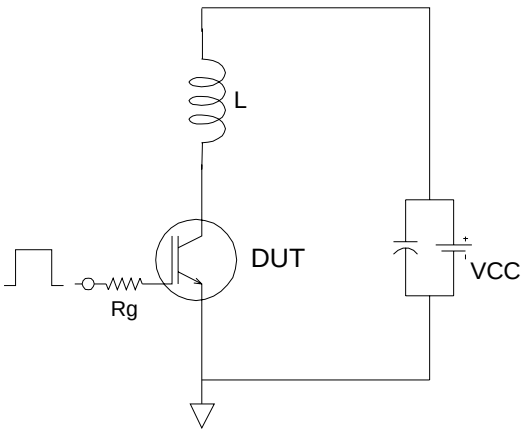


Fig. WF.1 - Typ. Turn-off Loss Waveform
@ Tj=125°C using Fig. CT.4

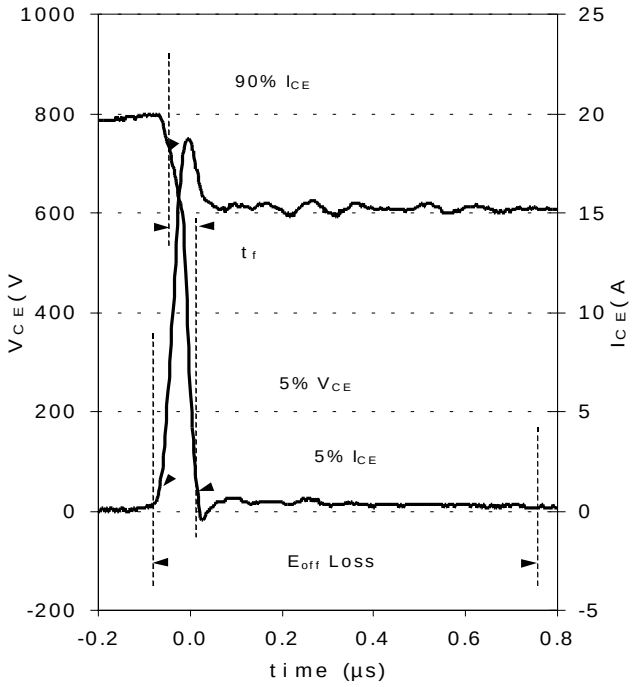


Fig. WF.2 - Typ. Turn-on Loss Waveform
@ Tj=125°C using Fig. CT.4

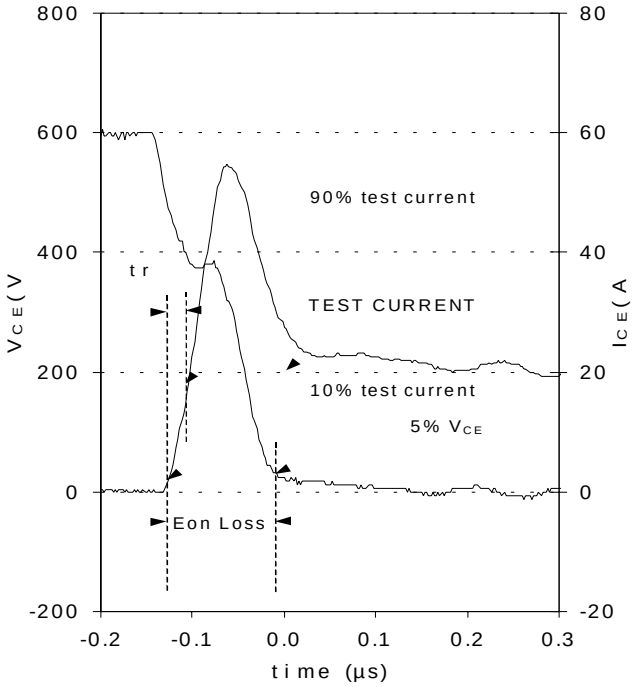
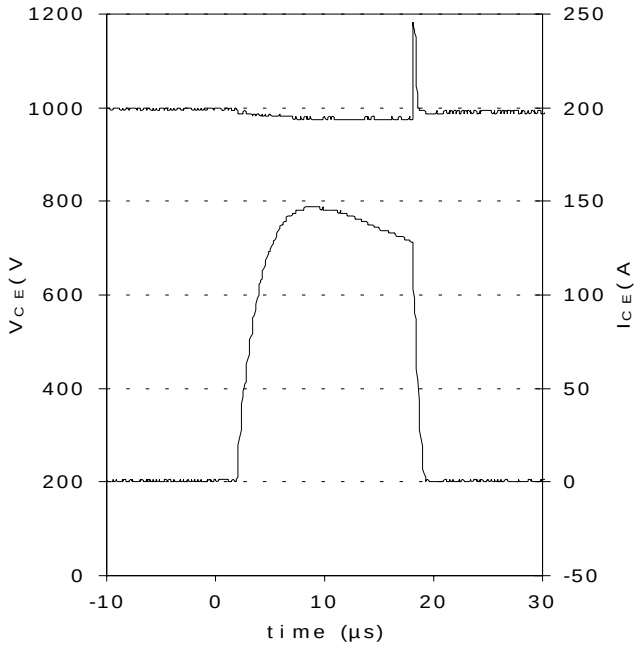
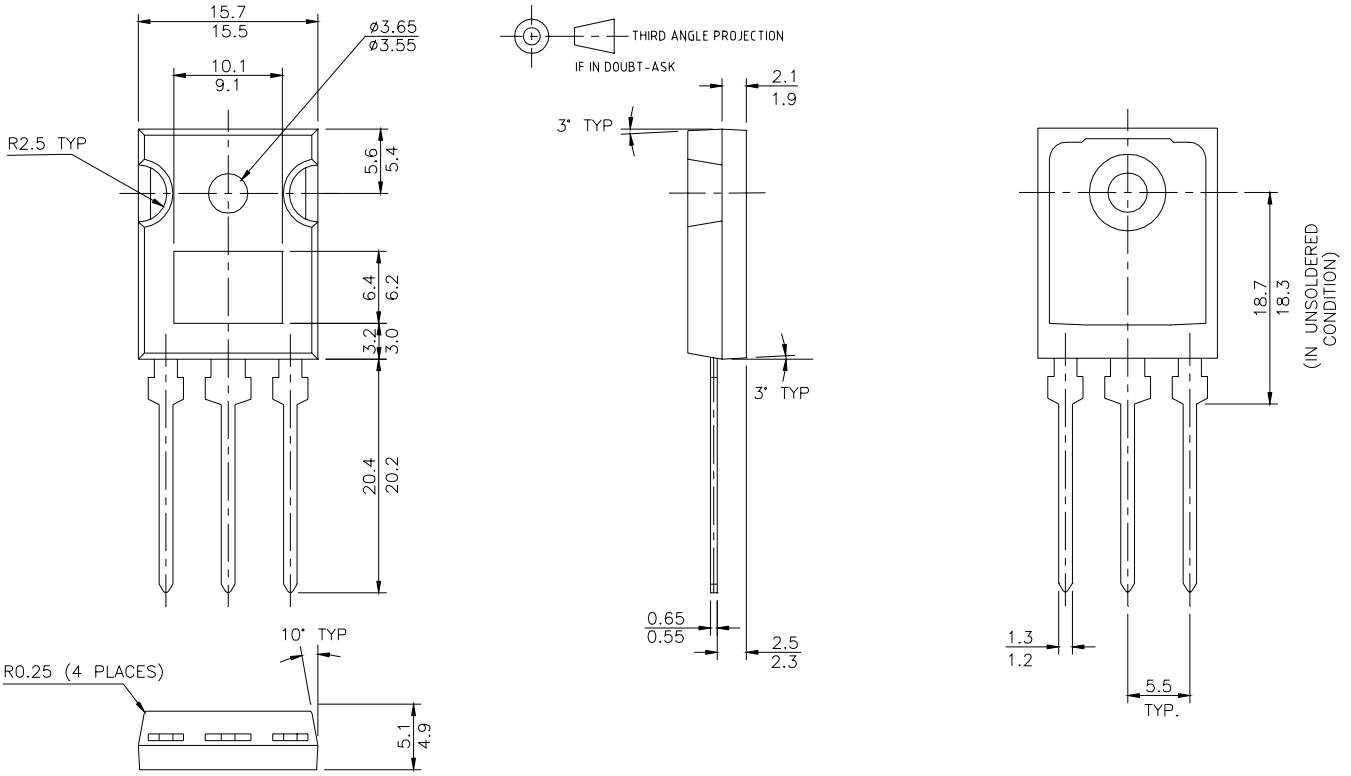


Fig. WF.3- Typ. S.C. Waveform
@ T_C=150°C using Fig. CT.3



TO-247AD Case Outline and Dimensions



Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.03/01

PD- 93817

International
IOR Rectifier

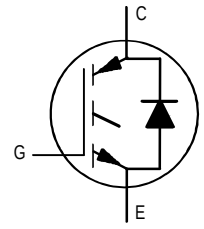
IRGP20B120UD-E

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

UltraFast CoPack IGBT

Features

- UltraFast Non Punch Through (NPT) Technology
- Low Diode V_F (1.67V Typical @ 20A & 25°C)
- 10 µs Short Circuit Capability
- Square RBSOA
- UltraSoft Diode Recovery Characteristics
- Positive $V_{CE(on)}$ Temperature Coefficient
- Extended Lead TO-247AD Package



N-channel

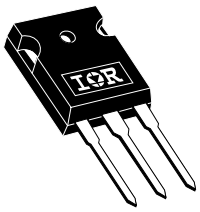
V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 3.05V

V_{GE} = 15V, I_C = 20A, 25°C

Benefits

- Benchmark Efficiency Above 20KHz
- Optimized for Welding, UPS, and Induction Heating Applications
- Rugged with UltraFast Performance
- Low EMI
- Significantly Less Snubber Required
- Excellent Current Sharing in Parallel Operation
- Longer Leads for Easier Mounting



TO-247AD

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current (Fig.1)	40	A
I_C @ T_C = 100°C	Continuous Collector Current (Fig.1)	20	
I_{CM}	Pulsed Collector Current (Fig.3, Fig. CT.5)	120	
I_{LM}	Clamped Inductive Load Current(Fig.4, Fig. CT.2)	120	
I_F @ T_C = 100°C	Diode Continuous Forward Current	20	
I_{FM}	Diode Maximum Forward Current	120	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation (Fig.2)	300	W
P_D @ T_C = 100°C	Maximum Power Dissipation (Fig.2)	120	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300, (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	——	——	0.42	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	——	——	0.83	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	——	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	——	40	
W_t	Weight	——	6 (0.21)	——	g (oz)
$Z_{\theta JC}$	Transient Thermal Impedance Junction-to-Case (Fig.24)				

Electrical Characteristics @ TJ = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	Fig.
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200			V	V_{GE} = 0V, I_c =250 µA	
$\Delta V_{(BR)CES} / \Delta Tj$	Temperature Coeff. of Breakdown Voltage		+1.2		V/°C	V_{GE} = 0V, I_c = 1 mA (25 -125 °C)	
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage		3.05	3.45	V	I_C = 20A, V_{GE} = 15V	5, 6
			3.37	3.80		I_C = 25A, V_{GE} = 15V	7, 9
			4.23	4.85		I_C = 40A, V_{GE} = 15V	10
			3.89	4.50		I_C = 20A, V_{GE} = 15V, T_J = 125°C	11
			4.31	5.06		I_C = 25A, V_{GE} = 15V, T_J = 125°C	
$V_{GE(th)}$	Gate Threshold Voltage	4.0	5.0	6.0	V	V_{CE} = V_{GE}, I_C = 250 µA	9,10,11,12
$\Delta V_{GE(th)} / \Delta Tj$	Temperature Coeff. of Threshold Voltage		- 1.2		mV/°C	V_{CE} = V_{GE}, I_C = 1 mA (25 -125 °C)	
g_{fe}	Forward Transconductance	13.6	15.7	17.8	S	V_{CE} = 50V, I_C = 20A, PW=80µs	
I_{CES}	Zero Gate Voltage Collector Current			250	µA	V_{GE} = 0V, V_{CE} = 1200V	
			420	750		V_{GE} = 0V, V_{CE} = 1200V, T_J =125°C	
			1482	2200		V_{GE} = 0V, V_{CE} = 1200V, T_J =150°C	
V_{FM}	Diode Forward Voltage Drop		1.67	1.96	V	I_C = 20A	8
			1.76	2.06		I_C = 25A	
			1.73	2.03		I_C = 20A, T_J = 125°C	
			1.87	2.18		I_C = 25A, T_J = 125°C	
I_{GES}	Gate-to-Emitter Leakage Current			±100	nA	V_{GE} = ±20V	

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	Fig.
Q_g	Total Gate charge (turn-on)		169	254	nC	I_C = 20A	23
Q_{ge}	Gate - Emitter Charge (turn-on)		24	36		V_{CC} = 600V	CT1
Q_{gc}	Gate - Collector Charge (turn-on)		82	126		V_{GE} = 15V	
E_{on}	Turn-On Switching Loss		850	1050	µJ	I_C = 20A, V_{CC} = 600V	CT4
E_{off}	Turn-Off Switching Loss		425	650		V_{GE} = 15V, Rg = 5Ω, L = 200µH	WF1
E_{tot}	Total Switching Loss		1275	1800		T_J = 25°C, Energy losses include tail and diode reverse recovery	WF2
E_{on}	Turn-on Switching Loss		1350	1550	µJ	Ic = 20A, V_{CC} = 600V	13, 15
E_{off}	Turn-off Switching Loss		610	875		V_{GE} = 15V, Rg = 5Ω, L = 200µH	CT4
E_{tot}	Total Switching Loss		1960	2425		T_J = 125°C, Energy losses include tail and diode reverse recovery	WF1 & 2
td(on)	Turn - on delay time		50	65	ns	Ic = 20A, V_{CC} = 600V	14, 16
tr	Rise time		20	30		V_{GE} = 15V, Rg = 5Ω, L = 200µH	CT4
td(off)	Turn - off delay time		204	230		T_J = 125°C	WF1
tf	Fall time		24	35			WF2
C_{ies}	Input Capacitance		2200		pF	V_{GE} = 0V	
C_{oes}	Output Capacitance		210			V_{CC} = 30V	22
C_{res}	Reverse Transfer Capacitance		85			f = 1.0 MHz	
RBSOA	Reverse bias safe operating area	FULL SQUARE				T_J = 150°C, Ic = 120A V_{CC} = 1000V, V_P = 1200V Rg = 5Ω, V_{GE} = +15V to 0V	4 CT2
SCSOA	Short Circuit Safe Operating Area	10	----	----	µs	T_J = 150°C V_{CC} = 900V, V_P = 1200V Rg = 5Ω, V_{GE} = +15V to 0V	CT3 WF4
E_{rec}	Reverse recovery energy of the diode		1600	2100	µJ	T_J = 125°C	17,18,19
trr	Diode Reverse recovery time		300		ns	V_{CC} = 600V, Ic = 20A	20, 21
Irr	Peak Reverse Recovery Current		32	36	A	V_{GE} = 15V, Rg = 5Ω, L = 200µH	CT4, WF3
Le	Internal Emitter Inductance		13		nH	Measured 5 mm from the package.	

Fig.1 - Maximum DC Collector Current vs. Case Temperature

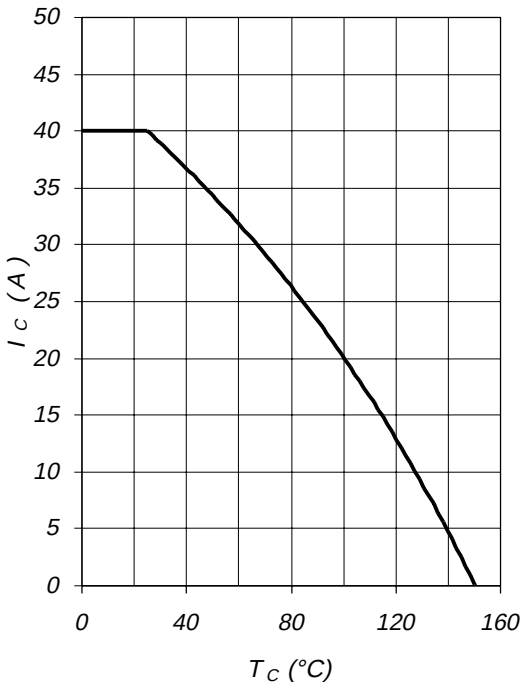


Fig.2 - Power Dissipation vs. Case Temperature

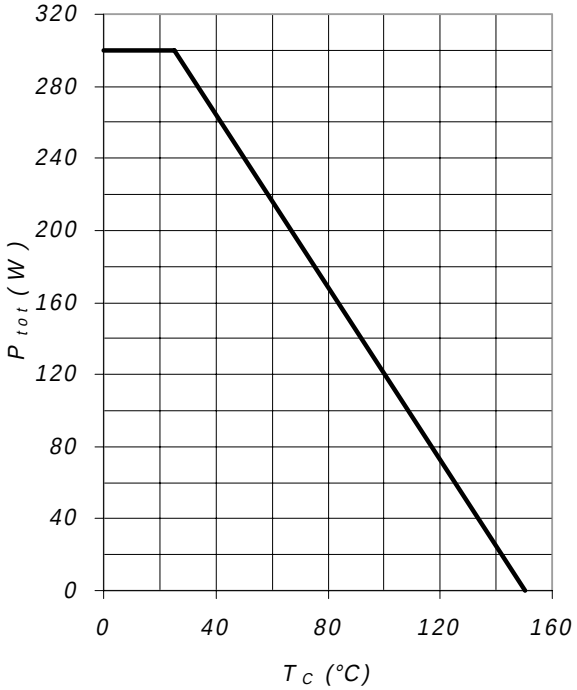


Fig.3 - Forward SOA
T_C=25°C; Tj≤150°C

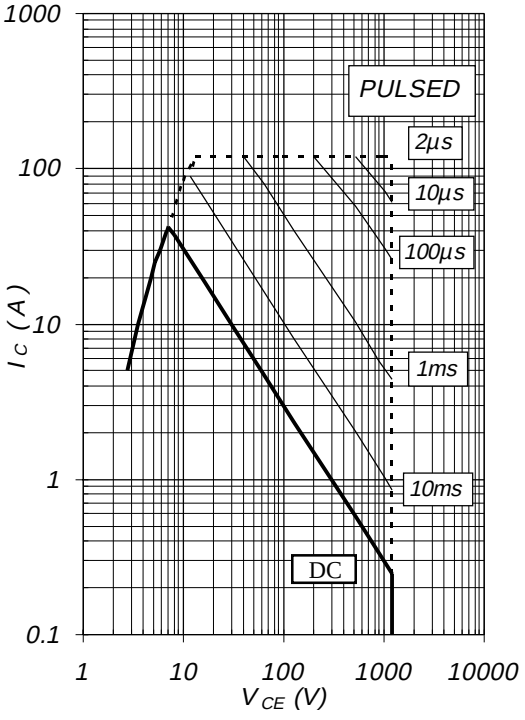


Fig.4 - Reverse Bias SOA
Tj = 150°C, V_{GE} = 15V

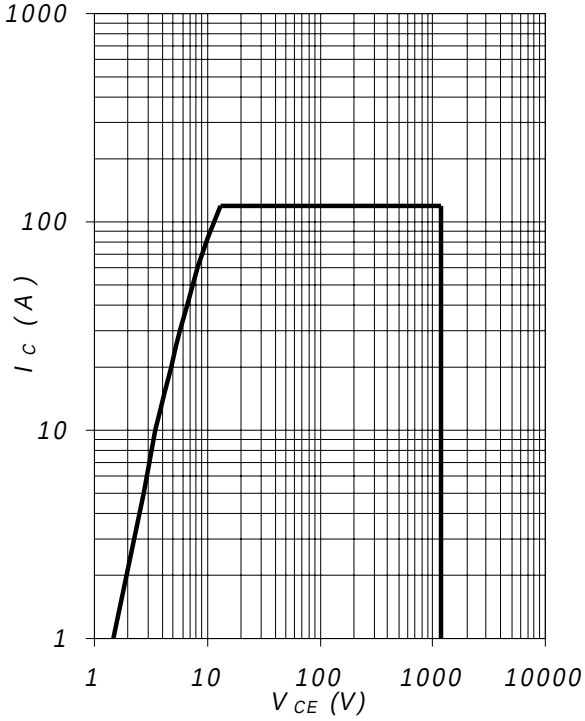


Fig.5 - Typical IGBT Output Characteristics
Tj= -40°C; tp=300µs

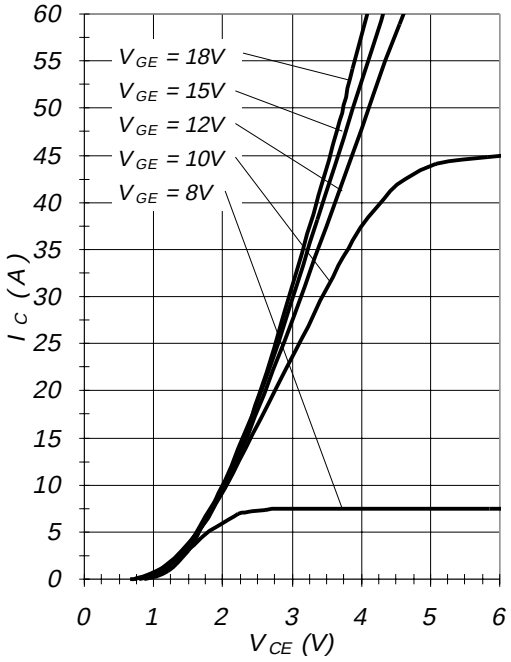


Fig.6 - Typical IGBT Output Characteristics
Tj=25°C; tp=300µs

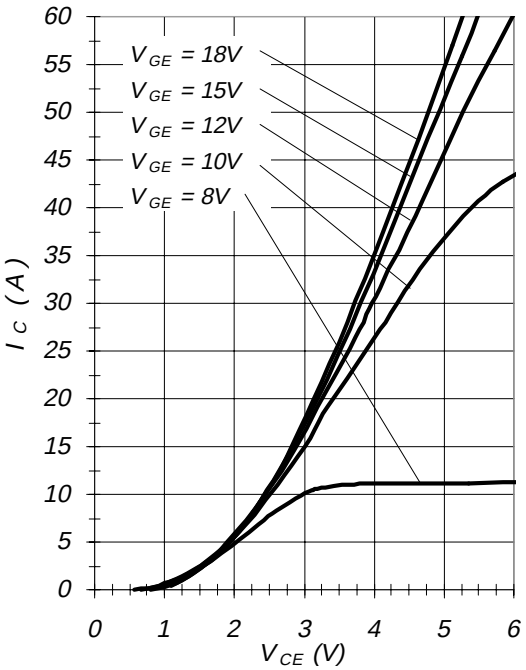


Fig.7 - Typical IGBT Output Characteristics
Tj=125°C; tp=300µs

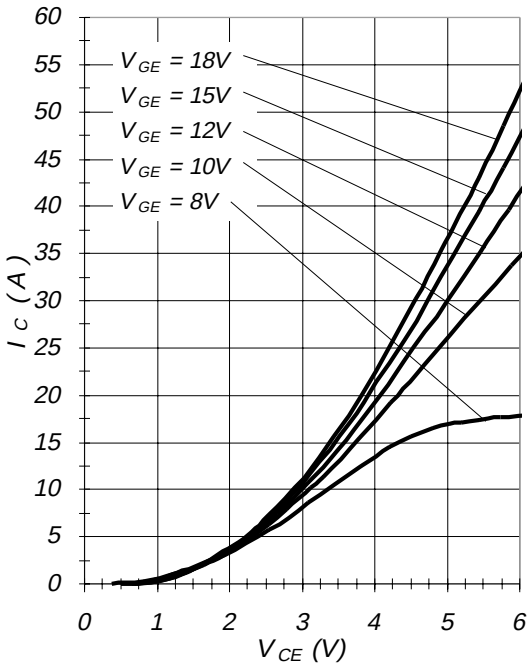


Fig.8 - Typical Diode Forward Characteristic
tp=300µs

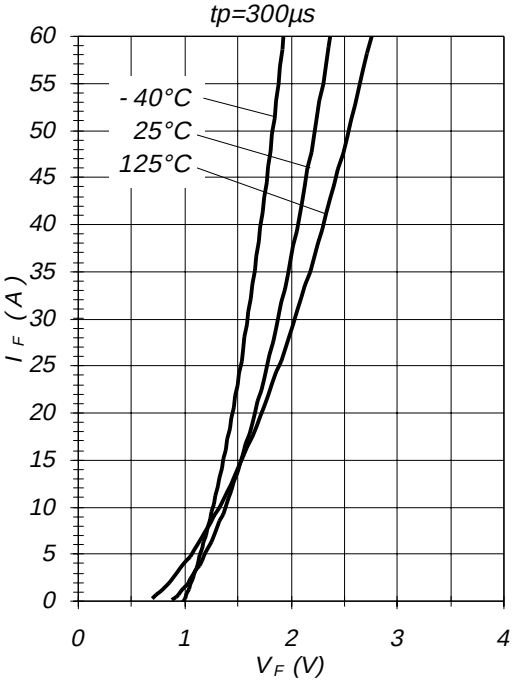


Fig.9 - Typical V_{CE} vs V_{GE}
Tj= -40°C

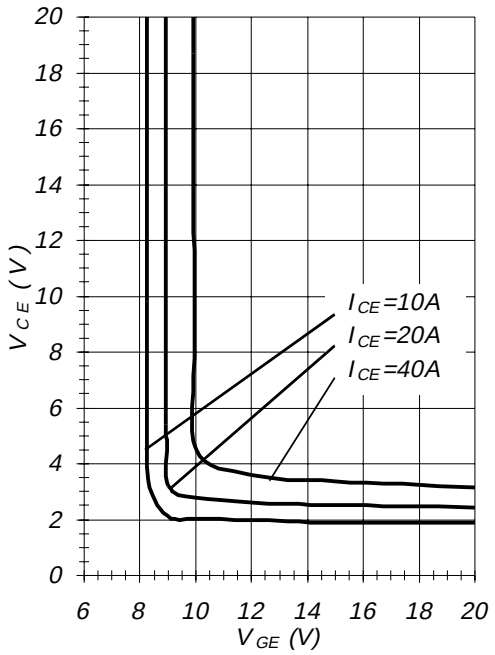


Fig.10 - Typical V_{CE} vs V_{GE}
Tj= 25°C

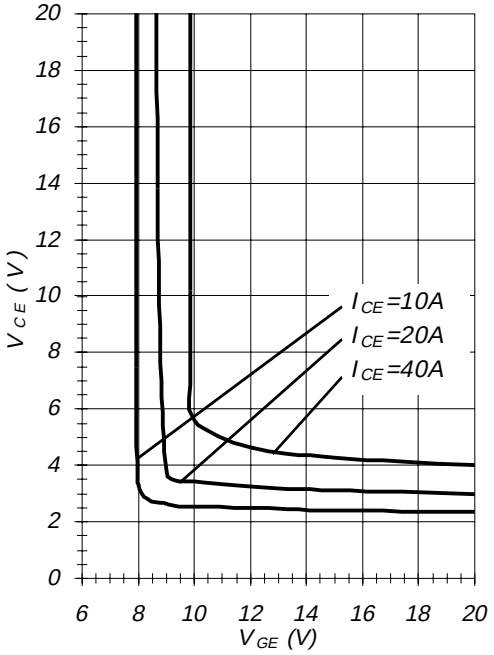


Fig.11 - Typical V_{CE} vs V_{GE}
Tj= 125°C

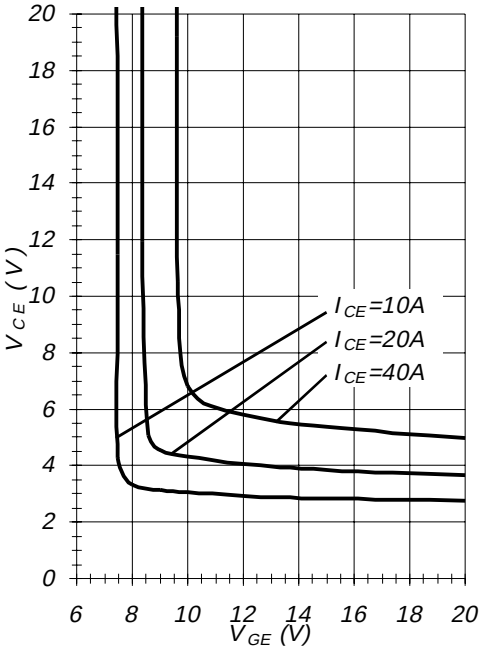


Fig.12 - Typ. Transfer Characteristics
V_{CE}=20V; tp=20µs

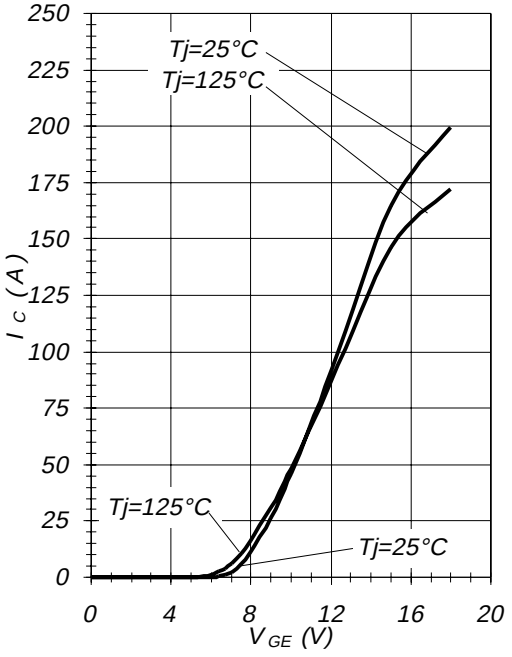


Fig.13 - Typical Energy Loss vs Ic
Tj=125°C; L=200µH; V_{CE}=600V;
Rg=22Ω; V_{GE}=15V

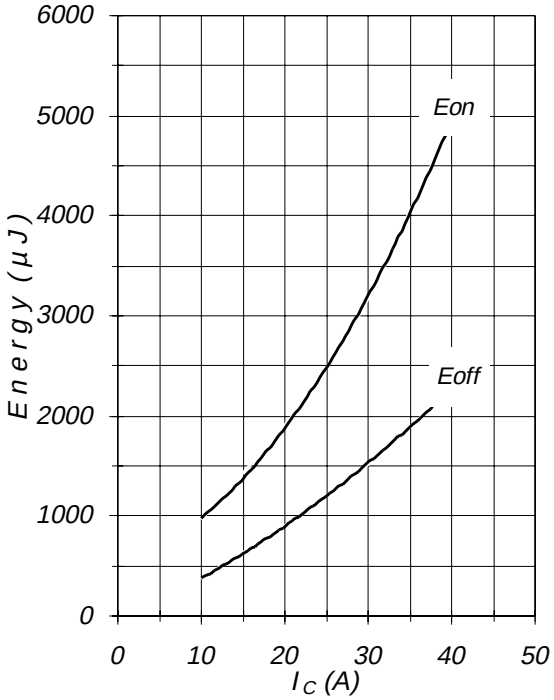


Fig.14 - Typical Switching Time vs Ic
Tj=125°C; L=200µH; V_{CE}=600V;
Rg=22Ω; V_{GE}=15V

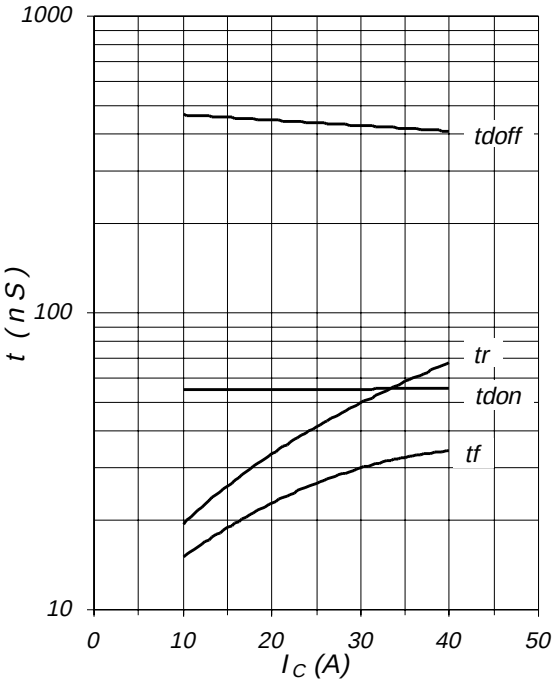


Fig.15 - Typical Energy Loss vs Rg
Tj=125°C; L=200µH; V_{CE}=600V;
I_{CE}=20A; V_{GE}=15V

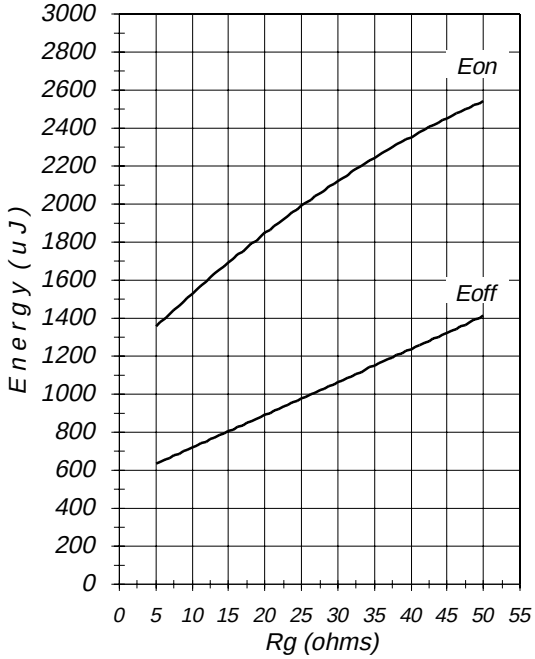


Fig.16 - Typical Switching Time vs Rg
Tj=125°C; L=200µH; V_{CE}=600V;
I_{CE}=20A; V_{GE}=15V

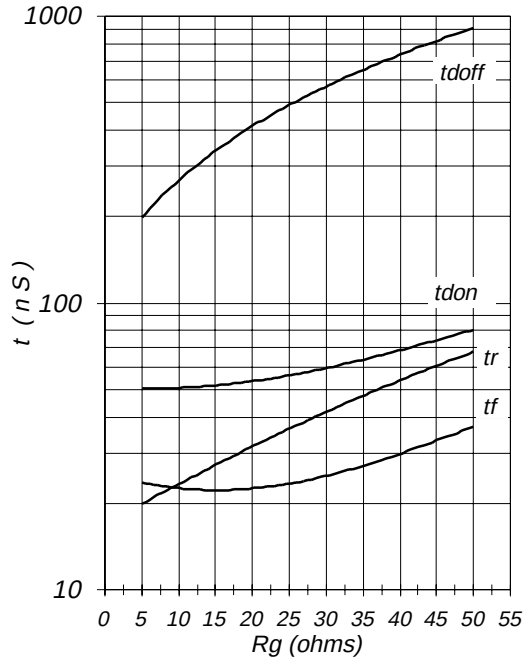


Fig.17 - Typical Diode I_{RR} vs I_F
Tj=125°C

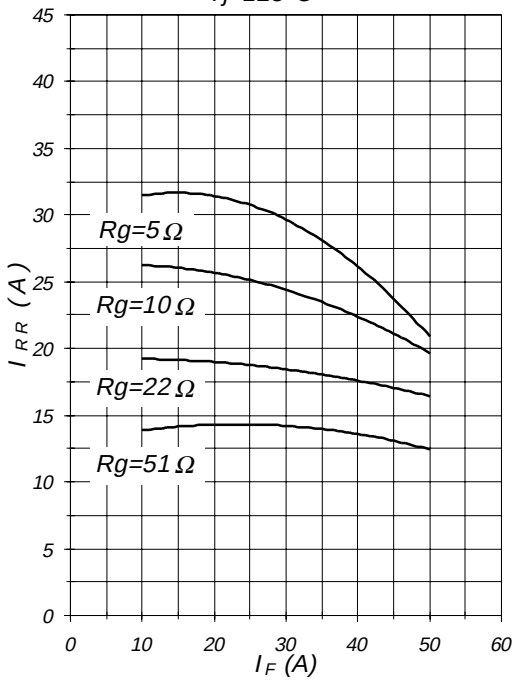


Fig.18 - Typical Diode I_{RR} vs Rg
Tj=125°C; I_F=20A



Fig.19 - Typical Diode I_{RR} vs dI_F/dt
V_{CC}=600V; V_{GE}=15V
I_F=20A; Tj=125°C

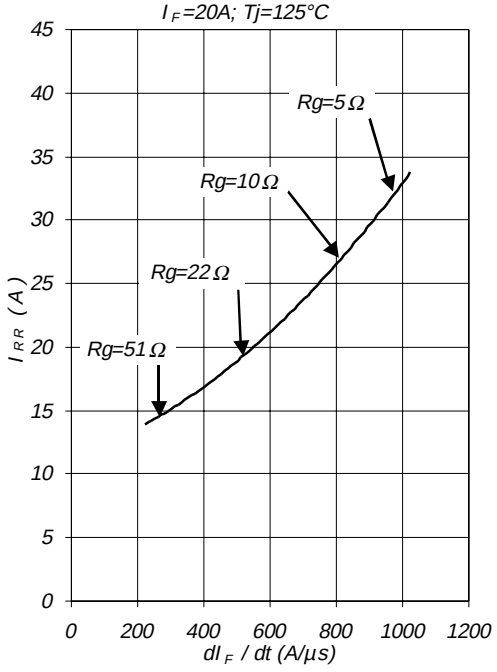


Fig.20 - Typical Diode Q_{RR}
V_{CC}=600V; V_{GE}=15V; Tj=125°C

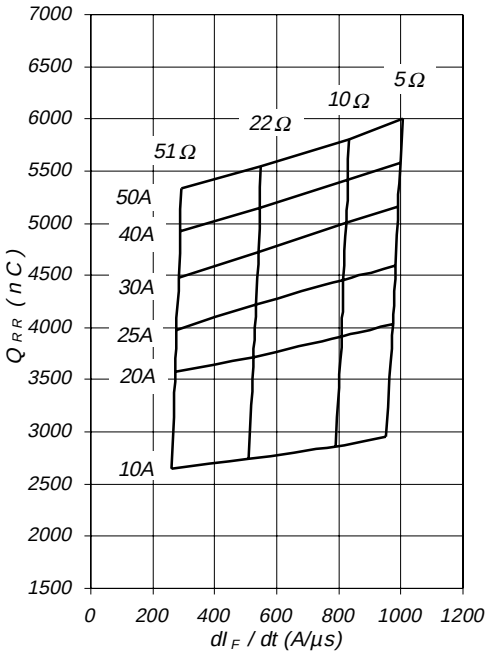


Fig.21 - Typ. Diode E_{rec} vs. I_F
Tj=125°C

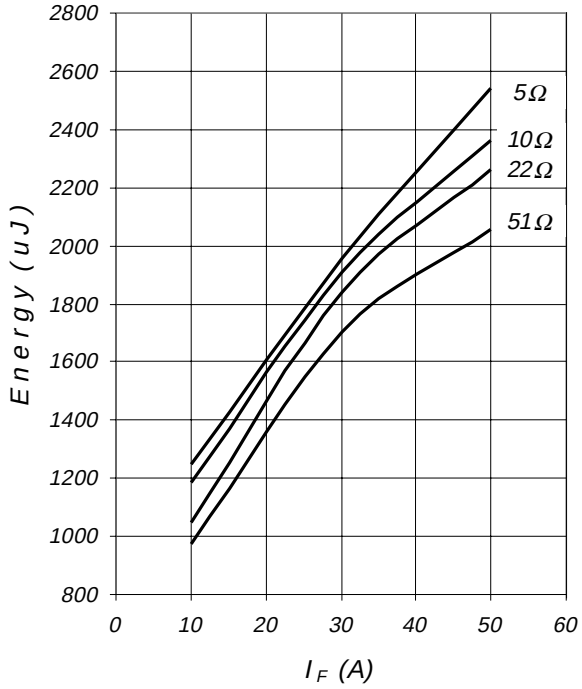


Fig.22 - Typical Capacitance vs V_{CE}
V_{GE}=0V; f=1MHz

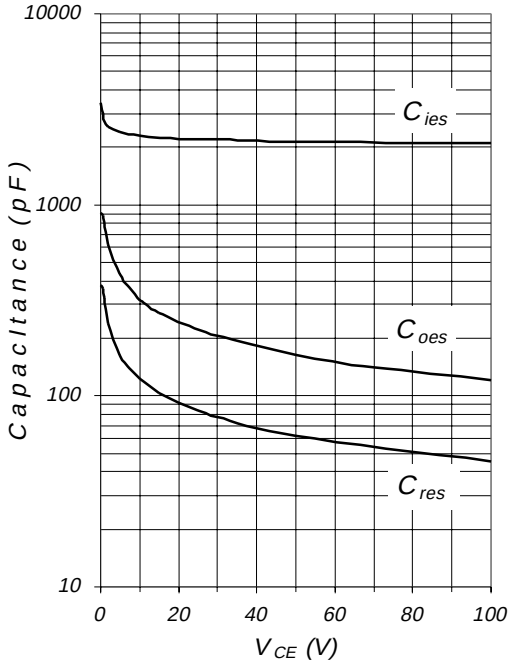


Fig.23 - Typ. Gate Charge vs. V_{GE}
I_C=20A; L=600µH

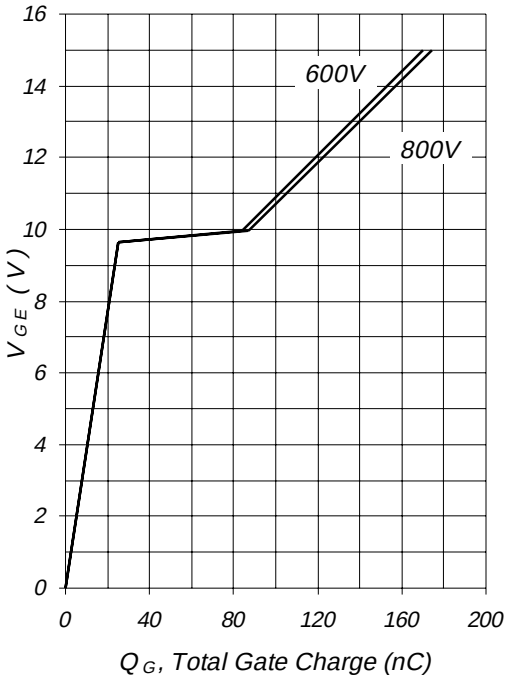


Fig.24 - Normalized Transient Thermal Impedance, Junction-to-Case

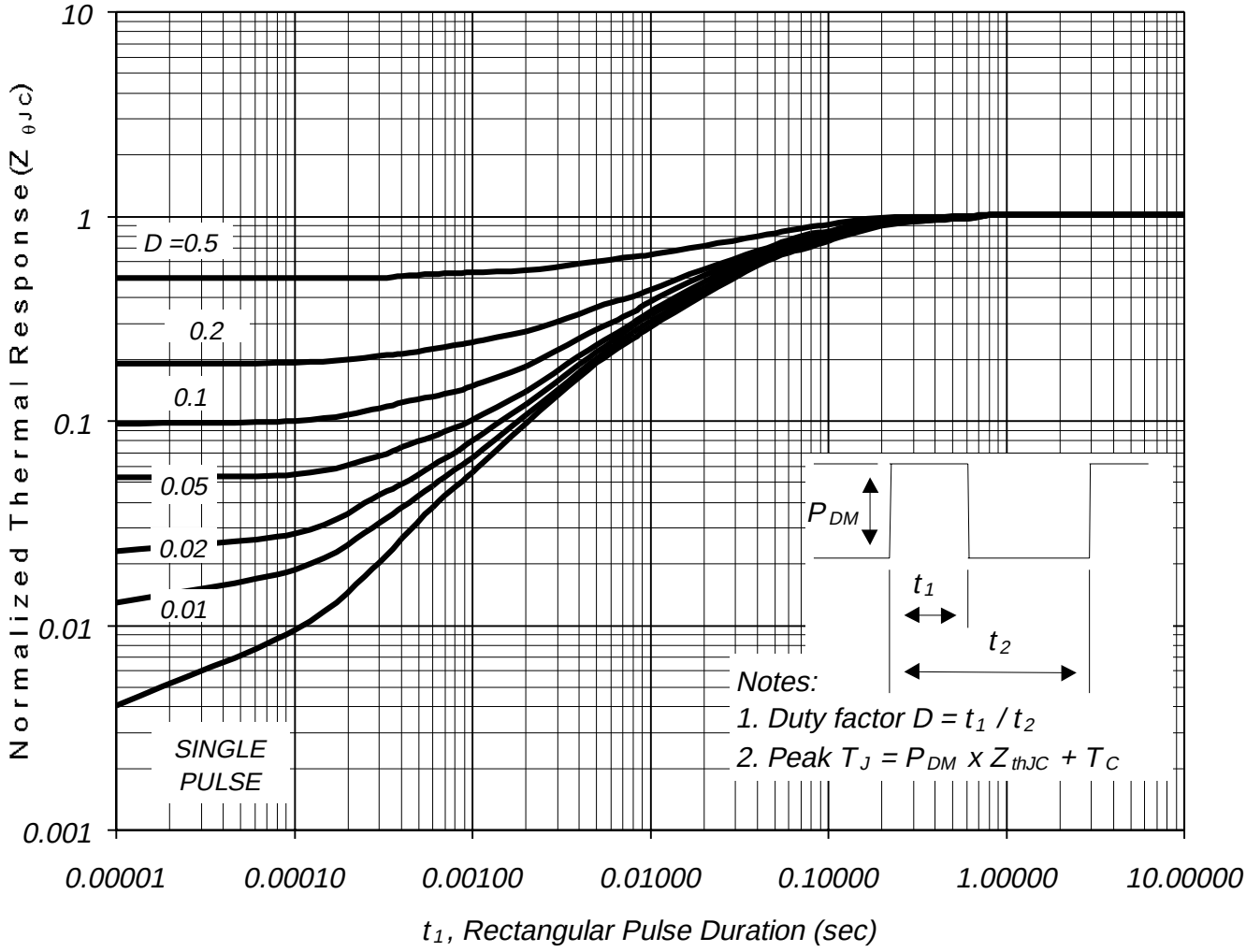


Fig. CT.1 - Gate Charge Circuit (turn-off)

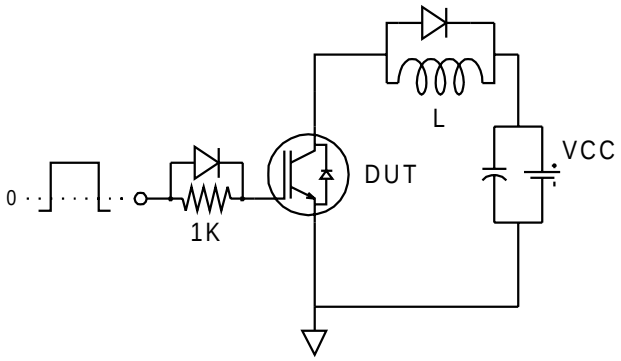


Fig. CT.2 - RBSOA Circuit

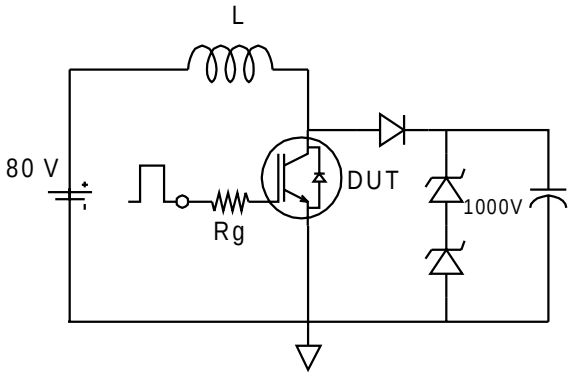


Fig. CT.3 - S.C. SOA Circuit

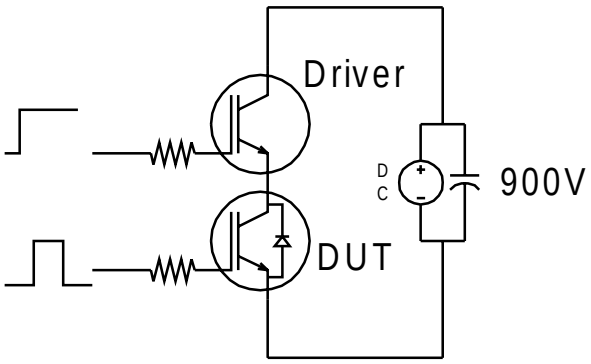


Fig. CT.4 - Switching Loss Circuit

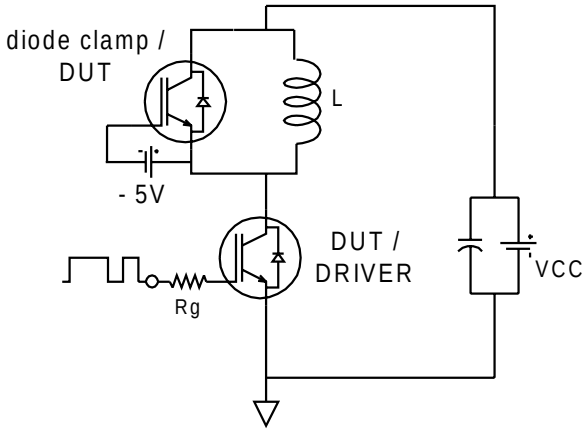


Fig. CT.5 - Resistive Load Circuit

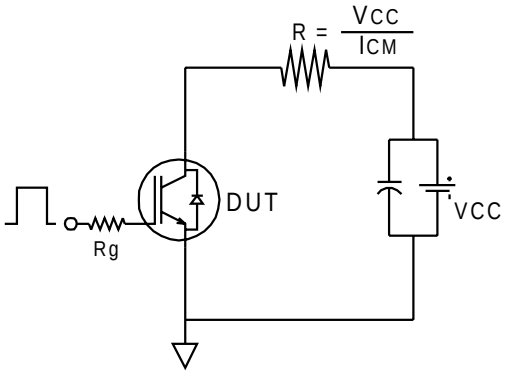


Fig. WF.1 - Typ. Turn-off Loss Waveform @ Tj=125°C using Fig. CT.4

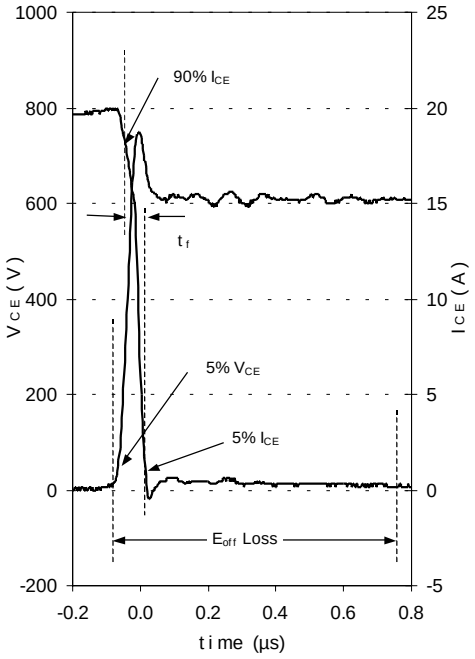


Fig. WF.2 - Typ. Turn-on Loss Waveform @ Tj=125°C using Fig. CT.4

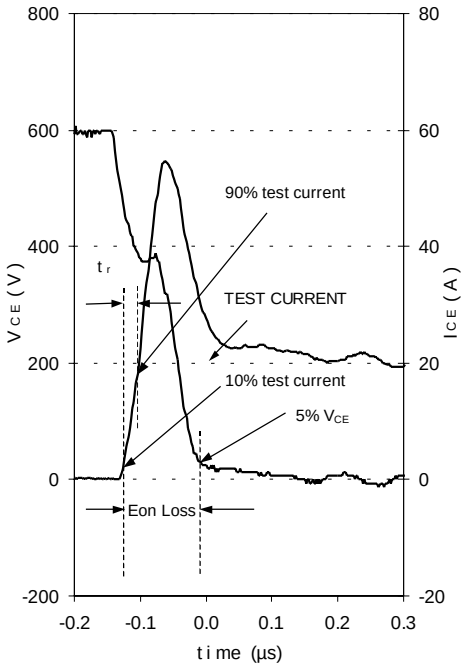


Fig. WF.3 - Typ. Diode Recovery Waveform @ Tj=125°C using Fig. CT.4

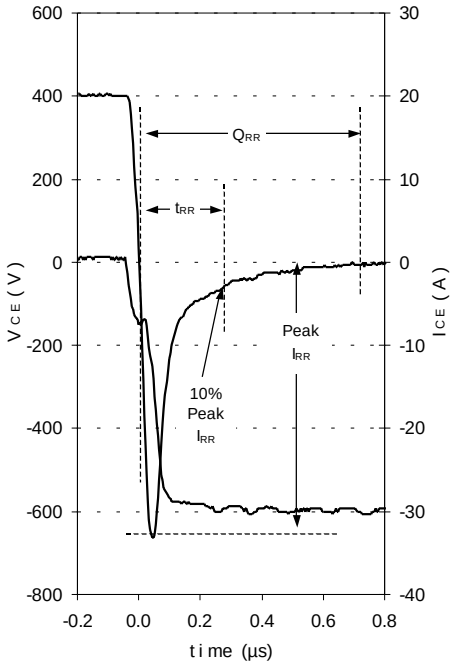
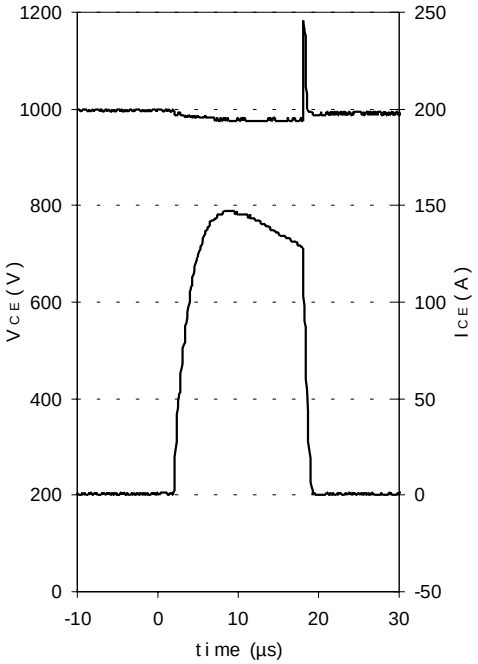
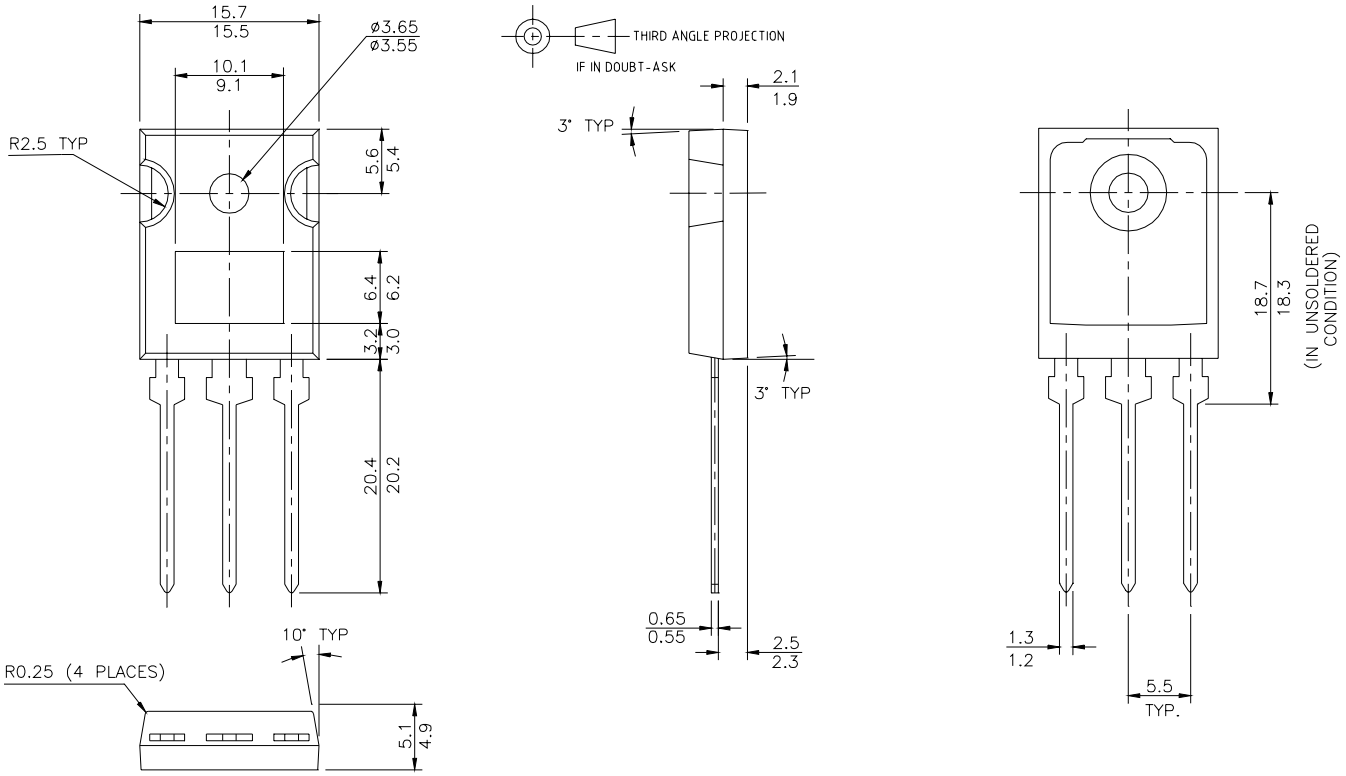


Fig. WF.4 - Typ. S.C. Waveform @ T_C=150°C using Fig. CT.3



TO-247AD Case Outline and Dimensions



International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 252-7105
IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936
Data and specifications subject to change without notice. 12/99

PD - 9.1576

International
IOR Rectifier

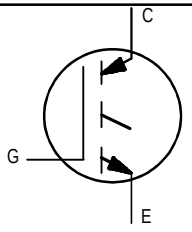
IRG4PH50K

INSULATED GATE BIPOLAR TRANSISTOR

Short Circuit Rated
UltraFast IGBT

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, V_{CC} = 720V, T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Latest generation design provides tighter parameter distribution and higher efficiency than previous generations



n-channel

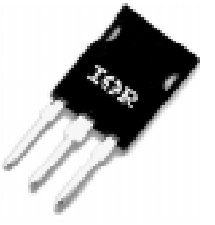
V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.77V

@V_{GE} = 15V, I_C = 24A

Benefits

- As a Freewheeling Diode we recommend our HEXFRED™ ultrafast, ultrasoft recovery diodes for minimum EMI/Noise and switching losses in the Diode and IGBT
- Latest generation 4 IGBTs offer highest power density motor controls possible
- This part replaces the IRGPH50K and IRGPH50M devices



TO-247 AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	45	A
I_C @ T_C = 100°C	Continuous Collector Current	24	
I_{CM}	Pulsed Collector Current ①	90	
I_{LM}	Clamped Inductive Load Current ②	90	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	190	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.64	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.91	—	V/°C	V_{GE} = 0V, I_C = 2.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.77	3.5	V	I_C = 24A V_{GE} = 15V
		—	3.28	—		I_C = 45A see figures 2, 5
		—	2.54	—		I_C = 24A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 2.0mA
g_{fe}	Forward Transconductance	13	19	—	S	V_{CE} = 100 V, I_C = 24A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	5000		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	180	270	nC	I_C = 24A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	25	38		V_{CC} = 400V see figure 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	70	110		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	36	—	ns	
t_r	Rise Time	—	27	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	200	300		I_C = 24A, V_{CC} = 960V
t_f	Fall Time	—	130	190		V_{GE} = 15V, R_G = 5.0Ω
E_{on}	Turn-On Switching Loss	—	1.21	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	2.25	—		see figures 9,10,14
E_{ts}	Total Switching Loss	—	3.46	4.1		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 720V, T_J = 125°C
						V_{GE} = 15V, R_G = 5.0Ω
$t_{d(on)}$	Turn-On Delay Time	—	35	—	ns	T_J = 150°C,
t_r	Rise Time	—	29	—		I_C = 24A, V_{CC} = 960V
$t_{d(off)}$	Turn-Off Delay Time	—	380	—		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	280	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	7.80	—	mJ	see figures 10,11,14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	2800	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	140	—		V_{CC} = 30V see figure 7
C_{res}	Reverse Transfer Capacitance	—	53	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited bymax. junction temperature. (see figure 13b)

② V_{CC} = 80% (V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 5.0Ω, (see figure 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

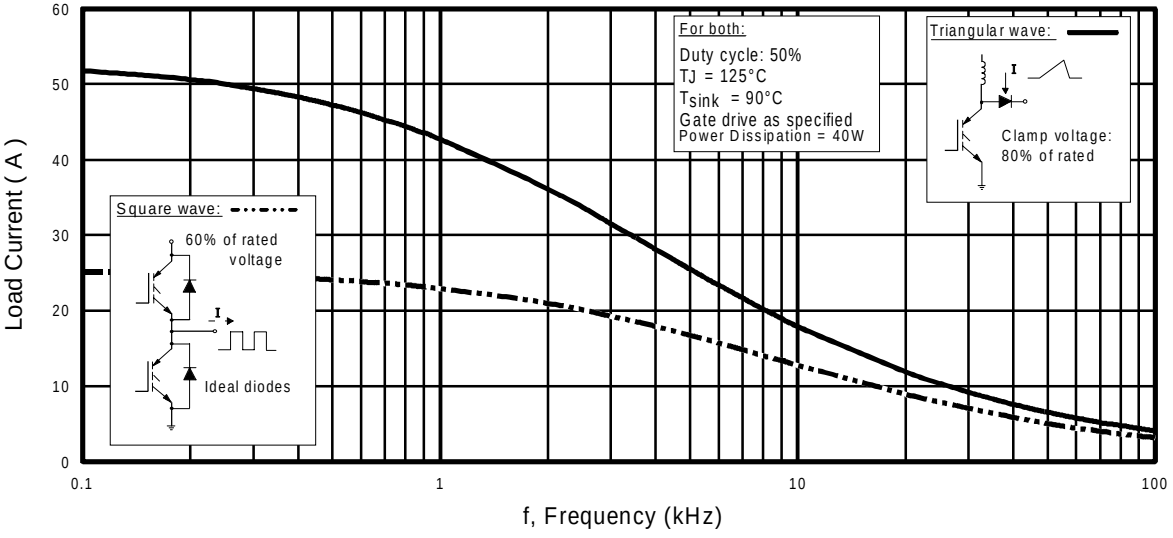


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

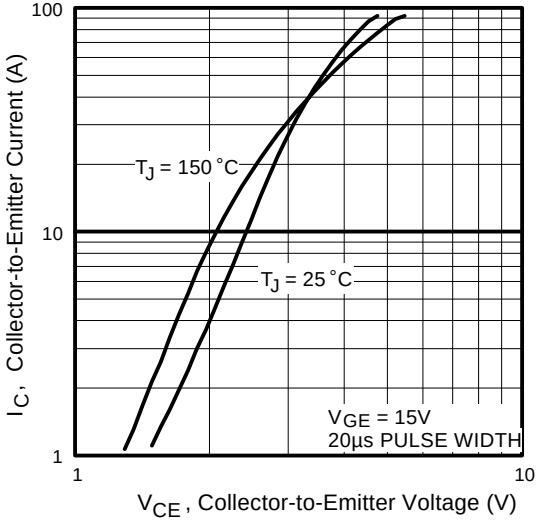


Fig. 2 - Typical Output Characteristics

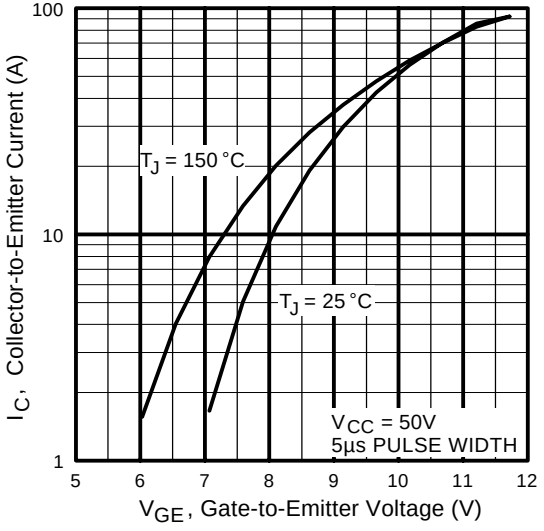


Fig. 3 - Typical Transfer Characteristics

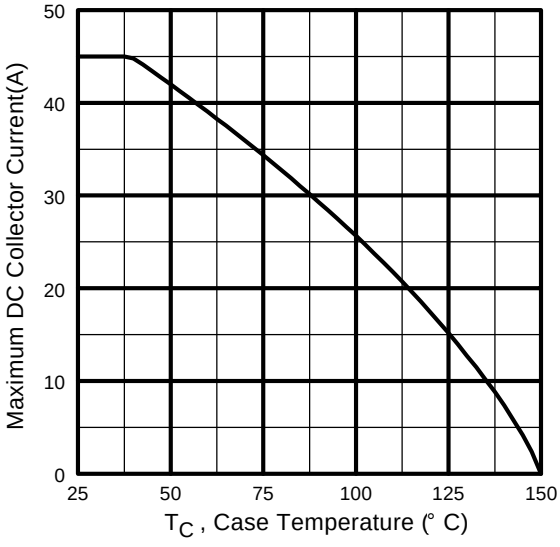


Fig. 4 - Maximum Collector Current vs. Case Temperature

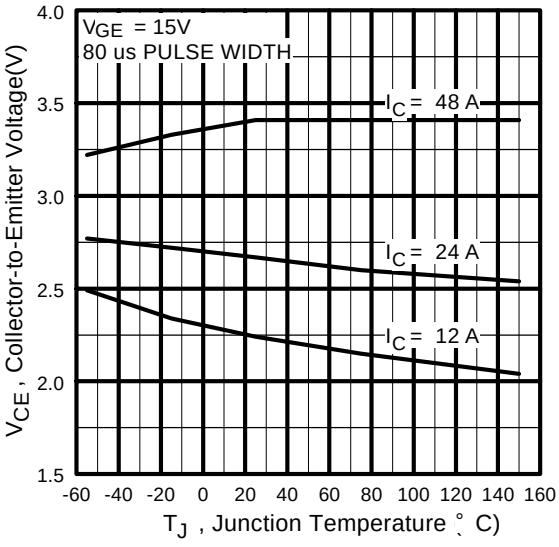


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

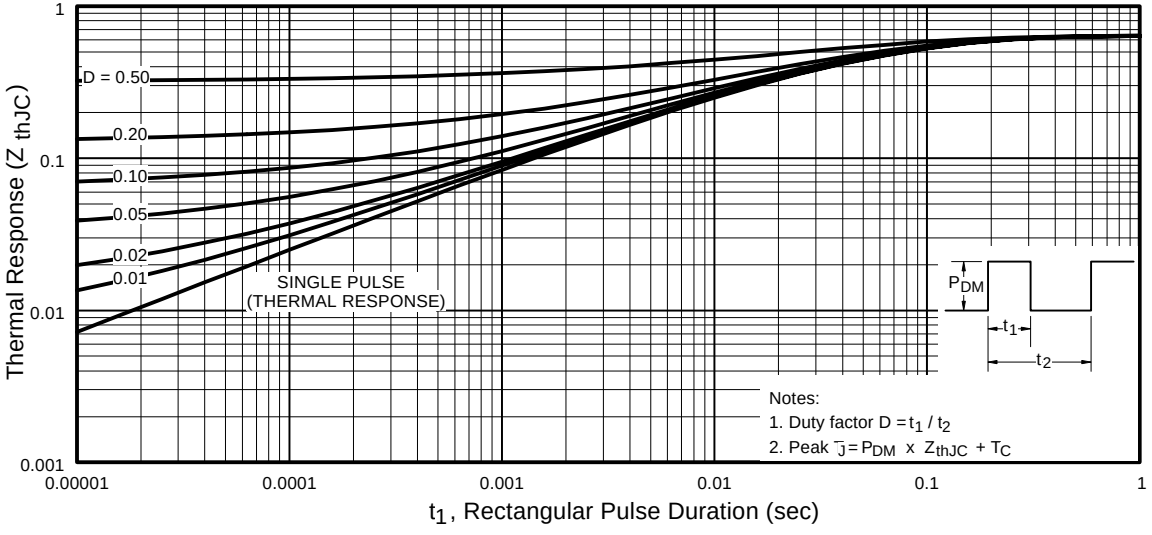


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

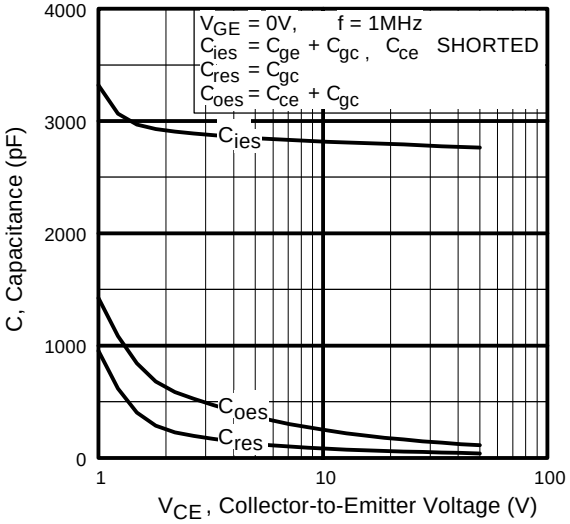


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

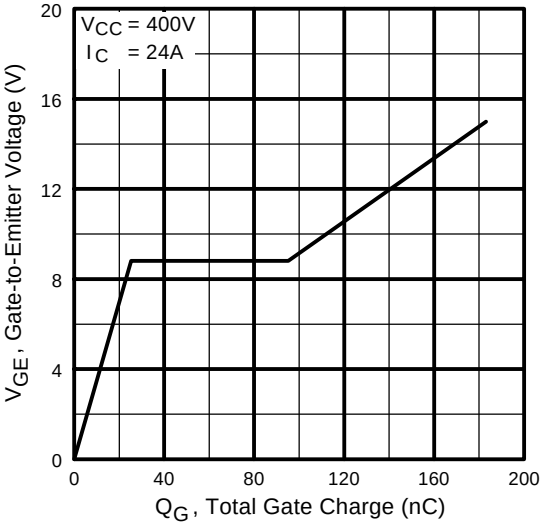


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

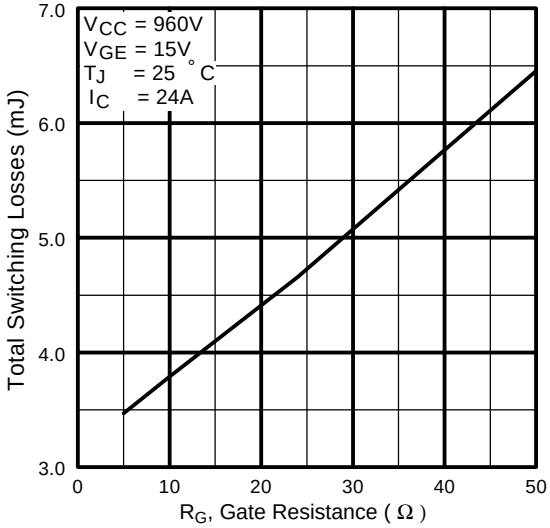


Fig. 9 - Typical Switching Losses vs. Gate Resistance

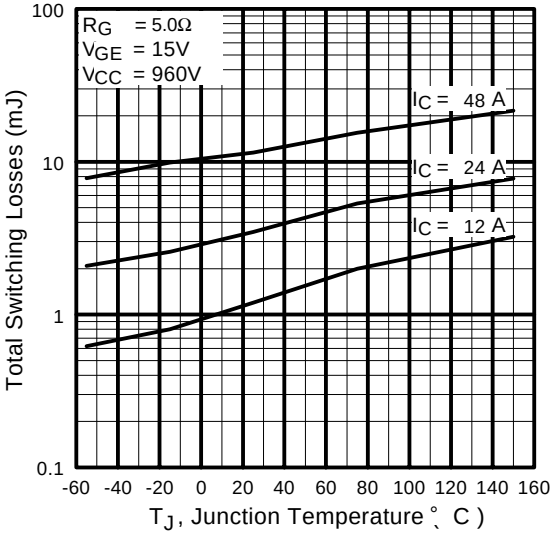


Fig. 10 - Typical Switching Losses vs. Junction Temperature

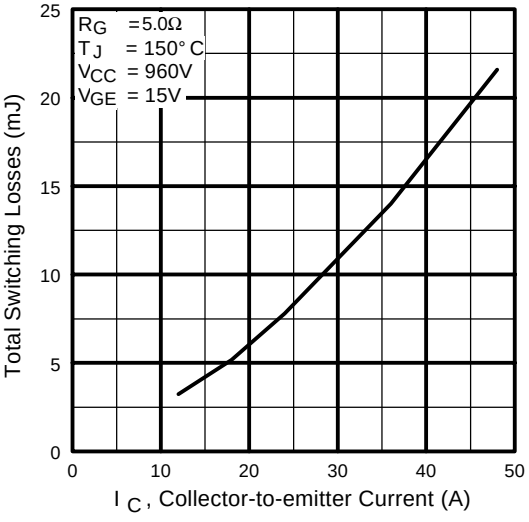


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

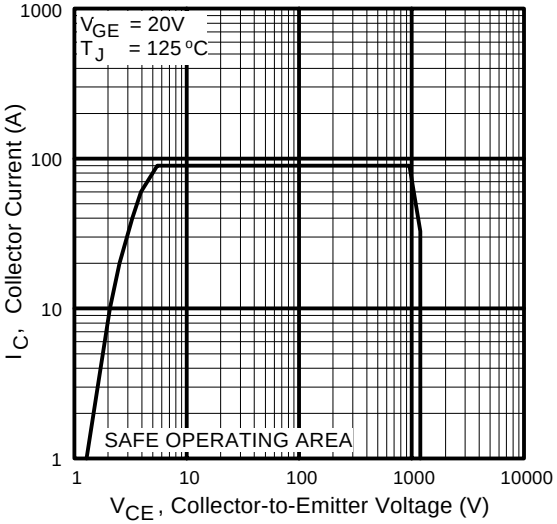


Fig. 12 - Turn-Off SOA

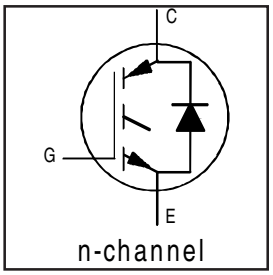
PD- 91575B

International
IOR Rectifier

IRG4PH50KD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
UltraFast IGBT



n-channel

V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.77V

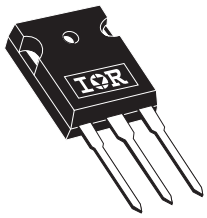
@V_{GE} = 15V, I_C = 24A

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, V_{CC} = 720V , T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Tighter parameter distribution and higher efficiency than previous generations
- IGBT co-packaged with HEXFRED™ ultrafast, ultrasoft recovery antiparallel diodes

Benefits

- Latest generation 4 IGBT's offer highest power density motor controls possible
- HEXFRED™ diodes optimized for performance with IGBTs. Minimized recovery characteristics reduce noise, EMI and switching losses
- This part replaces the IRGPH50KD2 and IRGPH50MD2 products
- For hints see design tip 97003



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	45	A
I_C @ T_C = 100°C	Continuous Collector Current	24	
I_{CM}	Pulsed Collector Current ①	90	
I_{LM}	Clamped Inductive Load Current ②	90	
I_F @ T_C = 100°C	Diode Continuous Forward Current	16	
I_{FM}	Diode Maximum Forward Current	90	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	——	——	0.64	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	——	——	0.83	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	——	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	——	40	
Wt	Weight	——	6 (0.21)	——	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.91	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.77	3.5	V	I_C = 24A V_{GE} = 15V
		—	3.28	—		I_C = 45A See Fig. 2, 5
		—	2.54	—		I_C = 24A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	13	19	—	S	V_{CE} = 100V, I_C = 24A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	6500		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	2.5	3.5	V	I_C = 16A See Fig. 13
		—	2.1	3.0		I_C = 16A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	180	270	nC	I_C = 24A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	25	38		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	70	110		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	87	—	ns	
t_r	Rise Time	—	100	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	140	300		I_C = 24A, V_{CC} = 800V
t_f	Fall Time	—	200	300		V_{GE} = 15V, R_G = 5.0Ω
E_{on}	Turn-On Switching Loss	—	3.83	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	1.90	—		and diode reverse recovery
E_{ts}	Total Switching Loss	—	5.73	7.9		See Fig. 9,10,18
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 720V, T_J = 125°C
						V_{GE} = 15V, R_G = 5.0Ω
$t_{d(on)}$	Turn-On Delay Time	—	67	—	ns	T_J = 150°C, See Fig. 10,11,18
t_r	Rise Time	—	72	—		I_C = 24A, V_{CC} = 800V
$t_{d(off)}$	Turn-Off Delay Time	—	310	—		V_{GE} = 15V, R_G = 5.0Ω,
t_f	Fall Time	—	390	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	8.36	—	mJ	and diode reverse recovery
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	2800	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	140	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	53	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	90	135	ns	T_J = 25°C See Fig.
		—	164	245		T_J = 125°C 14 I_F = 16A
I_{rr}	Diode Peak Reverse Recovery Current	—	5.8	10	A	T_J = 25°C See Fig.
		—	8.3	15		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	260	675	nC	T_J = 25°C See Fig.
		—	680	1838		T_J = 125°C 16 di/dt = 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	120	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	76	—		T_J = 125°C 17

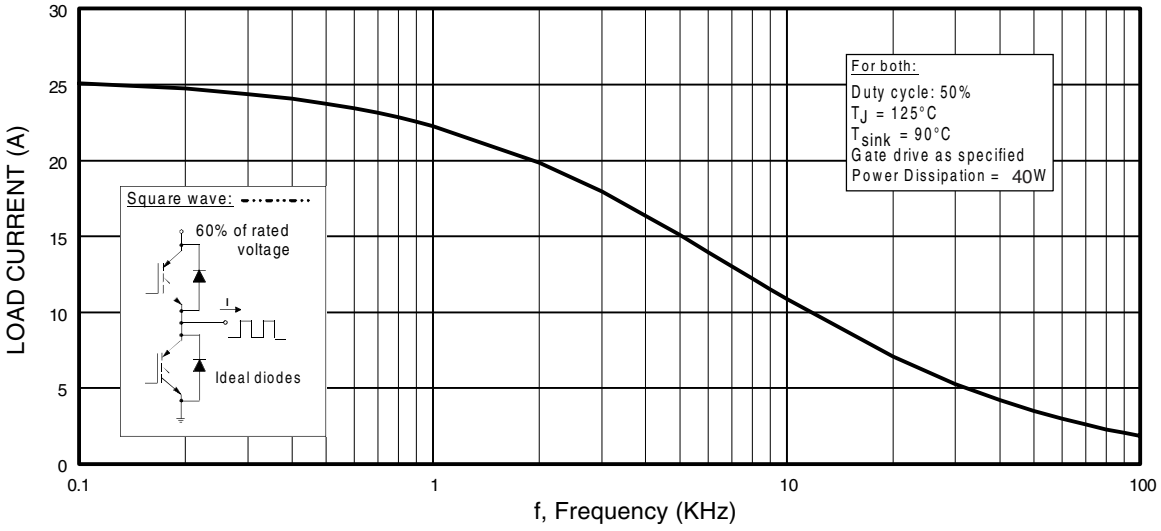


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

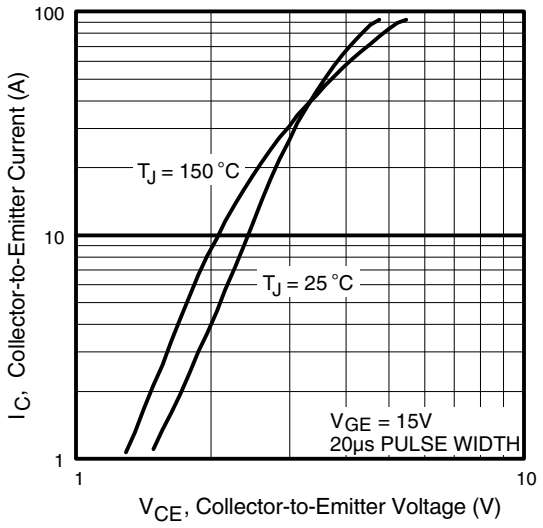


Fig. 2 - Typical Output Characteristics

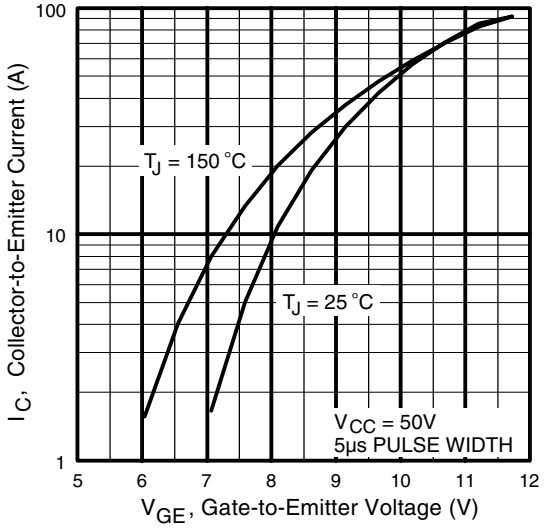


Fig. 3 - Typical Transfer Characteristics

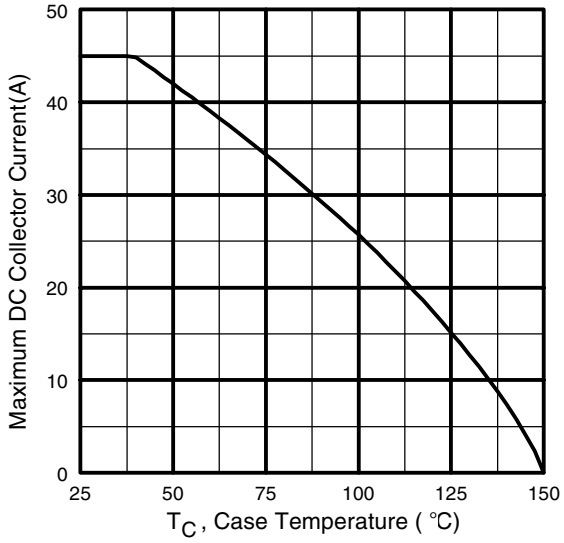


Fig. 4 - Maximum Collector Current vs. Case Temperature

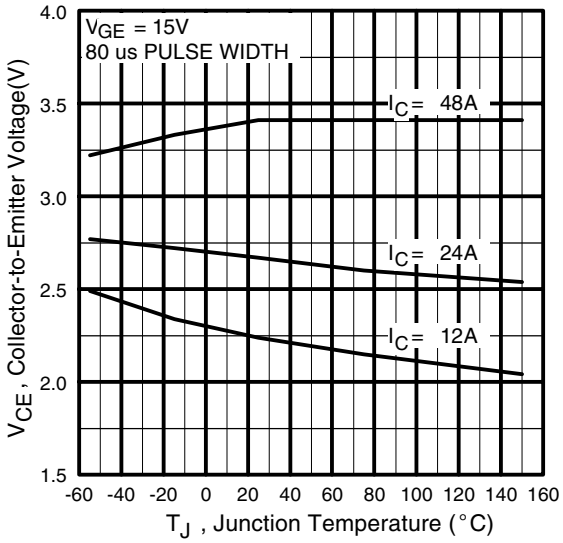


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

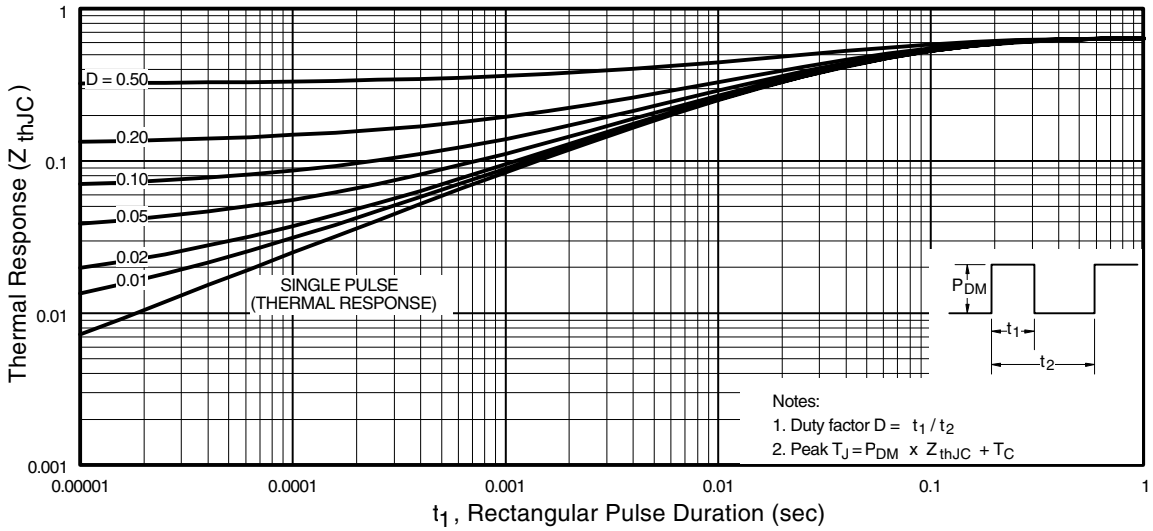


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

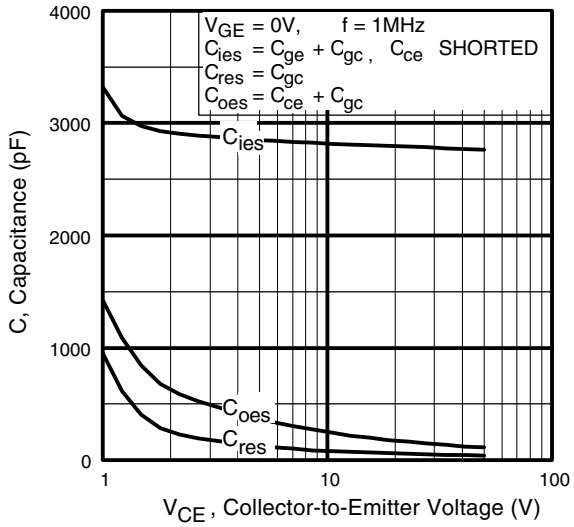


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

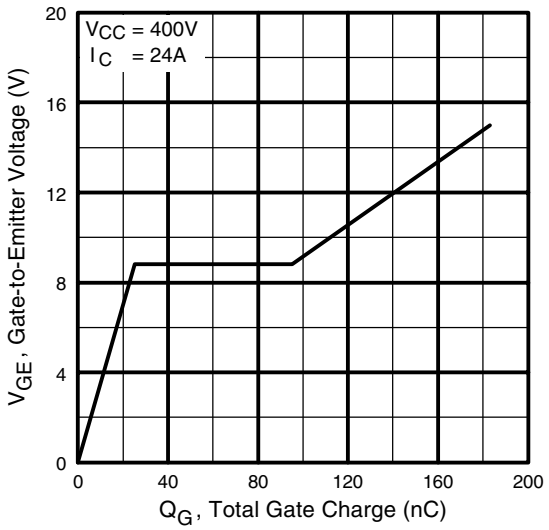


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

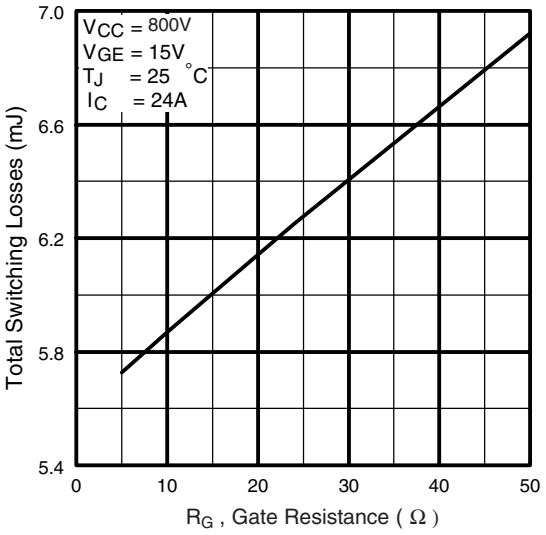


Fig. 9 - Typical Switching Losses vs. Gate Resistance

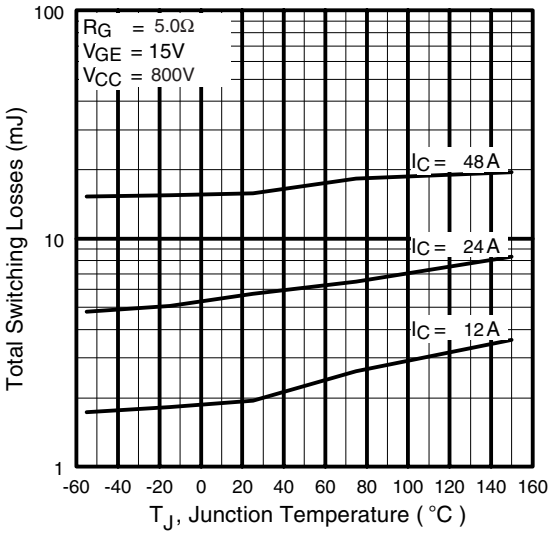


Fig. 10 - Typical Switching Losses vs. Junction Temperature

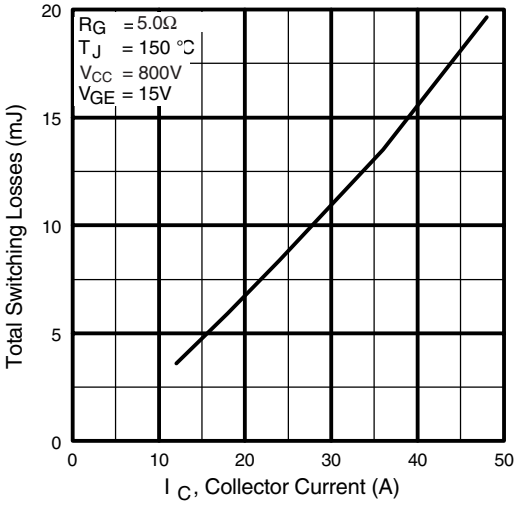


Fig. 11 - Typical Switching Losses vs. Collector Current

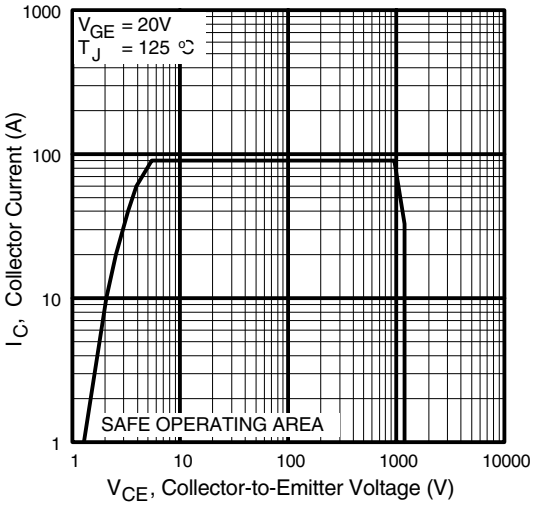


Fig. 12 - Turn-Off SOA

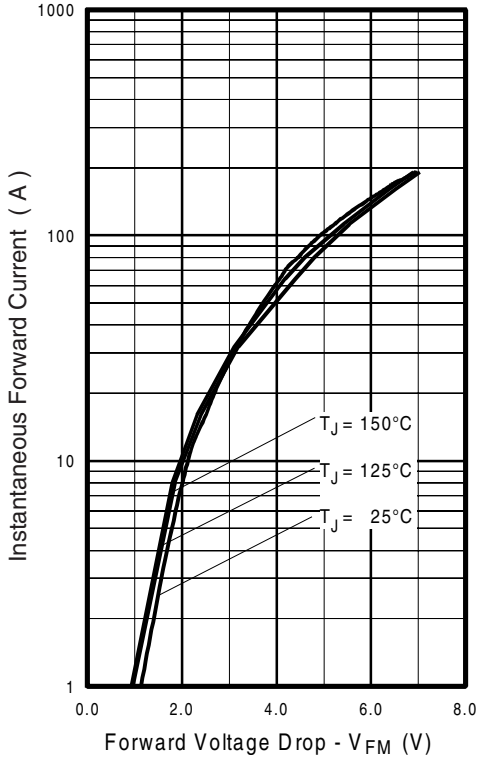


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

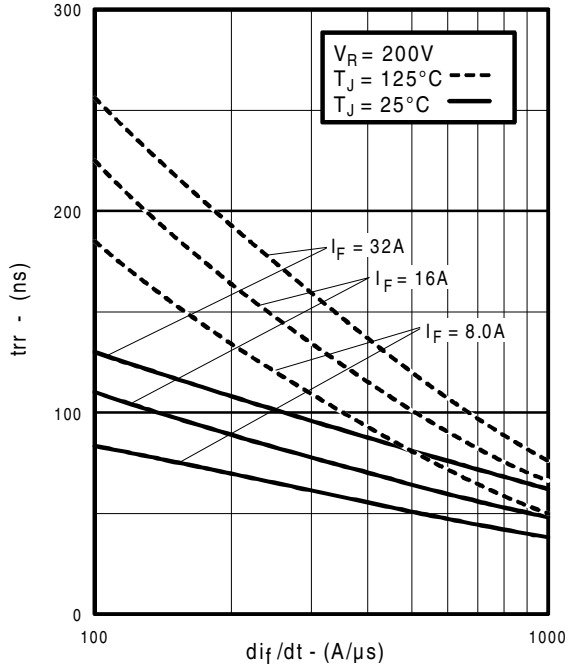


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

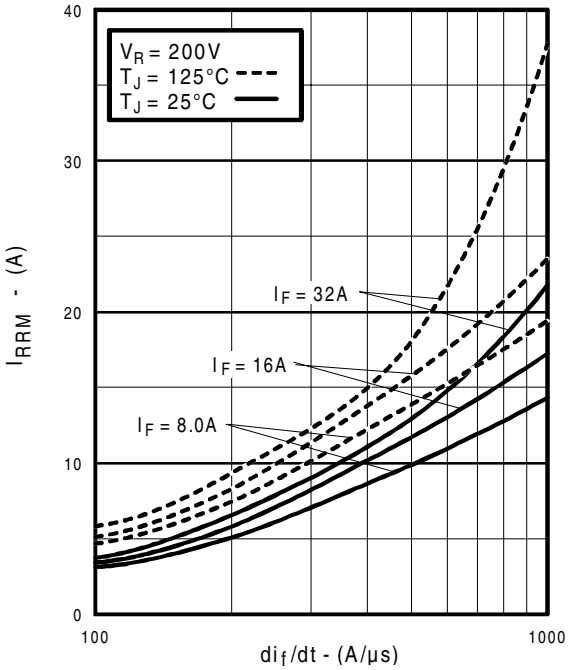


Fig. 15 - Typical Recovery Current vs. di_f/dt

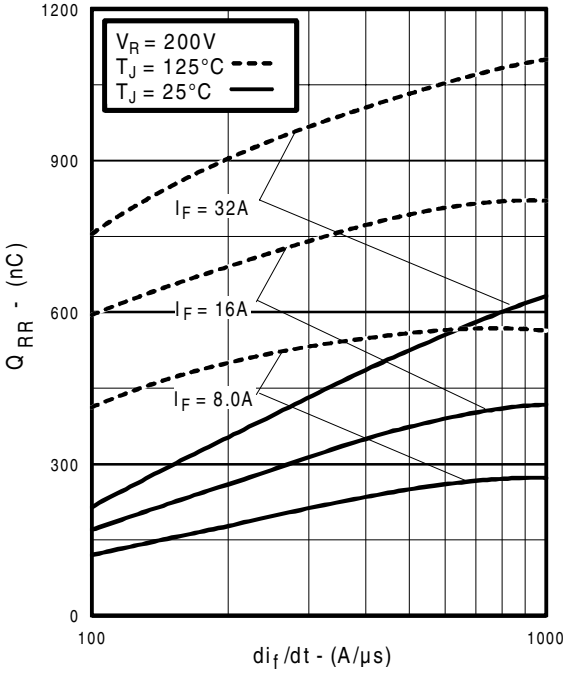


Fig. 16 - Typical Stored Charge vs. di_f/dt

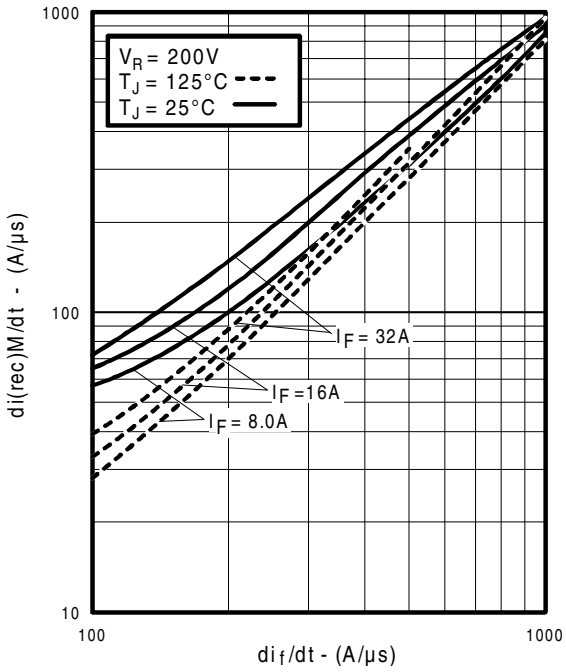


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

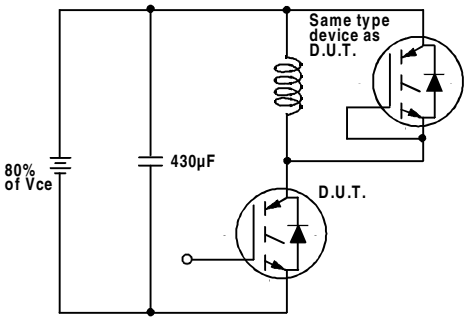


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

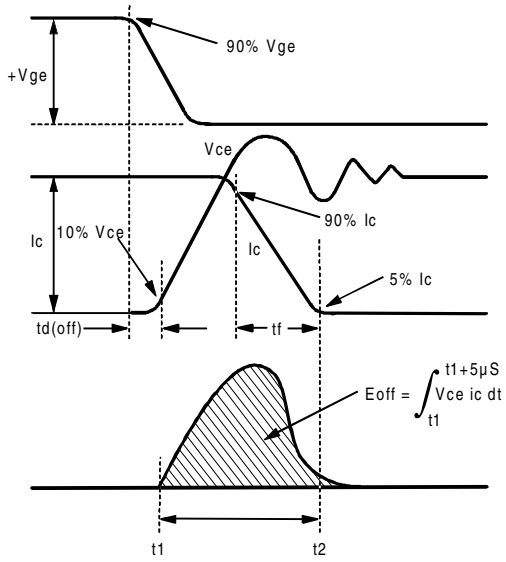


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

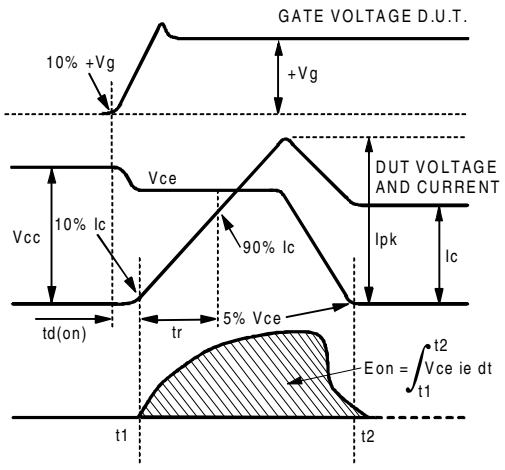


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

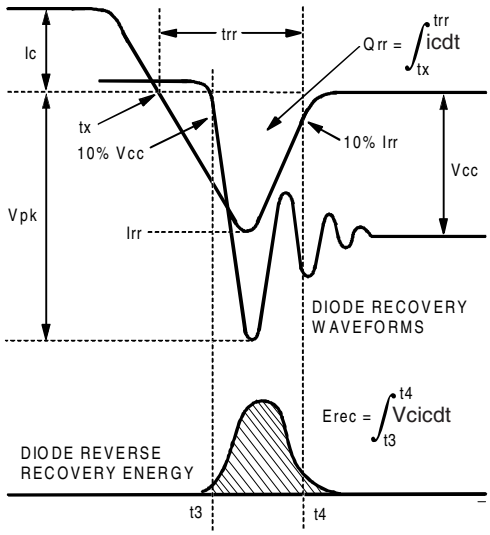


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

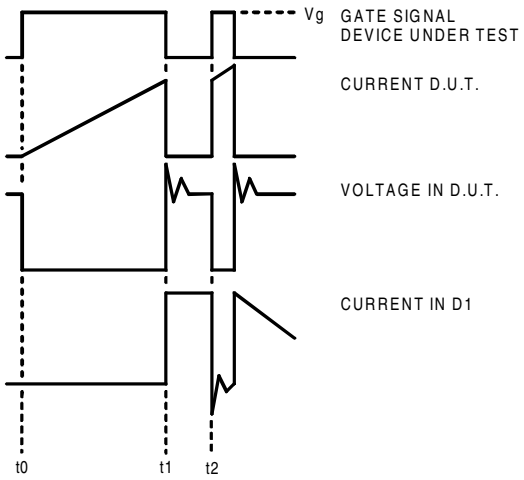


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

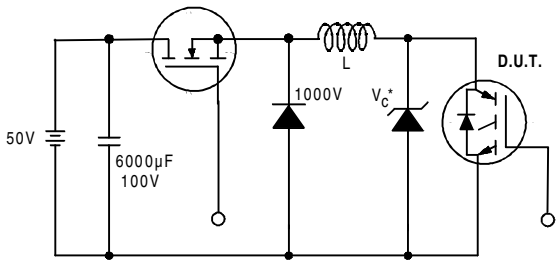


Figure 19. Clamped Inductive Load Test Circuit

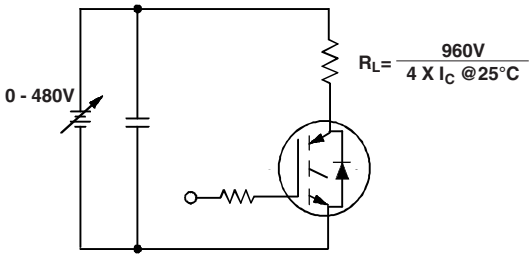


Figure 20. Pulsed Collector Current Test Circuit

Notes:

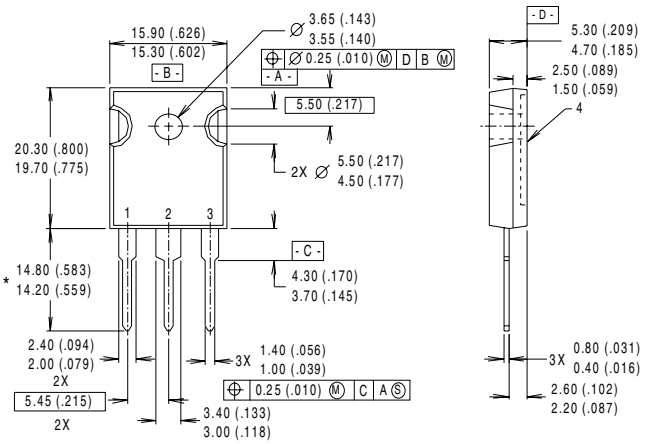
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 5.0Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 7/00

PD - 91574A

International
IOR Rectifier

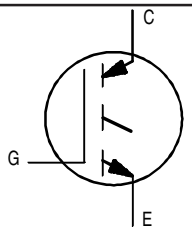
IRG4PH50U

INSULATED GATE BIPOLAR TRANSISTOR

Ultra Fast Speed IGBT

Features

- UltraFast: Optimized for high operating frequencies up to 40 kHz in hard switching, >200 kHz in resonant mode
- New IGBT design provides tighter parameter distribution and higher efficiency than previous generations
- Optimized for power conversion; SMPS, UPS and welding
- Industry standard TO-247AC package



n-channel

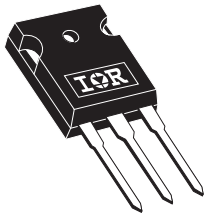
V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.78V

@V_{GE} = 15V, I_C = 24A

Benefits

- Higher switching frequency capability than competitive IGBTs
- Highest efficiency available
- Much lower conduction losses than MOSFETs
- More efficient than short circuit rated IGBTs



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	45	A
I_C @ T_C = 100°C	Continuous Collector Current	24	
I_{CM}	Pulsed Collector Current ①	180	
I_{LM}	Clamped Inductive Load Current ②	180	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	170	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.64	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

7/7/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.20	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.56	3.5	V	I_C = 20A
		—	2.78	3.7		I_C = 24A — V_{GE} = 15V
		—	3.20	—		I_C = 45A — See Fig.2, 5
		—	2.54	—		I_C = 24A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-13	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	23	35	—	S	V_{CE} = 100V, I_C = 24A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 24V, T_J = 25°C
		—	—	5000		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	160	250	nC	I_C = 24A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	27	40		V_{CC} = 400V — See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	53	83		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	35	—	ns	
t_r	Rise Time	—	15	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	200	350		I_C = 24A, V_{CC} = 960V
t_f	Fall Time	—	290	500		V_{GE} = 15V, R_G = 5.0Ω
E_{on}	Turn-On Switching Loss	—	0.53	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	1.41	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	1.94	2.6		
$t_{d(on)}$	Turn-On Delay Time	—	31	—	ns	T_J = 150°C
t_r	Rise Time	—	18	—		I_C = 24A, V_{CC} = 960V
$t_{d(off)}$	Turn-Off Delay Time	—	320	—		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	280	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	5.40	—	mJ	See Fig. 11, 14
E_{on}	Turn-On Switching Loss	—	0.35	—	mJ	T_J = 25°C, V_{GE} = 15V, R_G = 5.0Ω
E_{off}	Turn-Off Switching Loss	—	1.43	—		I_C = 20A, V_{CC} = 960V
E_{ts}	Total Switching Loss	—	1.78	2.9		Energy losses include "tail"
		—	4.56	—		See Fig. 9, 10, 11, 14, T_J = 150°C
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	3600	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	160	—		V_{CC} = 30V — See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	31	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 5.0Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

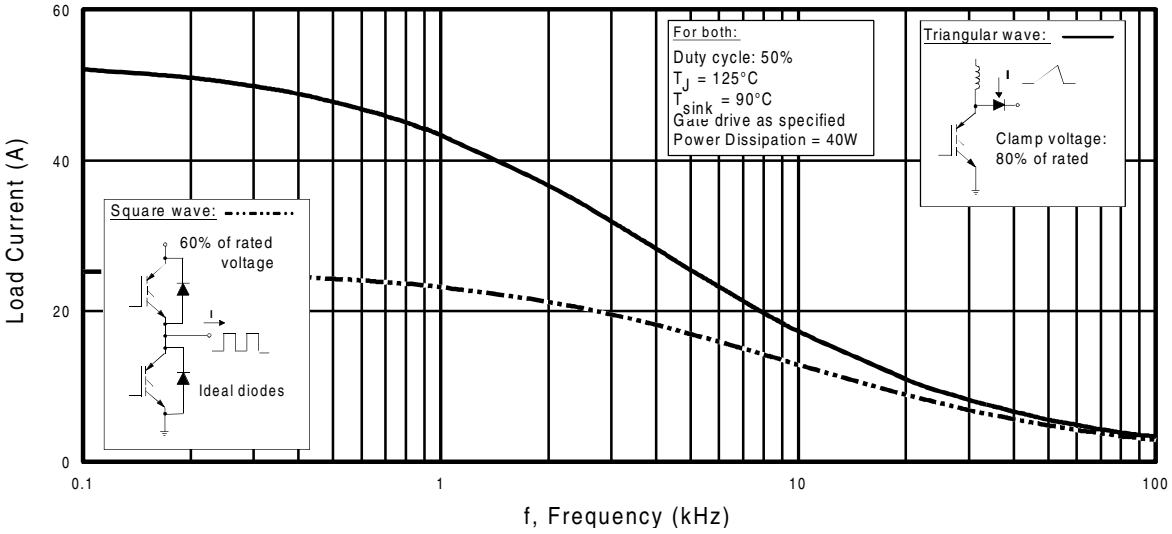


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

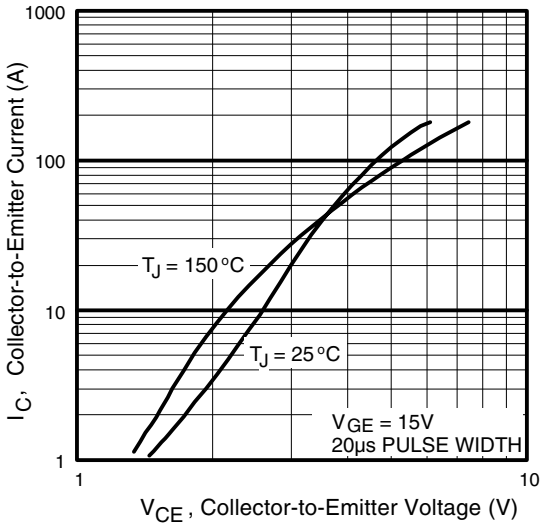


Fig. 2 - Typical Output Characteristics

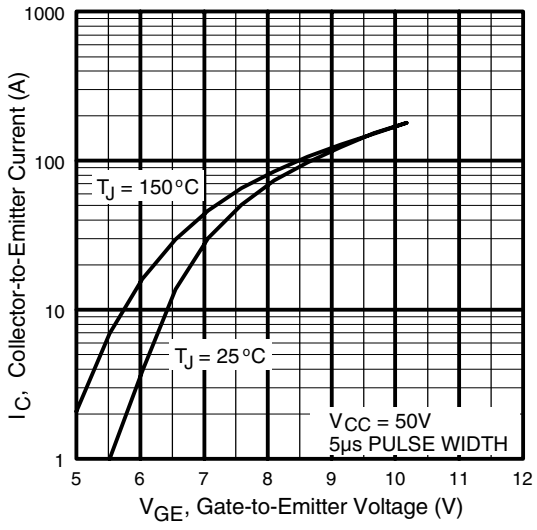


Fig. 3 - Typical Transfer Characteristics

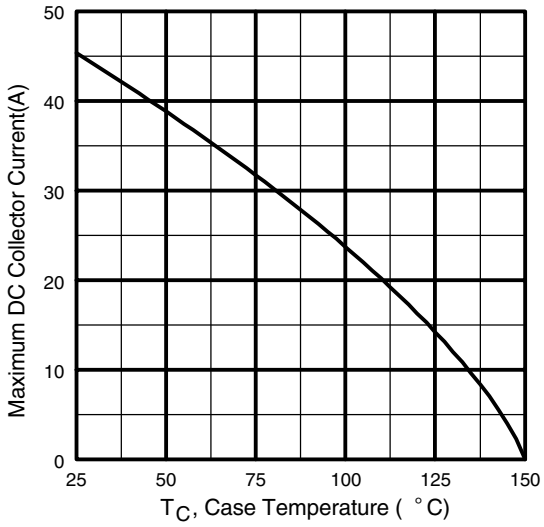


Fig. 4 - Maximum Collector Current vs. Case Temperature

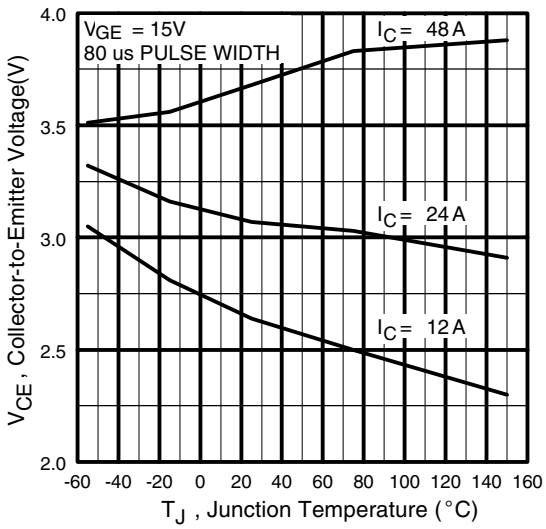


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

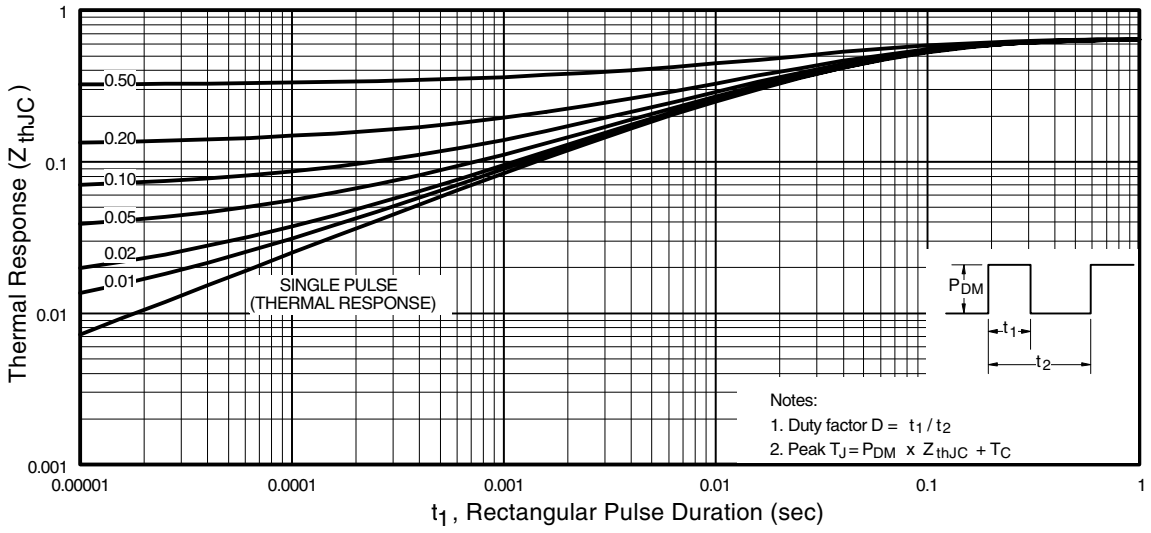


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

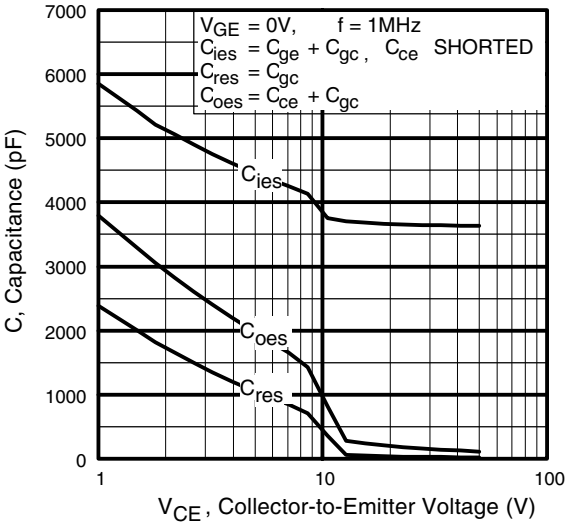


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

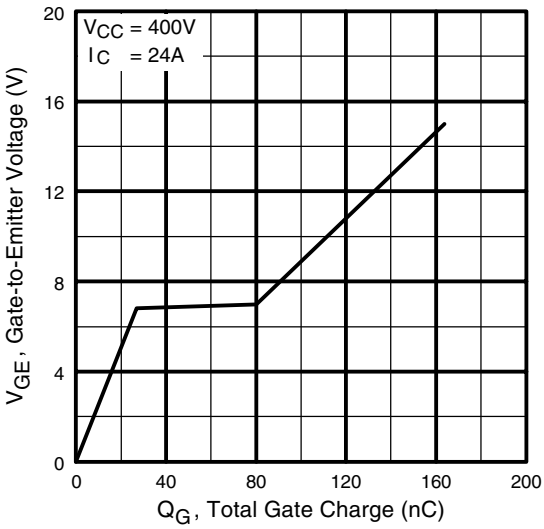


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

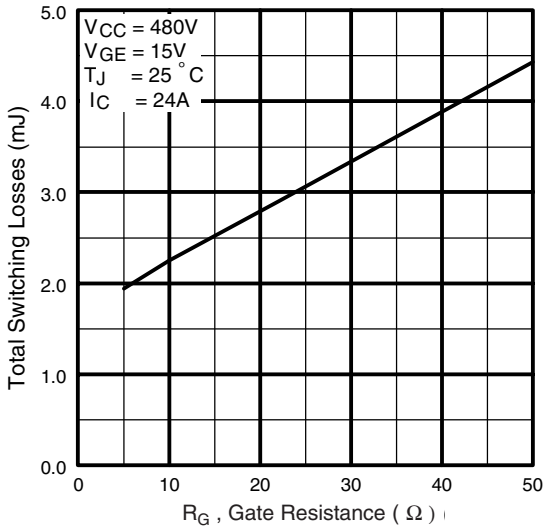


Fig. 9 - Typical Switching Losses vs. Gate Resistance

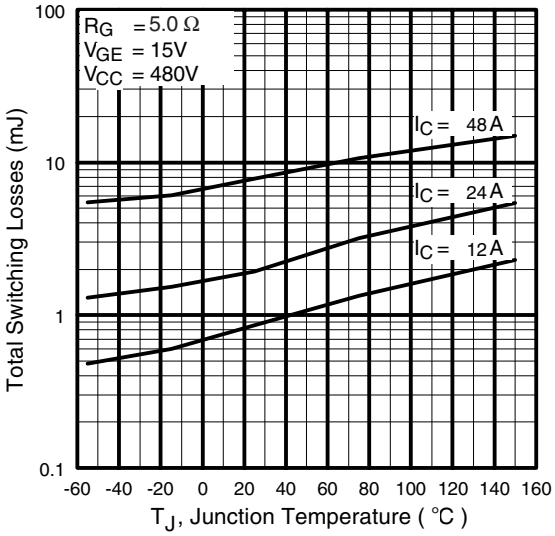


Fig. 10 - Typical Switching Losses vs. Junction Temperature

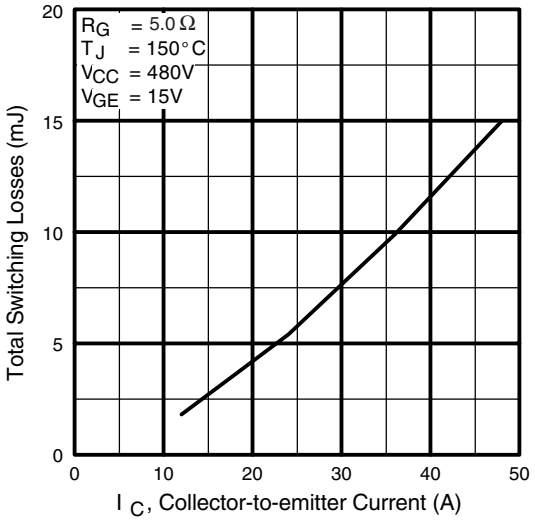


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

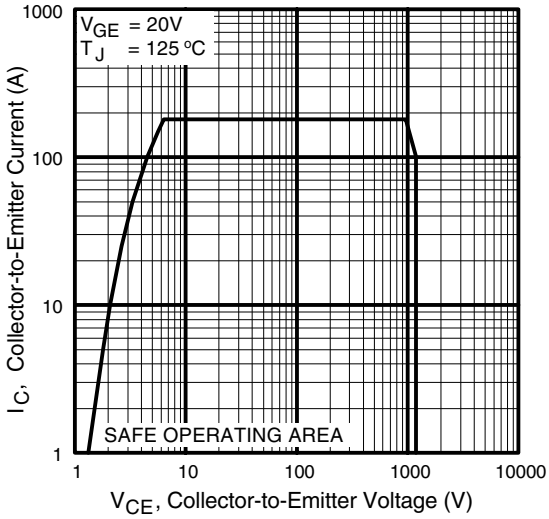


Fig. 12 - Turn-Off SOA

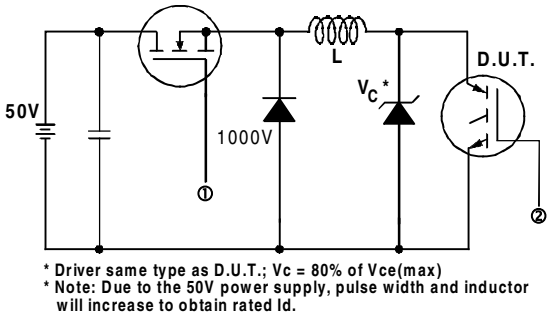


Fig. 13a - Clamped Inductive Load Test Circuit

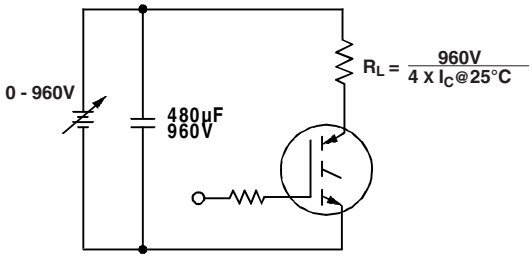


Fig. 13b - Pulsed Collector Current Test Circuit

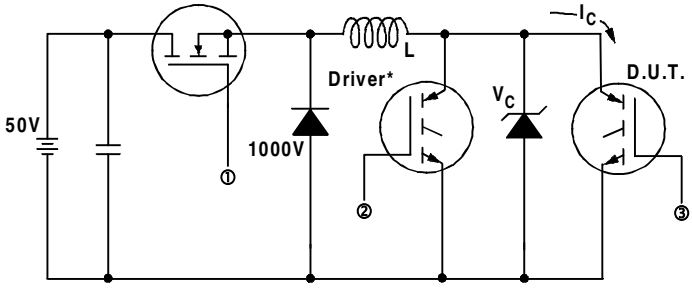


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 960V**

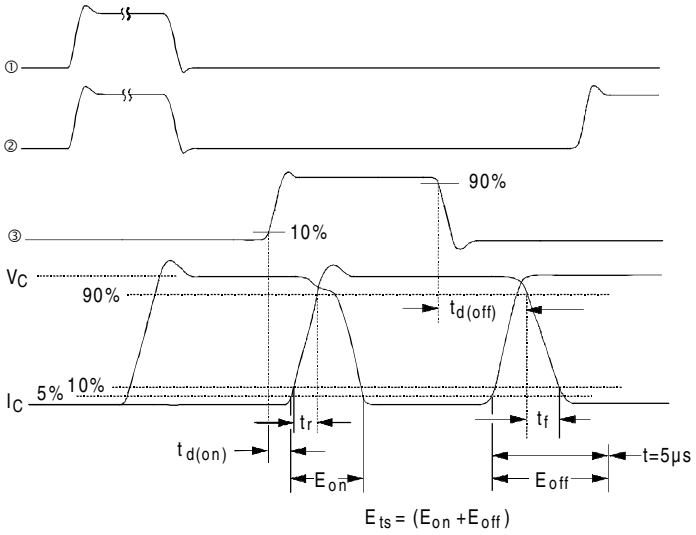
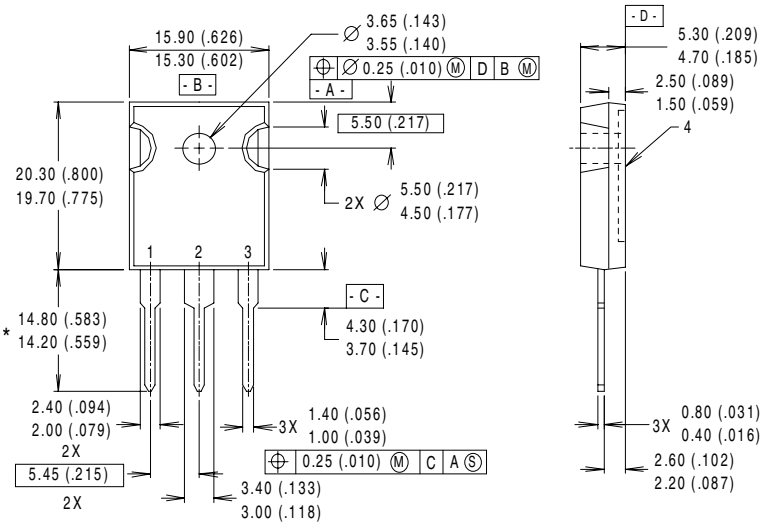


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 7/00

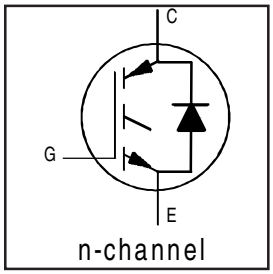
PD 91573A

International
IOR Rectifier

IRG4PH50UD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

UltraFast CoPack IGBT



V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.78V

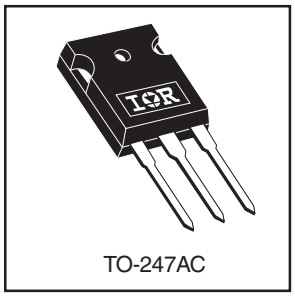
@V_{GE} = 15V, I_C = 24A

Features

- UltraFast: Optimized for high operating frequencies up to 40 kHz in hard switching, >200 kHz in resonant mode
- New IGBT design provides tighter parameter distribution and higher efficiency than previous generations
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-247AC package

Benefits

- Higher switching frequency capability than competitive IGBTs
- Highest efficiency available
- HEXFRED diodes optimized for performance with IGBT's . Minimized recovery characteristics require less/no snubbing



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	45	A
I_C @ T_C = 100°C	Continuous Collector Current	24	
I_{CM}	Pulsed Collector Current ①	180	
I_{LM}	Clamped Inductive Load Current ②	180	
I_F @ T_C = 100°C	Diode Continuous Forward Current	16	
I_{FM}	Diode Maximum Forward Current	180	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	——	——	0.64	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	——	——	0.83	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	——	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	——	40	
Wt	Weight	——	6 (0.21)	——	g (oz)

7/7/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.20	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.56	3.5	V	I_C = 20A V_{GE} = 15V
		—	2.78	3.7		I_C = 24A
		—	3.20	—		I_C = 45A See Fig. 2, 5
		—	2.54	—		I_C = 24A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-13	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	23	35	—	S	V_{CE} = 100V, I_C = 24A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	6500		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	2.5	3.5	V	I_C = 16A See Fig. 13
		—	2.1	3.0		I_C = 16A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	160	250	nC	I_C = 24A
Qge	Gate - Emitter Charge (turn-on)	—	27	40		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	53	80		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	47	—	ns	T_J = 25°C
t_r	Rise Time	—	24	—		I_C = 24A, V_{CC} = 800V
$t_{d(off)}$	Turn-Off Delay Time	—	110	170		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	180	260		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	2.10	—	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	1.50	—		See Fig. 9, 10, 18
E_{ts}	Total Switching Loss	—	3.60	4.6		
$t_{d(on)}$	Turn-On Delay Time	—	46	—	ns	T_J = 150°C, See Fig. 11, 18
t_r	Rise Time	—	27	—		I_C = 24A, V_{CC} = 800V
$t_{d(off)}$	Turn-Off Delay Time	—	240	—		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	330	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	6.38	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	3600	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	160	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	31	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	90	135	ns	T_J = 25°C See Fig.
		—	164	245		T_J = 125°C 14 I_F = 16A
I_{rr}	Diode Peak Reverse Recovery Current	—	5.8	10	A	T_J = 25°C See Fig.
		—	8.3	15		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	260	675	nC	T_J = 25°C See Fig.
		—	680	1838		T_J = 125°C 16 di/dt = 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	120	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	76	—		T_J = 125°C 17

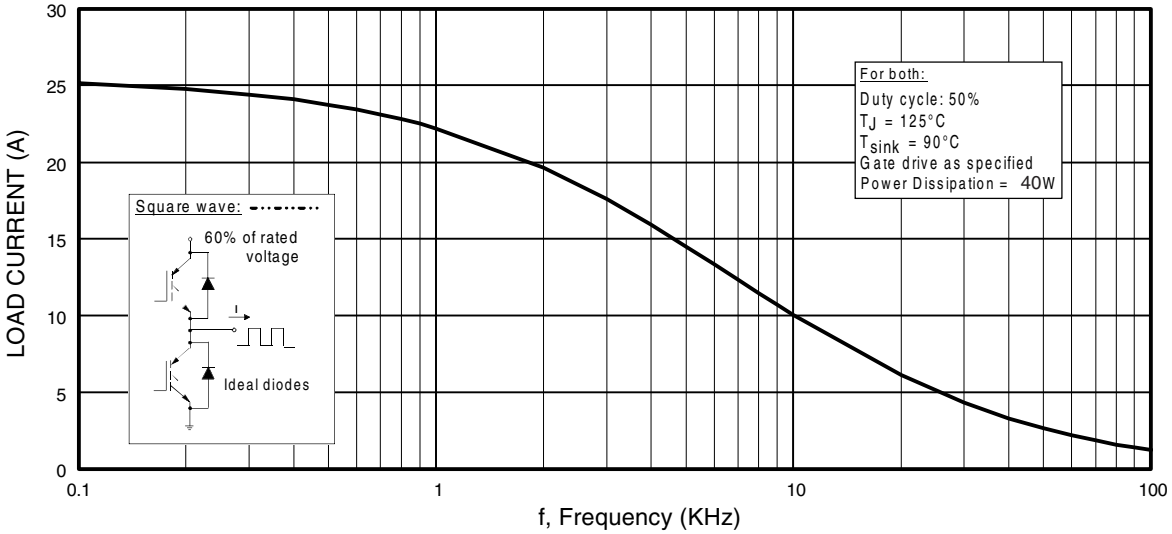


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

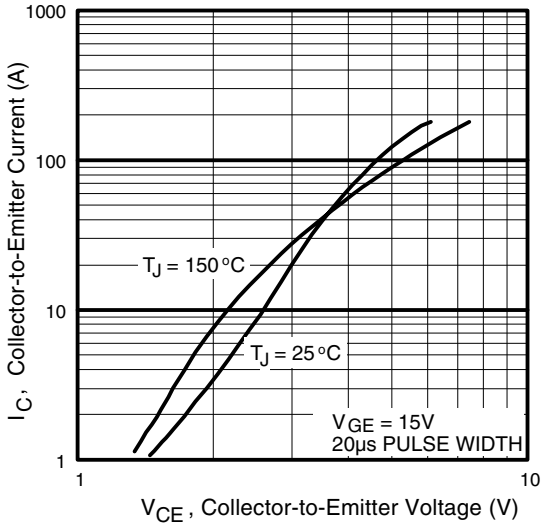


Fig. 2 - Typical Output Characteristics

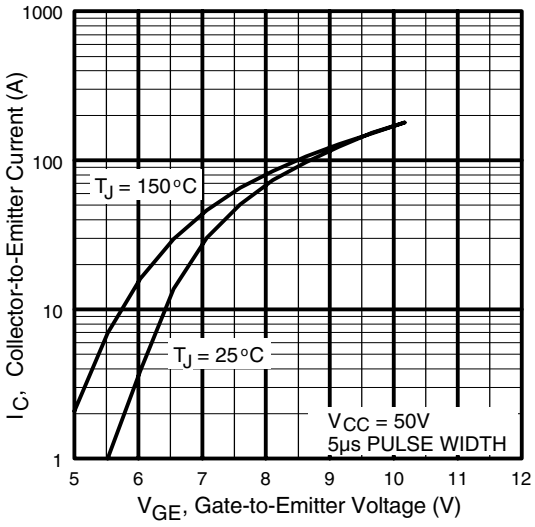


Fig. 3 - Typical Transfer Characteristics

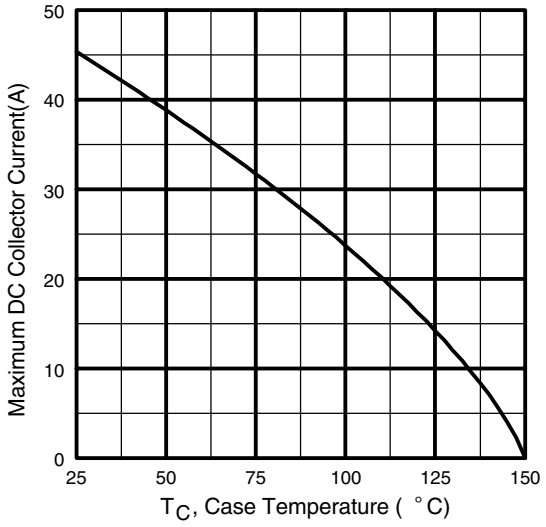


Fig. 4 - Maximum Collector Current vs. Case Temperature

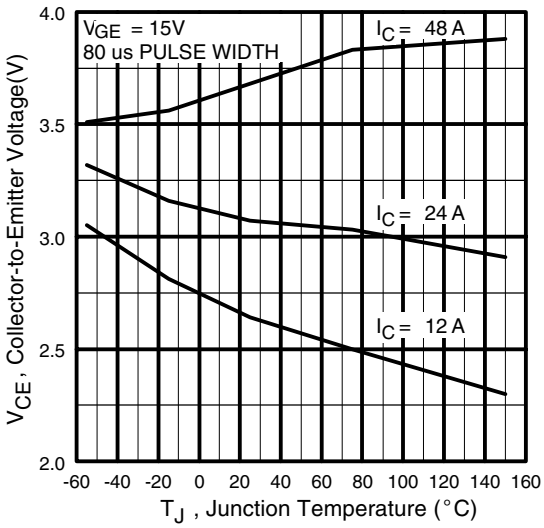


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

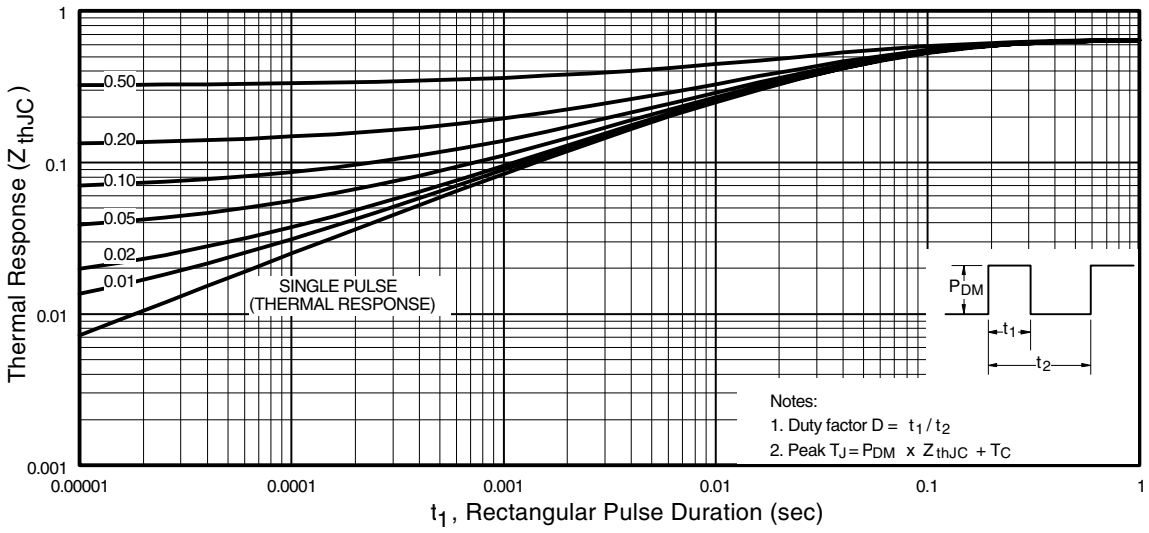


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

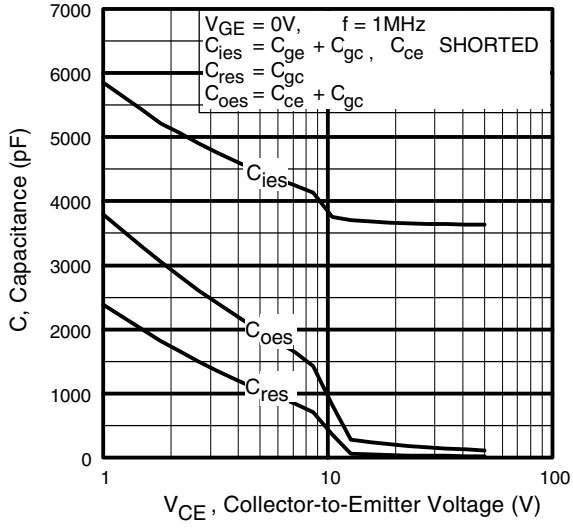


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

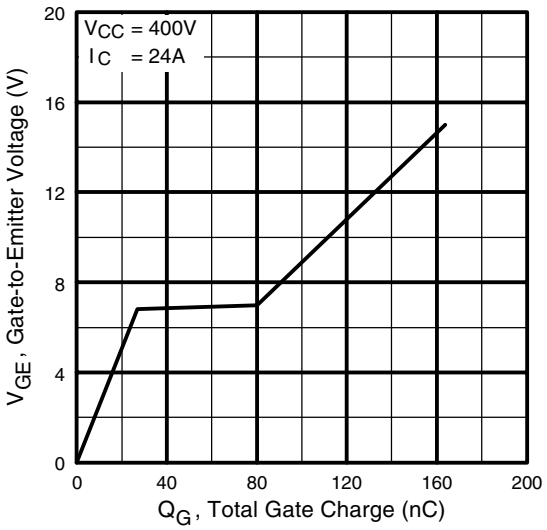


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

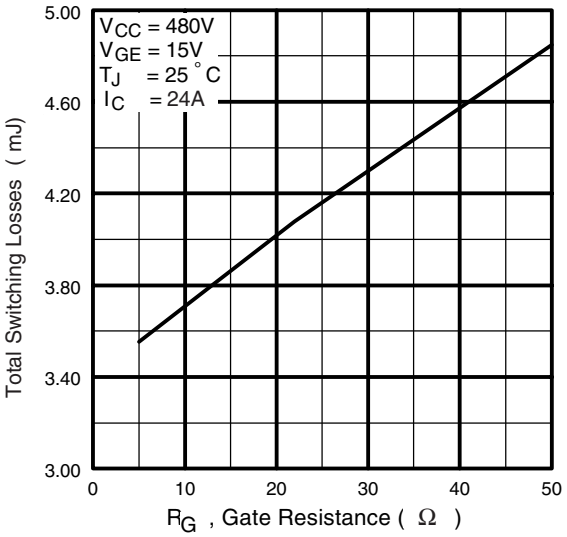


Fig. 9 - Typical Switching Losses vs. Gate Resistance

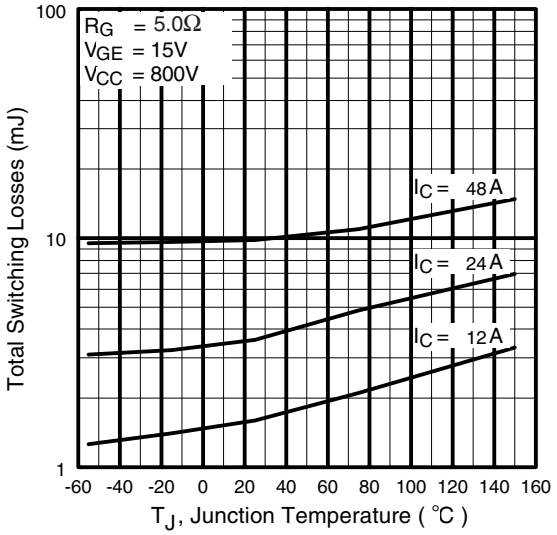


Fig. 10 - Typical Switching Losses vs. Junction Temperature

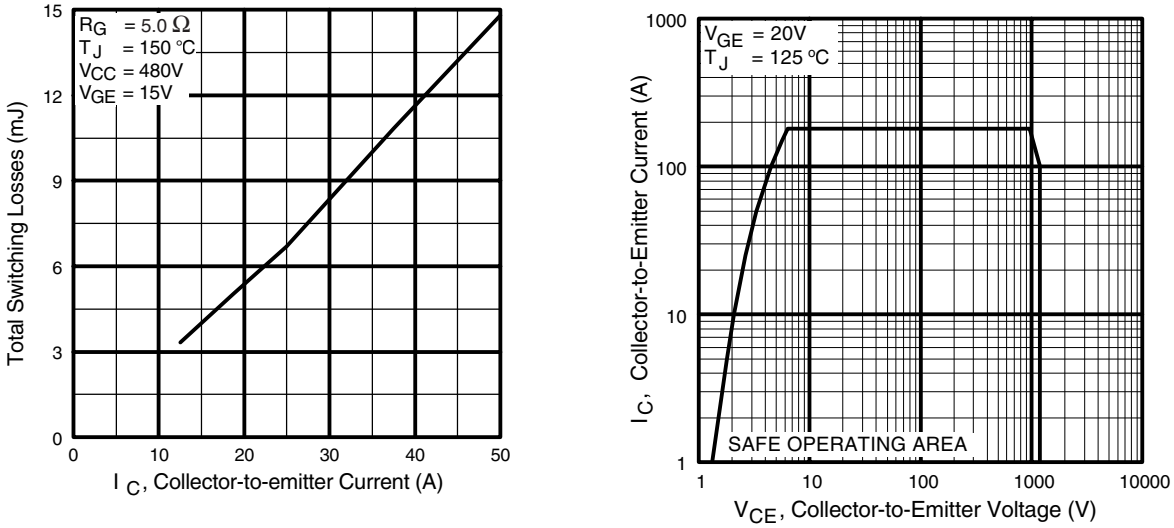


Fig. 11 - Typical Switching Losses vs.
Collector-to-Emitter Current

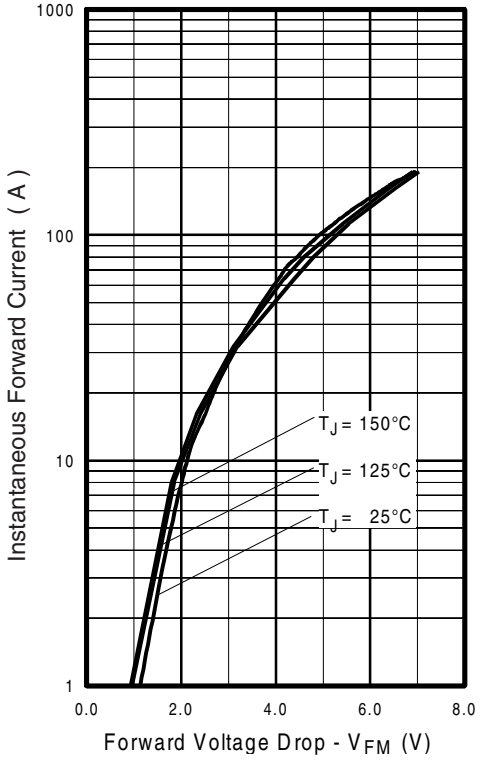


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

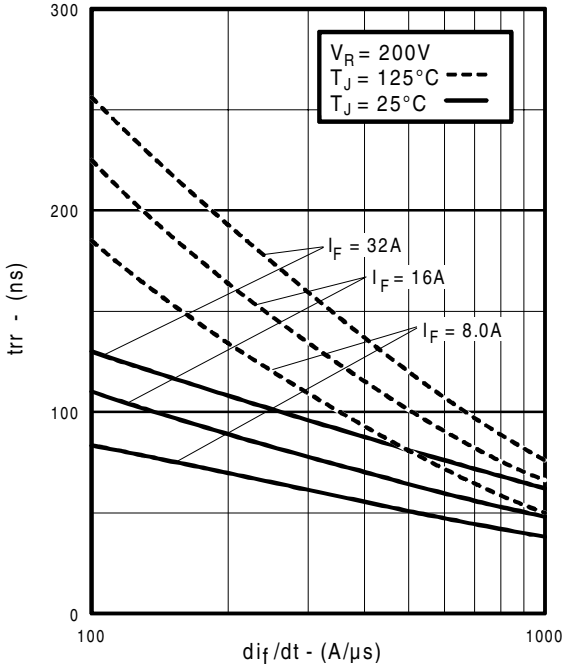


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

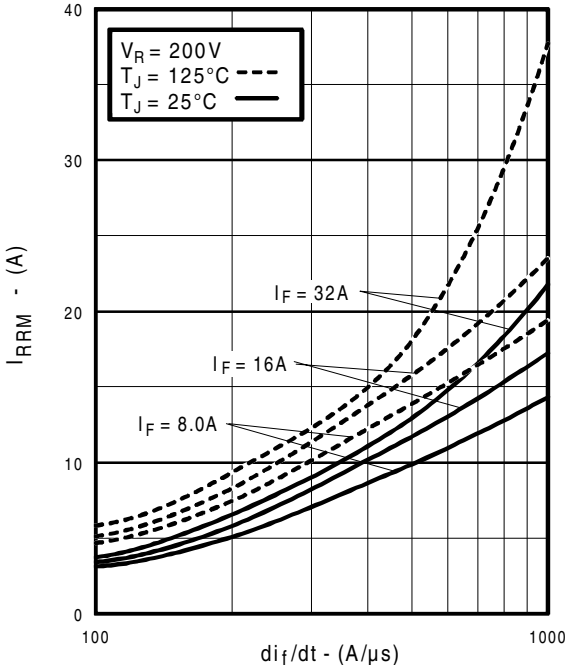


Fig. 15 - Typical Recovery Current vs. di_f/dt

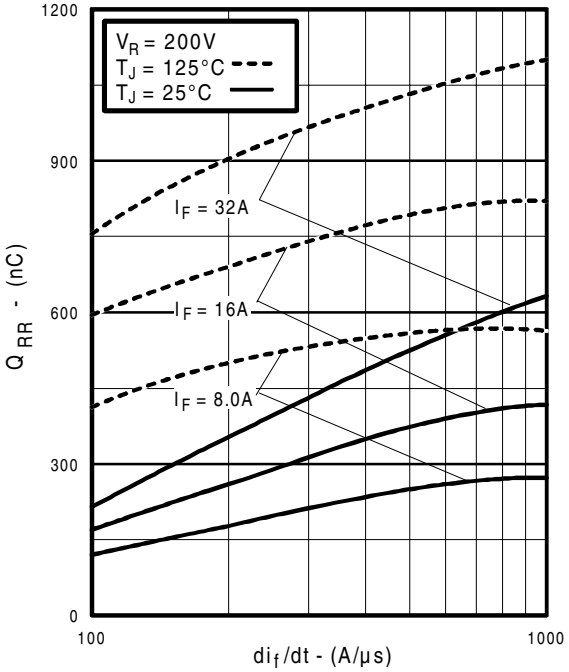


Fig. 16 - Typical Stored Charge vs. di_f/dt

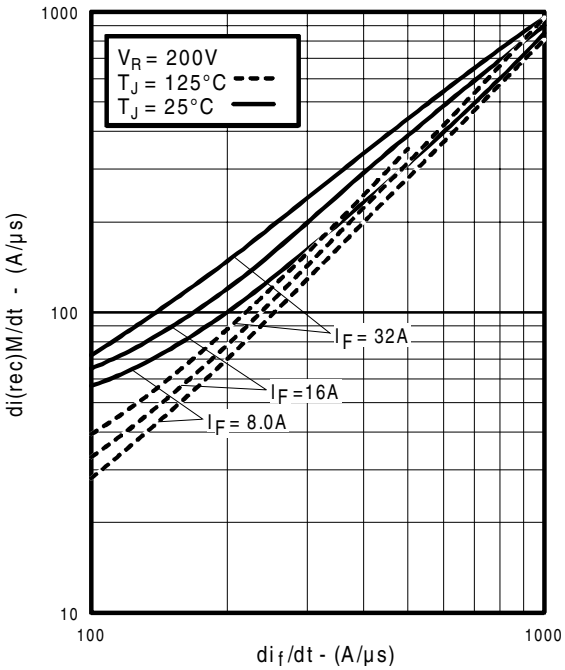


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

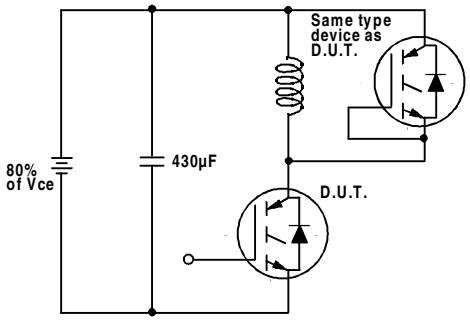


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

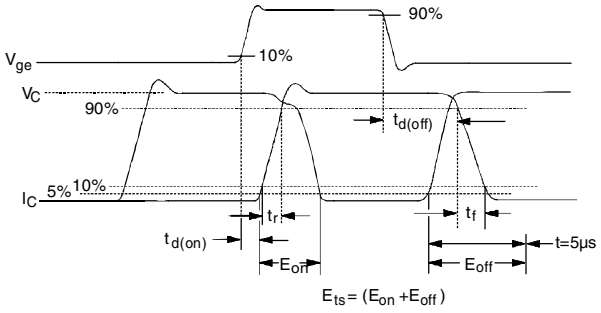


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

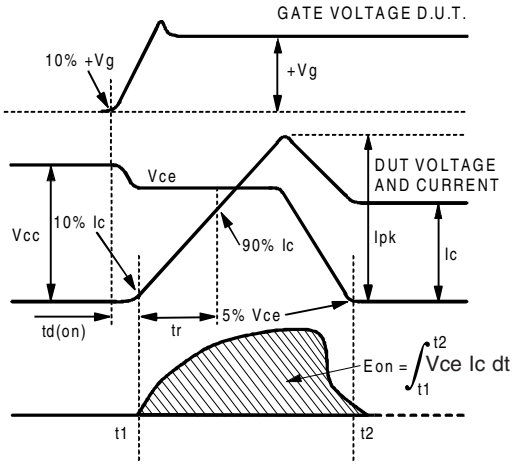


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

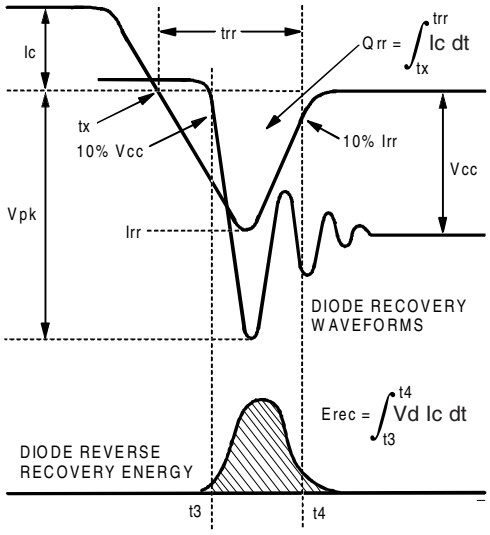


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

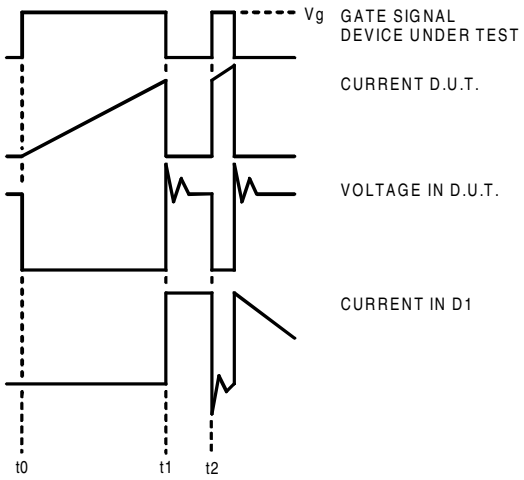


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

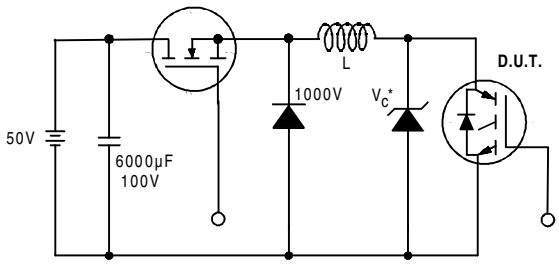


Figure 19. Clamped Inductive Load Test Circuit

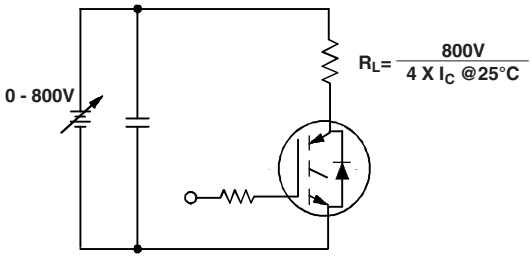


Figure 20. Pulsed Collector Current Test Circuit

Notes:

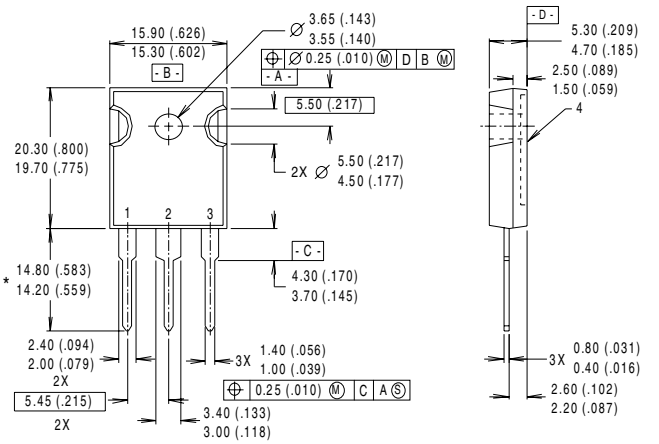
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 5.0Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 7/00

PD -91712A

International
IOR Rectifier

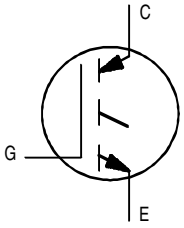
IRG4PH50S

INSULATED GATE BIPOLAR TRANSISTOR

Standard Speed IGBT

Features

- Standard: Optimized for minimum saturation voltage and low operating frequencies (< 1kHz)
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-247AC package



n-channel

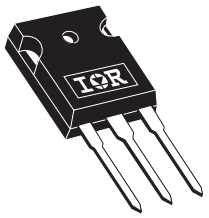
V_{CES} =1200V

$V_{CE(on)\ typ.}$ = 1.47V

@V_{GE} = 15V, I_C = 33A

Benefits

- Generation 4 IGBT's offer highest efficiency available
- IGBT's optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	57	A
I_C @ T_C = 100°C	Continuous Collector Current	33	
I_{CM}	Pulsed Collector Current①	114	
I_{LM}	Clamped Inductive Load Current ②	114	
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy③	270	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	80	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.64	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6.0 (0.21)	—	g (oz)

7/7/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0 A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.22	—	V/°C	V_{GE} = 0V, I_C = 2.0 mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.47	1.7	V	I_C = 33A V_{GE} = 15V
		—	1.75	—		I_C = 57A See Fig.2, 5
		—	1.55	—		I_C = 33A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$DV_{GE(th)}/DT_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	27	40	—	S	V_{CE} = 100V, I_C = 33A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	167	251	nC	I_C = 33A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	25	38		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	55	83		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	32	—	ns	
t_r	Rise Time	—	29	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	845	1268		I_C = 33A, V_{CC} = 960V
t_f	Fall Time	—	425	638		V_{GE} = 15V, R_G = 5.0Ω
E_{on}	Turn-On Switching Loss	—	1.80	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	19.6	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	21.4	44		
$t_{d(on)}$	Turn-On Delay Time	—	32	—	ns	T_J = 150°C,
t_r	Rise Time	—	30	—		I_C = 33A, V_{CC} = 960V
$t_{d(off)}$	Turn-Off Delay Time	—	1170	—		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	1000	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	37	—	mJ	See Fig. 10,11,14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	3600	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	160	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	30	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 5.0Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

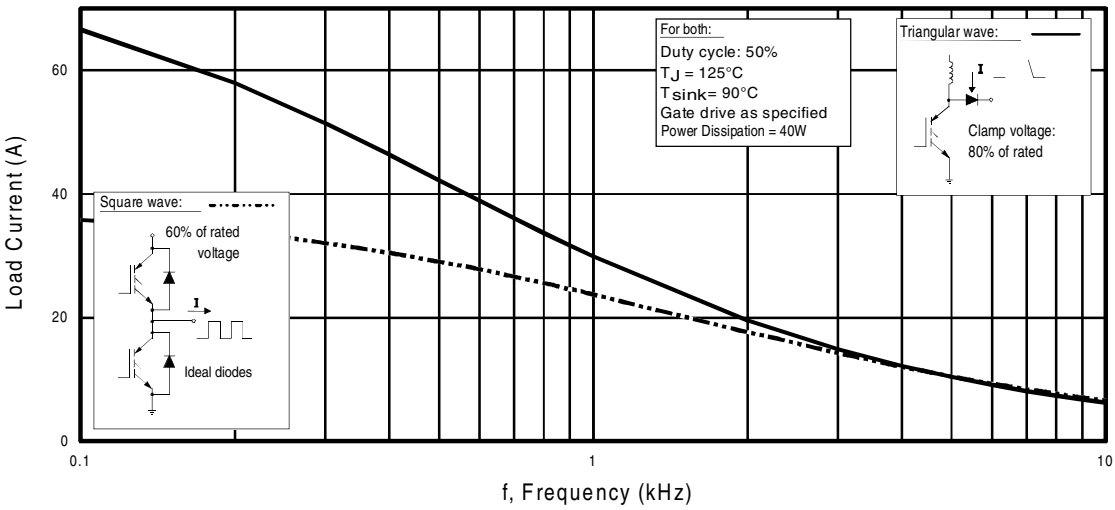


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

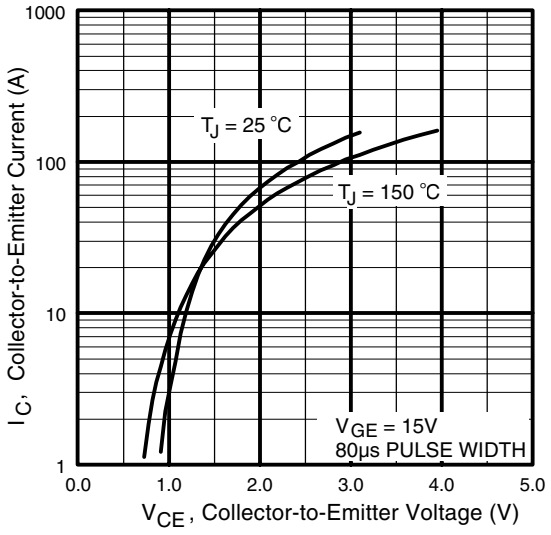


Fig. 2 - Typical Output Characteristics

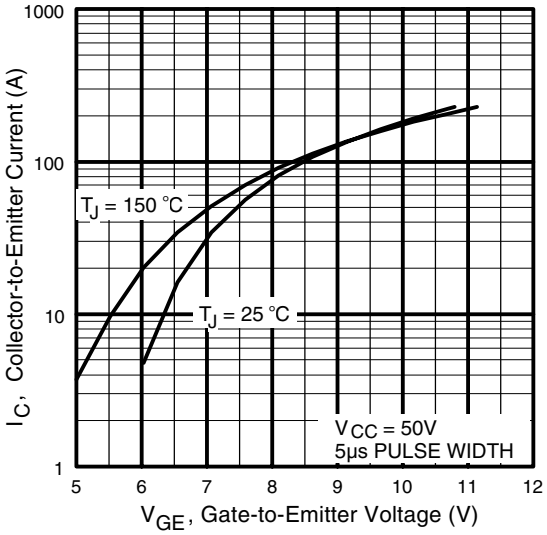


Fig. 3 - Typical Transfer Characteristics

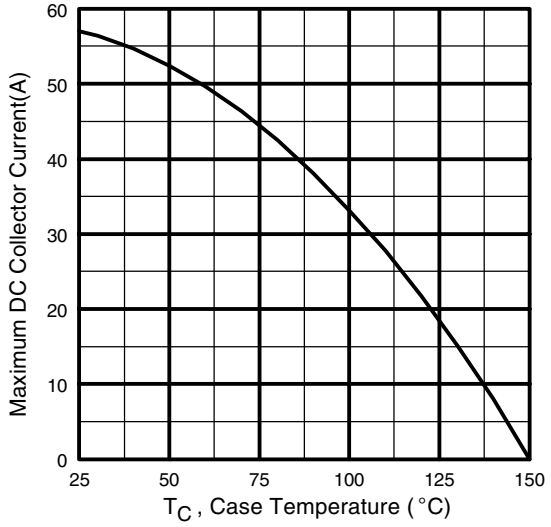


Fig. 4 - Maximum Collector Current vs. Case Temperature

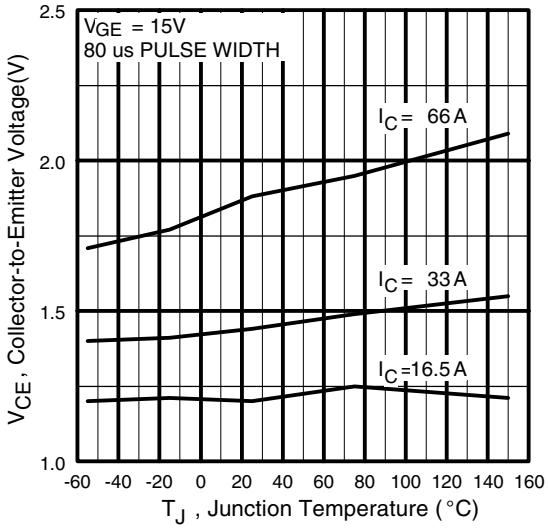


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

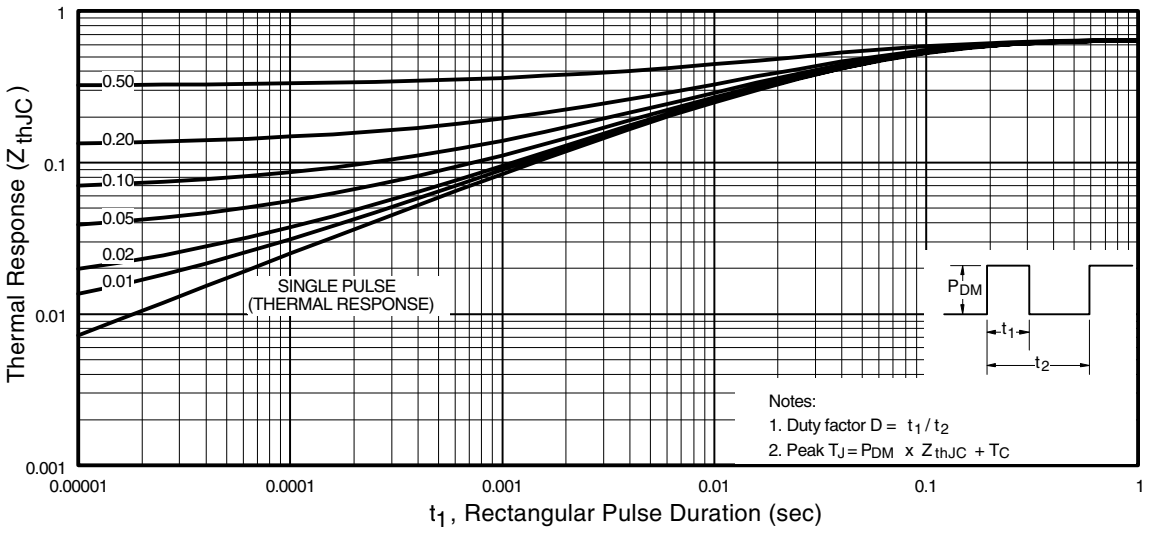


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

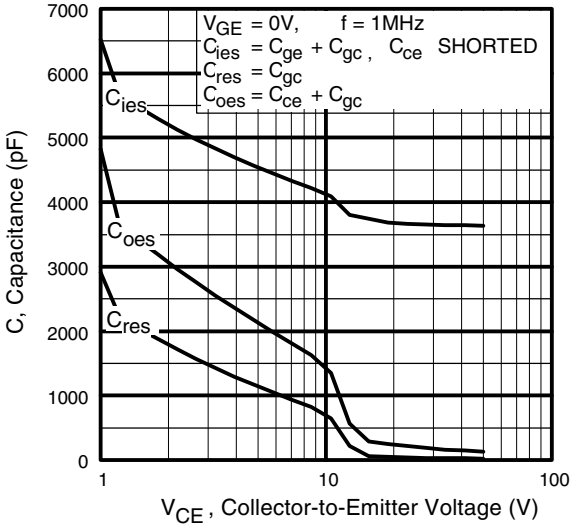


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

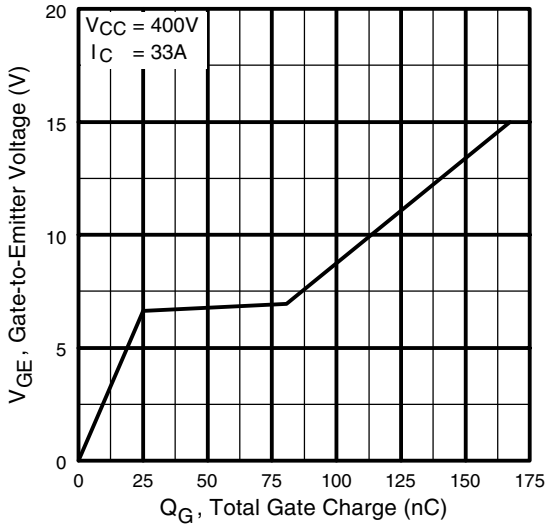


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

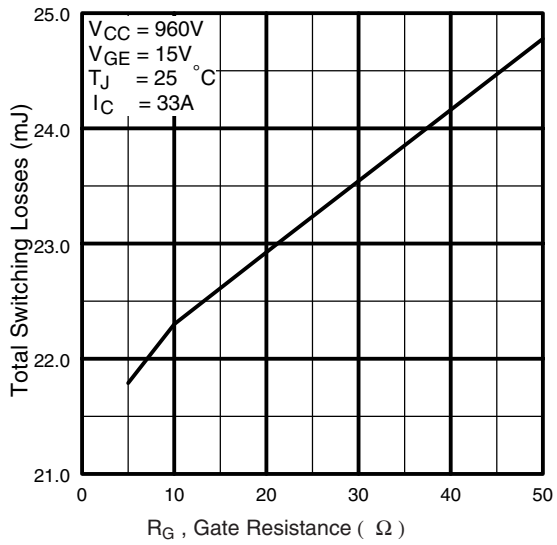


Fig. 9 - Typical Switching Losses vs. Gate Resistance

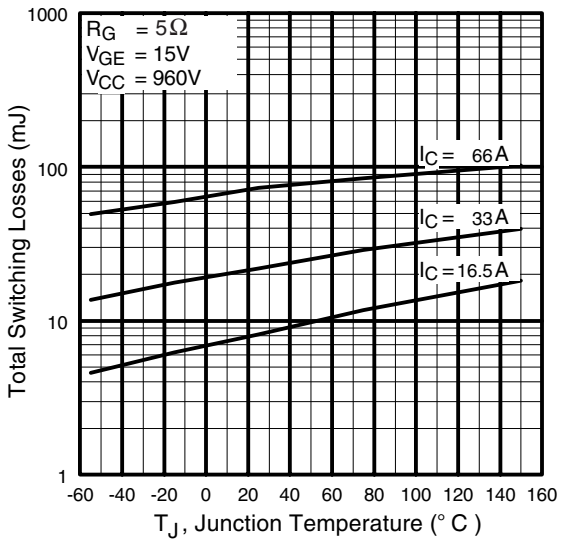


Fig. 10 - Typical Switching Losses vs. Junction Temperature

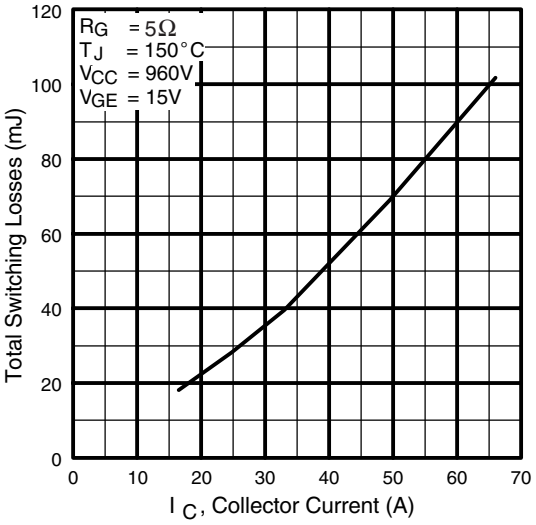


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

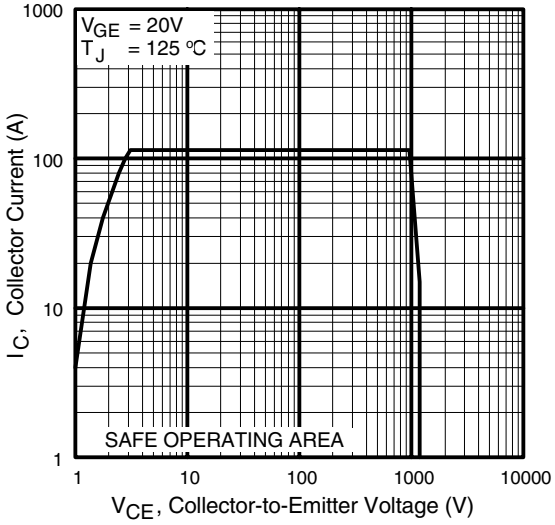


Fig. 12 - Reverse Bias SOA

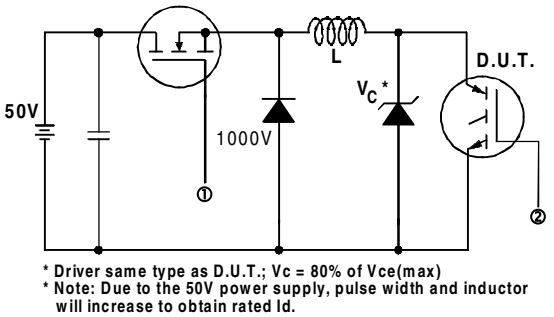


Fig. 13a - Clamped Inductive Load Test Circuit

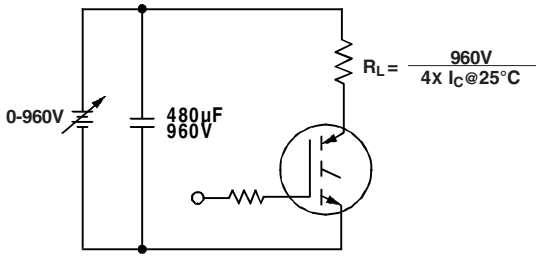


Fig. 13b - Pulsed Collector Current Test Circuit

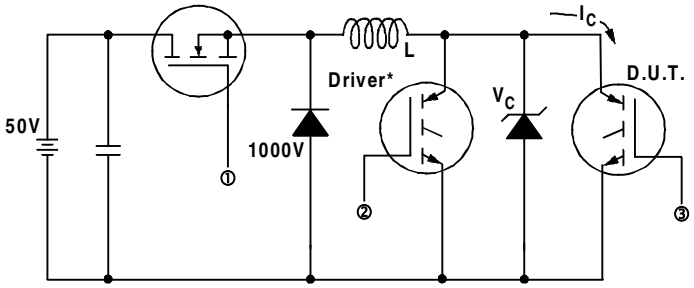


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = ----V**

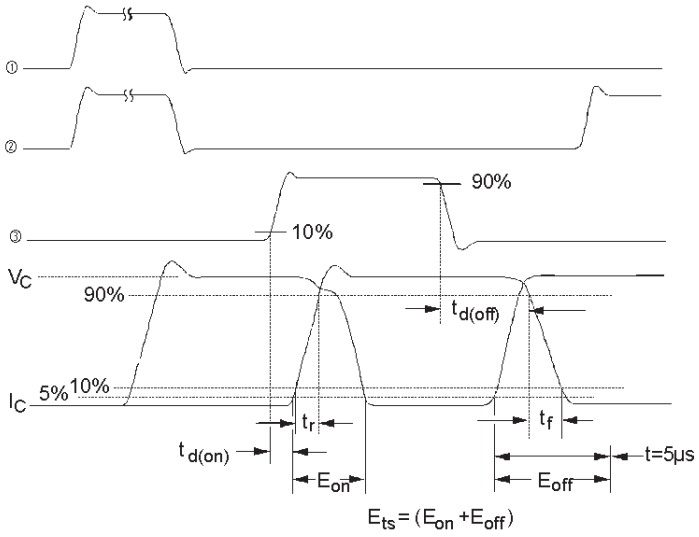
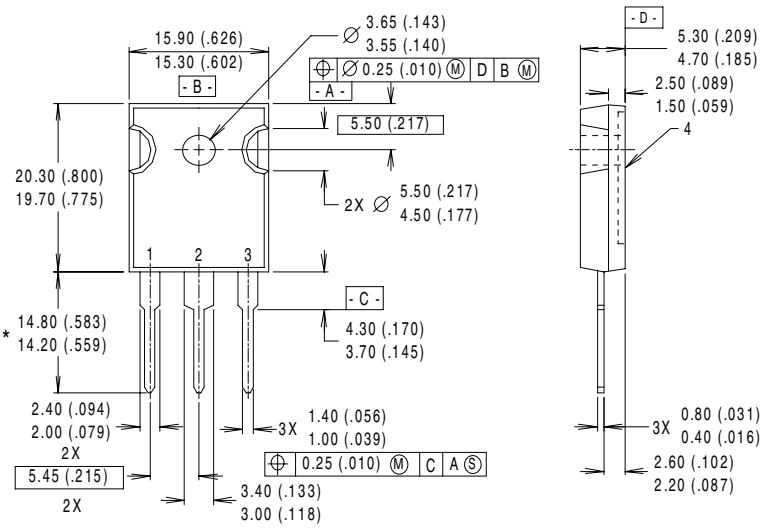


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 7/00

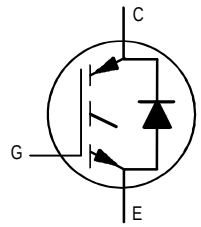
PD- 93818

International
IOR Rectifier

IRGP30B120KD-E

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Motor Control Co-Pack IGBT



N-channel

V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.28V

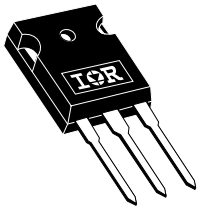
V_{GE} = 15V, I_C = 25A, 25°C

Features

- Low V_{CE}(on) Non Punch Through (NPT) Technology
- Low Diode V_F (1.76V Typical @ 25A & 25°C)
- 10 µs Short Circuit Capability
- Square RBSOA
- Ultrasoft Diode Recovery Characteristics
- Positive V_{CE}(on) Temperature Coefficient
- Extended Lead TO-247AD Package

Benefits

- Benchmark Efficiency for Motor Control Applications
- Rugged Transient Performance
- Low EMI
- Significantly Less Snubber Required
- Excellent Current Sharing in Parallel Operation
- Longer leads for Easier Mounting



TO-247AD

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current (Fig.1)	60	A
I_C @ T_C = 100°C	Continuous Collector Current (Fig.1)	30	
I_{CM}	Pulsed Collector Current (Fig.3, Fig. CT.5)	120	
I_{LM}	Clamped Inductive Load Current(Fig.4, Fig. CT.2)	120	
I_F @ T_C = 100°C	Diode Continuous Forward Current	30	
I_{FM}	Diode Maximum Forward Current	120	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation (Fig.2)	300	W
P_D @ T_C = 100°C	Maximum Power Dissipation (Fig.2)	120	
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300, (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	0.42	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	0.83	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	40	
W_t	Weight	—	6 (0.21)	—	g (oz)
$Z_{\theta JC}$	Transient Thermal Impedance Junction-to-Case (Fig.24)				

Electrical Characteristics @ TJ = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	Fig.
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200			V	V_{GE} = 0V,I_c =250 µA	
$\Delta V_{(BR)CES}$ / ΔTj	Temperature Coeff. of Breakdown Voltage		+1.2		V/°C	V_{GE} = 0V, I_c = 1 mA (25 -125 °C)	
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage		2.28	2.48	V	I_C = 25A, V_{GE} = 15V	5, 6
			2.46	2.66		I_C = 30A, V_{GE} = 15V	7, 9
			3.43	4.00		I_C = 60A, V_{GE} = 15V	10
			2.74	3.10		I_C = 25A, V_{GE} = 15V, T_J = 125°C	11
			2.98	3.35		I_C = 30A, V_{GE} = 15V, T_J = 125°C	
$V_{GE(th)}$	Gate Threshold Voltage	4.0	5.0	6.0	V	V_{CE} = V_{GE}, I_C = 250 µA	9,10,11,12
$\Delta V_{GE(th)}$ / ΔTj	Temperature Coeff. of Threshold Voltage		- 1.2		mV/°C	V_{CE} = V_{GE}, I_C = 1 mA (25 -125 °C)	
g_{fe}	Forward Transconductance	14.8	16.9	19.0	S	V_{CE} = 50V, I_C = 25A, PW=80µs	
I_{CES}	Zero Gate Voltage Collector Current			250	µA	V_{GE} = 0V,V_{CE} = 1200V	
			325	675		V_{GE} = 0v, V_{CE} = 1200V, T_J =125°C	
				2000		V_{GE} = 0v, V_{CE} = 1200V, T_J =150°C	
V_{FM}	Diode Forward Voltage Drop		1.76	2.06	V	I_C = 25A	8
			1.86	2.17		I_C = 30A	
			1.87	2.18		I_C = 25A, T_J = 125°C	
			2.01	2.40		I_C = 30A, T_J = 125°C	
I_{GES}	Gate-to-Emitter Leakage Current			±100	nA	V_{GE} = ±20V	

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	Fig.
Q_g	Total Gate charge (turn-on)		169	254	nC	I_C = 25A	23
Q_{ge}	Gate - Emitter Charge (turn-on)		19	29		V_{CC} =600V	CT1
Q_{gc}	Gate - Collector Charge (turn-on)		82	123		V_{GE} = 15V	
E_{on}	Turn-On Switching Loss		1066	1250	µJ	I_C = 25A, V_{CC} = 600V	CT4
E_{off}	Turn-Off Switching Loss		1493	1800		V_{GE} = 15V, Rg = 5Ω, L=200µH	WF1
E_{tot}	Total Switching Loss		2559	3050		T_J = 25°C, Energy losses include tail and diode reverse recovery	WF2
E_{on}	Turn-on Switching Loss		1660	1856	µJ	Ic =25A, V_{CC}=600V	13, 15
E_{off}	Turn-off Switching Loss		2118	2580		V_{GE} = 15V, Rg = 5Ω, L=200µH	CT4
E_{tot}	Total Switching Loss		3778	4436		T_J = 125°C, Energy losses include tail and diode reverse recovery	WF1 & 2
td(on)	Turn - on delay time		50	65	ns	Ic =25A, V_{CC}=600V	14, 16
tr	Rise time		25	35		V_{GE} = 15V, Rg = 5Ω, L=200µH	CT4
td(off)	Turn - off delay time		210	230		T_J = 125°C,	WF1
tf	Fall time		60	75			WF2
C_{ies}	Input Capacitance		2200		pF	V_{GE} = 0V	
C_{oes}	Output Capacitance		210			V_{CC} = 30V	22
C_{res}	Reverse Transfer Capacitance		85			f = 1.0 MHz	
RBSOA	Reverse bias safe operating area	FULL SQUARE				T_J =150°C, Ic = 120A V_{CC} = 1000V, V_P = 1200V Rg = 5Ω, V_{GE} = +15V to 0 V	4 CT2
SCSOA	Short Circuit Safe Operating Area	10	----	----	µs	T_J = 150°C V_{CC} = 900V,V_P = 1200V Rg = 5Ω, V_{GE} = +15V to 0 V	CT3 WF4
E_{rec}	Reverse recovery energy of the diode		1820	2400	µJ	T_J = 125°C	17,18,19
trr	Diode Reverse recovery time		300		ns	V_{CC} = 600V, Ic = 25A	20, 21
Irr	Peak Reverse Recovery Current		34	38	A	V_{GE} = 15V, Rg = 5Ω, L=200µH	CT4, WF3
Le	Internal Emitter Inductance		13		nH	Measured 5 mm from the package.	

Fig.1 - Maximum DC Collector Current vs. Case Temperature

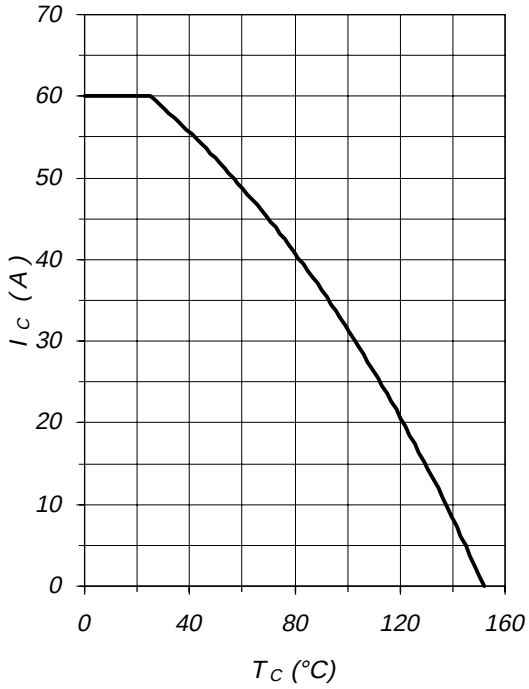


Fig.2 - Power Dissipation vs. Case Temperature

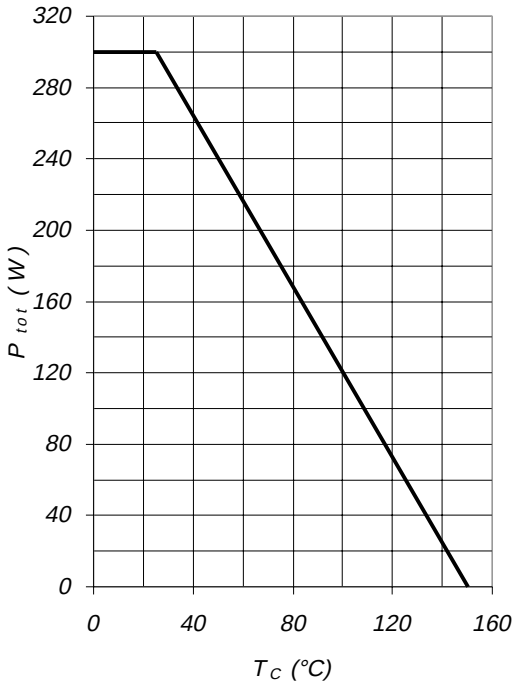


Fig.3 - Forward SOA
T_C=25°C; Tj≤150°C

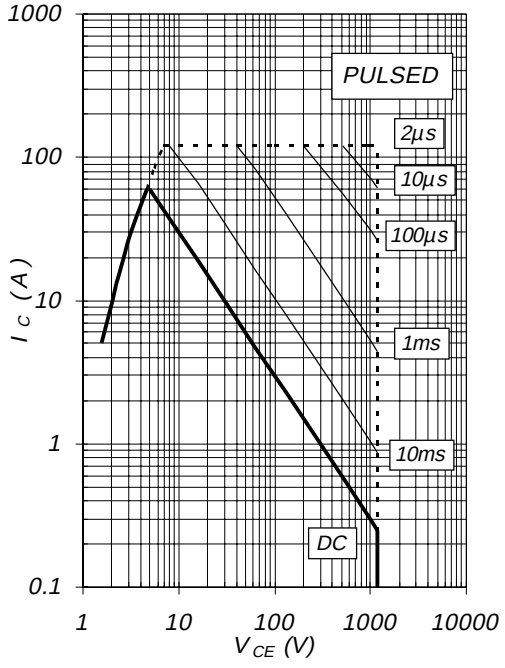


Fig.4 - Reverse Bias SOA
Tj = 150°C, V_{GE} = 15V

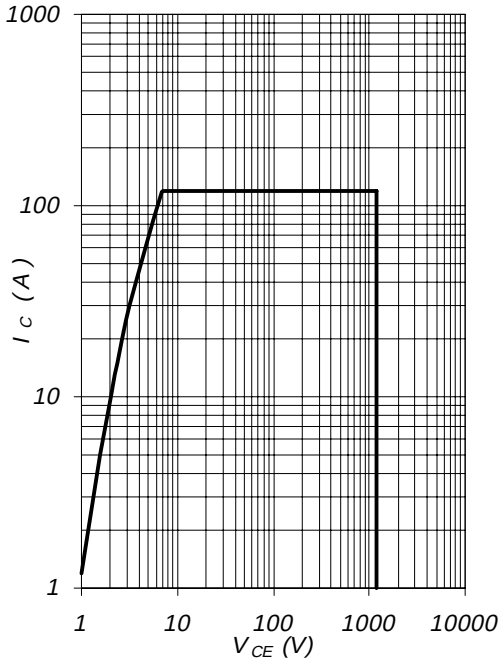


Fig.5 - Typical IGBT Output Characteristics
Tj= -40°C; tp=300µs

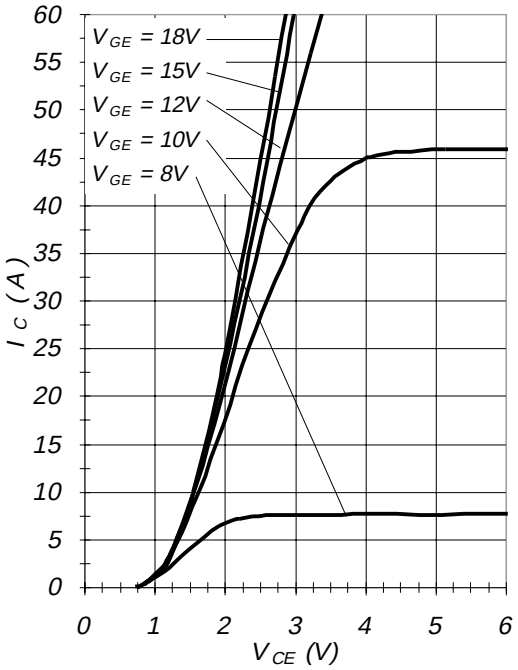


Fig.6 - Typical IGBT Output Characteristics
Tj=25°C; tp=300µs

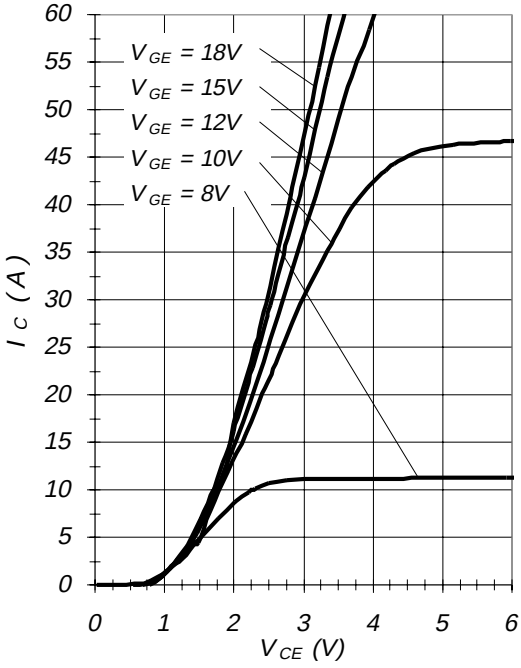


Fig.7 - Typical IGBT Output Characteristics
Tj=125°C; tp=300µs

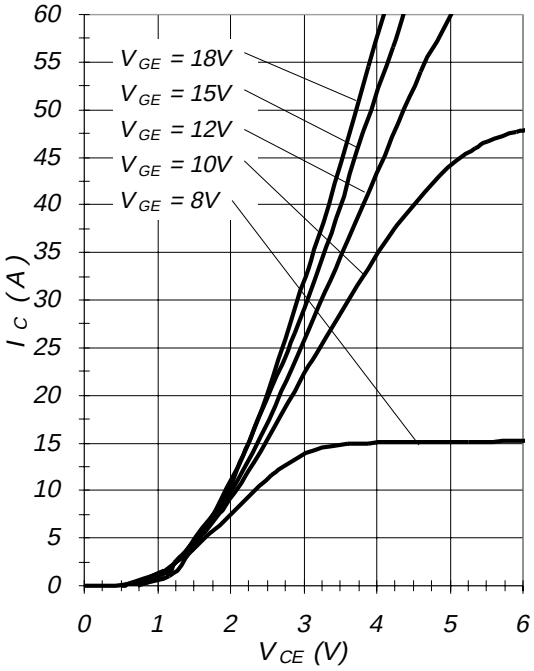


Fig.8 - Typical Diode Forward Characteristic
tp=300µs

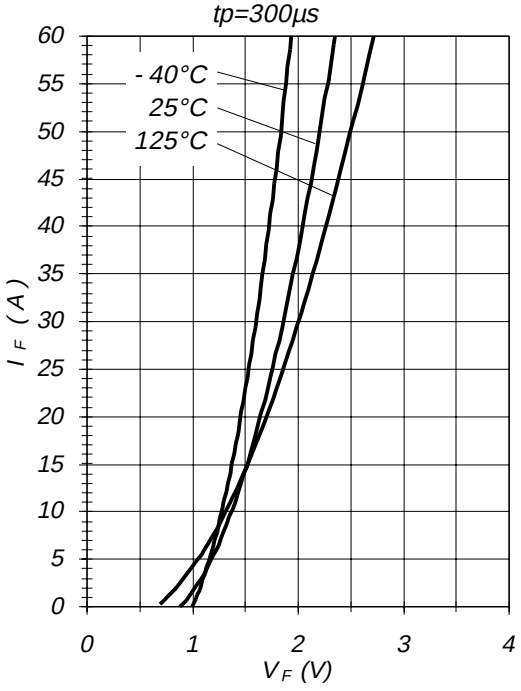


Fig.9 - Typical V_{CE} vs V_{GE}
Tj= -40°C

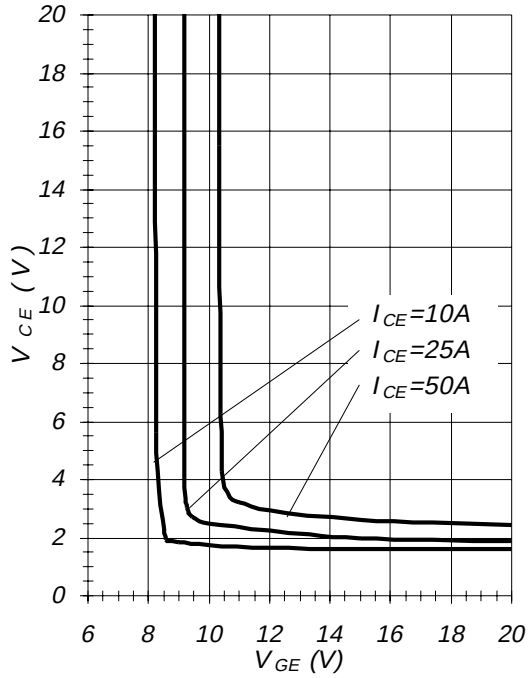


Fig.10 - Typical V_{CE} vs V_{GE}
Tj= 25°C

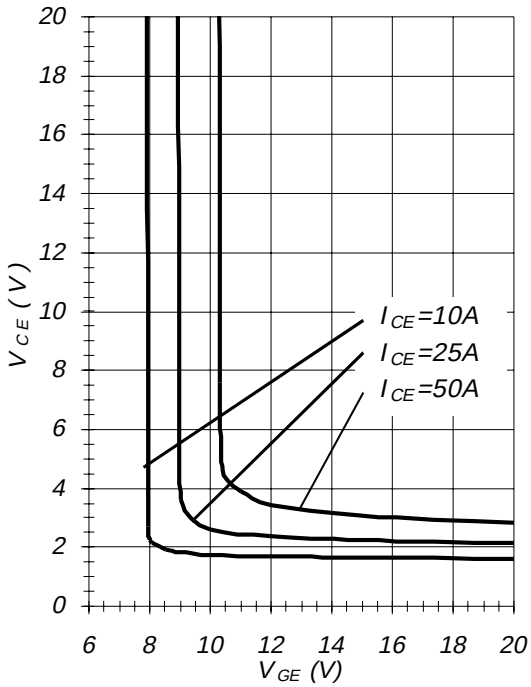


Fig.11 - Typical V_{CE} vs V_{GE}
Tj= 125°C

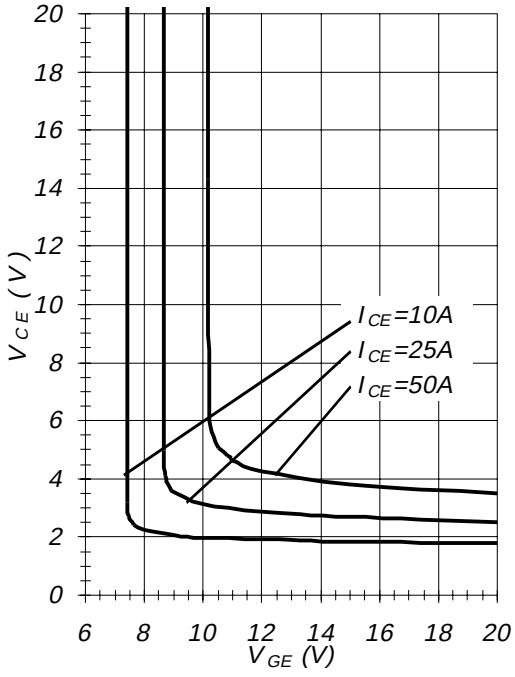


Fig.12 - Typ. Transfer Characteristics
V_{CE}=20V; tp=20µs

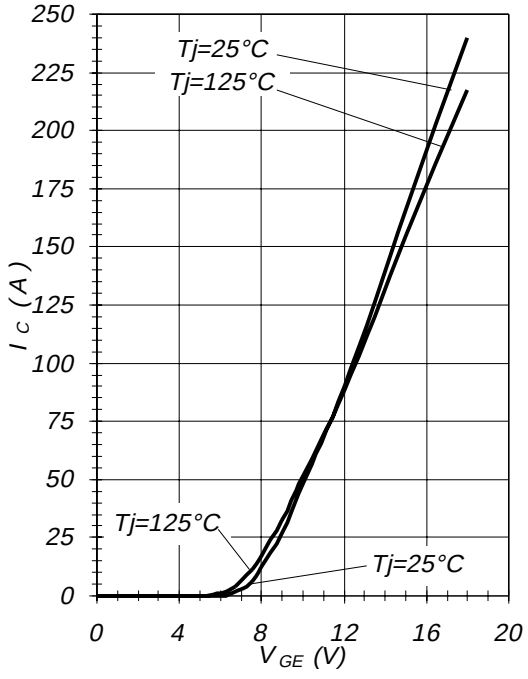


Fig.13 - Typical Energy Loss vs Ic
Tj=125°C; L=200µH; V_{CE}=600V;
Rg=22Ω ; V_{GE}=15V

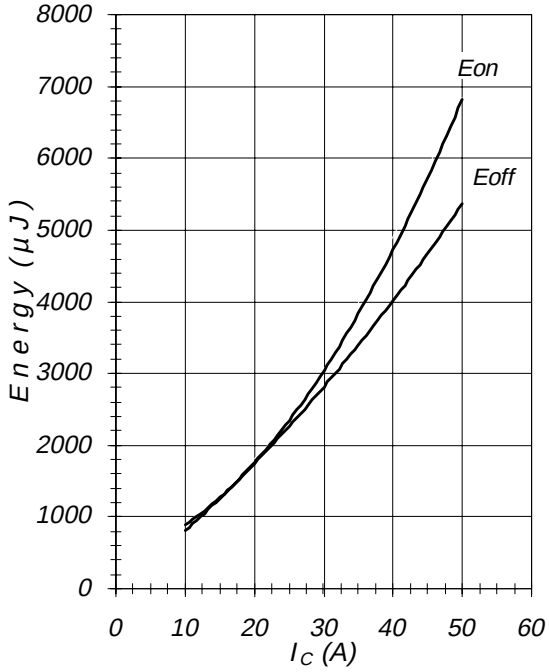


Fig.14 - Typical Switching Time vs Ic
Tj=125°C; L=200µH; V_{CE}=600V;
Rg=22Ω ;V_{GE}=15V

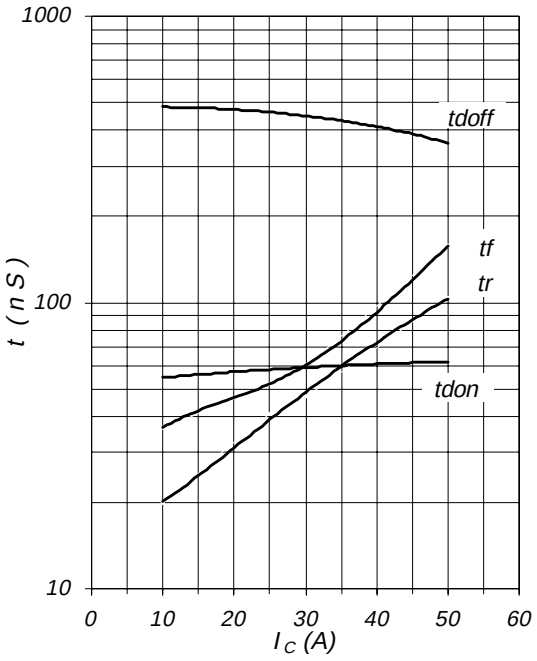


Fig.15 - Typical Energy Loss vs Rg
Tj=125°C; L=200µH; V_{CE}=600V;
I_{CE}=25A; V_{GE}=15V

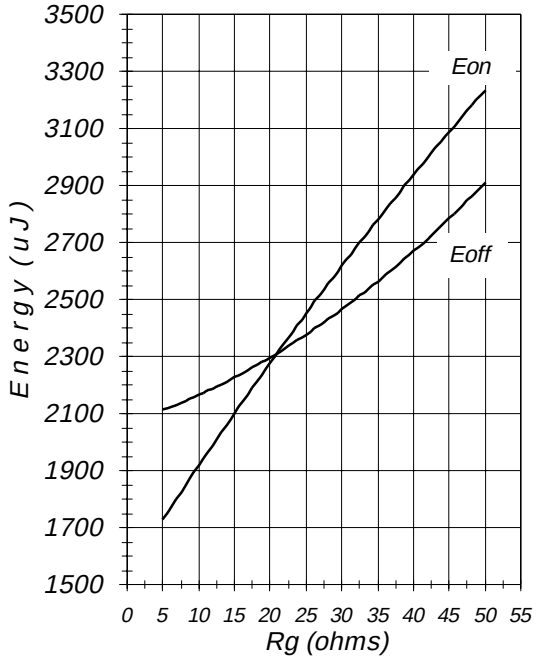


Fig.16 - Typical Switching Time vs Rg
Tj=125°C; L=200µH; V_{CE}=600V;
I_{CE}=25A; V_{GE}=15V

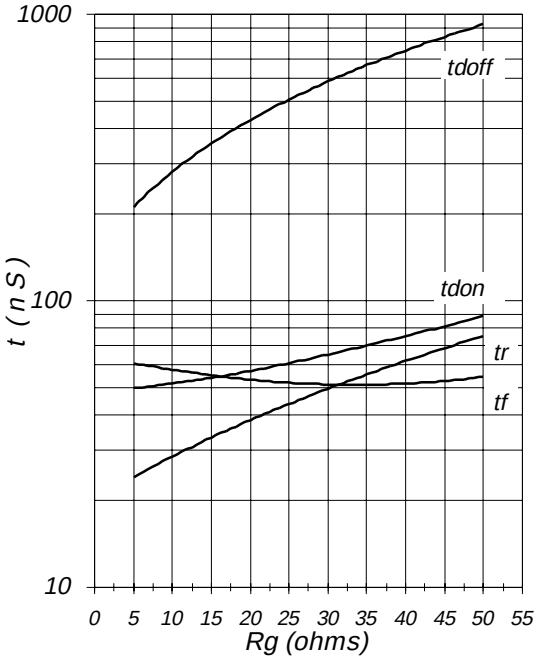


Fig.17 - Typical Diode I_{RR} vs I_F
Tj=125°C

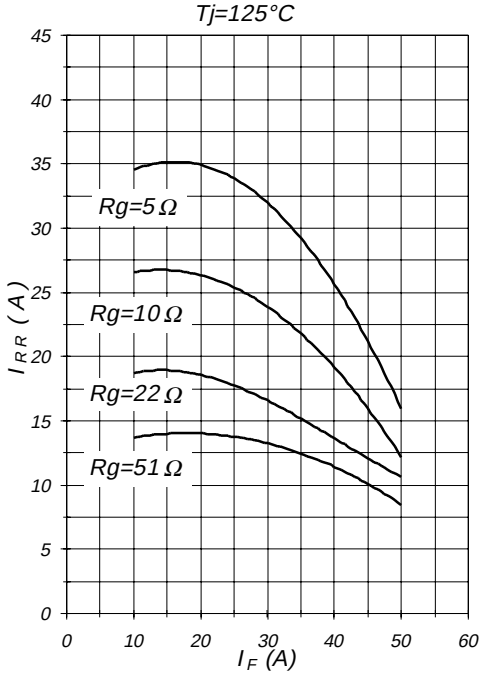


Fig.18 - Typical Diode I_{RR} vs Rg
Tj=125°C; I_F=25A

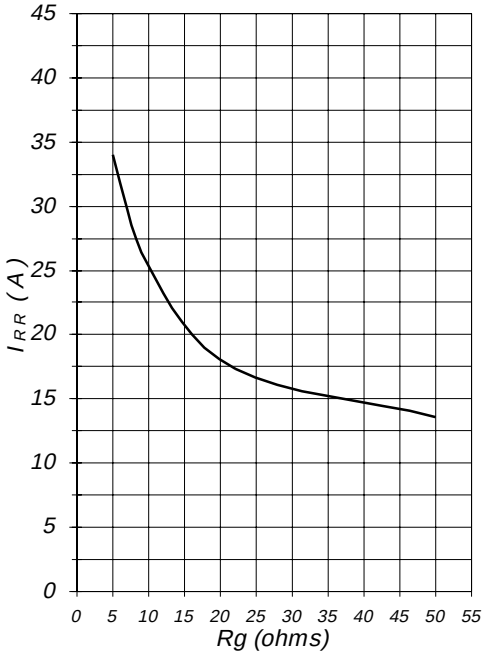


Fig.19 - Typical Diode I_{RR} vs dI_F/dt
V_{CC}=600V; V_{GE}=15V
I_F=25A; Tj=125°C

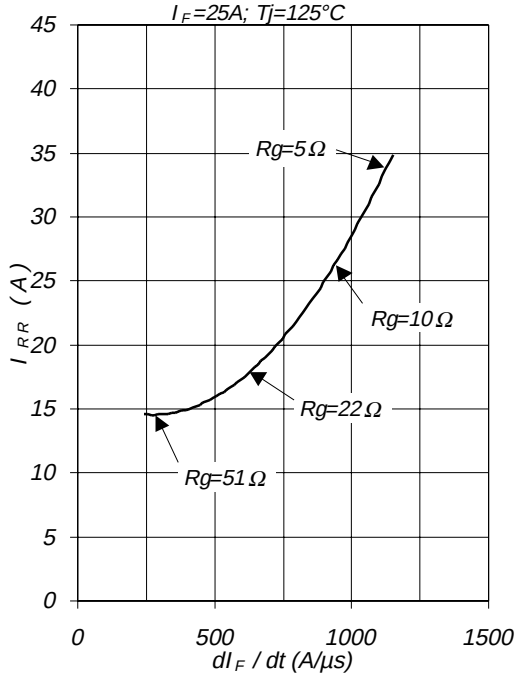


Fig.20 - Typical Diode Q_{RR}
V_{CC}=600V; V_{GE}=15V; Tj=125°C

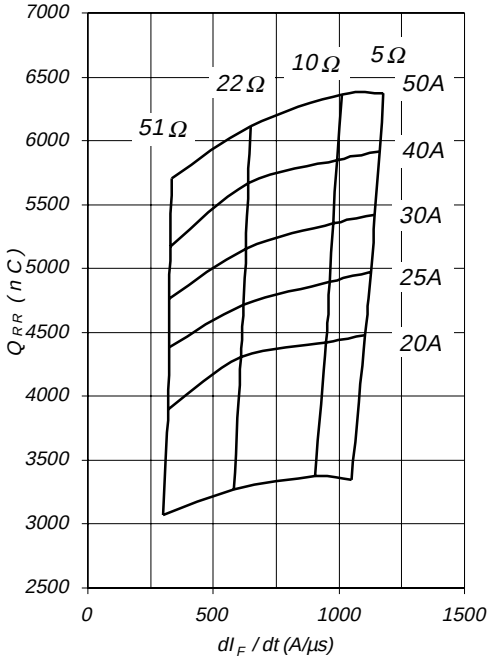


Fig.21 - Typ. Diode E_{rec} vs. I_F
Tj=125°C

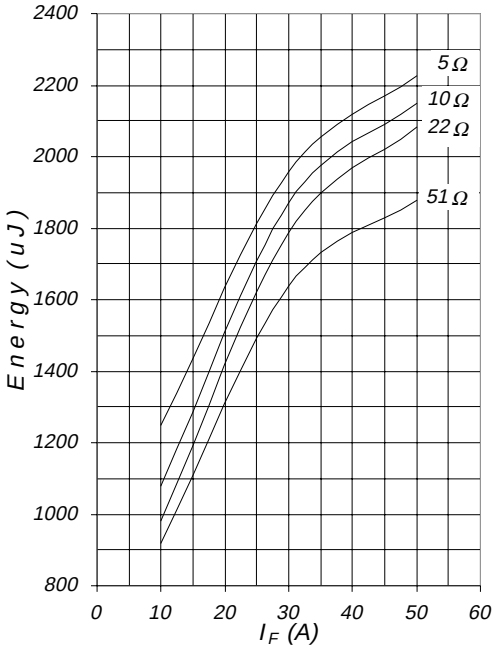


Fig.22 - Typical Capacitance vs V_{CE}
V_{GE}=0V; f=1MHz

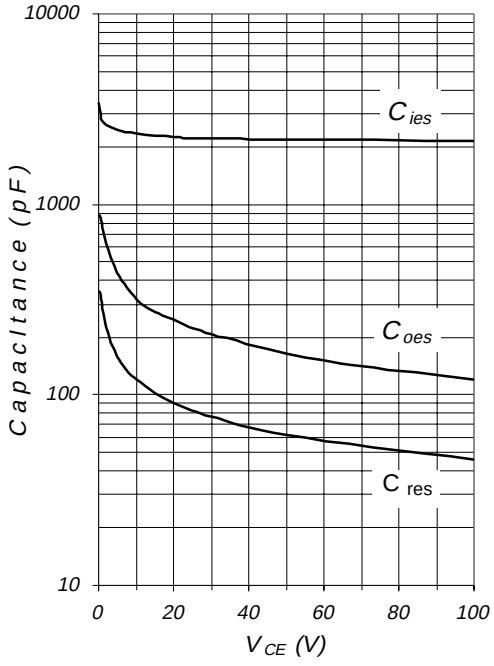


Fig.23 - Typ. Gate Charge vs. V_{GE}
I_C=25A; L=600µH

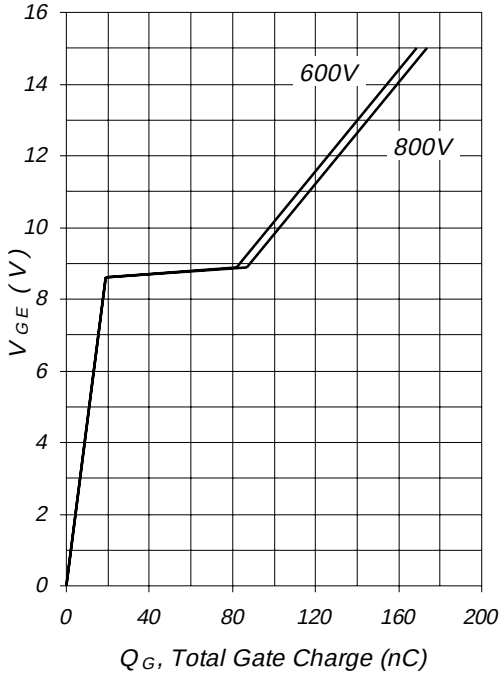


Fig.24 - Normalized Transient Thermal Impedance, Junction-to-Case

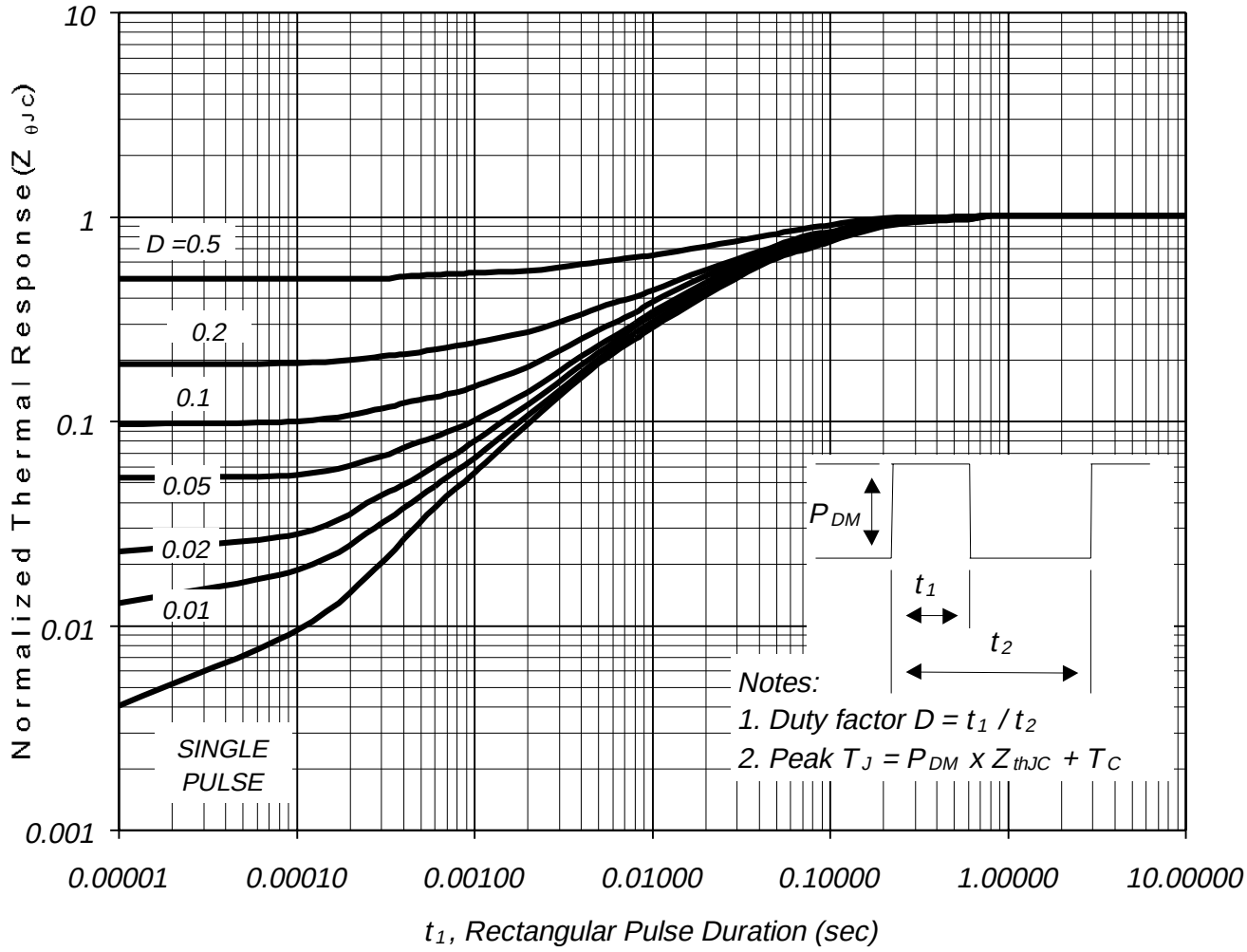


Fig. CT.1 - Gate Charge Circuit (turn-off)

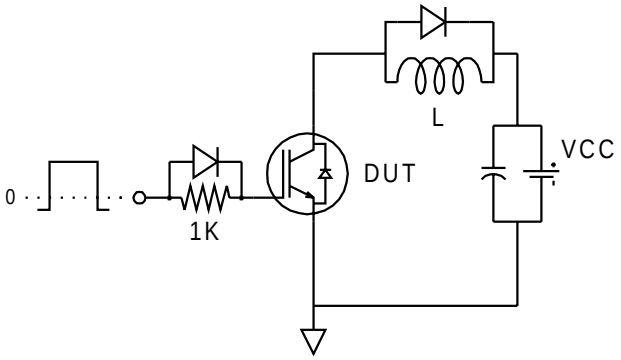


Fig. CT.2 - RBSOA Circuit

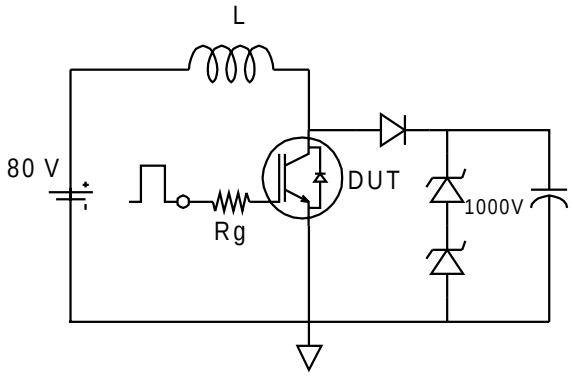


Fig. CT.3 - S.C. SOA Circuit

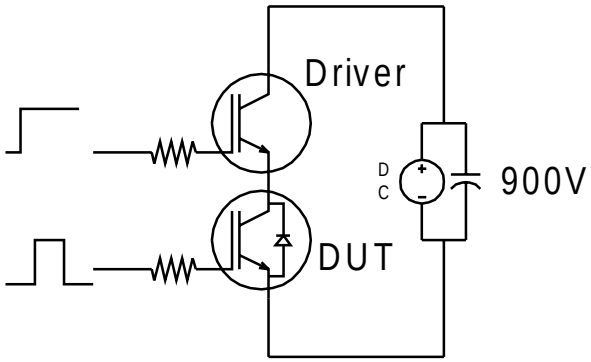


Fig. CT.4 - Switching Loss Circuit

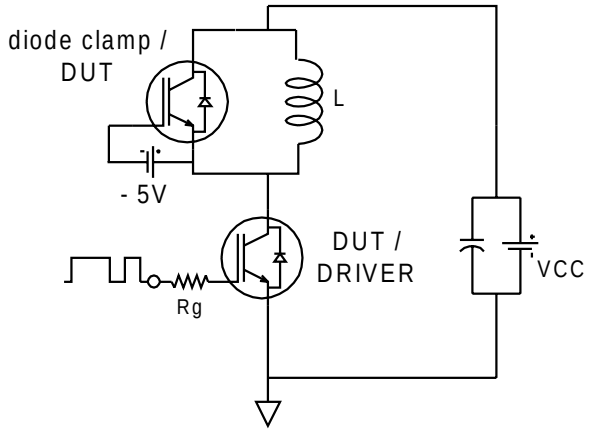


Fig. CT.5 - Resistive Load Circuit

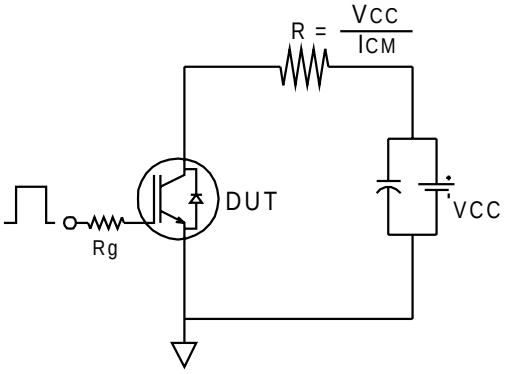


Fig. WF.1 - Typ. Turn-off Loss Waveform @ Tj=125°C using Fig. CT.4

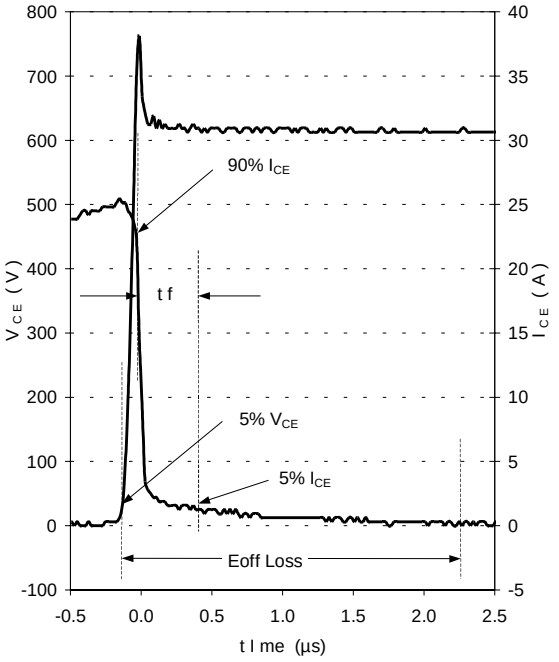


Fig. WF.2 - Typ. Turn-on Loss Waveform @ Tj=125°C using Fig. CT.4

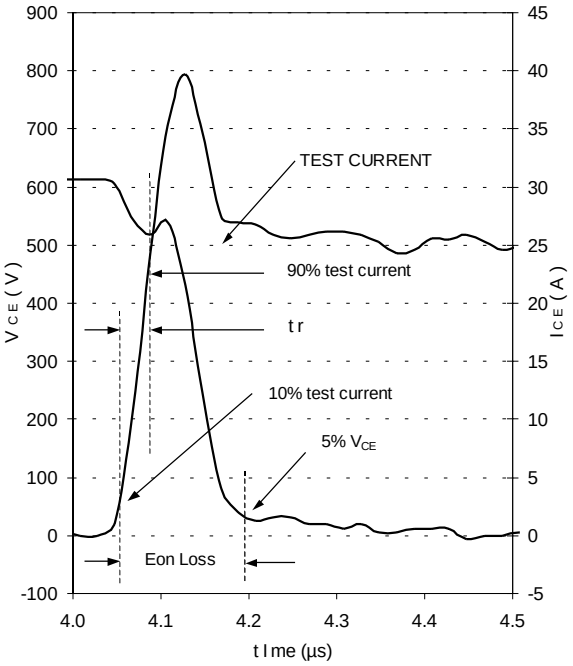


Fig. WF.3 - Typ. Diode Recovery Waveform @ Tj=125°C using Fig. CT.4

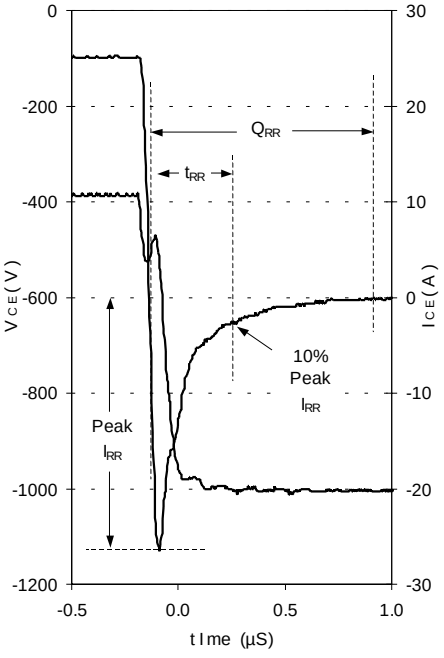
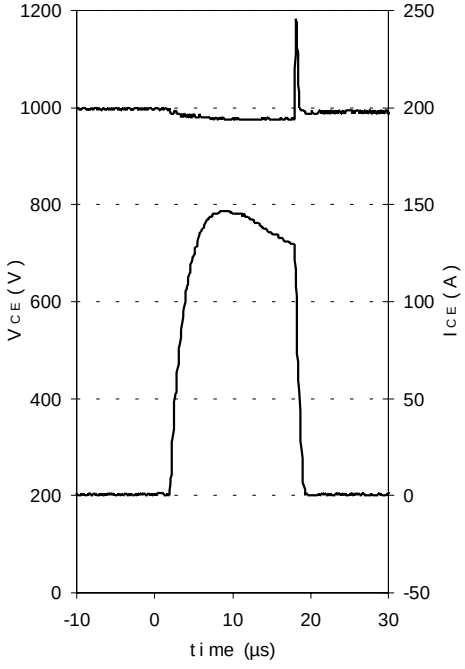
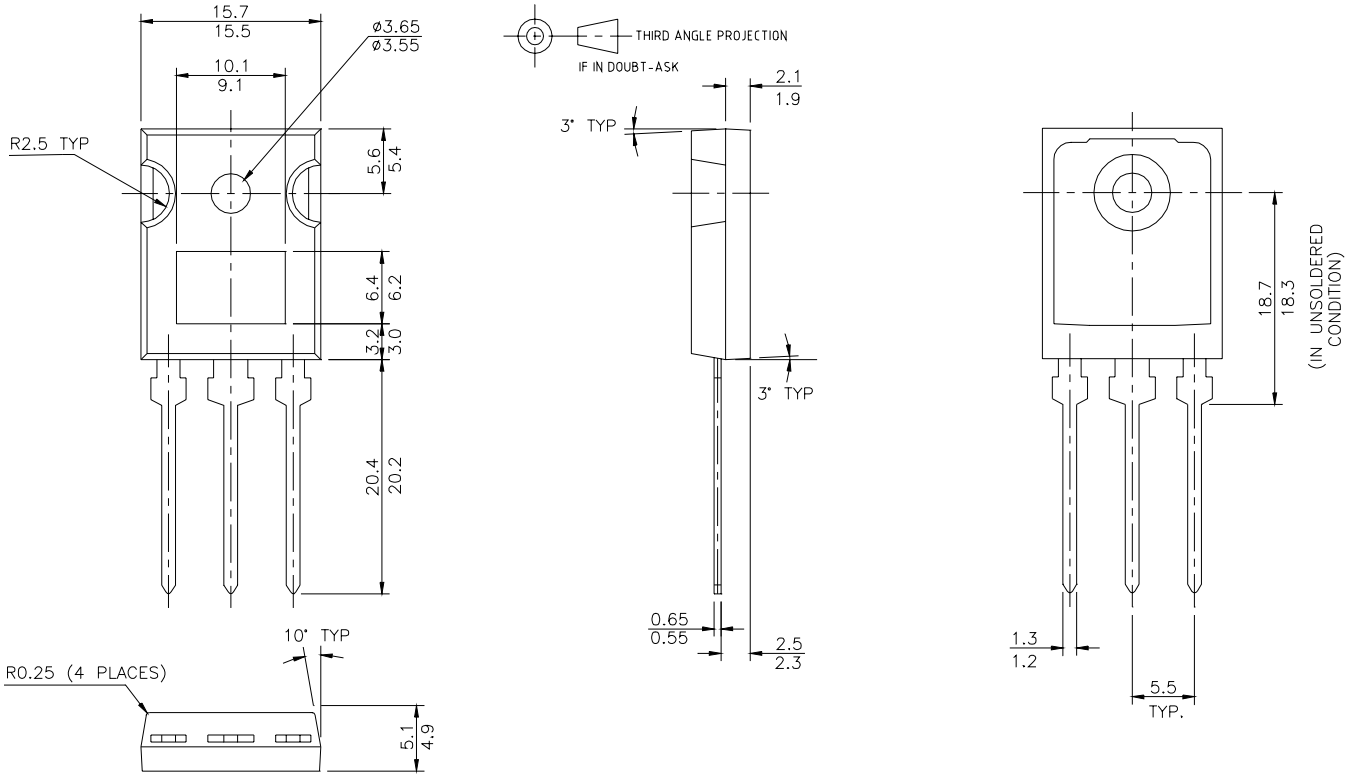


Fig. WF.4 - Typ. S.C. Waveform @ T_C=150°C using Fig. CT.3



TO-247AD Case Outline and Dimensions



International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 252-7105
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IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
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Data and specifications subject to change without notice. 12/99

PD - 91687A

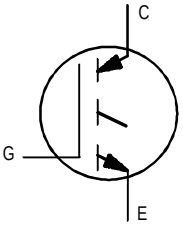
International
IOR Rectifier

PRELIMINARY

IRG4PSH71K

INSULATED GATE BIPOLAR TRANSISTOR

Short Circuit Rated
UltraFast IGBT



n-channel

V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.97V

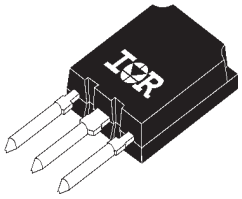
@V_{GE} = 15V, I_C = 42A

Features

- Hole-less clip/pressure mount package compatible with TO-247 and TO-264, with reinforced pins
- High short circuit rating IGBTs, optimized for motorcontrol
- Minimum switching losses combined with low conduction losses
- Tightest parameter distribution
- Creepage distance increased to 5.35mm

Benefits

- Highest current rating IGBT
- Maximum power density, twice the power handling of the TO-247, less space than TO-264



SUPER - 247

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	78	A
I_C @ T_C = 100°C	Continuous Collector Current	42	
I_{CM}	Pulsed Collector Current ①	156	
I_{LM}	Clamped Inductive Load Current ②	156	
t_{SC}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	170	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	350	W
P_D @ T_C = 100°C	Maximum Power Dissipation	140	
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	

Thermal Resistance\ Mechanical

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.36	°C/W
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	38	
	Recommended Clip Force	20.0(2.0)	—	—	N (kgf)
	Weight	—	6 (0.21)	—	g (oz)

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.1	—	V/°C	V_{GE} = 0V, I_C = 10mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.97	3.9	V	I_C = 42A V_{GE} = 15V
		—	3.44	—		I_C = 78A See Fig.2, 5
		—	2.60	—		I_C = 42A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-12	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.5mA
g_{fe}	Forward Transconductance ⑤	25	38	—	S	V_{CE} = 50V, I_C = 42A
I_{CES}	Zero Gate Voltage Collector Current	—	—	500	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	5.0	mA	V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	410	610	nC	I_C = 42A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	47	70		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	145	220		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	45	—	ns	T_J = 25°C
t_r	Rise Time	—	38	—		I_C = 42A, V_{CC} = 960V
$t_{d(off)}$	Turn-Off Delay Time	—	220	340		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	160	250		Energy losses include "tail"
E_{on}	Turn-On Switching Loss	—	2.35	—	mJ	See Fig. 9,10,14
E_{off}	Turn-Off Switching Loss	—	3.14	—		
E_{ts}	Total Switching Loss	—	5.49	8.3		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 720V, T_J = 125°C
						V_{GE} = 20V, R_G = 5.0Ω
$t_{d(on)}$	Turn-On Delay Time	—	42	—	ns	T_J = 150°C
t_r	Rise Time	—	41	—		I_C = 42A, V_{CC} = 960V
$t_{d(off)}$	Turn-Off Delay Time	—	460	—		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	250	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	11.5	—	mJ	See Fig. 10,11,14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	5770	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	400	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	100	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 5.0Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%

⑤ Pulse width 5.0µs, single shot

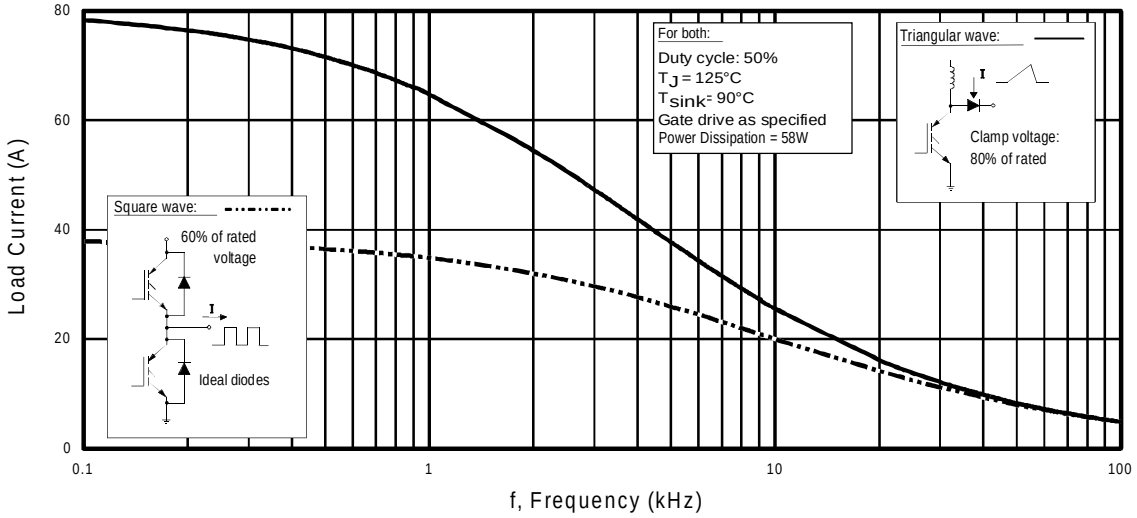


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

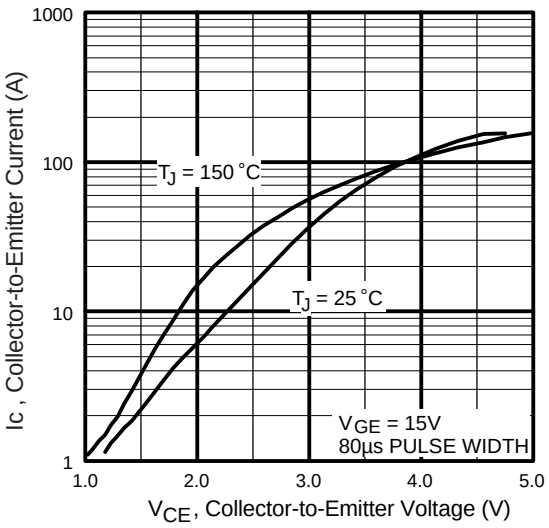


Fig. 2 - Typical Output Characteristics

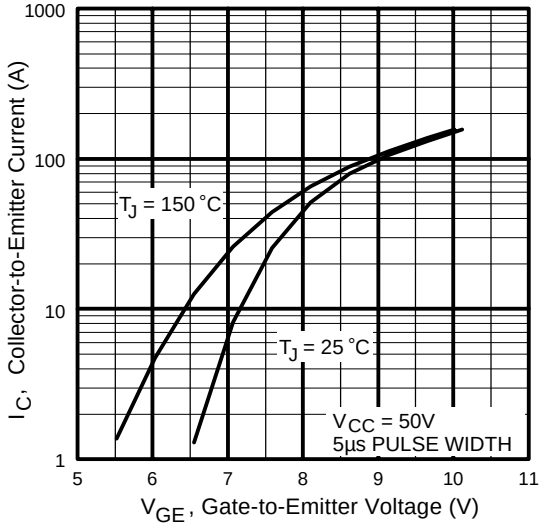


Fig. 3 - Typical Transfer Characteristics

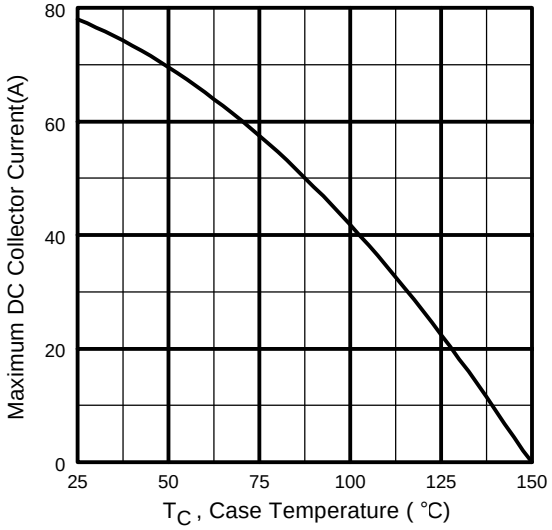


Fig. 4 - Maximum Collector Current vs. Case Temperature

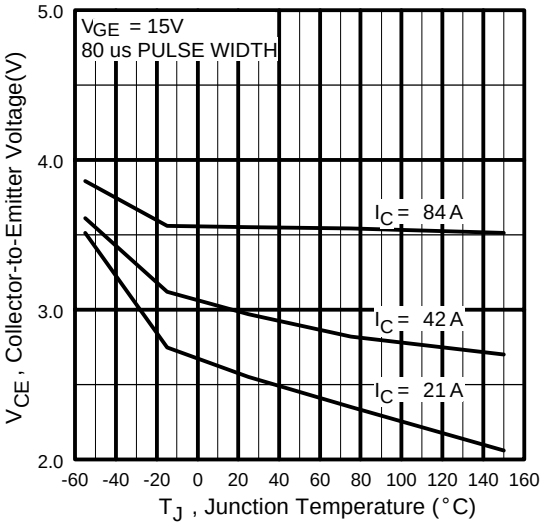


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

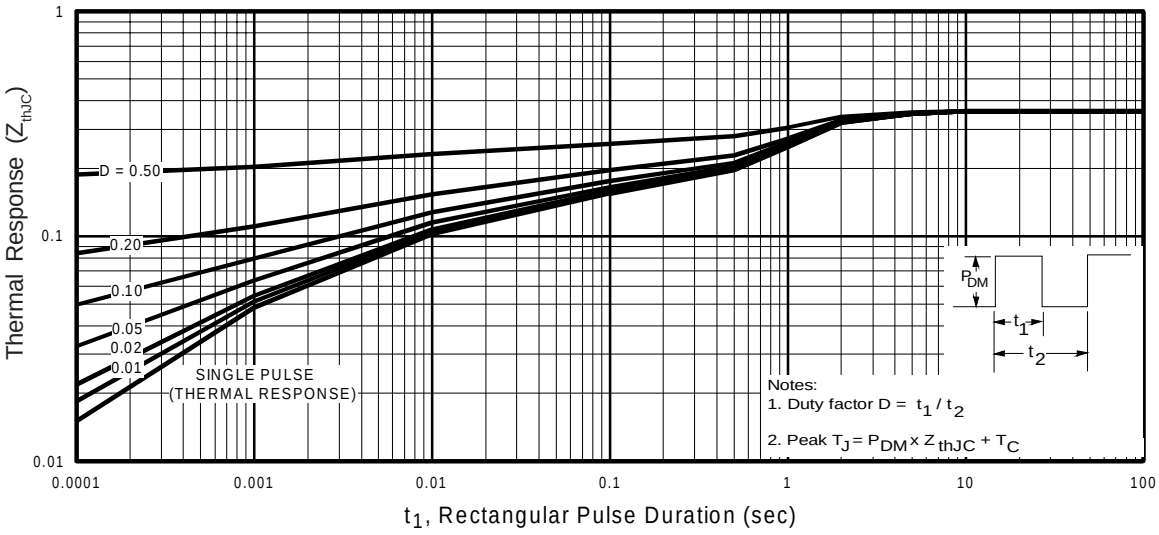


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

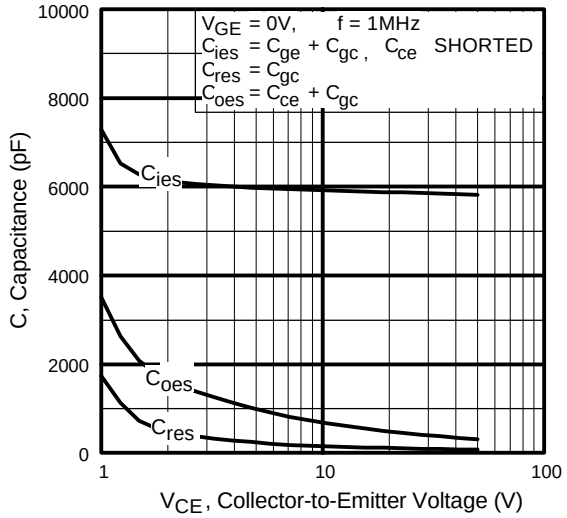


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

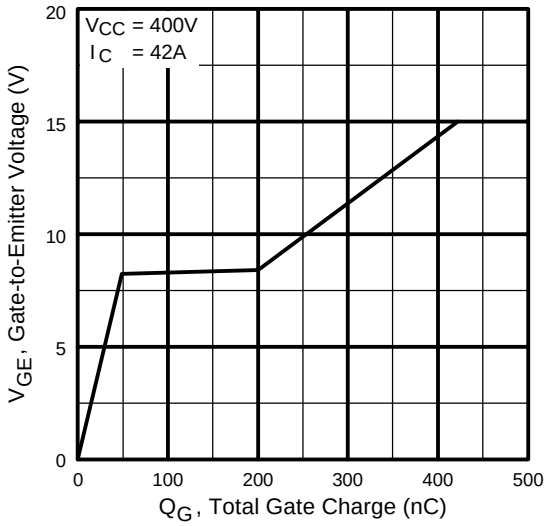


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

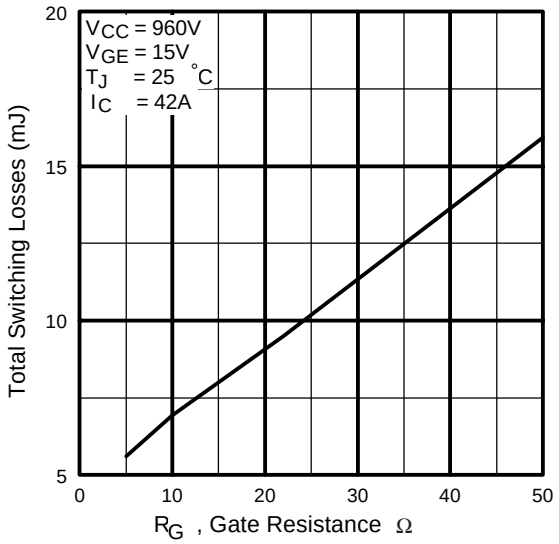


Fig. 9 - Typical Switching Losses vs. Gate Resistance

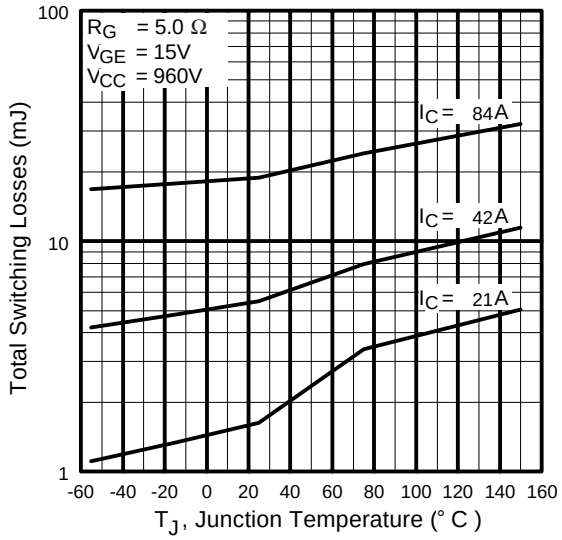


Fig. 10 - Typical Switching Losses vs. Junction Temperature

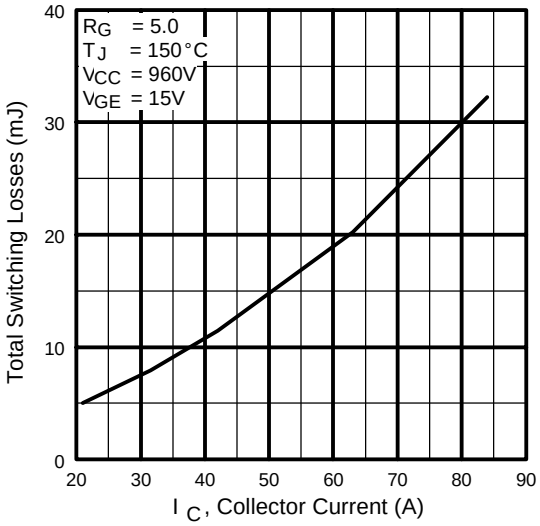


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

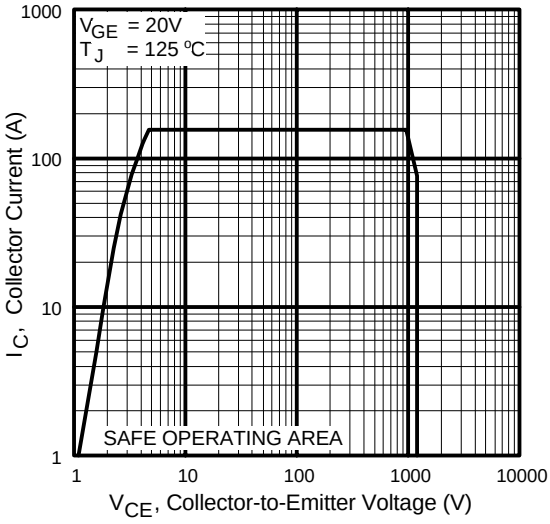


Fig. 12 - Turn-Off SOA

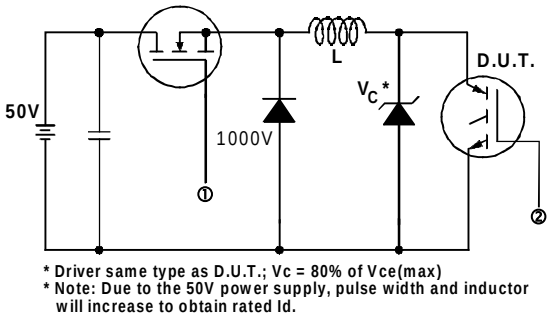


Fig. 13a - Clamped Inductive Load Test Circuit

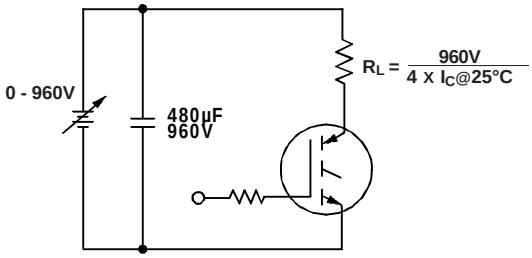


Fig. 13b - Pulsed Collector Current Test Circuit

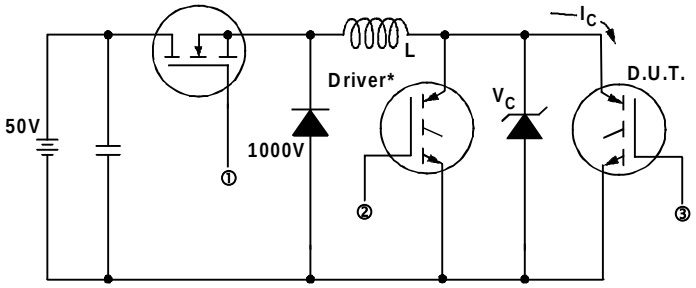


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 960V**

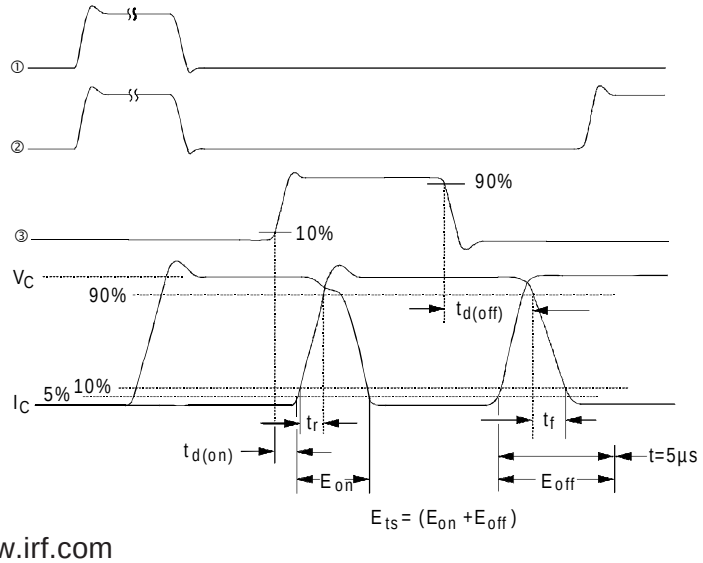
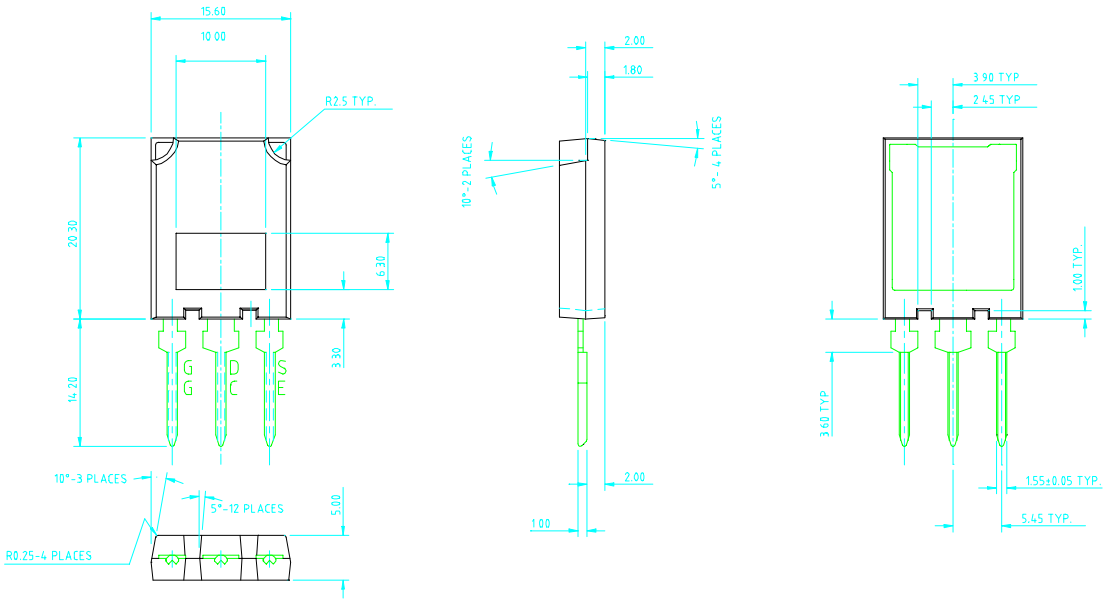


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — Super-247

Dimensions are shown in millimeters



International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936
http://www.irf.com/ Data and specifications subject to change without notice. 5/99

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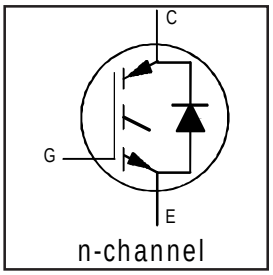
PD - 91688A

PRELIMINARY

IRG4PSH71KD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
UltraFast IGBT



V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.97V

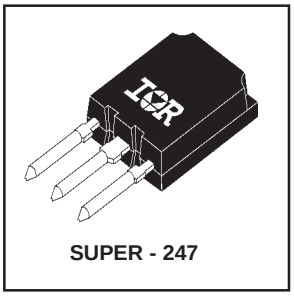
@V_{GE} = 15V, I_C = 42A

Features

- Hole-less clip/pressure mount package compatible with TO-247 and TO-264, with reinforced pins
- High short circuit rating IGBTs, optimized for motorcontrol
- Minimum switching losses combined with low conduction losses
- Tightest parameter distribution
- IGBT co-packaged with ultrafast soft recovery antiparallel diode
- Creepage distance increased to 5.35mm

Benefits

- Highest current rating copack IGBT
- Maximum power density, twice the power handling of the TO-247, less space than TO-264
- HEXFRED™ diode optimized for operation with IGBT, to minimize EMI, noise and switching losses



SUPER - 247

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	78	A
I_C @ T_C = 100°C	Continuous Collector Current	42	
I_{CM}	Pulsed Collector Current ①	156	
I_{LM}	Clamped Inductive Load Current ②	156	
I_F @ T_C = 100°C	Diode Continuous Forward Current	42	
I_{FM}	Diode Maximum Forward Current	156	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	350	W
P_D @ T_C = 100°C	Maximum Power Dissipation	140	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	

Thermal Resistance\ Mechanical

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	0.36	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	0.69	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	38	
	Recommended Clip Force	20.0(2.0)	—	—	N (kgf)
	Weight	—	6 (0.21)	—	g (oz)

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.1	—	V/°C	V_{GE} = 0V, I_C = 10mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.97	3.9	V	I_C = 42A V_{GE} = 15V
		—	3.44	—		I_C = 78A See Fig. 2, 5
		—	2.60	—		I_C = 42A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-12	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.5mA
g_{fe}	Forward Transconductance ④	25	38	—	S	V_{CE} = 50V, I_C = 42A
I_{CES}	Zero Gate Voltage Collector Current	—	—	500	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	10	mA	V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	2.5	3.7	V	I_C = 42A See Fig. 13
		—	2.4	—		I_C = 42A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	
Q_g	Total Gate Charge (turn-on)	—	410	610	nC	I_C = 42A	
Q_{ge}	Gate - Emitter Charge (turn-on)	—	47	70		V_{CC} = 400V See Fig.8	
Q_{gc}	Gate - Collector Charge (turn-on)	—	145	220		V_{GE} = 15V	
$t_{d(on)}$	Turn-On Delay Time	—	67	—	ns		
t_r	Rise Time	—	84	—		T_J = 25°C	
$t_{d(off)}$	Turn-Off Delay Time	—	230	350		I_C = 42A, V_{CC} = 800V	
t_f	Fall Time	—	130	190		V_{GE} = 15V, R_G = 5.0Ω	
E_{on}	Turn-On Switching Loss	—	5.68	—	mJ	Energy losses include "tail"	
E_{off}	Turn-Off Switching Loss	—	3.23	—		and diode reverse recovery	
E_{ts}	Total Switching Loss	—	8.90	11.6		See Fig. 9,10,18	
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 720V, T_J = 125°C	
						V_{GE} = 15V, R_G = 5.0Ω	
$t_{d(on)}$	Turn-On Delay Time	—	65	—	ns	T_J = 150°C, See Fig. 11,18	
t_r	Rise Time	—	87	—		I_C = 42A, V_{CC} = 800V	
$t_{d(off)}$	Turn-Off Delay Time	—	370	—		V_{GE} = 15V, R_G = 5.0Ω	
t_f	Fall Time	—	290	—		Energy losses include "tail"	
E_{ts}	Total Switching Loss	—	13.7	—	mJ	and diode reverse recovery	
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package	
C_{ies}	Input Capacitance	—	5770	—	pF	V_{GE} = 0V	
C_{oes}	Output Capacitance	—	400	—		V_{CC} = 30V See Fig. 7	
C_{res}	Reverse Transfer Capacitance	—	100	—		f = 1.0MHz	
t_{rr}	Diode Reverse Recovery Time	—	107	160	ns	T_J = 25°C See Fig.	I_F = 42A
		—	160	240		T_J = 125°C 14	
I_{rr}	Diode Peak Reverse Recovery Current	—	10	15	A	T_J = 25°C See Fig.	V_R = 200V
		—	16	24		T_J = 125°C 15	
Q_{rr}	Diode Reverse Recovery Charge	—	680	1020	nC	T_J = 25°C See Fig.	di/dt = 200A/µs
		—	1400	2100		T_J = 125°C 16	
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	250	—	A/µs	T_J = 25°C See Fig.	
	During t_b	—	320	—		T_J = 125°C 17	

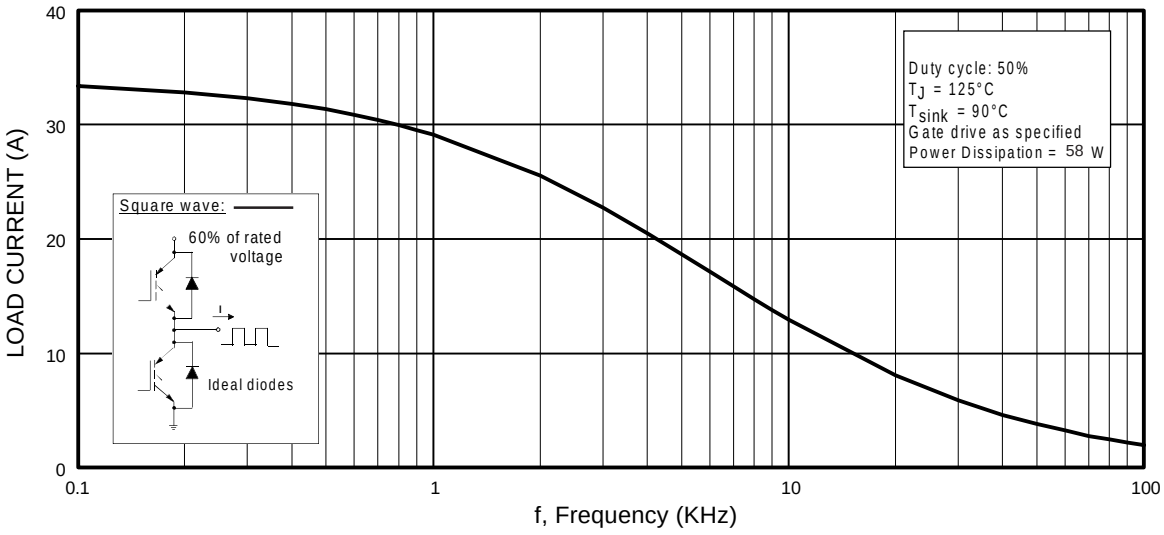


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

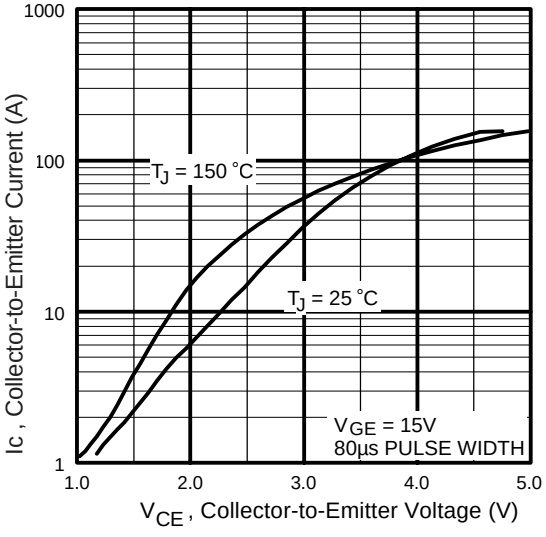


Fig. 2 - Typical Output Characteristics

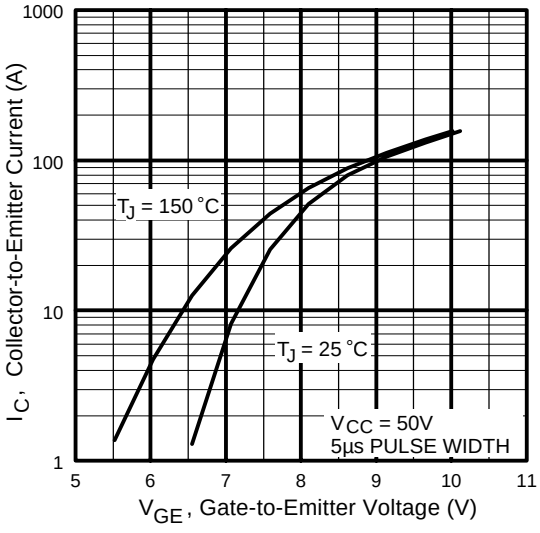


Fig. 3 - Typical Transfer Characteristics

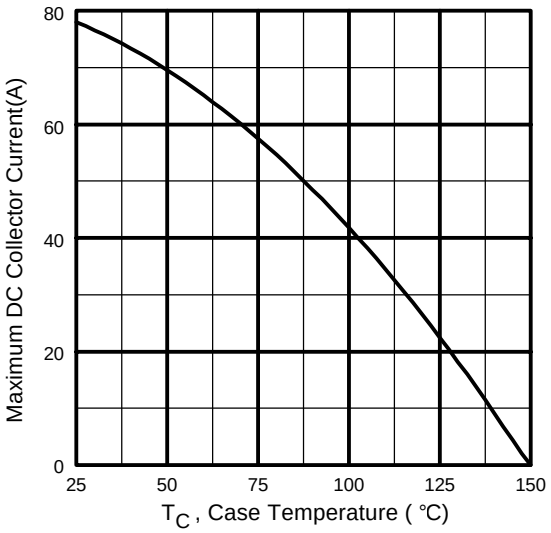


Fig. 4 - Maximum Collector Current vs. Case Temperature

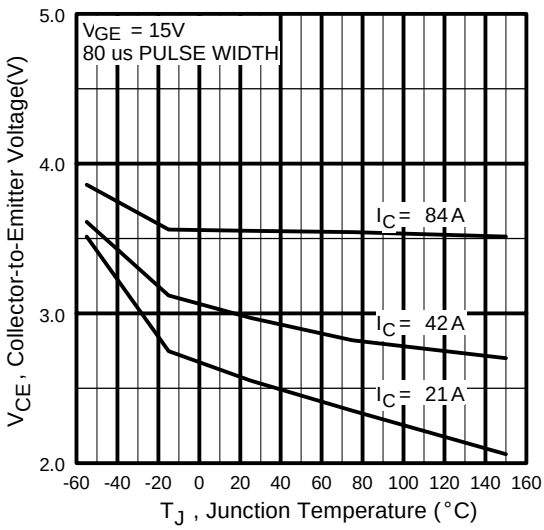


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

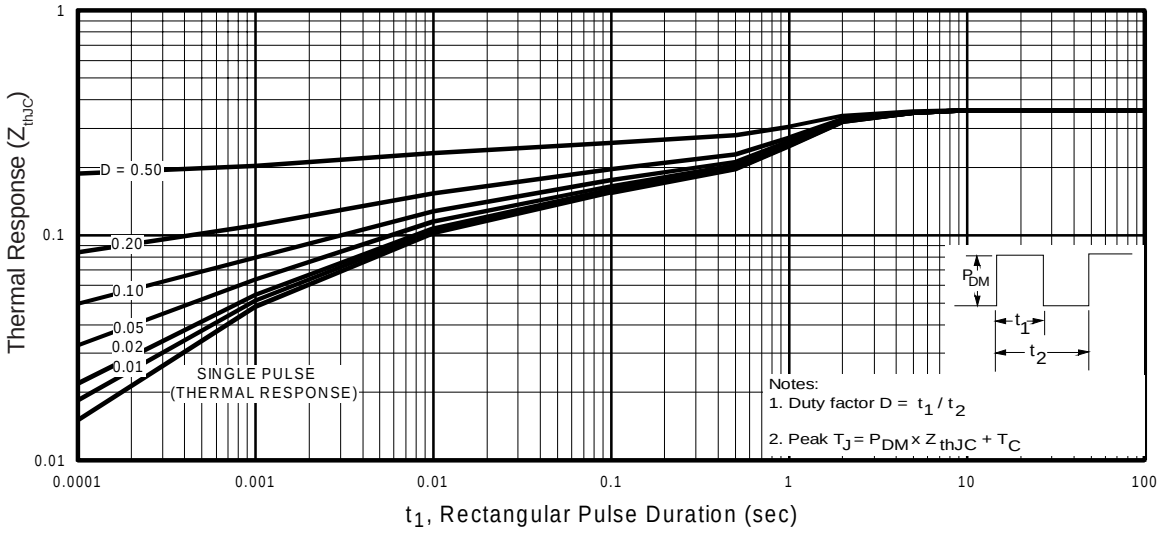


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

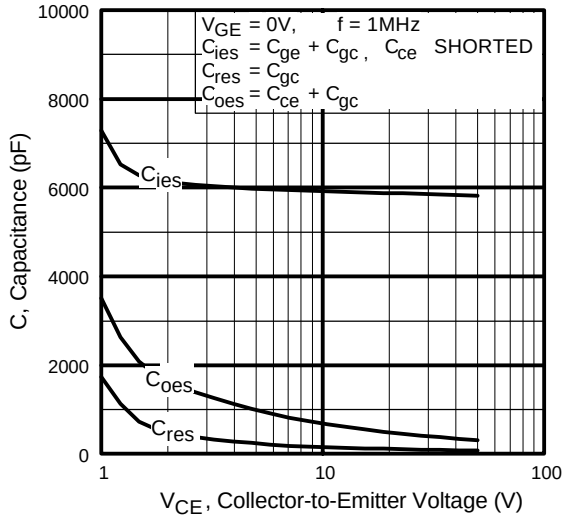


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

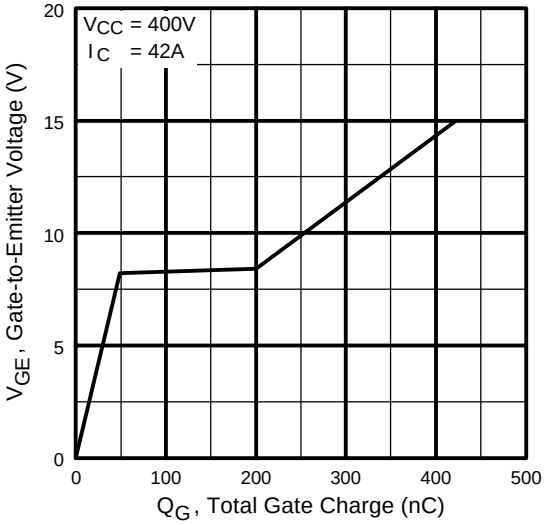


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

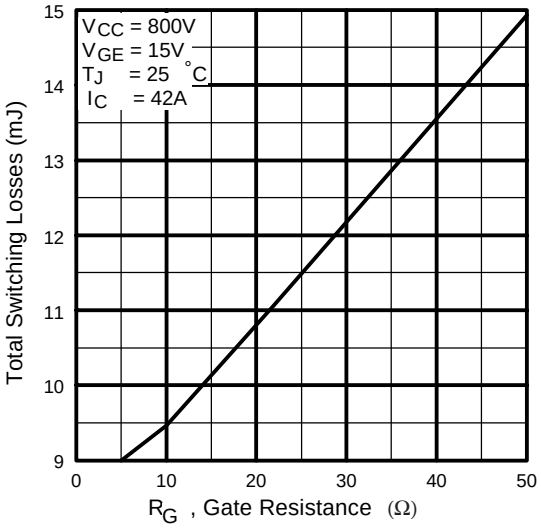


Fig. 9 - Typical Switching Losses vs. Gate Resistance

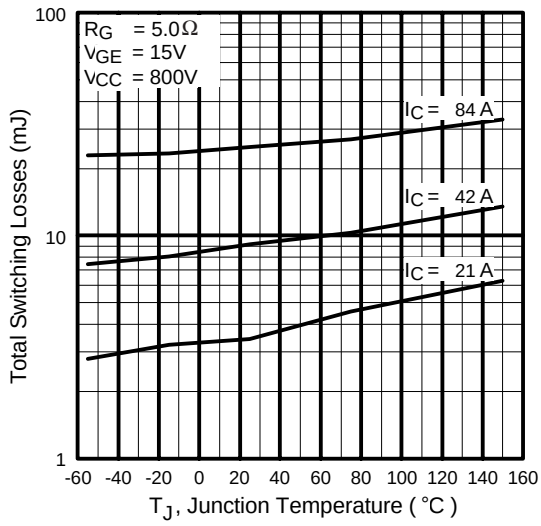
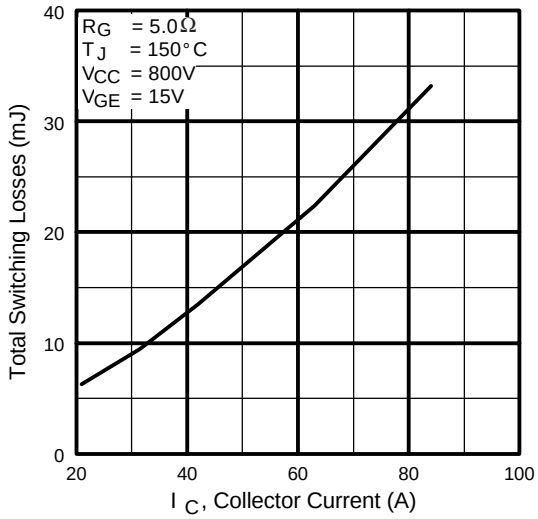
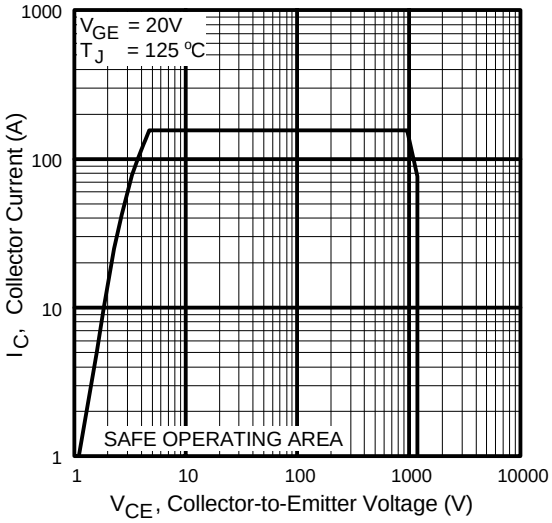


Fig. 10 - Typical Switching Losses vs. Junction Temperature





Collector-to-Emitter Current

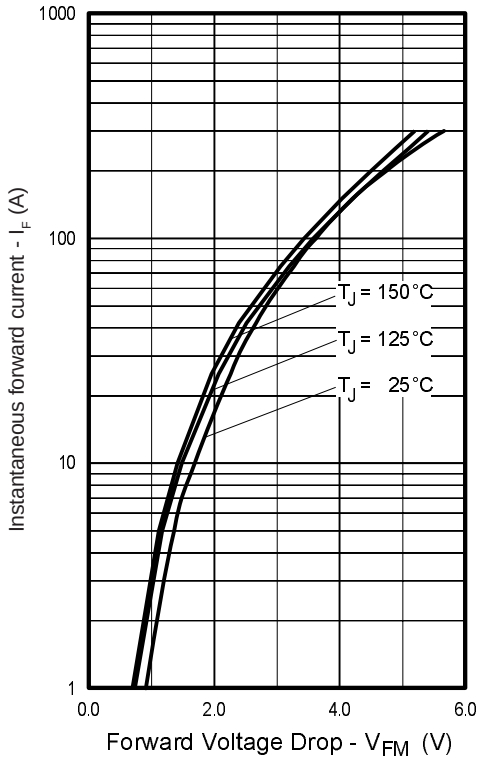


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

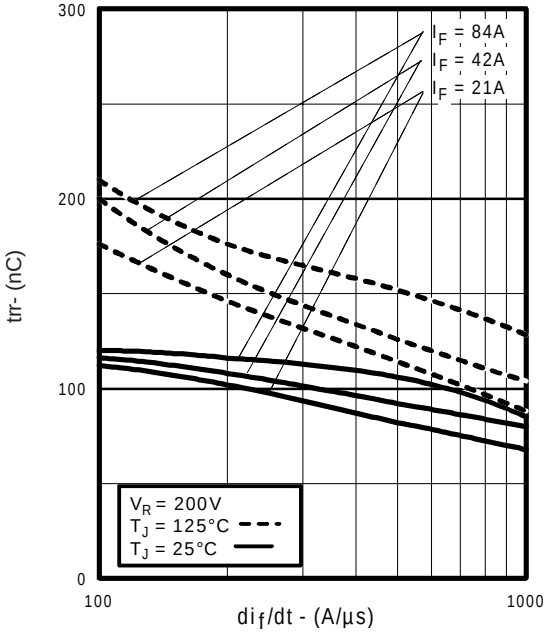


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

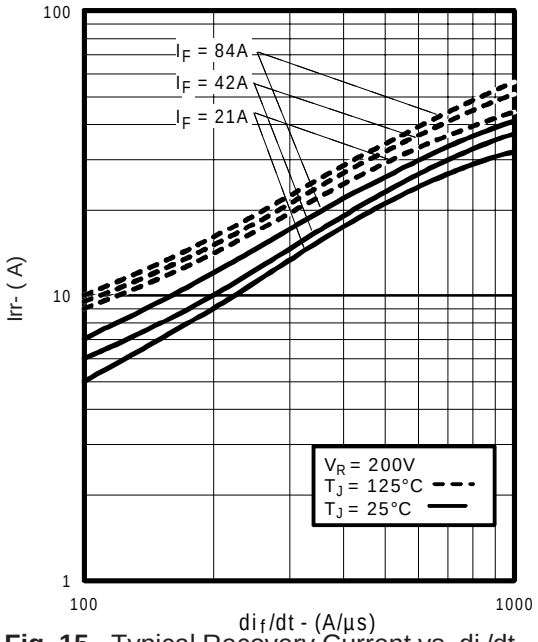


Fig. 15 - Typical Recovery Current vs. di_f/dt

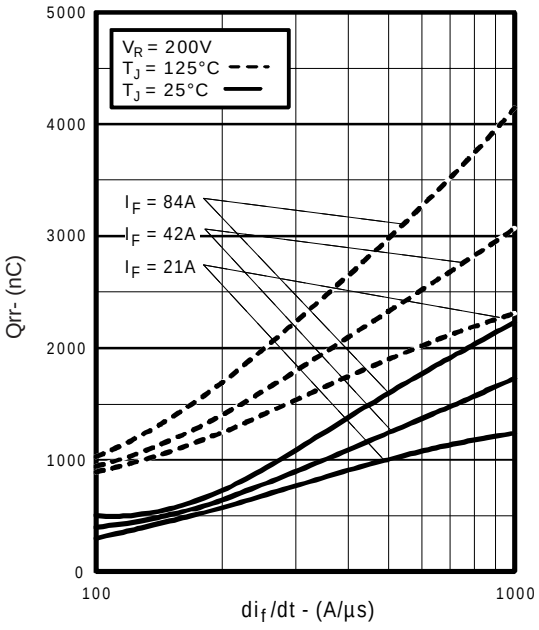


Fig. 16 - Typical Stored Charge vs. di_f/dt

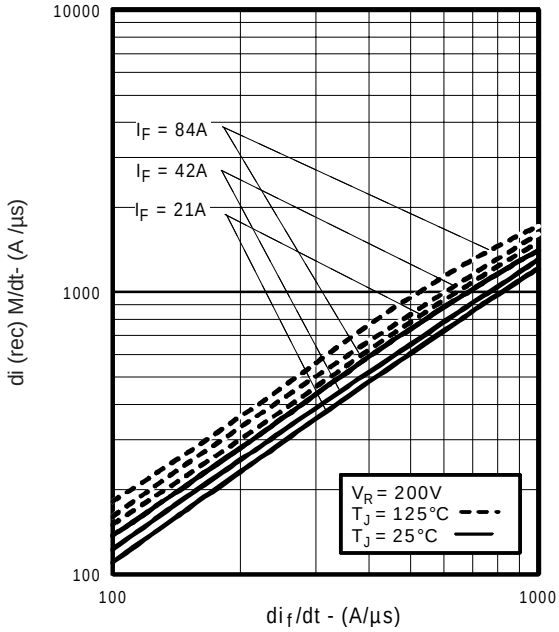


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

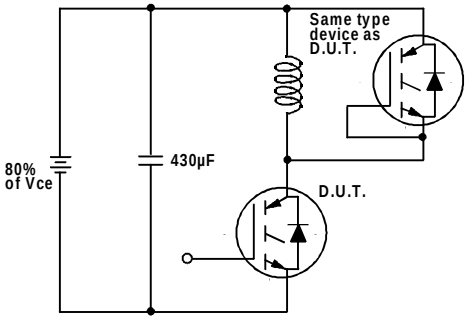


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

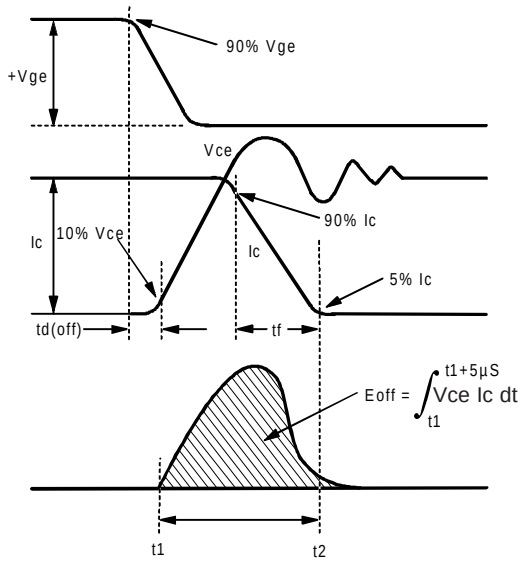


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

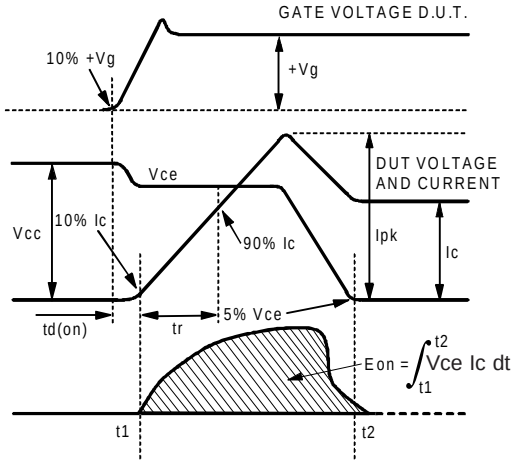


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

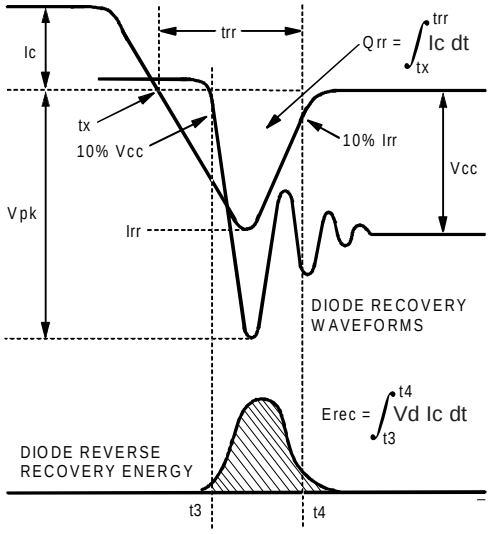


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

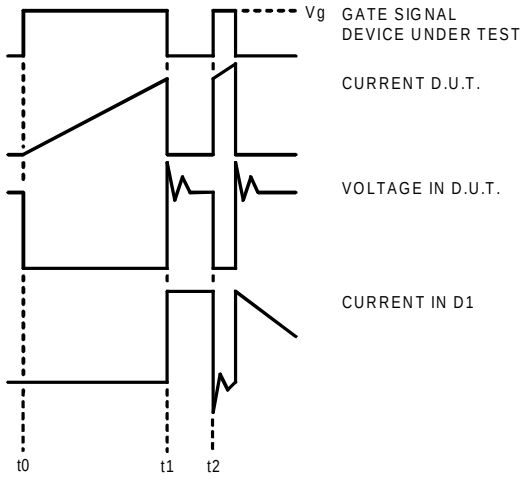


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

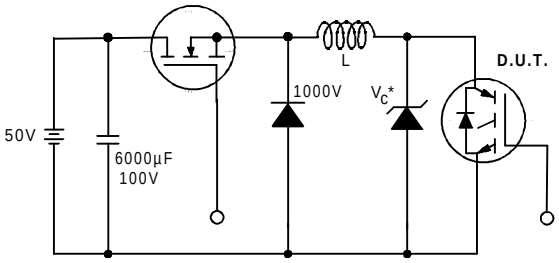


Figure 19. Clamped Inductive Load Test Circuit

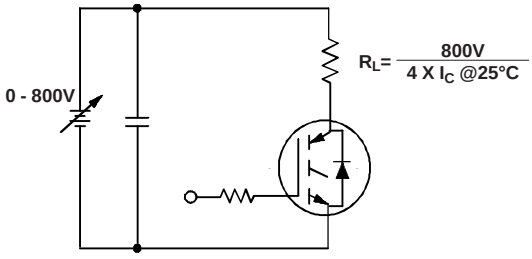


Figure 20. Pulsed Collector Current Test Circuit

Notes:

① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

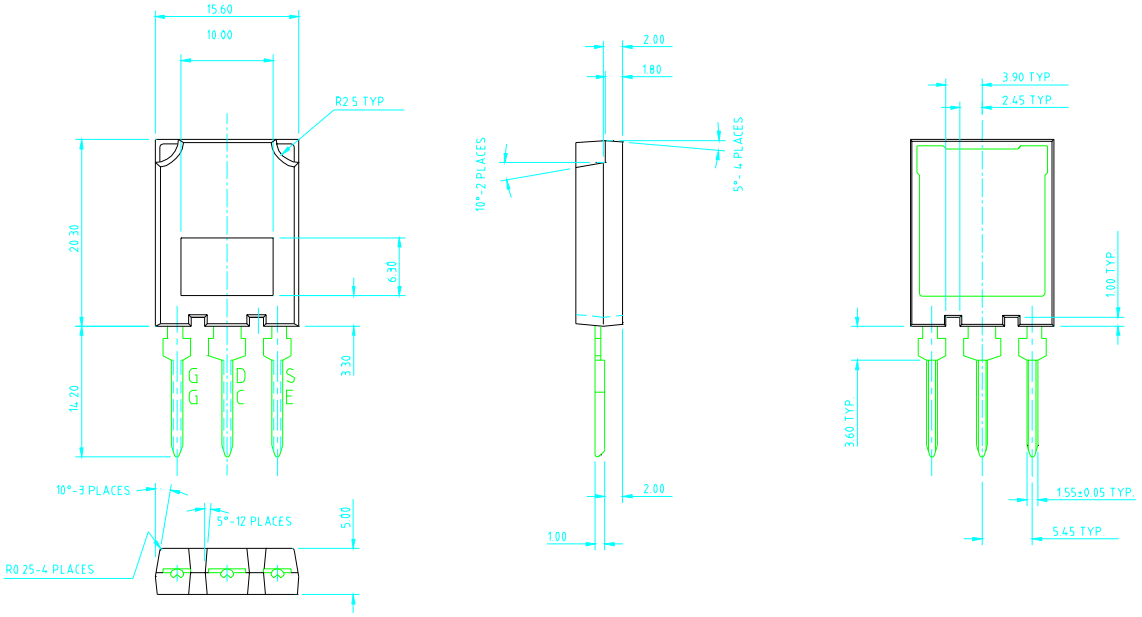
② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 5.0Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%

④ Pulse width 5.0µs, single shot

Case Outline and Dimensions — Super-247

Dimensions are shown in millimeters



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WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936

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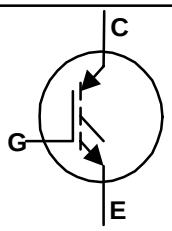
IRGPS40B120U

INSULATED GATE BIPOLAR TRANSISTOR

UltraFast IGBT

Features

- Low $V_{CE(on)}$ Non Punch Through IGBT Technology
- 10µs Short Circuit Capability
- Square RBSOA
- Positive $V_{CE(on)}$ Temperature Coefficient
- Super-247 Package



n-channel

V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 3.12V

@V_{GE} = 15V, I_C = 40A

T_J = 25°C

Benefits

- Benchmark Efficiency above 20KHz
- Rugged Transient Performance
- Low EMI
- Excellent Current Sharing in Parallel Operation



Super-247™

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	80	A
I_C @ T_C = 100°C	Continuous Collector Current	40	
I_{CM}	Pulsed Collector Current	160	
I_{LM}	Clamped Inductive Load Current	160	
E_{AS} @ T_C = 25°C	Avalanche Energy, single pulse I_C = 40 A, V_{CC} = 50V, R_{GE} = 5 Ω L = 200 µH	160	mJ
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	595	W
P_D @ T_C = 100°C	Maximum Power Dissipation	238	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	——	——	0.21	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	——	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	——	40	
Wt	Weight	——	6.0	——	g (oz)
L_E	Internal Emitter Inductance	——	13	——	nH

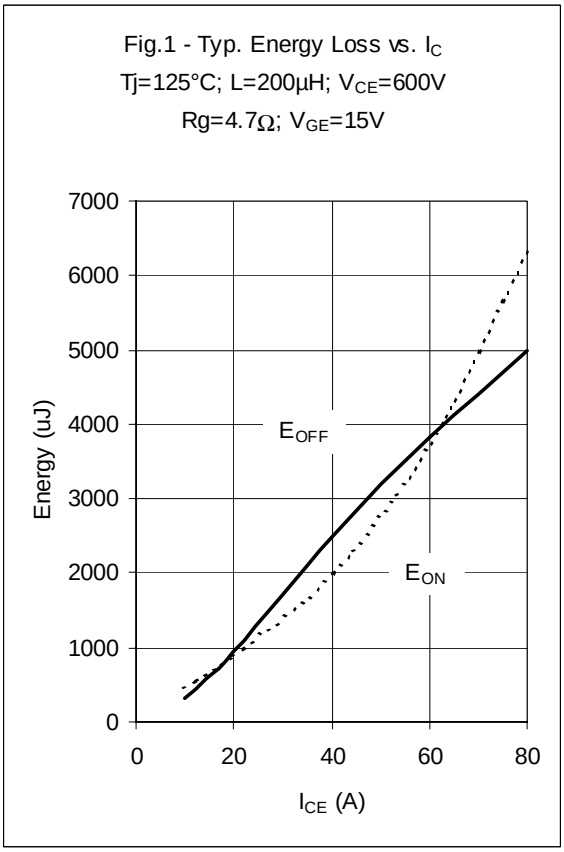
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ	Max	Units	Conditions	Ref. Fig.
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200			V	V_{GE} = 0V, I_c =500 µA	
$V_{(BR)CES}$/ Tj	Temperature Coeff. of Breakdown Voltage		0.4		V/°C	V_{GE} = 0V, I_c = 1 mA (25 -125 °C)	
VCE(on)	Collector-to-Emitter Saturation Voltage		3.12	3.50	V	IC = 40A, V_{GE} = 15V	
			3.41	3.85		I_C = 50A, V_{GE} = 15V	
			3.87	4.55		I_C =40A, V_{GE} = 15V, T_J = 125°C	
			4.26	5.10		IC = 50A, VGE = 15V, TJ = 125°C	
$V_{GE(th)}$	Gate Threshold Voltage	4.0	5.0	6.0	V	V_{CE} = V_{GE}, I_C = 250 µA	
	Temperature Coeff. of Threshold Voltage		-12		mV/°C	V_{CE} = V_{GE}, I_C = 1 mA (25 -125 °C)	
g_{fe}	Forward Transconductance		30.5		S	V_{CE} = 50V, I_C = 40A, PW =80 s	
I_{CES}	Zero Gate Voltage Collector Current		15		µA	V_{GE} = 0V, V_{CE} = 1200V	
			500			V_{GE} = 0v, V_{CE} = 1200V, T_J =125°C	
I_{GES}	Gate-to-Emitter Leakage Current			±100	nA	V_{GE} = ±20V	

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	Ref. Fig.
Q_g	Total Gate charge (turn-on)		340		nC	I_C = 40A	
Q_{ge}	Gate - Emitter Charge (turn-on)		40			V_{CC} =400V	
Q_{gc}	Gate - Collector Charge (turn-on)		165			V_{GE} = 15V	
E_{on}	Turn-On Switching Loss *		1515		µJ	I_C = 40A, V_{CC} = 600V	
E_{off}	Turn-Off Switching Loss *		1783			V_{GE} = 15V, Rg = 4.7 L=200µH, L_S=150nH	
E_{tot}	Total Switching Loss *		3300			T_J = 25°C, Energy losses include tail and diode reverse recovery	
td(on)	Turn - on delay time		76		ns	I_C = 40A, V_{CC} = 600V	
tr	Rise time		38			V_{GE} = 15V, Rg = 4.7 L=200µH, L^S =150nH	
td(off)	Turn - off delay time		292			T_J = 25°C,	
tf	Fall time		22				
E_{on}	Turn-on Switching Loss *		2273		µJ	I_C = 40A, V_{CC} = 600V	1
E_{off}	Turn-off Switching Loss *		2500			V_{GE} = 15V, Rg = 4.7 L=200µH, L^S =150nH	2
E_{tot}	Total Switching Loss *		4772			T_J = 125°C, Energy losses include tail and diode reverse recovery	3
td(on)	Turn - on delay time		76		ns	I_C = 40A, V_{CC} = 600V	
tr	Rise time		39			V_{GE} = 15V, Rg = 4.7 L=200µH, L^S =150nH	
td(off)	Turn - off delay time		332			T_J = 125°C,	
tf	Fall time		25				
C_{ies}	Input Capacitance		4400		pF	V_{GE} = 0V	
C_{oes}	Output Capacitance		420			V_{CC} = 30V	
C_{res}	Reverse Transfer Capacitance		170			f = 1.0 MHz	
RBSOA	Reverse bias safe operating area	FULL SQUARE				T_J =150°C, Ic = 160A V_{CC} = 1000V, V_P = 1200V Rg = 4.7 , V_{GE} = +15V to 0 V	
SCSOA	Short Circuit Safe Operating Area	10	----	----	µs	T_J = 150°C V_{CC} = 900V, V_P = 1200V Rg = 22 , V_{GE} = +15V to 0 V	

* Used Diode HF40D120ACE



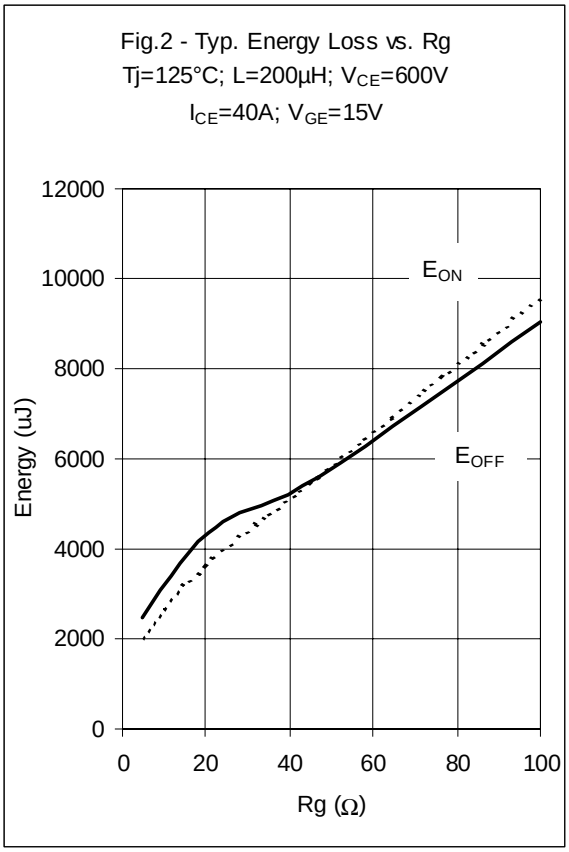
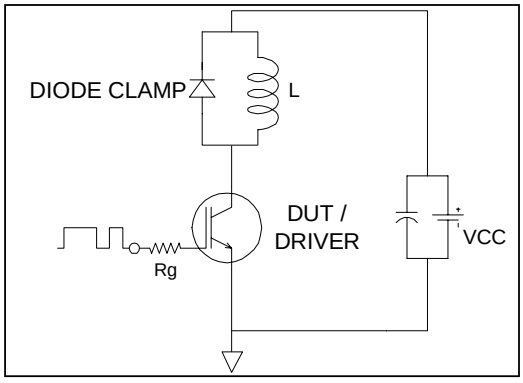
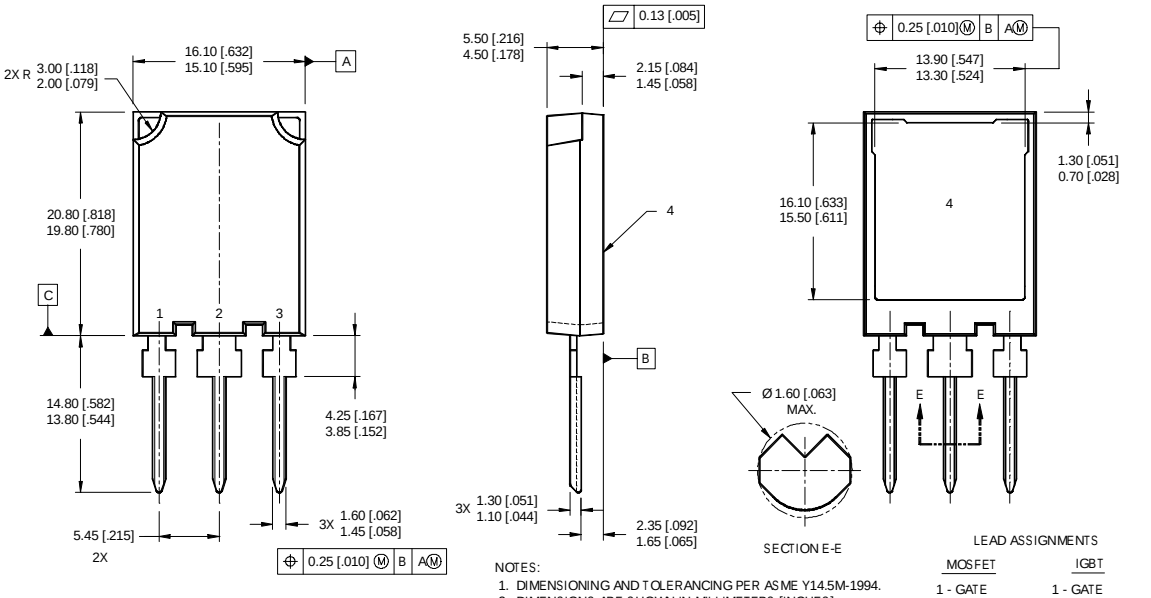


Fig.3 - Switching Loss Circuit



Super-247™ Package Outline



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. CONTROLLING DIMENSION: MILLIMETER
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-274AA

LEAD ASSIGNMENTS

MOSFET	IGBT
1 - GATE	1 - GATE
2 - DRAIN	2 - COLLECTOR
3 - SOURCE	3 - EMITTER
4 - DRAIN	4 - COLLECTOR

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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Visit us at www.irf.com for sales contact information.08/01

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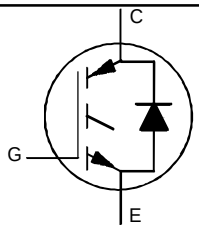
PD - 94240

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IRGPS40B120UD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

UltraFast CoPack IGBT



n-channel

V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 3.12V

@V_{GE} = 15V, I_C = 40A

T_J = 25°C

Features

- Low $V_{CE(on)}$ Non Punch Through IGBT Technology
- Low Diode V_F
- 10µs Short Circuit Capability
- Square RBSOA
- Ultrasoft Diode Reverse Recovery Characteristics
- Positive $V_{CE(on)}$ Temperature Coefficient
- Super-247 Package

Benefits

- Benchmark Efficiency above 20KHz
- Rugged Transient Performance
- Low EMI
- Excellent Current Sharing in Parallel Operation


Super-247™

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	80	A
I_C @ T_C = 100°C	Continuous Collector Current	40	
I_{CM}	Pulsed Collector Current	160	
I_{LM}	Clamped Inductive Load Current	160	
I_F @ T_C = 25°C	Diode Continuous Forward Current	80	
I_F @ T_C = 100°C	Diode Continuous Forward Current	40	
I_{FM}	Diode Maximum Forward Current	160	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	595	W
P_D @ T_C = 100°C	Maximum Power Dissipation	238	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	——	——	0.21	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	——	——	0.41	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	——	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	——	40	
Wt	Weight	——	6.0	——	g (oz)
L_E	Internal Emitter Inductance	——	13	——	nH

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IRGPS40B120UD

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ	Max	Units	Conditions	Ref. Fig.
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200			V	V_{GE} = 0V,I_c =500 µA	
$\Delta V_{(BR)CES}$ / ΔTj	Temperature Coeff. of Breakdown Voltage		0.4		V/°C	V_{GE} = 0V, I_c = 1 mA (25 -125 °C)	
VCE(on)	Collector-to-Emitter Saturation Voltage		3.12	3.50	V	IC = 40A, V_{GE} = 15V	
			3.41	3.85		I_C = 50A, V_{GE} = 15V	
			3.87	4.55		I_C =40A, V_{GE} = 15V, T_J = 125°C	
			4.26	5.10		IC = 50A, VGE = 15V, TJ = 125°C	
$V_{GE(th)}$	Gate Threshold Voltage	4.0	5.0	6.0	V	V_{CE} = V_{GE}, I_C = 250 µA	
	Temperature Coeff. of Threshold Voltage		-12		mV/°C	V_{CE} = V_{GE}, I_C = 1 mA (25 -125 °C)	
g_{fe}	Forward Transconductance		30.5		S	V_{CE} = 50V, I_C = 40A, PW =80µs	
I_{CES}	Zero Gate Voltage Collector Current		15		µA	V_{GE} = 0V,V_{CE} = 1200V	
			500			V_{GE} = 0v, V_{CE} = 1200V, T_J =125°C	
V_{FM}	Diode Forward Voltage Drop		2.03	2.40	V	I_F = 40A	
			2.19	2.60		I_F = 50A	
			2.26	2.66		I_F = 40A, TJ = 125°C	
			2.49	2.95		I_F = 50A, T_J = 125°C	
I_{GES}	Gate-to-Emitter Leakage Current			±100	nA	V_{GE} = ±20V	

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	Ref. Fig.
Q_g	Total Gate charge (turn-on)		340		nC	I_C = 40A	
Q_{ge}	Gate - Emitter Charge (turn-on)		40			V_{CC} =400V	
Q_{gc}	Gate - Collector Charge (turn-on)		165			V_{GE} = 15V	
E_{on}	Turn-On Switching Loss		1515		µJ	I_C = 40A, V_{CC} = 600V	
E_{off}	Turn-Off Switching Loss		1783			V_{GE} = 15V, Rg = 4.7Ω, L=200µH, L_S=150nH	
E_{tot}	Total Switching Loss		3300			T_J = 25°C, Energy losses include tail and diode reverse recovery	
td(on)	Turn - on delay time		76		ns	I_C = 40A, V_{CC} = 600V	
tr	Rise time		38			V_{GE} = 15V, Rg = 4.7Ω, L=200µH, L_S=150nH	
td(off)	Turn - off delay time		292			T_J = 25°C,	
tf	Fall time		22				
E_{on}	Turn-on Switching Loss		2273		µJ	I_C = 40A, V_{CC} = 600V	1
E_{off}	Turn-off Switching Loss		2500			V_{GE} = 15V, Rg = 4.7Ω, L=200µH, L_S=150nH	2
E_{tot}	Total Switching Loss		4772			T_J = 125°C, Energy losses include tail and diode reverse recovery	3
td(on)	Turn - on delay time		76		ns	I_C = 40A, V_{CC} = 600V	
tr	Rise time		39			V_{GE} = 15V, Rg = 4.7Ω, L=200µH, L_S=150nH	
td(off)	Turn - off delay time		332			T_J = 125°C,	
tf	Fall time		25				
C_{ies}	Input Capacitance		4400		pF	V_{GE} = 0V	
C_{oes}	Output Capacitance		420			V_{CC} = 30V	
C_{res}	Reverse Transfer Capacitance		170			f = 1.0 MHz	
RBSOA	Reverse bias safe operating area	FULL SQUARE				T_J =150°C, Ic = 160A V_{CC} = 1000V, V_P = 1200V Rg = 4.7Ω, V_{GE} = +15V to 0 V	
SCSOA	Short Circuit Safe Operating Area	10	----	----	µs	T_J = 150°C V_{CC} = 900V,V_P = 1200V Rg = 22Ω, V_{GE} = +15V to 0 V	
Erec	Reverse recovery energy of the diode		2800		µJ	T_J = 125°C	
trr	Diode Reverse recovery time		135		ns	V_{CC} = 600V, I_F = 40A	
Irr	Peak Reverse Recovery Current		49		A	V_{GE} = 15V, Rg = 4.7Ω, L=200µH, L_S=150nH	

Fig.1 - Typ. Energy Loss vs. I_C
Tj=125°C; L=200µH; V_{CE}=600V
Rg=4.7Ω; V_{GE}=15V

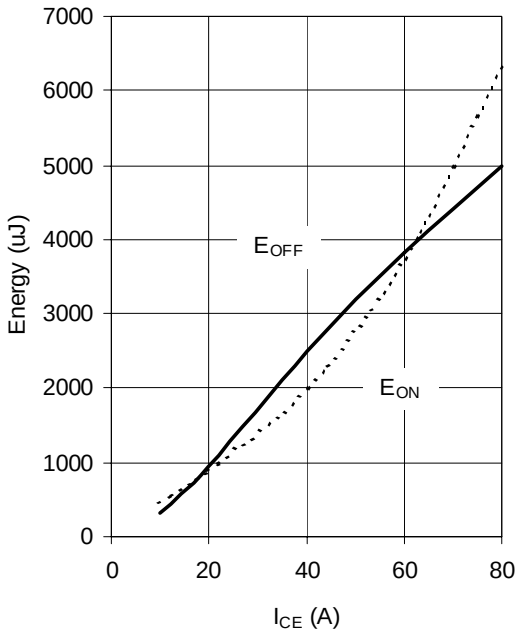


Fig.2 - Typ. Energy Loss vs. Rg
Tj=125°C; L=200µH; V_{CE}=600V
I_{CE}=40A; V_{GE}=15V

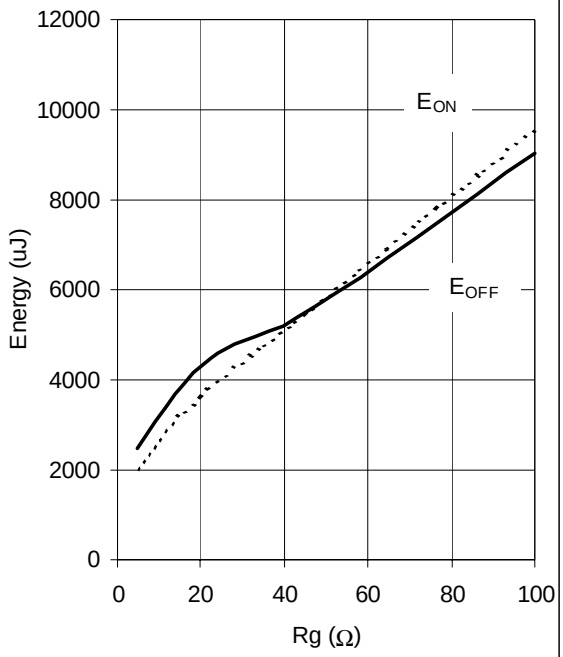
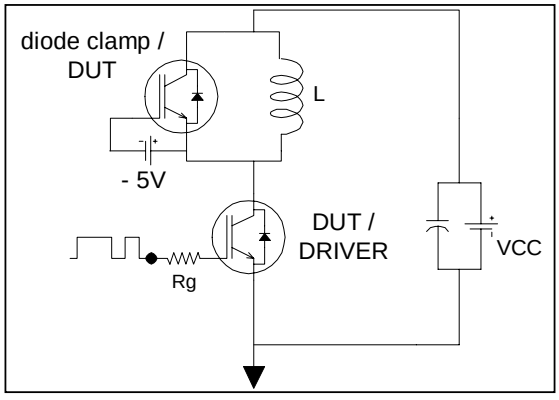


Fig.3 - Switching Loss Circuit

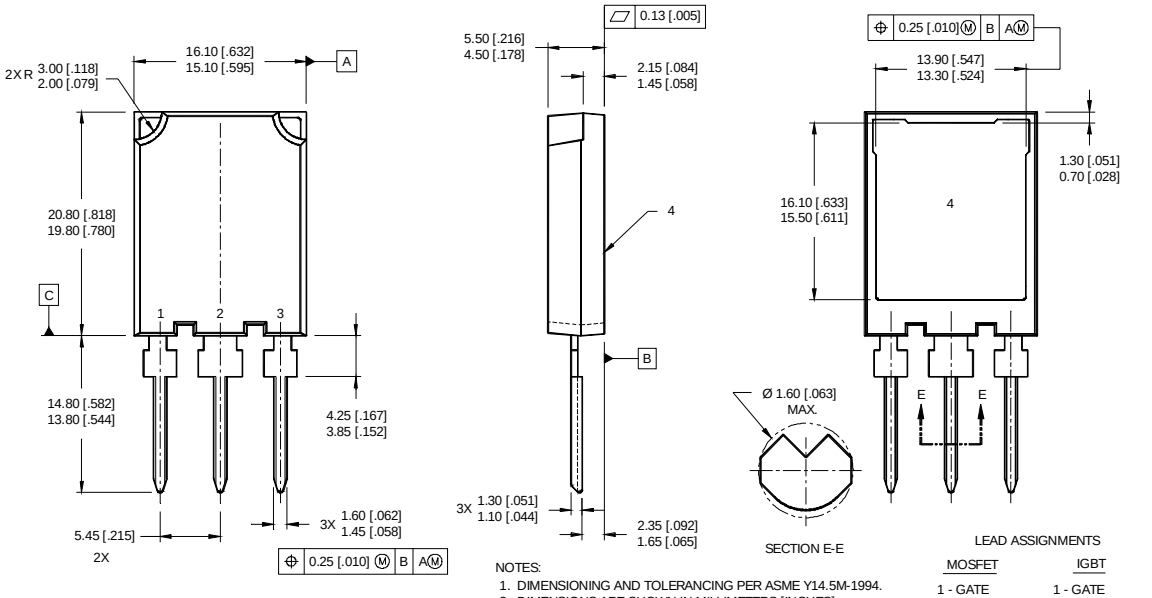


PROVISIONAL

IRGPS40B120UD

International
IOR Rectifier

Super-247™ Package Outline



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. CONTROLLING DIMENSION: MILLIMETER
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-274AA

LEAD ASSIGNMENTS

MOSFET	IGBT
1 - GATE	1 - GATE
2 - DRAIN	2 - COLLECTOR
3 - SOURCE	3 - EMITTER
4 - DRAIN	4 - COLLECTOR

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.6/01

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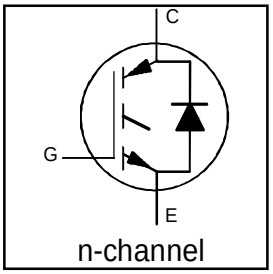
PD - 94239

International
IOR Rectifier

IRGPS60B120KD

Motor Control CoPack IGBT

INSULATED GATE BIPOLAR TRANSISTOR
WITH ULTRAFAST SOFT RECOVERY DIODE



n-channel

V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.5V

@V_{GE} = 15V, I_C = 60A

T_J = 25°C

Features

- Low $V_{CE(on)}$ Non Punch Through IGBT Technology
- Low Diode V_F
- 10µs Short Circuit Capability
- Square RBSOA
- Ultrasoft Diode Reverse Recovery Characteristics
- Positive $V_{CE(on)}$ Temperature Coefficient
- Super-247 Package

Benefits

- Benchmark Efficiency for Motor Control
- Rugged Transient Performance
- Low EMI
- Excellent Current Sharing in Parallel Operation


Super-247™

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	120	A
I_C @ T_C = 100°C	Continuous Collector Current	60	
I_{CM}	Pulsed Collector Current	240	
I_{LM}	Clamped Inductive Load Current	240	
I_F @ T_C = 25°C	Diode Continuous Forward Current	120	
I_F @ T_C = 100°C	Diode Continuous Forward Current	60	
I_{FM}	Diode Maximum Forward Current	240	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	595	W
P_D @ T_C = 100°C	Maximum Power Dissipation	238	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	——	——	0.21	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	——	——	0.41	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	——	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	——	40	
Wt	Weight	——	6.0	——	g (oz)
L_E	Internal Emitter Inductance	——	13	——	nH

PROVISIONAL

IRGPS60B120KD

International
IOR Rectifier

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ	Max	Units	Conditions	Ref. Fig.
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200			V	V_{GE} = 0V, I_c =500 µA	
$\Delta V_{(BR)CES}$ / ΔTj	Temperature Coeff. of Breakdown Voltage		0.4		V/°C	V_{GE} = 0V, I_c = 1 mA (25 -125 °C)	
VCE(on)	Collector-to-Emitter Saturation Voltage		2.33		V	IC = 50A, V_{GE} = 15V	
			2.50	2.75		I_C = 60A, V_{GE} = 15V	
			2.79			I_C =50A, V_{GE} = 15V, T_J = 125°C	
			3.04	3.50		IC = 60A, VGE = 15V, TJ = 125°C	
$V_{GE(th)}$	Gate Threshold Voltage	4.0	5.0	6.0	V	V_{CE} = V_{GE}, I_C = 250 µA	
	Temperature Coeff. of Threshold Voltage		-12		mV/°C	V_{CE} = V_{GE}, I_C = 1 mA (25 -125 °C)	
g_{fe}	Forward Transconductance		34.4		S	V_{CE} = 50V, I_C = 60A, PW =80µs	
I_{CES}	Zero Gate Voltage Collector Current		20		µA	V_{GE} = 0V, V_{CE} = 1200V	
			650			V_{GE} = 0v, V_{CE} = 1200V, T_J =125°C	
V_{FM}	Diode Forward Voltage Drop		1.82		V	I_F = 50A	
			1.93	2.30		I_F = 60A	
			1.96			I_F = 50A, TJ = 125°C	
			2.13	2.50		I_F = 60A, T_J = 125°C	
I_{GES}	Gate-to-Emitter Leakage Current			±100	nA	V_{GE} = ±20V	

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	Ref. Fig.
Q_g	Total Gate charge (turn-on)		340		nC	I_C = 60A	
Q_{ge}	Gate - Emitter Charge (turn-on)		40			V_{CC} =400V	
Q_{gc}	Gate - Collector Charge (turn-on)		165			V_{GE} = 15V	
E_{on}	Turn-On Switching Loss		3214		µJ	I_C = 60A, V_{CC} = 600V	
E_{off}	Turn-Off Switching Loss		4783			V_{GE} = 15V, Rg = 4.7Ω, L=200µH, L_S=150nH	
E_{tot}	Total Switching Loss		8000			T_J = 25°C, Energy losses include tail and diode reverse recovery	
td(on)	Turn - on delay time		76		ns	I_C = 60A, V_{CC} = 600V	
tr	Rise time		46			V_{GE} = 15V, Rg = 4.7Ω, L=200µH, L_S=150nH	
td(off)	Turn - off delay time		320			T_J = 25°C,	
tf	Fall time		37				
E_{on}	Turn-on Switching Loss		5032		µJ	I_C = 60A, V_{CC} = 600V	1
E_{off}	Turn-off Switching Loss		7457			V_{GE} = 15V, Rg = 4.7Ω, L=200µH, L_S=150nH	2
E_{tot}	Total Switching Loss		12500			T_J = 125°C, Energy losses include tail and diode reverse recovery	3
td(on)	Turn - on delay time		80		ns	I_C = 15A, V_{CC} = 600V	
tr	Rise time		48			V_{GE} = 15V, Rg = 4.7Ω, L=200µH, L_S=150nH	
td(off)	Turn - off delay time		340			T_J = 125°C,	
tf	Fall time		47				
C_{ies}	Input Capacitance		4400		pF	V_{GE} = 0V	
C_{oes}	Output Capacitance		420			V_{CC} = 30V	
C_{res}	Reverse Transfer Capacitance		170			f = 1.0 MHz	
RBSOA	Reverse bias safe operating area	FULL SQUARE				T_J =150°C, Ic = 240A V_{CC} = 1000V, V_P = 1200V Rg = 4.7Ω, V_{GE} = +15V to 0 V	
SCSOA	Short Circuit Safe Operating Area	10	----	----	µs	T_J = 150°C V_{CC} = 900V, V_P = 1200V Rg = 22Ω, V_{GE} = +15V to 0 V	
Erec	Reverse recovery energy of the diode		3780		µJ	T_J = 125°C	
trr	Diode Reverse recovery time		165		ns	V_{CC} = 600V, I_F = 60A	
Irr	Peak Reverse Recovery Current		51		A	V_{GE} = 15V, Rg = 4.7Ω, L=200µH, L_S=150nH	

Fig.1 - Typ. Energy Loss vs. I_C
Tj=125°C; L=200µH; V_{CE}=600V
Rg=4.7Ω; V_{GE}=15V

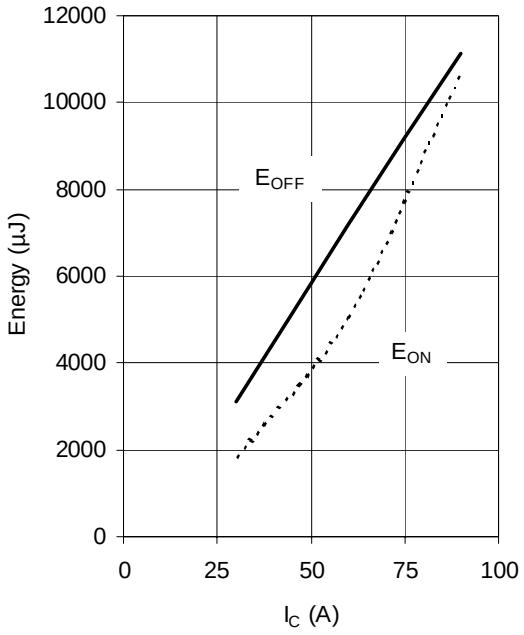


Fig.2 - Typ. Energy Loss vs. Rg
Tj=125°C; L=200µH; V_{CE}=600V
I_{CE}=60A; V_{GE}=15V

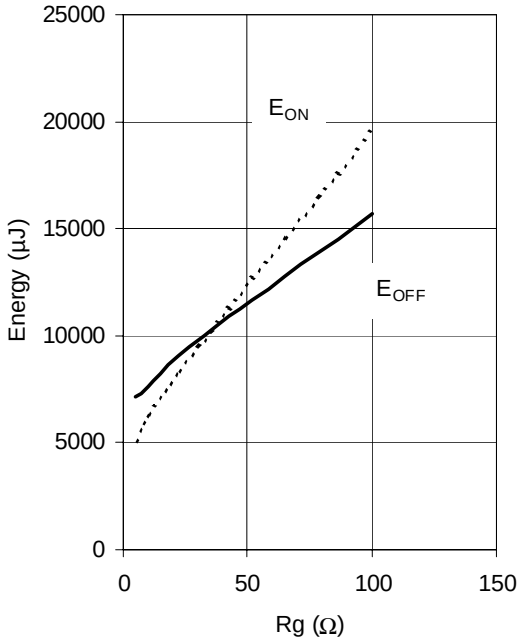
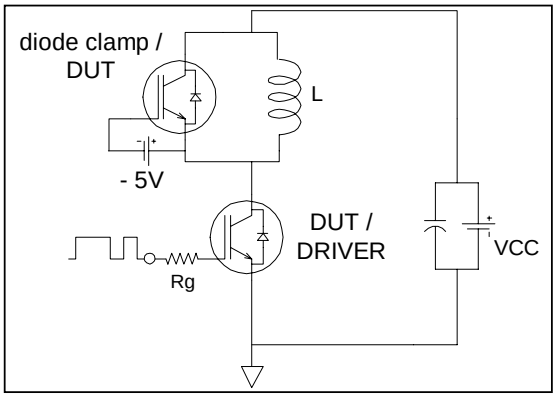


Fig.3 - Switching Loss Circuit

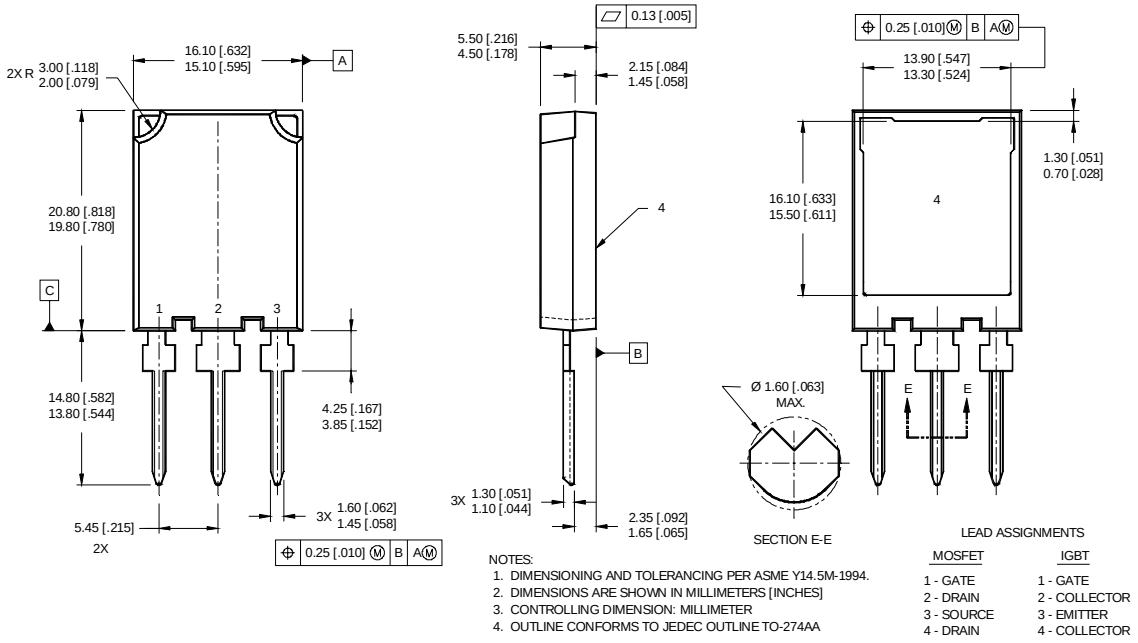


PROVISIONAL

IRGPS60B120KD

International
IOR Rectifier

Super-247™ Package Outline



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. CONTROLLING DIMENSION: MILLIMETER
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-274AA

LEAD ASSIGNMENTS

MOSFET	IGBT
1 - GATE	1 - GATE
2 - DRAIN	2 - COLLECTOR
3 - SOURCE	3 - EMITTER
4 - DRAIN	4 - COLLECTOR

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
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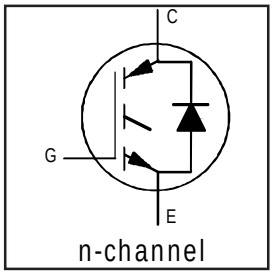
PD- 91751A

International
IOR Rectifier

IRG4IBC30FD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Fast CoPack IGBT



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.59V

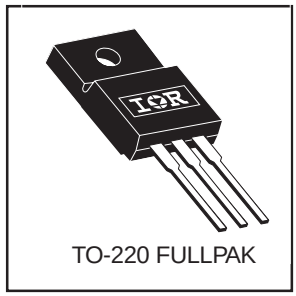
@V_{GE} = 15V, I_C = 17A

Features

- Very Low 1.59V votage drop
- 2.5kV, 60s insulation voltage ⑤
- 4.8 mm creapage distance to heatsink
- Fast: Optimized for medium operating frequencies (1-5 kHz in hard switching, >20 kHz in resonant mode).
- IGBT co-packaged with HEXFRED™ ultrafast, ultrasoft recovery antiparallel diodes
- Tighter parameter distribution
- Industry standard Isolated TO-220 Fullpak™ outline

Benefits

- Simplified assembly
- Highest efficiency and power density
- HEXFRED™ antiparallel Diode minimizes switching losses and EMI



TO-220 FULLPAK

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	20.3	A
I_C @ T_C = 100°C	Continuous Collector Current	11	
I_{CM}	Pulsed Collector Current ①	120	
I_{LM}	Clamped Inductive Load Current ②	120	
I_F @ T_C = 100°C	Diode Continuous Forward Current	8.5	
I_{FM}	Diode Maximum Forward Current	120	
Visol	RMS Isolation Voltage, Terminal to Case⑤	2500	V
V_{GE}	Gate-to-Emitter Voltage	± 20	
P_D @ T_C = 25°C	Maximum Power Dissipation	45	W
P_D @ T_C = 100°C	Maximum Power Dissipation	18	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	2.8	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	4.1	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	65	
Wt	Weight	2.0 (0.07)	—	g (oz)

3/26/99

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.69	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.59	1.8	V	I_C = 17A V_{GE} = 15V
		—	1.99	—		I_C = 31A See Fig. 2, 5
		—	1.70	—		I_C = 17A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	6.1	10	—	S	V_{CE} = 100V, I_C = 17A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 12A See Fig. 13
		—	1.3	1.6		I_C = 12A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	51	77		I_C = 17A
Qge	Gate - Emitter Charge (turn-on)	—	7.9	12	nC	V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	19	28		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	42	—		T_J = 25°C
t_r	Rise Time	—	26	—	ns	I_C = 17A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	230	350		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	160	230		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	0.63	—		diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	1.39	—	mJ	See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	—	2.02	3.9		
$t_{d(on)}$	Turn-On Delay Time	—	42	—		T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	—	27	—	ns	I_C = 17A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	310	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	310	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	3.2	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1100	—		V_{GE} = 0V
C_{oes}	Output Capacitance	—	74	—	pF	V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	14	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	42	60	ns	T_J = 25°C See Fig.
		—	80	120		T_J = 125°C 14 I_F = 12A
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	6.0	A	T_J = 25°C See Fig.
		—	5.6	10		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	80	180	nC	T_J = 25°C See Fig.
		—	220	600		T_J = 125°C 16 di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	180	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	120	—		T_J = 125°C 17

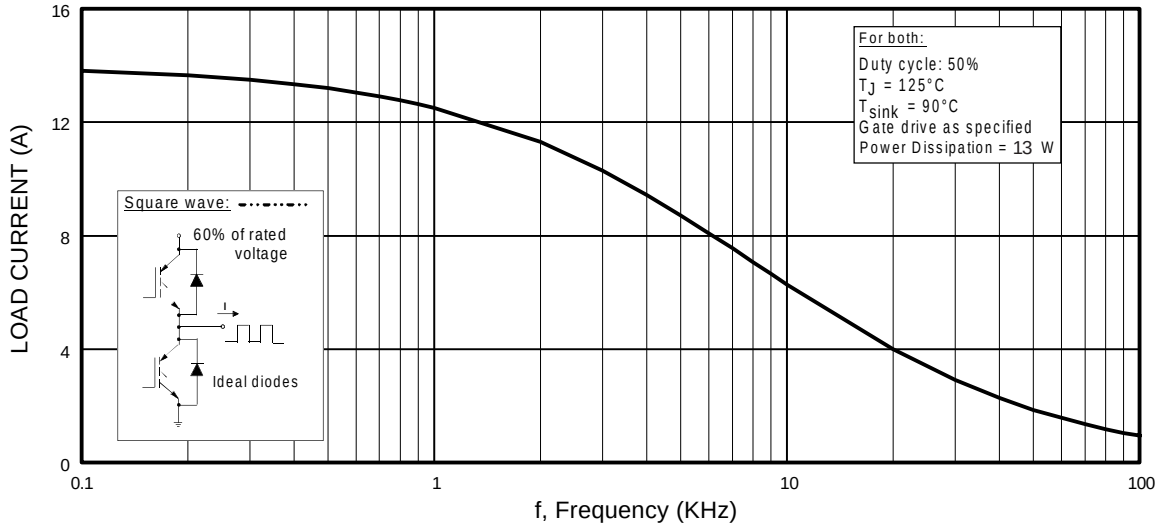


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

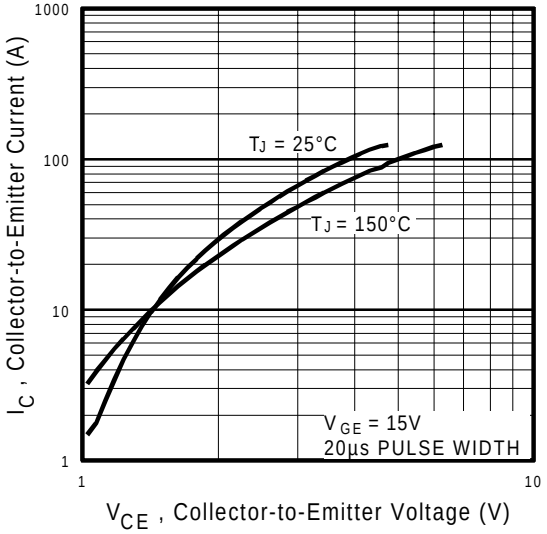


Fig. 2 - Typical Output Characteristics

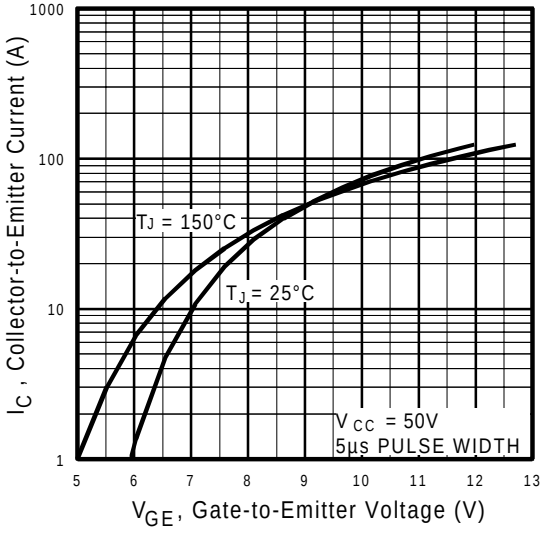


Fig. 3 - Typical Transfer Characteristics

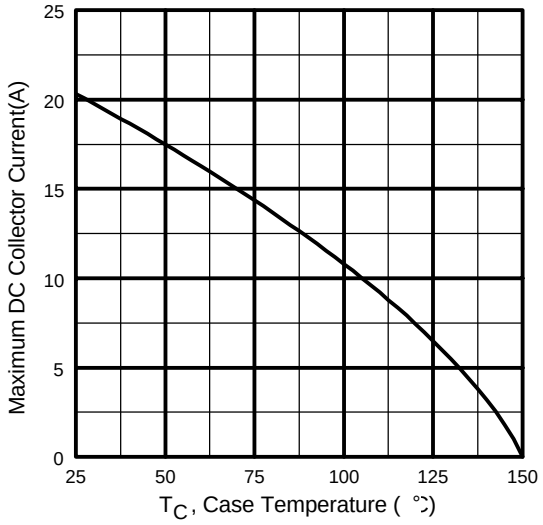


Fig. 4 - Maximum Collector Current vs. Case Temperature

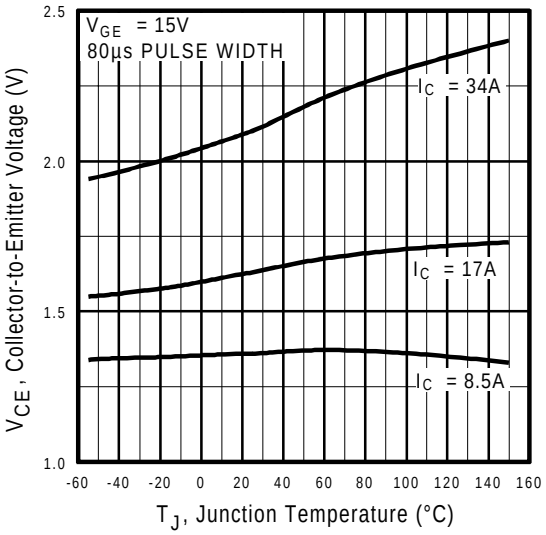


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

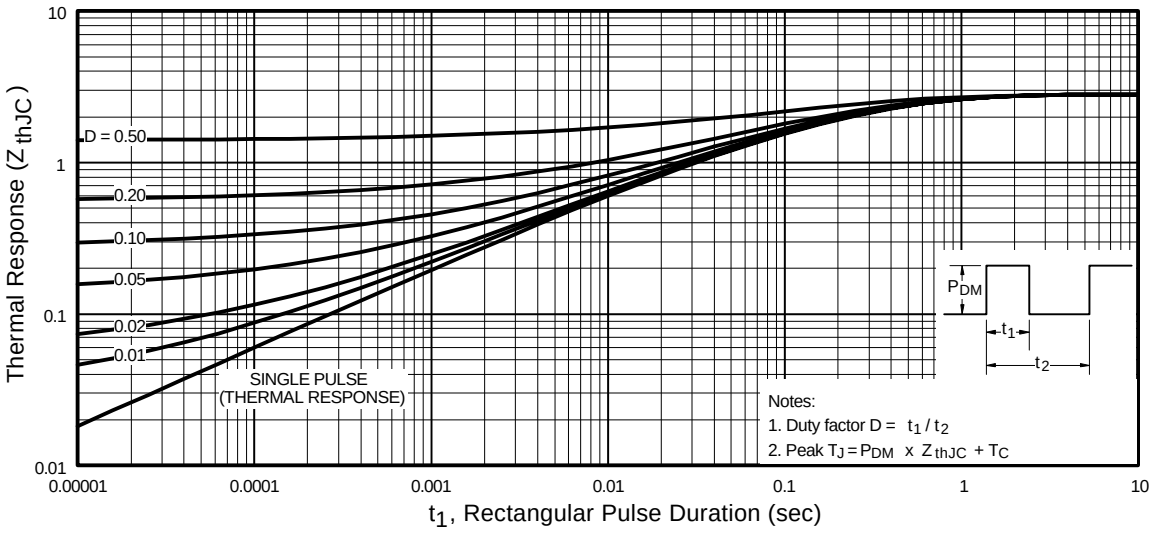


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

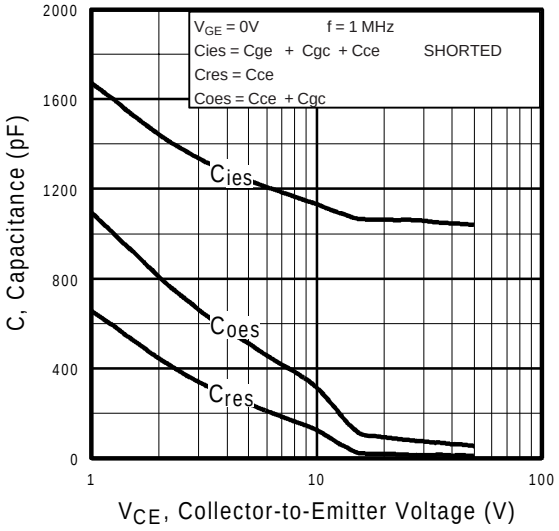


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

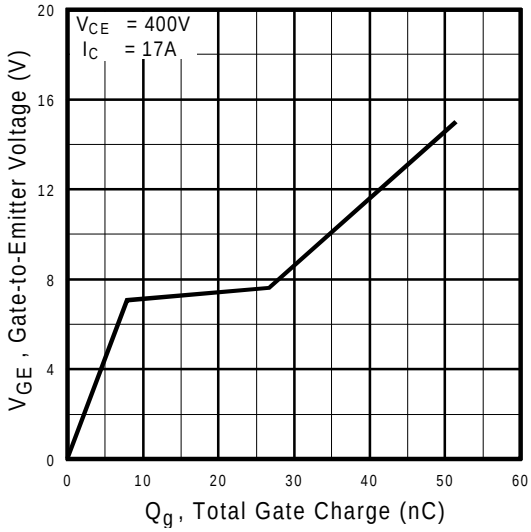


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

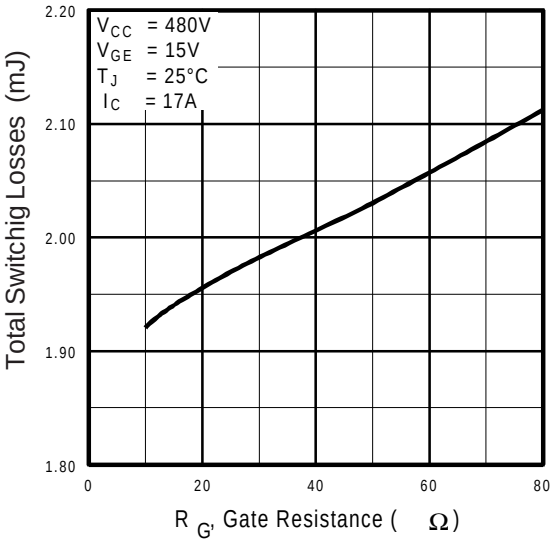


Fig. 9 - Typical Switching Losses vs. Gate Resistance

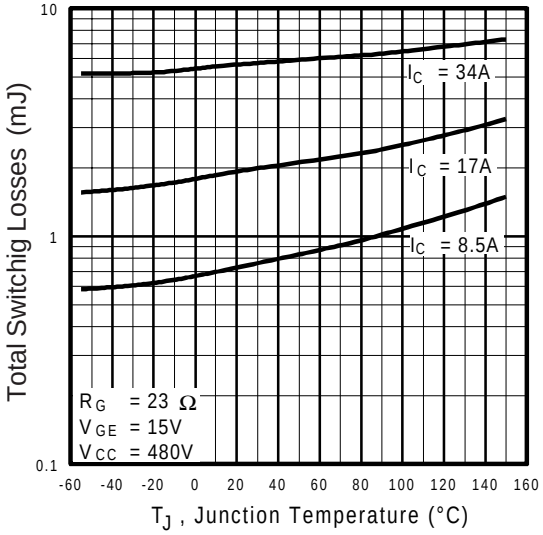


Fig. 10 - Typical Switching Losses vs. Junction Temperature

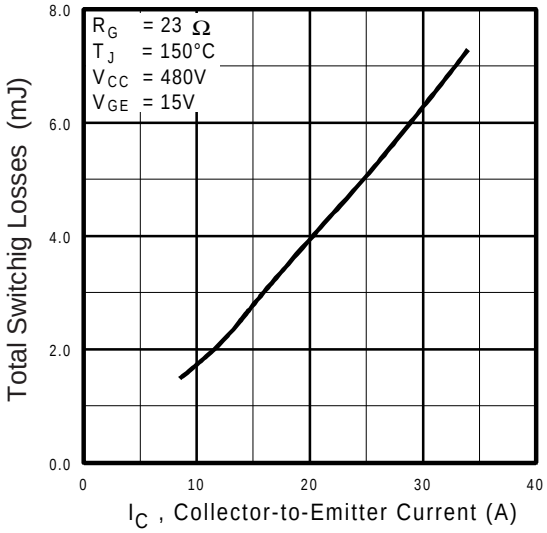


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

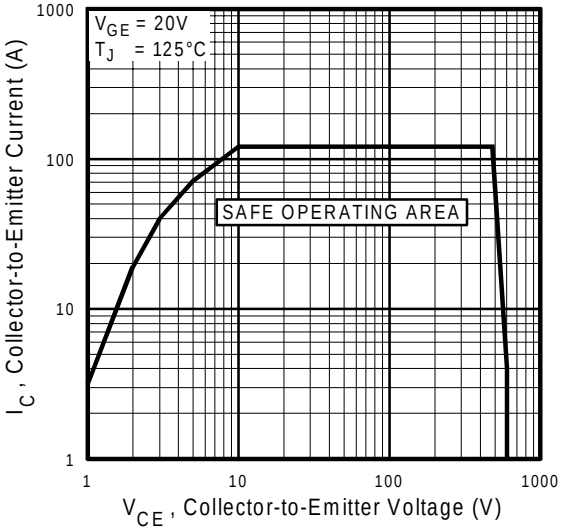


Fig. 12 - Turn-Off SOA

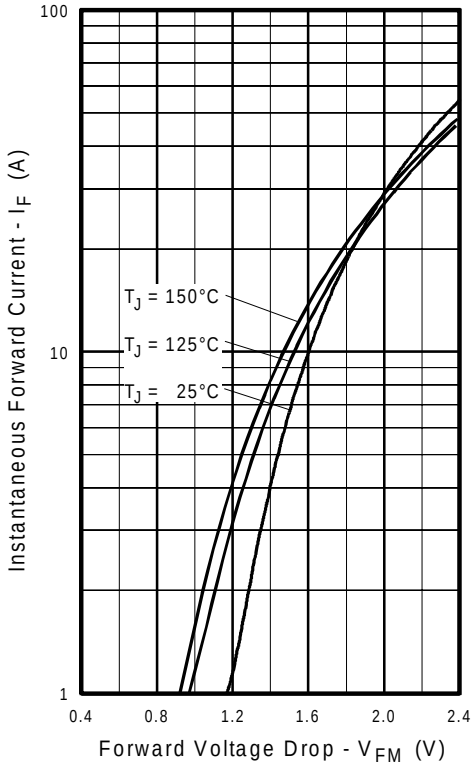


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

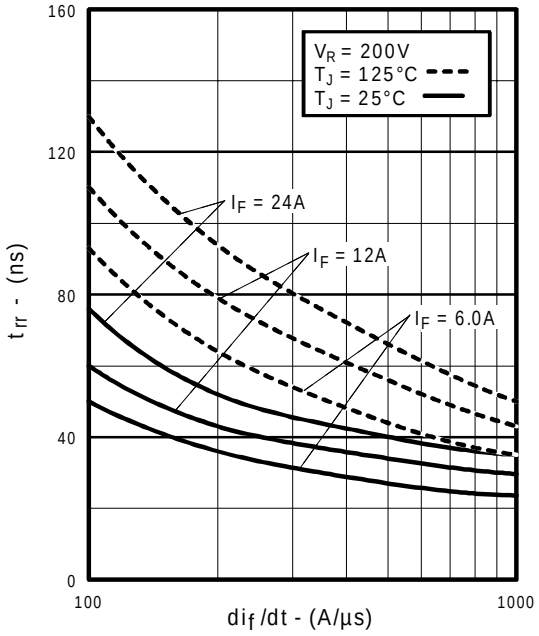


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

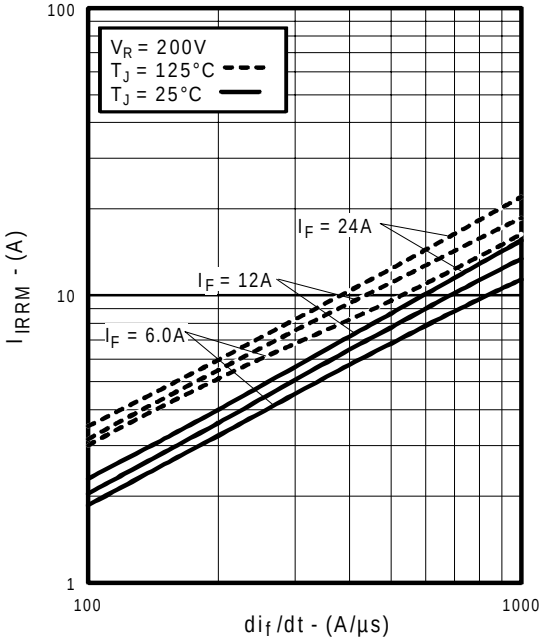


Fig. 15 - Typical Recovery Current vs. di_f/dt

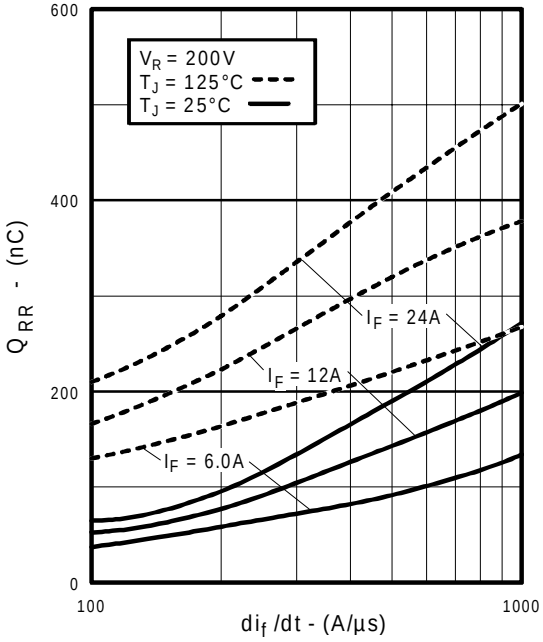


Fig. 16 - Typical Stored Charge vs. di_f/dt

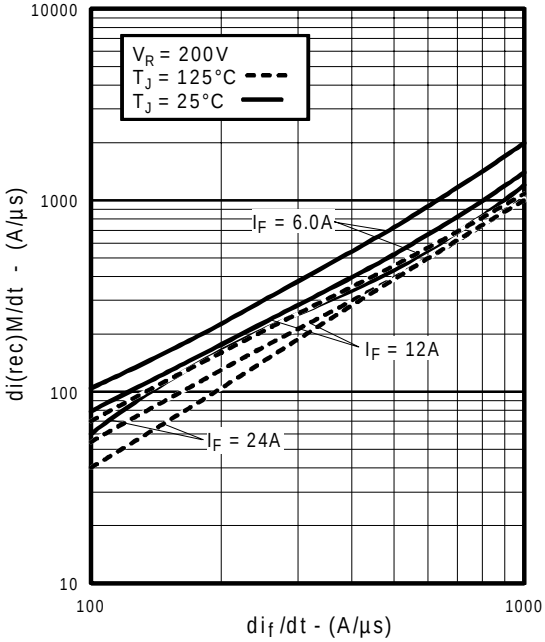


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

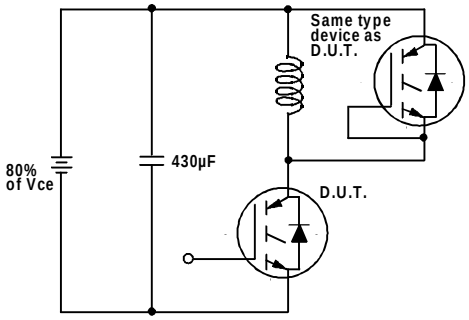


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

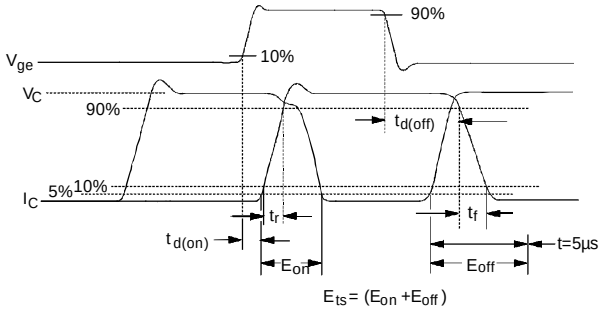


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

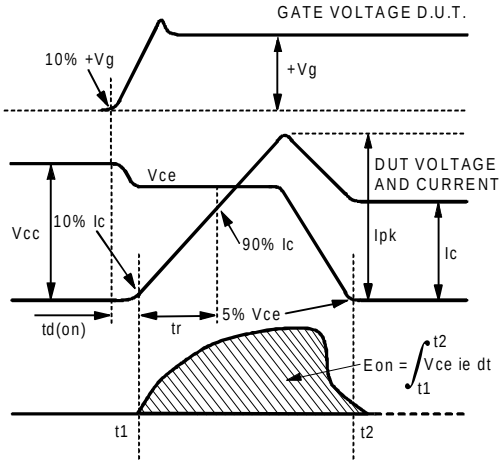


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

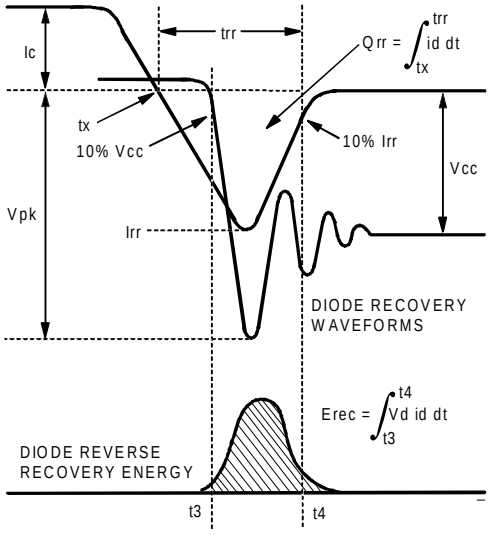


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

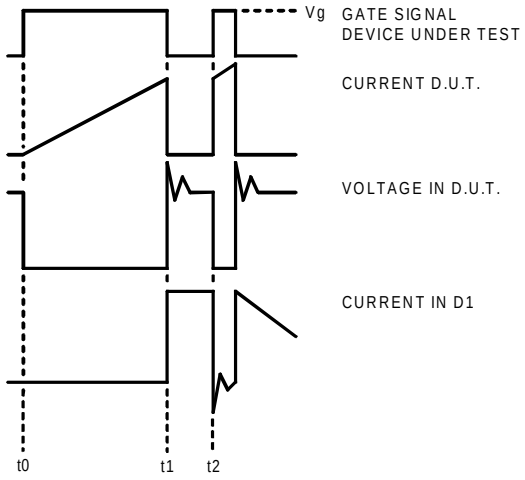


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

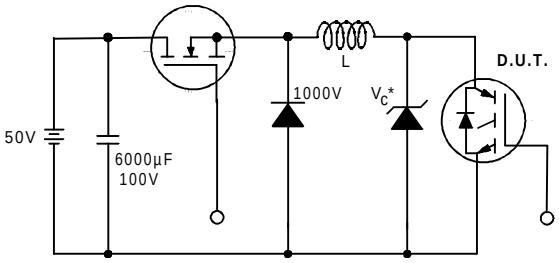


Figure 19. Clamped Inductive Load Test Circuit

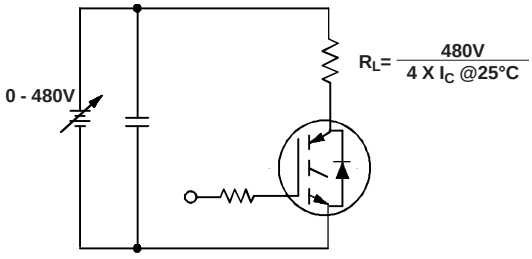


Figure 20. Pulsed Collector Current Test Circuit

Notes:

① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

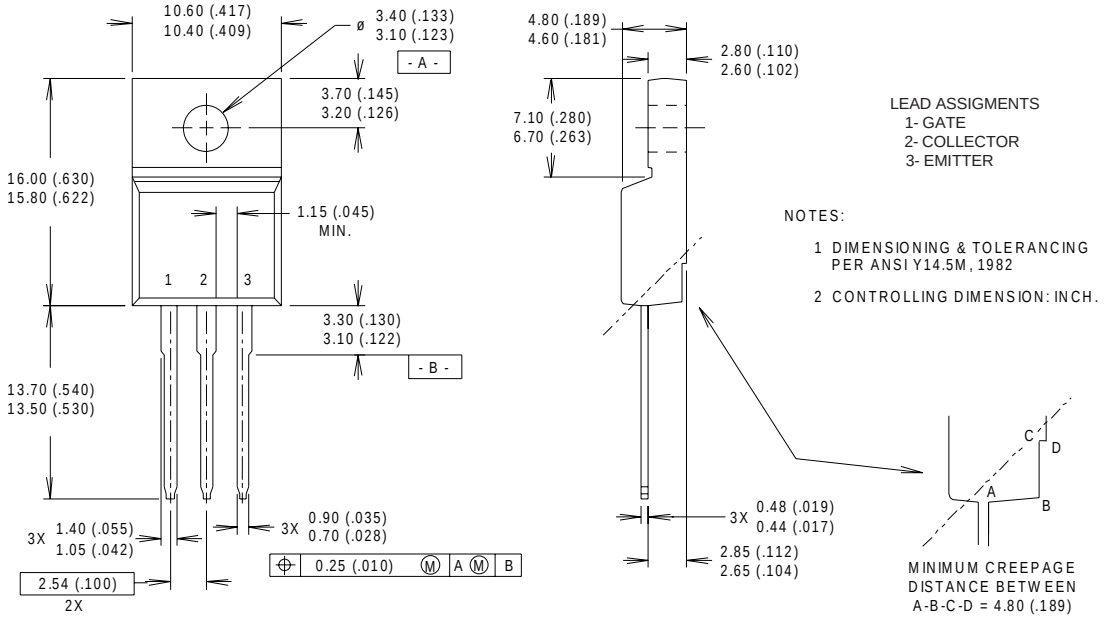
② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 23Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

⑤ t = 60s, f = 60Hz

Case Outline — TO-220 FULLPAK



International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936
http://www.irf.com/ Data and specifications subject to change without notice. 3/99

PD - 91731A

International
IOR Rectifier

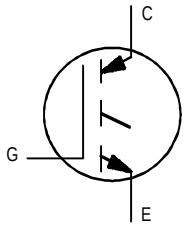
IRG4RC20F

INSULATED GATE BIPOLAR TRANSISTOR

Fast Speed IGBT

Features

- Fast: Optimized for medium operating frequencies (1-5 kHz in hard switching, >20 kHz in resonant mode).
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than previous generation IGBTs.
- Industry standard TO-252AA package
- Combines very low $V_{CE(on)}$ with low switching losses



N-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.82V

@V_{GE} = 15V, I_C = 12A

Benefits

- Generation 4 IGBTs offer highest efficiency
- Optimized for specific application conditions
- High power density and current rating



D-Pak
TO-252AA

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	22	A
I_C @ T_C = 100°C	Continuous Collector Current	12	
I_{CM}	Pulsed Collector Current ①	44	
I_{LM}	Clamped Inductive Load Current ②	44	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	5.0	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	66	W
P_D @ T_C = 100°C	Maximum Power Dissipation	26	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.9	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
Wt	Weight	0.3 (0.01)	—	g (oz)

* When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.72	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.82	2.1	V	I_C = 12A V_{GE} = 15V
		—	2.42	—		I_C = 22A See Fig.2, 5
		—	2.04	—		I_C = 12A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	5.2	7.75	—	S	V_{CE} = 100V, I_C = 12A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	27	40	nC	I_C = 12A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	4.8	6.8		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	11.4	17		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	26	—	ns	
t_r	Rise Time	—	24	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	194	290		I_C = 12A, V_{CC} = 480V
t_f	Fall Time	—	226	340		V_{GE} = 15V, R_G = 50Ω
E_{on}	Turn-On Switching Loss	—	0.19	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.92	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	1.11	1.4		
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	T_J = 150°C,
t_r	Rise Time	—	26	—		I_C = 12A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	263	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	443	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.89	—	mJ	See Fig. 11, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	540	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	37	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	7.0	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 50Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

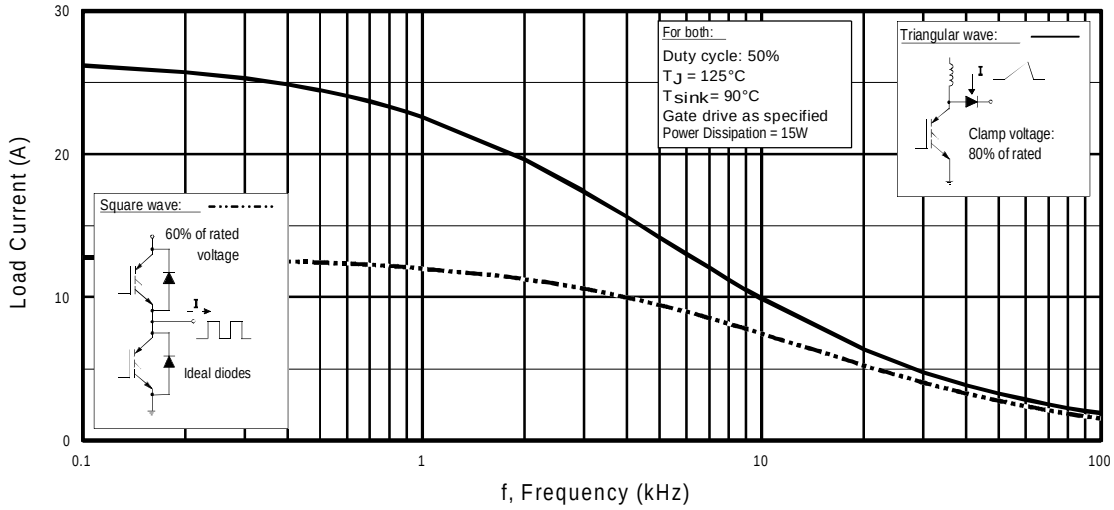


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

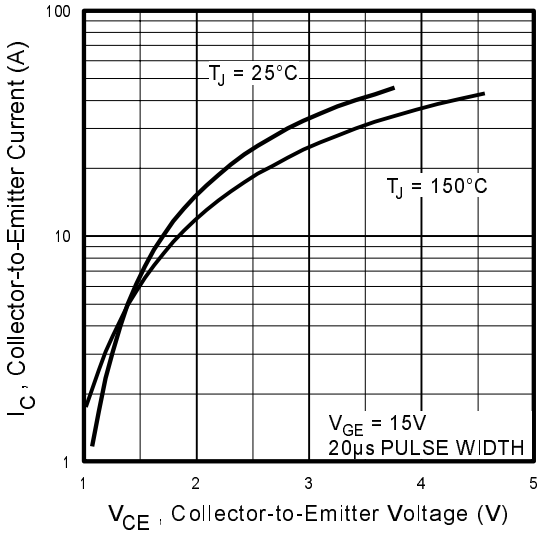


Fig. 2 - Typical Output Characteristics

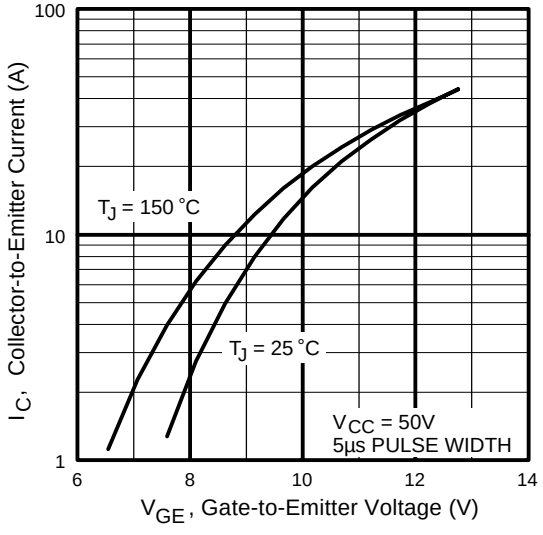


Fig. 3 - Typical Transfer Characteristics

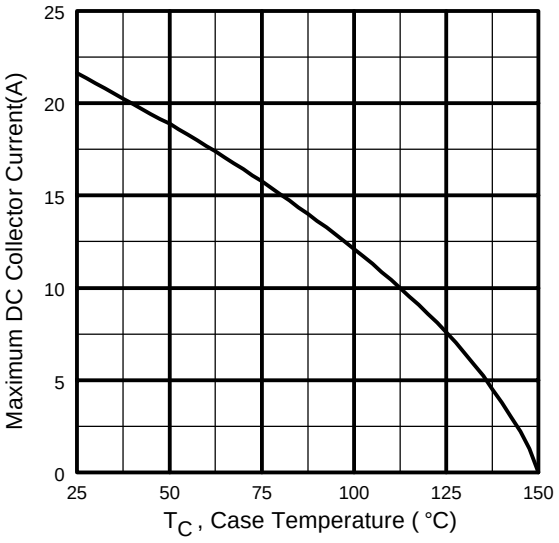


Fig. 4 - Maximum Collector Current vs. Case Temperature

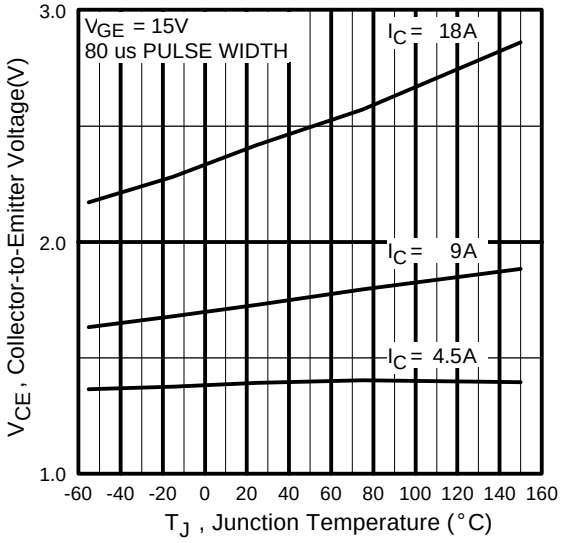


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

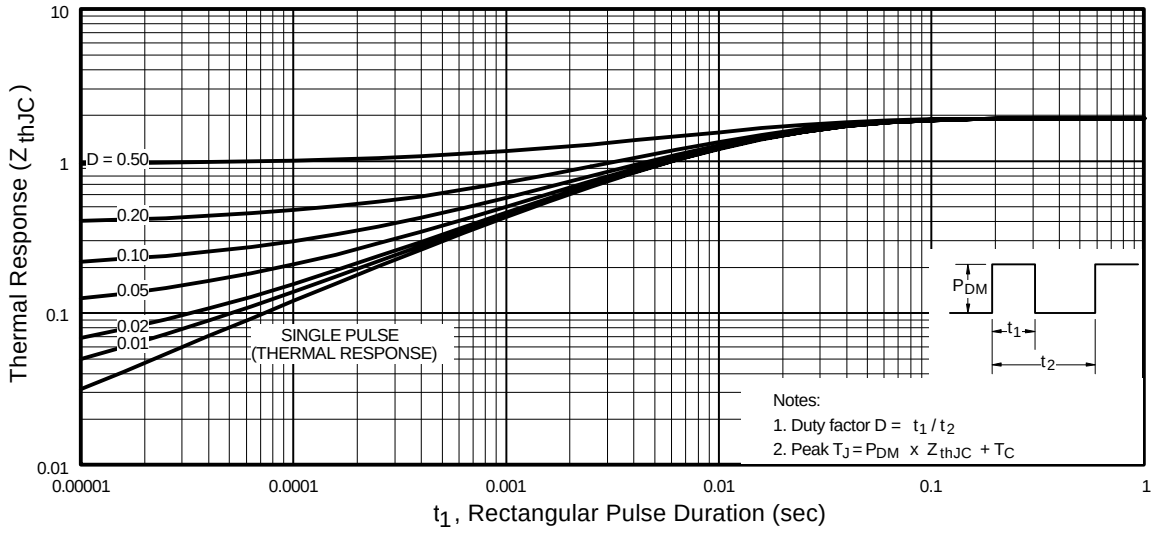


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

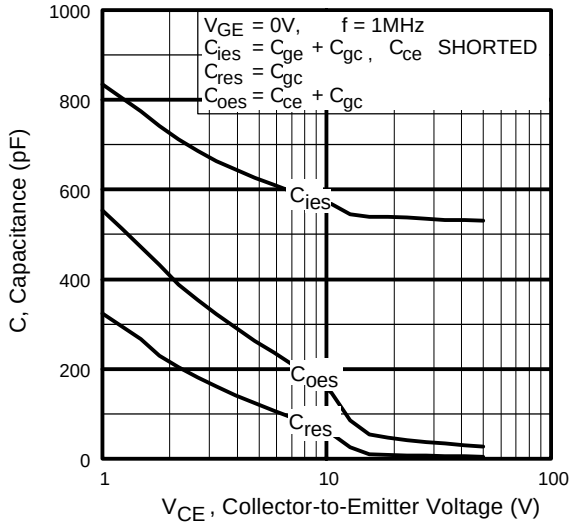


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

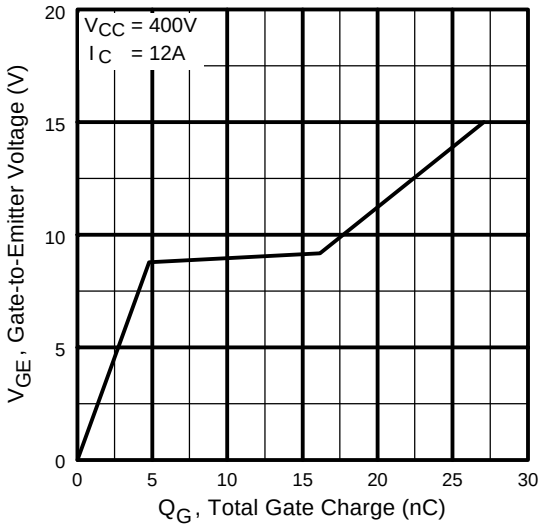


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

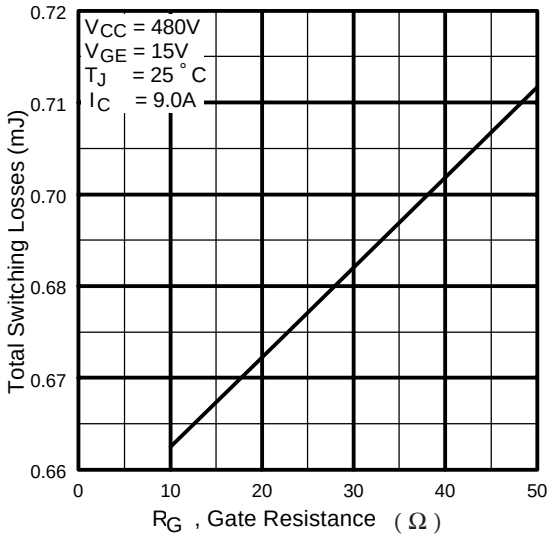


Fig. 9 - Typical Switching Losses vs. Gate Resistance

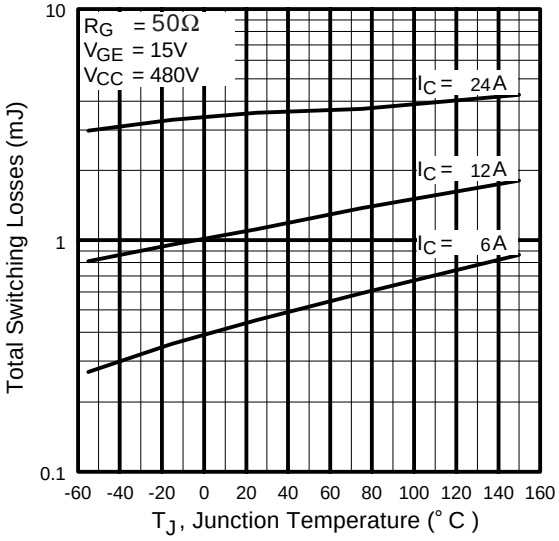


Fig. 10 - Typical Switching Losses vs. Junction Temperature

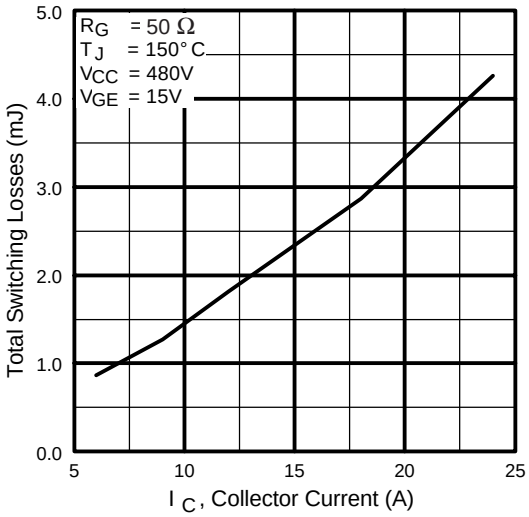


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

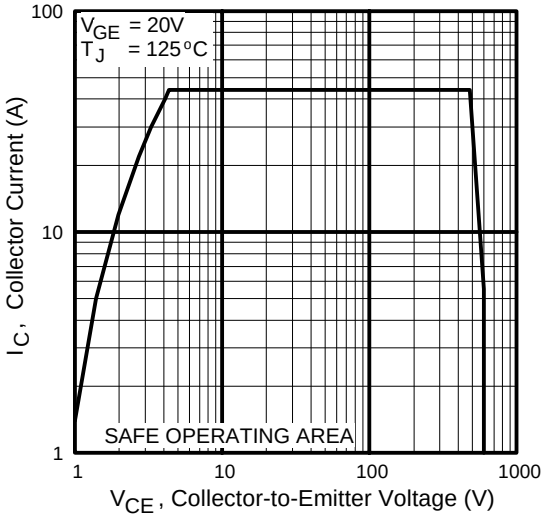


Fig. 12 - Turn-Off SOA

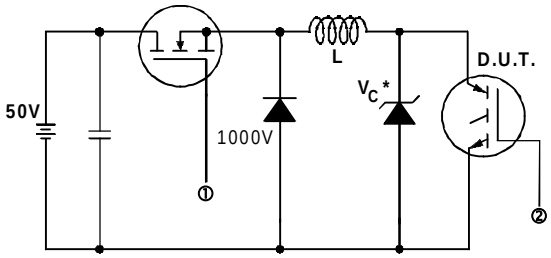


Fig. 13a - Clamped Inductive Load Test Circuit

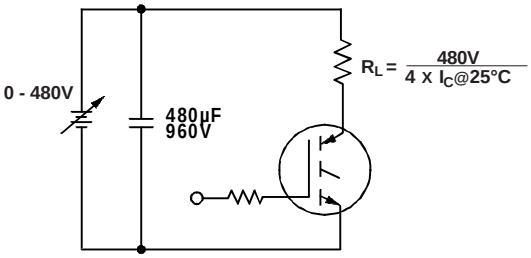


Fig. 13b - Pulsed Collector Current Test Circuit

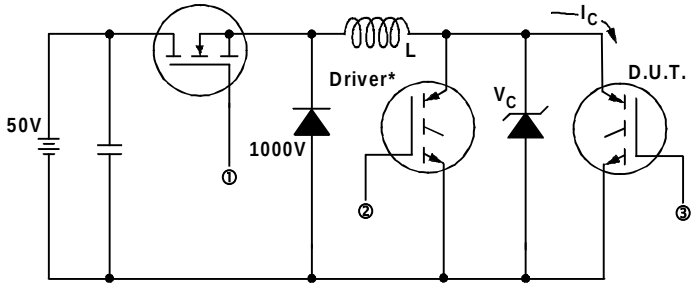


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

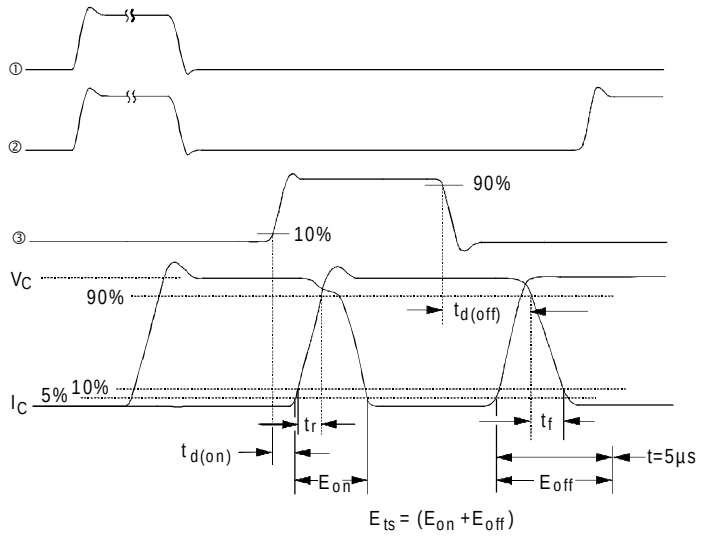
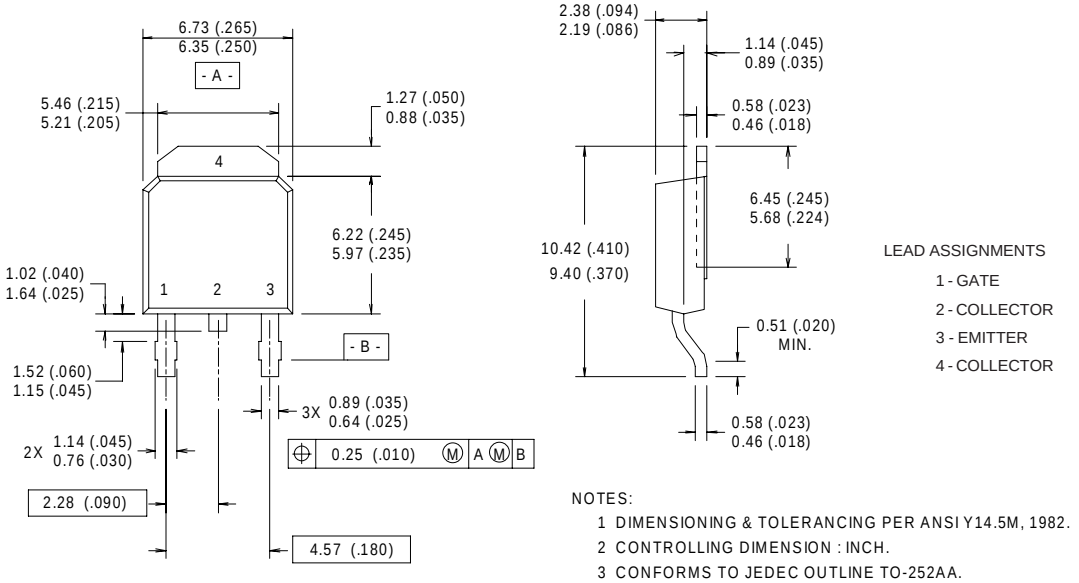


Fig. 14b - Switching Loss Waveforms

D-Pak (TO-252AA) Package Outline

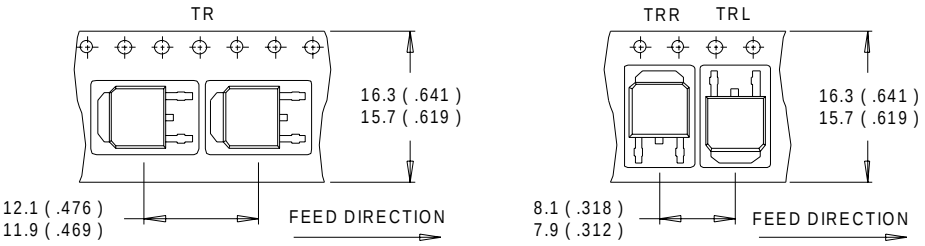
Dimensions are shown in millimeters (inches)



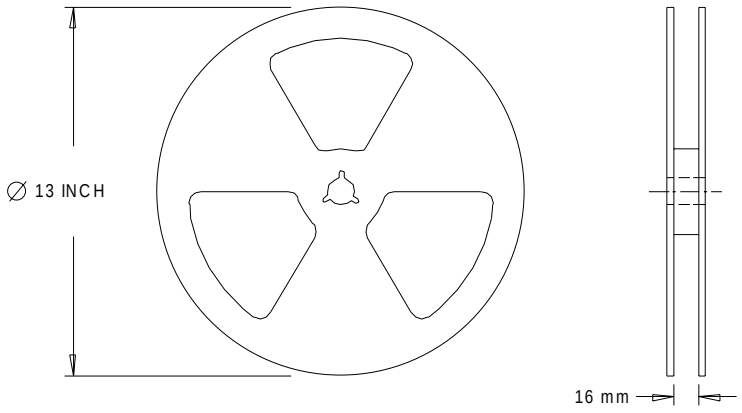
LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

D-Pak (TO-252AA) Tape & Reel Information



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information. 2/01

PD - 91452E

International
IOR Rectifier

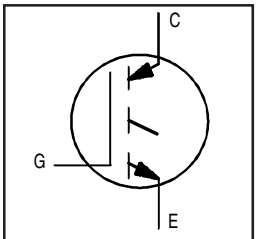
IRG4BC30U

INSULATED GATE BIPOLAR TRANSISTOR

UltraFast Speed IGBT

Features

- UltraFast: optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-220AB package



n-channel

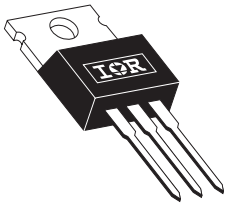
$V_{CES} = 600V$

$V_{CE(on)\ typ.} = 1.95V$

$@V_{GE} = 15V, I_C = 12A$

Benefits

- Generation 4 IGBTs offer highest efficiency available
- IGBTs optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	23	A
I_C @ T_C = 100°C	Continuous Collector Current	12	
I_{CM}	Pulsed Collector Current ①	92	
I_{LM}	Clamped Inductive Load Current ②	92	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	10	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	80	
Wt	Weight	2 (0.07)	—	g (oz)

4/17/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.63	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.95	2.1	V	I_C = 12A V_{GE} = 15V
		—	2.52	—		I_C = 23A See Fig.2, 5
		—	2.09	—		I_C = 12A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-13	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	3.1	8.6	—	S	V_{CE} = 100V, I_C = 12A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	50	75	nC	I_C = 12A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	8.1	12		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	18	27		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	
t_r	Rise Time	—	9.6	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	78	120		I_C = 12A, V_{CC} = 480V
t_f	Fall Time	—	97	150		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.16	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.20	—		See Fig. 10, 11, 13, 14
E_{ts}	Total Switching Loss	—	0.36	0.50		
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	T_J = 150°C,
t_r	Rise Time	—	13	—		I_C = 12A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	180	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	140	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.73	—	mJ	See Fig. 13, 14
L_E	Internal Source Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1100	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	73	—		V_{CC} = 30V See Fig.7
C_{res}	Reverse Transfer Capacitance	—	14	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 23Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

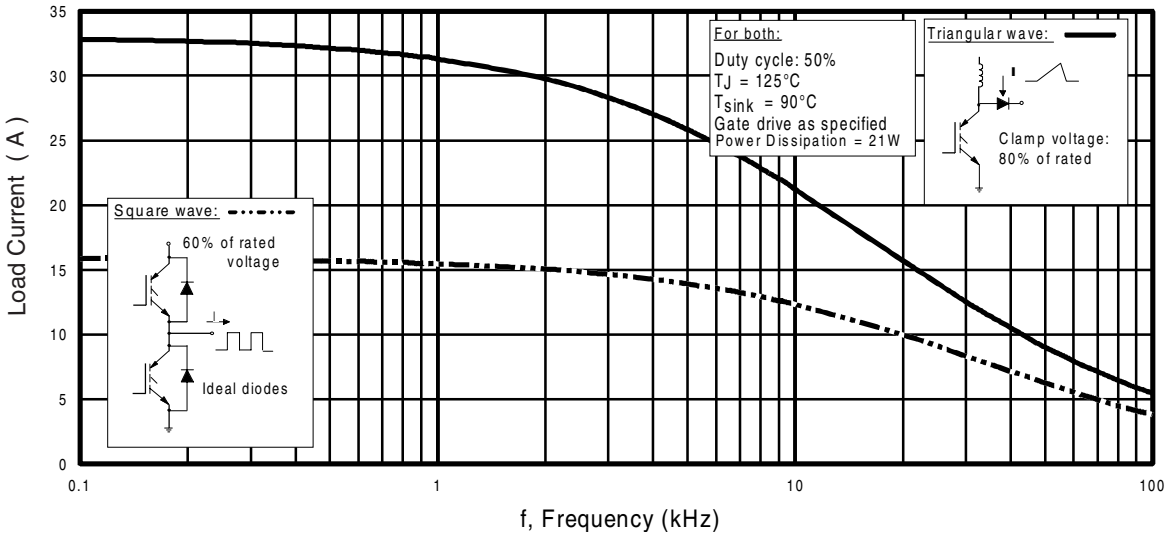


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

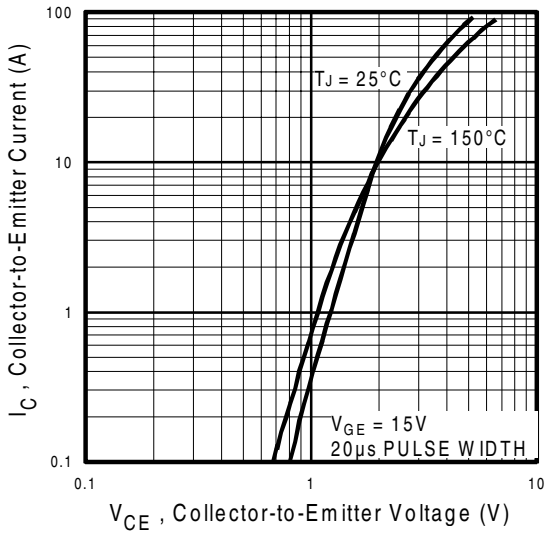


Fig. 2 - Typical Output Characteristics

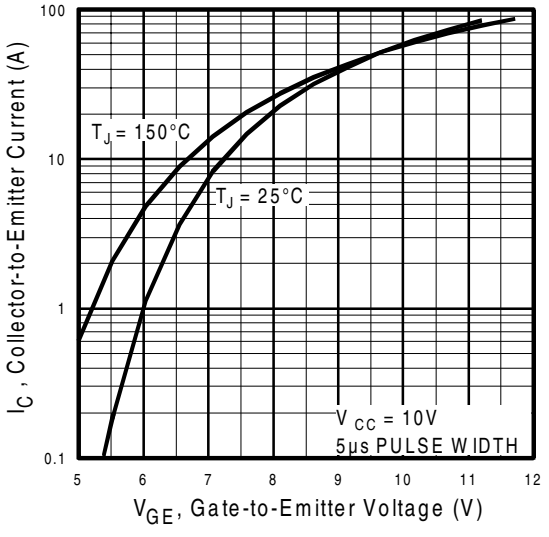


Fig. 3 - Typical Transfer Characteristics

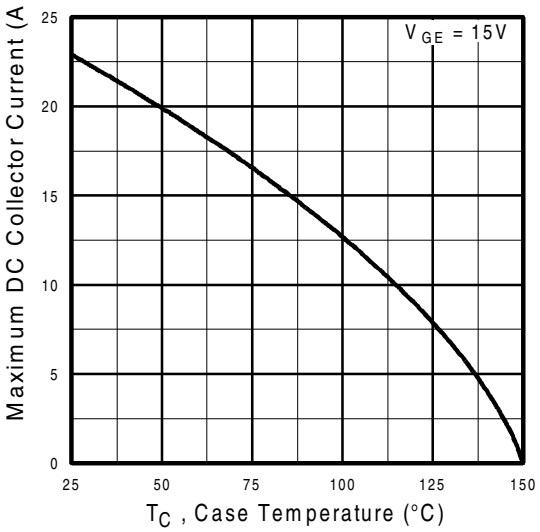


Fig. 4 - Maximum Collector Current vs. Case Temperature

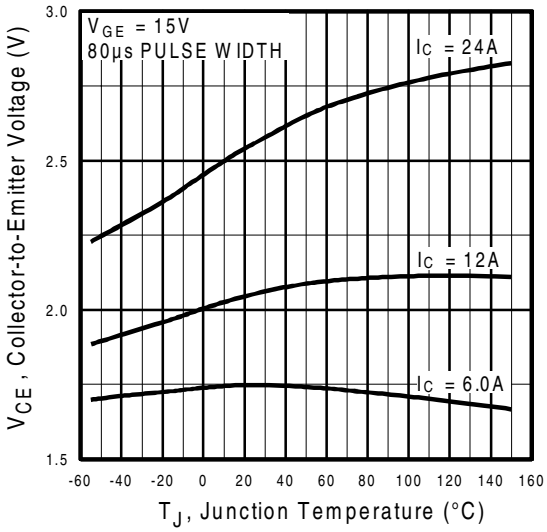


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

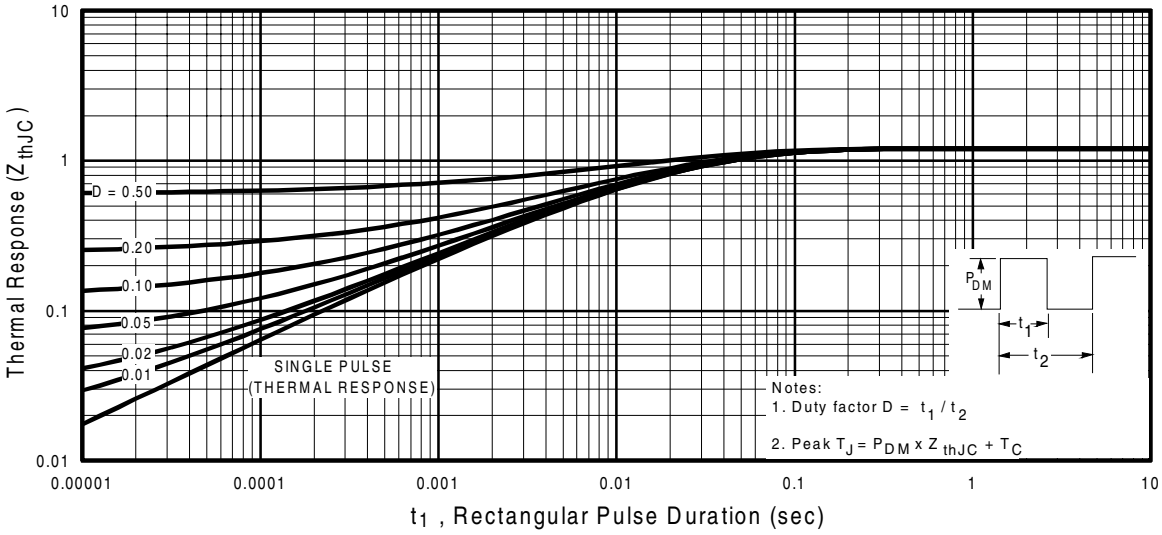


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

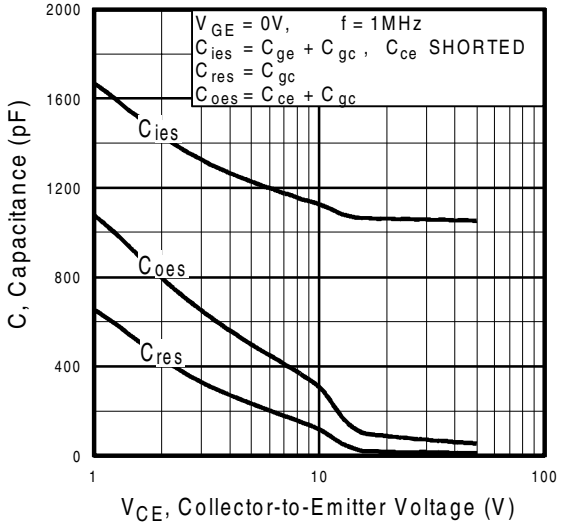


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

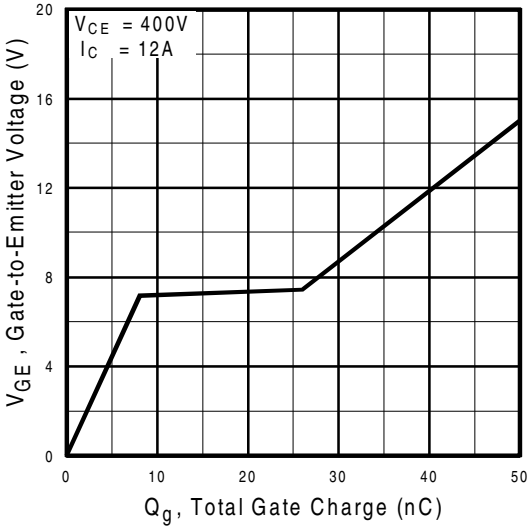


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

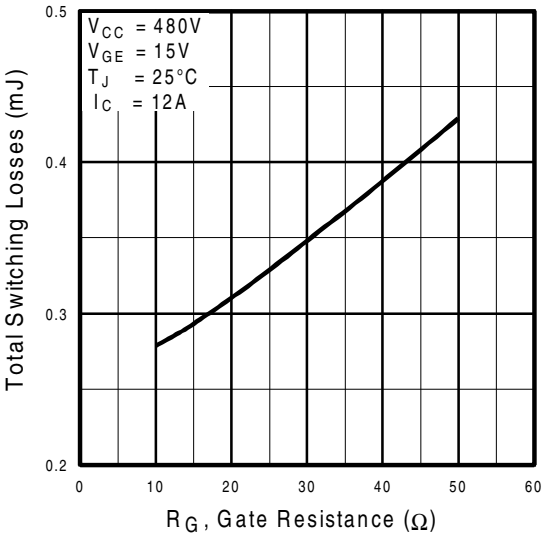


Fig. 9 - Typical Switching Losses vs. Gate Resistance

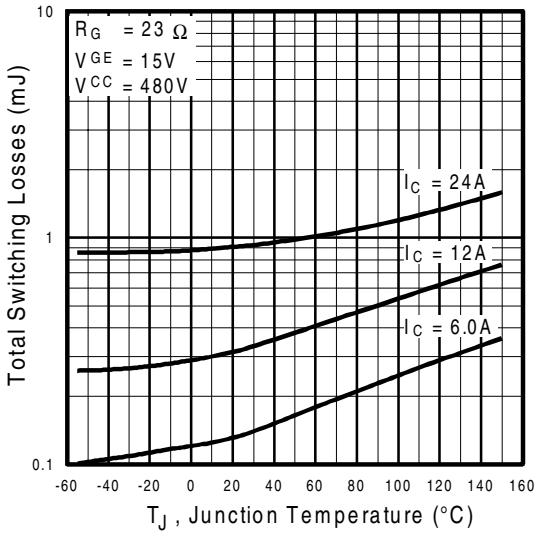


Fig. 10 - Typical Switching Losses vs. Junction Temperature

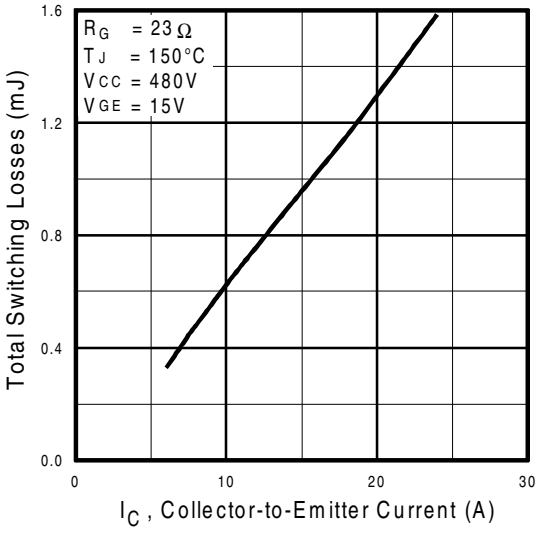


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

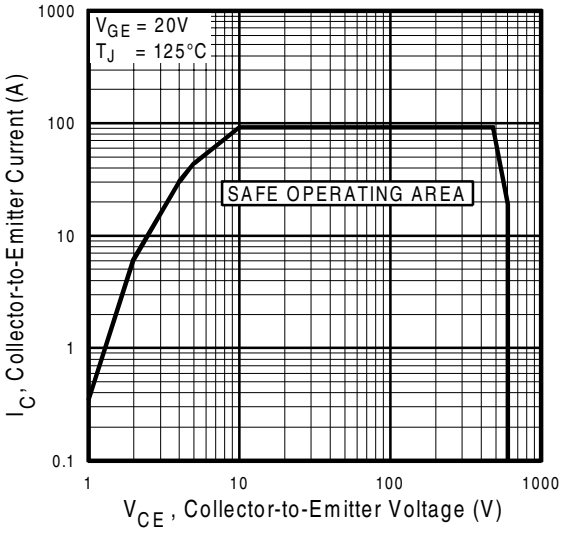


Fig. 12 - Turn-Off SOA

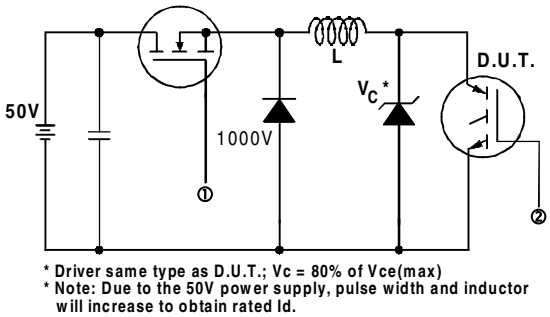


Fig. 13a - Clamped Inductive Load Test Circuit

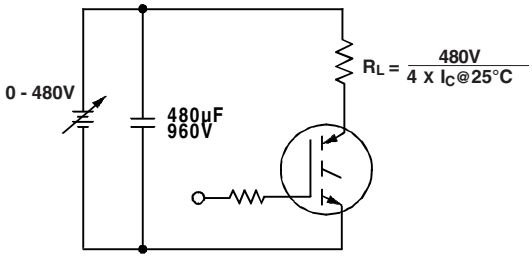


Fig. 13b - Pulsed Collector Current Test Circuit

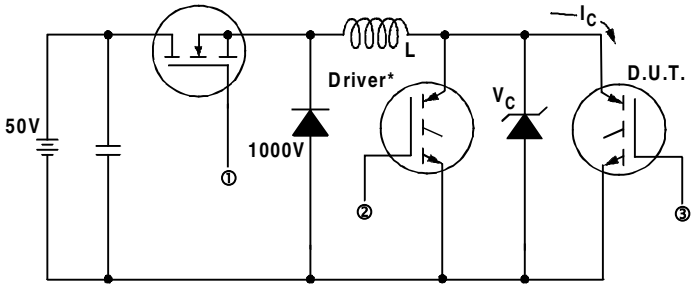


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

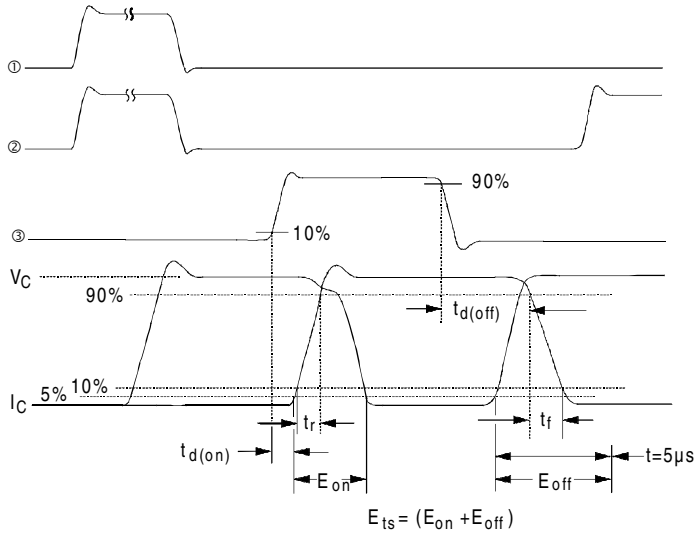
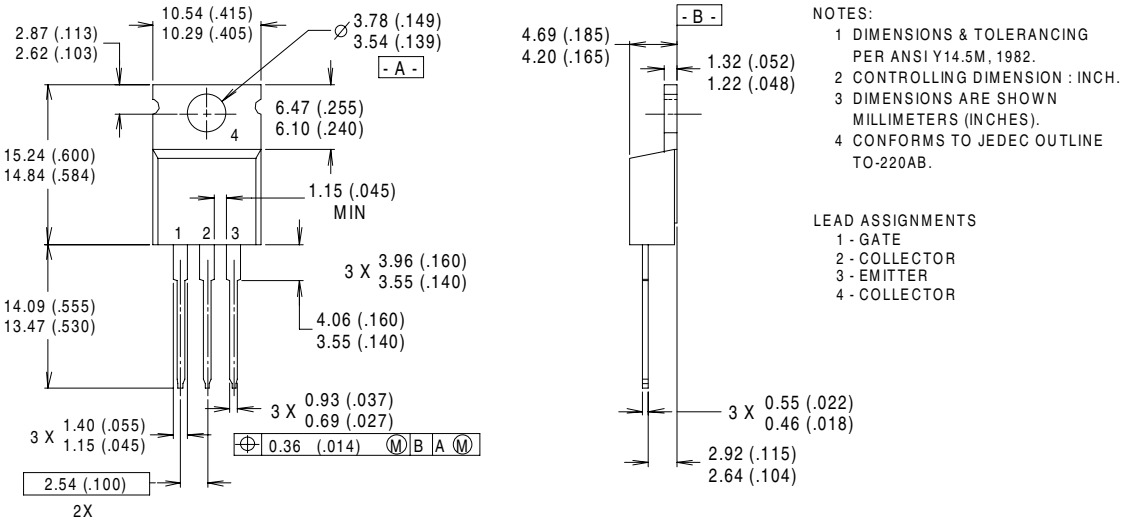


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-220AB



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-220AB.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD 91453B

International
IOR Rectifier

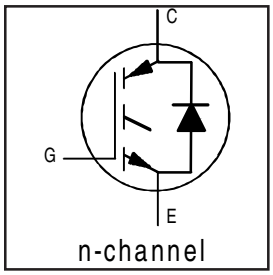
IRG4BC30UD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

UltraFast CoPack IGBT

Features

- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-220AB package

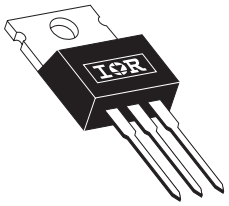


n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.95V

@V_{GE} = 15V, I_C = 12A



TO-220AB

Benefits

- Generation -4 IGBT's offer highest efficiencies available
- IGBTs optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBTs . Minimized recovery characteristics require less/no snubbing
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	23	A
I_C @ T_C = 100°C	Continuous Collector Current	12	
I_{CM}	Pulsed Collector Current ①	92	
I_{LM}	Clamped Inductive Load Current ②	92	
I_F @ T_C = 100°C	Diode Continuous Forward Current	12	
I_{FM}	Diode Maximum Forward Current	92	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	------	------	1.2	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	------	------	2.5	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	------	0.50	------	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	-----	-----	80	
Wt	Weight	------	2 (0.07)	------	g (oz)

4/17/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	----	----	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	----	0.63	----	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	----	1.95	2.1	V	I_C = 12A V_{GE} = 15V
		----	2.52	----		I_C = 23A See Fig. 2, 5
		----	2.09	----		I_C = 12A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	----	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	----	-11	----	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	3.1	8.6	----	S	V_{CE} = 100V, I_C = 12A
I_{CES}	Zero Gate Voltage Collector Current	----	----	250	µA	V_{GE} = 0V, V_{CE} = 600V
		----	----	2500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	----	1.4	1.7	V	I_C = 12A See Fig. 13
		----	1.3	1.6		I_C = 12A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	----	----	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	----	50	75	nC	I_C = 12A
Qge	Gate - Emitter Charge (turn-on)	----	8.1	12		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	----	18	27		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	----	40	----	ns	T_J = 25°C
t_r	Rise Time	----	21	----		I_C = 12A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	91	140		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	----	80	130		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	----	0.38	----	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	----	0.16	----		See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	----	0.54	0.9		
$t_{d(on)}$	Turn-On Delay Time	----	40	----	ns	T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	----	22	----		I_C = 12A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	120	----		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	----	180	----		Energy losses include "tail" and
E_{ts}	Total Switching Loss	----	0.89	----	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	----	7.5	----	nH	Measured 5mm from package
C_{ies}	Input Capacitance	----	1100	----	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	----	73	----		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	----	14	----		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	----	42	60	ns	T_J = 25°C See Fig.
		----	80	120		T_J = 125°C 14 I_F = 12A
I_{rr}	Diode Peak Reverse Recovery Current	----	3.5	6.0	A	T_J = 25°C See Fig.
		----	5.6	10		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	----	80	180	nC	T_J = 25°C See Fig.
		----	220	600		T_J = 125°C 16 di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	----	180	----	A/µs	T_J = 25°C See Fig.
	During t_b	----	120	----		T_J = 125°C 17

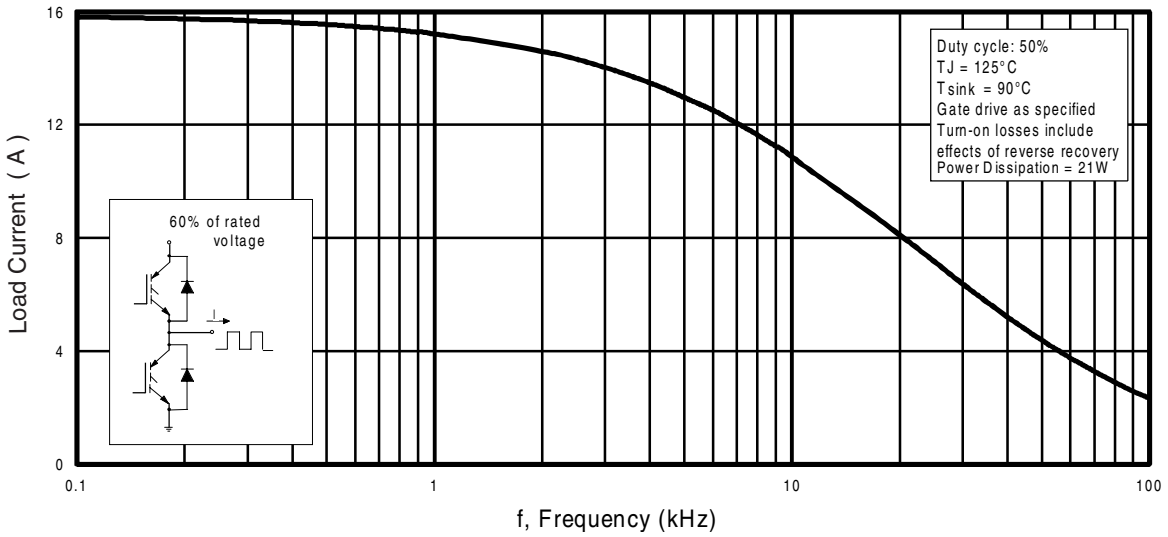


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

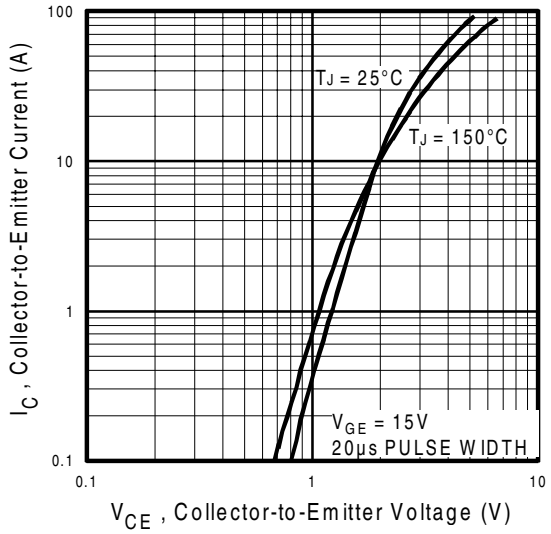


Fig. 2 - Typical Output Characteristics

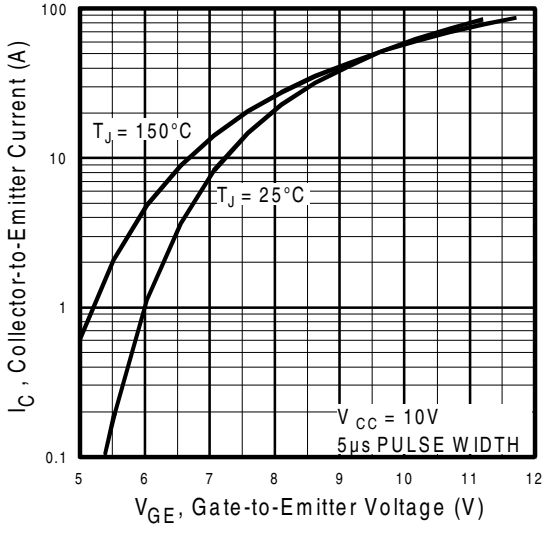


Fig. 3 - Typical Transfer Characteristics

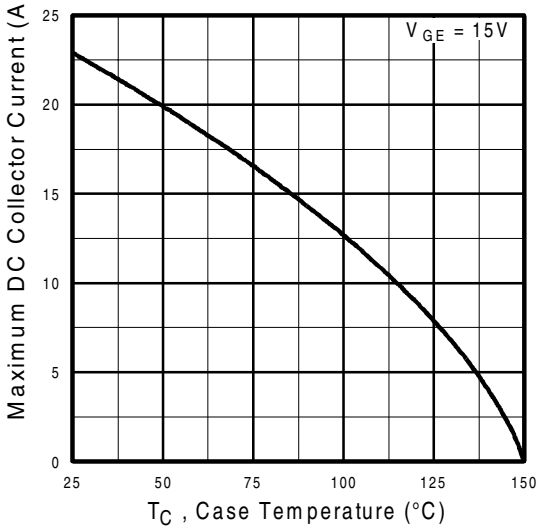


Fig. 4 - Maximum Collector Current vs. Case Temperature

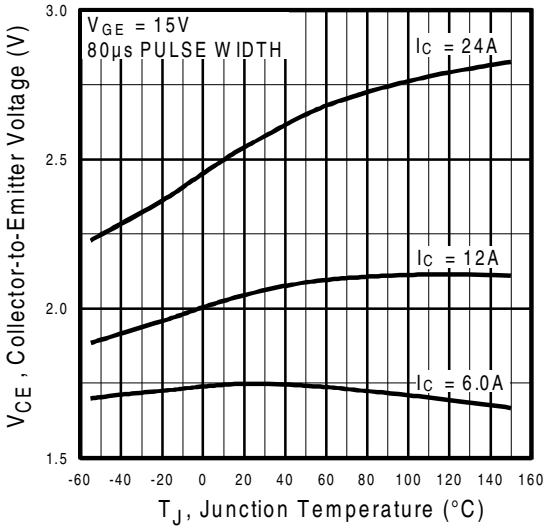


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

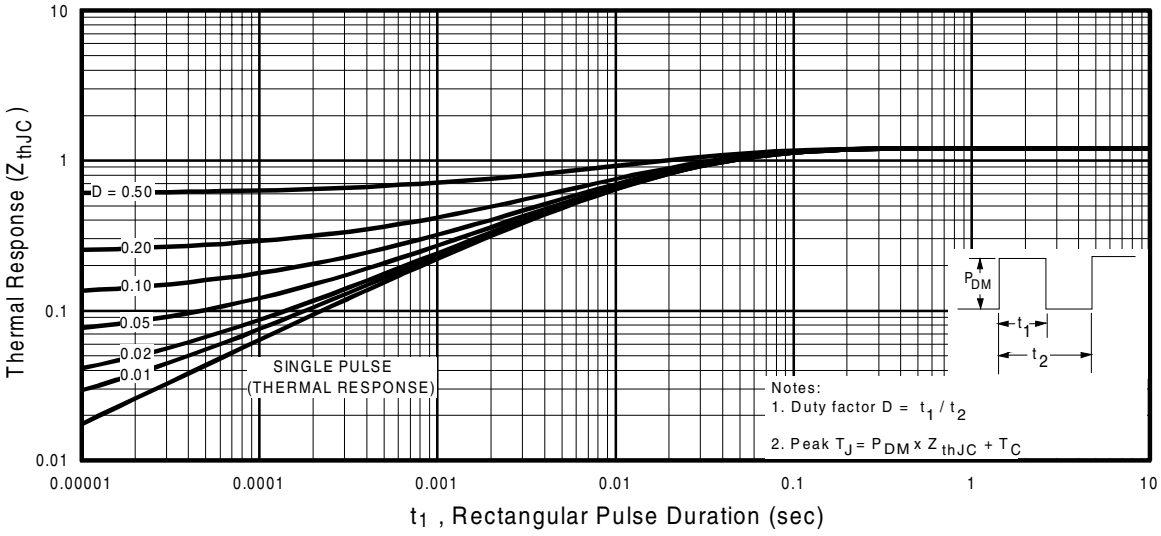


Fig. 6 - Maximum IGBT Effective Transient Thermal Impedance, Junction-to-Case

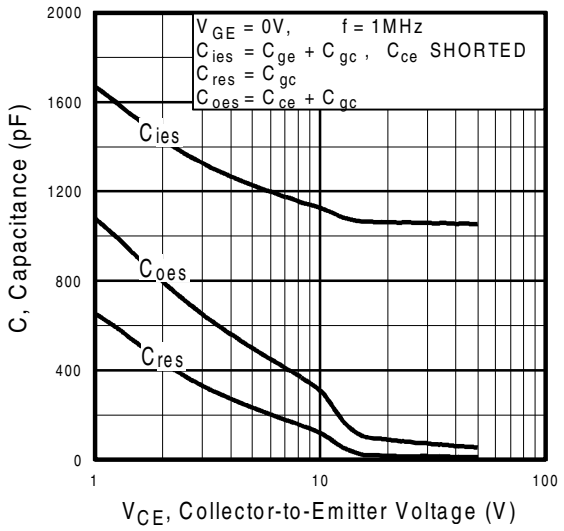


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

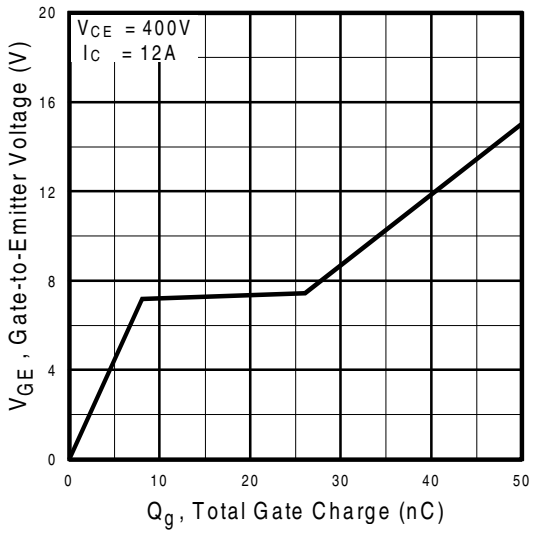


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

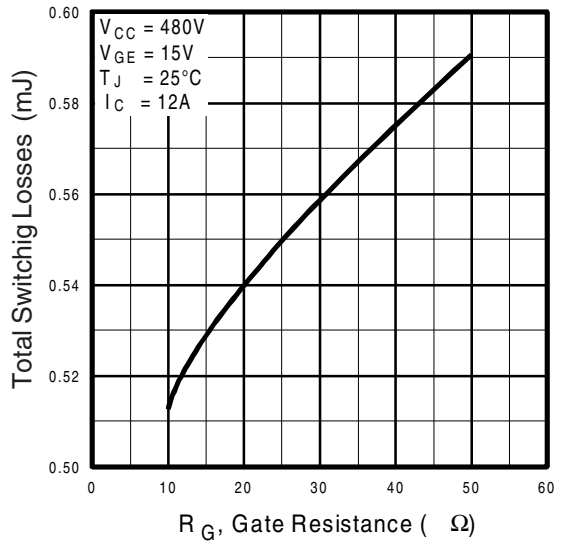


Fig. 9 - Typical Switching Losses vs. Gate Resistance

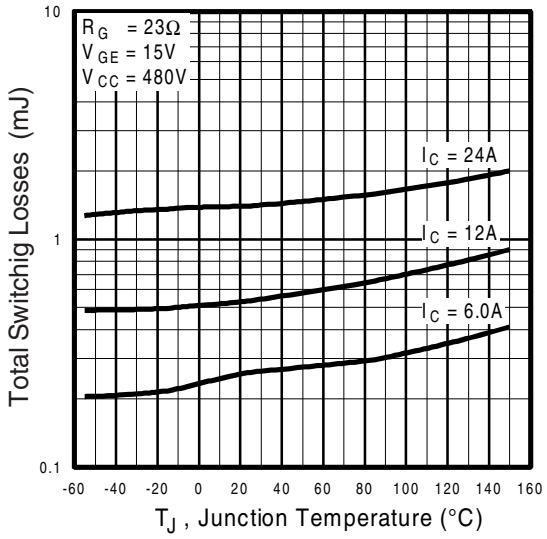


Fig. 10 - Typical Switching Losses vs. Junction Temperature

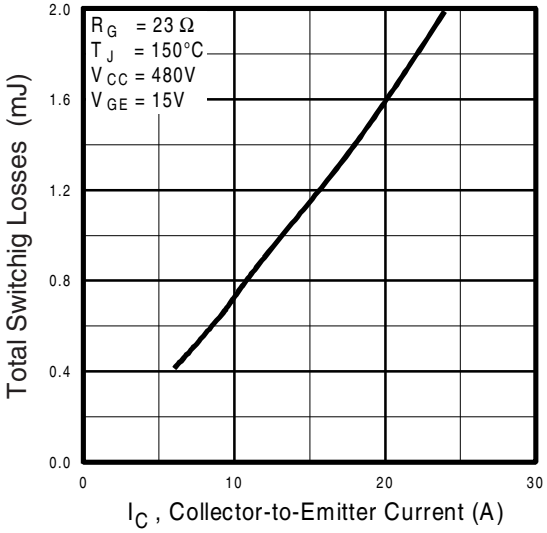


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

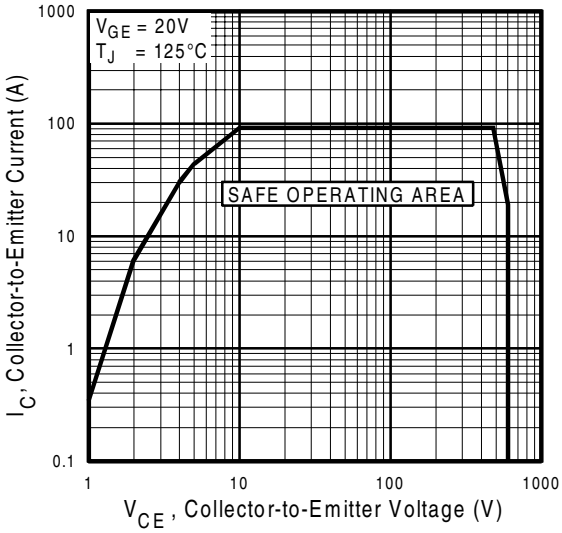


Fig. 12 - Turn-Off SOA

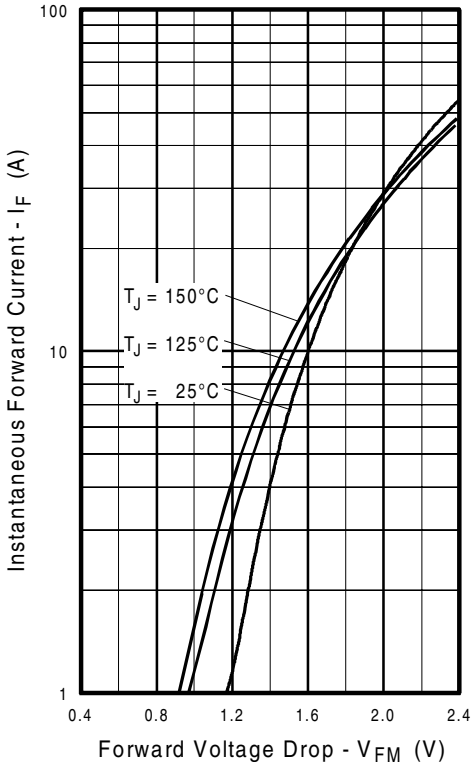


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

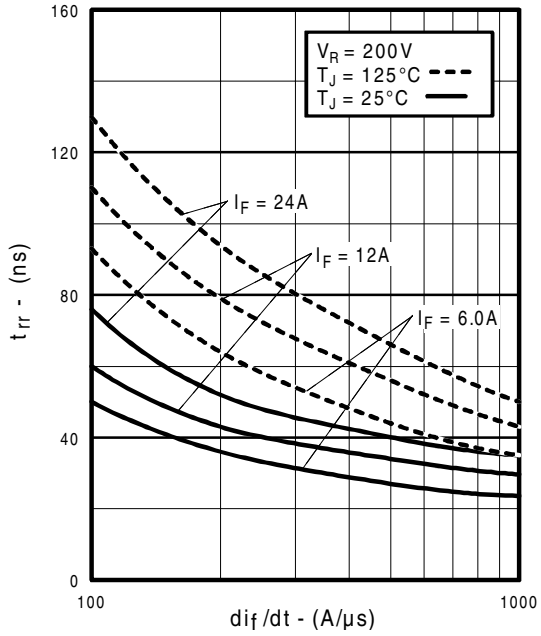


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

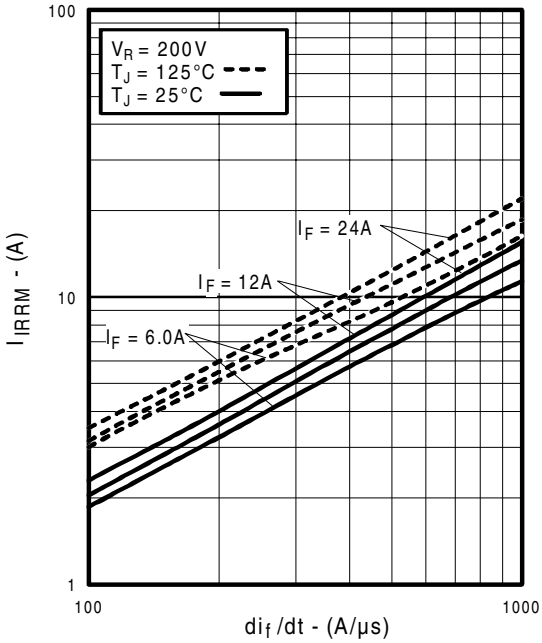


Fig. 15 - Typical Recovery Current vs. di_f/dt

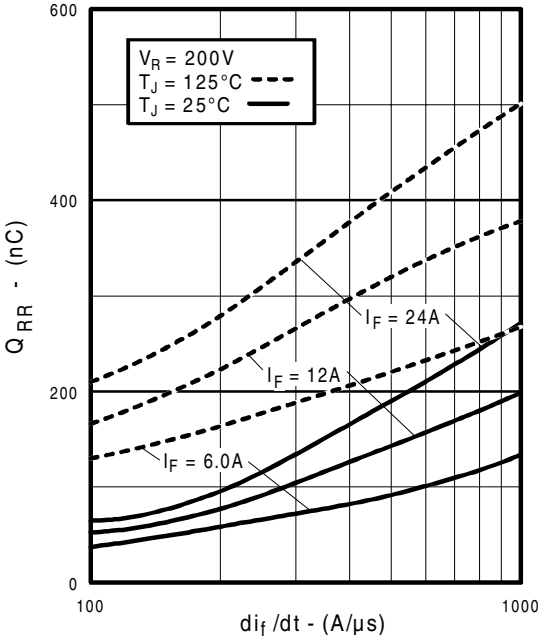


Fig. 16 - Typical Stored Charge vs. di_f/dt

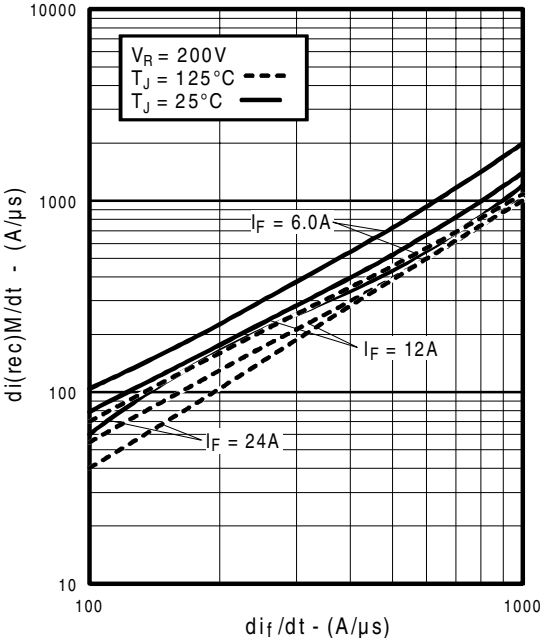


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

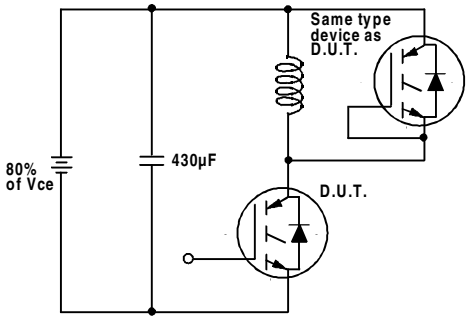


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

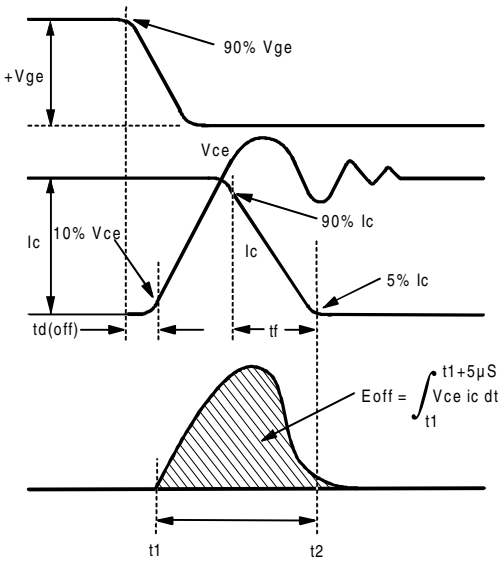


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

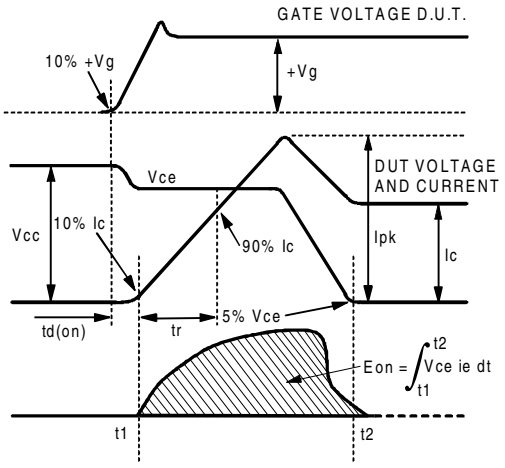


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

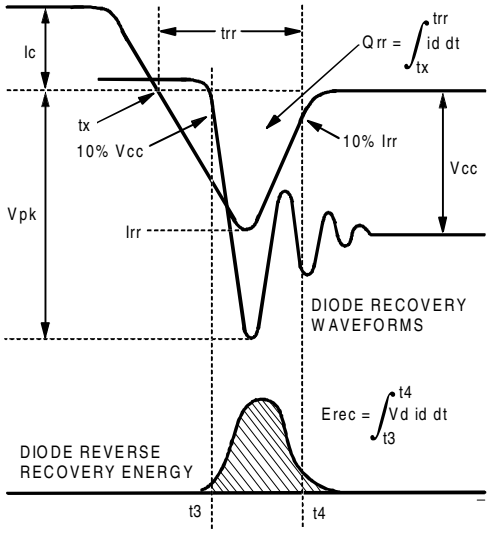


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

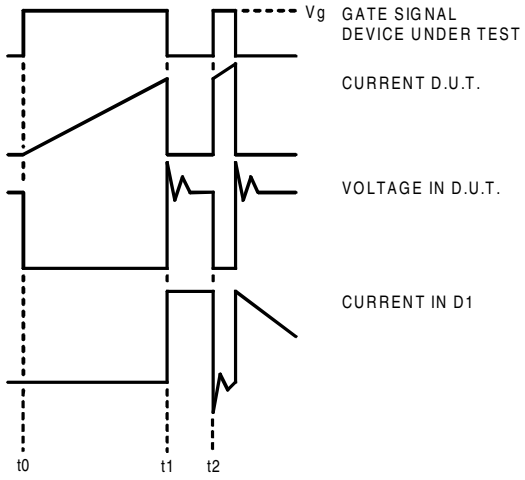


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

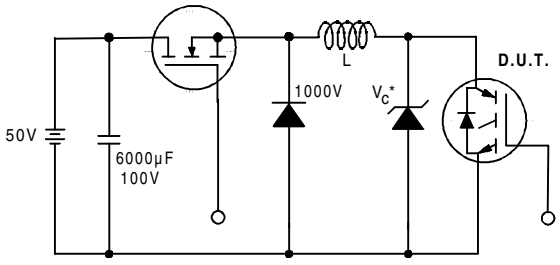


Figure 19. Clamped Inductive Load Test Circuit

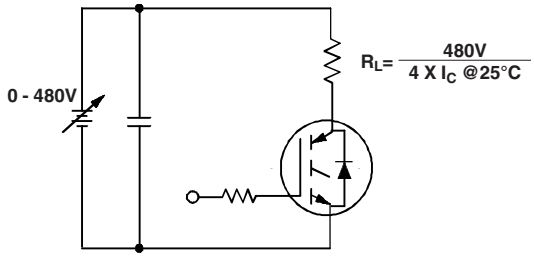


Figure 20. Pulsed Collector Current Test Circuit

Notes:

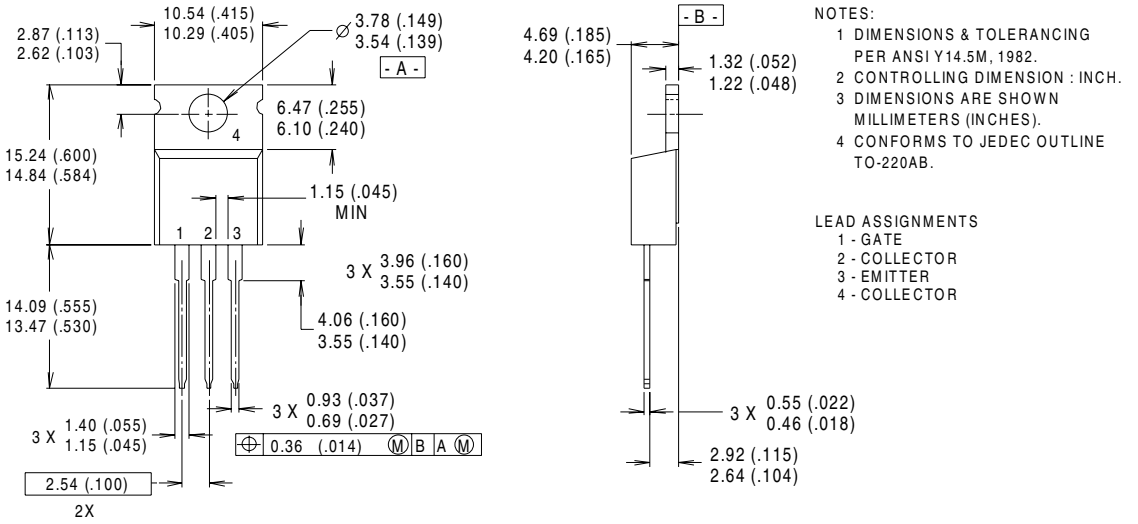
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 23Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD 91461E

International
IOR Rectifier

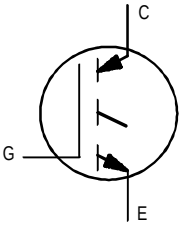
IRG4PC30U

INSULATED GATE BIPOLAR TRANSISTOR

UltraFast Speed IGBT

Features

- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-247AC package



n-channel

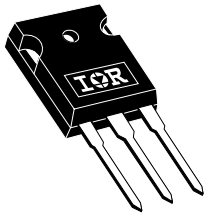
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.95V

@V_{GE} = 15V, I_C = 12A

Benefits

- Generation 4 IGBT's offer highest efficiency available
- IGBT's optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	23	A
I_C @ T_C = 100°C	Continuous Collector Current	12	
I_{CM}	Pulsed Collector Current ①	92	
I_{LM}	Clamped Inductive Load Current ②	92	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	10	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

12/30/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.63	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.95	2.1	V	I_C = 12A V_{GE} = 15V
		—	2.52	—		I_C = 23A See Fig.2, 5
		—	2.09	—		I_C = 12A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-13	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	3.1	8.6	—	S	V_{CE} = 100 V, I_C = 12A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	50	75	nC	I_C = 12A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	8.1	12		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	18	27		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	
t_r	Rise Time	—	9.6	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	78	120		I_C = 12A, V_{CC} = 480V
t_f	Fall Time	—	97	150		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.16	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.20	—		See Fig. 10, 11, 13, 14
E_{ts}	Total Switching Loss	—	0.36	0.50		
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	T_J = 150°C,
t_r	Rise Time	—	13	—		I_C = 12A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	180	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	140	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.73	—	mJ	See Fig. 13, 14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1100	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	73	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	14	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 23Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

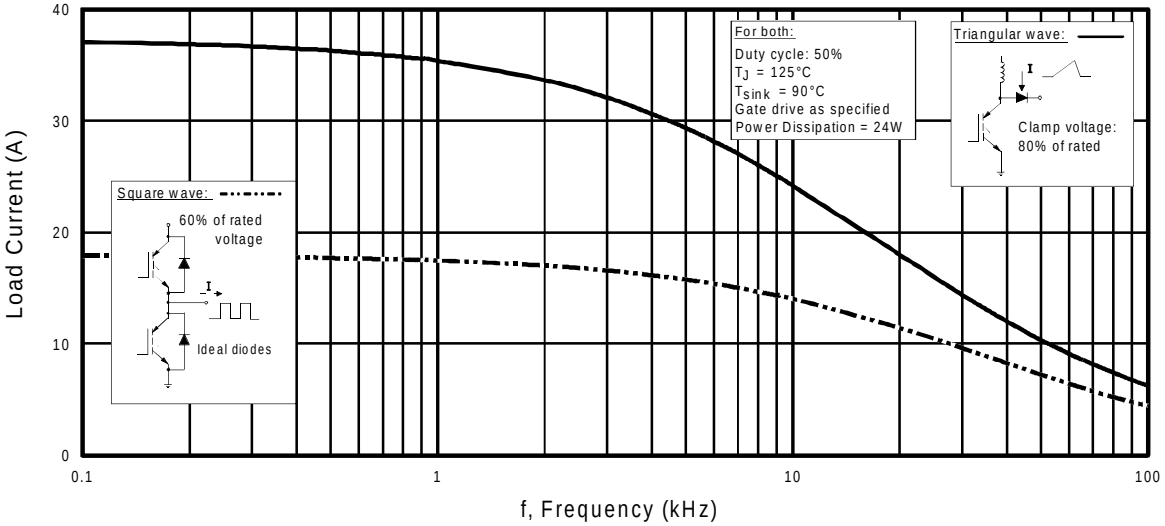


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

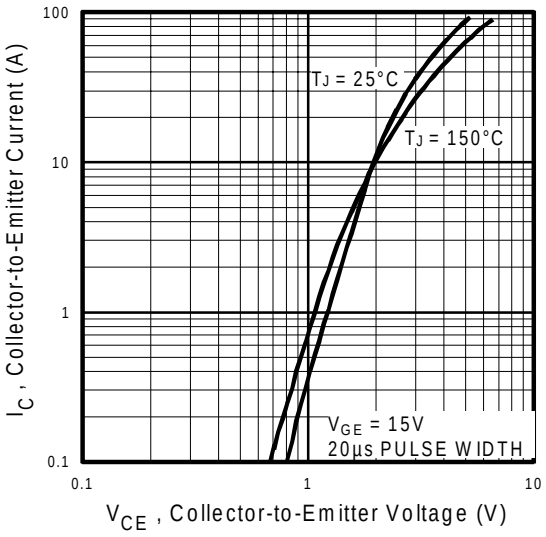


Fig. 2 - Typical Output Characteristics

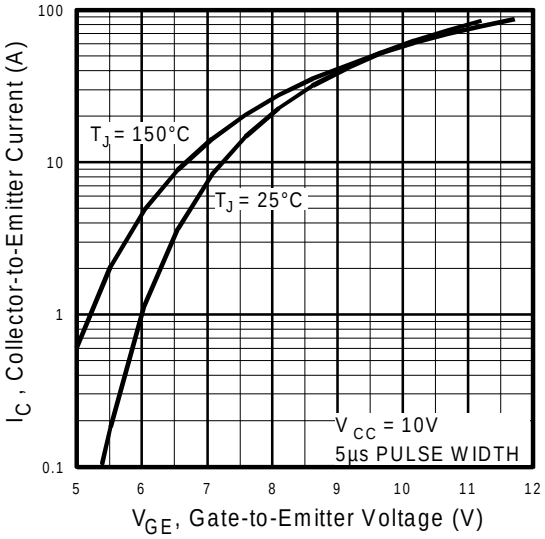


Fig. 3 - Typical Transfer Characteristics

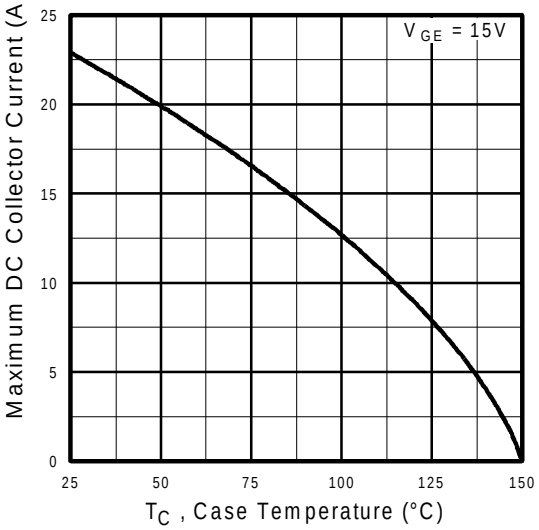


Fig. 4 - Maximum Collector Current vs. Case Temperature

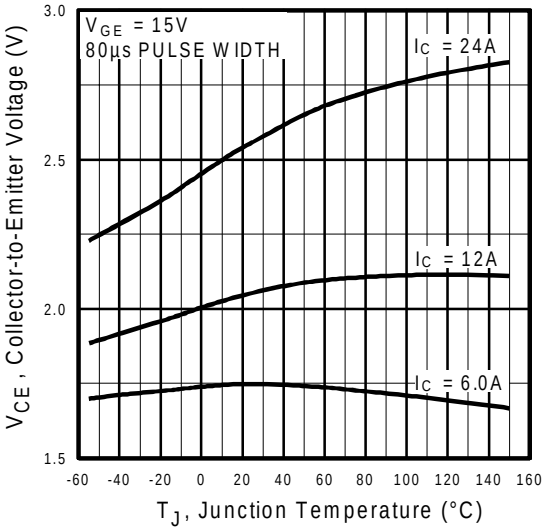


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

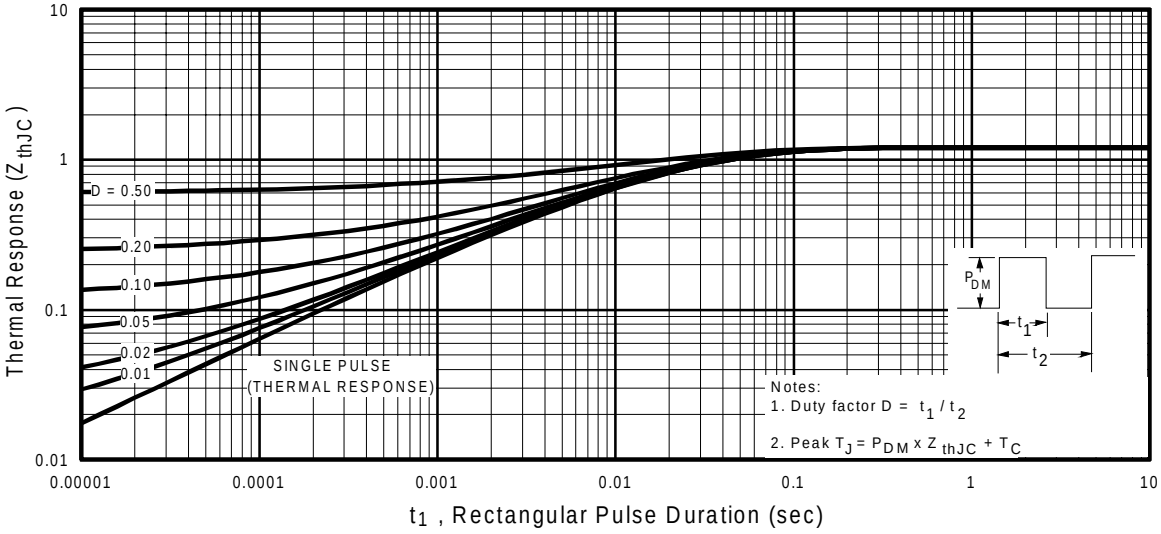


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

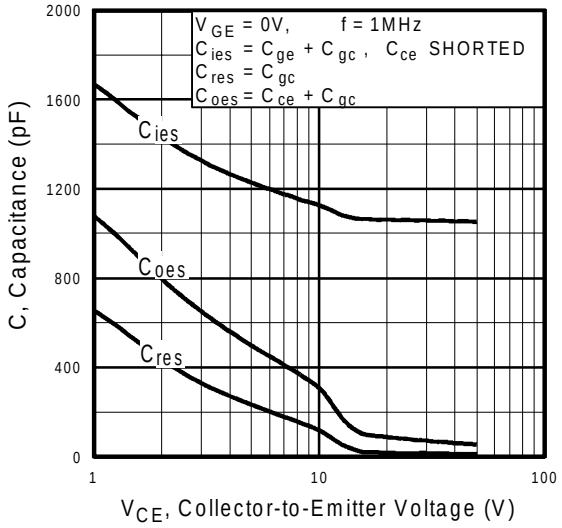


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

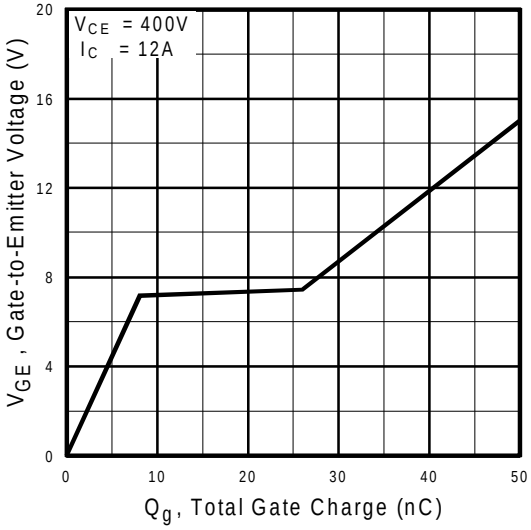


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

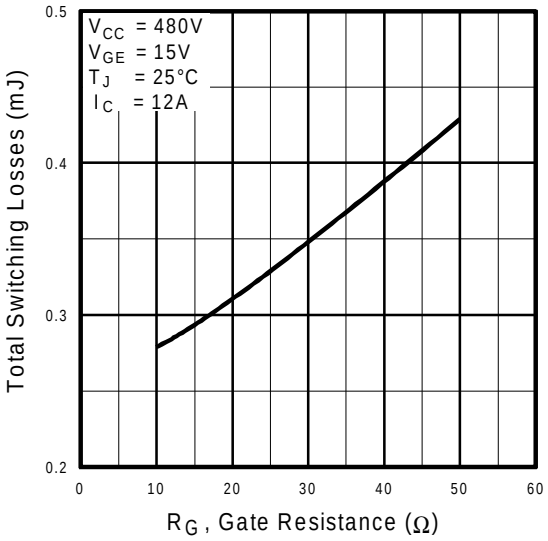


Fig. 9 - Typical Switching Losses vs. Gate Resistance

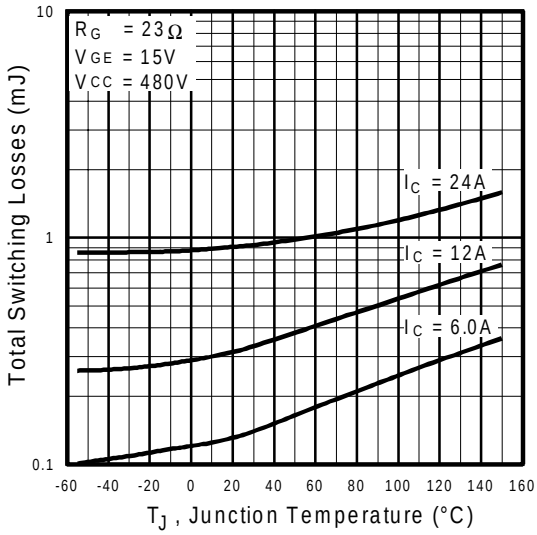


Fig. 10 - Typical Switching Losses vs. Junction Temperature

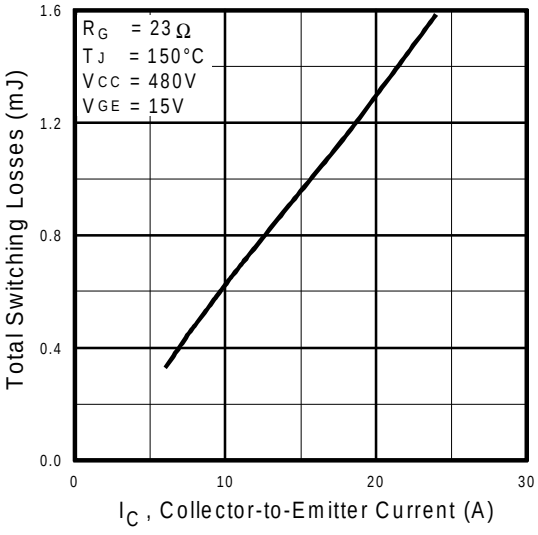


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

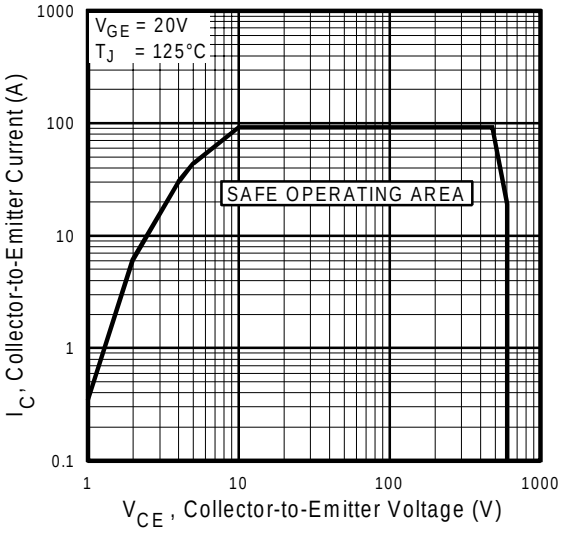


Fig. 12 - Turn-Off SOA

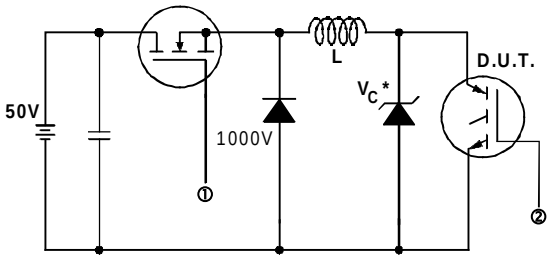


Fig. 13a - Clamped Inductive Load Test Circuit

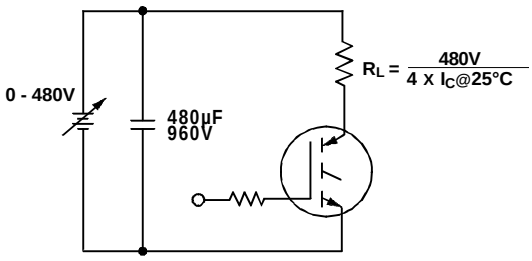


Fig. 13b - Pulsed Collector Current Test Circuit

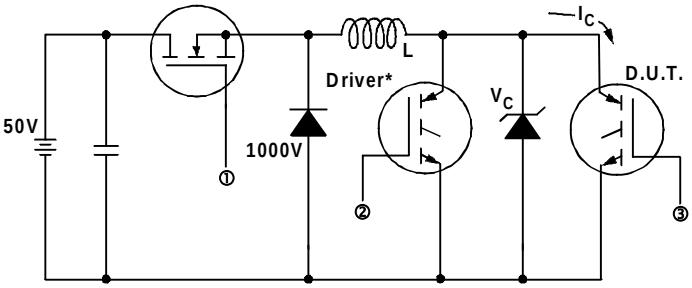


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

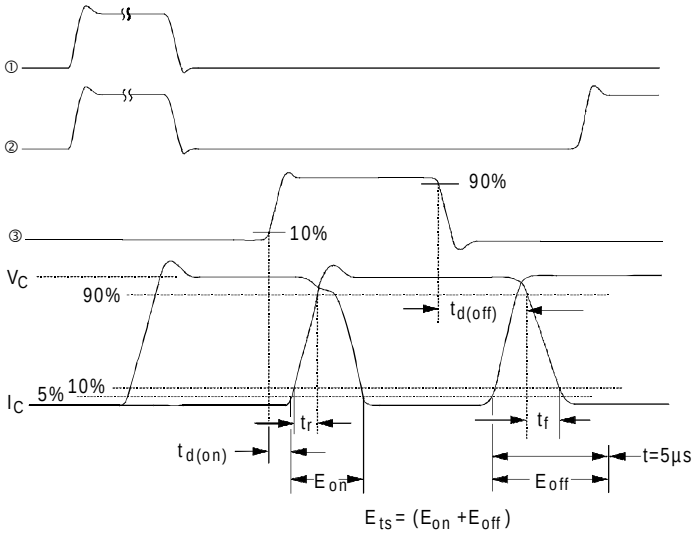
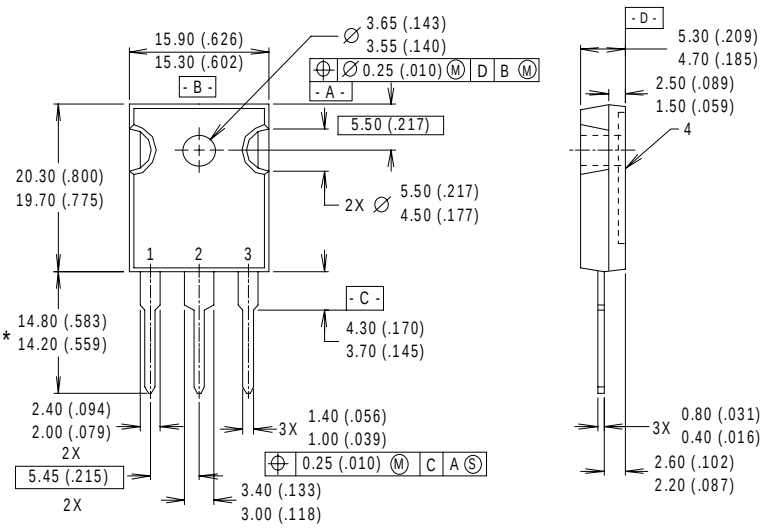


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
Data and specifications subject to change without notice. 12/00

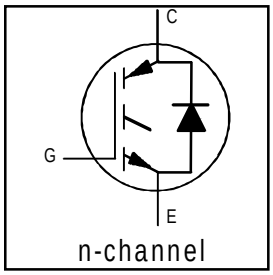
PD 91462B

International
IOR Rectifier

IRG4PC30UD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

UltraFast CoPack IGBT



n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.95V

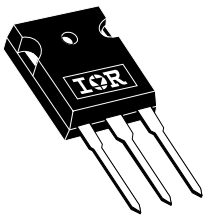
@V_{GE} = 15V, I_C = 12A

Features

- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-247AC package

Benefits

- Generation -4 IGBT's offer highest efficiencies available
- IGBT's optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBT's . Minimized recovery characteristics require less/no snubbing
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's


TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	23	A
I_C @ T_C = 100°C	Continuous Collector Current	12	
I_{CM}	Pulsed Collector Current ①	92	
I_{LM}	Clamped Inductive Load Current ②	92	
I_F @ T_C = 100°C	Diode Continuous Forward Current	12	
I_{FM}	Diode Maximum Forward Current	92	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	------	------	1.2	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	------	------	2.5	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	------	0.24	------	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	-----	-----	40	
Wt	Weight	------	6 (0.21)	------	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	----	----	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	----	0.63	----	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	----	1.95	2.1	V	I_C = 12A V_{GE} = 15V
		----	2.52	----		I_C = 23A See Fig. 2, 5
		----	2.09	----		I_C = 12A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	----	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	----	-11	----	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	3.1	8.6	----	S	V_{CE} = 100V, I_C = 12A
I_{CES}	Zero Gate Voltage Collector Current	----	----	250	µA	V_{GE} = 0V, V_{CE} = 600V
		----	----	2500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	----	1.4	1.7	V	I_C = 12A See Fig. 13
		----	1.3	1.6		I_C = 12A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	----	----	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	----	50	75		I_C = 12A
Qge	Gate - Emitter Charge (turn-on)	----	8.1	12	nC	V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	----	18	27		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	----	40	----		T_J = 25°C
t_r	Rise Time	----	21	----	ns	I_C = 12A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	91	140		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	----	80	130		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	----	0.38	----		diode reverse recovery.
E_{off}	Turn-Off Switching Loss	----	0.16	----	mJ	See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	----	0.54	0.9		
$t_{d(on)}$	Turn-On Delay Time	----	40	----		T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	----	22	----	ns	I_C = 12A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	120	----		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	----	180	----		Energy losses include "tail" and
E_{ts}	Total Switching Loss	----	0.89	----	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	----	13	----	nH	Measured 5mm from package
C_{ies}	Input Capacitance	----	1100	----		V_{GE} = 0V
C_{oes}	Output Capacitance	----	73	----	pF	V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	----	14	----		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	----	42	60	ns	T_J = 25°C See Fig.
		----	80	120		T_J = 125°C 14 I_F = 12A
I_{rr}	Diode Peak Reverse Recovery Current	----	3.5	6.0	A	T_J = 25°C See Fig.
		----	5.6	10		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	----	80	180	nC	T_J = 25°C See Fig.
		----	220	600		T_J = 125°C 16 di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	----	180	----	A/µs	T_J = 25°C See Fig.
	During t_b	----	120	----		T_J = 125°C 17

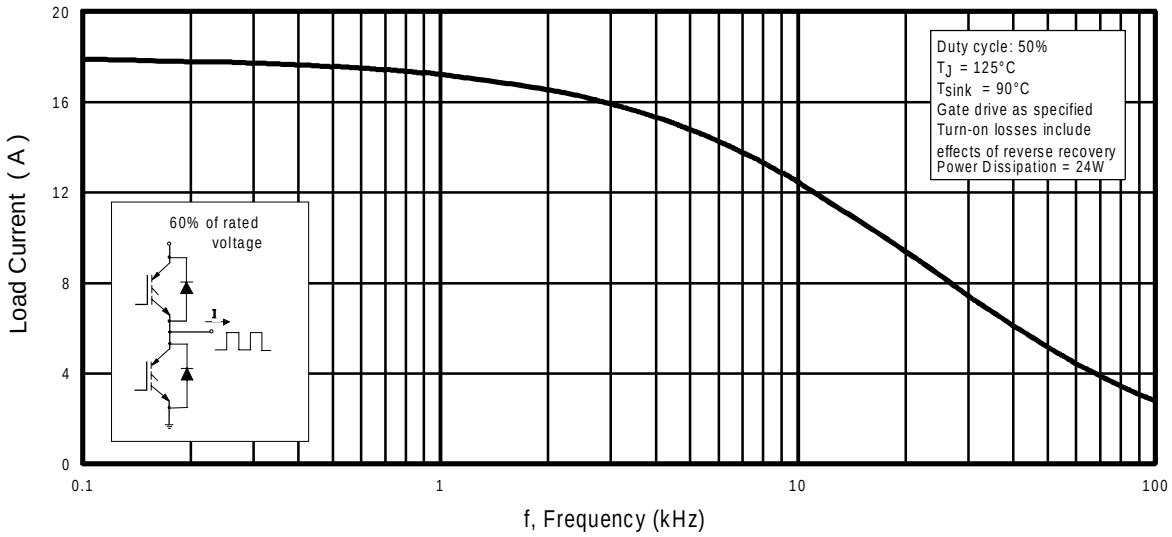


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

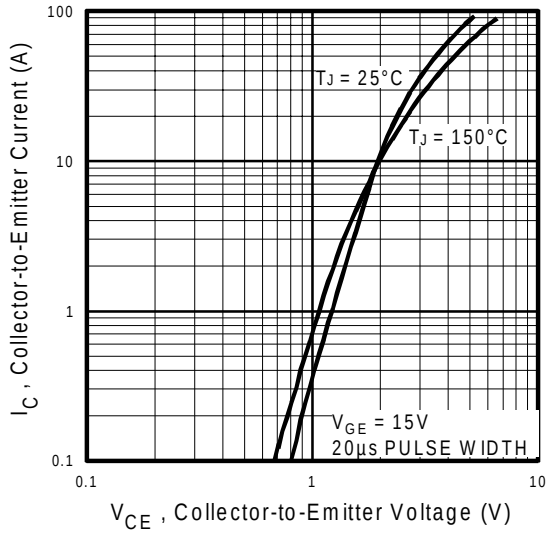


Fig. 2 - Typical Output Characteristics

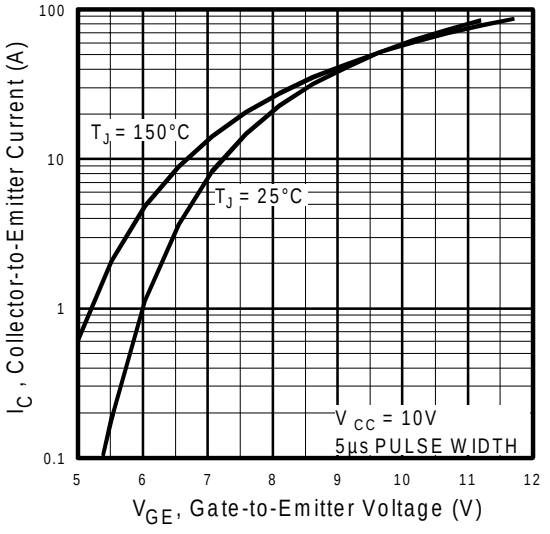


Fig. 3 - Typical Transfer Characteristics

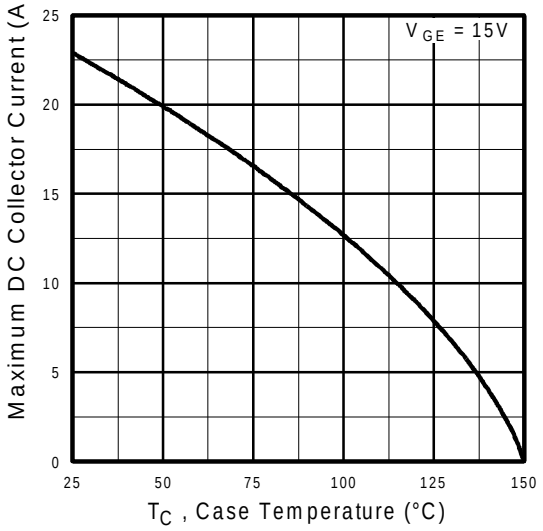


Fig. 4 - Maximum Collector Current vs. Case Temperature

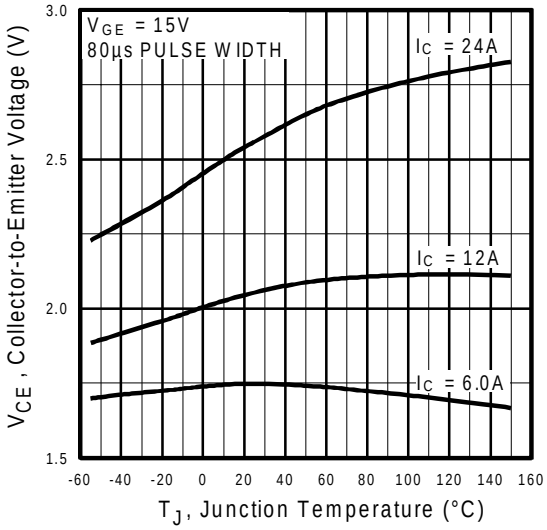


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

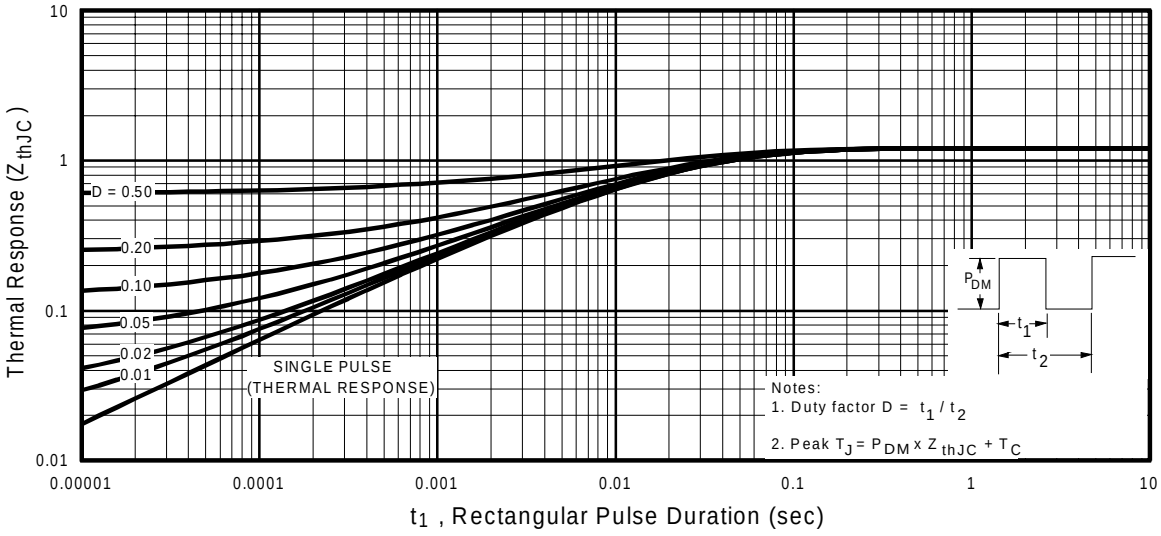


Fig. 6 - Maximum IGBT Effective Transient Thermal Impedance, Junction-to-Case

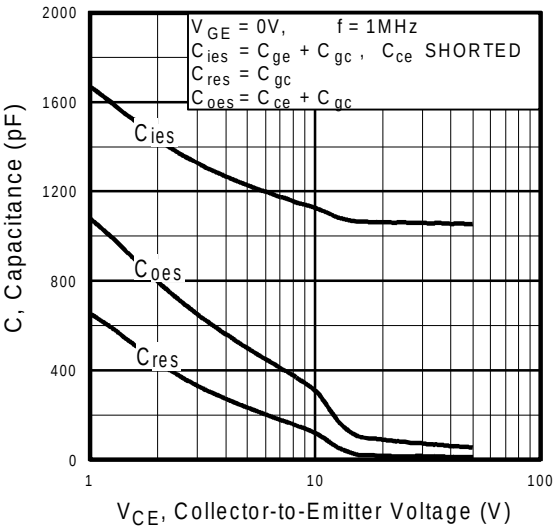


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

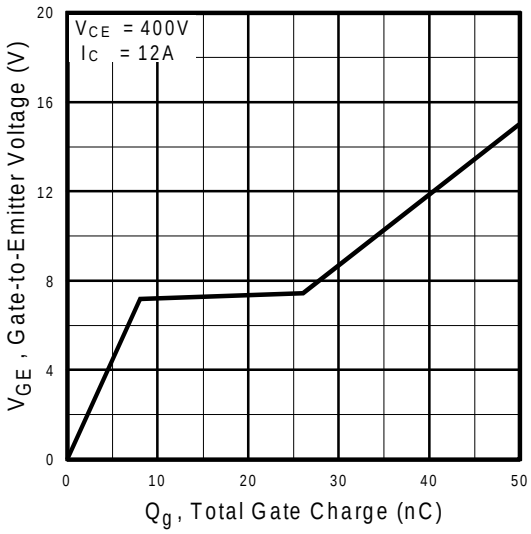


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

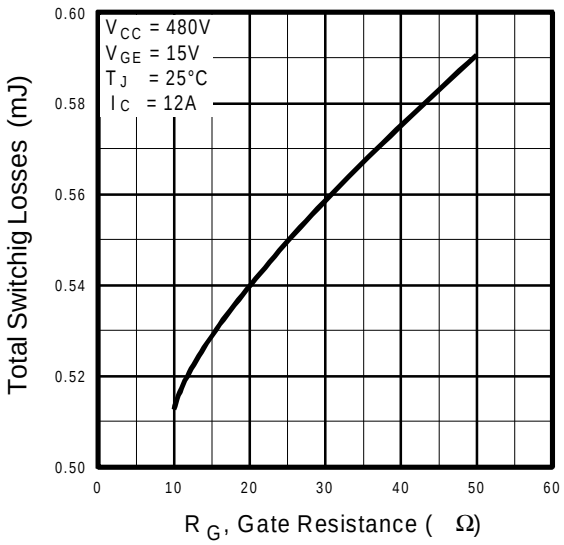


Fig. 9 - Typical Switching Losses vs. Gate Resistance

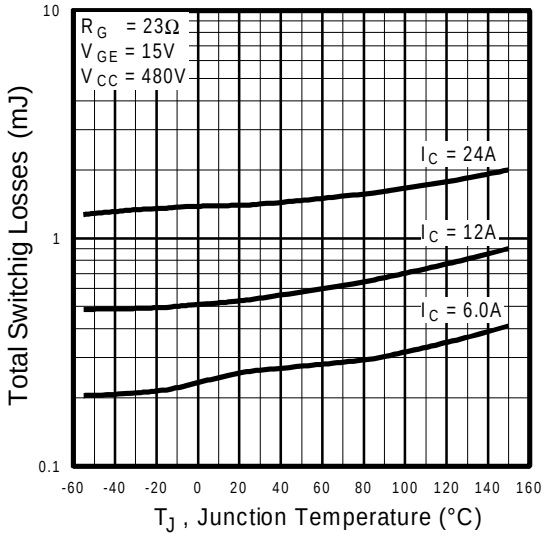


Fig. 10 - Typical Switching Losses vs. Junction Temperature

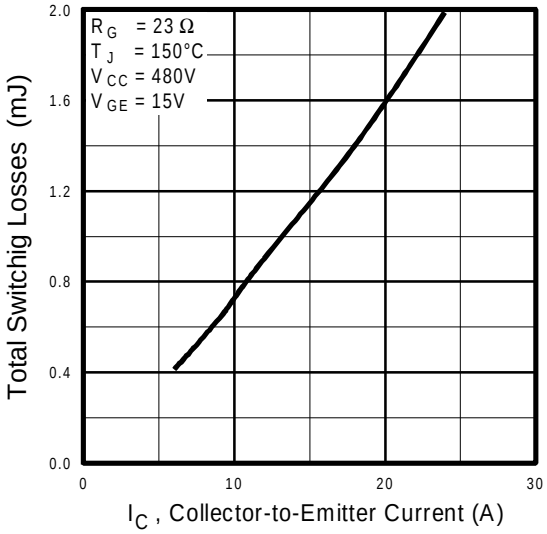


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

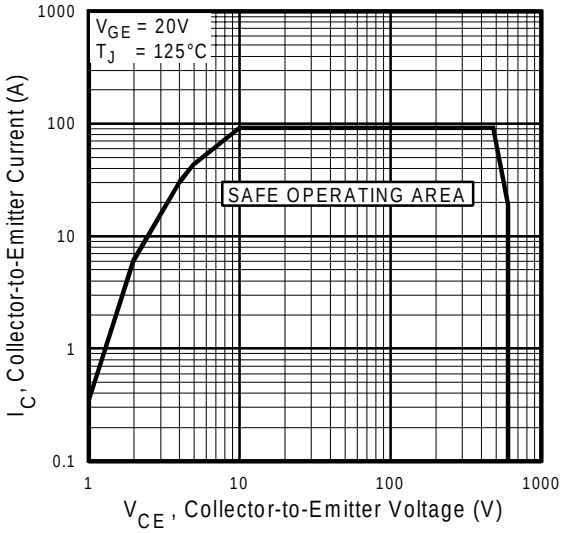


Fig. 12 - Turn-Off SOA

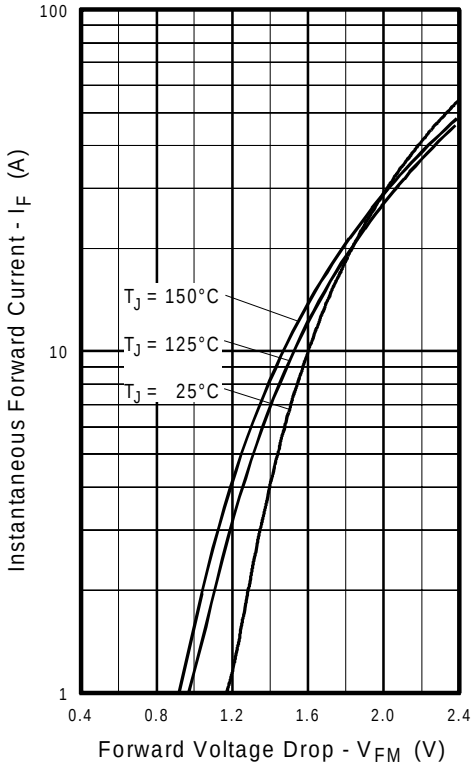


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

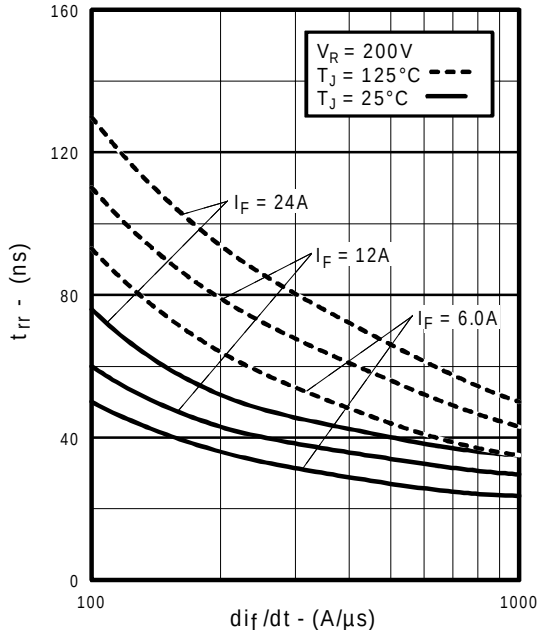


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

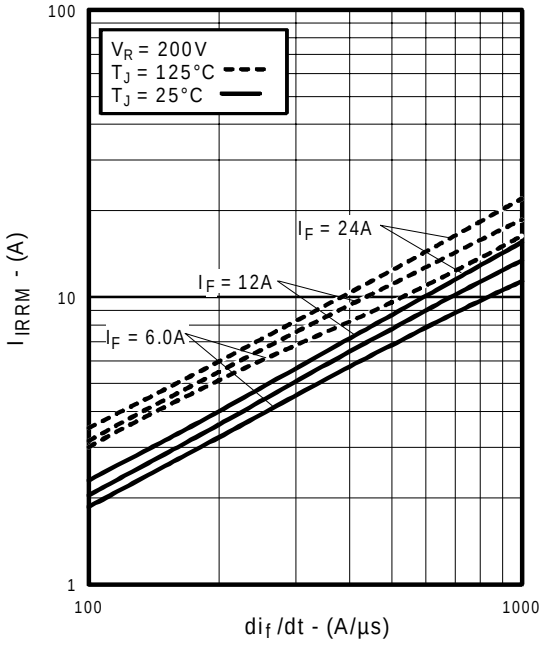


Fig. 15 - Typical Recovery Current vs. di_f/dt

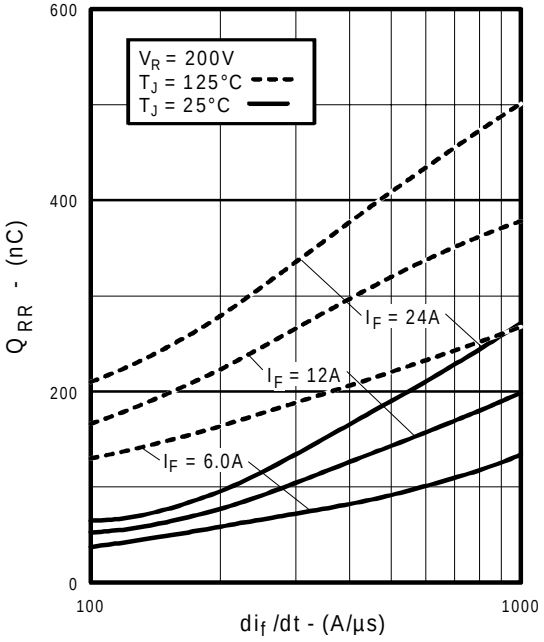


Fig. 16 - Typical Stored Charge vs. di_f/dt

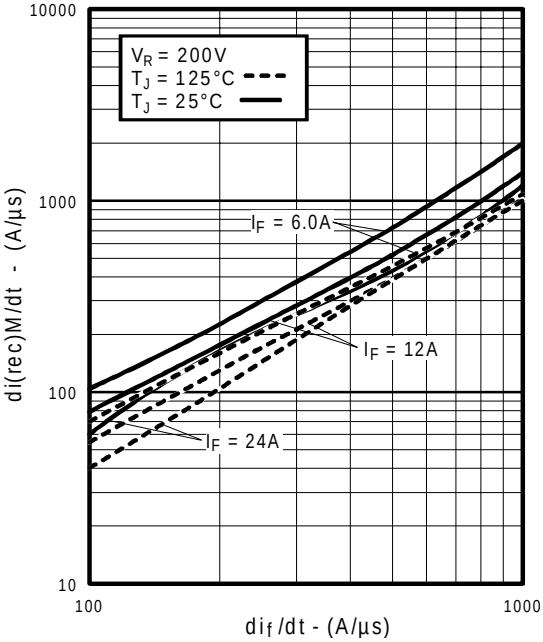


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

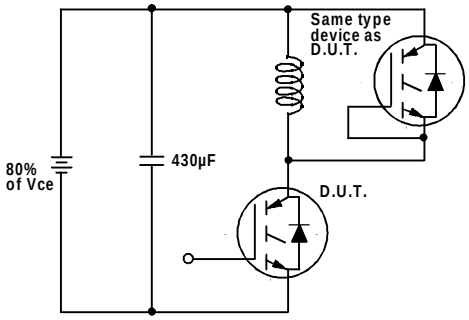


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

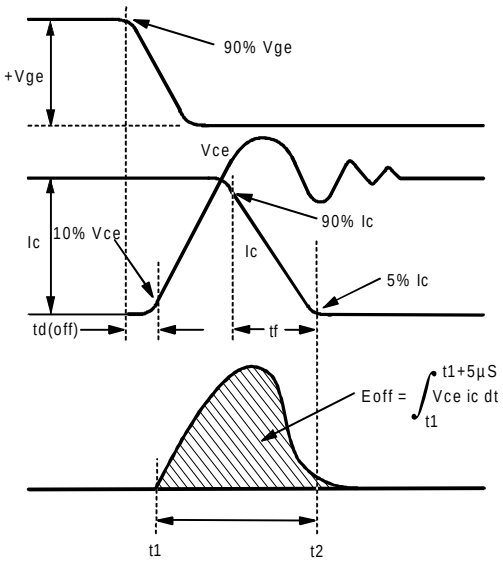


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

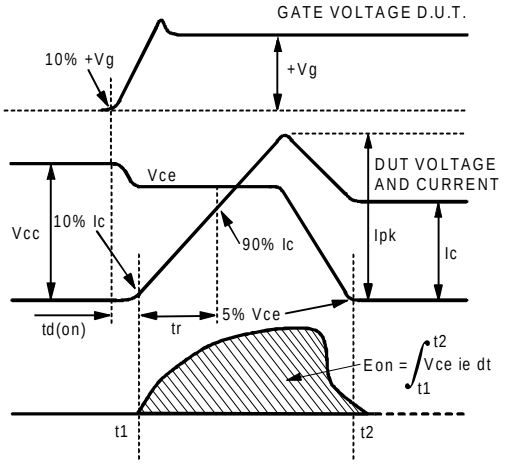


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

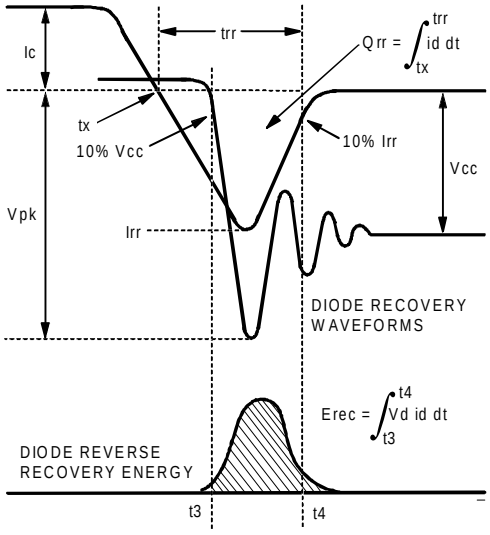


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

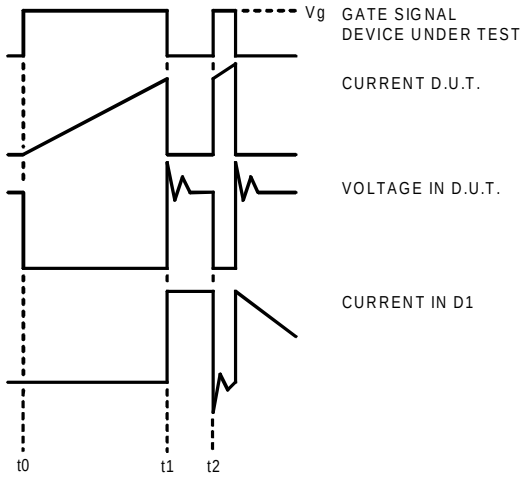


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

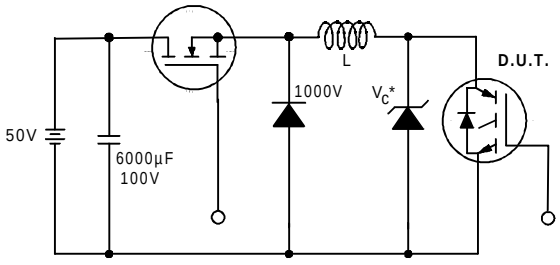


Figure 19. Clamped Inductive Load Test Circuit

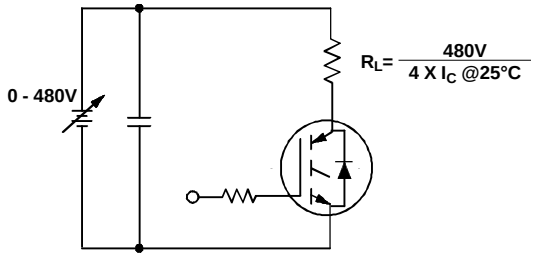


Figure 20. Pulsed Collector Current Test Circuit

Notes:

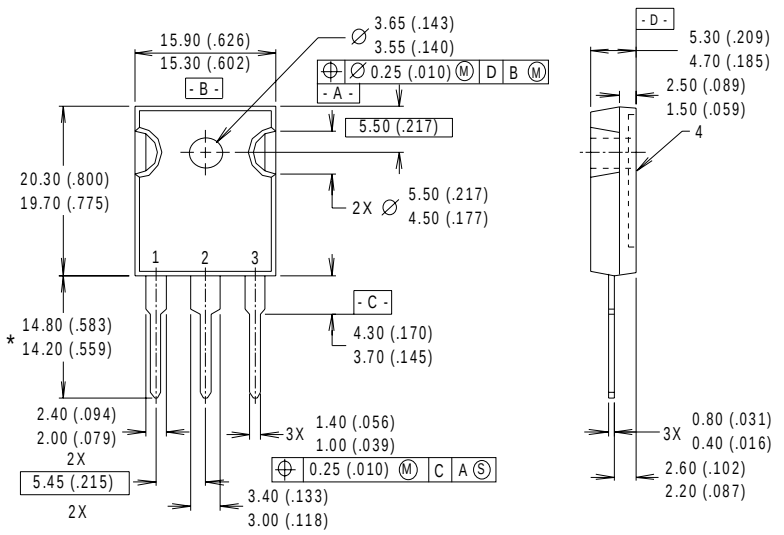
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 23Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
Data and specifications subject to change without notice. 12/00

International
IOR Rectifier

PD - 91803

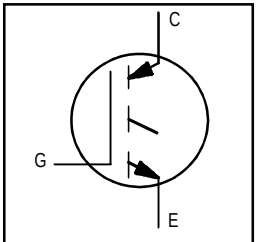
IRG4BC30U-S

INSULATED GATE BIPOLAR TRANSISTOR

UltraFast Speed IGBT

Features

- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard D^2Pak package



n-channel

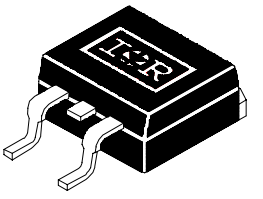
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.95V

@V_{GE} = 15V, I_C = 12A

Benefits

- Generation 4 IGBT's offer highest efficiency available
- IGBT's optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's



D^2Pak

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	23	A
I_C @ T_C = 100°C	Continuous Collector Current	12	
I_{CM}	Pulsed Collector Current ①	92	
I_{LM}	Clamped Inductive Load Current ②	92	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	10	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient, (PCB Mounted,steady-state)*	——	40	

* When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$DV_{(BR)CES}/DT_J$	Temperature Coeff. of Breakdown Voltage	—	0.63	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.95	2.1	V	I_C = 12A V_{GE} = 15V
		—	2.52	—		I_C = 23A See Fig.2, 5
		—	2.09	—		I_C = 12A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$DV_{GE(th)}/DT_J$	Temperature Coeff. of Threshold Voltage	—	-13	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	3.1	8.6	—	S	V_{CE} = 100V, I_C = 12A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	50	75	nC	I_C = 12A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	8.1	12		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	18	27		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	
t_r	Rise Time	—	9.6	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	78	120		I_C = 12A, V_{CC} = 480V
t_f	Fall Time	—	97	150		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.16	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.20	—		See Fig. 10, 11, 13, 14
E_{ts}	Total Switching Loss	—	0.36	0.50		
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	T_J = 150°C,
t_r	Rise Time	—	13	—		I_C = 12A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	180	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	140	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.73	—	mJ	See Fig. 13, 14
L_E	Internal Source Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1100	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	73	—		V_{CC} = 30V See Fig.7
C_{res}	Reverse Transfer Capacitance	—	14	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 23Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width £ 80µs; duty factor £ 0.1%.

⑤ Pulse width 5.0µs, single shot.

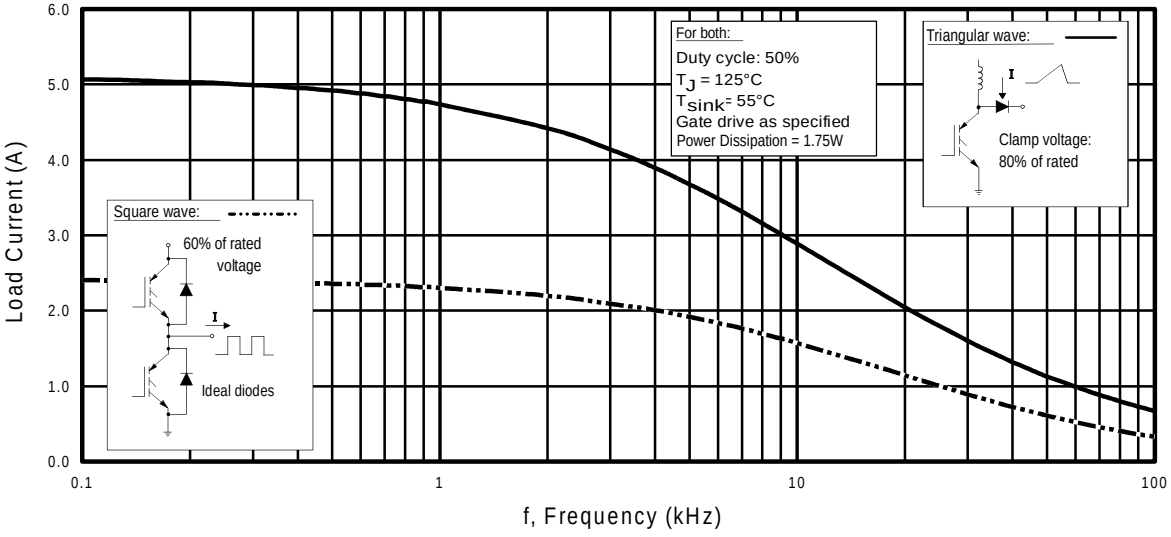


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

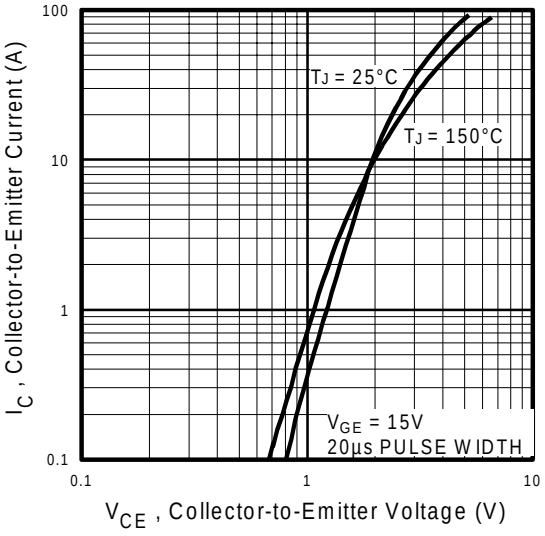


Fig. 2 - Typical Output Characteristics

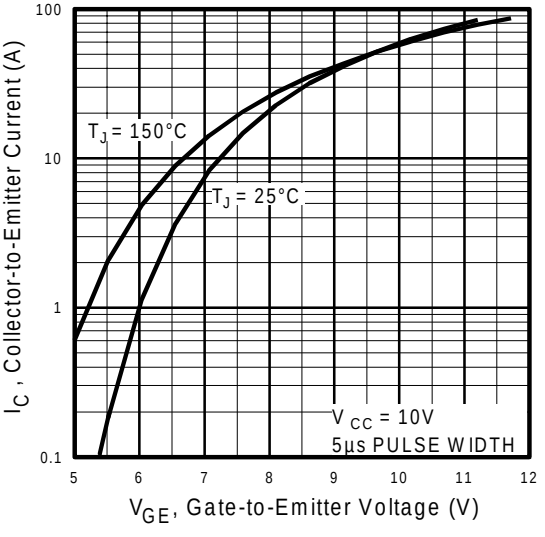


Fig. 3 - Typical Transfer Characteristics

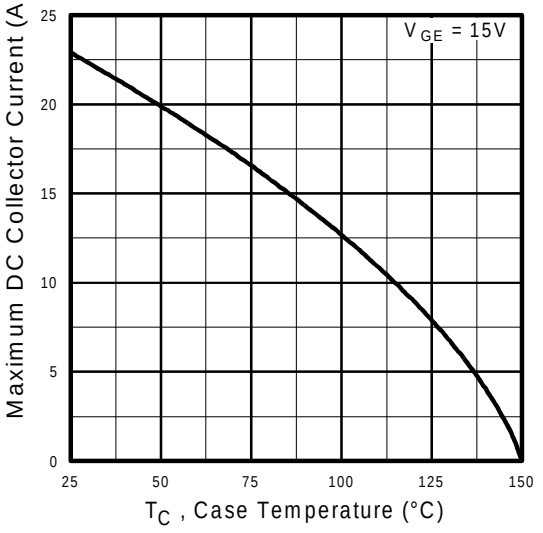


Fig. 4 - Maximum Collector Current vs.Case Temperature

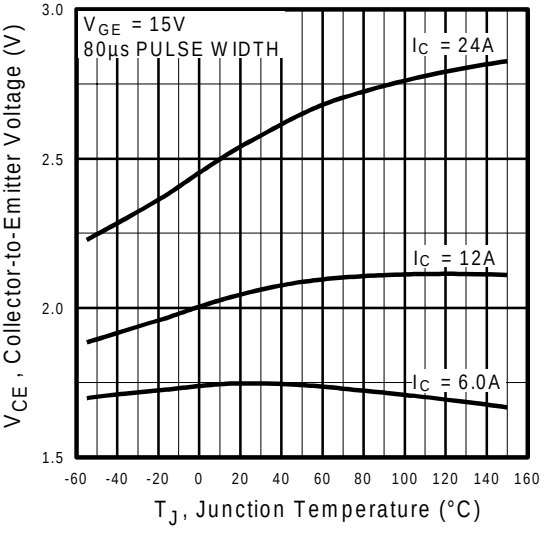


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

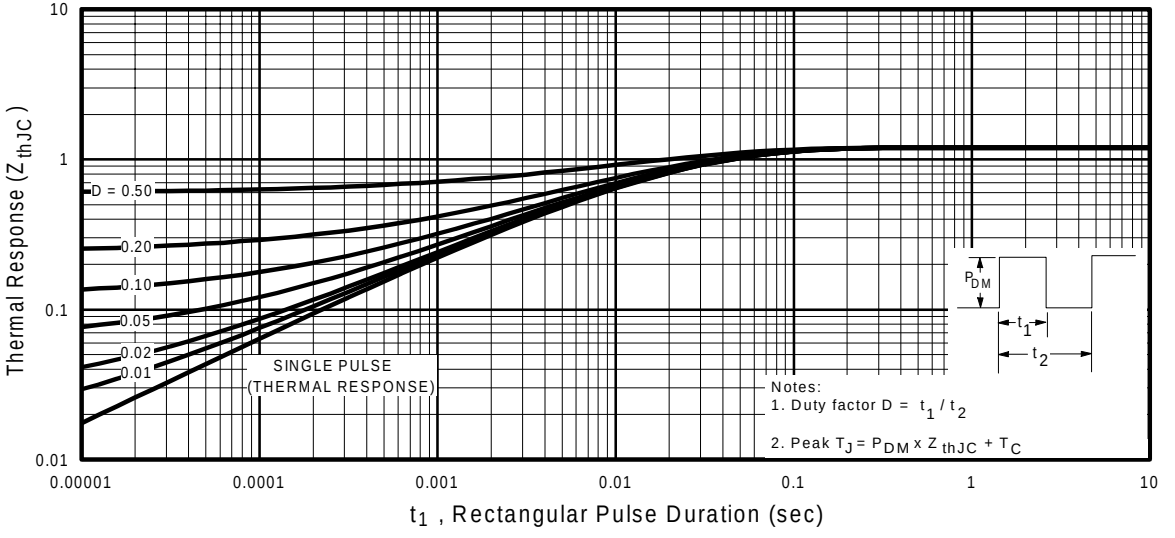


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

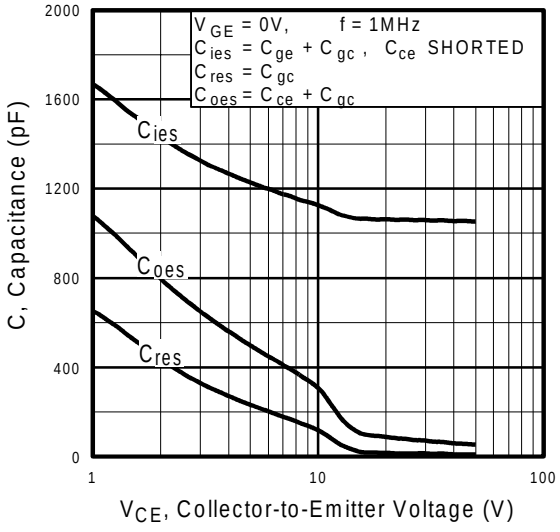


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

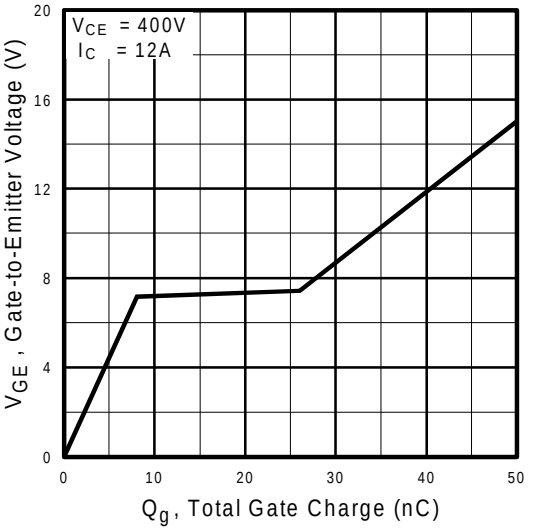


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

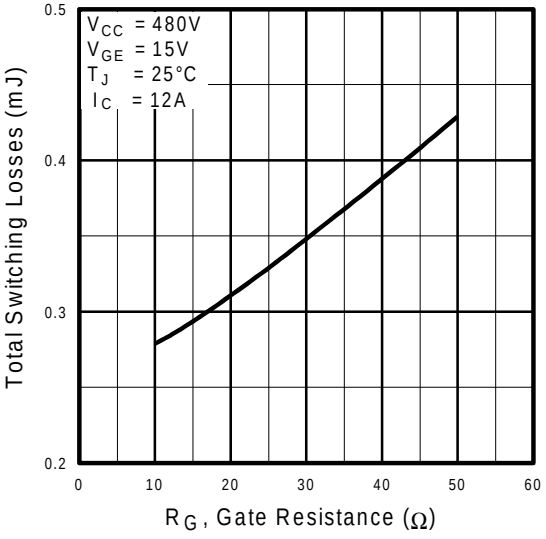


Fig. 9 - Typical Switching Losses vs. Gate Resistance

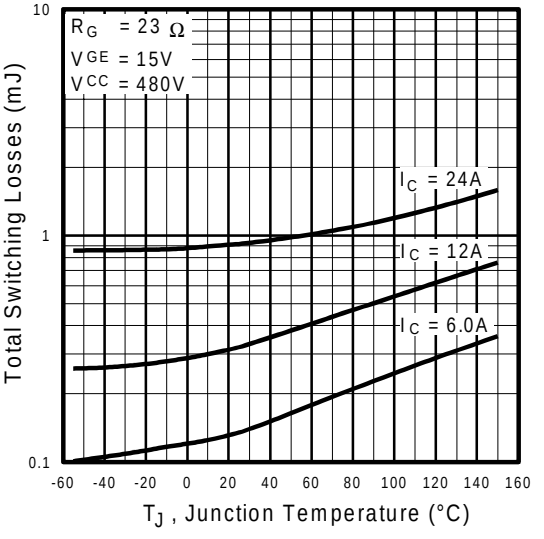


Fig. 10 - Typical Switching Losses vs. Junction Temperature

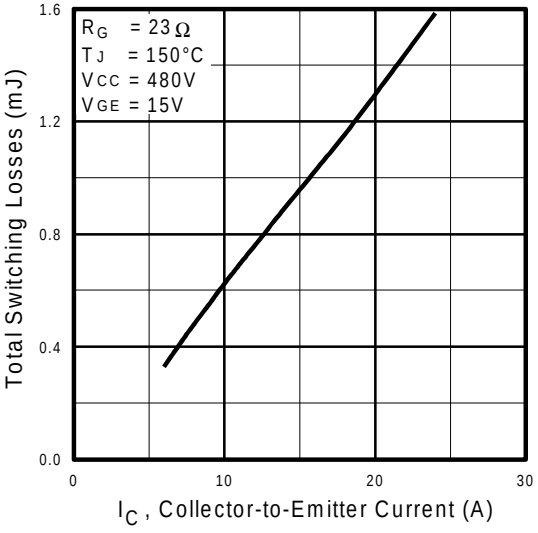


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

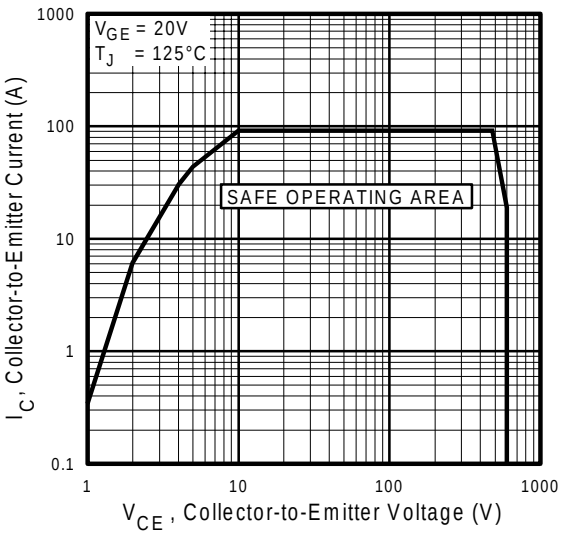


Fig. 12 - Turn-Off SOA

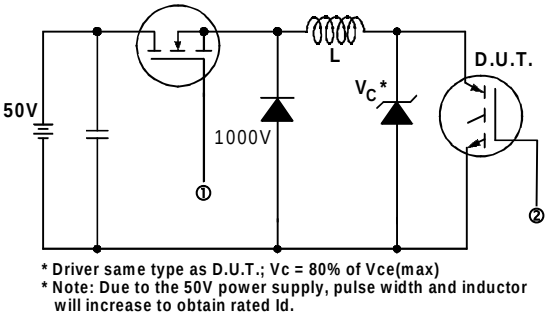


Fig. 13a - Clamped Inductive Load Test Circuit

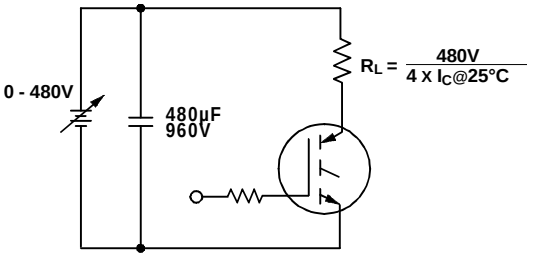


Fig. 13b - Pulsed Collector Current Test Circuit

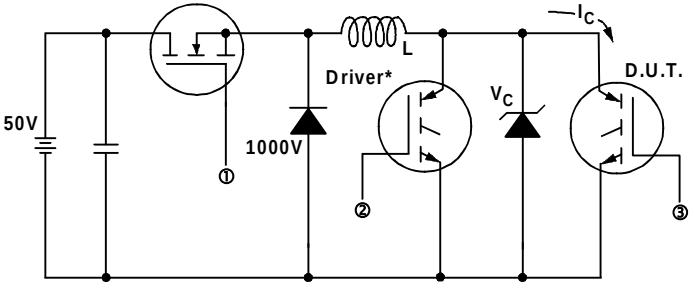


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

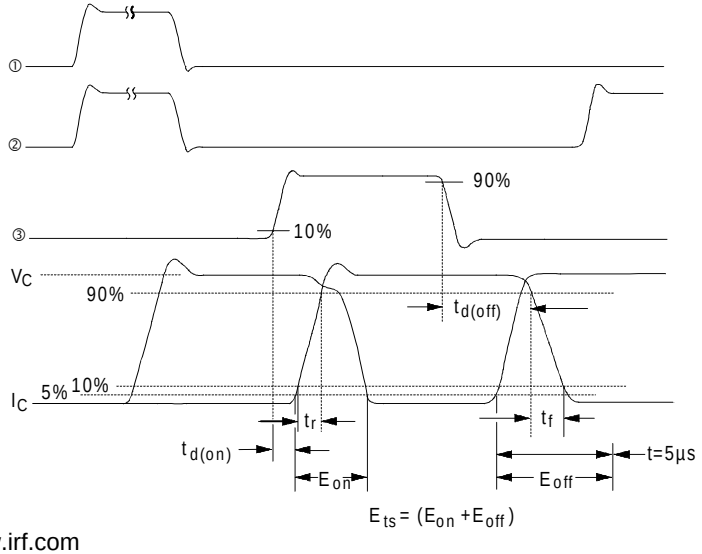
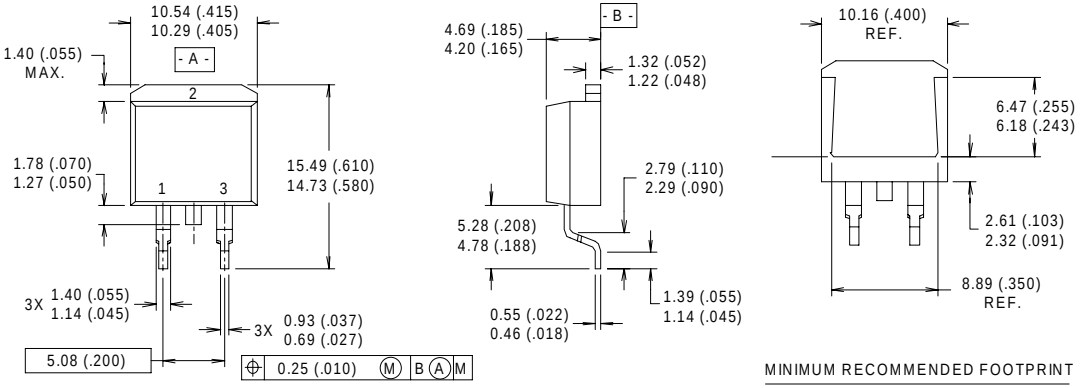


Fig. 14b - Switching Loss Waveforms

D^{2}Pak Package Outline



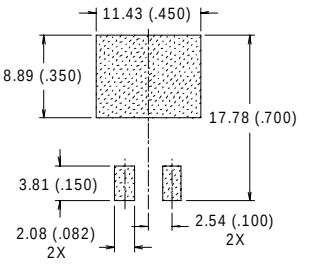
NOTES:

1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

1 - GATE
2 - DRAIN
3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT



International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936
http://www.irf.com/ Data and specifications subject to change without notice. 9/98

International
IOR Rectifier

PD - 91619B

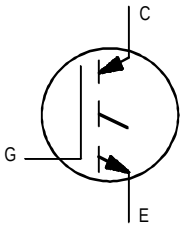
IRG4BC30K-S

Short Circuit Rated
UltraFast IGBT

INSULATED GATE BIPOLAR TRANSISTOR

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, @360V V_{CE} (start), T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Latest generation design provides tighter parameter distribution and higher efficiency than previous generations



n-channel

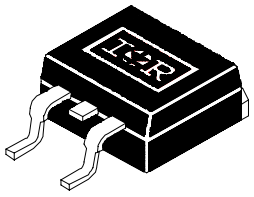
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.21V

@V_{GE} = 15V, I_C = 16A

Benefits

- As a Freewheeling Diode we recommend our HEXFRED™ ultrafast, ultrasoft recovery diodes for minimum EMI / Noise and switching losses in the Diode and IGBT
- Latest generation 4 IGBTs offer highest power density motor controls possible
- This part replaces the IRGBC30K-S and IRGBC30M-S devices



D²Pak

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	28	A
I_C @ T_C = 100°C	Continuous Collector Current	16	
I_{CM}	Pulsed Collector Current ①	58	
I_{LM}	Clamped Inductive Load Current ②	58	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	260	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted,steady-state)⑥	—	40	
Wt	Weight	1.44	—	g

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.54	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.21	—	V	I_C = 14A
		—	2.21	2.7		I_C = 16A V_{GE} = 15V
		—	2.88	—		I_C = 28A See Fig.2, 5
		—	2.36	—		I_C = 16A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-12	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	5.4	8.1	—	S	V_{CE} = 100V, I_C = 16A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1100		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	67	100	nC	I_C = 16A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	11	16		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	25	37		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	26	—	ns	
t_r	Rise Time	—	28	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	130	200		I_C = 16A, V_{CC} = 480V
t_f	Fall Time	—	120	170		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.36	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.51	—		See Fig. 9,10,14
E_{ts}	Total Switching Loss	—	0.87	1.3		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 400V, T_J = 125°C
						V_{GE} = 15V, R_G = 23Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	T_J = 150°C,
t_r	Rise Time	—	29	—		I_C = 16A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	190	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	190	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.2	—	mJ	See Fig. 11,14
E_{on}	Turn-On Switching Loss	—	0.26	—	mJ	T_J = 25°C, V_{GE} = 15V, R_G = 23Ω
E_{off}	Turn-Off Switching Loss	—	0.36	—		I_C = 14A, V_{CC} = 480V
E_{ts}	Total Switching Loss	—	0.62	—		Energy losses include "tail"
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	920	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	110	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	27	—		f = 1.0MHz

Details of note ① through ⑥ are on the last page

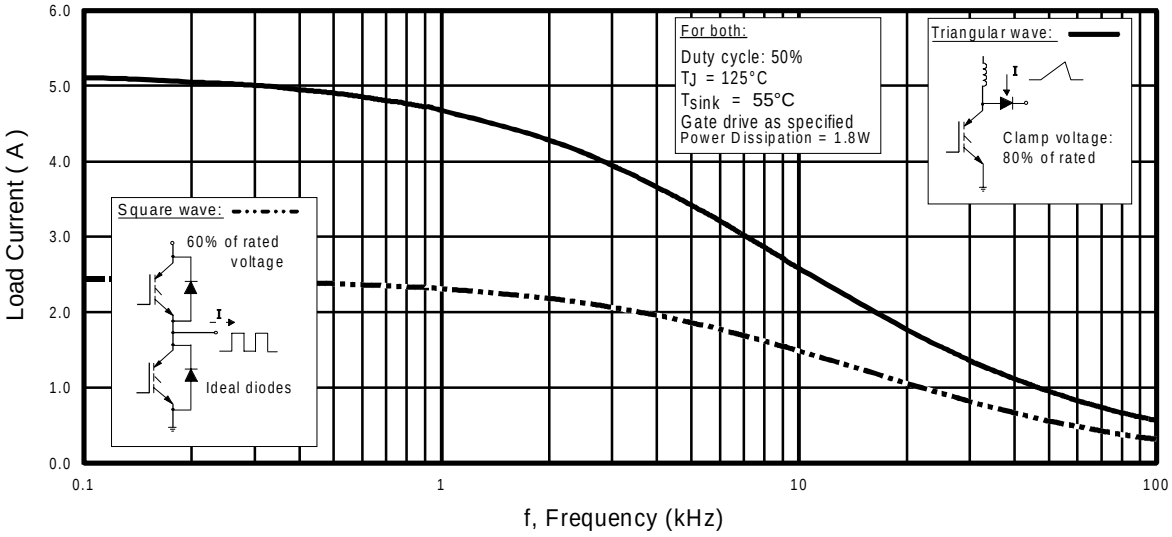


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

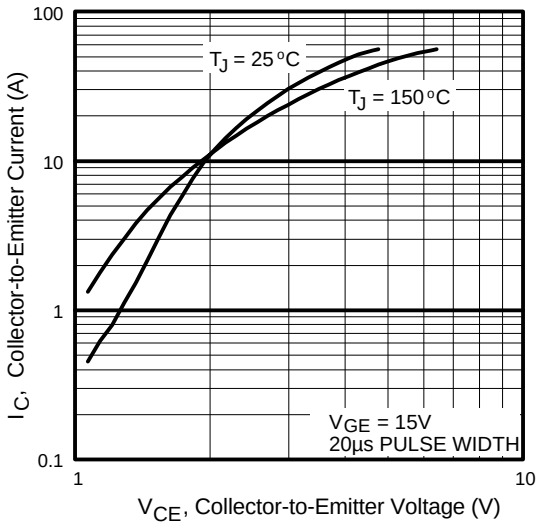


Fig. 2 - Typical Output Characteristics

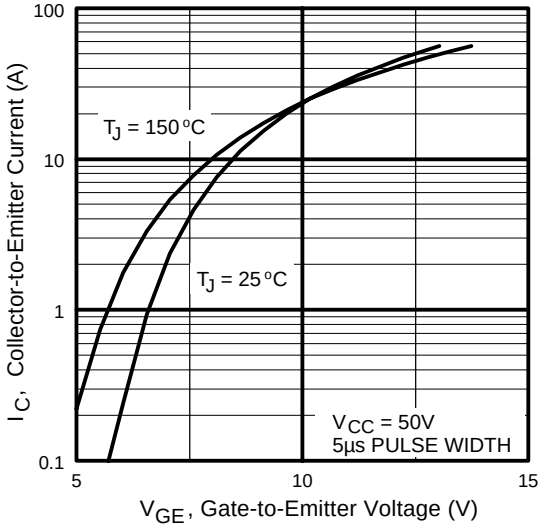


Fig. 3 - Typical Transfer Characteristics

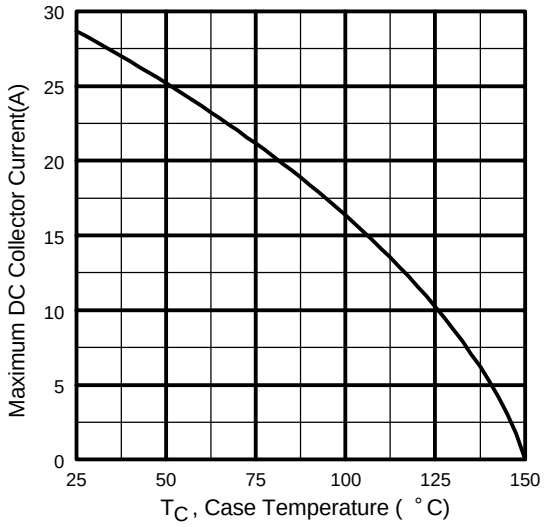


Fig. 4 - Maximum Collector Current vs. Case Temperature

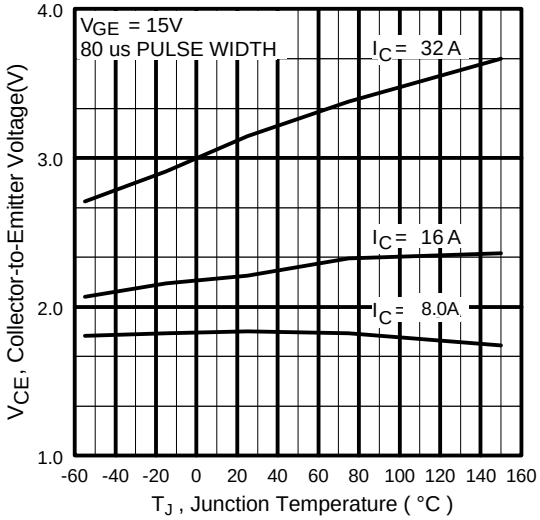


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

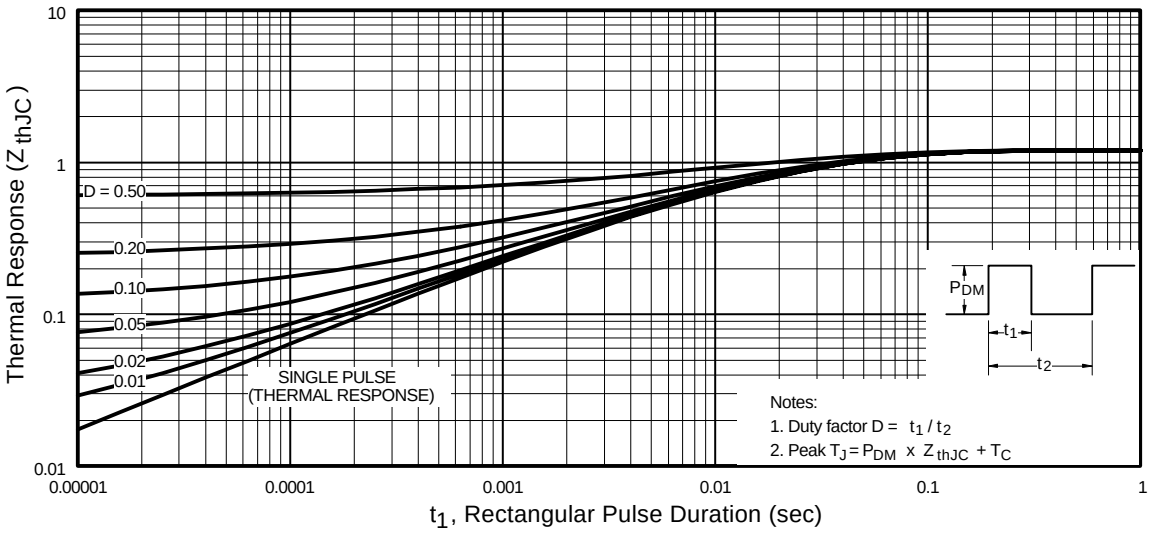


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

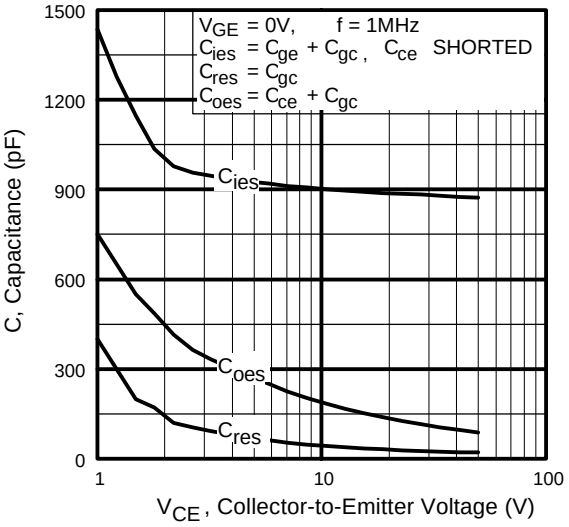


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

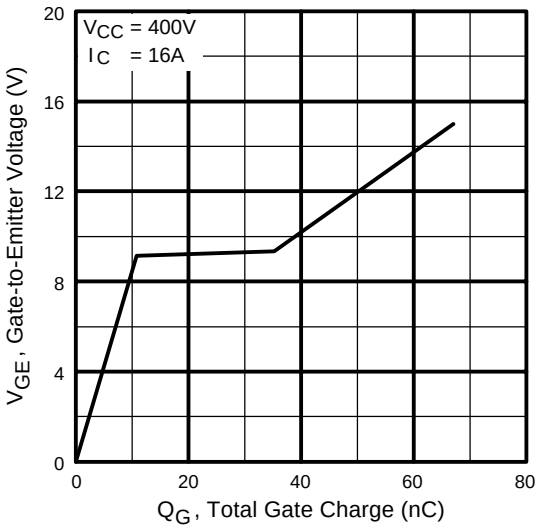


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

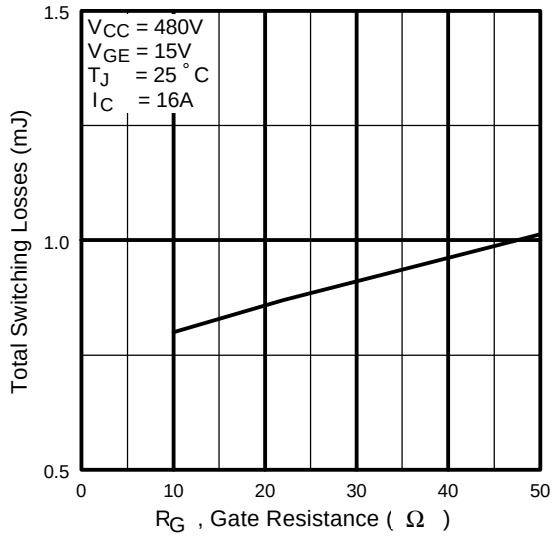


Fig. 9 - Typical Switching Losses vs. Gate Resistance

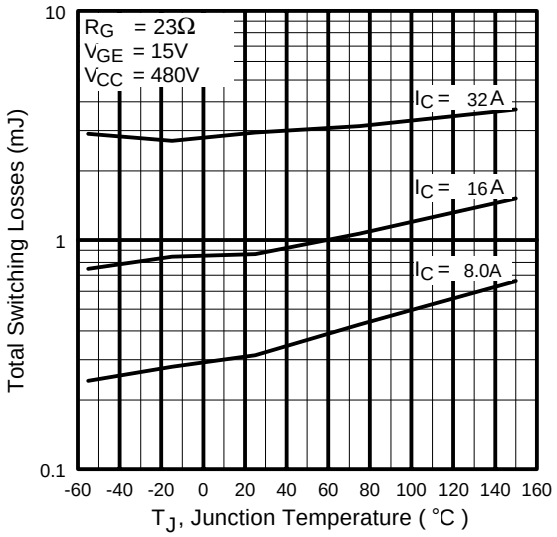


Fig. 10 - Typical Switching Losses vs. Junction Temperature

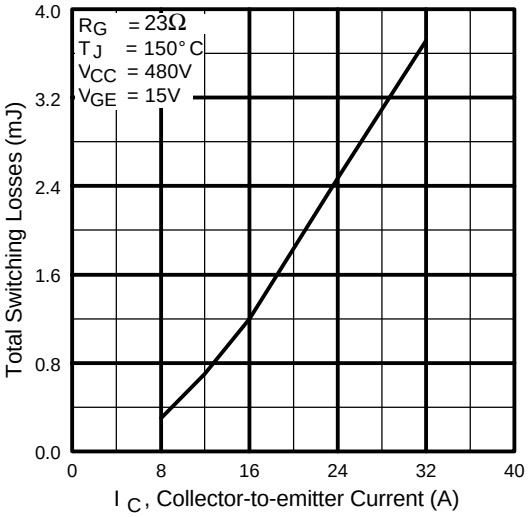


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

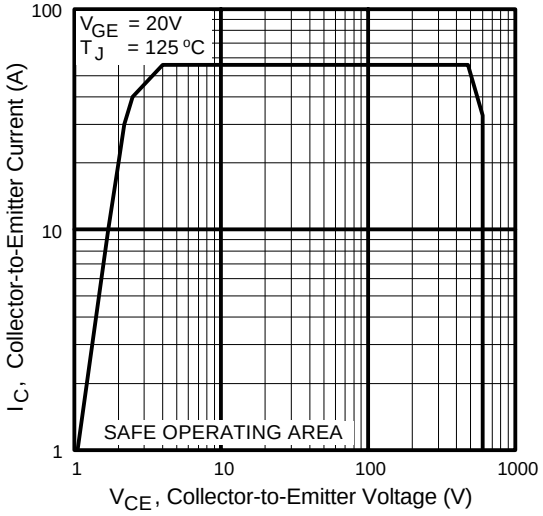
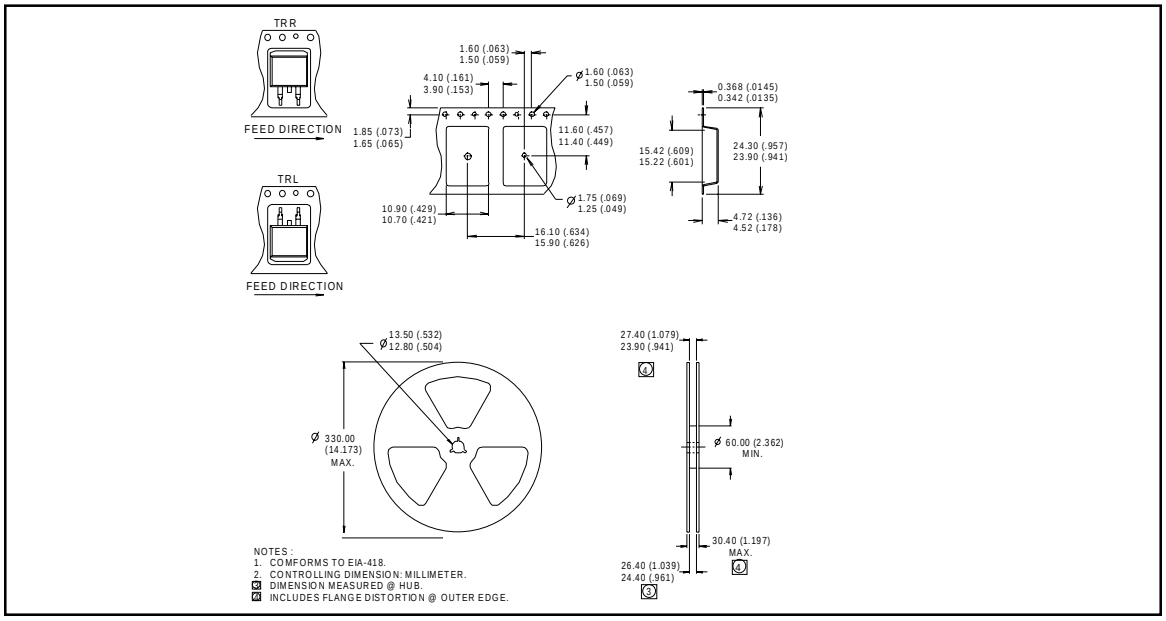


Fig. 12 - Turn-Off SOA

Tape & Reel Information

D²Pak



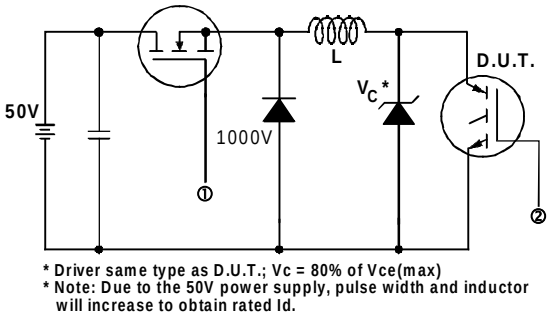


Fig. 13a - Clamped Inductive Load Test Circuit

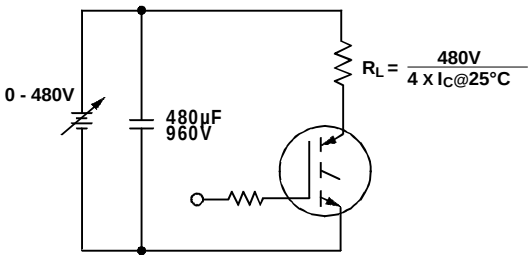


Fig. 13b - Pulsed Collector Current Test Circuit

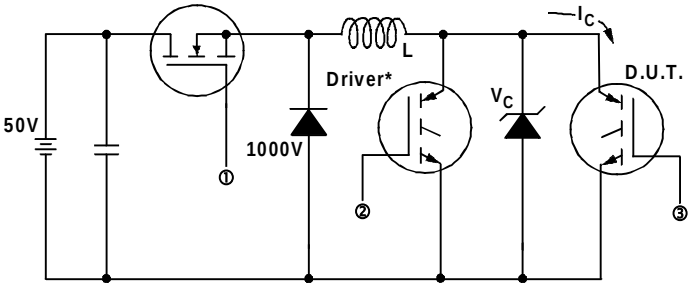


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

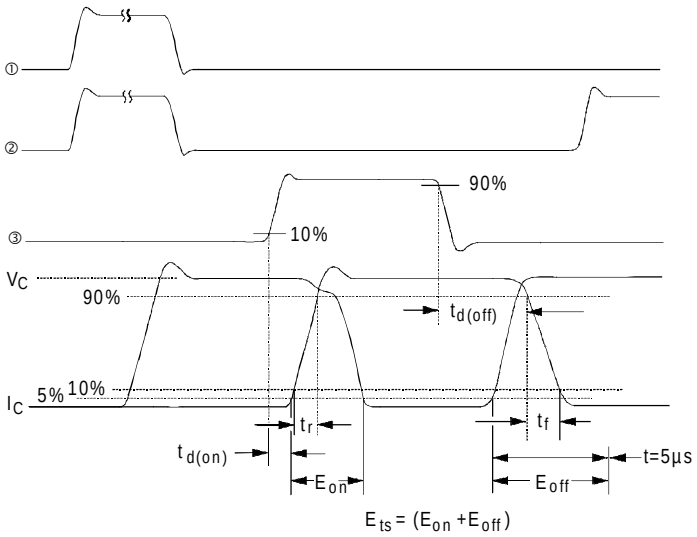


Fig. 14b - Switching Loss Waveforms

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 23Ω, (See fig. 13a)

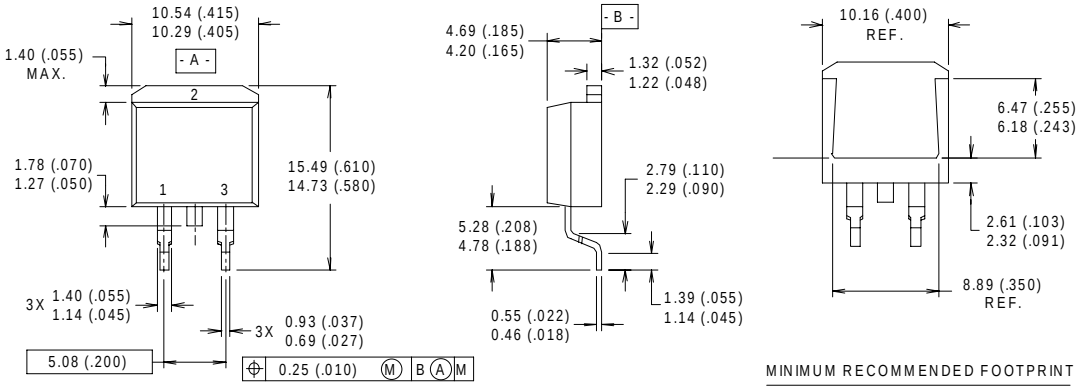
③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

⑥ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

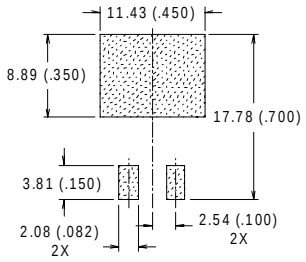
D²Pak Package Outline



NOTES:
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT



International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 10/00

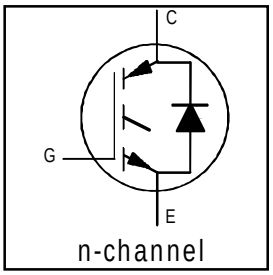
PD -91594C

International
IOR Rectifier

IRG4BC30KD-S

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

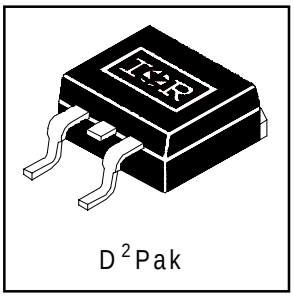
Short Circuit Rated
UltraFast IGBT



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.21V

@V_{GE} = 15V, I_C = 16A



Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, @360V V_{CE} (start), T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- tighter parameter distribution and higher efficiency than previous generations
- IGBT co-packaged with HEXFRED™ ultrafast, ultrasoft recovery antiparallel diodes

Benefits

- Latest generation 4 IGBTs offer highest power density motor controls possible
- HEXFRED™ diodes optimized for performance with IGBTs. Minimized recovery characteristic reduce noise, EMI and switching losses
- This part replaces the IRGBC30KD2-S and IRGBC30MD2-S products
- For hints see design tip 97003

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	28	A
I_C @ T_C = 100°C	Continuous Collector Current	16	
I_{CM}	Pulsed Collector Current ①	58	
I_{LM}	Clamped Inductive Load Current ②	58	
I_F @ T_C = 100°C	Diode Continuous Forward Current	12	
I_{FM}	Diode Maximum Forward Current	58	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	1.2	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode		2.5	
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted,steady-state)⑤	—	40	
Wt	Weight	1.44	—	g

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.54	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.21	2.7	V	I_C = 16A V_{GE} = 15V
		—	2.88	—		I_C = 28A See Fig. 2, 5
		—	2.36	—		I_C = 16A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-12	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	5.4	8.1	—	S	V_{CE} = 100V, I_C = 16A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 12A See Fig. 13
		—	1.3	1.6		I_C = 12A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	67	100	nC	I_C = 16A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	11	16		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	25	37		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	60	—	ns	
t_r	Rise Time	—	42	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	160	250		I_C = 16A, V_{CC} = 480V
t_f	Fall Time	—	80	120		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.60	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.58	—		and diode reverse recovery
E_{ts}	Total Switching Loss	—	1.18	1.6		See Fig. 9,10,14
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 360V, T_J = 125°C
						V_{GE} = 15V, R_G = 10Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	58	—	ns	T_J = 150°C, See Fig. 11,14
t_r	Rise Time	—	42	—		I_C = 16A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	210	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	160	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.69	—	mJ	and diode reverse recovery
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	920	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	110	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	27	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	42	60	ns	T_J = 25°C See Fig. 14 — I_F = 12A
		—	80	120		T_J = 125°C
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	6.0	A	T_J = 25°C See Fig. 15 — V_R = 200V
		—	5.6	10		T_J = 125°C
Q_{rr}	Diode Reverse Recovery Charge	—	80	180	nC	T_J = 25°C See Fig. 16 — di/dt = 200Aµs
		—	220	600		T_J = 125°C
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	180	—	A/µs	T_J = 25°C See Fig. 17
	During t_b	—	160	—		T_J = 125°C

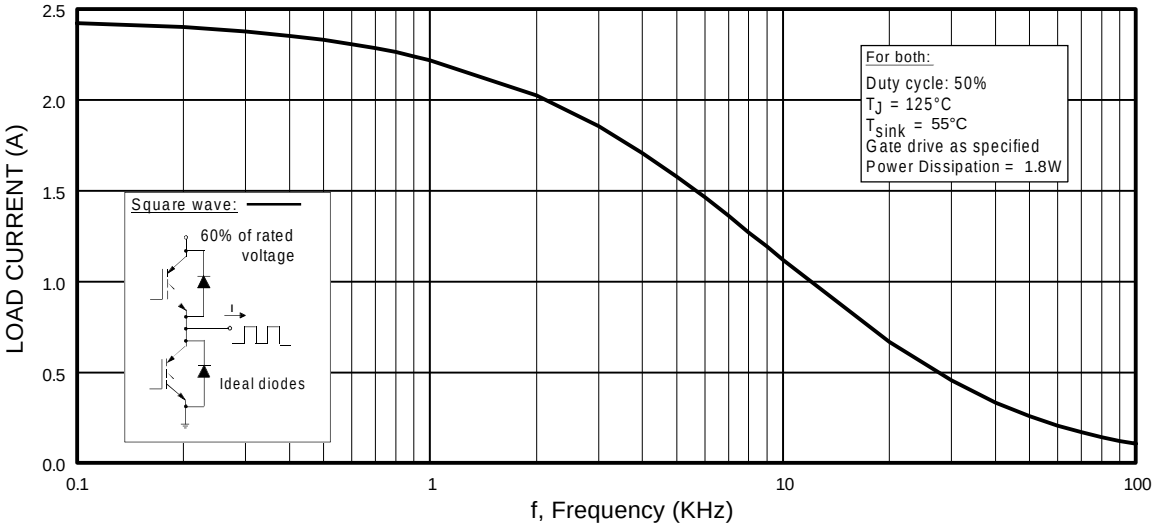


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

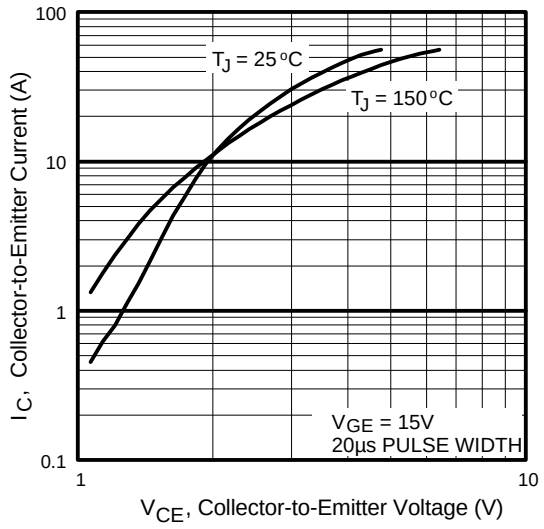


Fig. 2 - Typical Output Characteristics

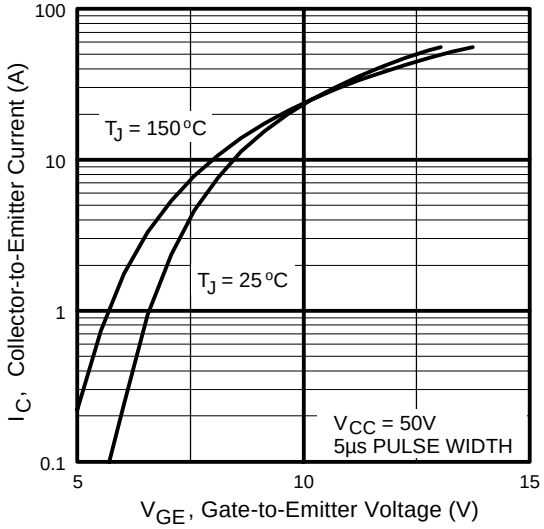


Fig. 3 - Typical Transfer Characteristics

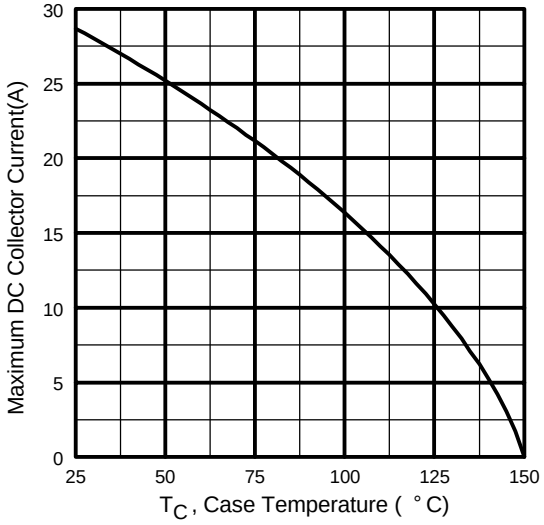


Fig. 4 - Maximum Collector Current vs. Case Temperature

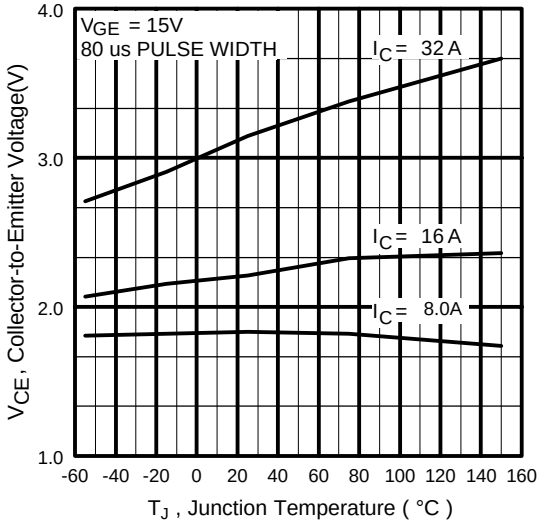


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

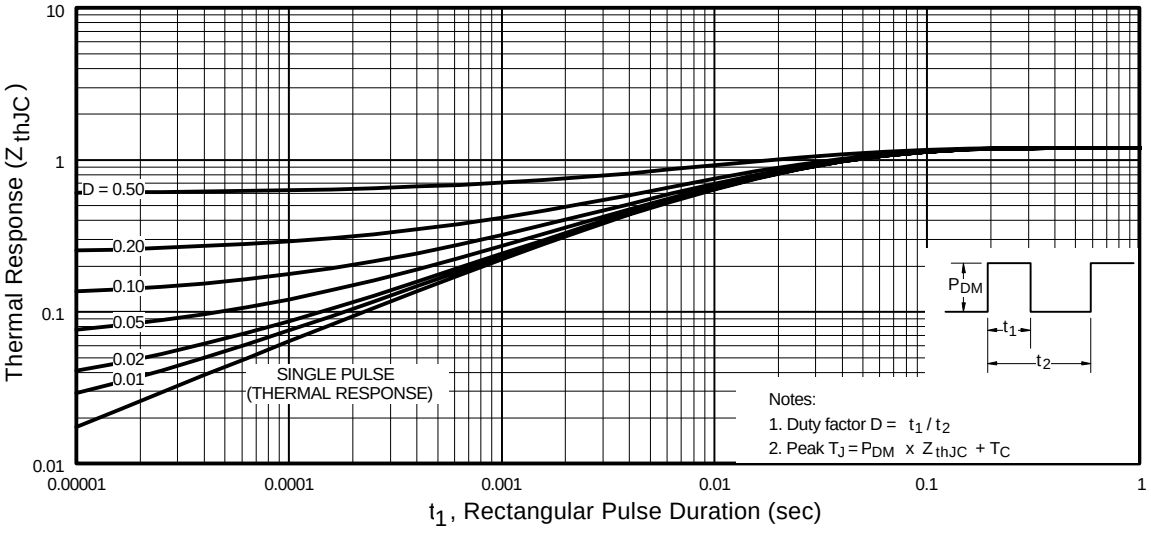


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

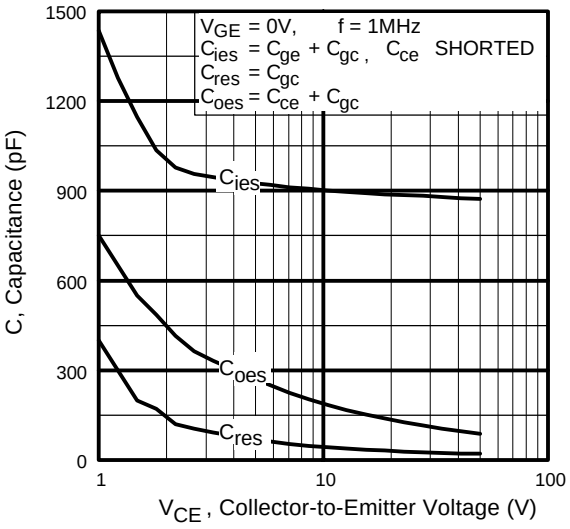


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

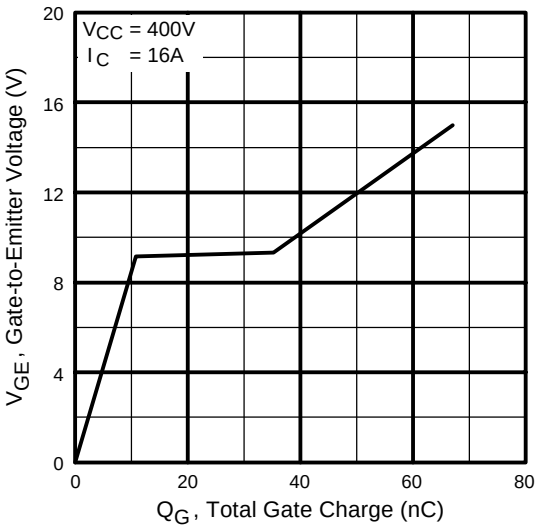


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

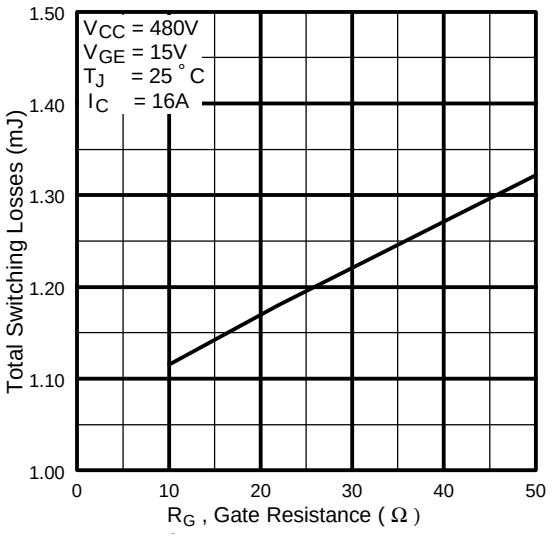


Fig. 9 - Typical Switching Losses vs. Gate Resistance

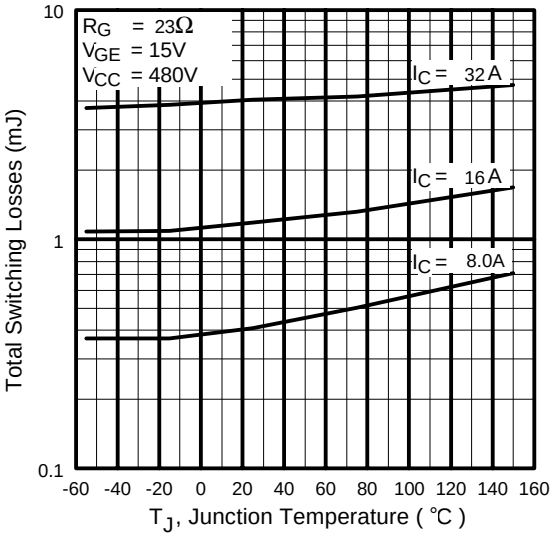


Fig. 10 - Typical Switching Losses vs. Junction Temperature

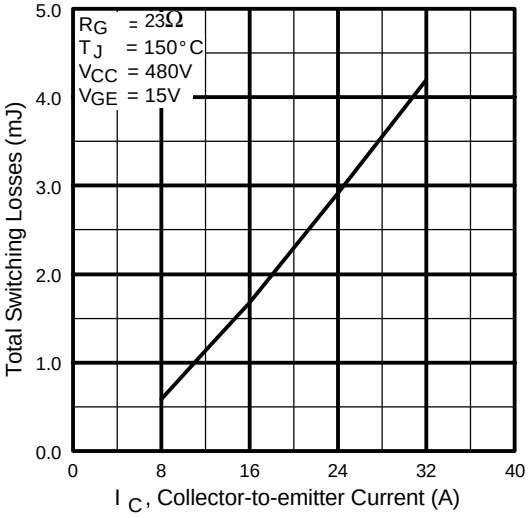


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

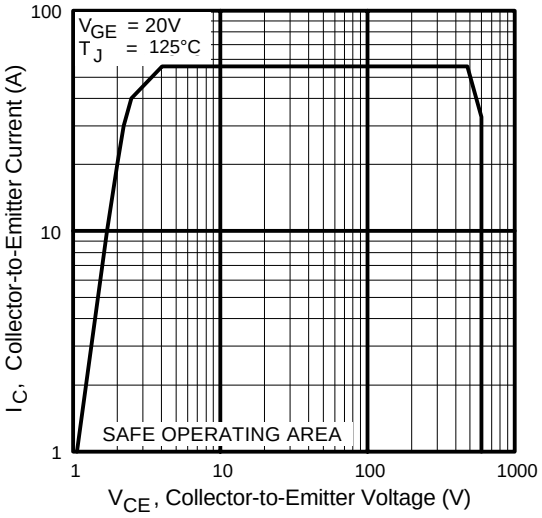


Fig. 12 - Turn-Off SOA

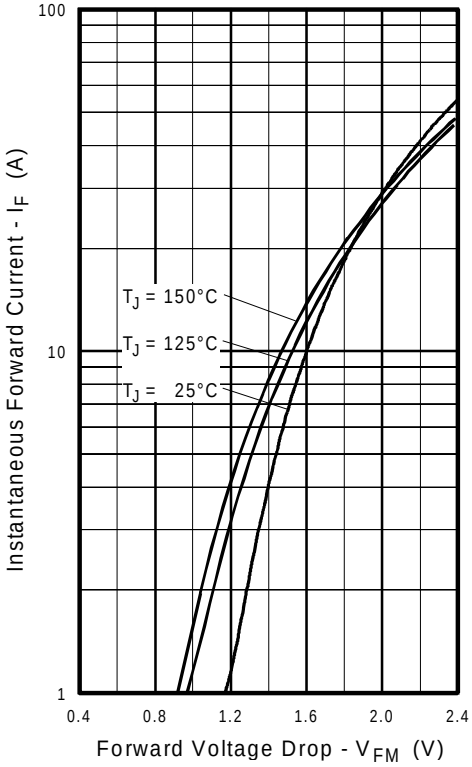


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

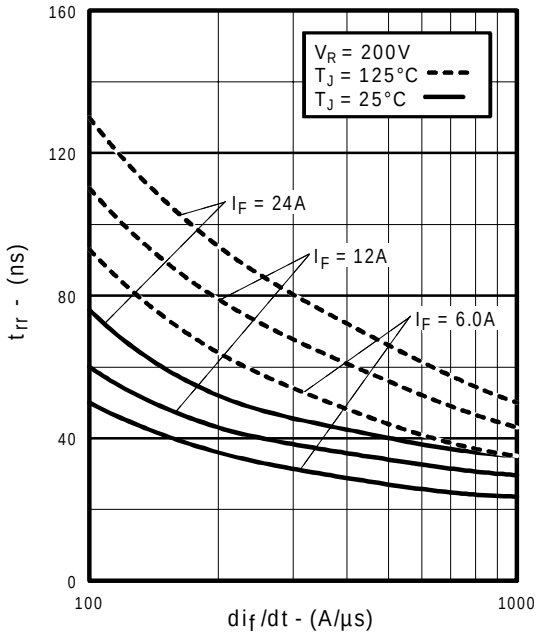


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

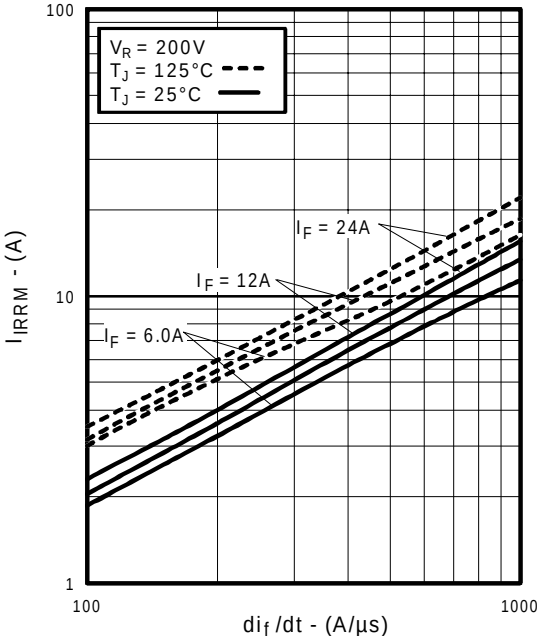


Fig. 15 - Typical Recovery Current vs. di_f/dt

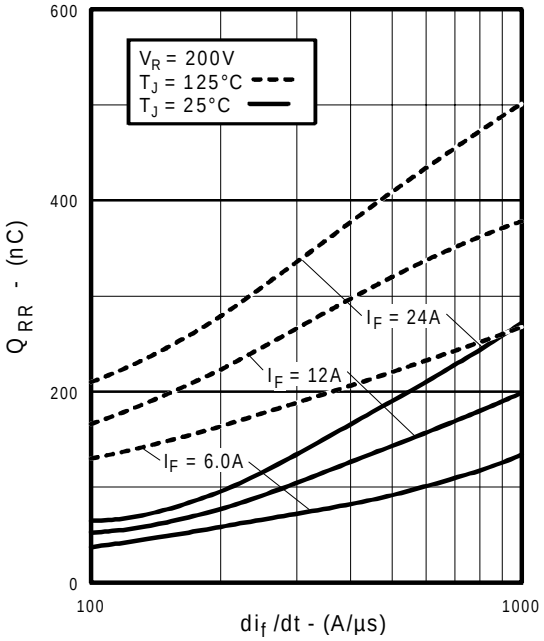


Fig. 16 - Typical Stored Charge vs. di_f/dt

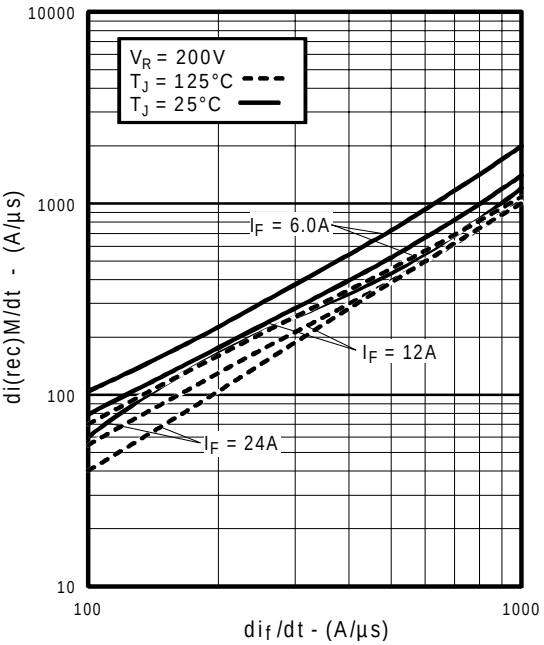


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

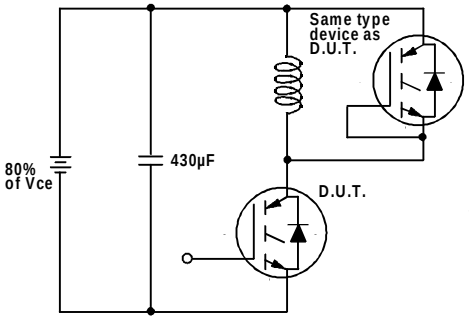


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

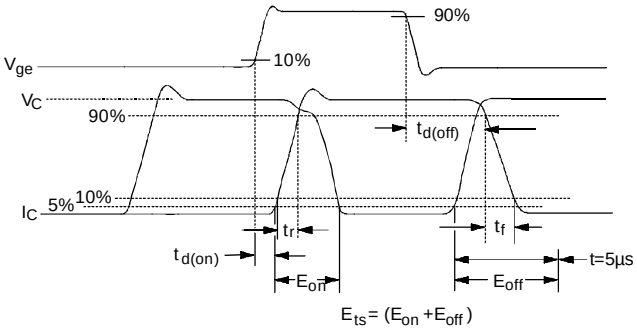


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

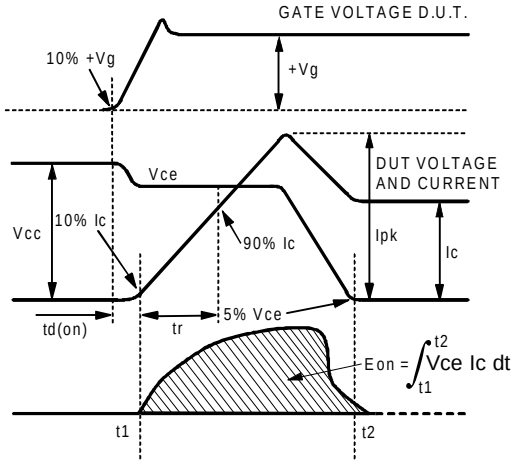


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

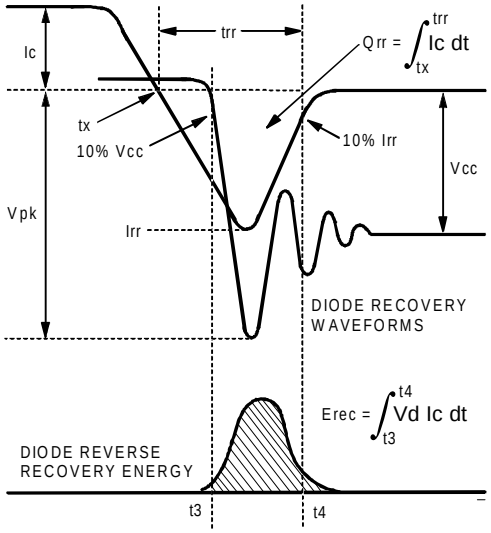


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

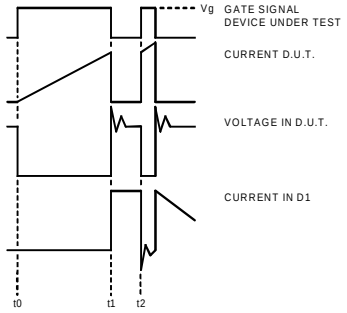


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

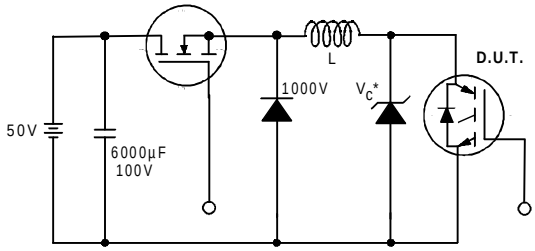


Figure 19. Clamped Inductive Load Test Circuit

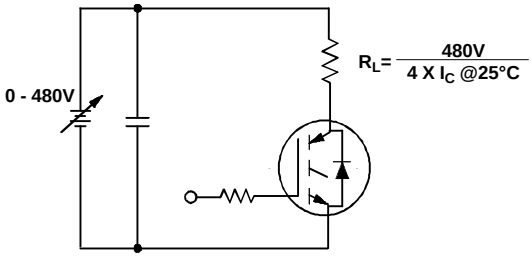
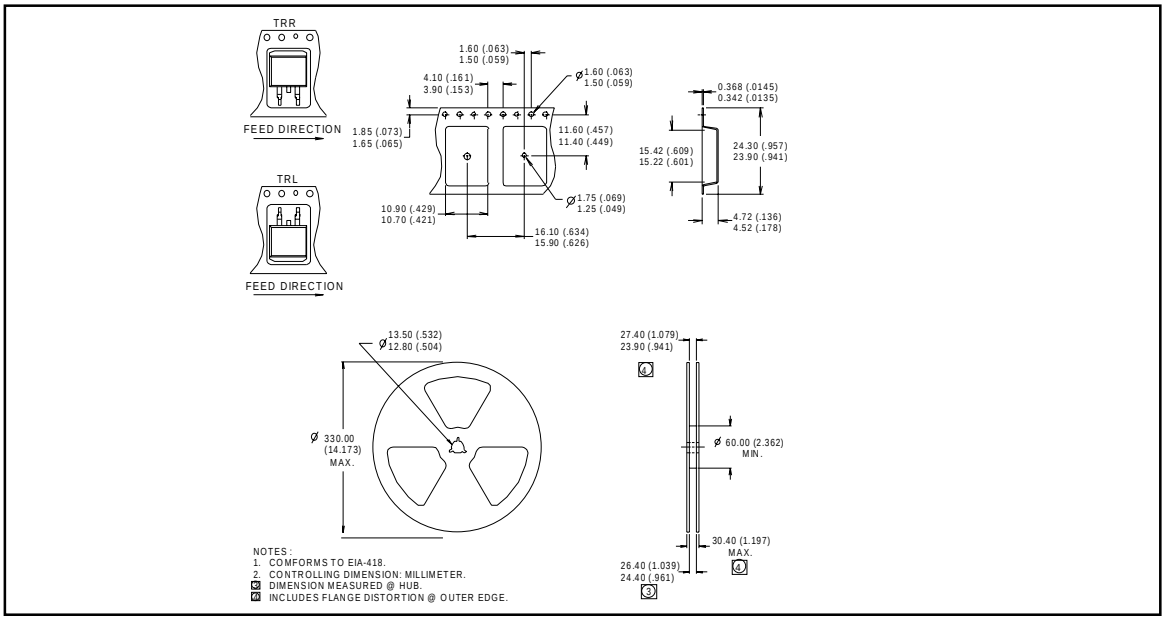


Figure 20. Pulsed Collector Current Test Circuit

Tape & Reel Information

D^2Pak



Notes:

① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

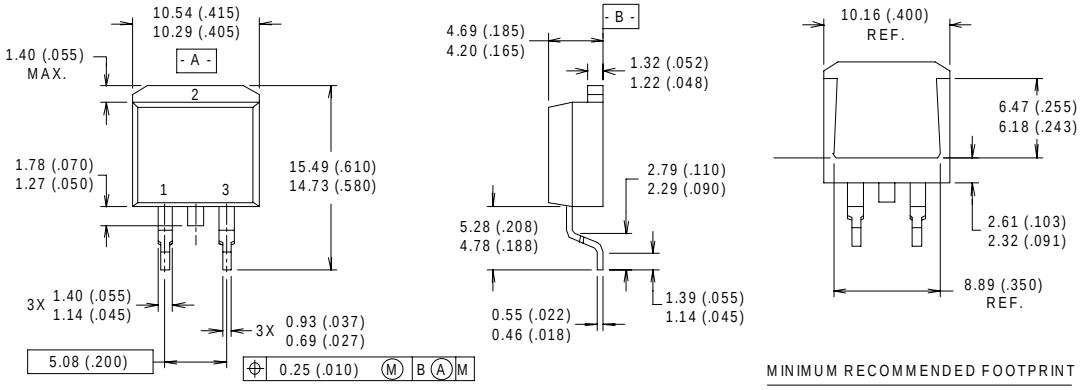
② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 23Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

⑤ When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

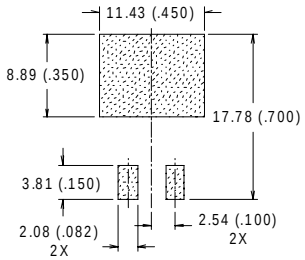
D²Pak Package Outline



NOTES:
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT



International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 10/00

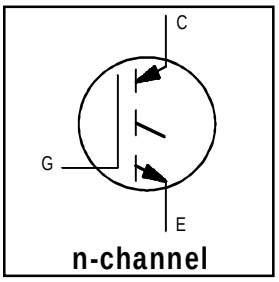
International
IOR Rectifier

PD - 91596A

IRG4BC30K

Short Circuit Rated
UltraFast IGBT

INSULATED GATE BIPOLAR TRANSISTOR



n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.21V

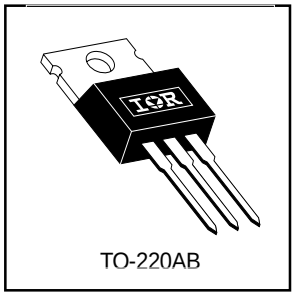
@V_{GE} = 15V, I_C = 16A

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, @360V V_{CE} (start), T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Latest generation design provides tighter parameter distribution and higher efficiency than previous generations

Benefits

- As a Freewheeling Diode we recommend our HEXFRED™ ultrafast, ultrasoft recovery diodes for minimum EMI / Noise and switching losses in the Diode and IGBT
- Latest generation 4 IGBTs offer highest power density motor controls possible
- This part replaces the IRGBC30K and IRGBC30M devices



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	28	A
I_C @ T_C = 100°C	Continuous Collector Current	16	
I_{CM}	Pulsed Collector Current ①	58	
I_{LM}	Clamped Inductive Load Current ②	58	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	260	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	80	
Wt	Weight	1.44	—	g

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.54	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.21	—	V	I_C = 14A
		—	2.21	2.7		I_C = 16A — V_{GE} = 15V
		—	2.88	—		I_C = 28A — See Fig.2, 5
		—	2.36	—		I_C = 16A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-12	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	5.4	8.1	—	S	V_{CE} = 100V, I_C = 16A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1100		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	67	100	nC	I_C = 16A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	11	16		V_{CC} = 400V — See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	25	37		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	26	—	ns	
t_r	Rise Time	—	28	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	130	200		I_C = 16A, V_{CC} = 480V
t_f	Fall Time	—	120	170		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.36	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.51	—		See Fig. 9,10,14
E_{ts}	Total Switching Loss	—	0.87	1.3		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 400V, T_J = 125°C
						V_{GE} = 15V, R_G = 23Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	T_J = 150°C,
t_r	Rise Time	—	29	—		I_C = 16A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	190	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	190	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.2	—	mJ	See Fig. 11,14
E_{on}	Turn-On Switching Loss	—	0.26	—		T_J = 25°C, V_{GE} = 15V, R_G = 23Ω
E_{off}	Turn-Off Switching Loss	—	0.36	—		I_C = 14A, V_{CC} = 480V
E_{ts}	Total Switching Loss	—	0.62	—		Energy losses include "tail"
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	920	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	110	—		V_{CC} = 30V — See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	27	—		f = 1.0MHz

Details of note ① through ⑤ are on the last page

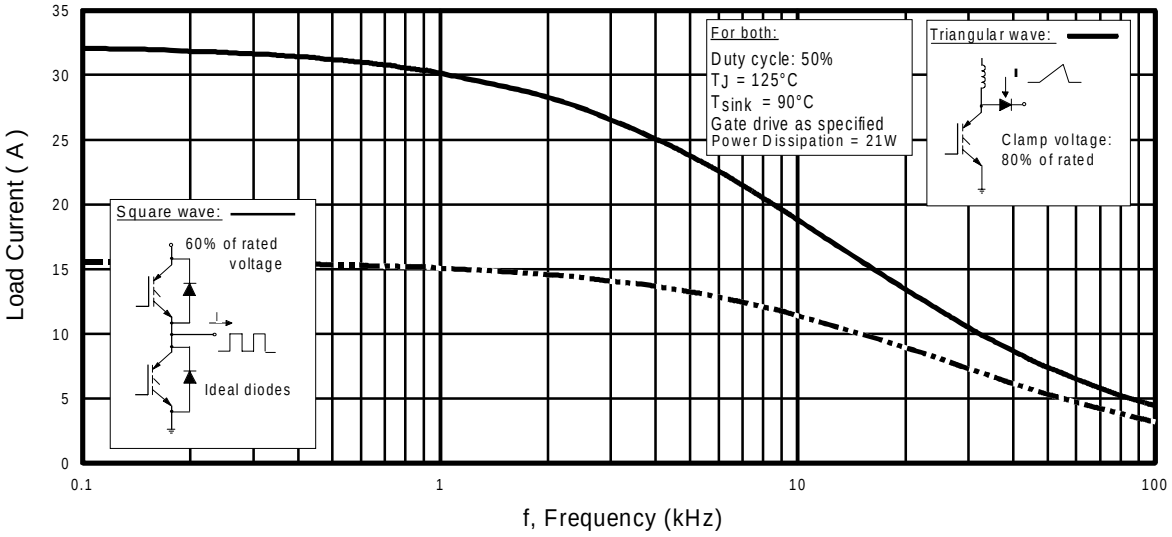


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

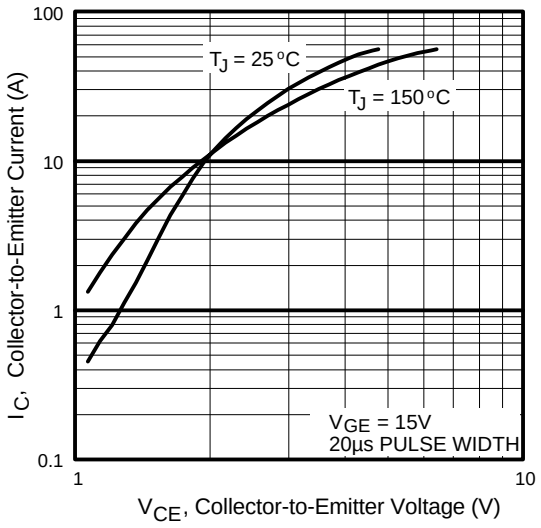


Fig. 2 - Typical Output Characteristics

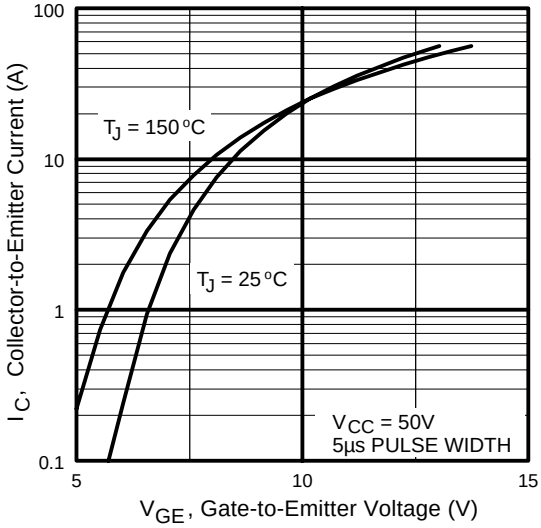


Fig. 3 - Typical Transfer Characteristics

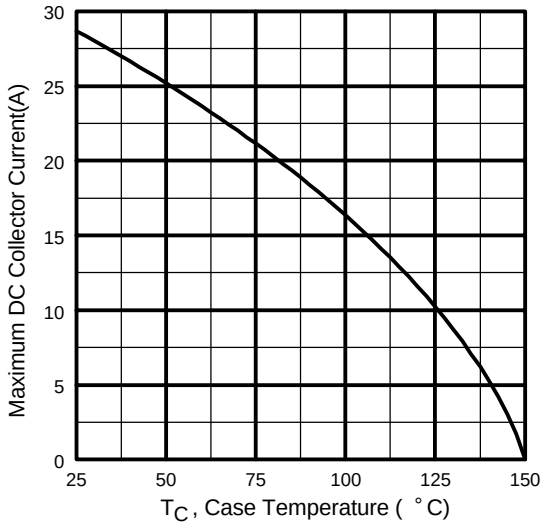


Fig. 4 - Maximum Collector Current vs. Case Temperature

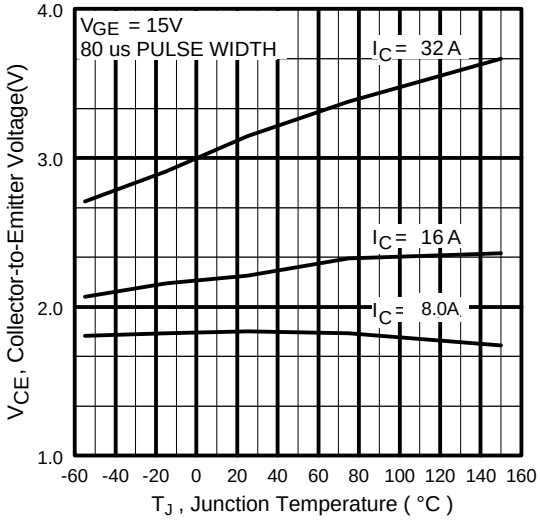


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

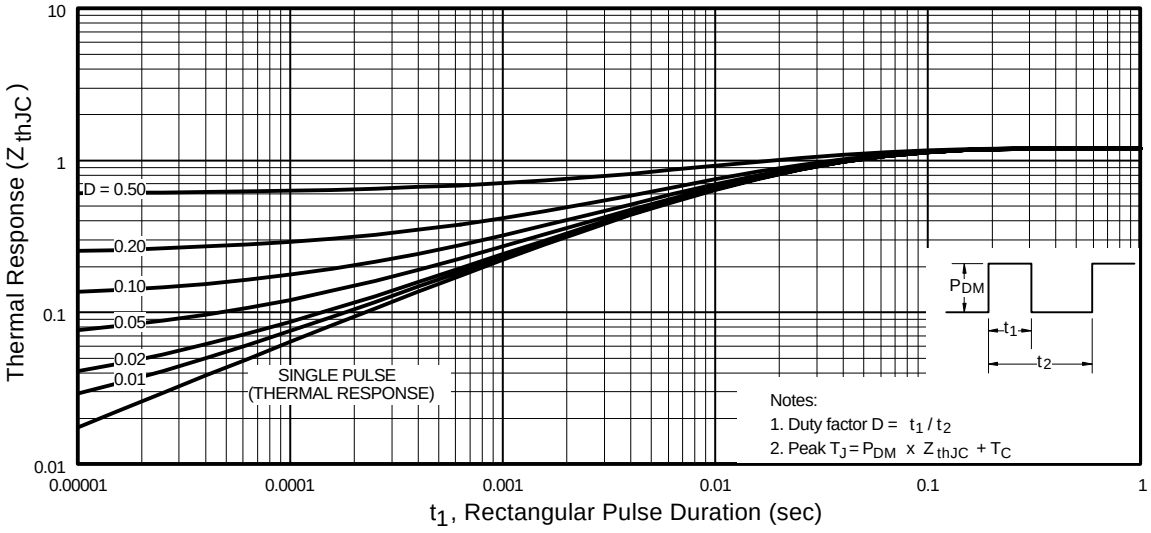


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

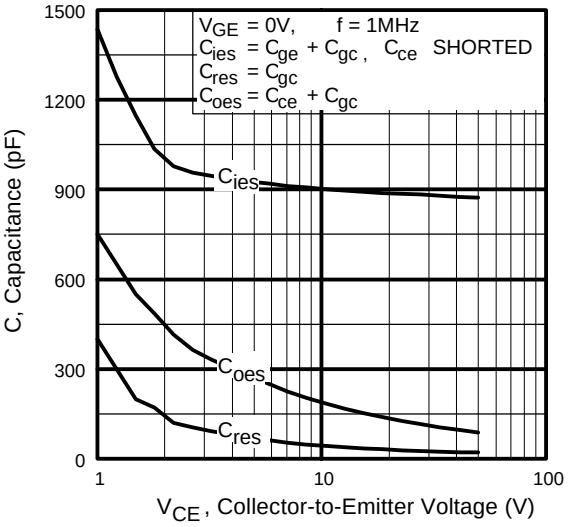


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

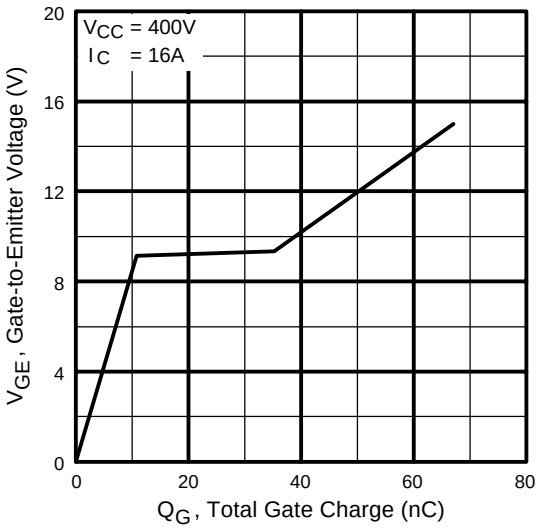


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

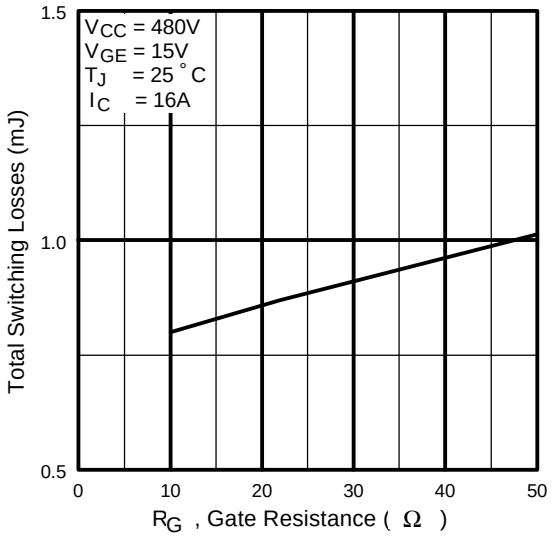


Fig. 9 - Typical Switching Losses vs. Gate Resistance

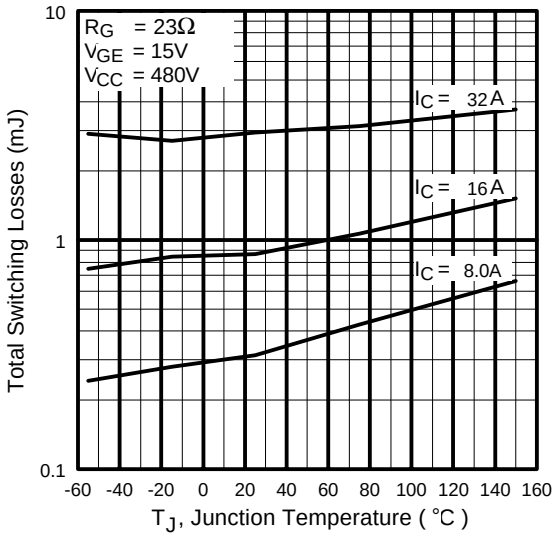


Fig. 10 - Typical Switching Losses vs. Junction Temperature

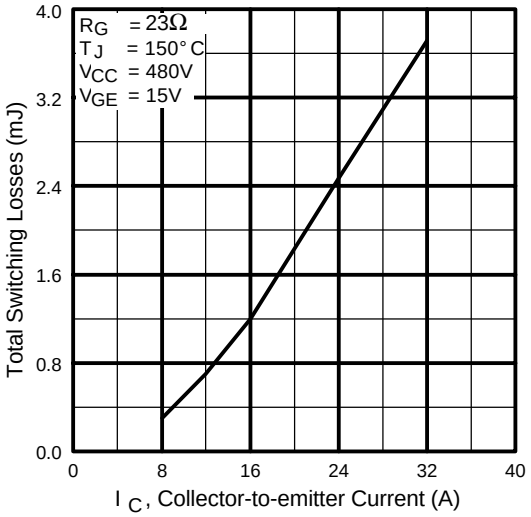


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

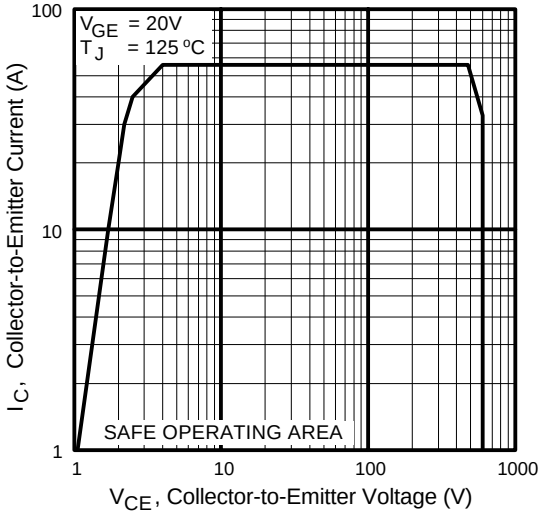


Fig. 12 - Turn-Off SOA

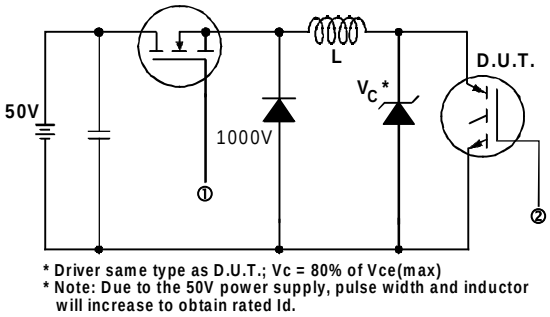


Fig. 13a - Clamped Inductive Load Test Circuit

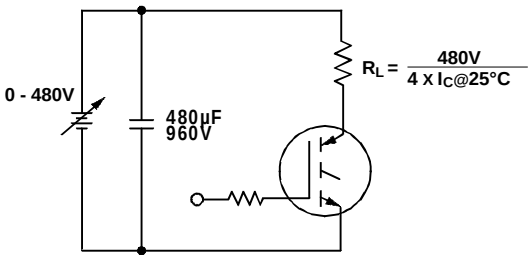


Fig. 13b - Pulsed Collector Current Test Circuit

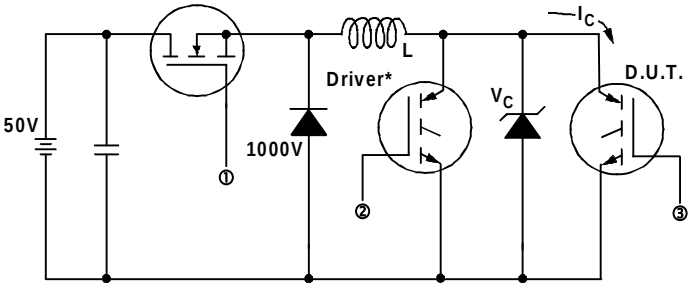


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

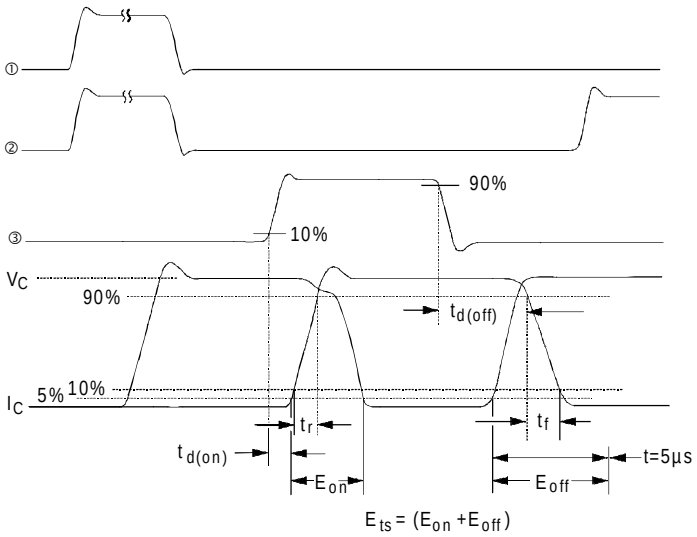


Fig. 14b - Switching Loss Waveforms

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

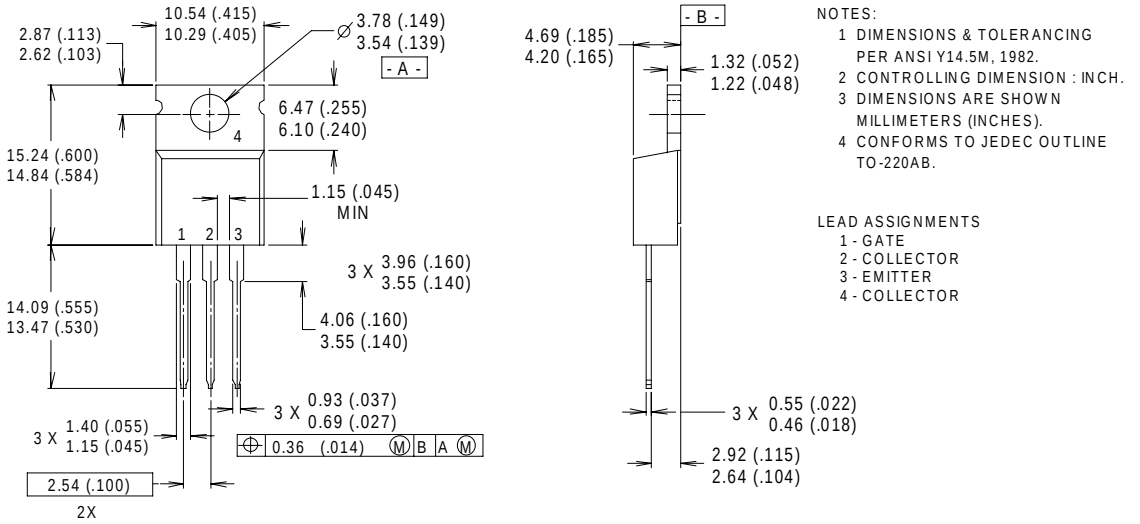
② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 23Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

Case Outline and Dimensions — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB

Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

Data and specifications subject to change without notice. 10/00

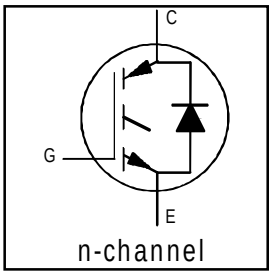
PD -91595A

International
IOR Rectifier

IRG4BC30KD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
UltraFast IGBT



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.21V

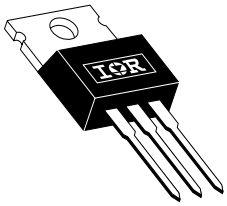
@V_{GE} = 15V, I_C = 16A

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, @360V V_{CE} (start), T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- tighter parameter distribution and higher efficiency than previous generations
- IGBT co-packaged with HEXFRED™ ultrafast, ultrasoft recovery antiparallel diodes

Benefits

- Latest generation 4 IGBTs offer highest power density motor controls possible
- HEXFRED™ diodes optimized for performance with IGBTs. Minimized recovery characteristics reduce noise, EMI and switching losses
- This part replaces the IRGBC30KD2 and IRGBC30MD2 products
- For hints see design tip 97003



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	28	A
I_C @ T_C = 100°C	Continuous Collector Current	16	
I_{CM}	Pulsed Collector Current ①	58	
I_{LM}	Clamped Inductive Load Current ②	58	
I_F @ T_C = 100°C	Diode Continuous Forward Current	12	
I_{FM}	Diode Maximum Forward Current	58	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	1.2	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	2.5	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	80	
Wt	Weight	—	2 (0.07)	—	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.54	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.21	2.7	V	I_C = 16A V_{GE} = 15V
		—	2.88	—		I_C = 28A See Fig. 2, 5
		—	2.36	—		I_C = 16A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-12	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	5.4	8.1	—	S	V_{CE} = 100V, I_C = 16A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 12A See Fig. 13
		—	1.3	1.6		I_C = 12A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	67	100	nC	I_C = 16A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	11	16		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	25	37		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	60	—	ns	
t_r	Rise Time	—	42	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	160	250		I_C = 16A, V_{CC} = 480V
t_f	Fall Time	—	80	120		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.60	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.58	—		and diode reverse recovery
E_{ts}	Total Switching Loss	—	1.18	1.6		See Fig. 9,10,14
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 360V, T_J = 125°C
						V_{GE} = 15V, R_G = 10Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	58	—	ns	T_J = 150°C, See Fig. 11,14
t_r	Rise Time	—	42	—		I_C = 16A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	210	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	160	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.69	—	mJ	and diode reverse recovery
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	920	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	110	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	27	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	42	60	ns	T_J = 25°C See Fig. 14 I_F = 12A
		—	80	120		T_J = 125°C
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	6.0	A	T_J = 25°C See Fig. 15 V_R = 200V
		—	5.6	10		T_J = 125°C
Q_{rr}	Diode Reverse Recovery Charge	—	80	180	nC	T_J = 25°C See Fig. 16 di/dt = 200Aµs
		—	220	600		T_J = 125°C
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	180	—	A/µs	T_J = 25°C See Fig. 17
	During t_b	—	160	—		T_J = 125°C

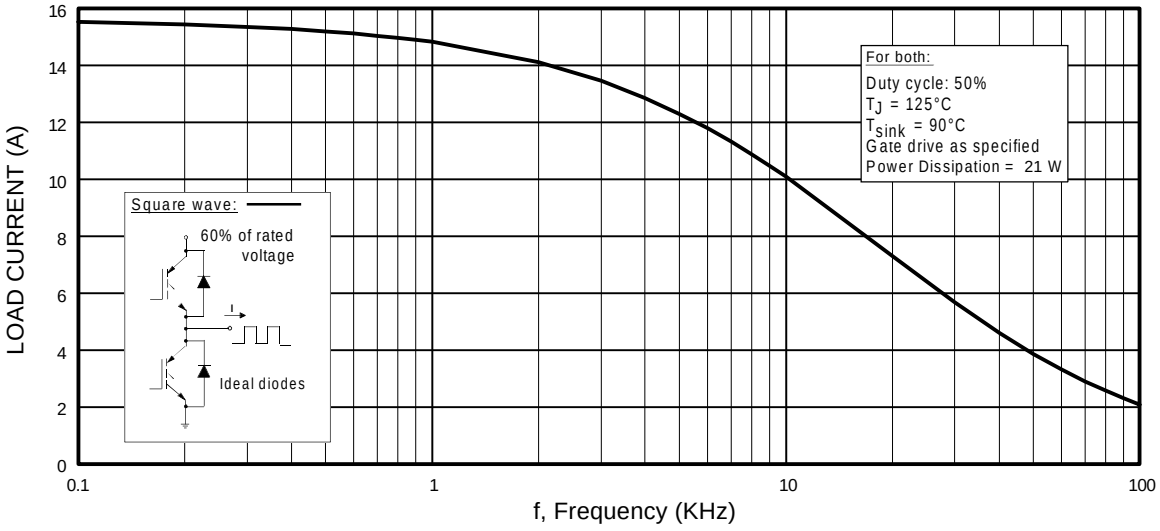


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

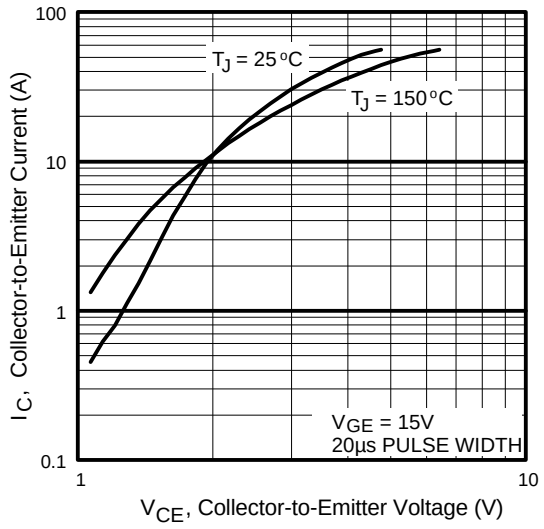


Fig. 2 - Typical Output Characteristics

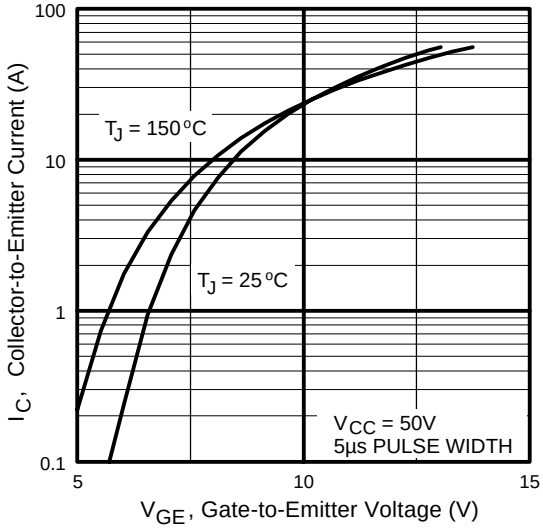


Fig. 3 - Typical Transfer Characteristics

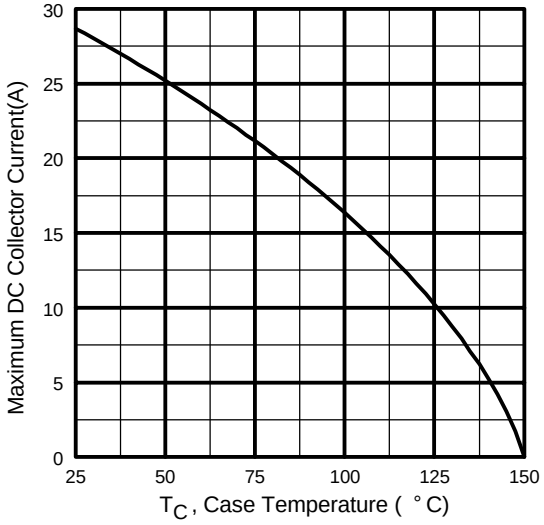


Fig. 4 - Maximum Collector Current vs. Case Temperature

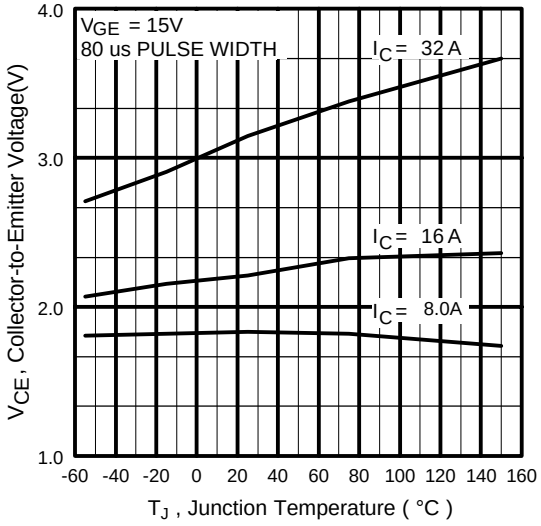


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

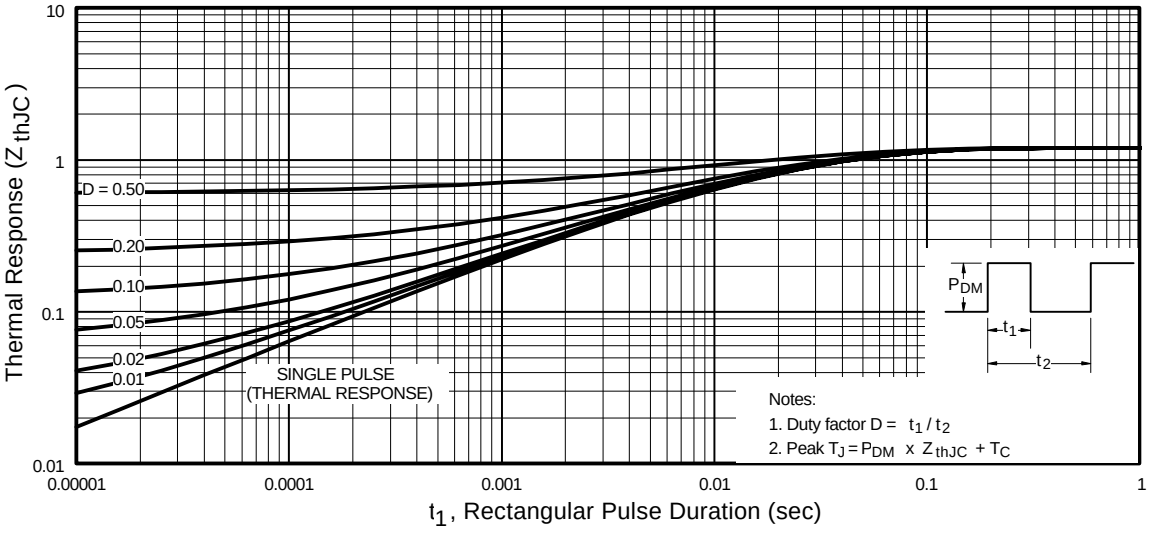


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

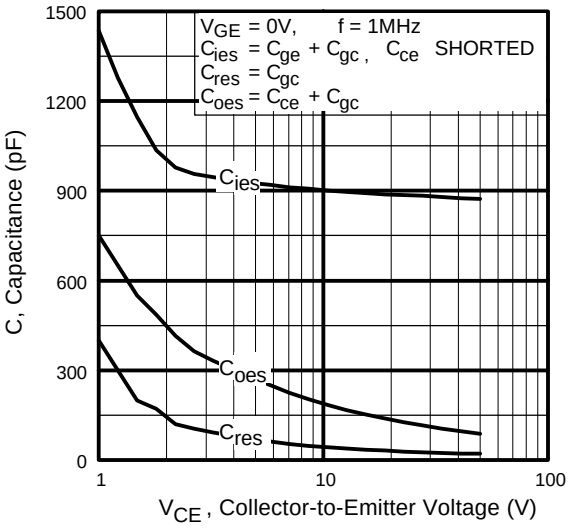


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

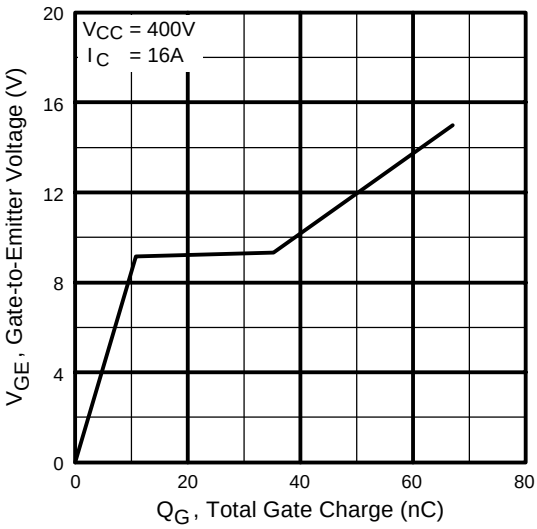


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

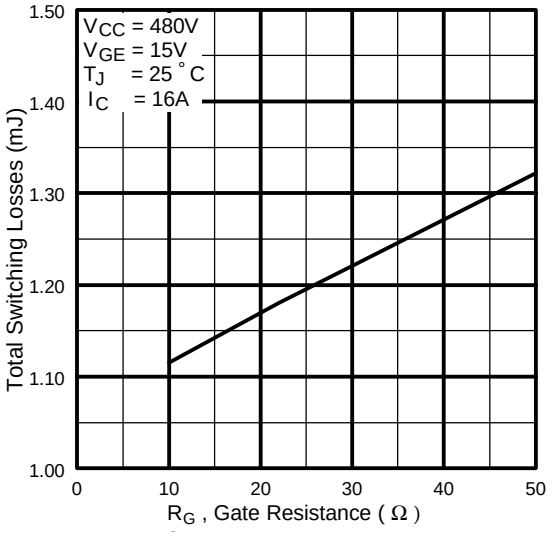


Fig. 9 - Typical Switching Losses vs. Gate Resistance

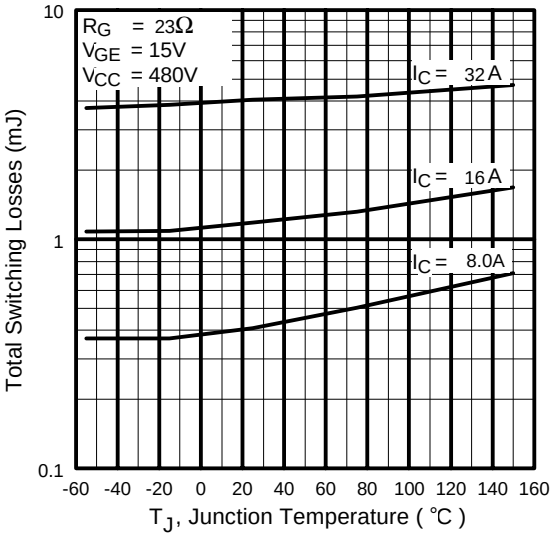


Fig. 10 - Typical Switching Losses vs. Junction Temperature

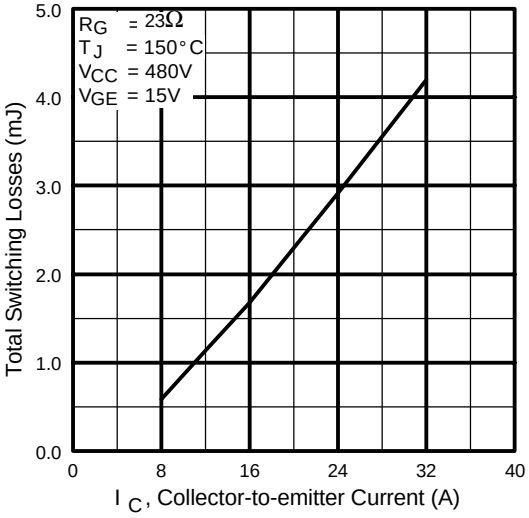


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

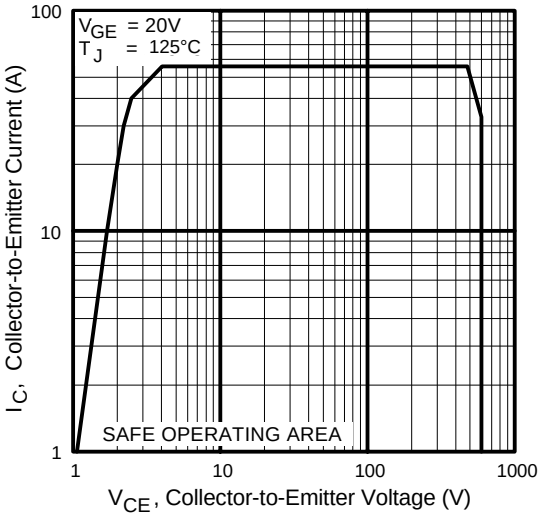


Fig. 12 - Turn-Off SOA

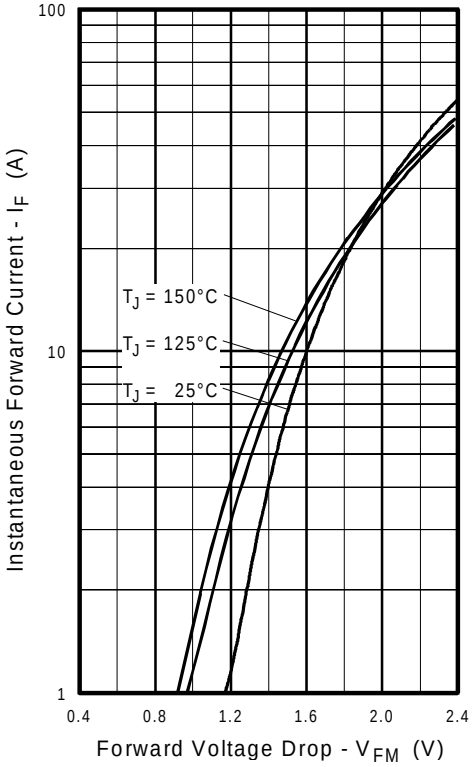


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

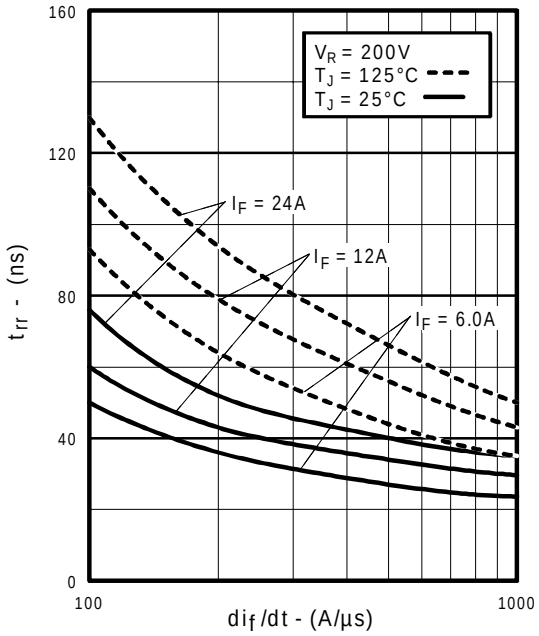


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

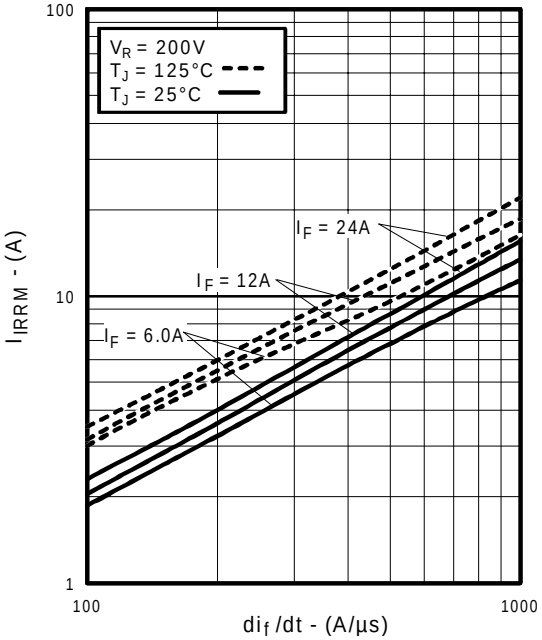


Fig. 15 - Typical Recovery Current vs. di_f/dt

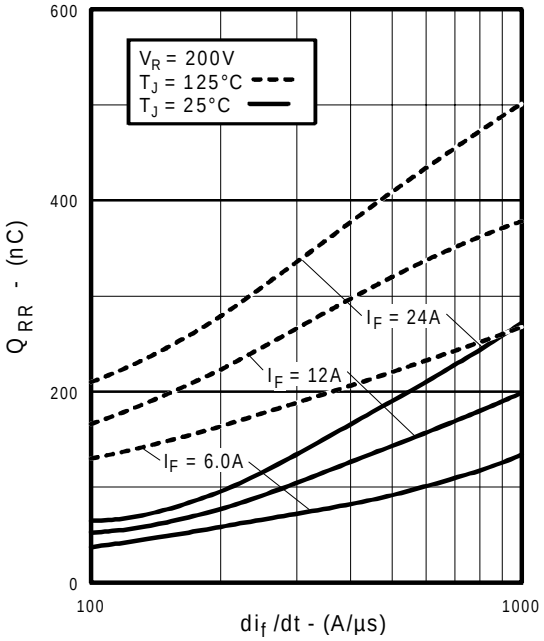


Fig. 16 - Typical Stored Charge vs. di_f/dt

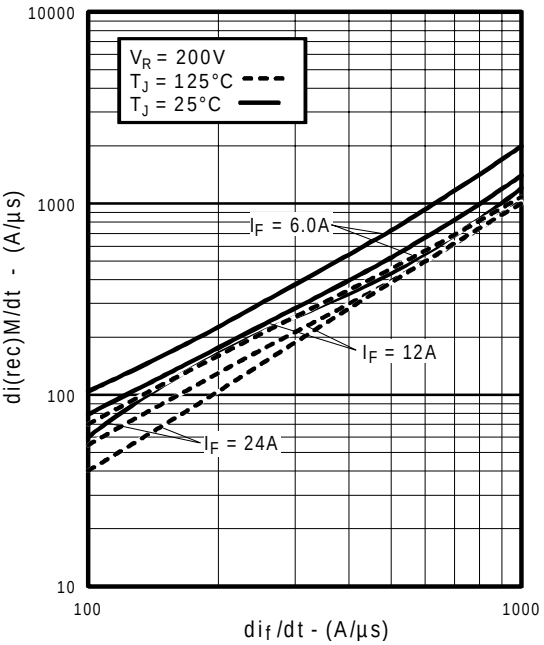


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

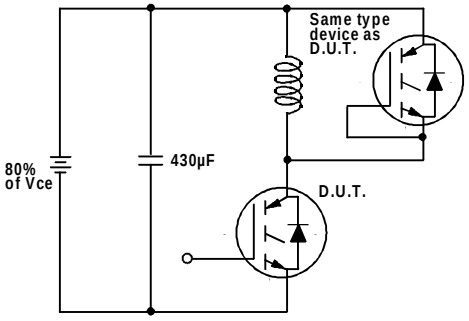


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

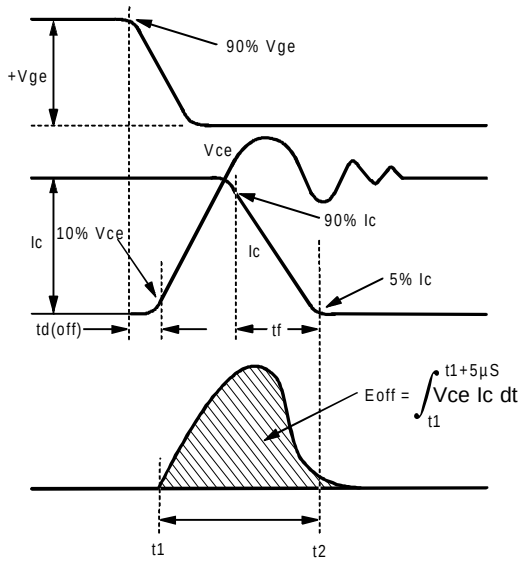


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

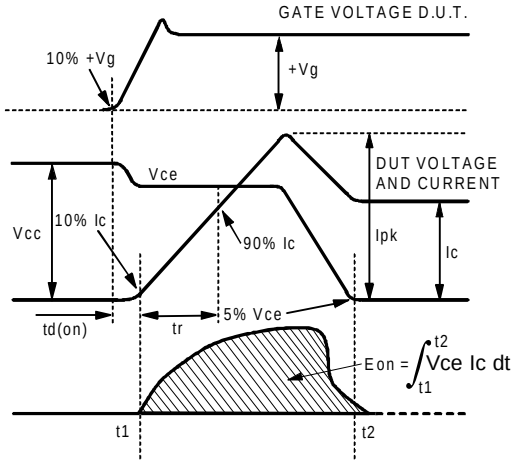


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

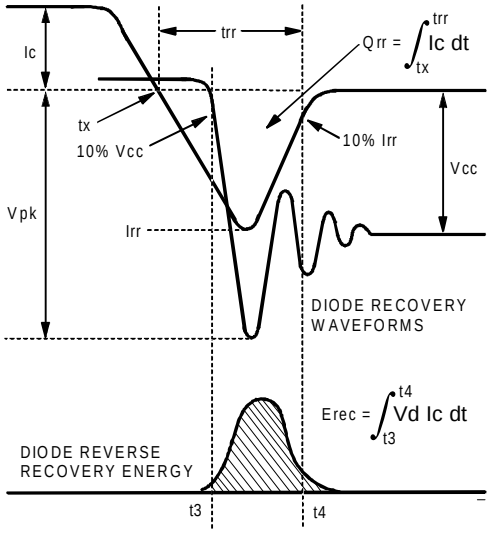


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

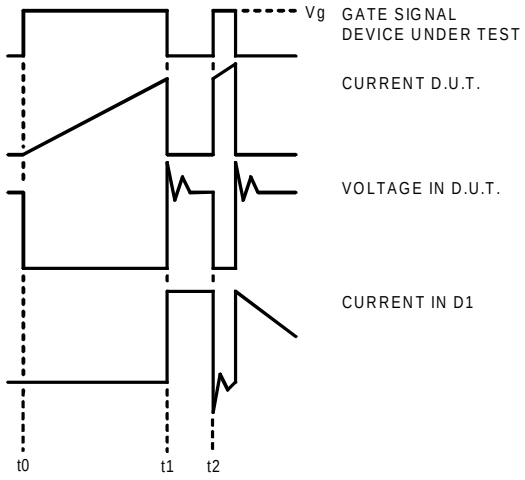


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

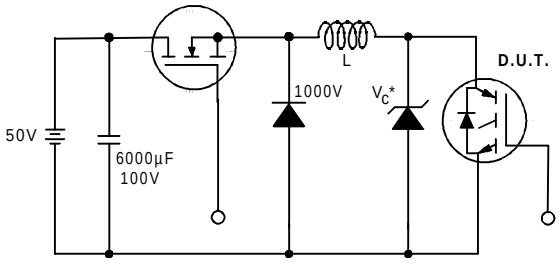


Figure 19. Clamped Inductive Load Test Circuit

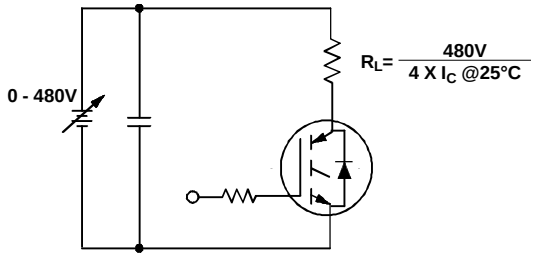


Figure 20. Pulsed Collector Current Test Circuit

Notes:

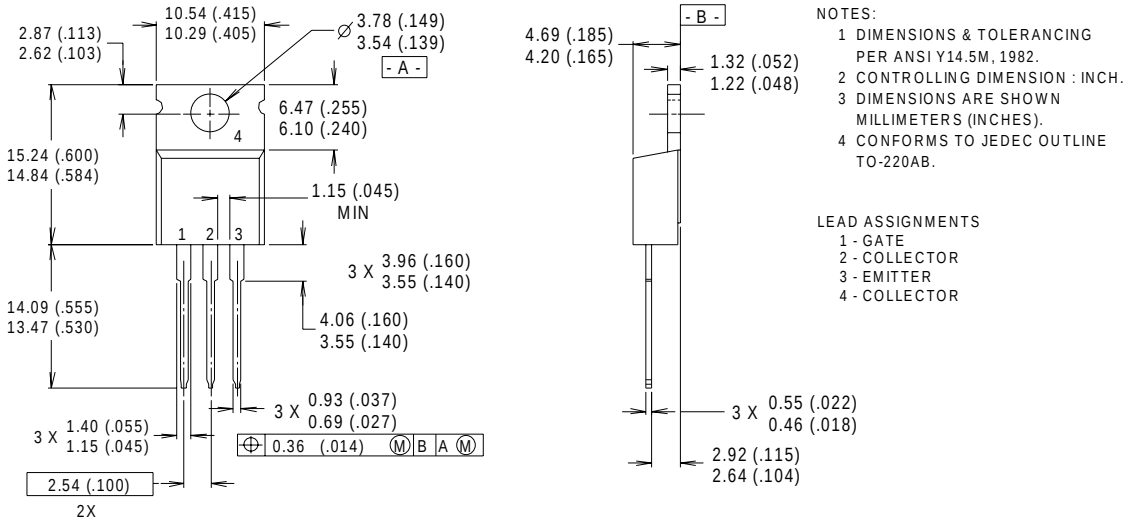
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 23Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB

Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

Data and specifications subject to change without notice. 10/00

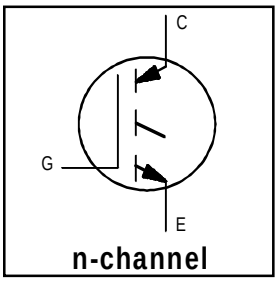
PD - 91588A

International
IOR Rectifier

IRG4PC30K

Short Circuit Rated
UltraFast IGBT

INSULATED GATE BIPOLAR TRANSISTOR



n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.21V

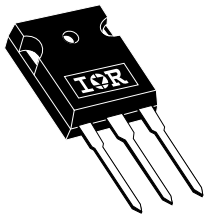
@V_{GE} = 15V, I_C = 16A

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, @360V V_{CE} (start), T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Latest generation design provides tighter parameter distribution and higher efficiency than previous generations

Benefits

- As a Freewheeling Diode we recommend our HEXFRED™ ultrafast, ultrasoft recovery diodes for minimum EMI / Noise and switching losses in the Diode and IGBT
- Latest generation 4 IGBTs offer highest power density motor controls possible
- This part replaces the IRGPC30K and IRGPC30M devices



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	28	A
I_C @ T_C = 100°C	Continuous Collector Current	16	
I_{CM}	Pulsed Collector Current ①	58	
I_{LM}	Clamped Inductive Load Current ②	58	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	260	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

4/15/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.54	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.21	—	V	I_C = 14A
		—	2.21	2.7		I_C = 16A V_{GE} = 15V
		—	2.88	—		I_C = 28A See Fig.2, 5
		—	2.36	—		I_C = 16A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-12	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	5.4	8.1	—	S	V_{CE} = 100V, I_C = 16A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1100		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	67	100	nC	I_C = 16A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	11	16		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	25	37		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	26	—	ns	
t_r	Rise Time	—	28	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	130	200		I_C = 16A, V_{CC} = 480V
t_f	Fall Time	—	120	170		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.36	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.51	—		See Fig. 9,10,14
E_{ts}	Total Switching Loss	—	0.87	1.3		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 400V, T_J = 125°C
						V_{GE} = 15V, R_G = 23Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	T_J = 150°C,
t_r	Rise Time	—	29	—		I_C = 16A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	190	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	190	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.2	—	mJ	See Fig. 11,14
E_{on}	Turn-On Switching Loss	—	0.26	—		T_J = 25°C, V_{GE} = 15V, R_G = 23Ω
E_{off}	Turn-Off Switching Loss	—	0.36	—		I_C = 14A, V_{CC} = 480V
E_{ts}	Total Switching Loss	—	0.62	—		Energy losses include "tail"
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	920	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	110	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	27	—		f = 1.0MHz

Details of note ① through ⑤ are on the last page

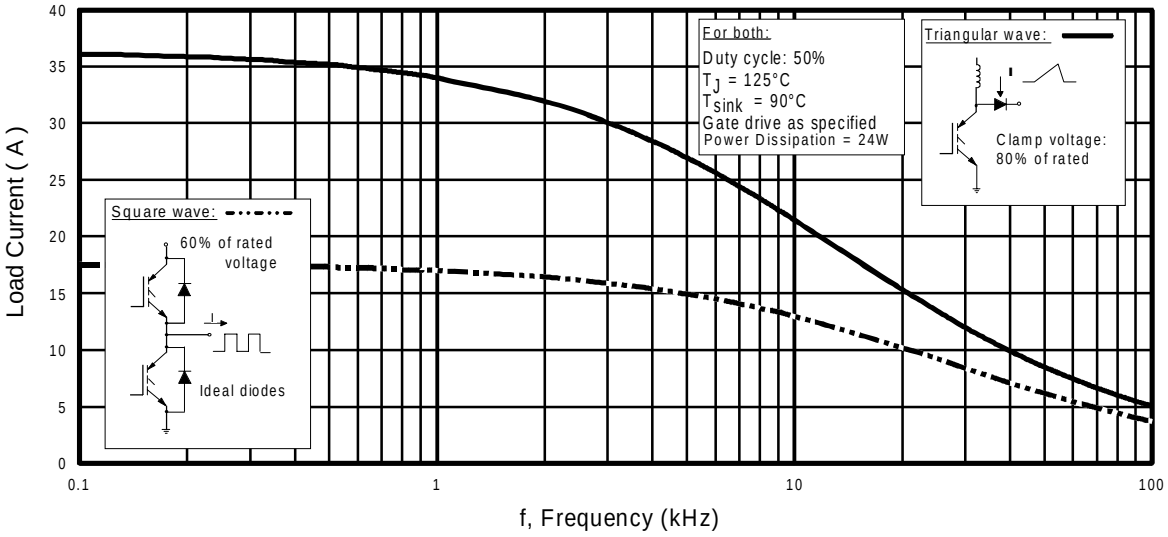


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

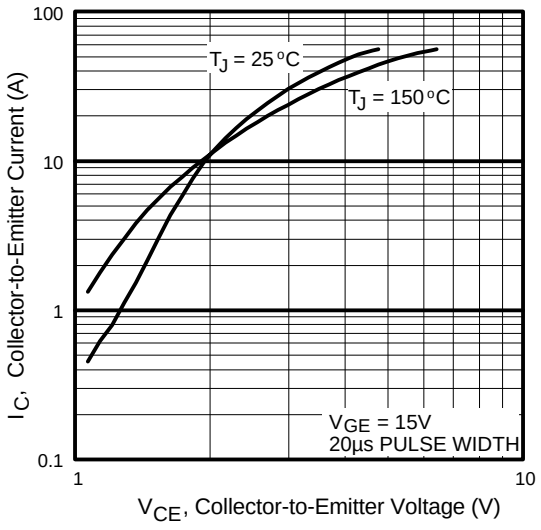


Fig. 2 - Typical Output Characteristics

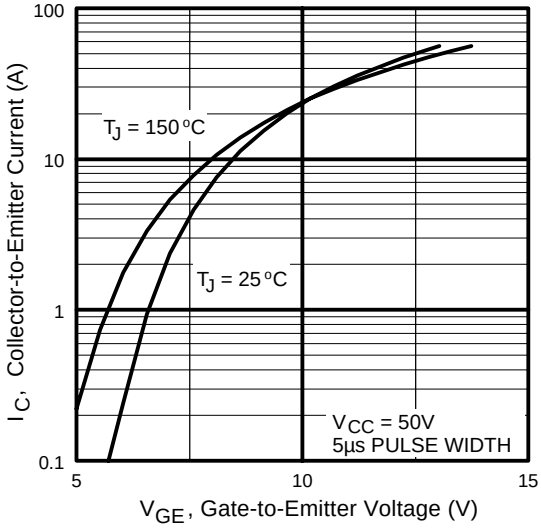


Fig. 3 - Typical Transfer Characteristics

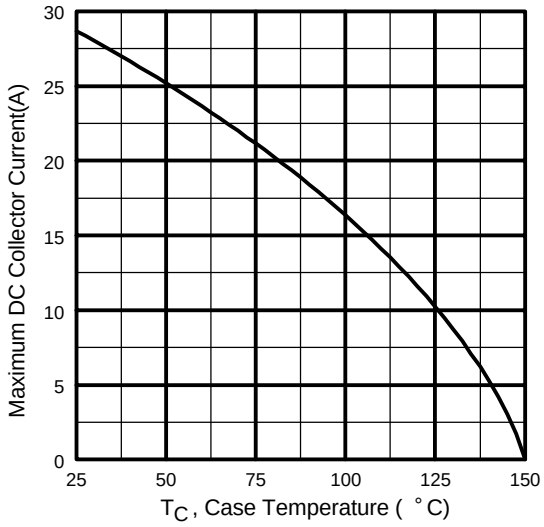


Fig. 4 - Maximum Collector Current vs. Case Temperature

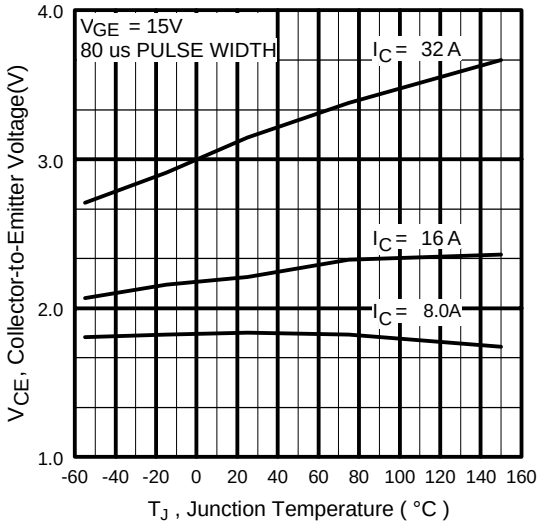


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

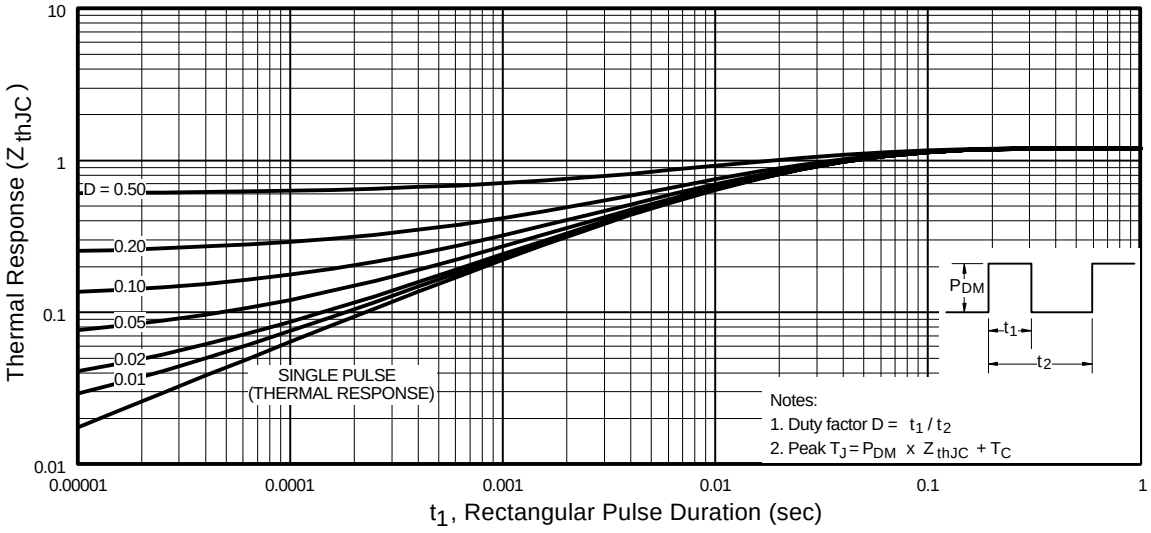


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

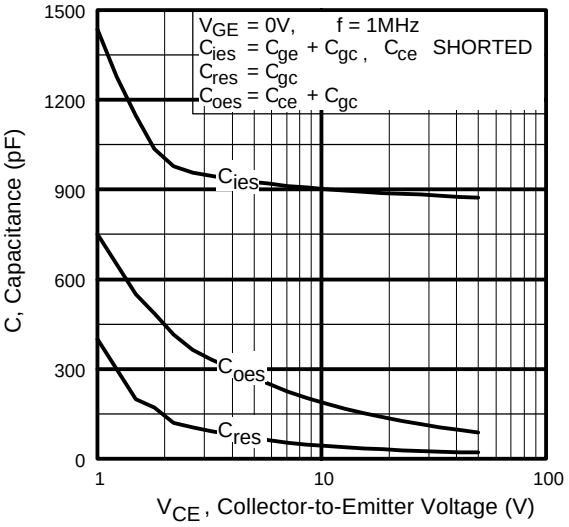


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

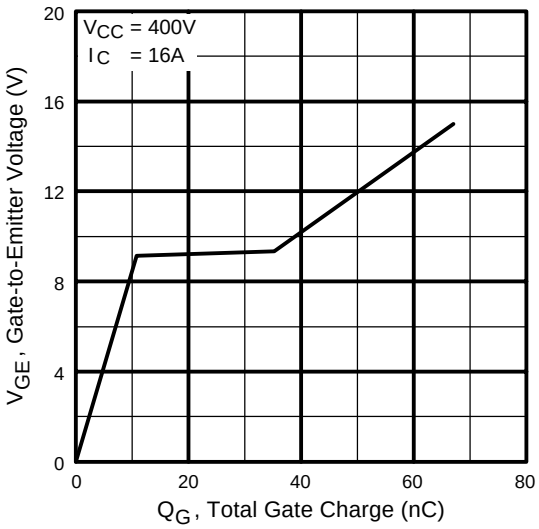


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

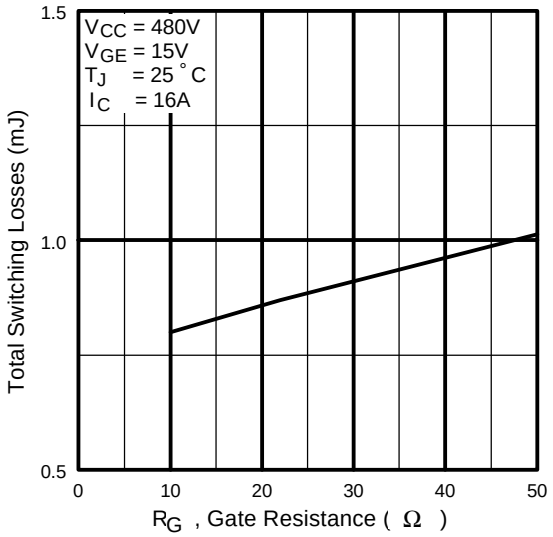


Fig. 9 - Typical Switching Losses vs. Gate Resistance

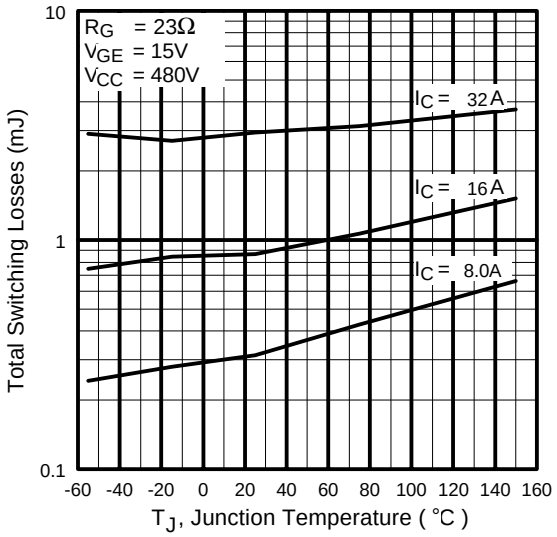


Fig. 10 - Typical Switching Losses vs. Junction Temperature

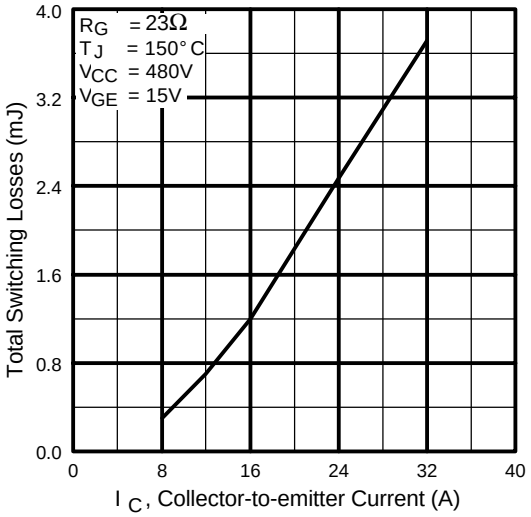


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

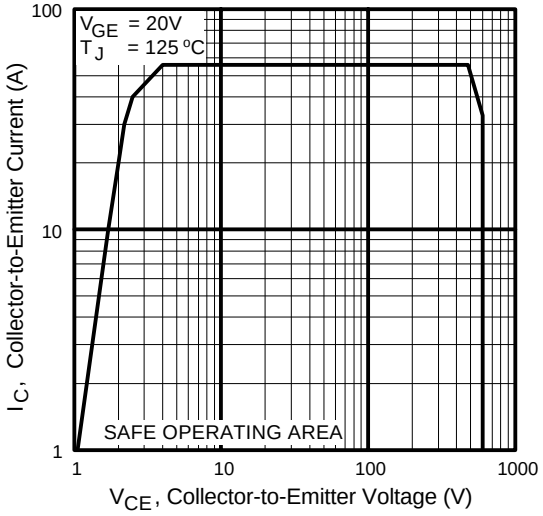


Fig. 12 - Turn-Off SOA

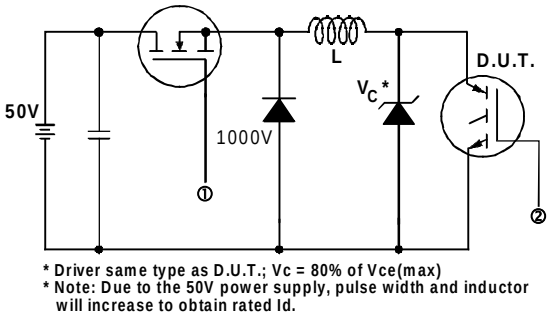


Fig. 13a - Clamped Inductive Load Test Circuit

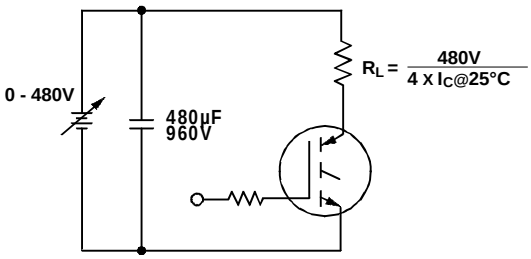


Fig. 13b - Pulsed Collector Current Test Circuit

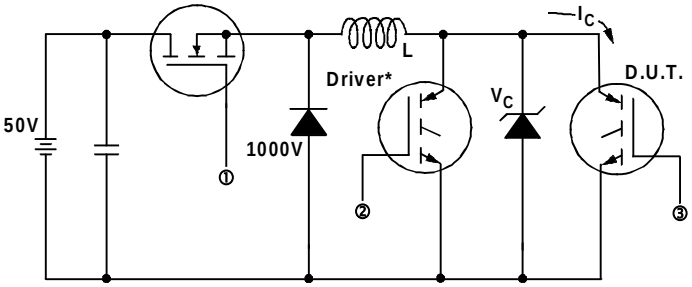


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

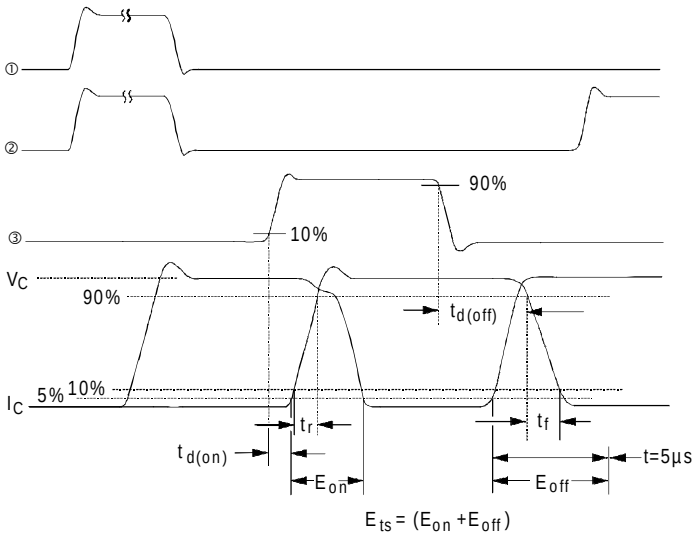


Fig. 14b - Switching Loss Waveforms

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

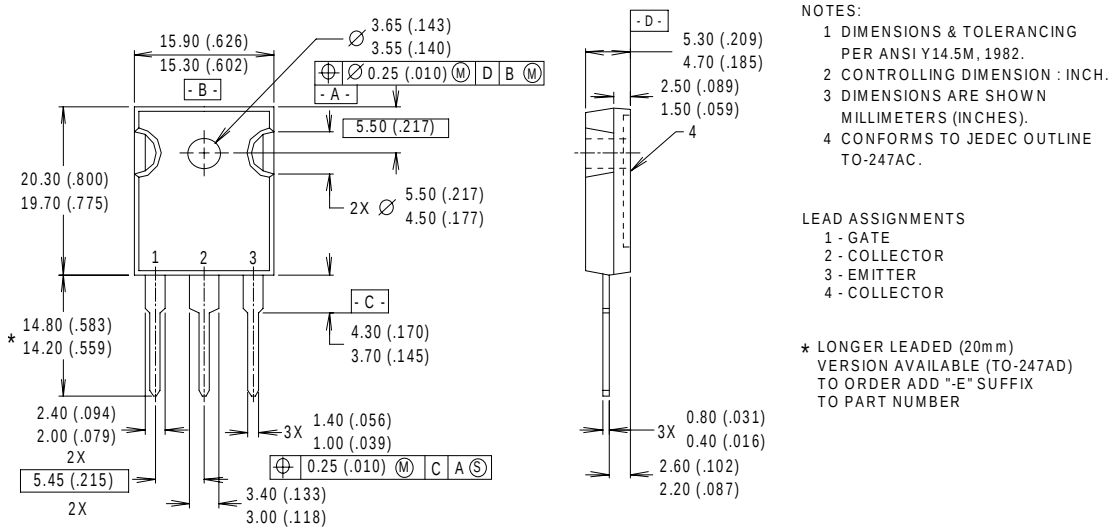
② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 23Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

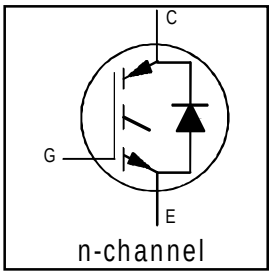
PD -91587A

International
IOR Rectifier

IRG4PC30KD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
UltraFast IGBT



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.21V

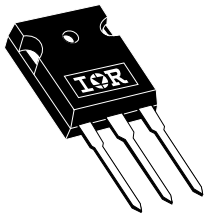
@V_{GE} = 15V, I_C = 16A

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, @360V V_{CE} (start), T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Tighter parameter distribution and higher efficiency than previous generations
- IGBT co-packaged with HEXFRED™ ultrafast, ultrasoft recovery antiparallel diodes

Benefits

- Latest generation 4 IGBTs offer highest power density motor controls possible
- HEXFRED™ diodes optimized for performance with IGBTs. Minimized recovery characteristics reduce noise, EMI and switching losses
- This part replaces the IRGBC30KD2 and IRGBC30MD2 products
- For hints see design tip 97003



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	28	A
I_C @ T_C = 100°C	Continuous Collector Current	16	
I_{CM}	Pulsed Collector Current ①	58	
I_{LM}	Clamped Inductive Load Current ②	58	
I_F @ T_C = 100°C	Diode Continuous Forward Current	12	
I_{FM}	Diode Maximum Forward Current	58	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	1.2	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	2.5	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	40	
Wt	Weight	—	6 (0.21)	—	g (oz)

4/15/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.54	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.21	2.7	V	I_C = 16A V_{GE} = 15V
		—	2.88	—		I_C = 28A See Fig. 2, 5
		—	2.36	—		I_C = 16A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-12	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	5.4	8.1	—	S	V_{CE} = 100V, I_C = 16A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 12A See Fig. 13
		—	1.3	1.6		I_C = 12A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	67	100	nC	I_C = 16A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	11	16		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	25	37		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	60	—	ns	
t_r	Rise Time	—	42	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	160	250		I_C = 16A, V_{CC} = 480V
t_f	Fall Time	—	80	120		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.60	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.58	—		and diode reverse recovery
E_{ts}	Total Switching Loss	—	1.18	1.6		See Fig. 9,10,14
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 360V, T_J = 125°C
						V_{GE} = 15V, R_G = 10Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	58	—	ns	T_J = 150°C, See Fig. 11,14
t_r	Rise Time	—	42	—		I_C = 16A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	210	—		V_{GE} = 15V, R_G = 23Ω,
t_f	Fall Time	—	160	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.69	—	mJ	and diode reverse recovery
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	920	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	110	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	27	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	42	60	ns	T_J = 25°C See Fig. 14 I_F = 12A
		—	80	120		T_J = 125°C
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	6.0	A	T_J = 25°C See Fig. 15 V_R = 200V
		—	5.6	10		T_J = 125°C
Q_{rr}	Diode Reverse Recovery Charge	—	80	180	nC	T_J = 25°C See Fig. 16 di/dt = 200Aµs
		—	220	600		T_J = 125°C
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	180	—	A/µs	T_J = 25°C See Fig. 17
	During t_b	—	160	—		T_J = 125°C

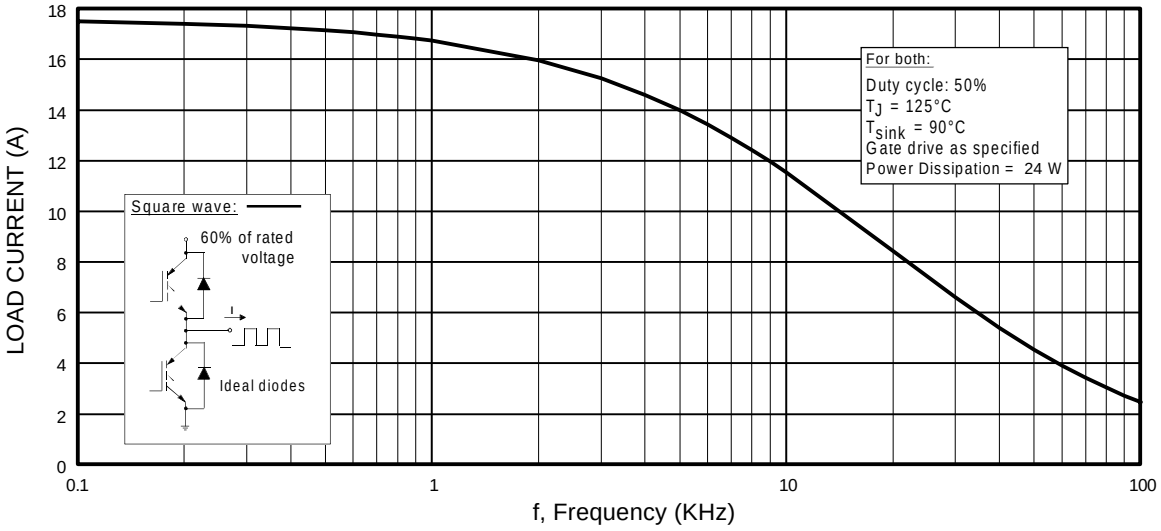


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

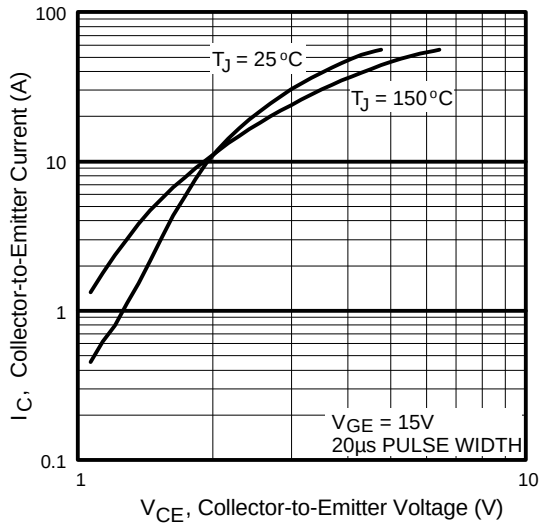


Fig. 2 - Typical Output Characteristics

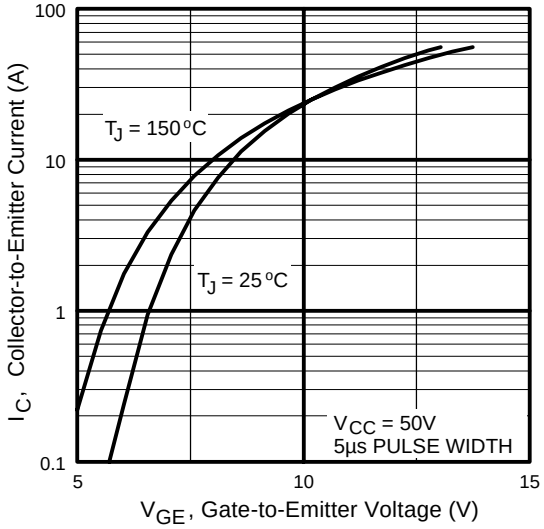


Fig. 3 - Typical Transfer Characteristics

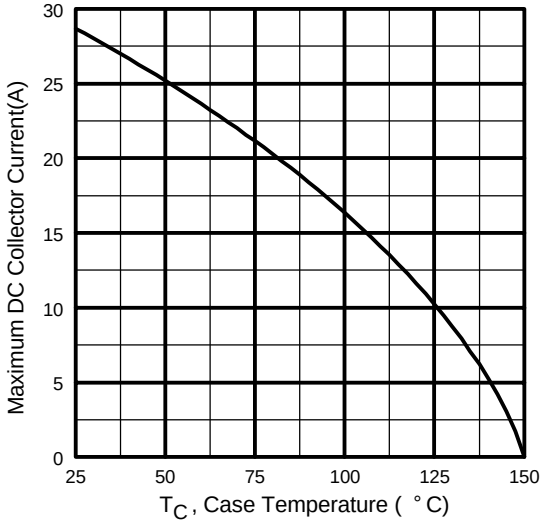


Fig. 4 - Maximum Collector Current vs. Case Temperature

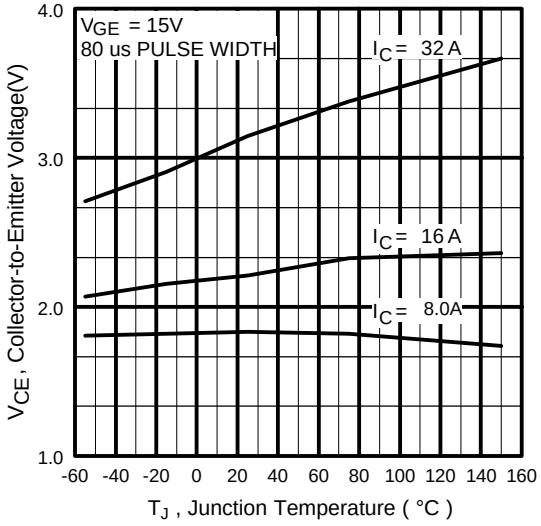


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

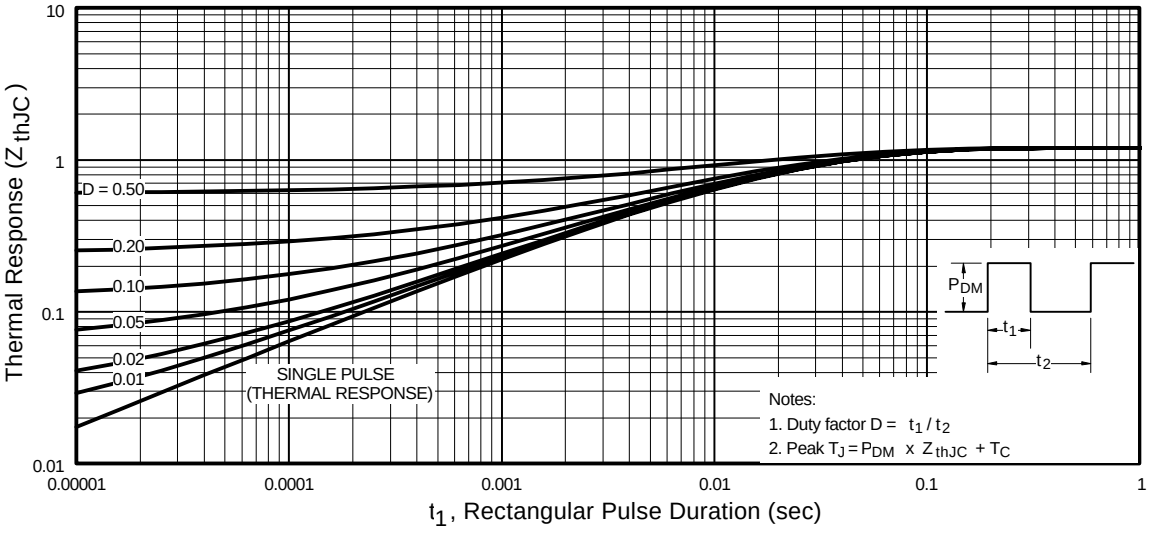


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

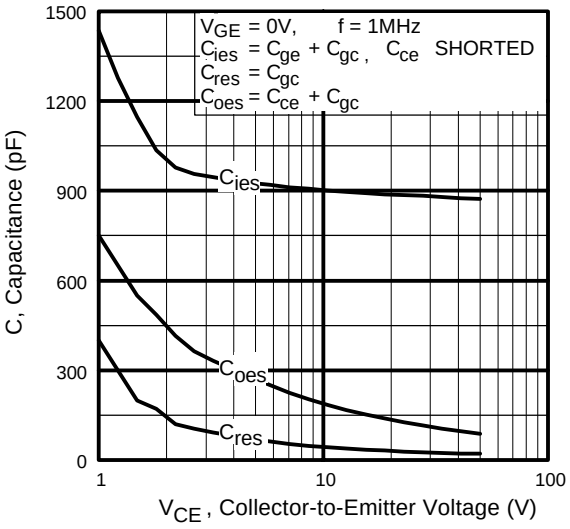


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

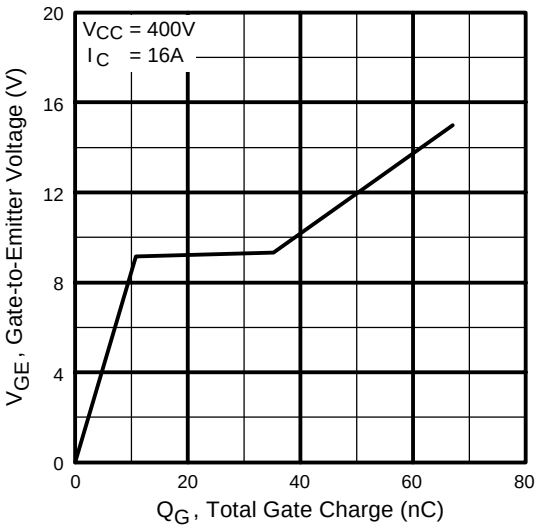


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

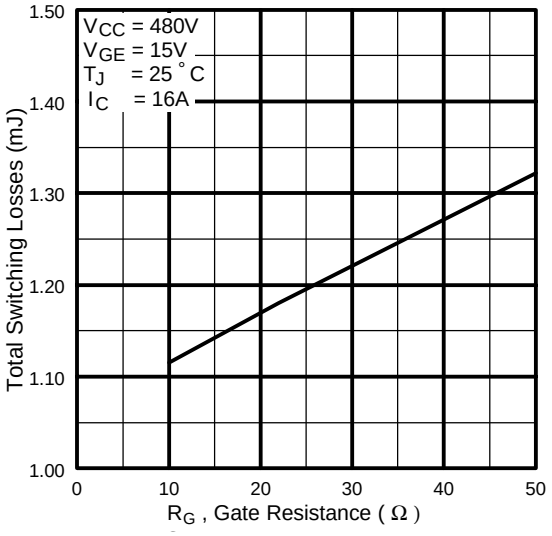


Fig. 9 - Typical Switching Losses vs. Gate Resistance

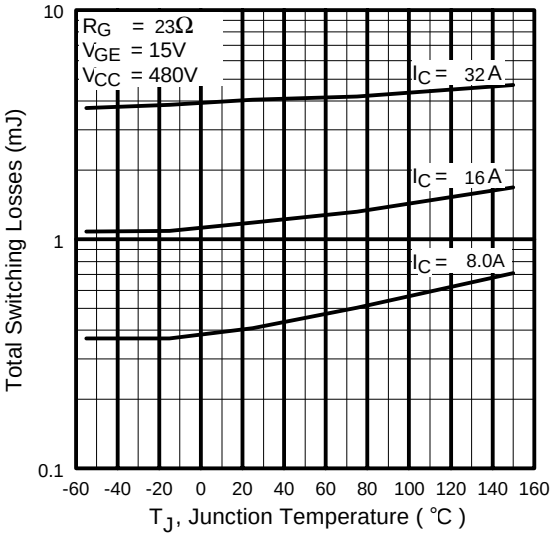


Fig. 10 - Typical Switching Losses vs. Junction Temperature

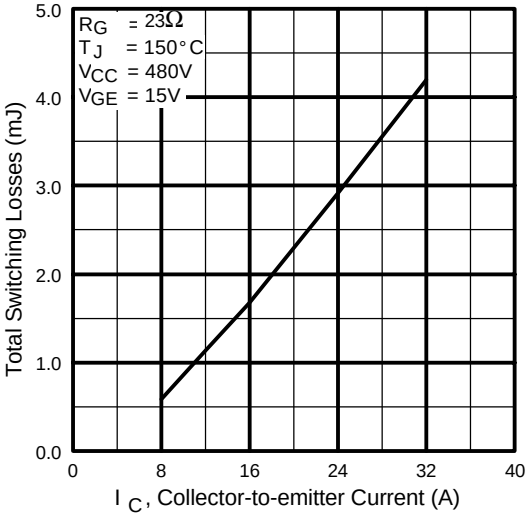


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

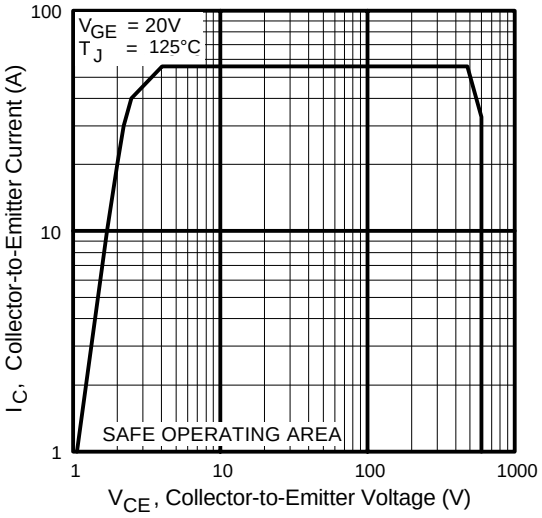


Fig. 12 - Turn-Off SOA

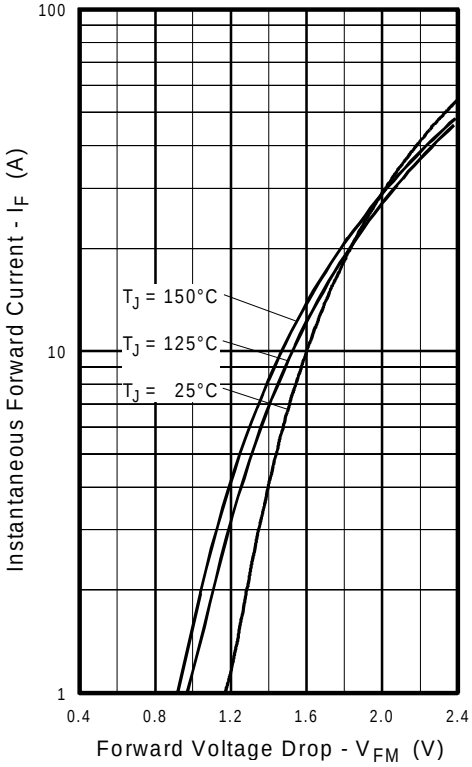


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

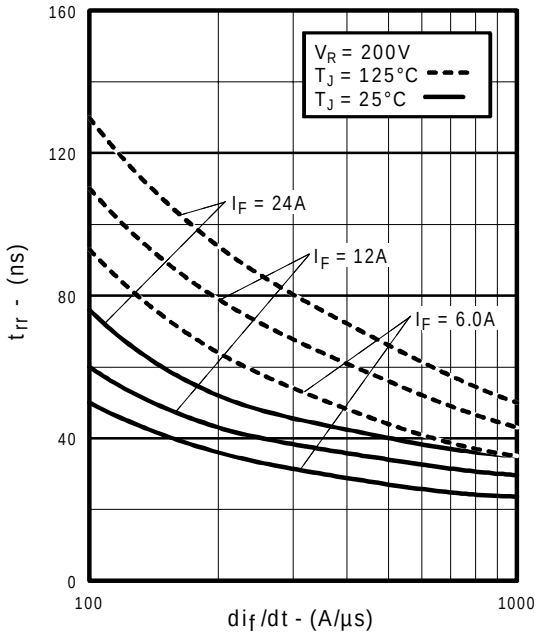


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

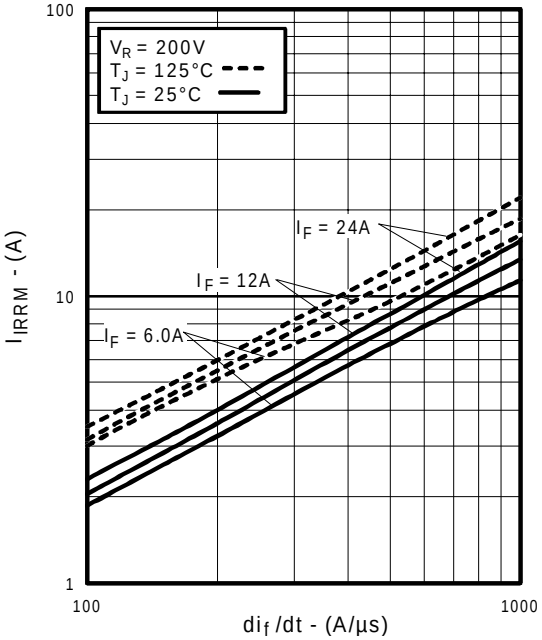


Fig. 15 - Typical Recovery Current vs. di_f/dt

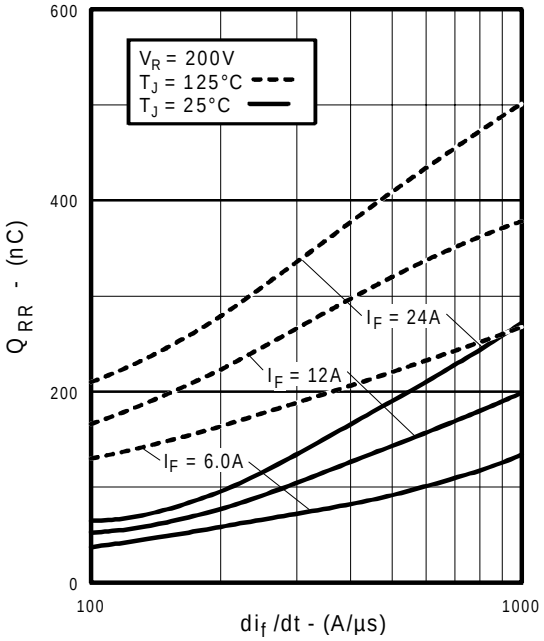


Fig. 16 - Typical Stored Charge vs. di_f/dt

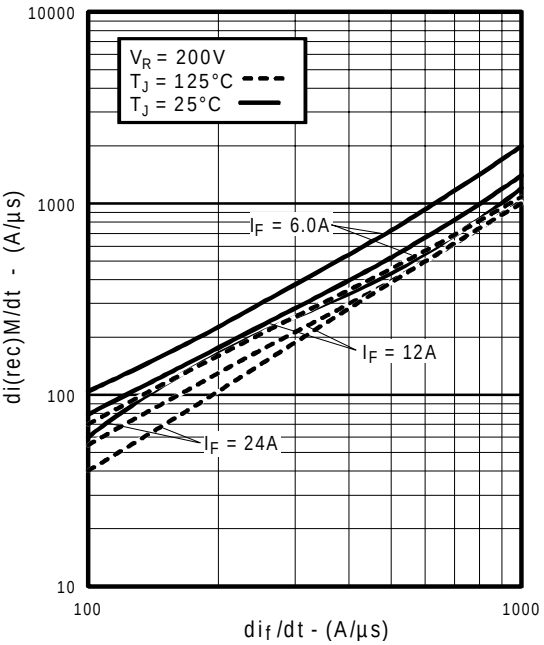


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

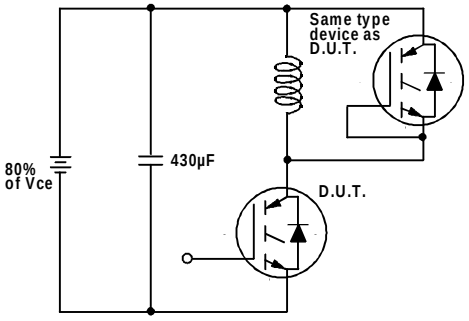


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

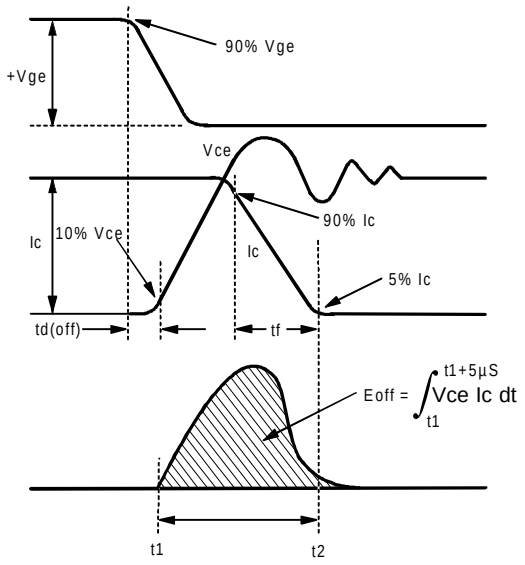


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

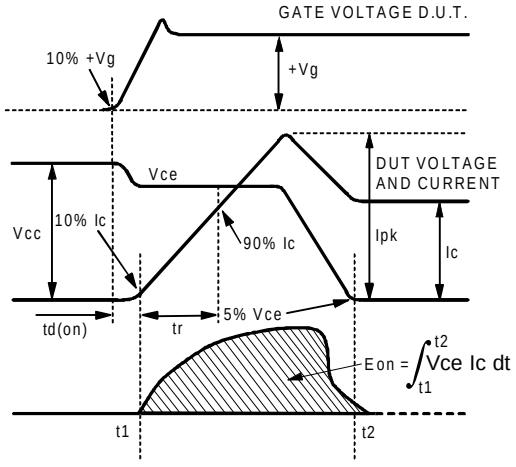


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

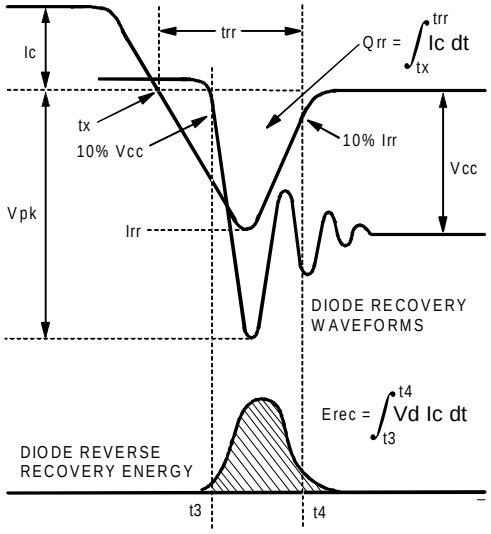


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

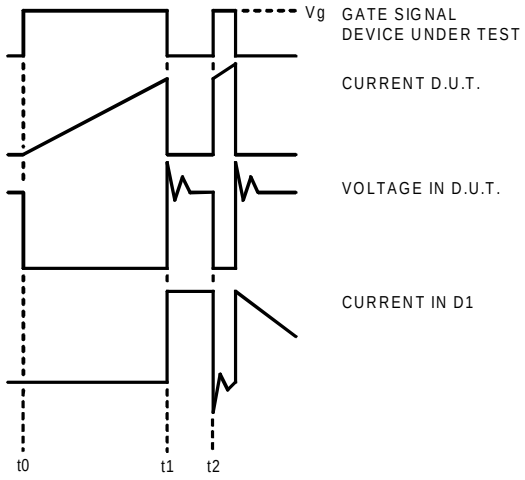


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

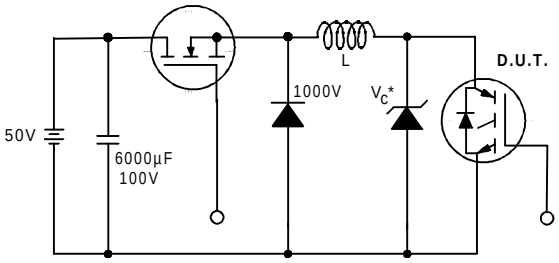


Figure 19. Clamped Inductive Load Test Circuit

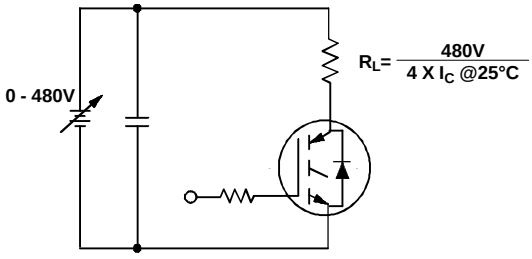


Figure 20. Pulsed Collector Current Test Circuit

Notes:

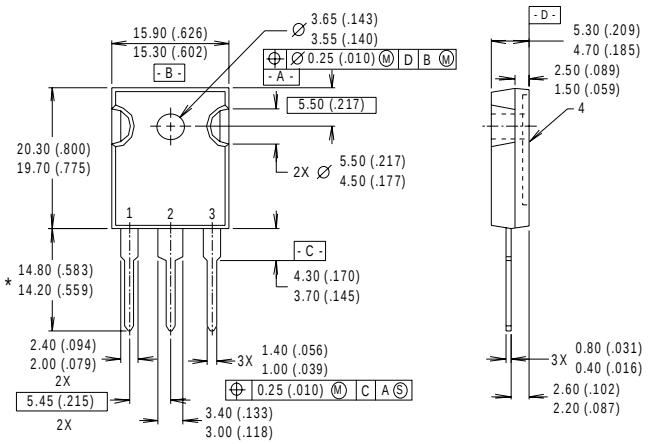
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 23Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD - 91450B

International
IOR Rectifier

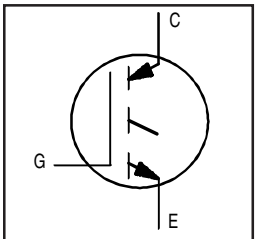
IRG4BC30F

INSULATED GATE BIPOLAR TRANSISTOR

Fast Speed IGBT

Features

- Fast: optimized for medium operating frequencies (1-5 kHz in hard switching, >20 kHz in resonant mode).
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-220AB package



n-channel

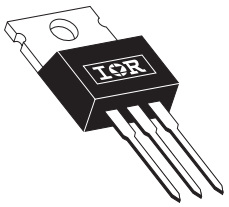
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.59V

@V_{GE} = 15V, I_C = 17A

Benefits

- Generation 4 IGBTs offer highest efficiency available
- IGBTs optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	31	A
I_C @ T_C = 100°C	Continuous Collector Current	17	
I_{CM}	Pulsed Collector Current ①	120	
I_{LM}	Clamped Inductive Load Current ②	120	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	10	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	80	
Wt	Weight	2.0 (0.07)	—	g (oz)

4/17/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.69	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.59	1.8	V	I_C = 17A V_{GE} = 15V
		—	1.99	—		I_C = 31A See Fig.2, 5
		—	1.7	—		I_C = 17A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	6.1	10	—	S	V_{CE} = 100V, I_C = 17A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	51	77	nC	I_C = 17A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	7.9	12		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	19	28		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	
t_r	Rise Time	—	15	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	200	300		I_C = 17A, V_{CC} = 480V
t_f	Fall Time	—	180	270		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.23	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	1.18	—		See Fig. 10, 11, 13, 14
E_{ts}	Total Switching Loss	—	1.41	2.0		
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	T_J = 150°C,
t_r	Rise Time	—	16	—		I_C = 17A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	290	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	350	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	2.5	—	mJ	See Fig. 13, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1100	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	74	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	14	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 23Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

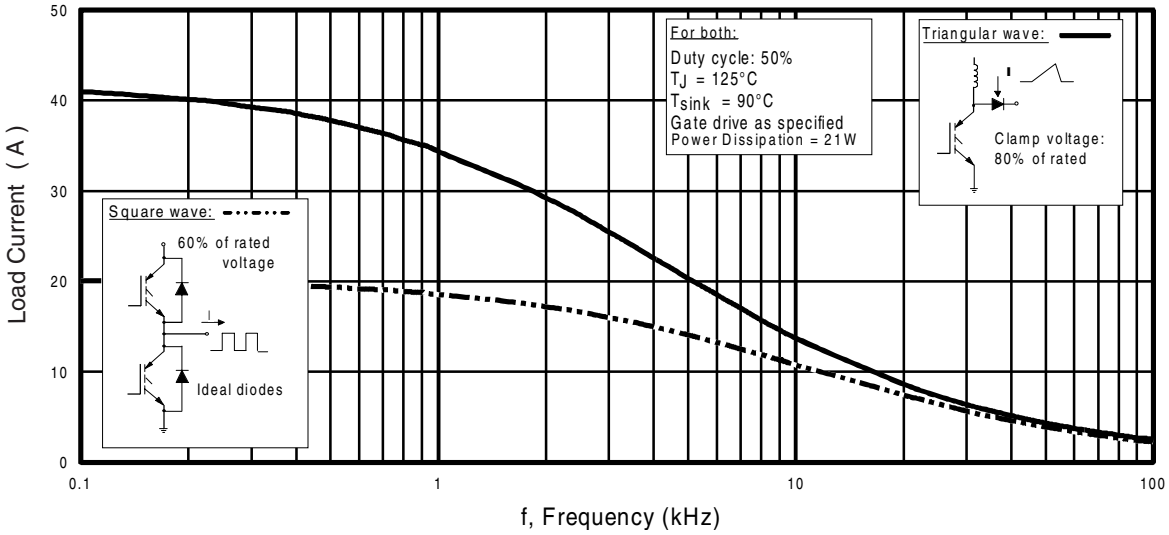


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

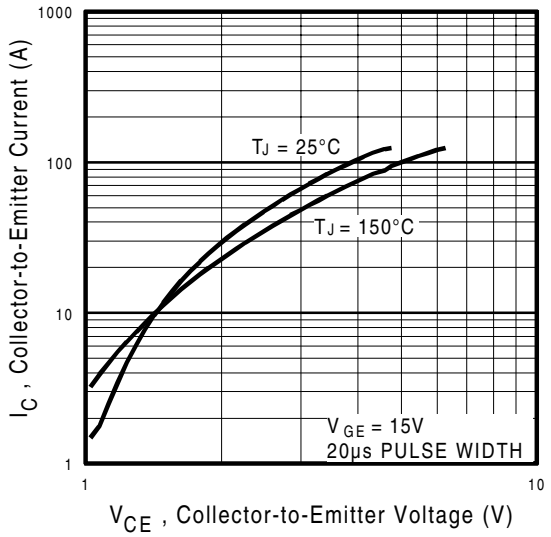


Fig. 2 - Typical Output Characteristics

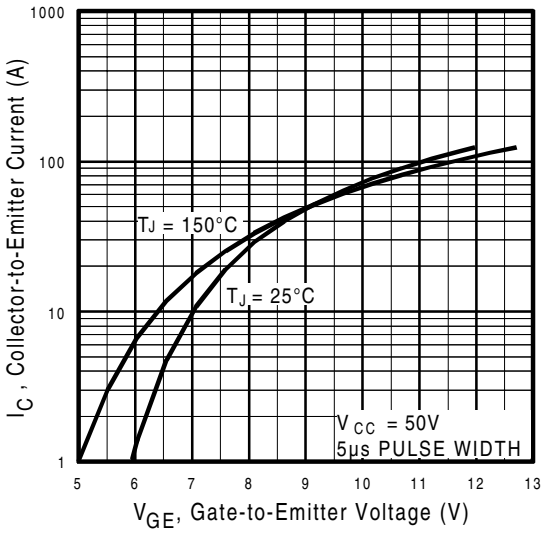


Fig. 3 - Typical Transfer Characteristics

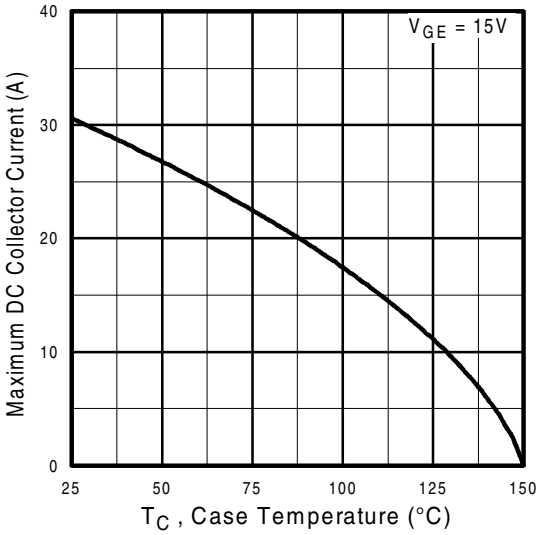


Fig. 4 - Maximum Collector Current vs. Case Temperature

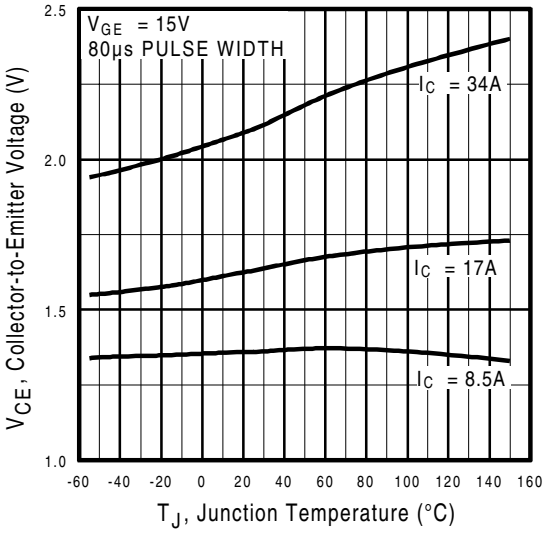


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

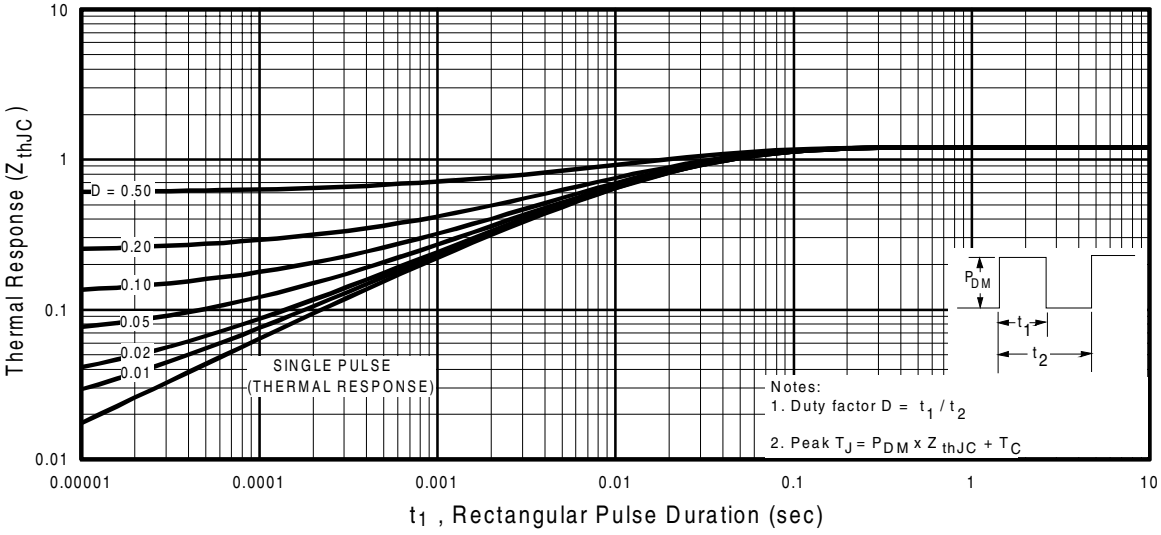


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

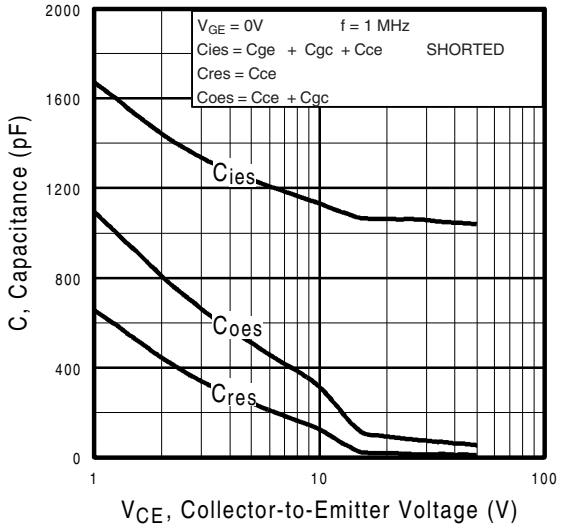


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

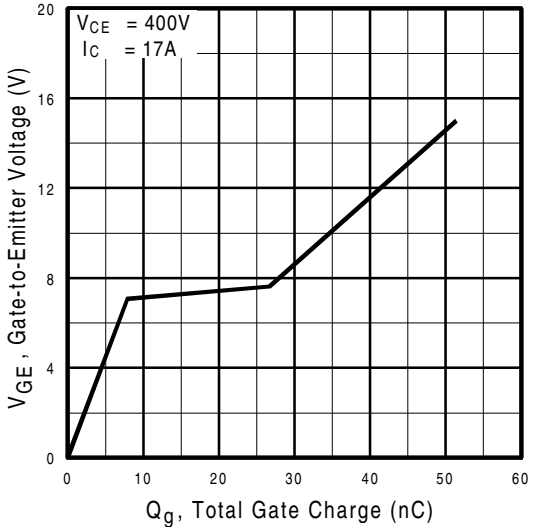


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

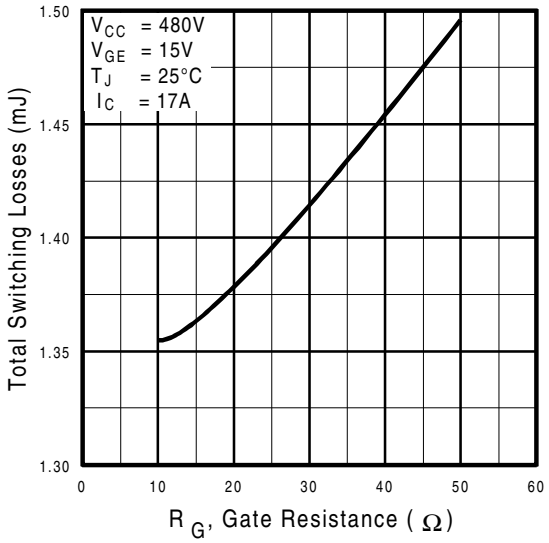


Fig. 9 - Typical Switching Losses vs. Gate Resistance

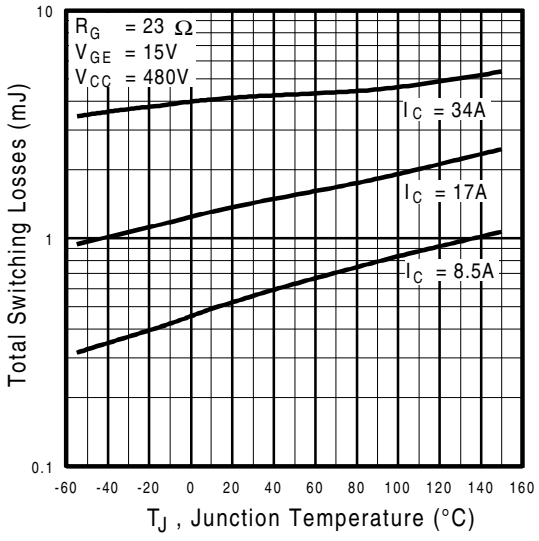


Fig. 10 - Typical Switching Losses vs. Junction Temperature

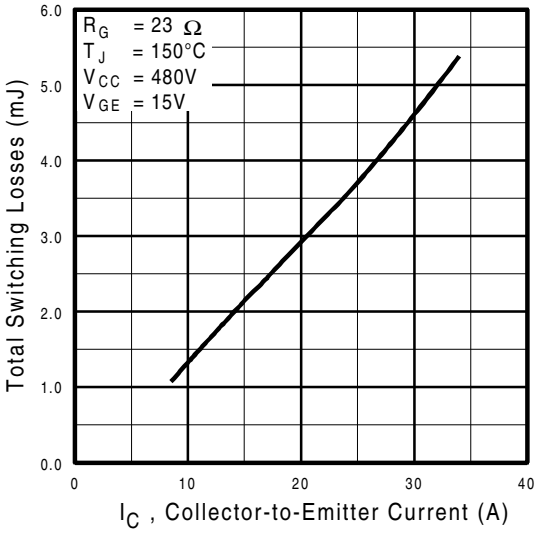


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

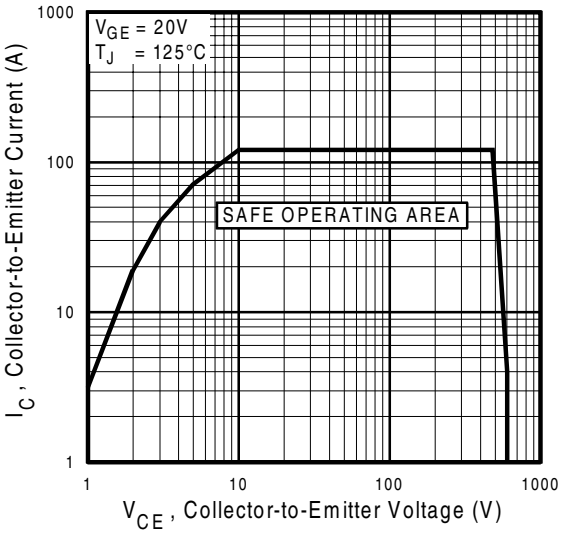


Fig. 12 - Turn-Off SOA

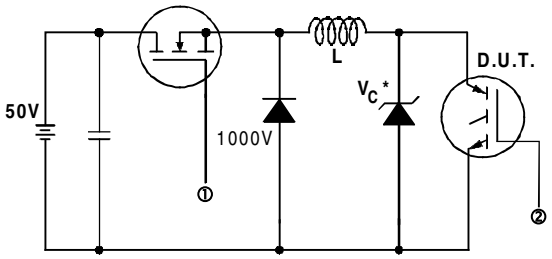


Fig. 13a - Clamped Inductive Load Test Circuit

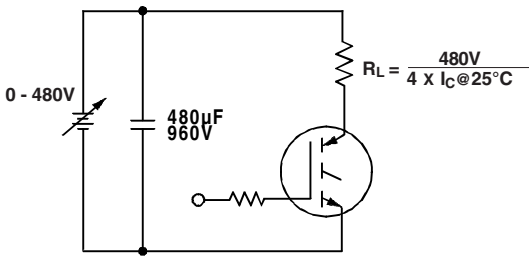


Fig. 13b - Pulsed Collector Current Test Circuit

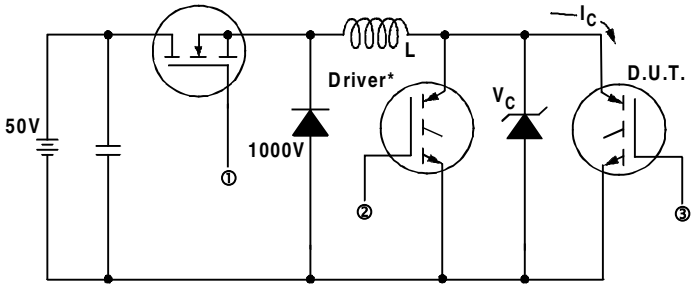


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

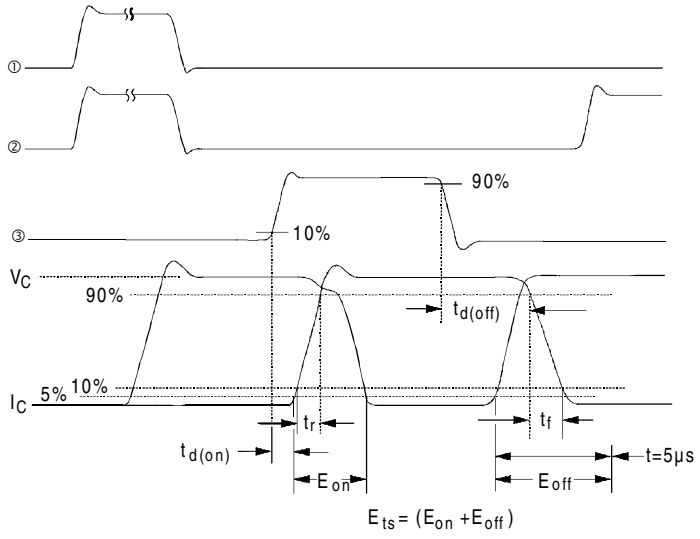
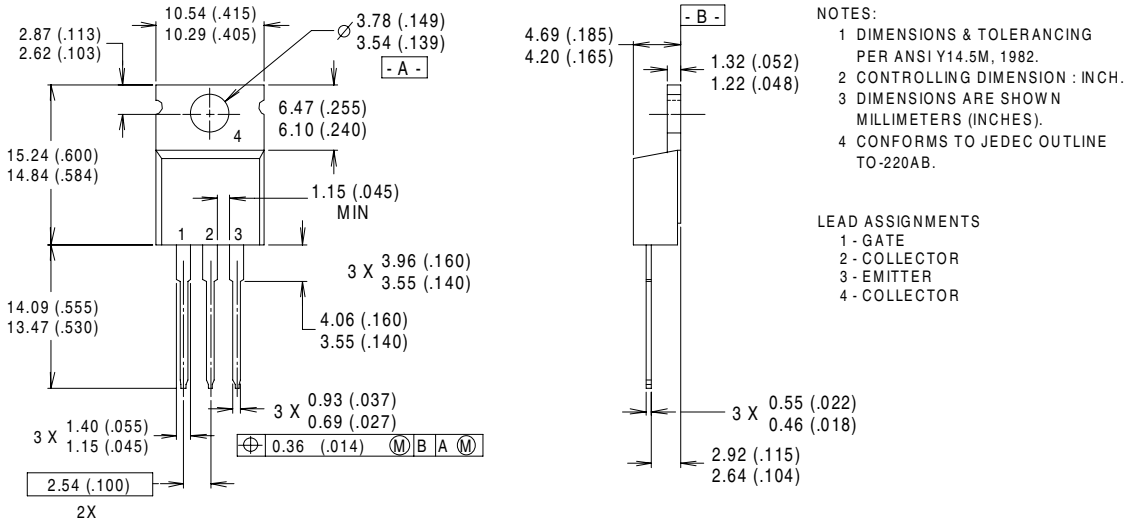


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

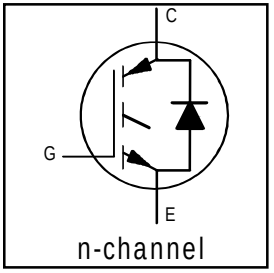
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

International
IOR Rectifier

IRG4BC30FD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Fast CoPack IGBT



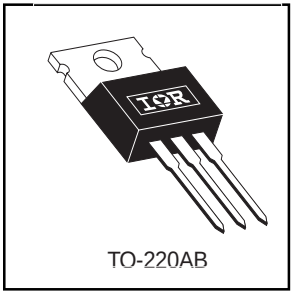
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.59V

@V_{GE} = 15V, I_C = 17A

Features

- Fast: Optimized for medium operating frequencies (1-5 kHz in hard switching, >20 kHz in resonant mode).
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-220AB package



TO-220AB

Benefits

- Generation -4 IGBT's offer highest efficiencies available
- IGBT's optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBT's . Minimized recovery characteristics require less/no snubbing
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	31	A
I_C @ T_C = 100°C	Continuous Collector Current	17	
I_{CM}	Pulsed Collector Current ①	120	
I_{LM}	Clamped Inductive Load Current ②	120	
I_F @ T_C = 100°C	Diode Continuous Forward Current	12	
I_{FM}	Diode Maximum Forward Current	120	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	------	------	1.2	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	------	------	2.5	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	------	0.50	------	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	-----	-----	80	
Wt	Weight	------	2 (0.07)	------	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	----	----	V	V_{GE} = 0V, I_C = 250µA
$DV_{(BR)CES}/DT_J$	Temperature Coeff. of Breakdown Voltage	----	0.69	----	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	----	1.59	1.8	V	I_C = 17A V_{GE} = 15V
		----	1.99	----		I_C = 31A See Fig. 2, 5
		----	1.70	----		I_C = 17A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	----	6.0		V_{CE} = V_{GE}, I_C = 250µA
$DV_{GE(th)}/DT_J$	Temperature Coeff. of Threshold Voltage	----	-11	----	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	6.1	10	----	S	V_{CE} = 100V, I_C = 17A
I_{CES}	Zero Gate Voltage Collector Current	----	----	250	µA	V_{GE} = 0V, V_{CE} = 600V
		----	----	2500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	----	1.4	1.7	V	I_C = 12A See Fig. 13
		----	1.3	1.6		I_C = 12A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	----	----	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	----	51	77		I_C = 17A
Qge	Gate - Emitter Charge (turn-on)	----	7.9	12	nC	V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	----	19	28		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	----	42	----		T_J = 25°C
t_r	Rise Time	----	26	----	ns	I_C = 17A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	230	350		V_{GE} = 15V, R_G = 23W
t_f	Fall Time	----	160	230		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	----	0.63	----		diode reverse recovery.
E_{off}	Turn-Off Switching Loss	----	1.39	----	mJ	See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	----	2.02	3.9		
$t_{d(on)}$	Turn-On Delay Time	----	42	----		T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	----	27	----	ns	I_C = 17A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	310	----		V_{GE} = 15V, R_G = 23W
t_f	Fall Time	----	310	----		Energy losses include "tail" and
E_{ts}	Total Switching Loss	----	3.2	----	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	----	7.5	----	nH	Measured 5mm from package
C_{ies}	Input Capacitance	----	1100	----		V_{GE} = 0V
C_{oes}	Output Capacitance	----	74	----	pF	V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	----	14	----		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	----	42	60	ns	T_J = 25°C See Fig.
		----	80	120		T_J = 125°C 14 I_F = 12A
I_{rr}	Diode Peak Reverse Recovery Current	----	3.5	6.0	A	T_J = 25°C See Fig.
		----	5.6	10		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	----	80	180	nC	T_J = 25°C See Fig.
		----	220	600		T_J = 125°C 16 di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	----	180	----	A/µs	T_J = 25°C See Fig.
	During t_b	----	120	----		T_J = 125°C 17

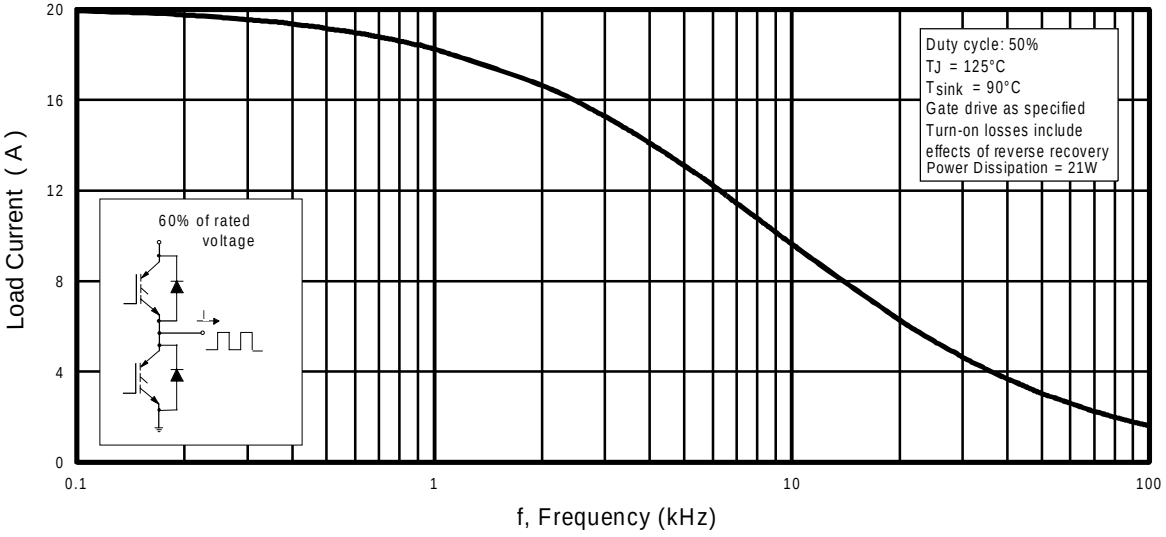


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

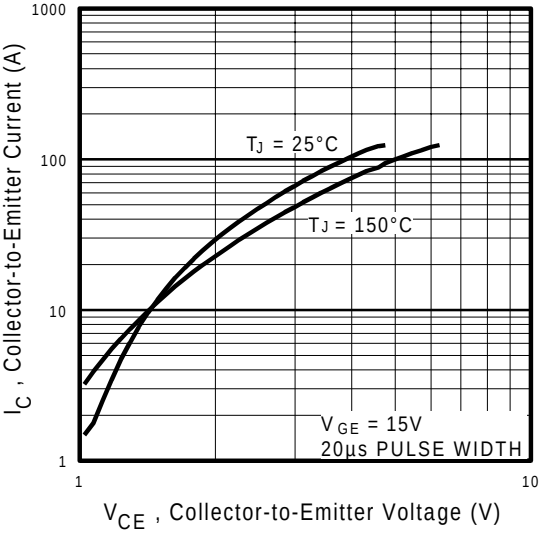


Fig. 2 - Typical Output Characteristics

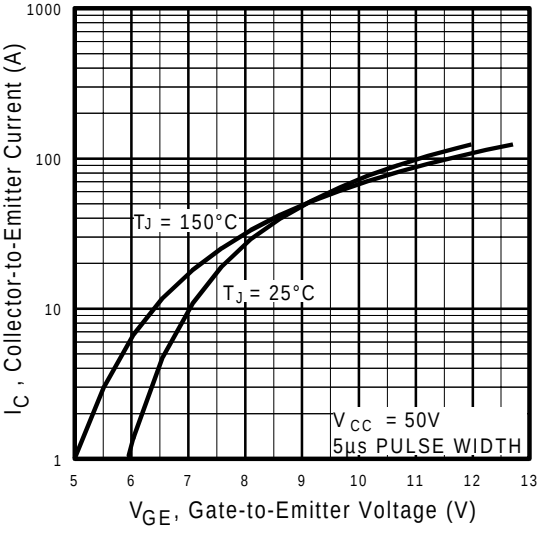


Fig. 3 - Typical Transfer Characteristics

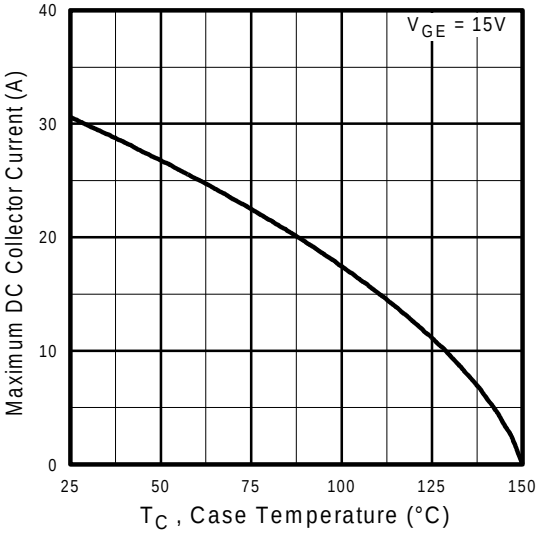


Fig. 4 - Maximum Collector Current vs. Case Temperature

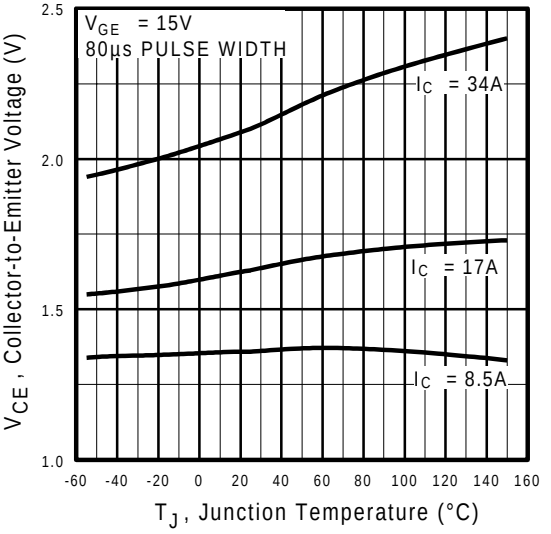


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

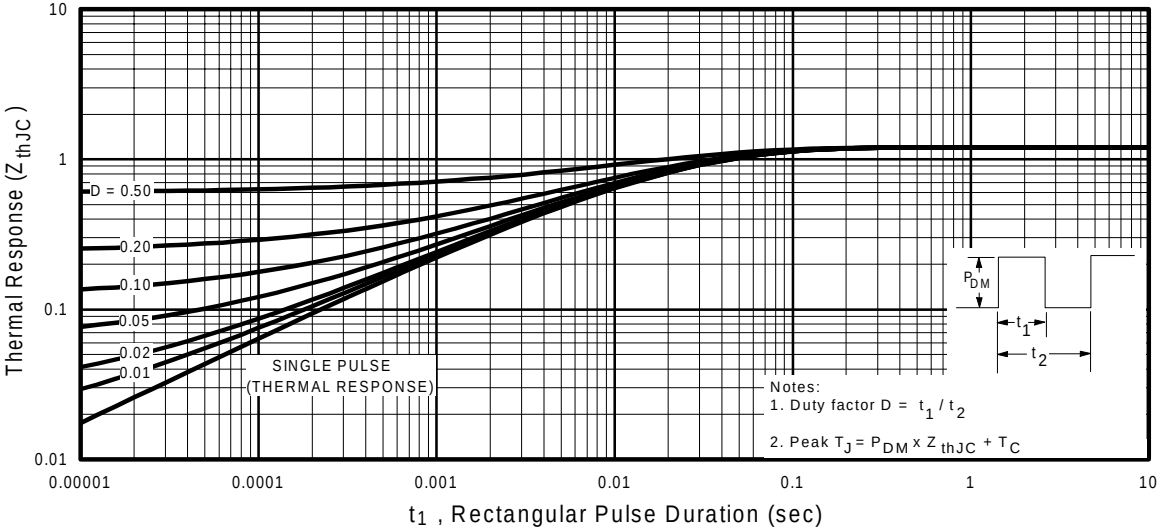


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

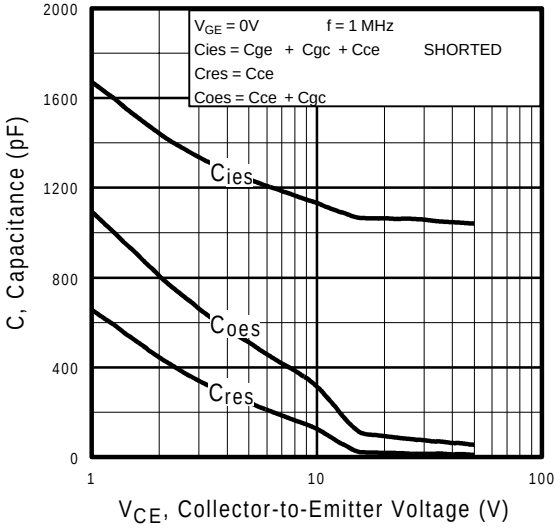


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

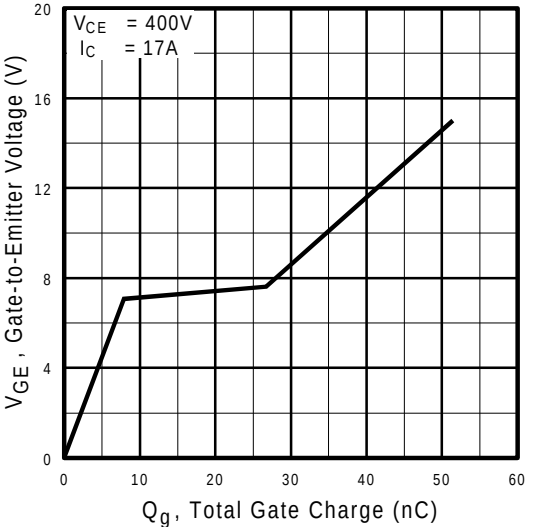


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

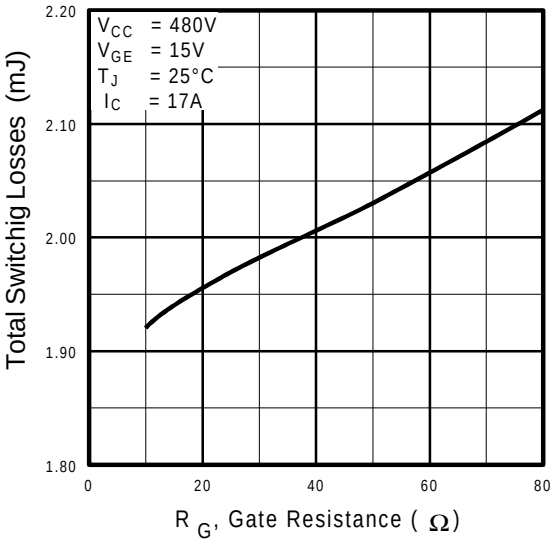


Fig. 9 - Typical Switching Losses vs. Gate Resistance

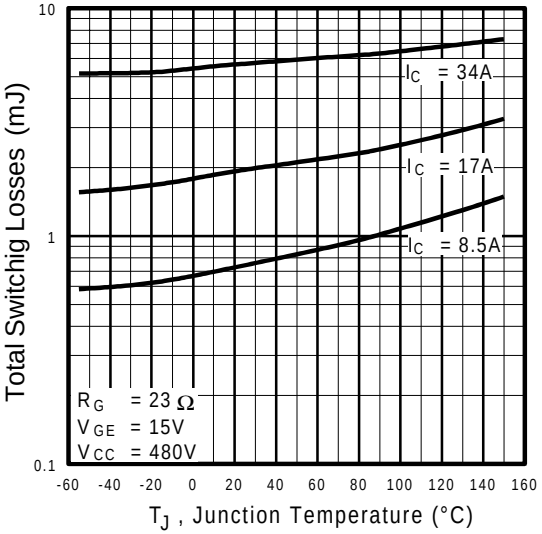


Fig. 10 - Typical Switching Losses vs. Junction Temperature

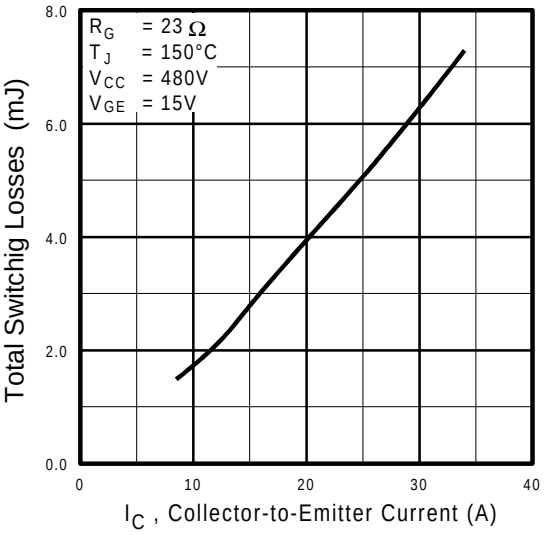


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

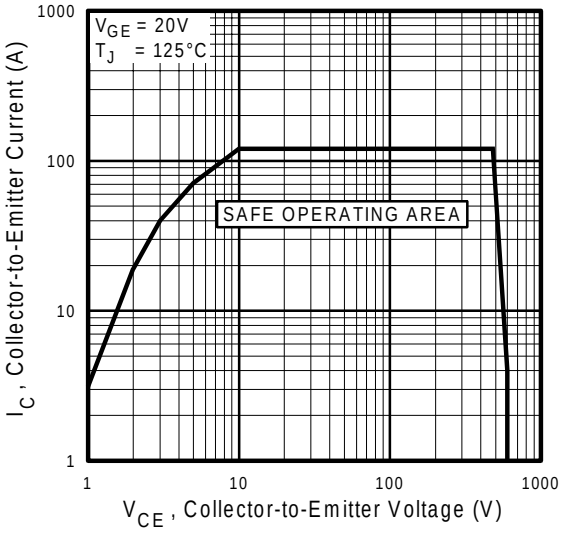


Fig. 12 - Turn-Off SOA

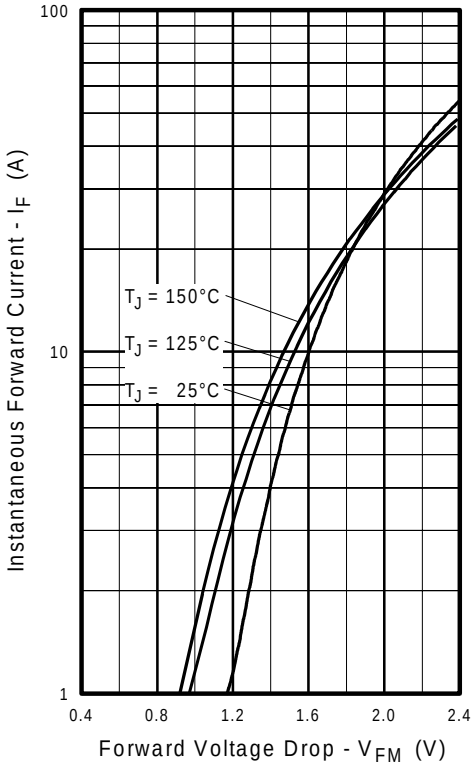


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

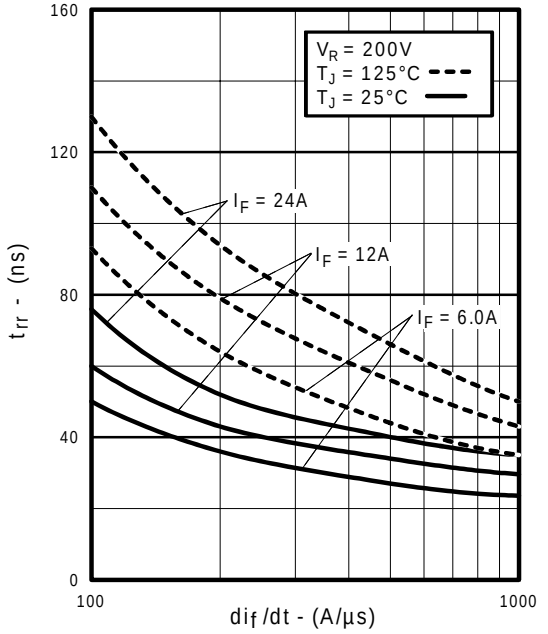


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

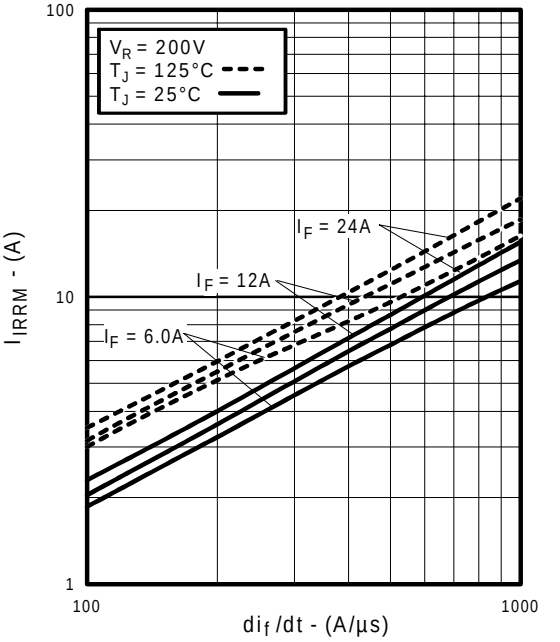


Fig. 15 - Typical Recovery Current vs. di_f/dt

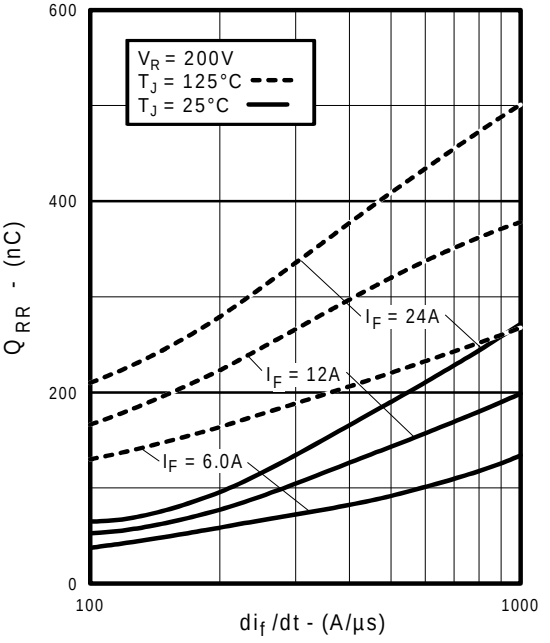


Fig. 16 - Typical Stored Charge vs. di_f/dt

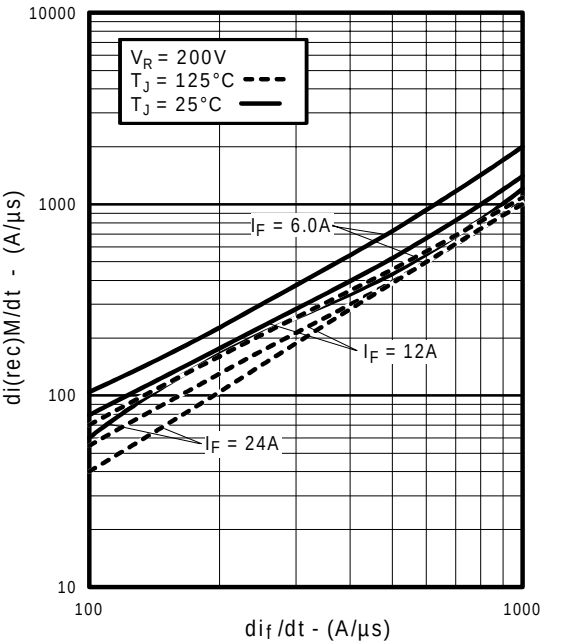


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

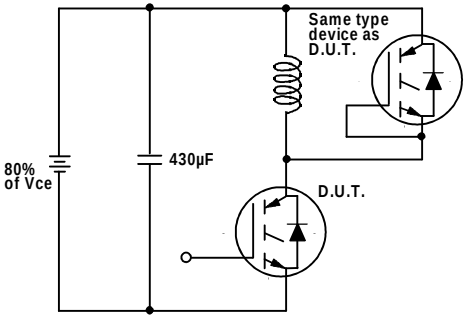


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

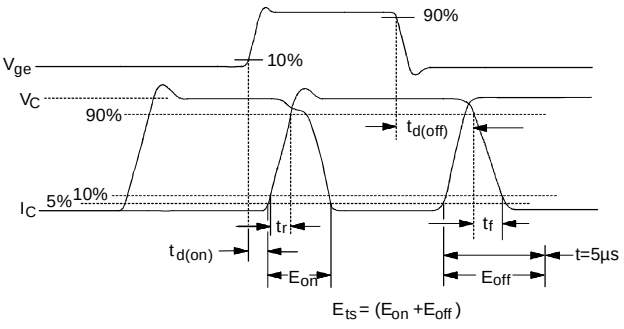


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

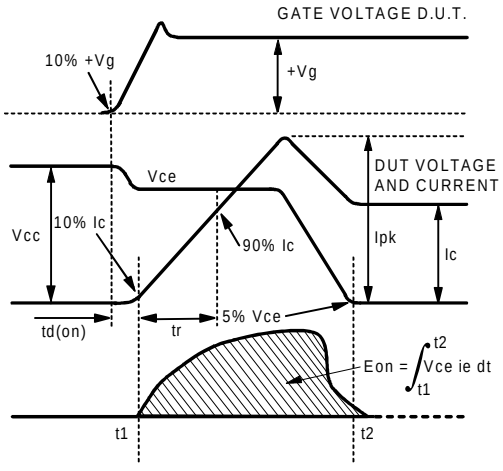


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

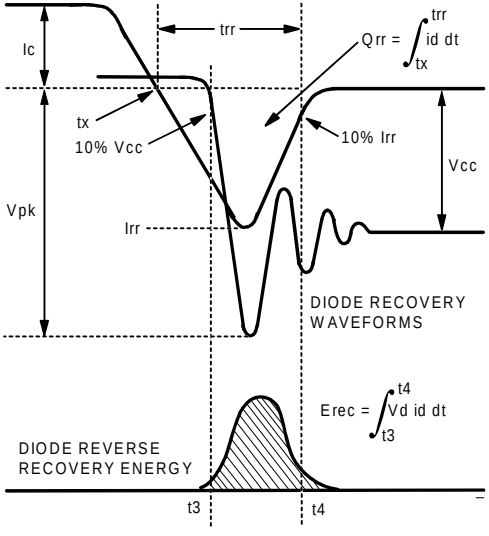


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

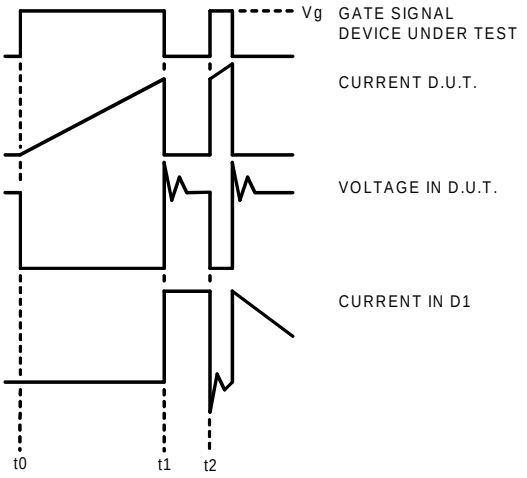


Figure 18e. *Macro Waveforms for Figure 18a's Test Circuit*

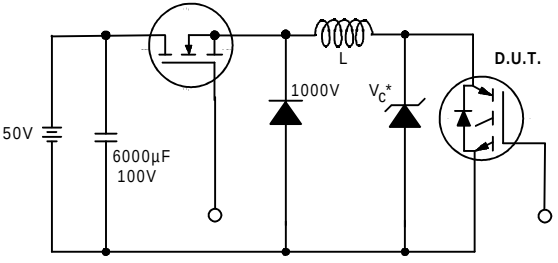


Figure 19. *Clamped Inductive Load Test Circuit*

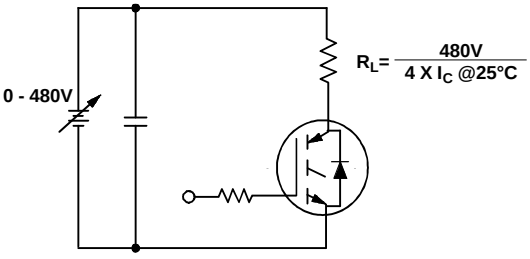


Figure 20. *Pulsed Collector Current Test Circuit*

Notes:

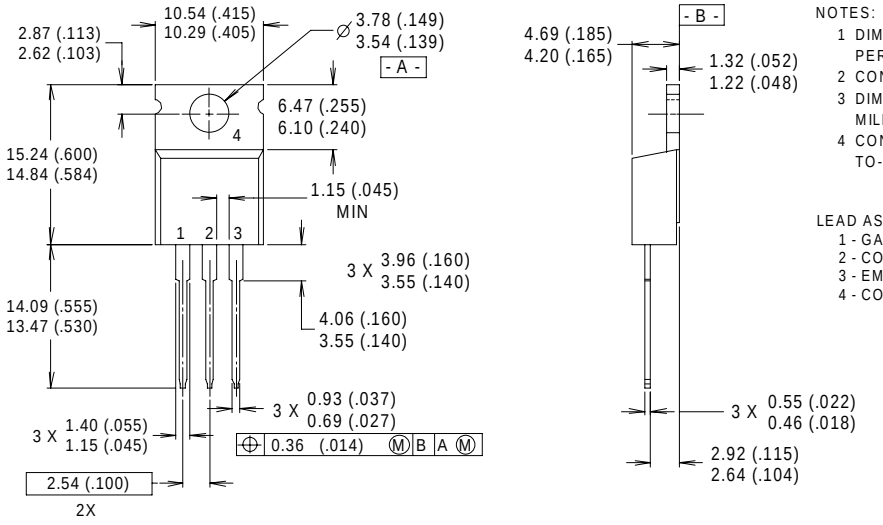
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 23W (figure 19)

③ Pulse width £ 80µs; duty factor £ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB

Dimensions in Millimeters and (Inches)

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936

http://www.irf.com/ Data and specifications subject to change without notice. 12/98

PD 91459B

International
IOR Rectifier

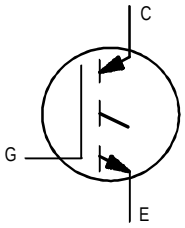
IRG4PC30F

INSULATED GATE BIPOLAR TRANSISTOR

Fast Speed IGBT

Features

- Fast: Optimized for medium operating frequencies (1-5 kHz in hard switching, >20 kHz in resonant mode).
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-247AC package



n-channel

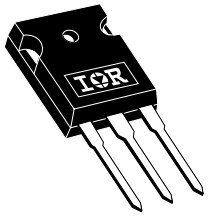
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.59V

@V_{GE} = 15V, I_C = 17A

Benefits

- Generation 4 IGBT's offer highest efficiency available
- IGBT's optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	31	A
I_C @ T_C = 100°C	Continuous Collector Current	17	
I_{CM}	Pulsed Collector Current ①	120	
I_{LM}	Clamped Inductive Load Current ②	120	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	10	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	℃
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

1229//00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.69	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.59	1.8	V	I_C = 17A V_{GE} = 15V
		—	1.99	—		I_C = 31A See Fig.2, 5
		—	1.7	—		I_C = 17A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	6.1	10	—	S	V_{CE} = 100V, I_C = 17A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	51	77	nC	I_C = 17A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	7.9	12		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	19	28		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	
t_r	Rise Time	—	15	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	200	300		I_C = 17A, V_{CC} = 480V
t_f	Fall Time	—	180	270		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.23	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	1.18	—		See Fig. 10, 11, 13, 14
E_{ts}	Total Switching Loss	—	1.41	2.0		
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	T_J = 150°C,
t_r	Rise Time	—	16	—		I_C = 17A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	290	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	350	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	2.5	—	mJ	See Fig. 13, 14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1100	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	74	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	14	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 23Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

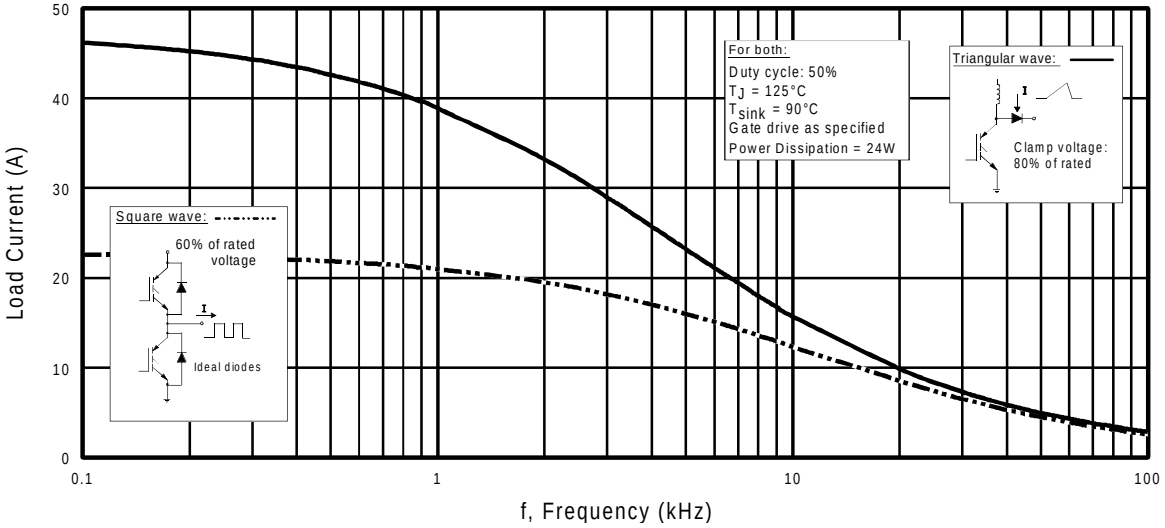


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

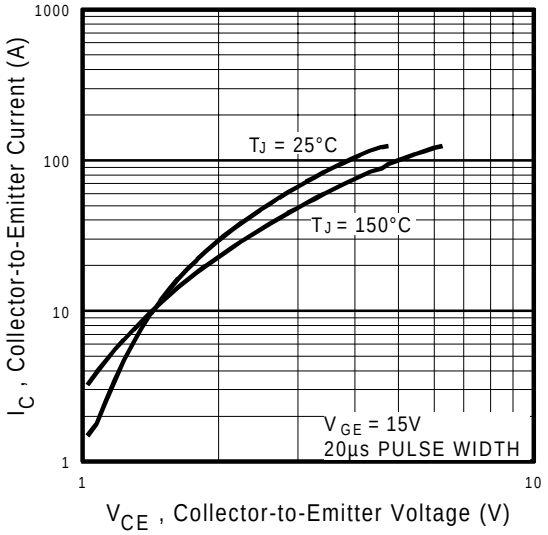


Fig. 2 - Typical Output Characteristics

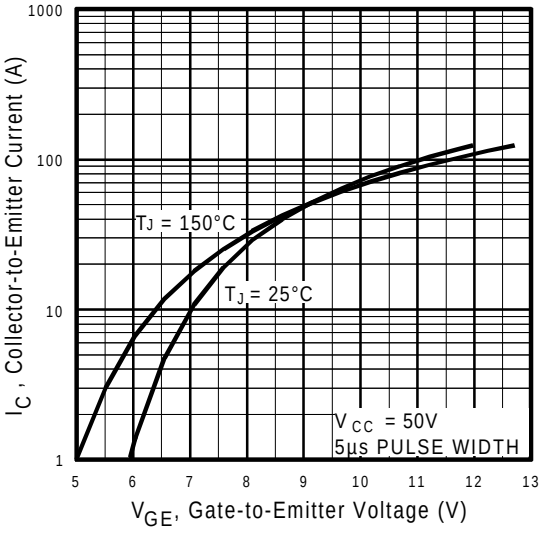


Fig. 3 - Typical Transfer Characteristics

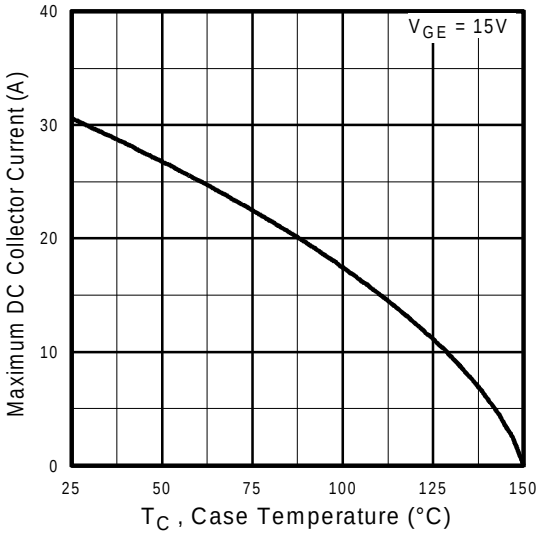


Fig. 4 - Maximum Collector Current vs. Case Temperature

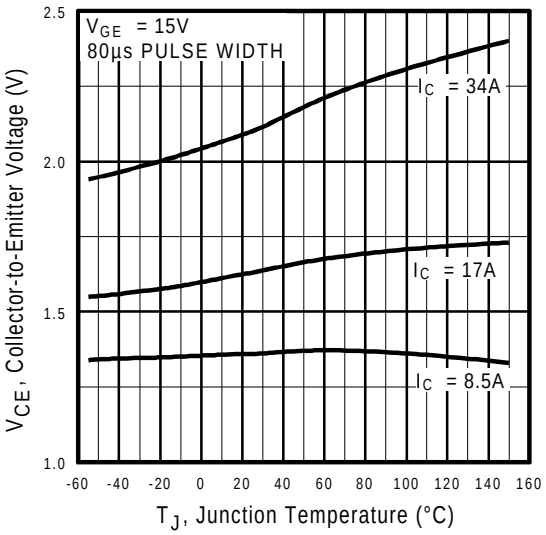


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

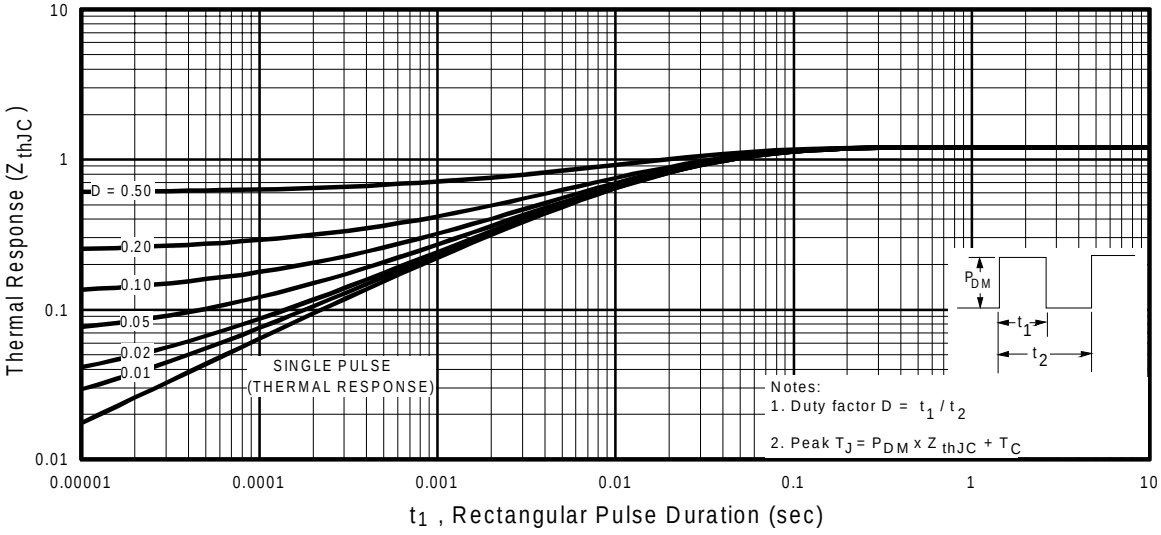


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

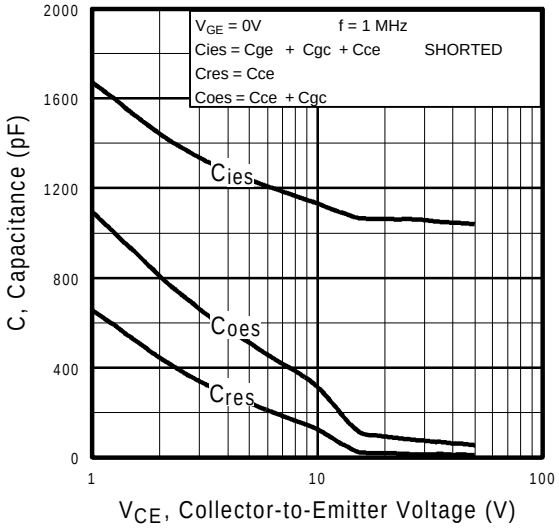


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

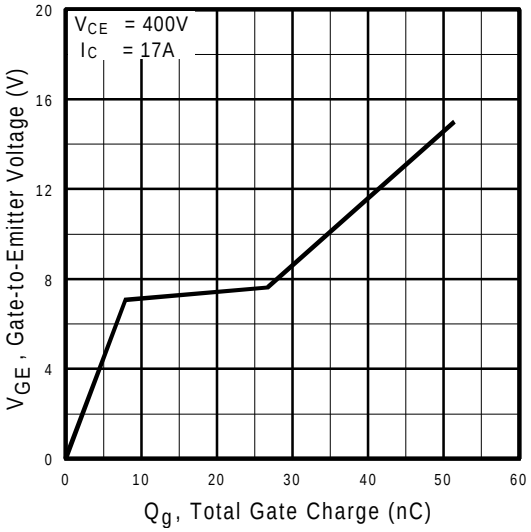


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

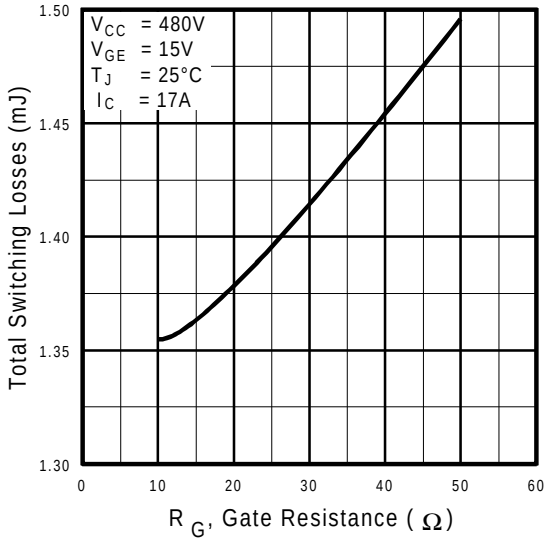


Fig. 9 - Typical Switching Losses vs. Gate Resistance

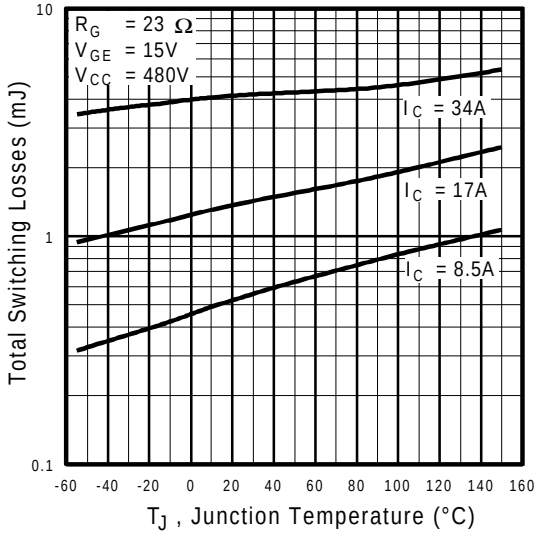


Fig. 10 - Typical Switching Losses vs. Junction Temperature

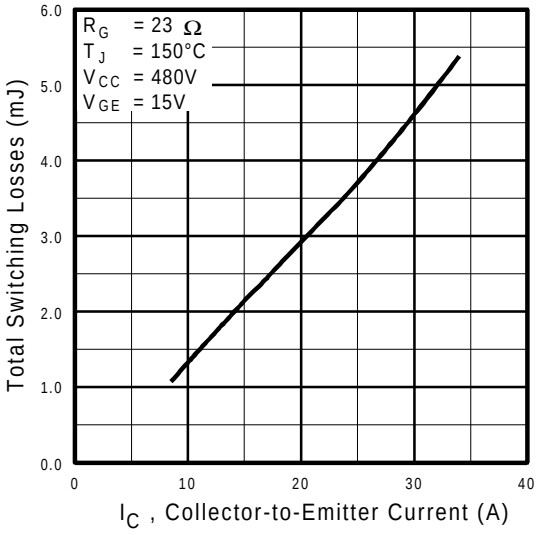


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

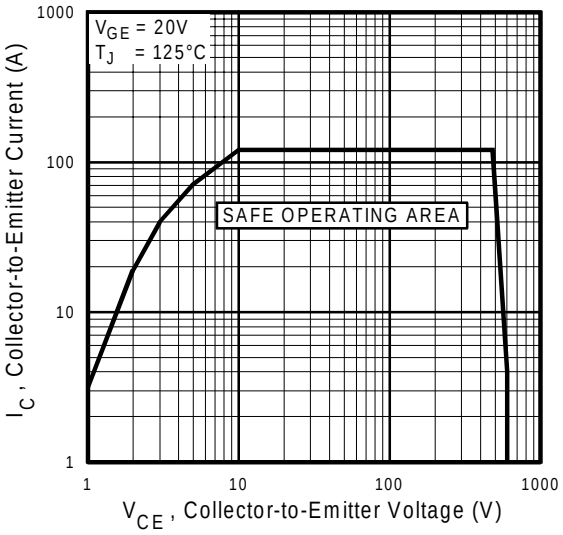


Fig. 12 - Turn-Off SOA

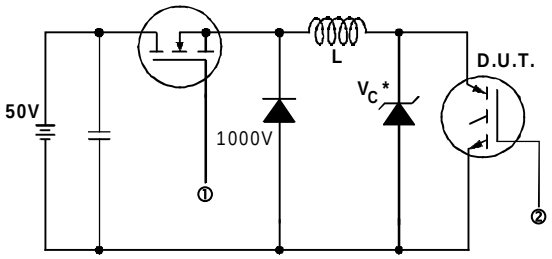


Fig. 13a - Clamped Inductive Load Test Circuit

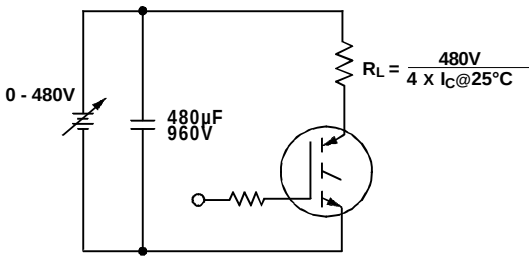


Fig. 13b - Pulsed Collector Current Test Circuit

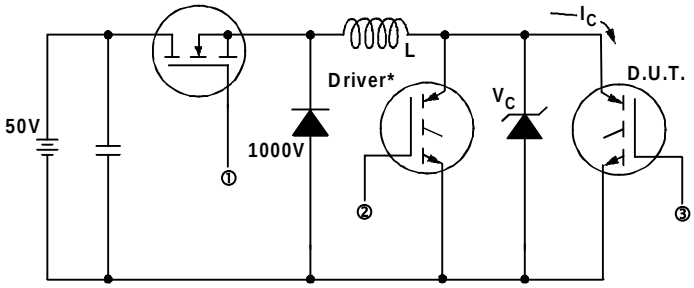


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

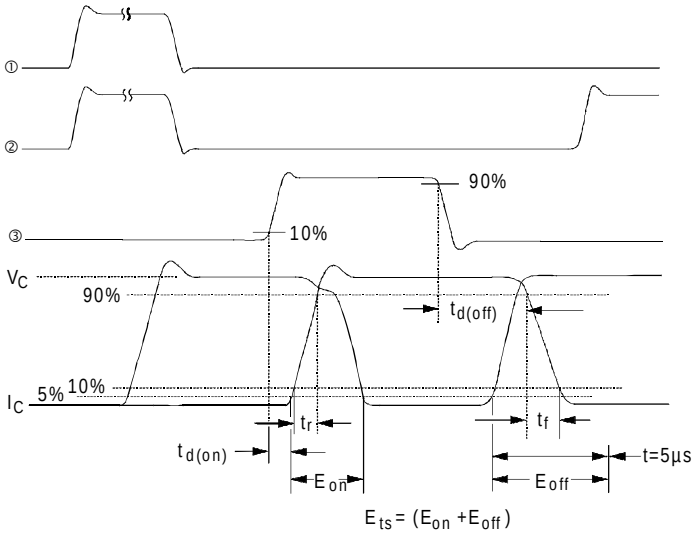
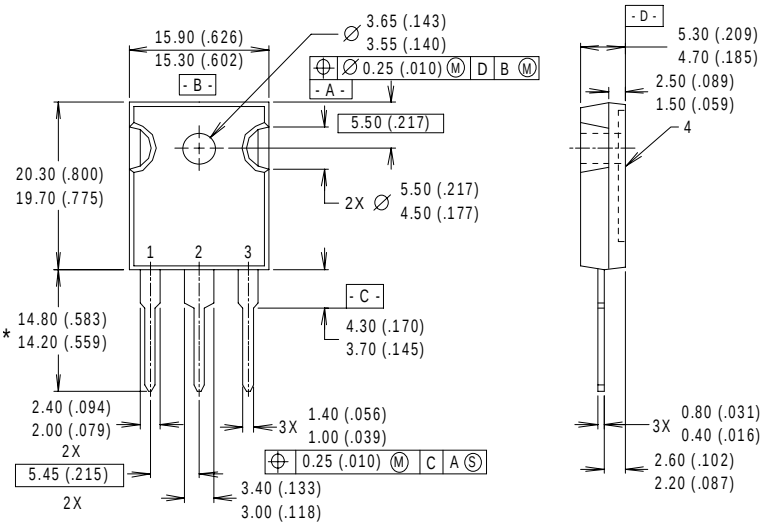


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
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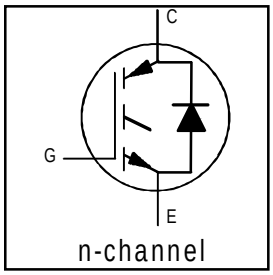
PD 91460B

International
IOR Rectifier

IRG4PC30FD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Fast CoPack IGBT



n-channel

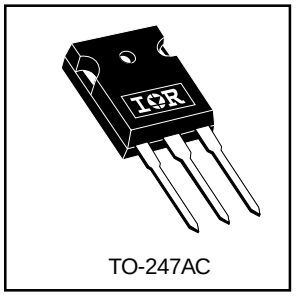
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.59V

@V_{GE} = 15V, I_C = 17A

Features

- Fast: Optimized for medium operating frequencies (1-5 kHz in hard switching, >20 kHz in resonant mode).
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-247AC package


TO-247AC

Benefits

- Generation -4 IGBT's offer highest efficiencies available
- IGBT's optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBT's . Minimized recovery characteristics require less/no snubbing
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	31	A
I_C @ T_C = 100°C	Continuous Collector Current	17	
I_{CM}	Pulsed Collector Current ①	120	
I_{LM}	Clamped Inductive Load Current ②	120	
I_F @ T_C = 100°C	Diode Continuous Forward Current	12	
I_{FM}	Diode Maximum Forward Current	120	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	1.2	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	2.5	
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.69	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.59	1.8	V	I_C = 17A V_{GE} = 15V
		—	1.99	—		I_C = 31A See Fig. 2, 5
		—	1.70	—		I_C = 17A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	6.1	10	—	S	V_{CE} = 100V, I_C = 17A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 12A See Fig. 13
		—	1.3	1.6		I_C = 12A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	51	77		I_C = 17A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	7.9	12	nC	V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	19	28		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	42	—		T_J = 25°C
t_r	Rise Time	—	26	—	ns	I_C = 17A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	230	350		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	160	230		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	0.63	—		diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	1.39	—	mJ	See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	—	2.02	3.9		
$t_{d(on)}$	Turn-On Delay Time	—	42	—		T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	—	27	—	ns	I_C = 17A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	310	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	310	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	3.2	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1100	—		V_{GE} = 0V
C_{oes}	Output Capacitance	—	74	—	pF	V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	14	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	42	60	ns	T_J = 25°C See Fig.
		—	80	120		T_J = 125°C 14 I_F = 12A
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	6.0	A	T_J = 25°C See Fig.
		—	5.6	10		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	80	180	nC	T_J = 25°C See Fig.
		—	220	600		T_J = 125°C 16 di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	180	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	120	—		T_J = 125°C 17

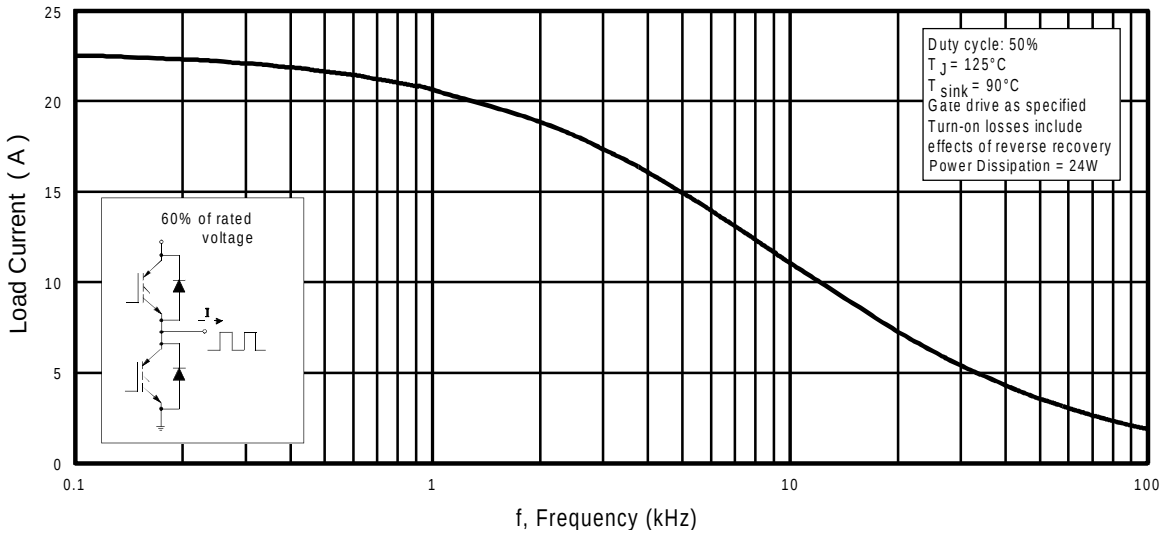


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

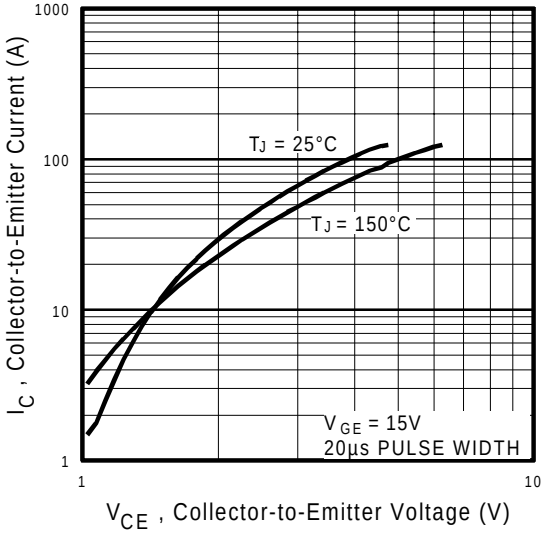


Fig. 2 - Typical Output Characteristics

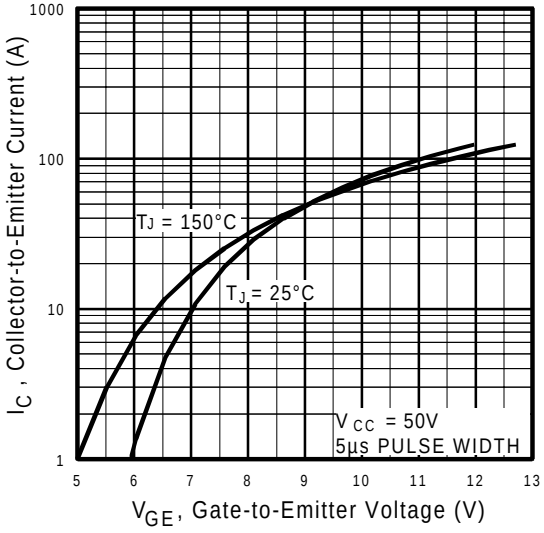


Fig. 3 - Typical Transfer Characteristics

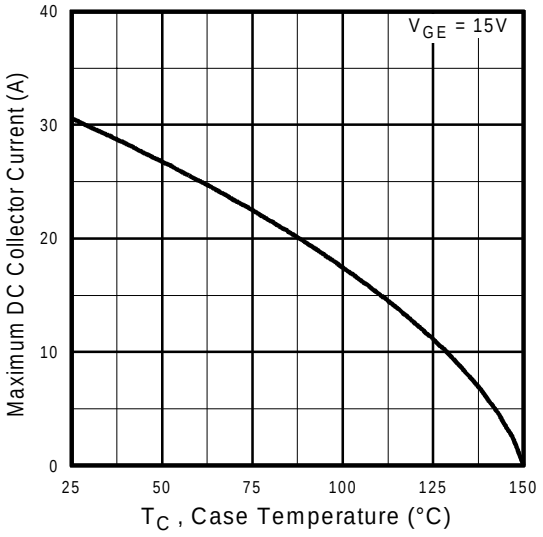


Fig. 4 - Maximum Collector Current vs. Case Temperature

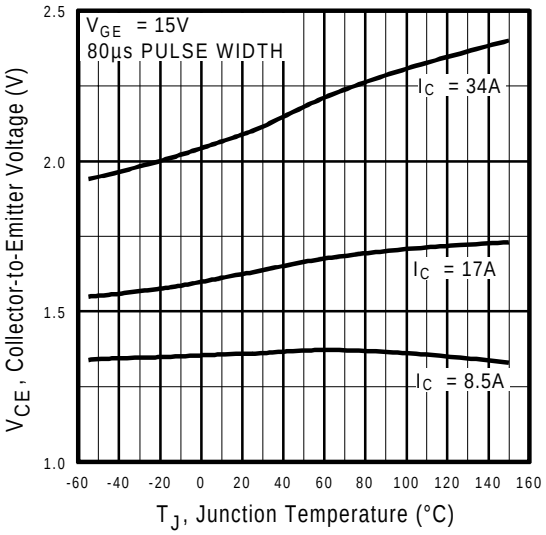


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

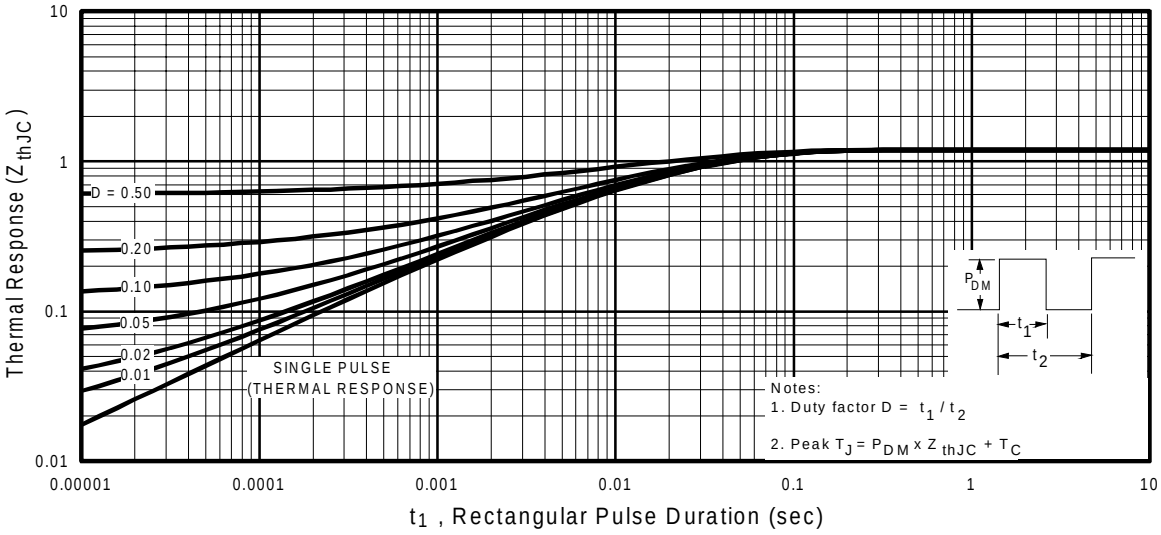


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

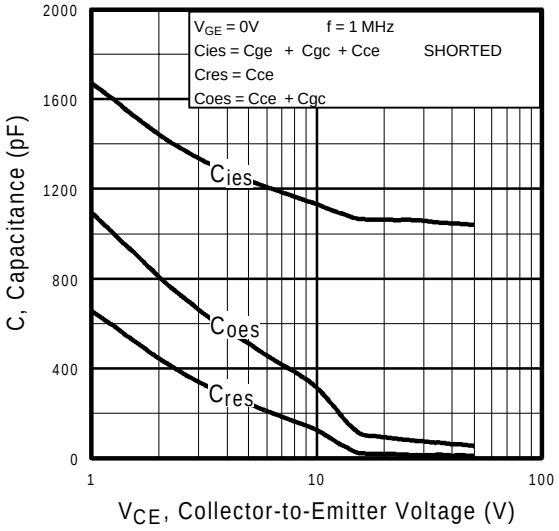


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

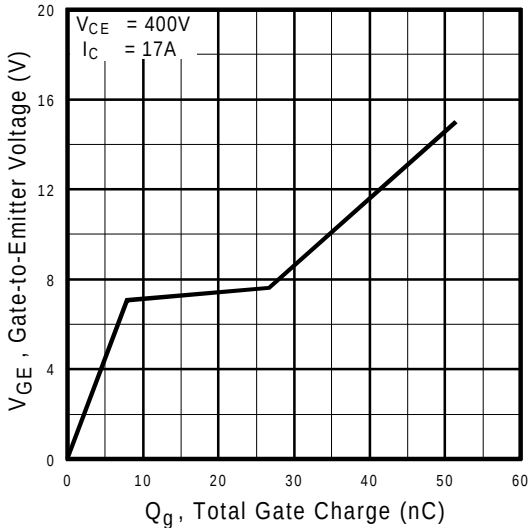


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

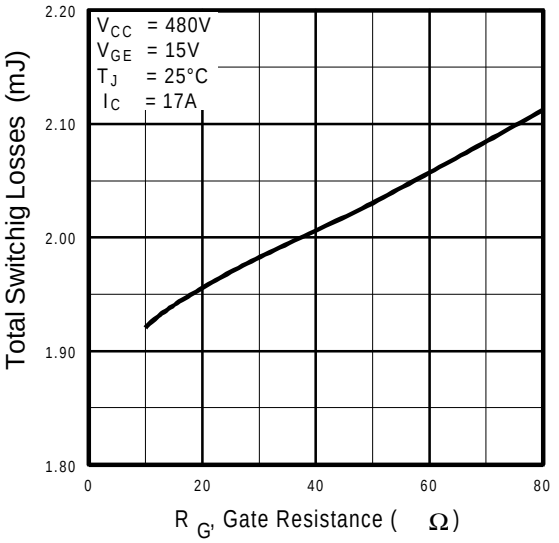


Fig. 9 - Typical Switching Losses vs. Gate Resistance

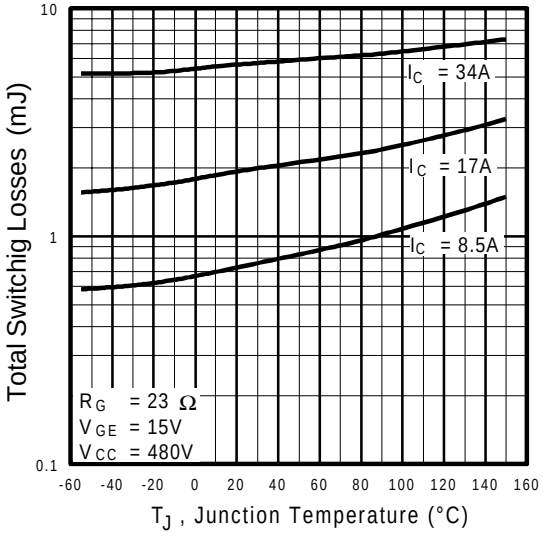


Fig. 10 - Typical Switching Losses vs. Junction Temperature

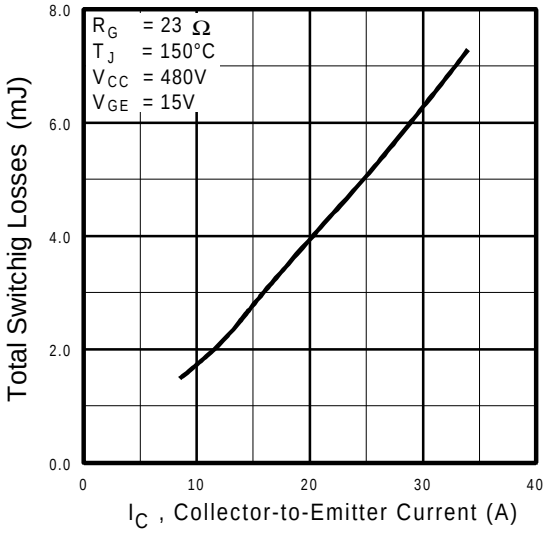


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

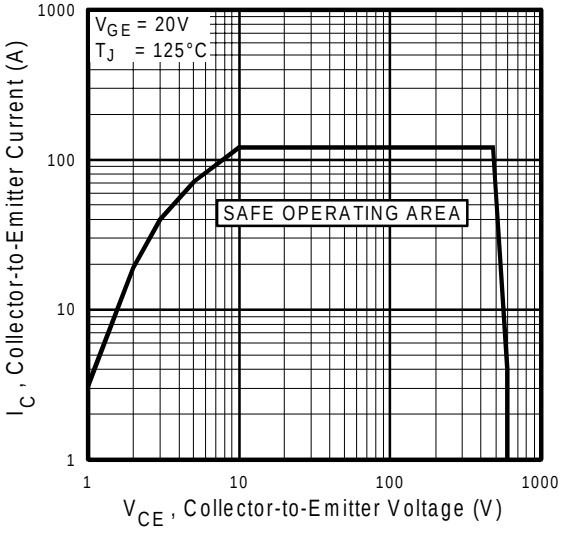


Fig. 12 - Turn-Off SOA

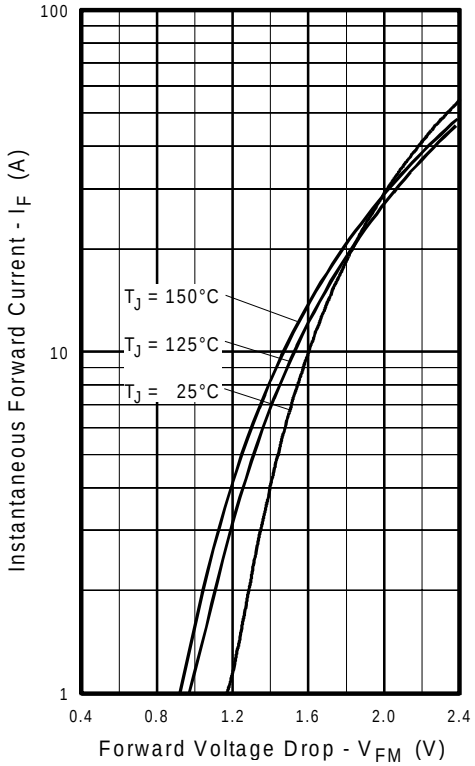


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

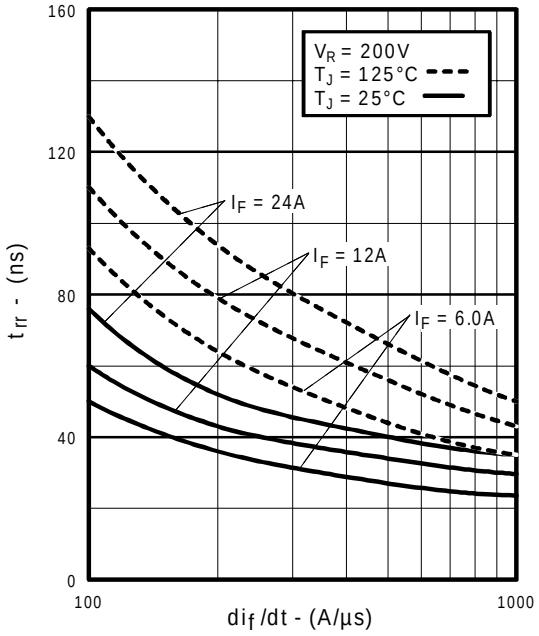


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

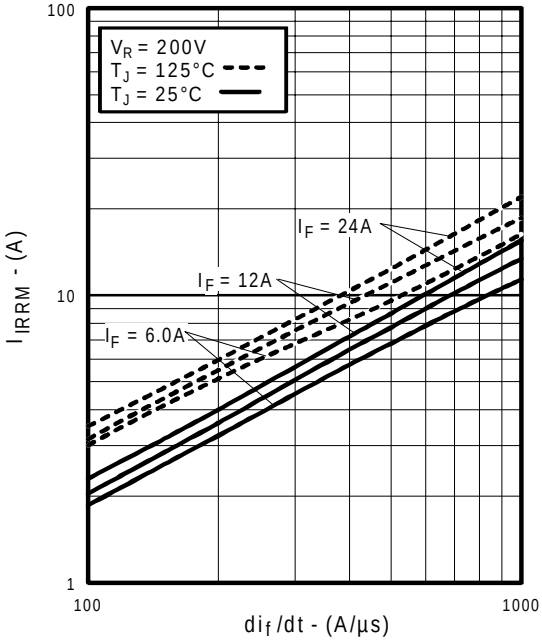


Fig. 15 - Typical Recovery Current vs. di_f/dt

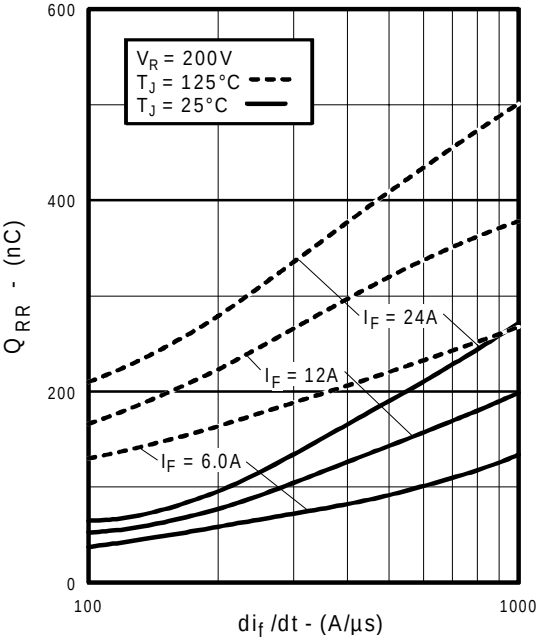


Fig. 16 - Typical Stored Charge vs. di_f/dt

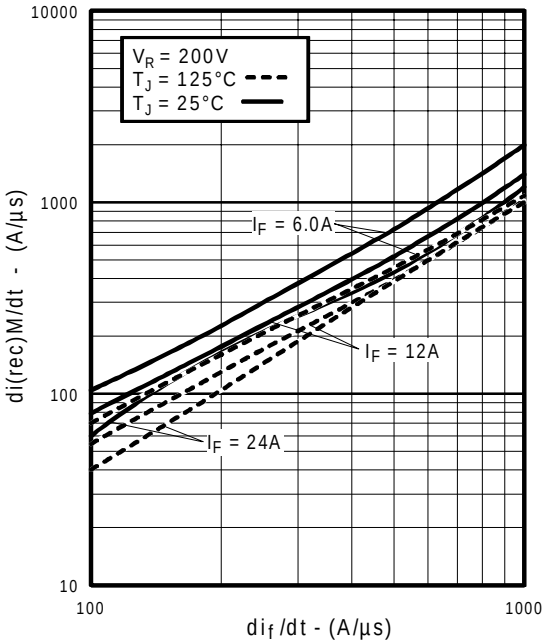


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

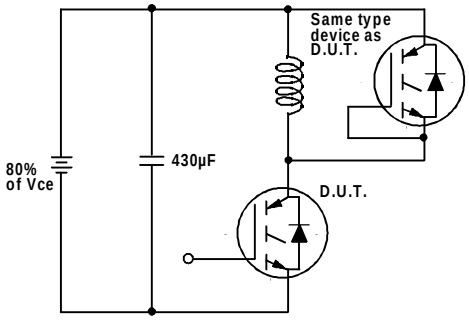


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

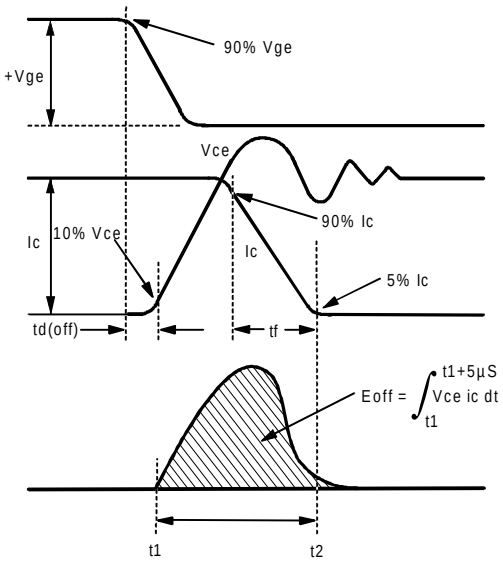


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

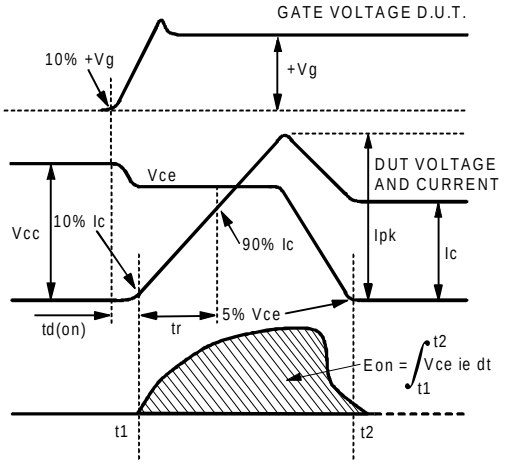


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

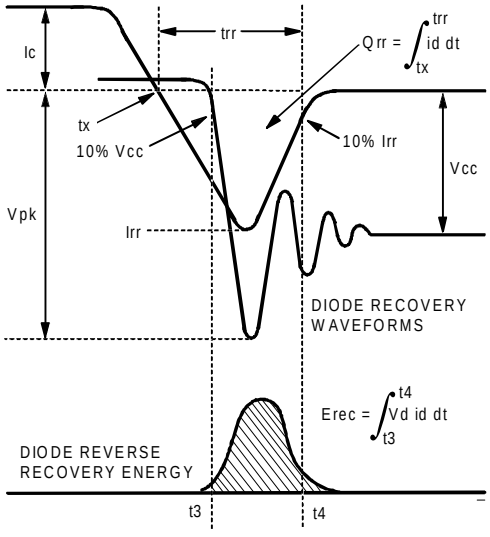


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

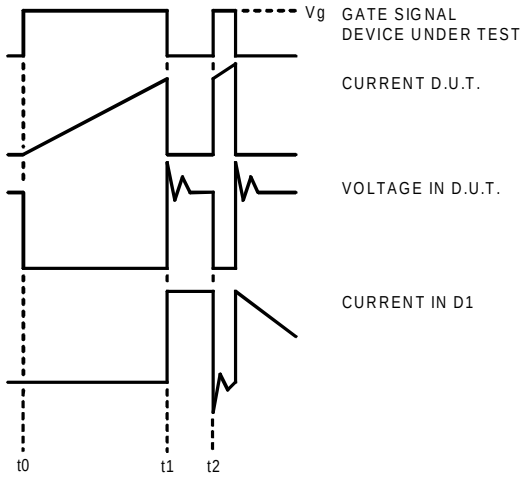


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

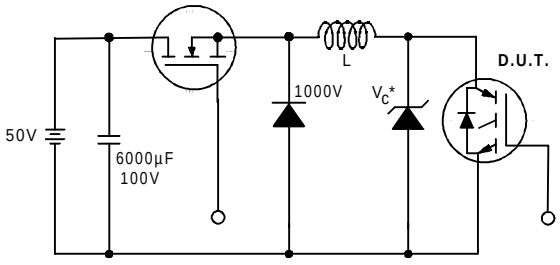


Figure 19. Clamped Inductive Load Test Circuit

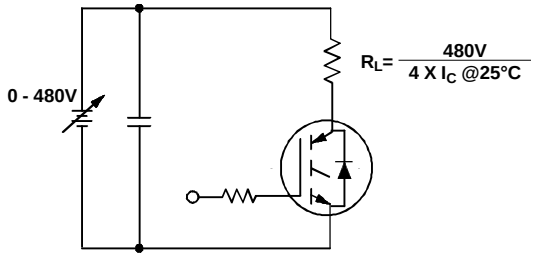


Figure 20. Pulsed Collector Current Test Circuit

Notes:

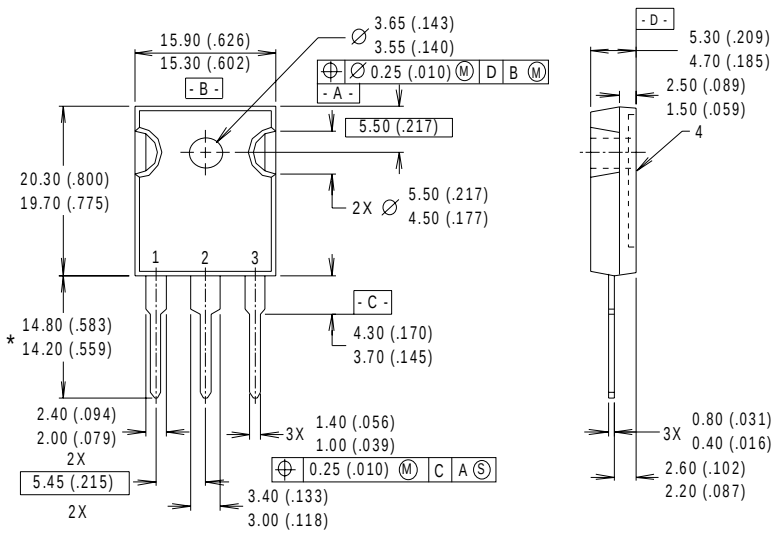
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 23Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
Data and specifications subject to change without notice. 12/00

PD - 94069

International
IOR Rectifier

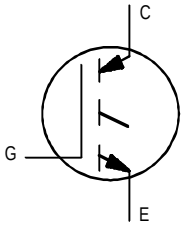
IRG4BC30S-S

INSULATED GATE BIPOLAR TRANSISTOR

Standard Speed IGBT

Features

- Standard: optimized for minimum saturation voltage and low operating frequencies (< 1kHz)
- Generation 4 IGBT design provides tight parameter distribution and high efficiency



n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.4V

@V_{GE} = 15V, I_C = 18A

Benefits

- Generation 4 IGBTs offer highest efficiency available
- IGBTs optimized for specified application conditions



D^2Pak

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	34	A
I_C @ T_C = 100°C	Continuous Collector Current	18	
I_{CM}	Pulsed Collector Current ①	68	
I_{LM}	Clamped Inductive Load Current ②	68	
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	10	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	1.44	—	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.75	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.40	1.6	V	I_C = 18A V_{GE} = 15V
		—	1.84	—		I_C = 34A See Fig. 2, 5
		—	1.45	—		I_C = 18A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	6.0	11	—	S	V_{CE} = 100V, I_C = 18A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	50	75	nC	I_C = 18A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	7.3	11		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	17	26		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	22	—	ns	
t_r	Rise Time	—	18	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	540	810		I_C = 18A, V_{CC} = 480V
t_f	Fall Time	—	390	590		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.26	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	3.45	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	3.71	5.6		
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	T_J = 150°C,
t_r	Rise Time	—	19	—		I_C = 18A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	790	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	760	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	6.55	—	mJ	See Fig. 11, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1100	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	72	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	13	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature (See fig. 13b).

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 23Ω, (See fig. 13a).

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

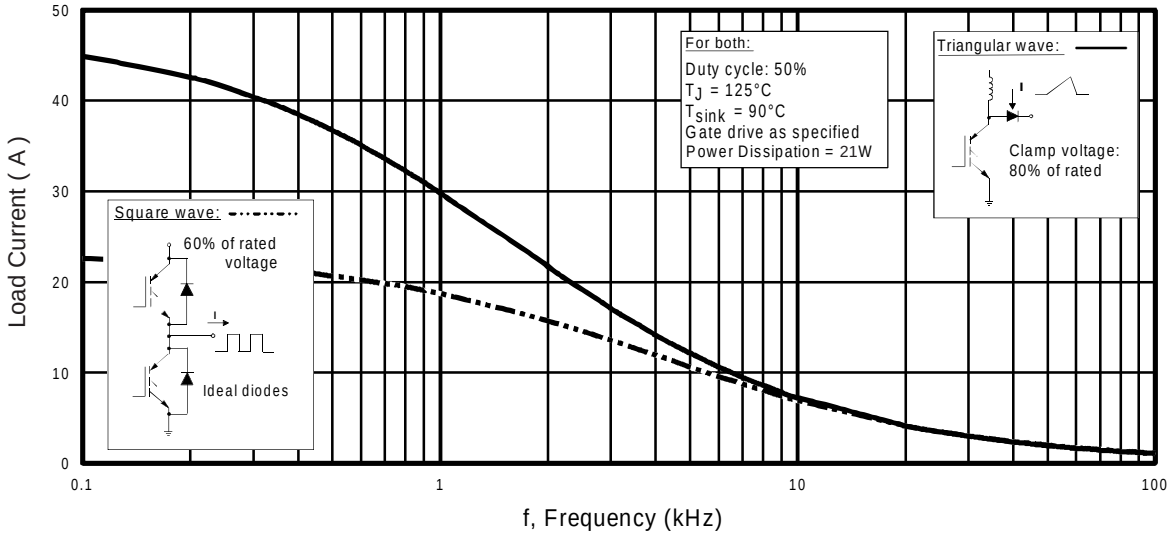


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

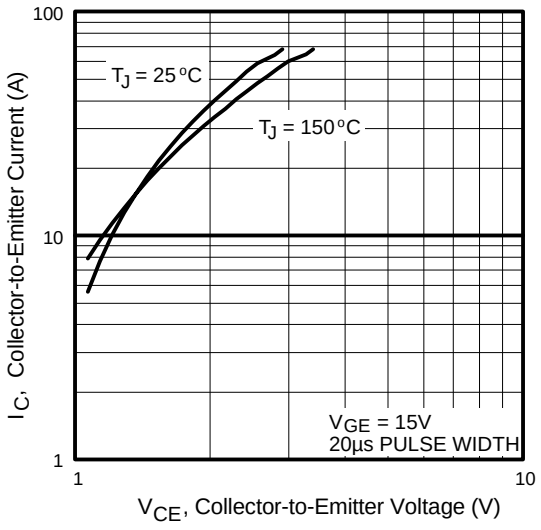


Fig. 2 - Typical Output Characteristics

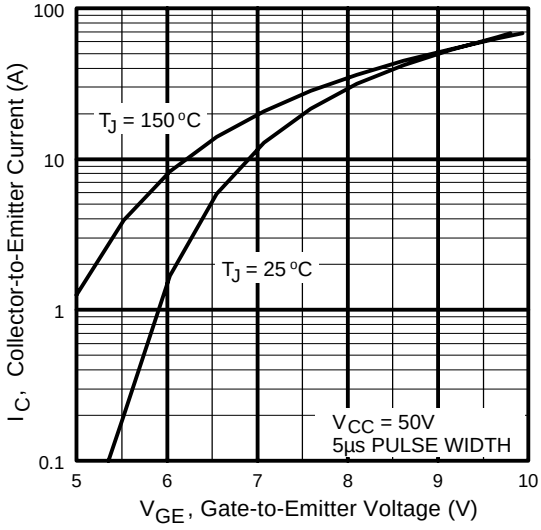


Fig. 3 - Typical Transfer Characteristics

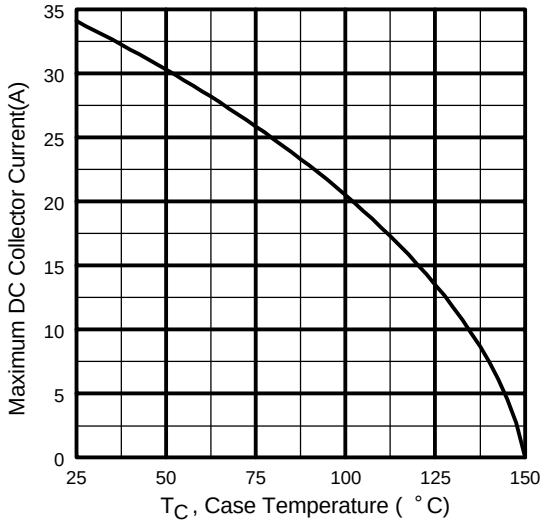


Fig. 4 - Maximum Collector Current vs. Case Temperature

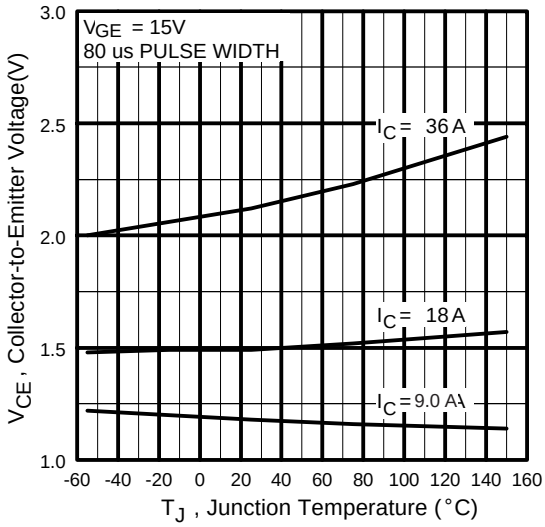


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

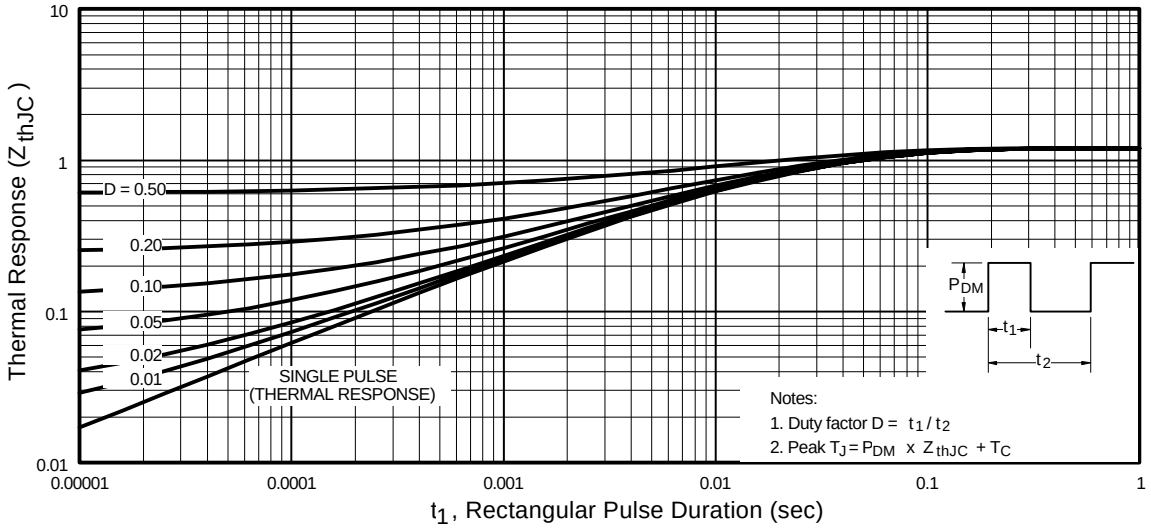


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

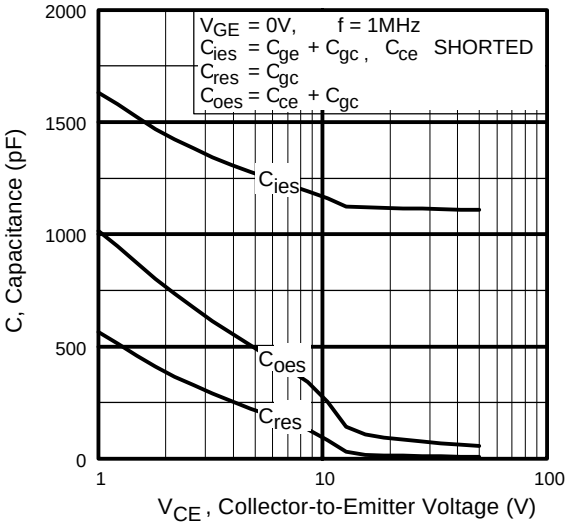


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

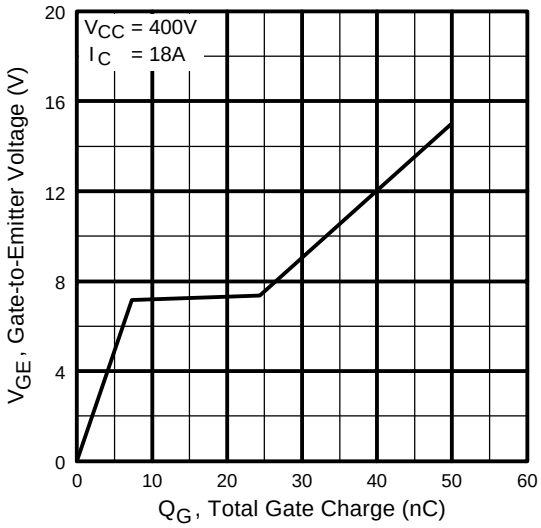


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

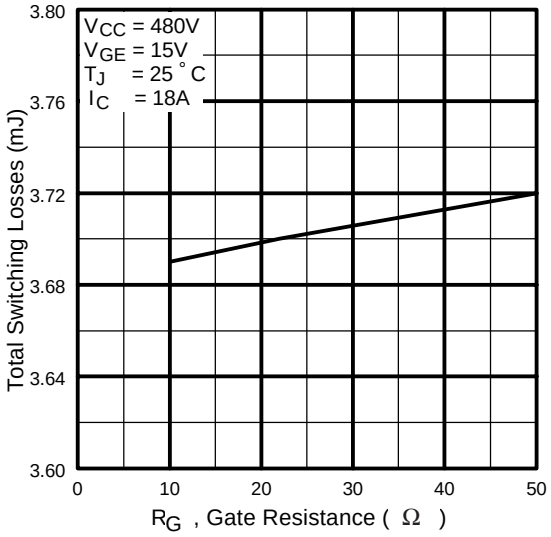


Fig. 9 - Typical Switching Losses vs. Gate Resistance

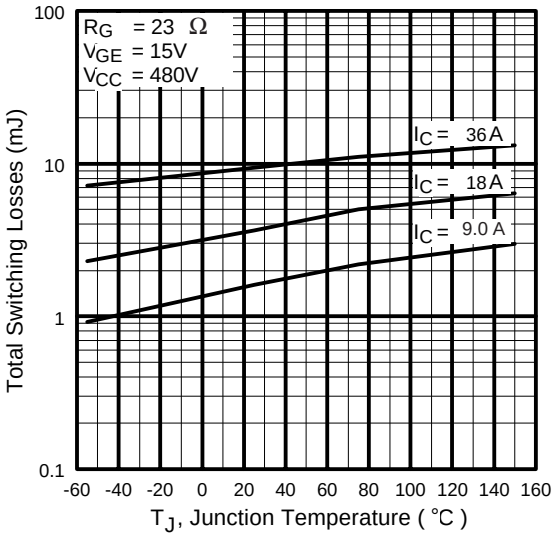


Fig. 10 - Typical Switching Losses vs. Junction Temperature

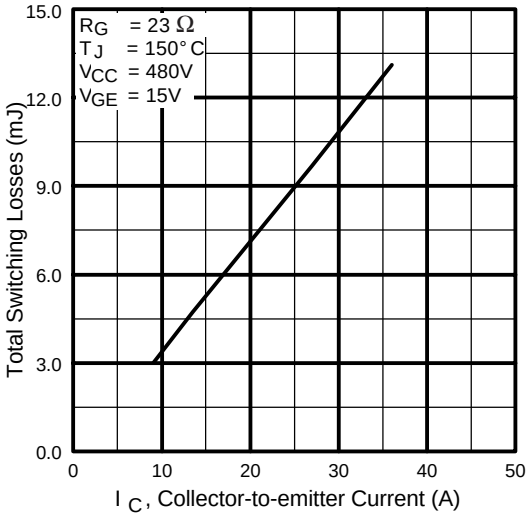


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

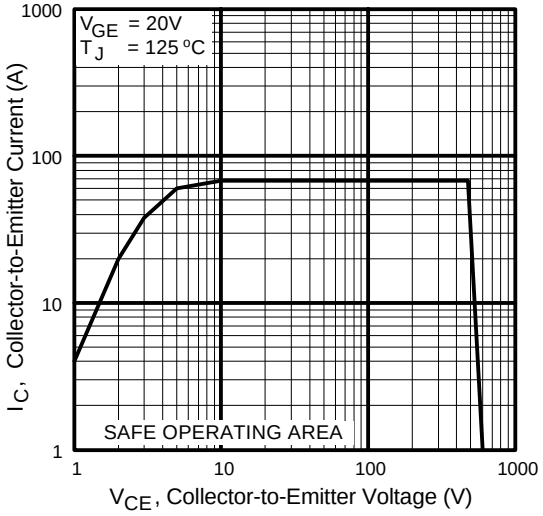


Fig. 12 - Turn-Off SOA

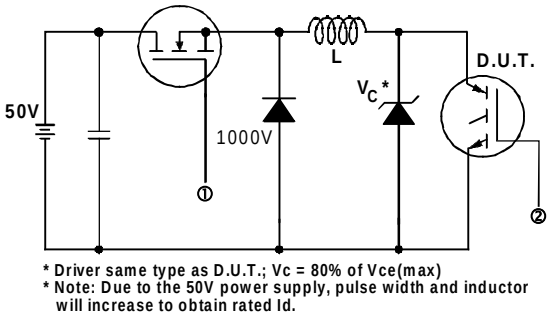


Fig. 13a - Clamped Inductive Load Test Circuit

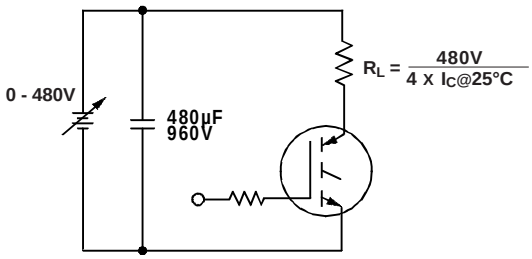


Fig. 13b - Pulsed Collector Current Test Circuit

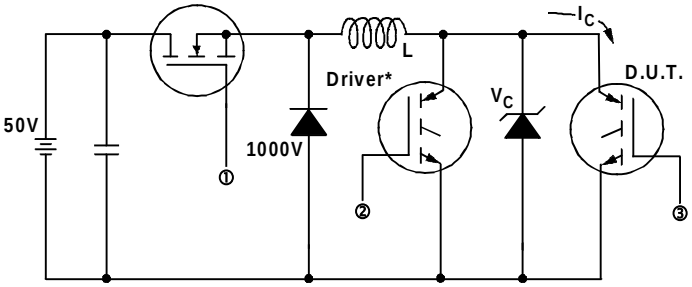


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

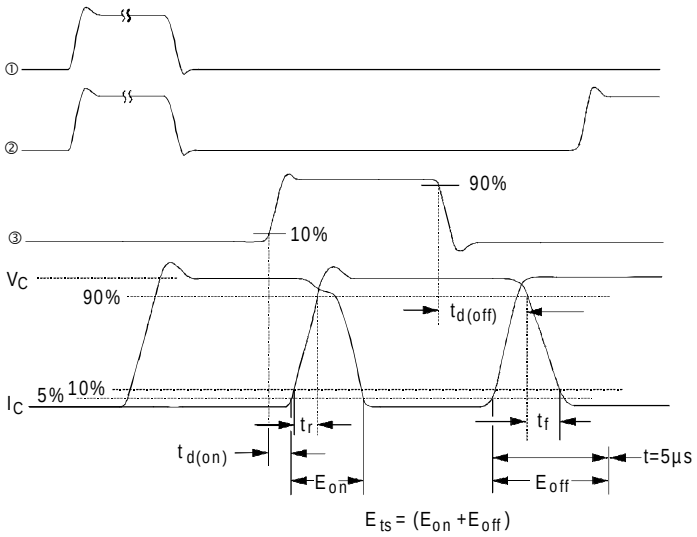
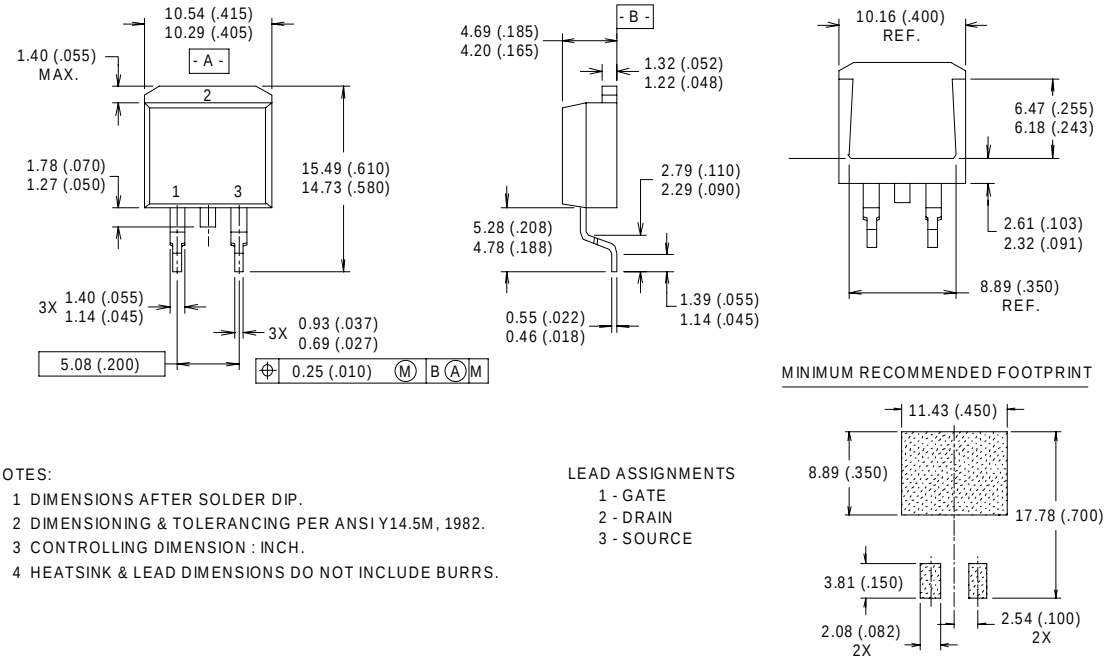


Fig. 14b - Switching Loss Waveforms

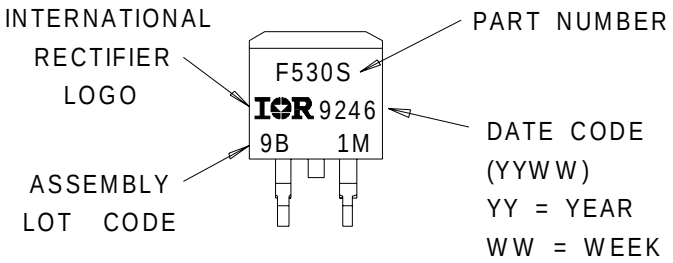
D²Pak Package Outline



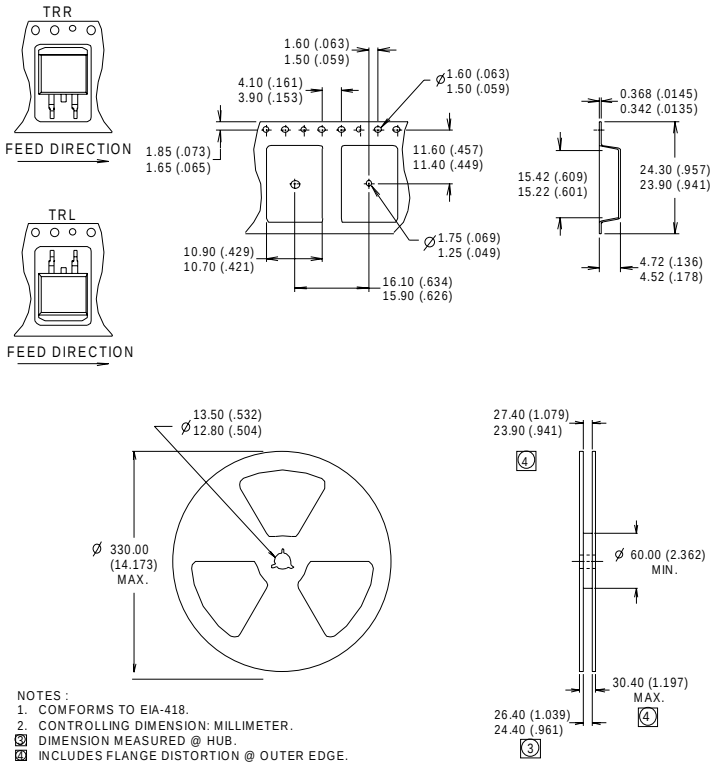
NOTES:
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

D²Pak Part Marking Information



D²Pak Tape & Reel Information



NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.12/00

PD - 91593A

International
IOR Rectifier

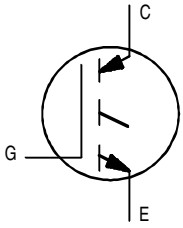
IRG4BC30S

INSULATED GATE BIPOLAR TRANSISTOR

Standard Speed IGBT

Features

- Standard: optimized for minimum saturation voltage and low operating frequencies (< 1kHz)
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-220AB package



n-channel

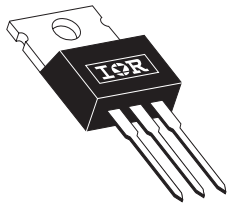
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.4V

@V_{GE} = 15V, I_C = 18A

Benefits

- Generation 4 IGBTs offer highest efficiency available
- IGBTs optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	34	A
I_C @ T_C = 100°C	Continuous Collector Current	18	
I_{CM}	Pulsed Collector Current ①	68	
I_{LM}	Clamped Inductive Load Current ②	68	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	10	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	80	
Wt	Weight	2.0 (0.07)	—	g (oz)

4/17/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.75	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.40	1.6	V	I_C = 18A V_{GE} = 15V
		—	1.84	—		I_C = 34A See Fig.2, 5
		—	1.45	—		I_C = 18A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	6.0	11	—	S	V_{CE} = 100V, I_C = 18A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	50	75	nC	I_C = 18A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	7.3	11		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	17	26		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	22	—	ns	
t_r	Rise Time	—	18	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	540	810		I_C = 18A, V_{CC} = 480V
t_f	Fall Time	—	390	590		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.26	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	3.45	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	3.71	5.6		
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	T_J = 150°C,
t_r	Rise Time	—	19	—		I_C = 18A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	790	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	760	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	6.55	—	mJ	See Fig. 11, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1100	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	72	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	13	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 23Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

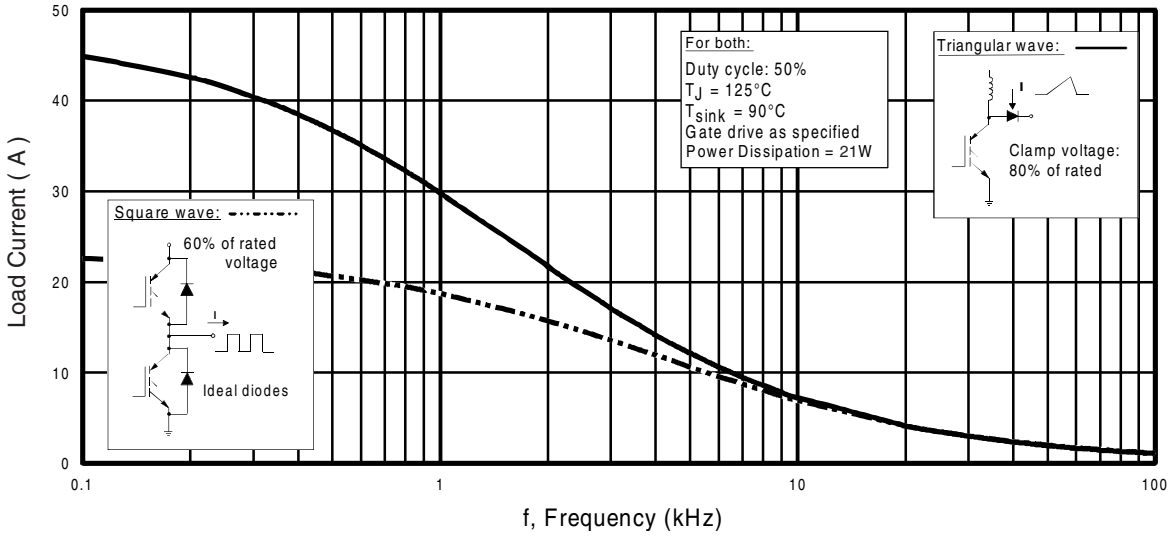


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

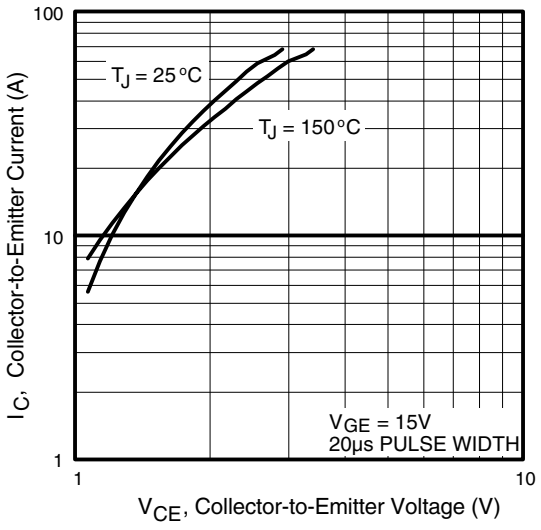


Fig. 2 - Typical Output Characteristics

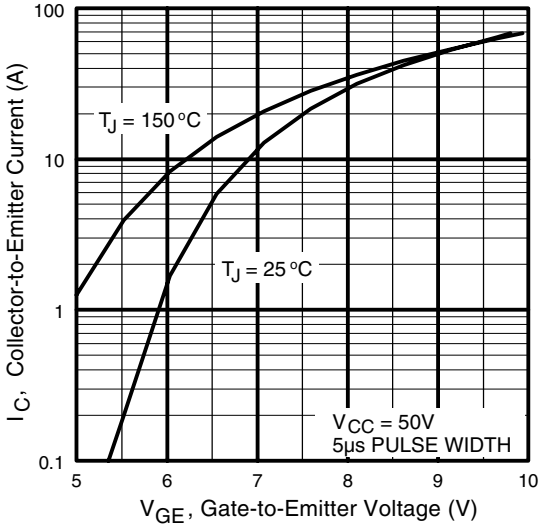


Fig. 3 - Typical Transfer Characteristics

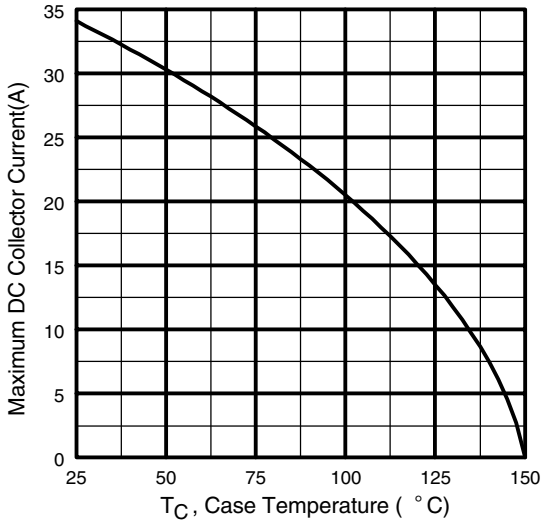


Fig. 4 - Maximum Collector Current vs. Case Temperature

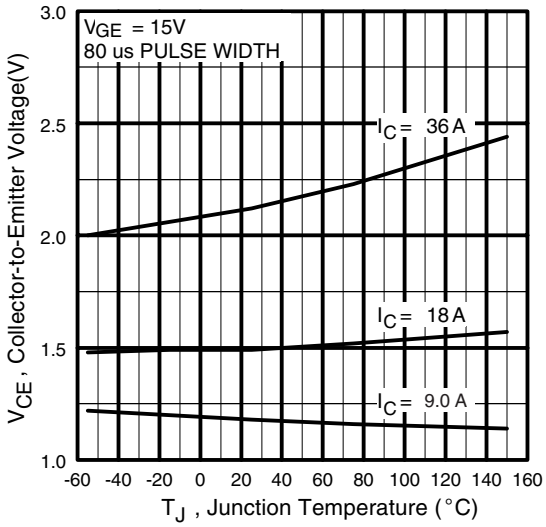


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

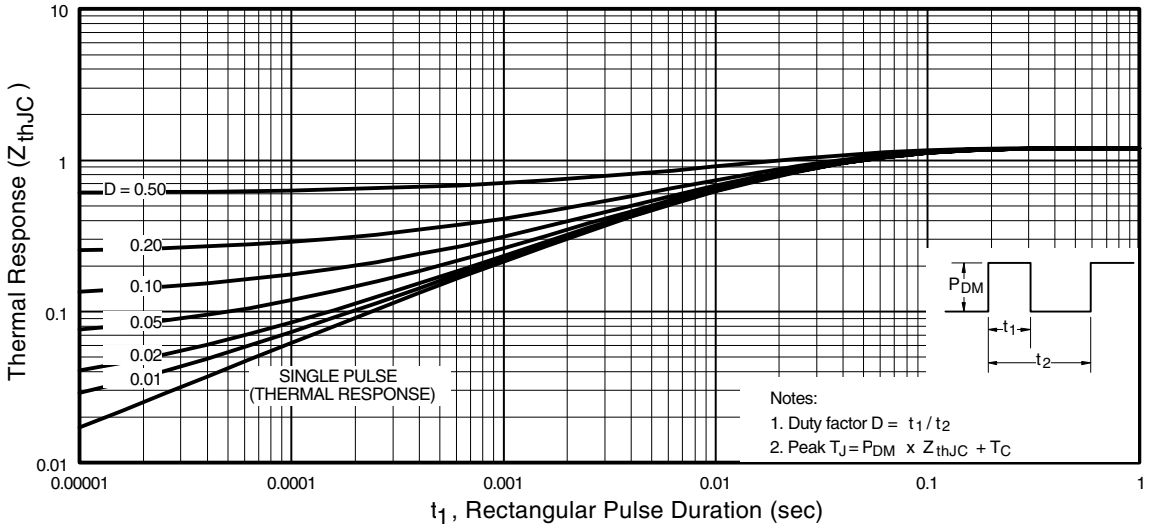


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

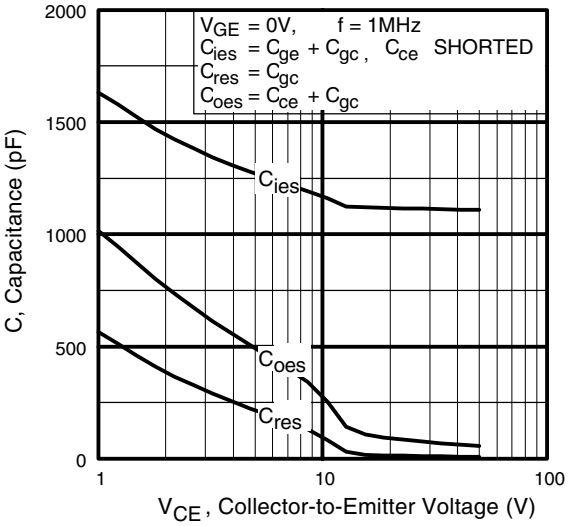


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

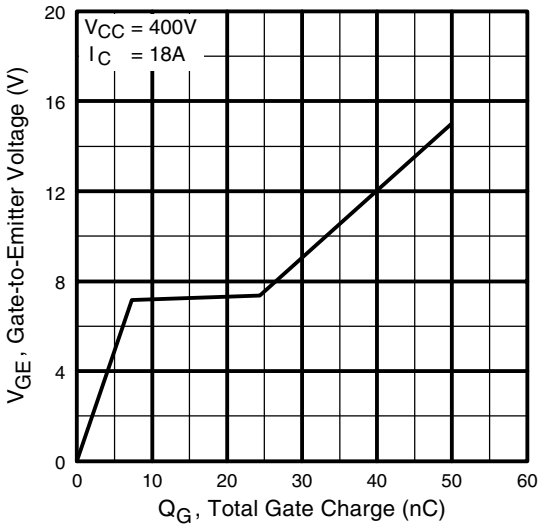


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

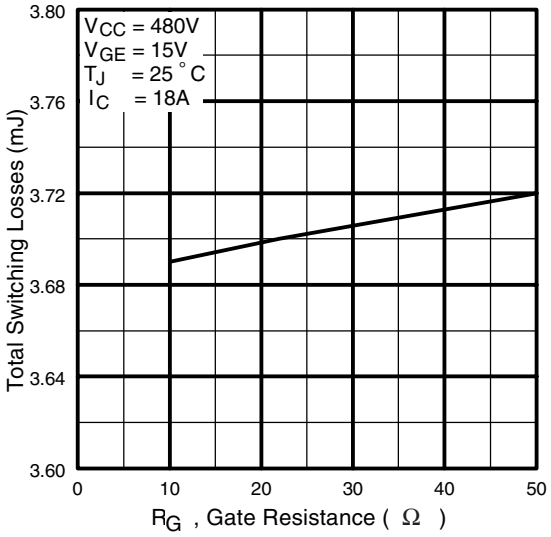


Fig. 9 - Typical Switching Losses vs. Gate Resistance

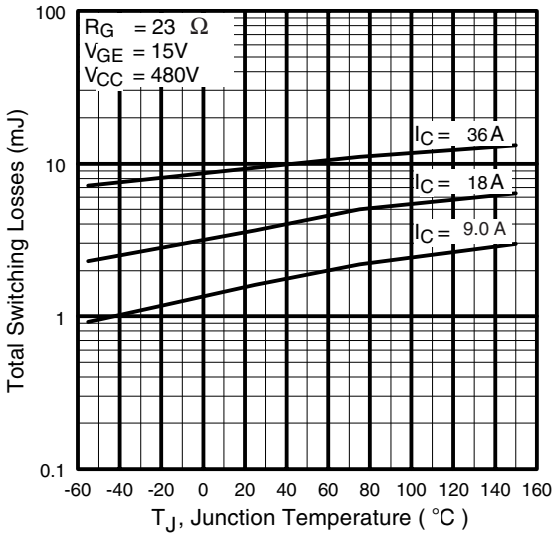


Fig. 10 - Typical Switching Losses vs. Junction Temperature

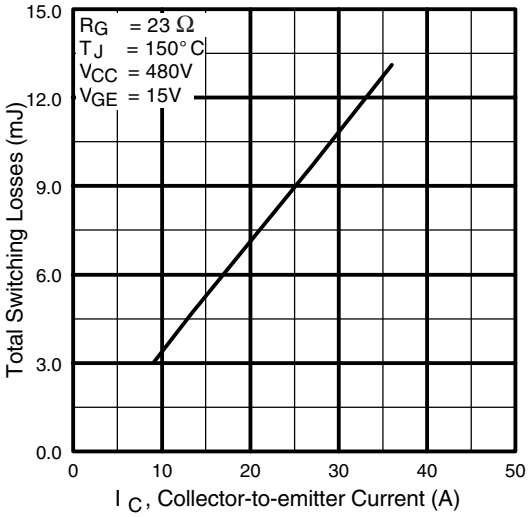


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

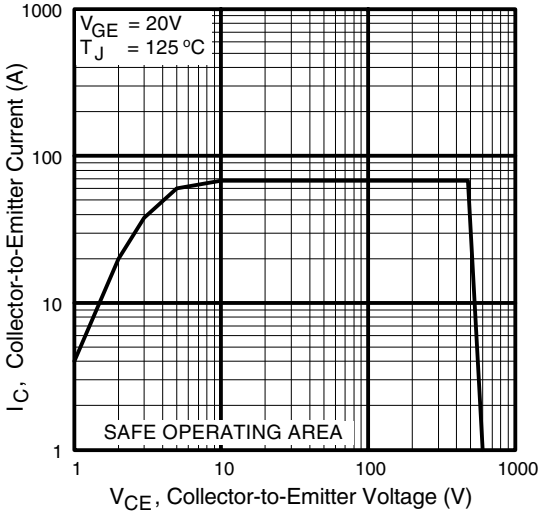


Fig. 12 - Turn-Off SOA

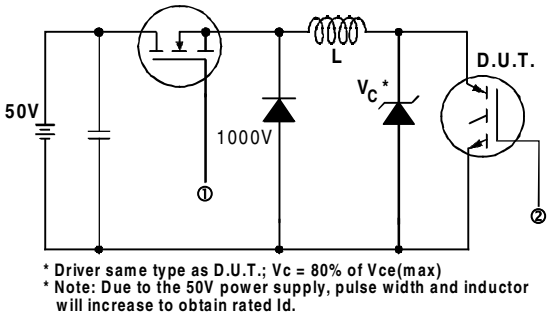


Fig. 13a - Clamped Inductive Load Test Circuit

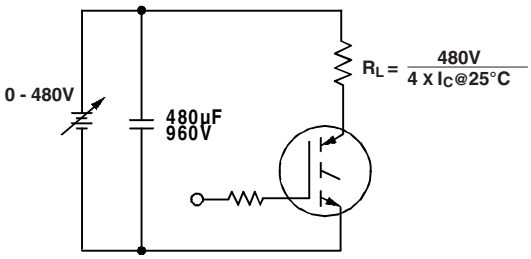


Fig. 13b - Pulsed Collector Current Test Circuit

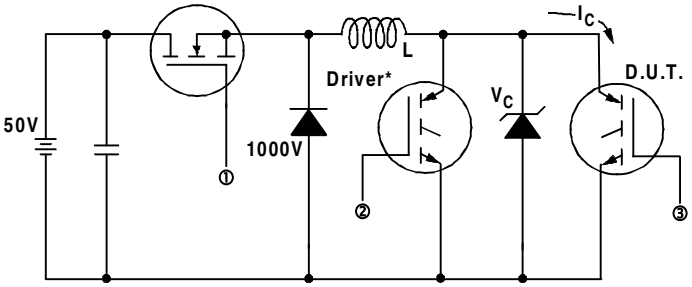


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

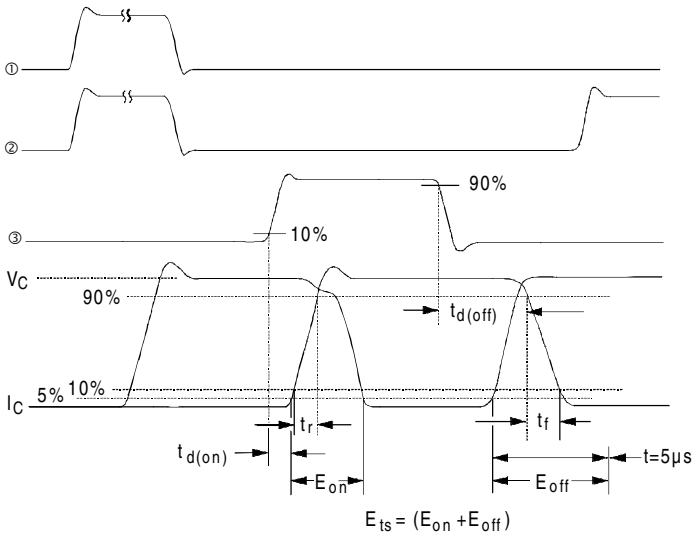
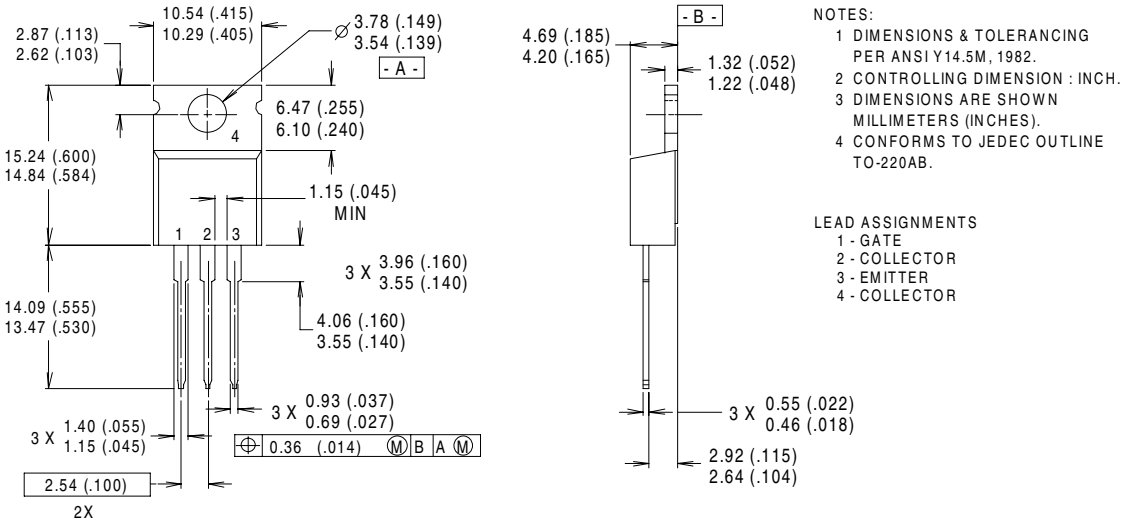


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-220AB



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-220AB.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD - 91586A

International
IOR Rectifier

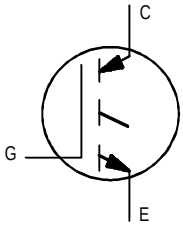
IRG4PC30S

INSULATED GATE BIPOLAR TRANSISTOR

Standard Speed IGBT

Features

- Standard: Optimized for minimum saturation voltage and low operating frequencies (< 1kHz)
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-247AC package



n-channel

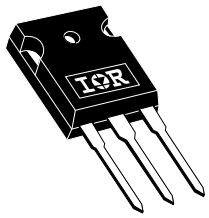
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$V_{CE(on)\ typ.}$ = 1.4V

@V_{GE} = 15V, I_C = 18A

Benefits

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- IGBTs optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	34	A
I_C @ T_C = 100°C	Continuous Collector Current	18	
I_{CM}	Pulsed Collector Current ①	68	
I_{LM}	Clamped Inductive Load Current ②	68	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	10	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

4/15/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.75	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.40	1.6	V	I_C = 18A V_{GE} = 15V
		—	1.84	—		I_C = 34A See Fig.2, 5
		—	1.45	—		I_C = 18A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	6.0	11	—	S	V_{CE} = 100V, I_C = 18A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	50	75	nC	I_C = 18A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	7.3	11		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	17	26		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	22	—	ns	
t_r	Rise Time	—	18	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	540	810		I_C = 18A, V_{CC} = 480V
t_f	Fall Time	—	390	590		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.26	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	3.45	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	3.71	5.6		
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	T_J = 150°C,
t_r	Rise Time	—	19	—		I_C = 18A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	790	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	760	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	6.55	—	mJ	See Fig. 11, 14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1100	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	72	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	13	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 23Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

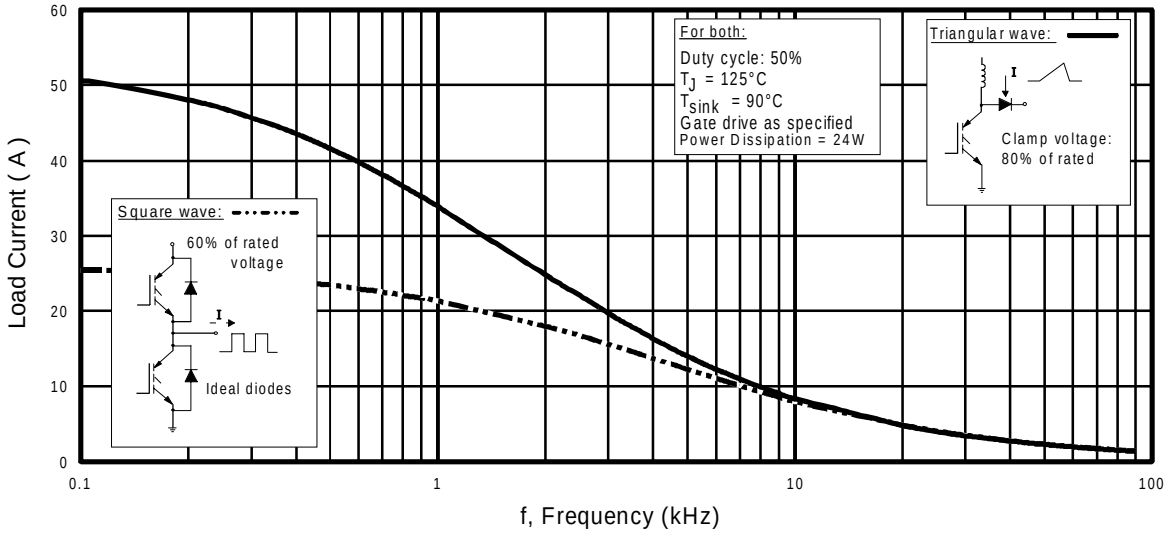


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

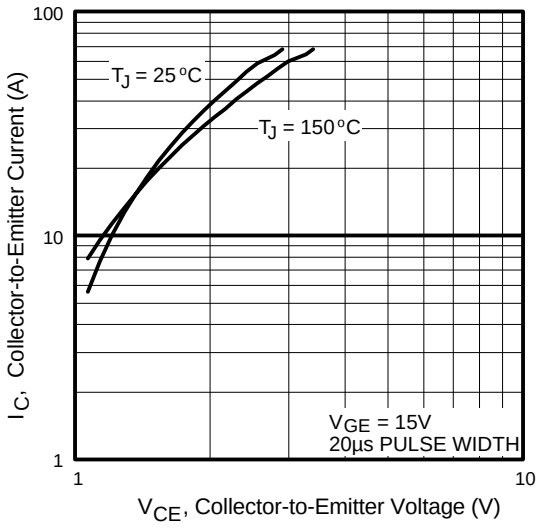


Fig. 2 - Typical Output Characteristics

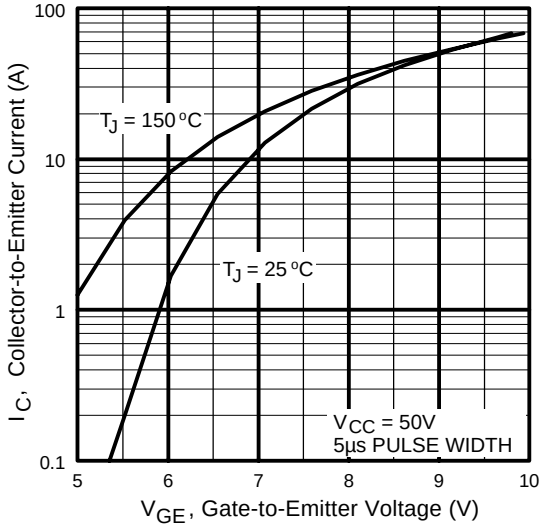


Fig. 3 - Typical Transfer Characteristics

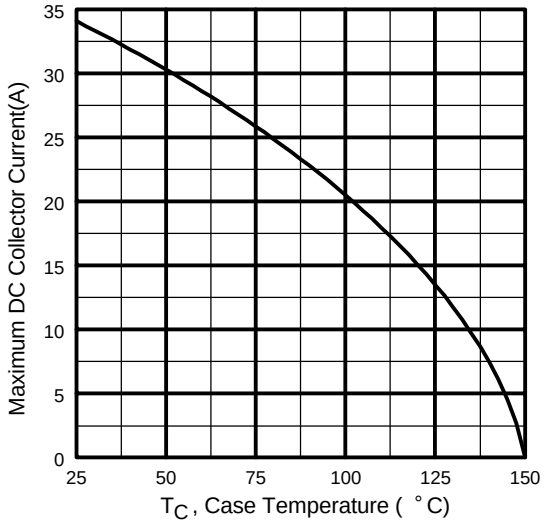


Fig. 4 - Maximum Collector Current vs. Case Temperature

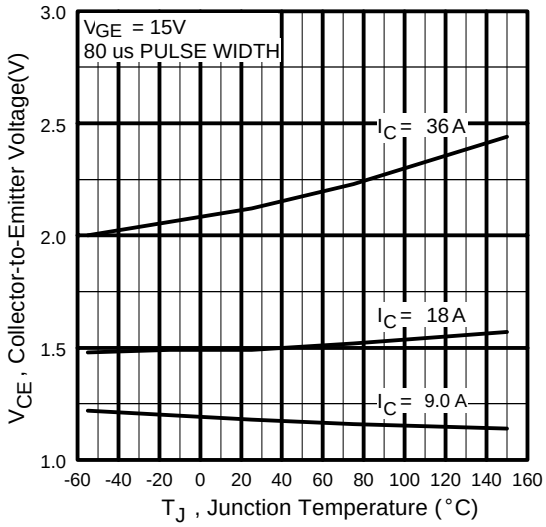


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

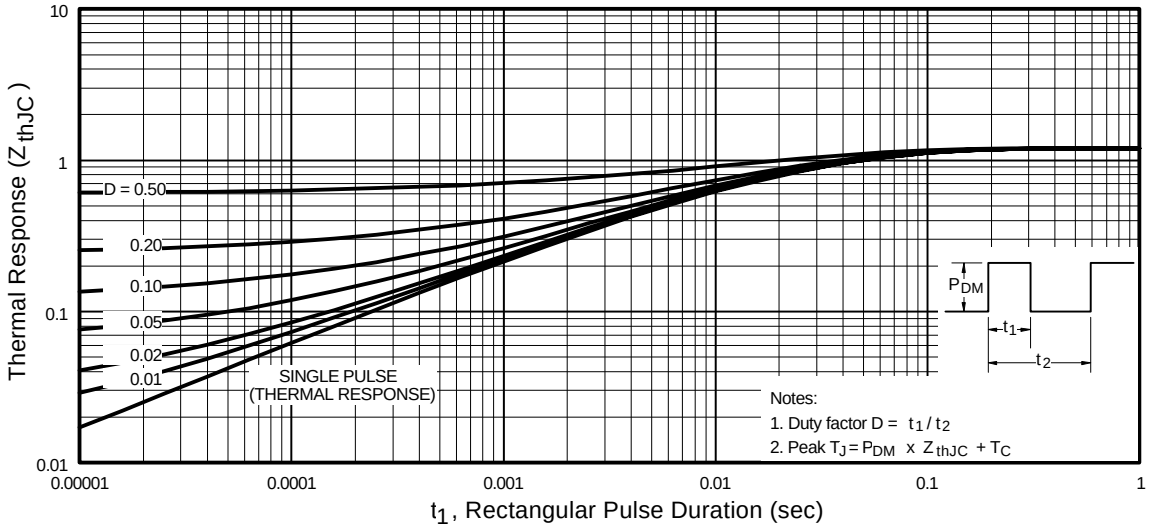


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

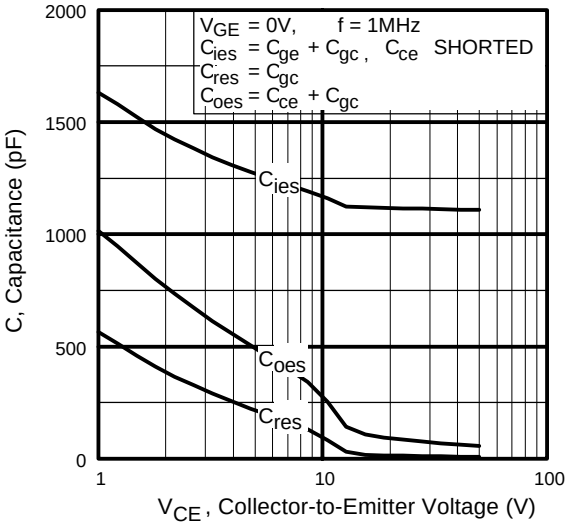


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

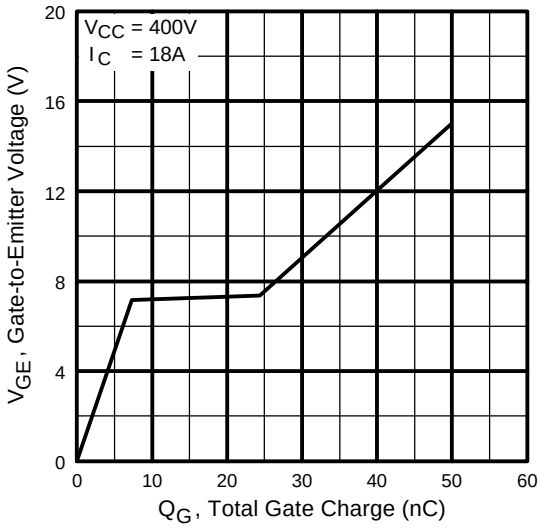


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

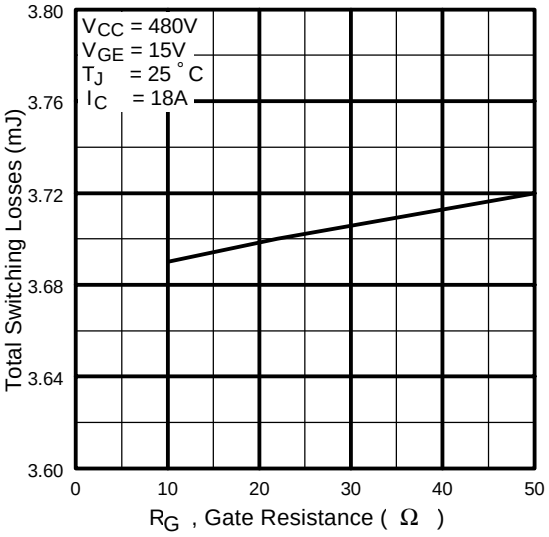


Fig. 9 - Typical Switching Losses vs. Gate Resistance

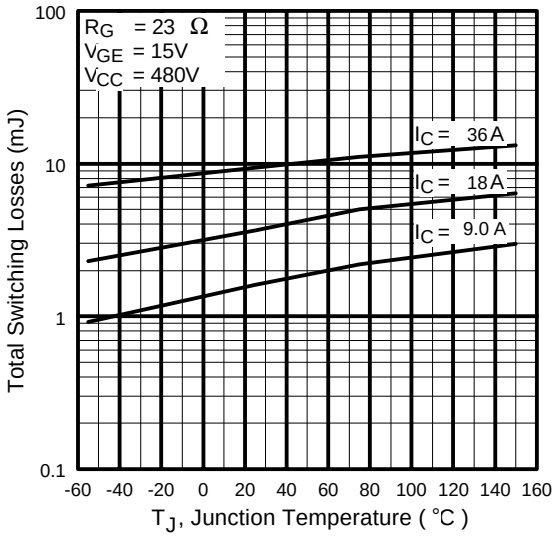


Fig. 10 - Typical Switching Losses vs. Junction Temperature

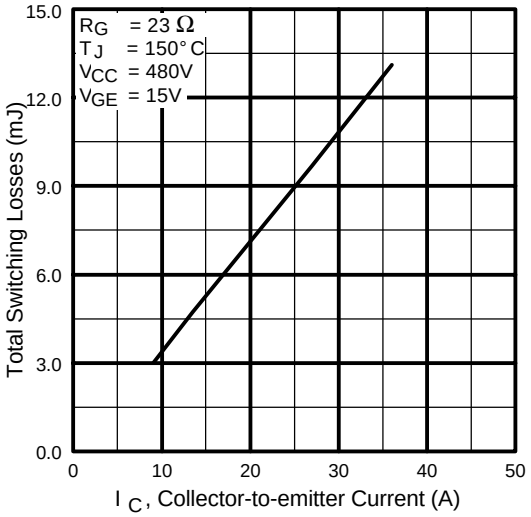


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

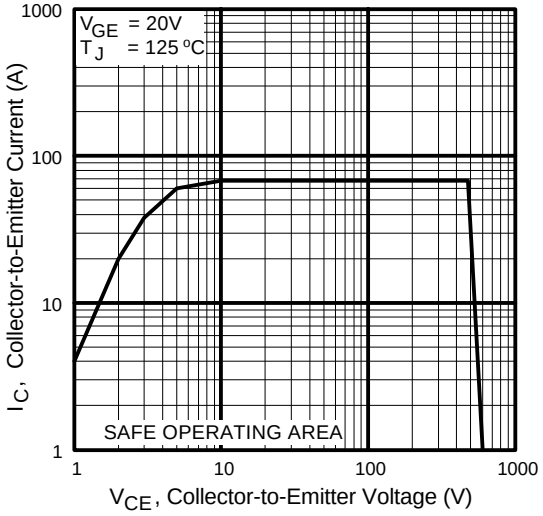


Fig. 12 - Turn-Off SOA

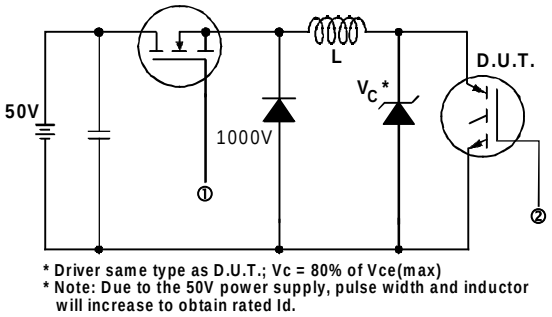


Fig. 13a - Clamped Inductive Load Test Circuit

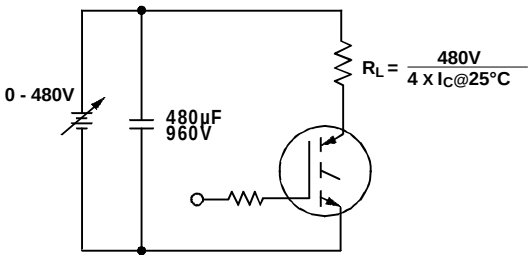


Fig. 13b - Pulsed Collector Current Test Circuit

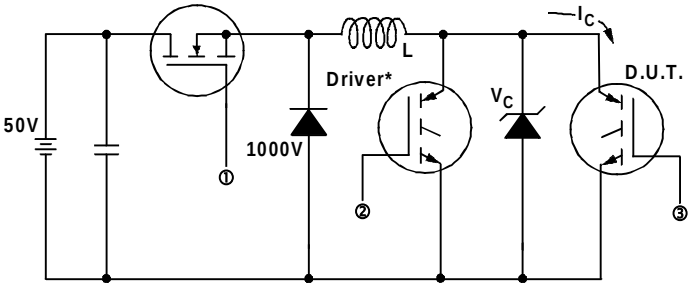


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

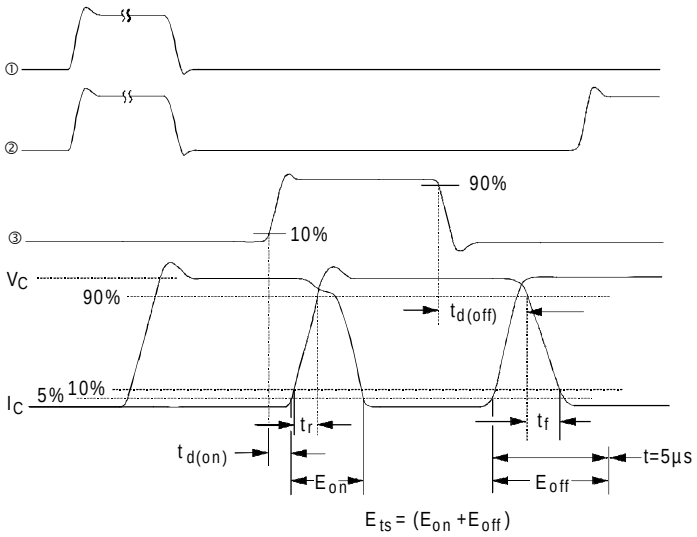
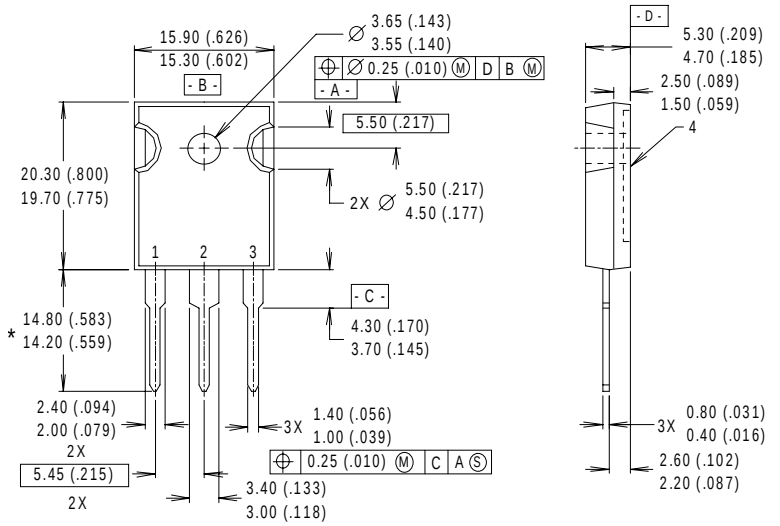


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD - 91456E

International
IOR Rectifier

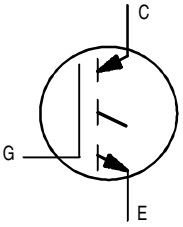
IRG4BC40U

INSULATED GATE BIPOLAR TRANSISTOR

UltraFast Speed IGBT

Features

- UltraFast: optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-220AB package



n-channel

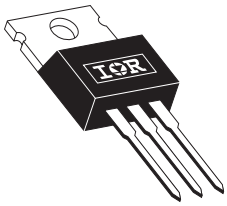
$V_{CES} = 600V$

$V_{CE(on)\ typ.} = 1.72V$

$@V_{GE} = 15V, I_C = 20A$

Benefits

- Generation 4 IGBTs offer highest efficiency available
- IGBTs optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	40	A
I_C @ T_C = 100°C	Continuous Collector Current	20	
I_{CM}	Pulsed Collector Current ①	160	
I_{LM}	Clamped Inductive Load Current ②	160	
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	15	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	------	------	0.77	°C/W
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	------	0.50	------	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	------	------	80	
Wt	Weight	------	2 (0.07)	------	g (oz)

4/17/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	----	----	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	----	----	V	V_{GE} = 0V, I_C = 1.0A See Fig. 2, 5
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	----	0.63	----	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	----	1.72	2.1	V	I_C = 20A V_{GE} = 15V
		----	2.15	----		I_C = 40A
		----	1.7	----		I_C = 20A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	----	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	----	-13	----	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	11	18	----	S	V_{CE} = 100V, I_C = 20A
I_{CES}	Zero Gate Voltage Collector Current	----	----	250	µA	V_{GE} = 0V, V_{CE} = 600V
		----	----	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		----	----	2500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	----	----	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	----	100	150	nC	I_C = 20A
Q_{ge}	Gate - Emitter Charge (turn-on)	----	16	25		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	----	40	60		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	----	34	----	ns	T_J = 25°C
t_r	Rise Time	----	19	----		I_C = 20A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	110	175		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	----	120	180		Energy losses include "tail"
E_{on}	Turn-On Switching Loss	----	0.32	----	mJ	See Fig. 10, 11, 13, 14
E_{off}	Turn-Off Switching Loss	----	0.35	----		
E_{ts}	Total Switching Loss	----	0.67	1.0		
$t_{d(on)}$	Turn-On Delay Time	----	30	----	ns	T_J = 150°C,
t_r	Rise Time	----	19	----		I_C = 20A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	220	----		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	----	160	----		Energy losses include "tail"
E_{ts}	Total Switching Loss	----	1.4	----	mJ	See Fig. 13, 14
L_E	Internal Emitter Inductance	----	7.5	----	nH	Measured 5mm from package
C_{ies}	Input Capacitance	----	2100	----	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	----	140	----		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	----	34	----		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 10Ω, (see fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

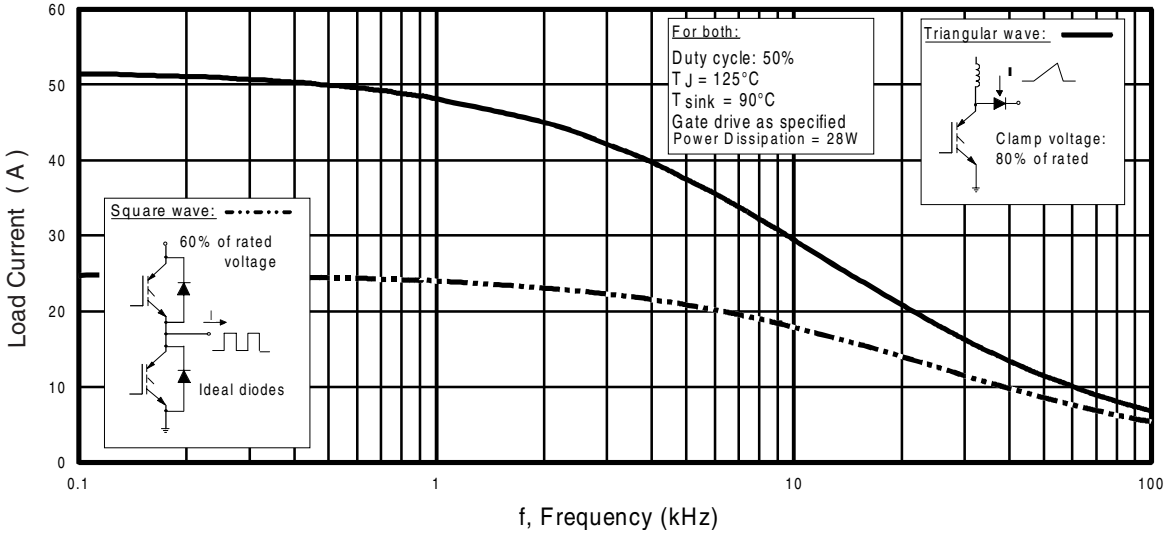


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

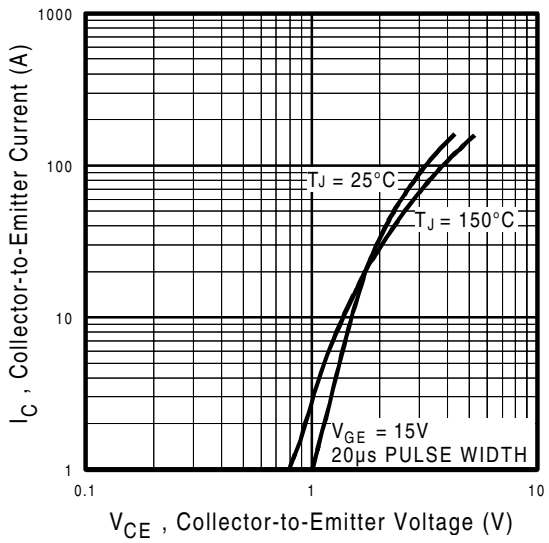


Fig. 2 - Typical Output Characteristics
$T_C = 25°C$

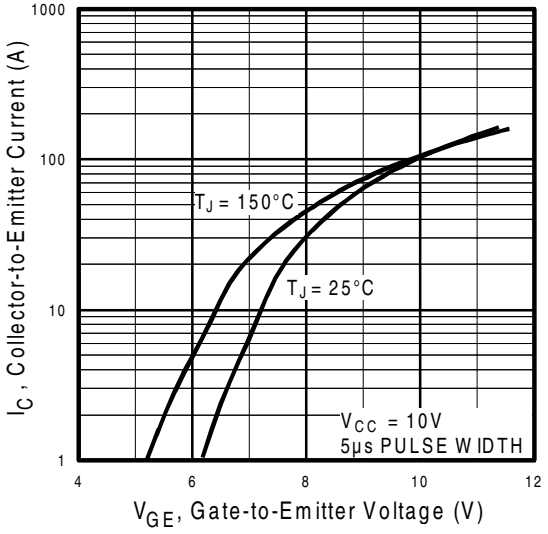


Fig. 3 - Typical Transfer Characteristics

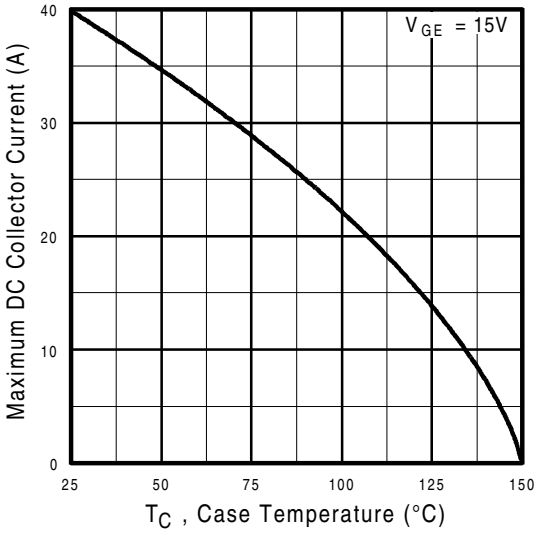


Fig. 4 - Maximum Collector Current vs. Case Temperature

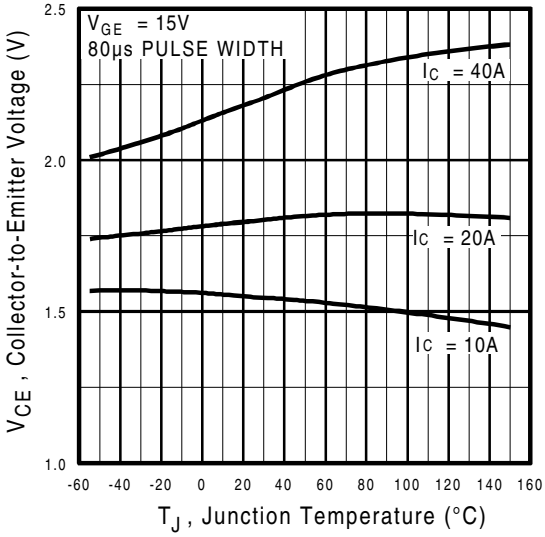


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

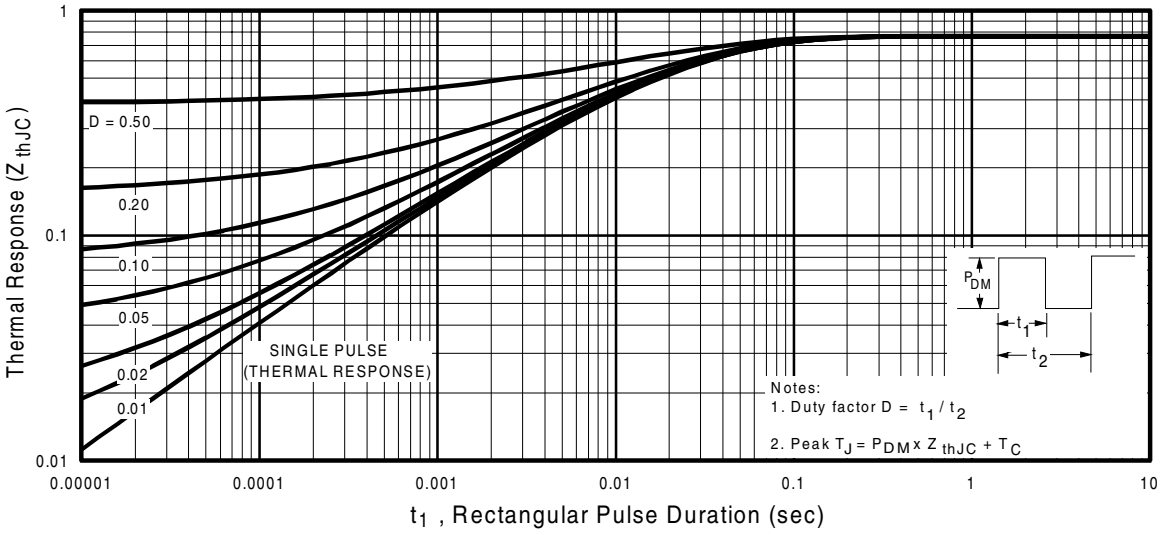


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

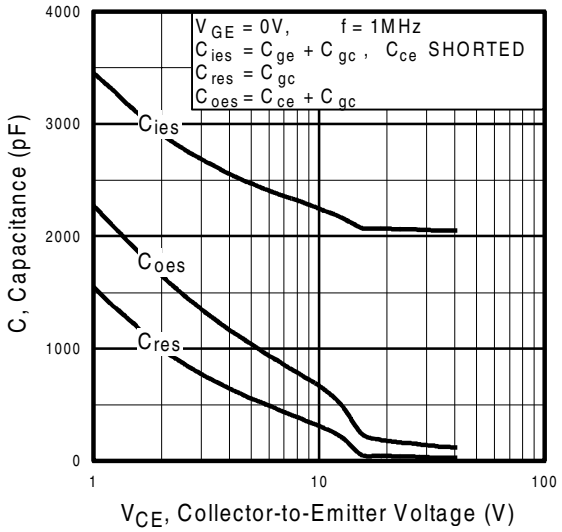


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

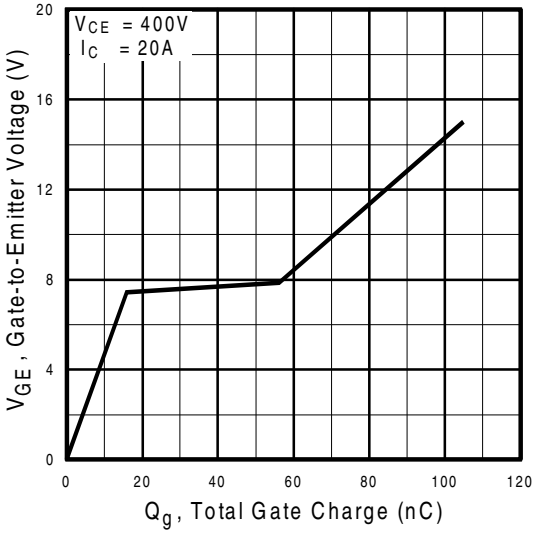


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

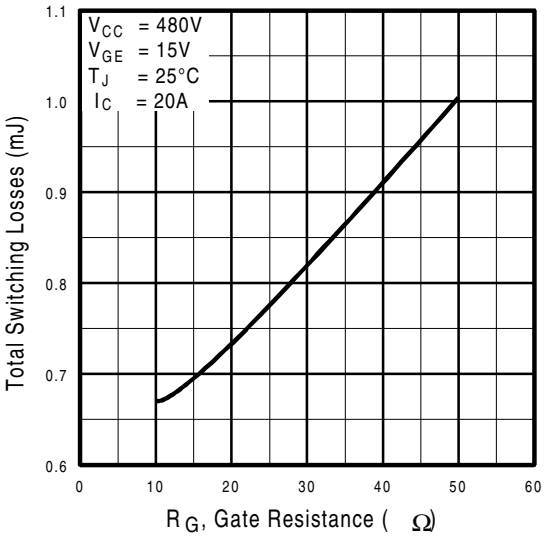


Fig. 9 - Typical Switching Losses vs. Gate Resistance

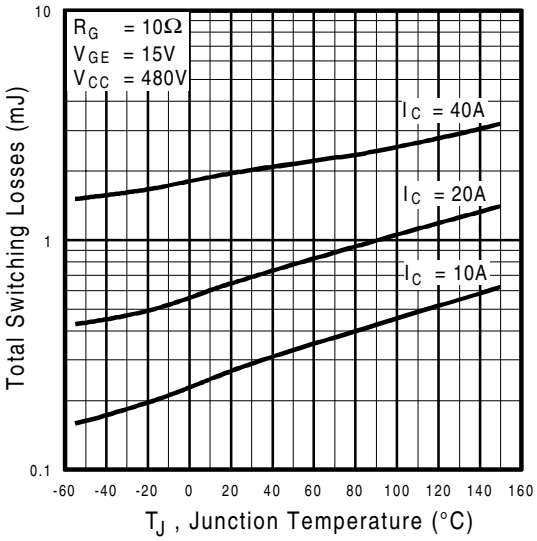


Fig. 10 - Typical Switching Losses vs. Junction Temperature

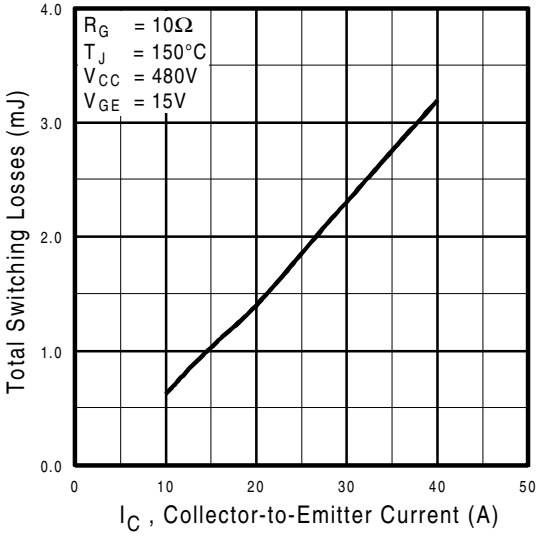


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

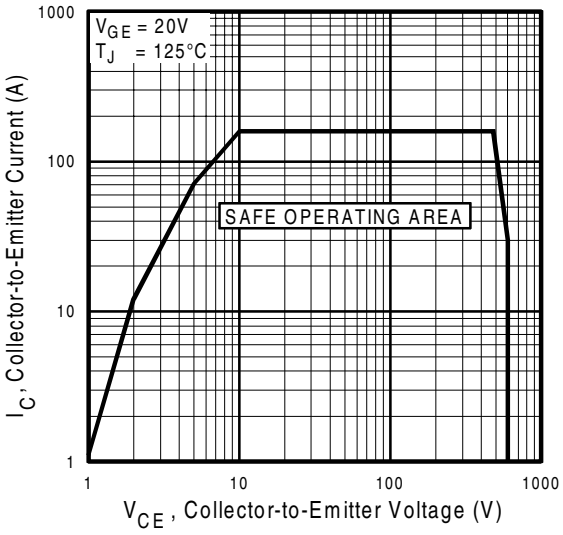


Fig. 12 - Turn-Off SOA

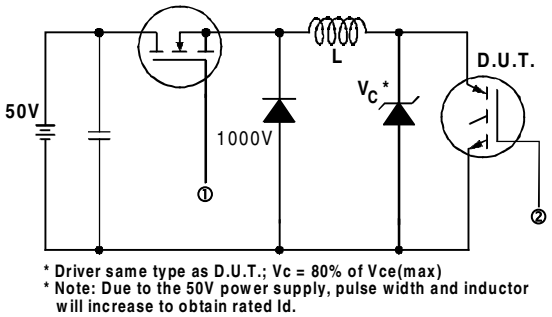


Fig. 13a - Clamped Inductive Load Test Circuit

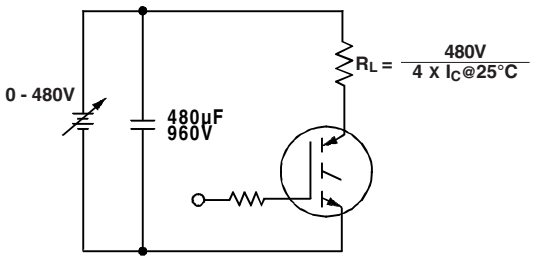


Fig. 13b - Pulsed Collector Current Test Circuit

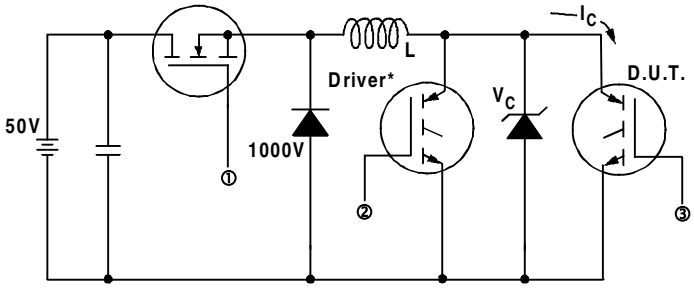


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

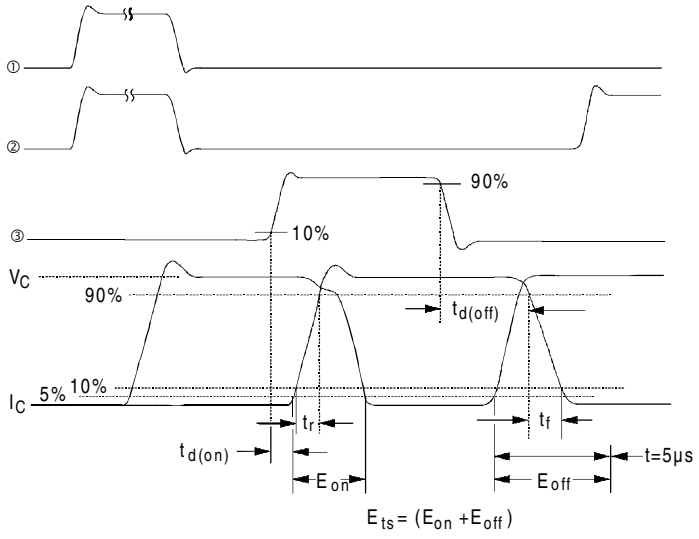
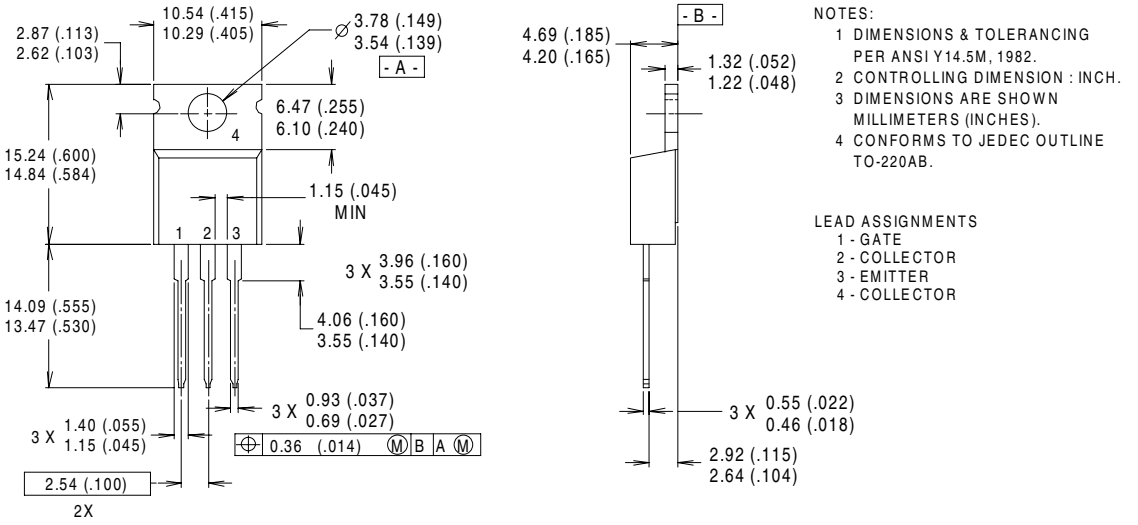


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD 91466E

International
IOR Rectifier

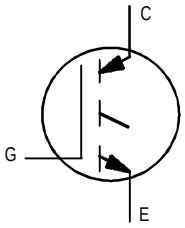
IRG4PC40U

INSULATED GATE BIPOLAR TRANSISTOR

UltraFast Speed IGBT

Features

- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-247AC package



n-channel

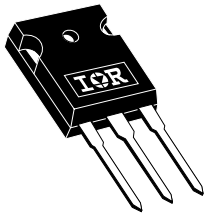
$V_{CES} = 600V$

$V_{CE(on)\ typ.} = 1.72V$

$@V_{GE} = 15V, I_C = 20A$

Benefits

- Generation 4 IGBT's offer highest efficiency available
- IGBT's optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	40	A
I_C @ T_C = 100°C	Continuous Collector Current	20	
I_{CM}	Pulsed Collector Current ①	160	
I_{LM}	Clamped Inductive Load Current ②	160	
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	15	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	℃
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	------	------	0.77	°C/W
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	------	0.24	------	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	------	------	40	
Wt	Weight	------	6 (0.21)	------	g (oz)

12/30/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	----	----	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	----	----	V	V_{GE} = 0V, I_C = 1.0A See Fig. 2, 5
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	----	0.63	----	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	----	1.72	2.1	V	I_C = 20A V_{GE} = 15V
		----	2.15	----		I_C = 40A
		----	1.7	----		I_C = 20A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	----	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	----	-13	----	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	11	18	----	S	V_{CE} = 100V, I_C = 20A
I_{CES}	Zero Gate Voltage Collector Current	----	----	250	µA	V_{GE} = 0V, V_{CE} = 600V
		----	----	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		----	----	2500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	----	----	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	----	100	150	nC	I_C = 20A
Q_{ge}	Gate - Emitter Charge (turn-on)	----	16	25		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	----	40	60		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	----	34	----	ns	T_J = 25°C
t_r	Rise Time	----	19	----		I_C = 20A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	110	175		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	----	120	180		Energy losses include "tail"
E_{on}	Turn-On Switching Loss	----	0.32	----	mJ	See Fig. 10, 11, 13, 14
E_{off}	Turn-Off Switching Loss	----	0.35	----		
E_{ts}	Total Switching Loss	----	0.67	1.0		
$t_{d(on)}$	Turn-On Delay Time	----	30	----	ns	T_J = 150°C,
t_r	Rise Time	----	19	----		I_C = 20A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	220	----		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	----	160	----		Energy losses include "tail"
E_{ts}	Total Switching Loss	----	1.4	----	mJ	See Fig. 13, 14
L_E	Internal Emitter Inductance	----	13	----	nH	Measured 5mm from package
C_{ies}	Input Capacitance	----	2100	----	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	----	140	----		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	----	34	----		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 10Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

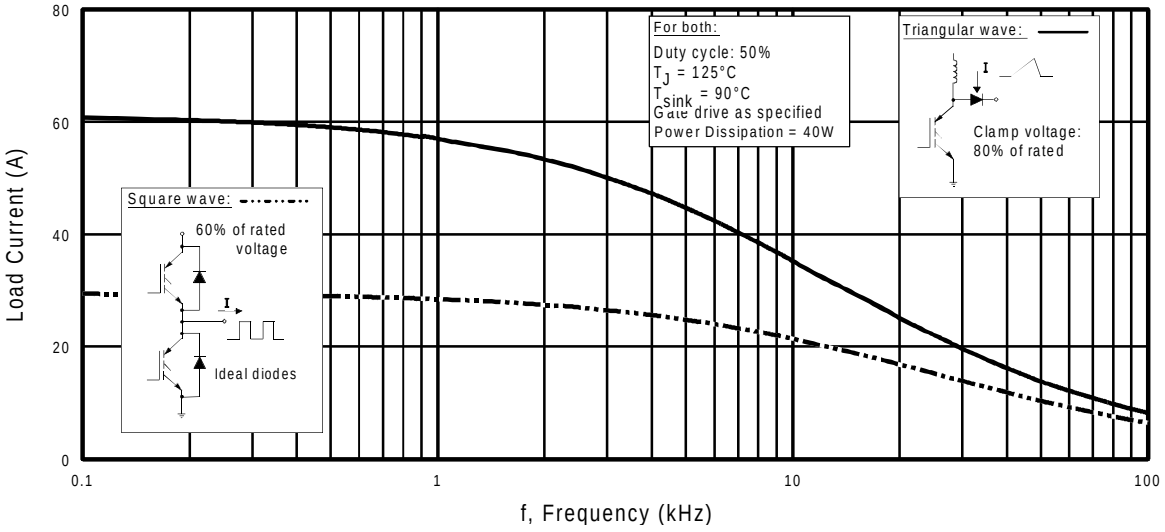


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

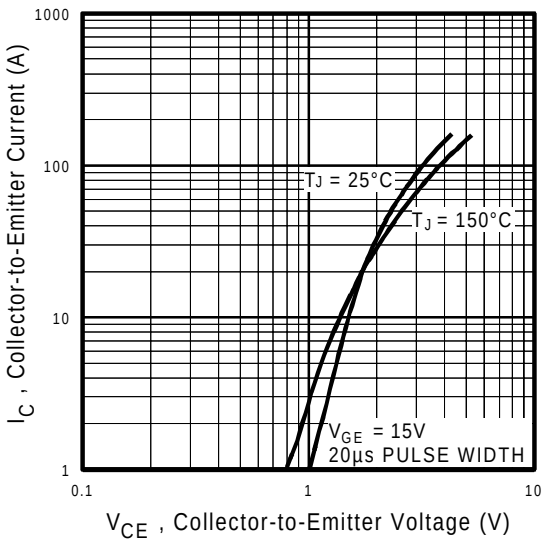


Fig. 2 - Typical Output Characteristics

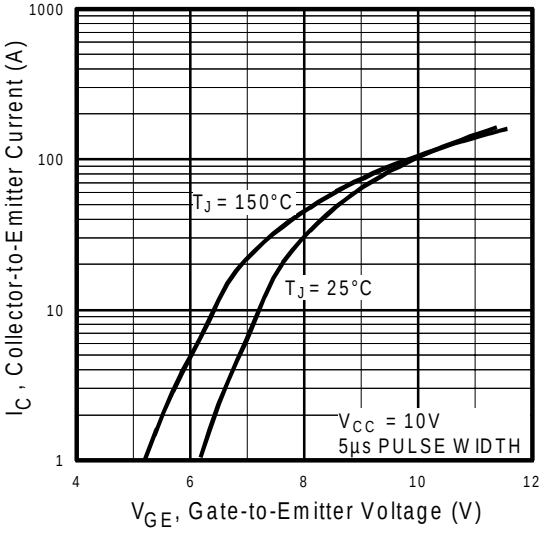


Fig. 3 - Typical Transfer Characteristics

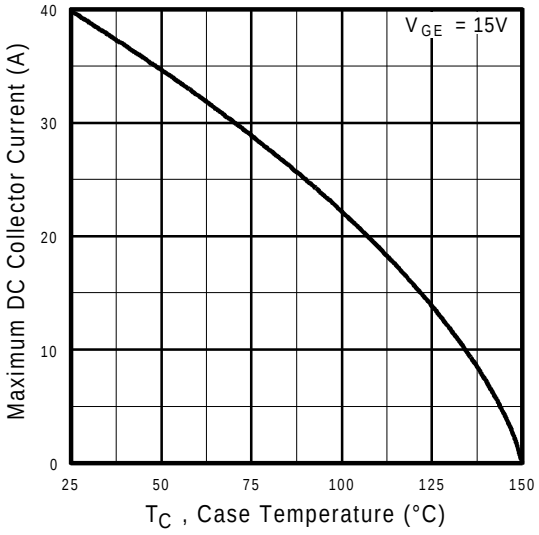


Fig. 4 - Maximum Collector Current vs. Case Temperature

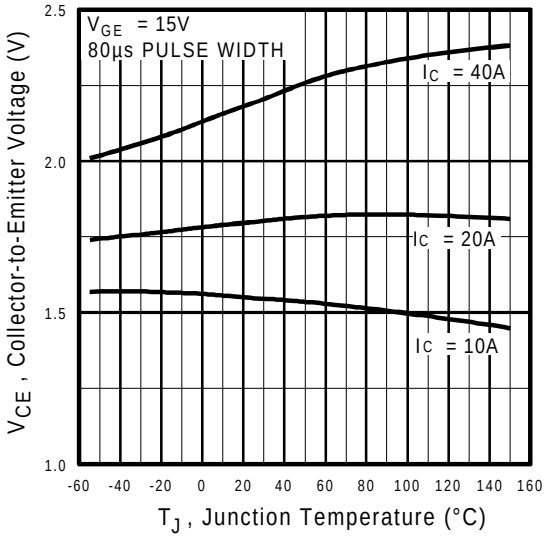


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

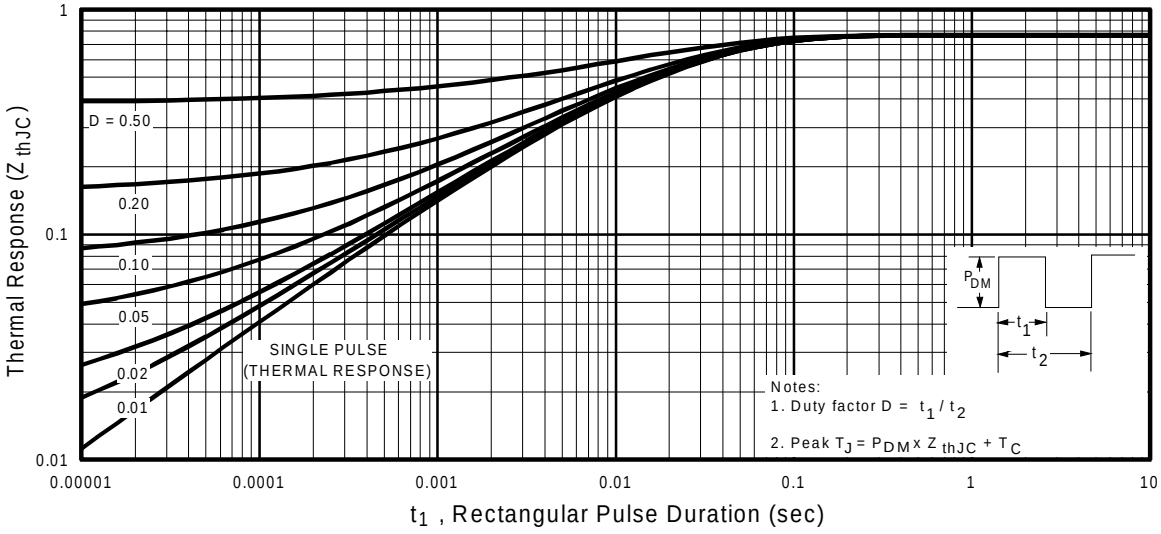


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

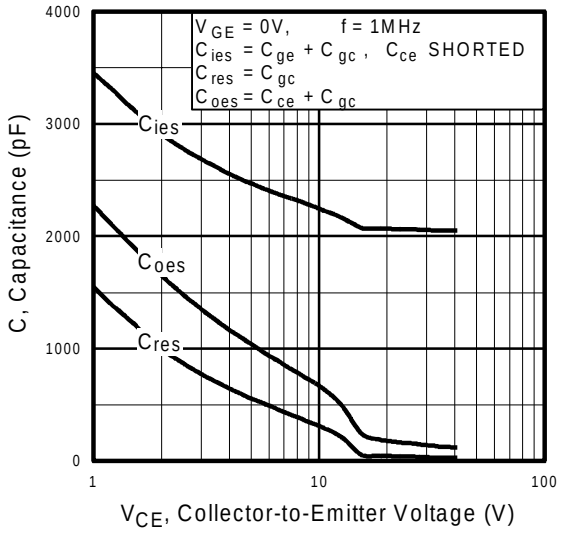


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

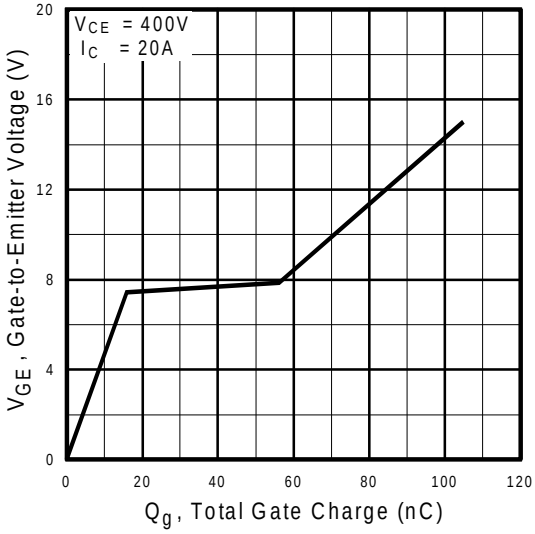


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

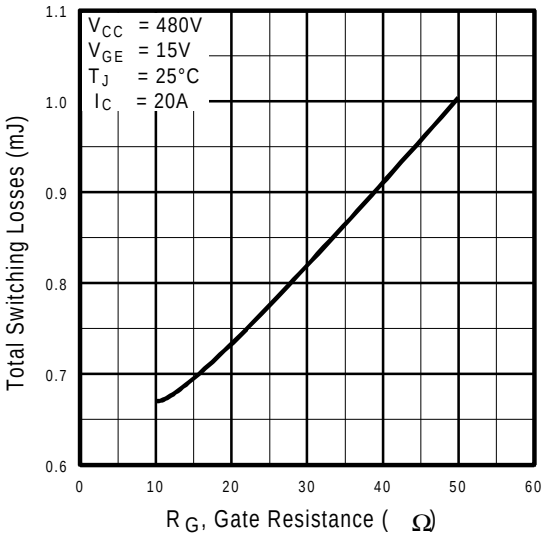


Fig. 9 - Typical Switching Losses vs. Gate Resistance

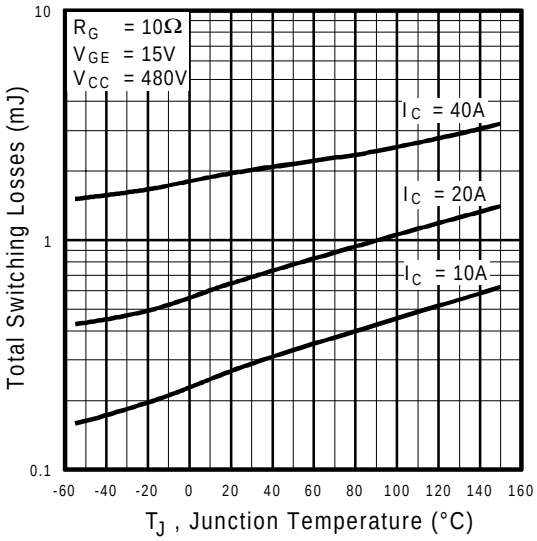


Fig. 10 - Typical Switching Losses vs. Junction Temperature

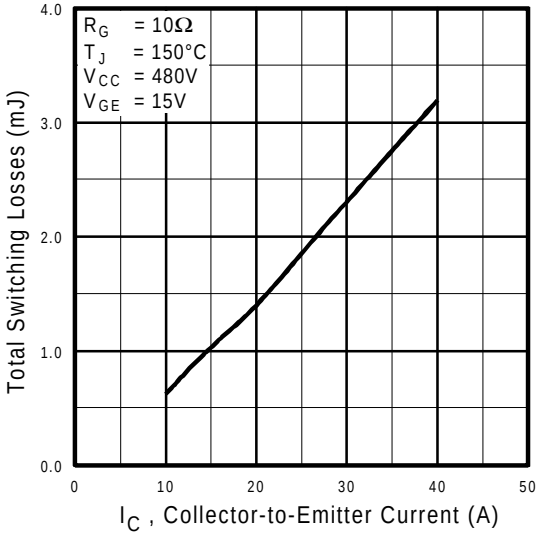


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

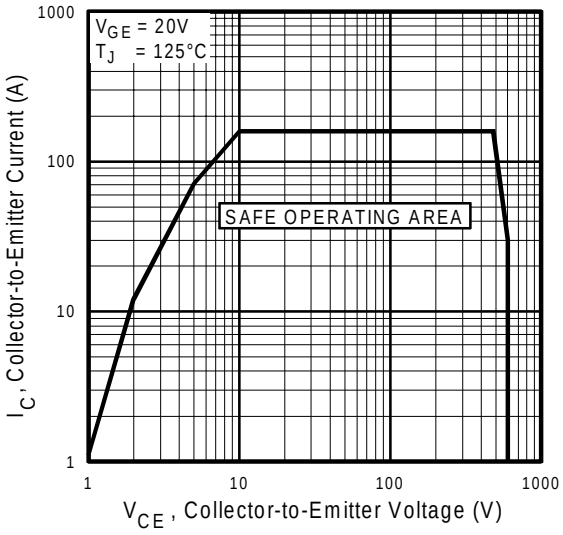


Fig. 12 - Turn-Off SOA

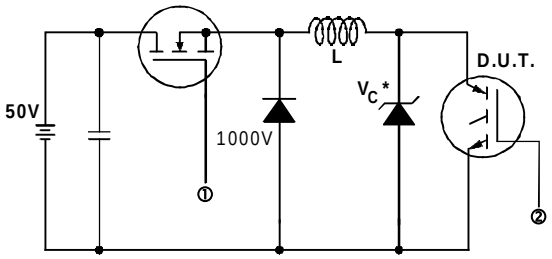


Fig. 13a - Clamped Inductive Load Test Circuit

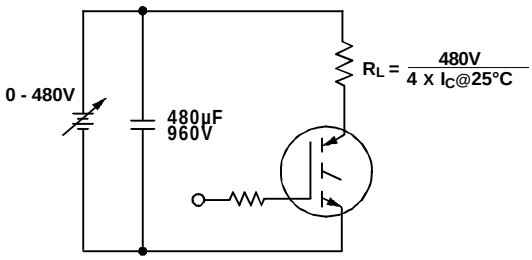


Fig. 13b - Pulsed Collector Current Test Circuit

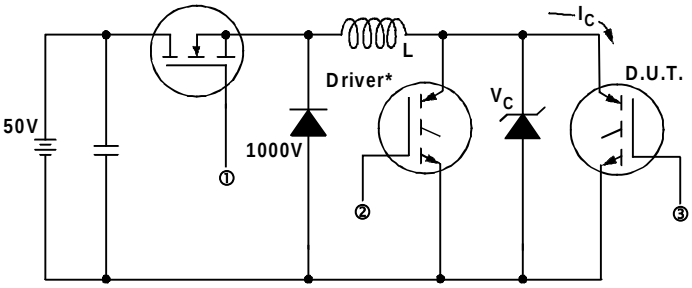


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

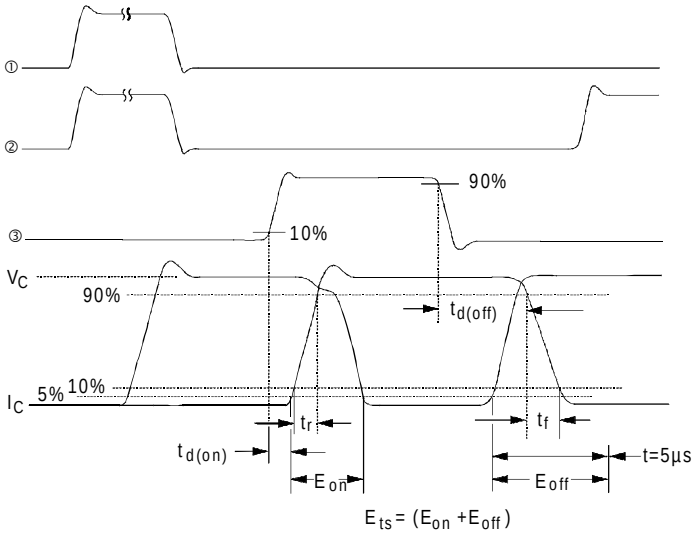
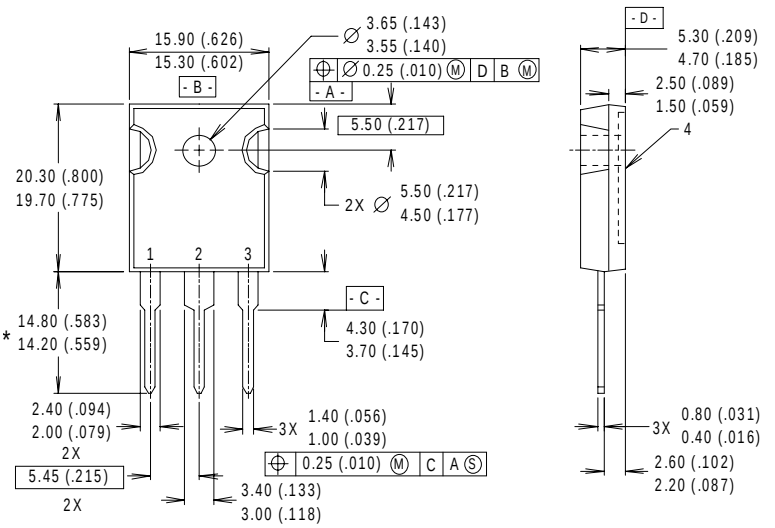


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
Data and specifications subject to change without notice. 12/00

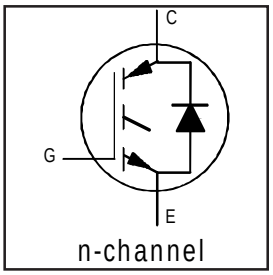
PD 9.1467D

International
IOR Rectifier

IRG4PC40UD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

UltraFast CoPack IGBT



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.72V

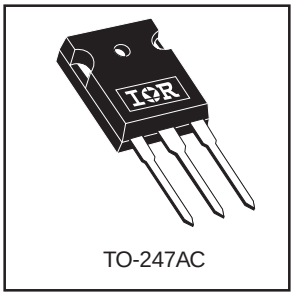
@V_{GE} = 15V, I_C = 20A

Features

- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-247AC package

Benefits

- Generation -4 IGBT's offer highest efficiencies available
- IGBT's optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBT's . Minimized recovery characteristics require less/no snubbing
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	40	A
I_C @ T_C = 100°C	Continuous Collector Current	20	
I_{CM}	Pulsed Collector Current ①	160	
I_{LM}	Clamped Inductive Load Current ②	160	
I_F @ T_C = 100°C	Diode Continuous Forward Current	15	
I_{FM}	Diode Maximum Forward Current	160	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	------	------	0.77	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	------	------	1.7	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	------	0.24	------	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	-----	-----	40	
Wt	Weight	------	6 (0.21)	------	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	----	----	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	----	0.63	----	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	----	1.72	2.1	V	I_C = 20A V_{GE} = 15V
		----	2.15	----		I_C = 40A See Fig. 2, 5
		----	1.7	----		I_C = 20A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	----	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	----	-13	----	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	11	18	----	S	V_{CE} = 100V, I_C = 20A
I_{CES}	Zero Gate Voltage Collector Current	----	----	250	µA	V_{GE} = 0V, V_{CE} = 600V
		----	----	3500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	----	1.3	1.7	V	I_C = 15A See Fig. 13
		----	1.2	1.6		I_C = 15A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	----	----	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	----	100	150	nC	I_C = 20A
Qge	Gate - Emitter Charge (turn-on)	----	16	25		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	----	40	60		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	----	54	----	ns	T_J = 25°C
t_r	Rise Time	----	57	----		I_C = 20A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	110	165		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	----	80	120		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	----	0.71	----	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	----	0.35	----		See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	----	1.10	1.5		
$t_{d(on)}$	Turn-On Delay Time	----	40	----	ns	T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	----	52	----		I_C = 20A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	200	----		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	----	130	----		Energy losses include "tail" and
E_{ts}	Total Switching Loss	----	1.6	----	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	----	13	----	nH	Measured 5mm from package
C_{ies}	Input Capacitance	----	2100	----	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	----	140	----		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	----	34	----		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	----	42	60	ns	T_J = 25°C See Fig.
		----	74	120		T_J = 125°C 14 I_F = 15A
I_{rr}	Diode Peak Reverse Recovery Current	----	4.0	6.0	A	T_J = 25°C See Fig.
		----	6.5	10		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	----	80	180	nC	T_J = 25°C See Fig.
		----	220	600		T_J = 125°C 16 di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	----	190	----	A/µs	T_J = 25°C
	During t_b	----	160	----		T_J = 125°C

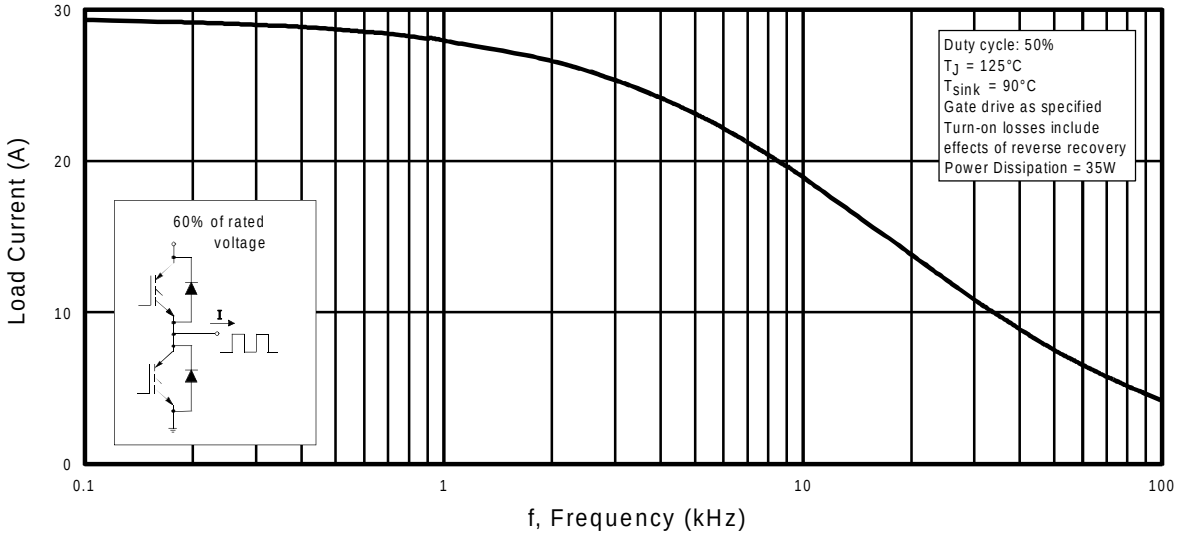


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

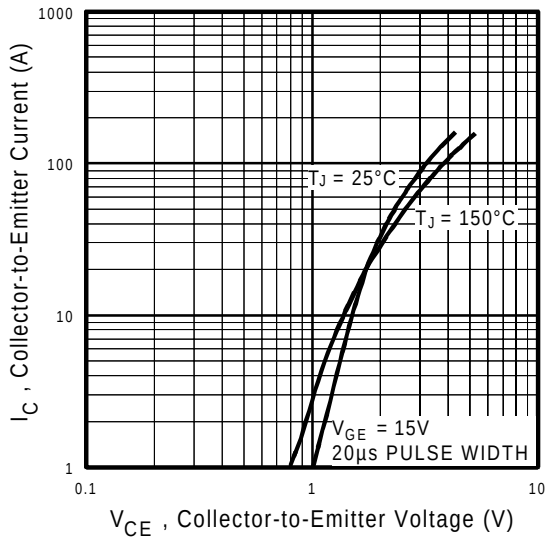


Fig. 2 - Typical Output Characteristics

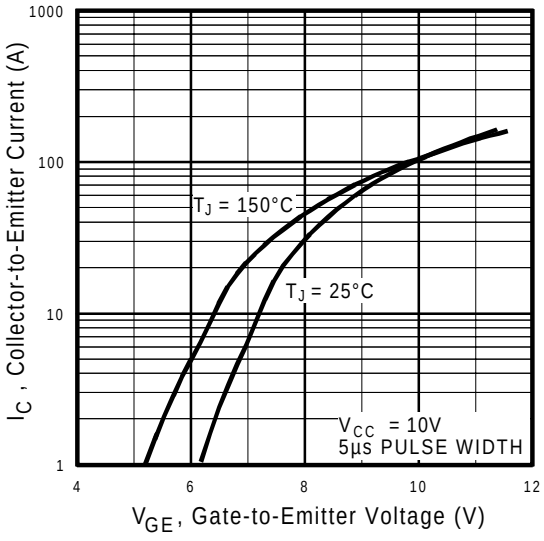


Fig. 3 - Typical Transfer Characteristics

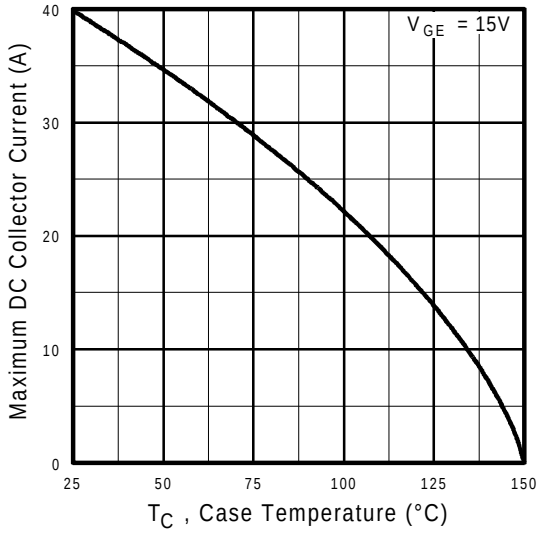


Fig. 4 - Maximum Collector Current vs. Case Temperature

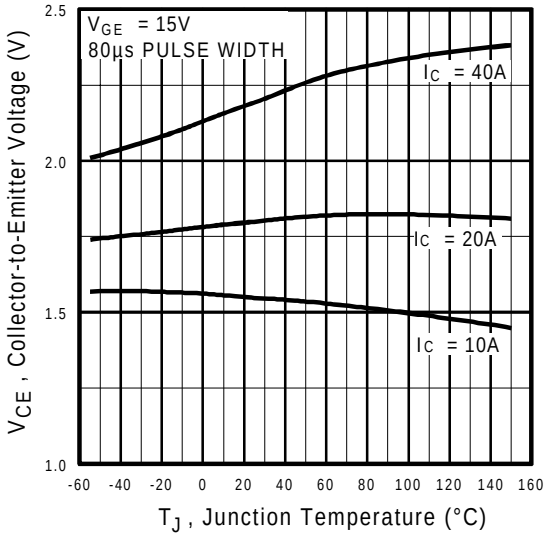


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

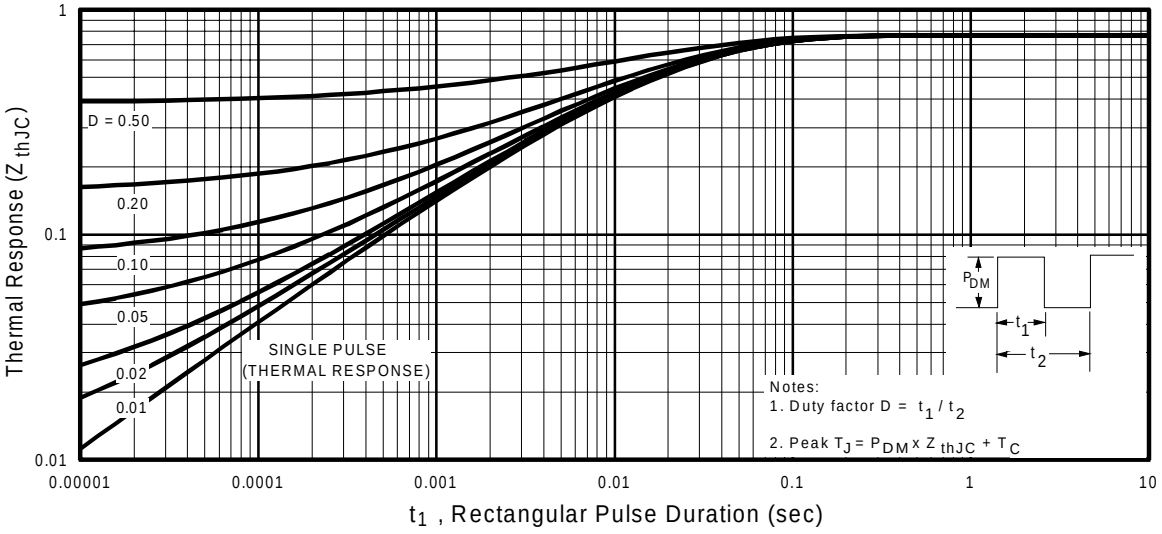


Fig. 6 - Maximum IGBT Effective Transient Thermal Impedance, Junction-to-Case

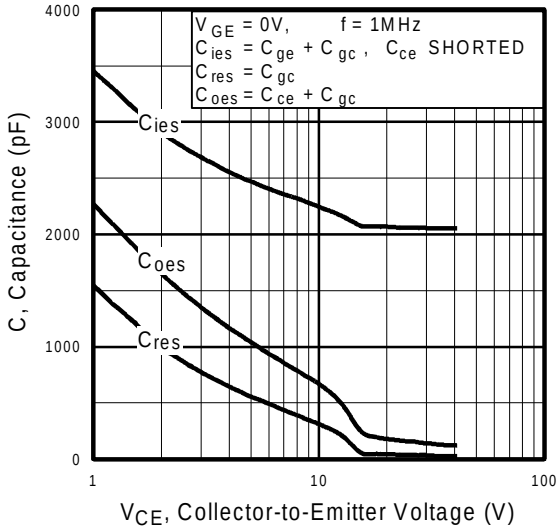


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

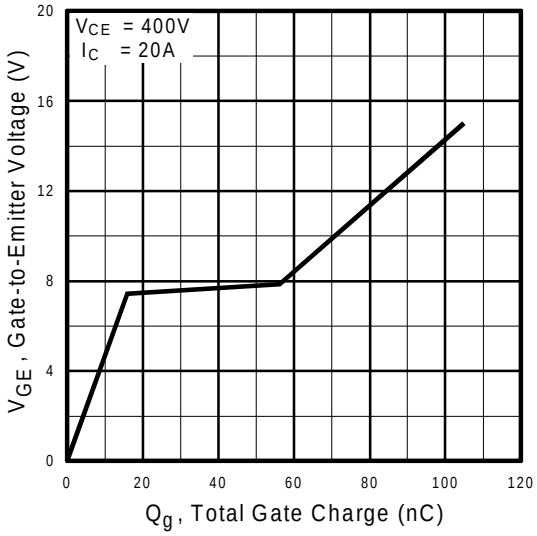


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

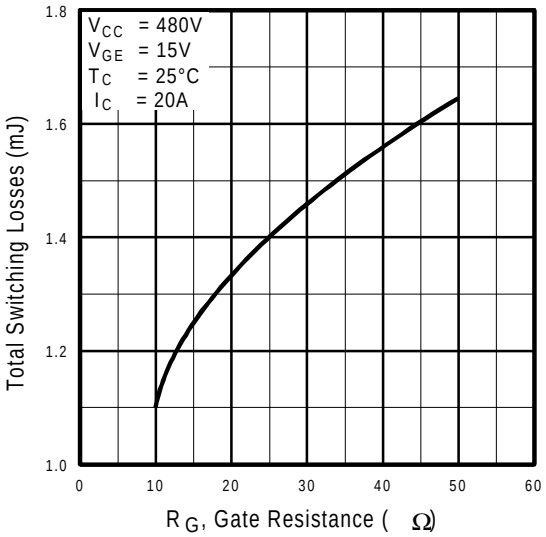


Fig. 9 - Typical Switching Losses vs. Gate Resistance

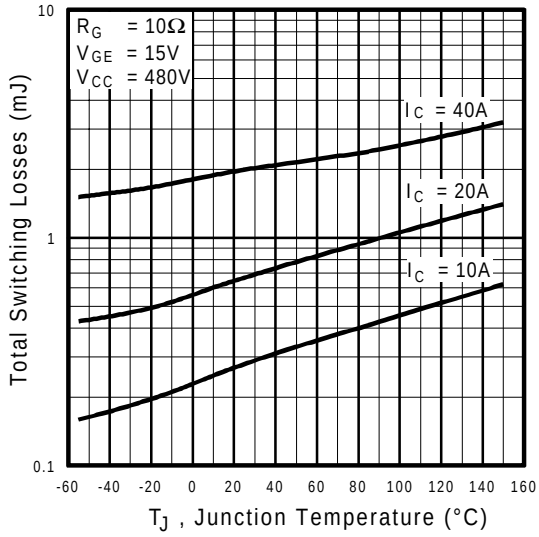


Fig. 10 - Typical Switching Losses vs. Junction Temperature

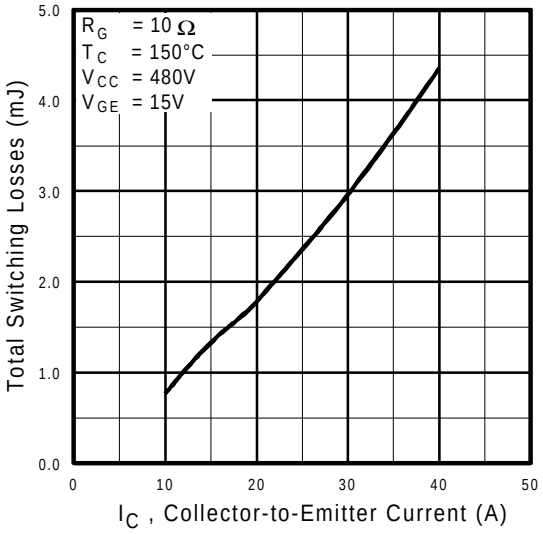


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

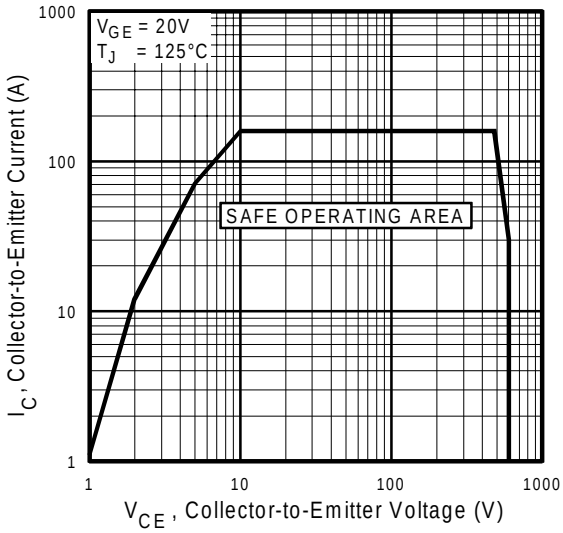


Fig. 12 - Turn-Off SOA

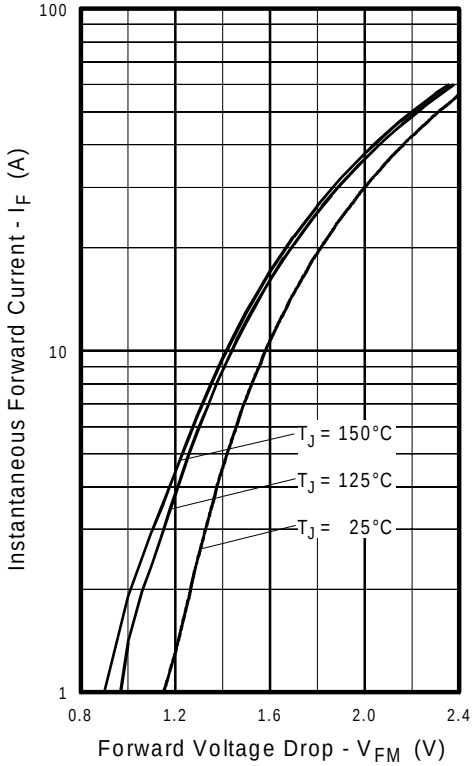


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

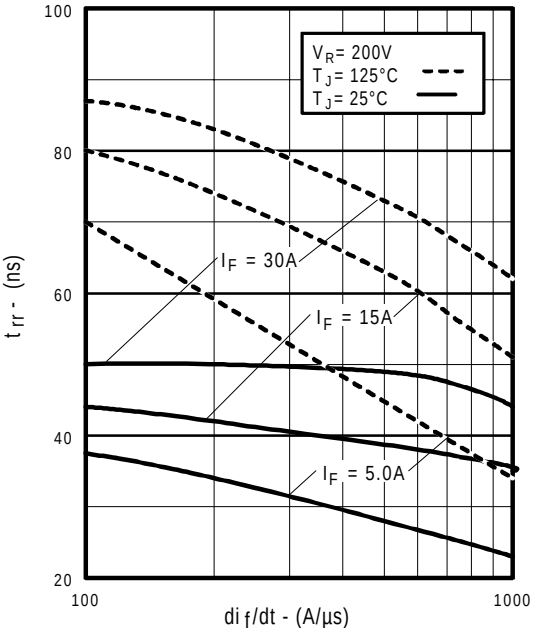


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

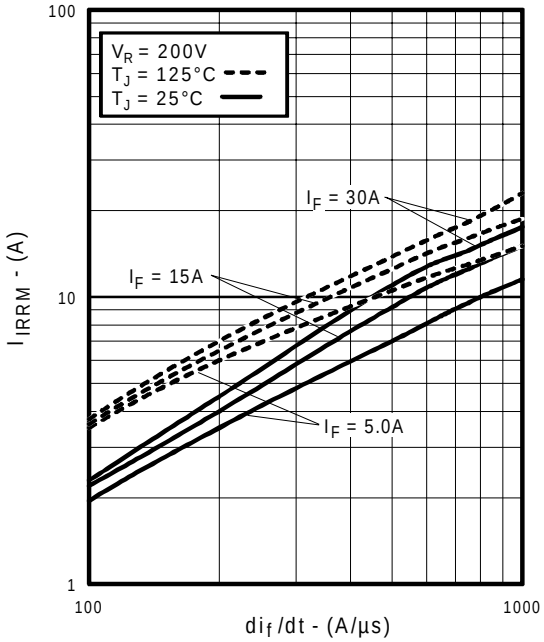


Fig. 15 - Typical Recovery Current vs. di_f/dt

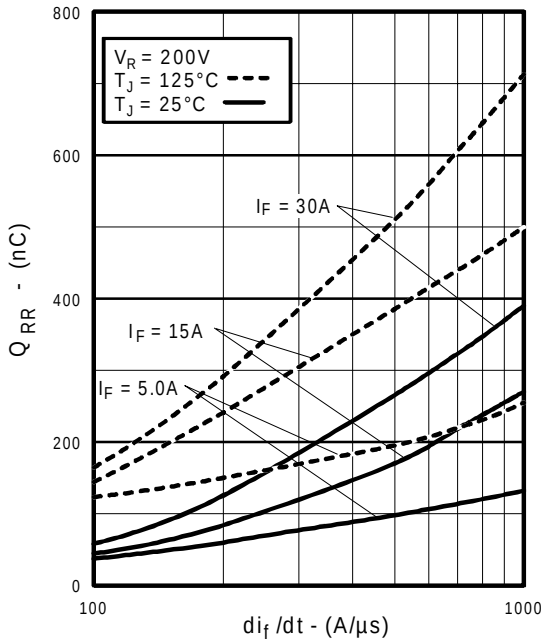


Fig. 16 - Typical Stored Charge vs. di_f/dt

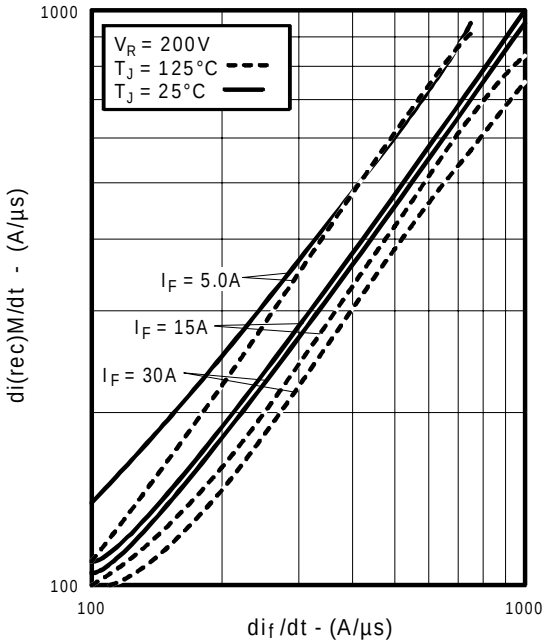


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

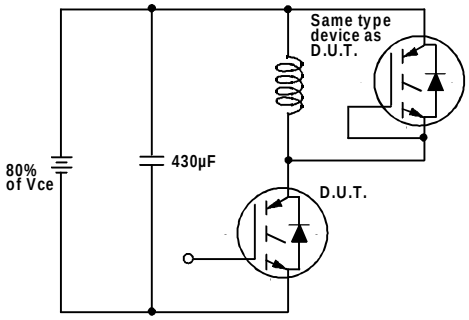


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

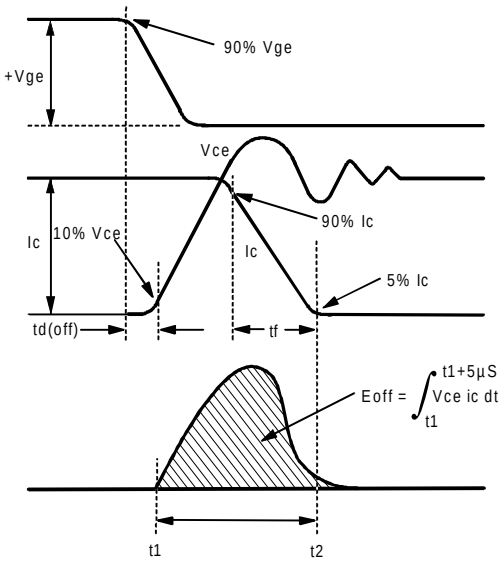


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

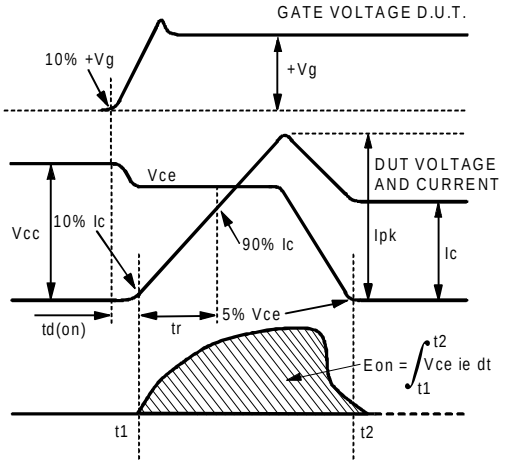


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

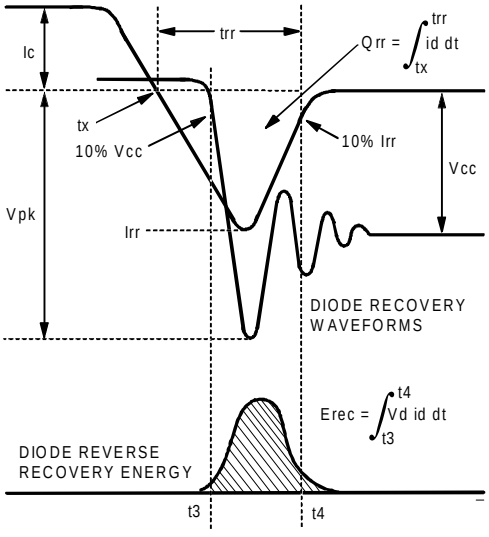


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

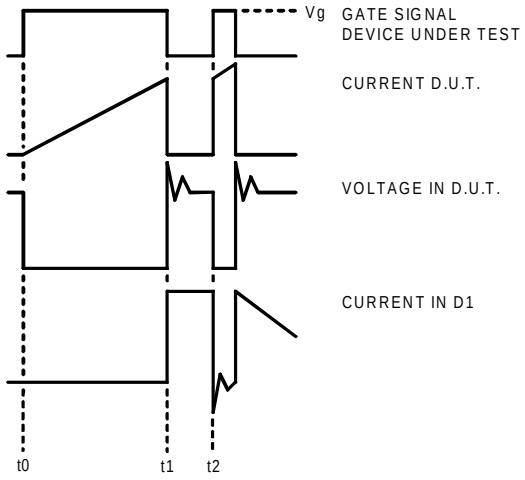


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

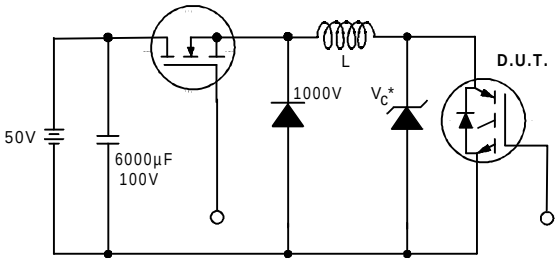


Figure 19. Clamped Inductive Load Test Circuit

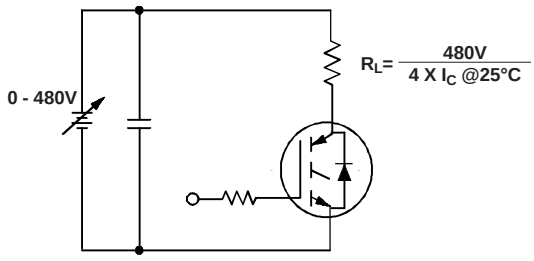


Figure 20. Pulsed Collector Current Test Circuit

Notes:

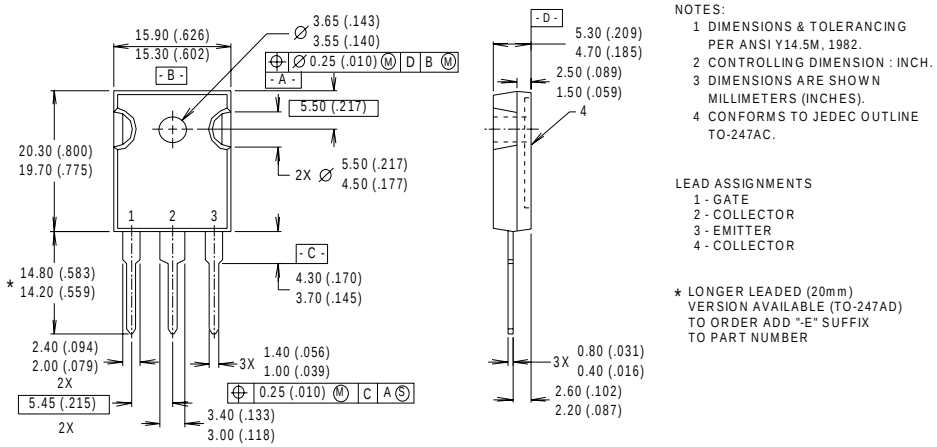
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 10Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371

International
IOR Rectifier

PD - 91592B

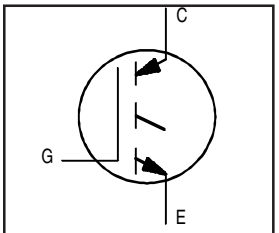
IRG4BC40K

Short Circuit Rated
UltraFast IGBT

INSULATED GATE BIPOLAR TRANSISTOR

Features

- Short Circuit Rated UltraFast: optimized for high operating frequencies >5.0 kHz , and Short Circuit Rated to 10µs @ 125°C, V_{GE} = 15V
- Generation 4 IGBT design provides higher efficiency than Generation 3
- Industry standard TO-247AC package



n-channel

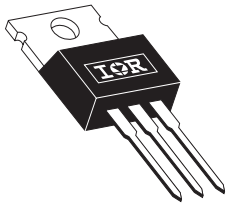
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.1V

@V_{GE} = 15V, I_C = 25A

Benefits

- Generation 4 IGBTs offer highest efficiency available
- IGBTs optimized for specified application conditions



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	42	A
I_C @ T_C = 100°C	Continuous Collector Current	25	
I_{CM}	Pulsed Collector Current ①	84	
I_{LM}	Clamped Inductive Load Current ②	84	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	15	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.77	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	80	
Wt	Weight	2 (0.07)	—	g (oz)

4/17/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.46	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.10	2.6	V	I_C = 25A V_{GE} = 15V
		—	2.70	—		I_C = 42A See Fig.2, 5
		—	2.14	—		I_C = 25A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-13	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	7.0	14	—	S	V_{CE} = 100 V, I_C = 25A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	2000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	120	180	nC	I_C = 25A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	16	24		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	51	77		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	30	—	ns	
t_r	Rise Time	—	15	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	140	210		I_C = 25A, V_{CC} = 480V
t_f	Fall Time	—	140	210		V_{GE} = 15V, R_G = 10Ω
E_{on}	Turn-On Switching Loss	—	0.62	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.33	—		See Fig. 9,10,14
E_{ts}	Total Switching Loss	—	0.95	1.4		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 400V, T_J = 125°C
						V_{GE} = 15V, R_G = 10Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	30	—	ns	T_J = 150°C,
t_r	Rise Time	—	18	—		I_C = 25A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	190	—		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	—	150	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.9	—	mJ	See Fig. 11,14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1600	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	130	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	55	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 10Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

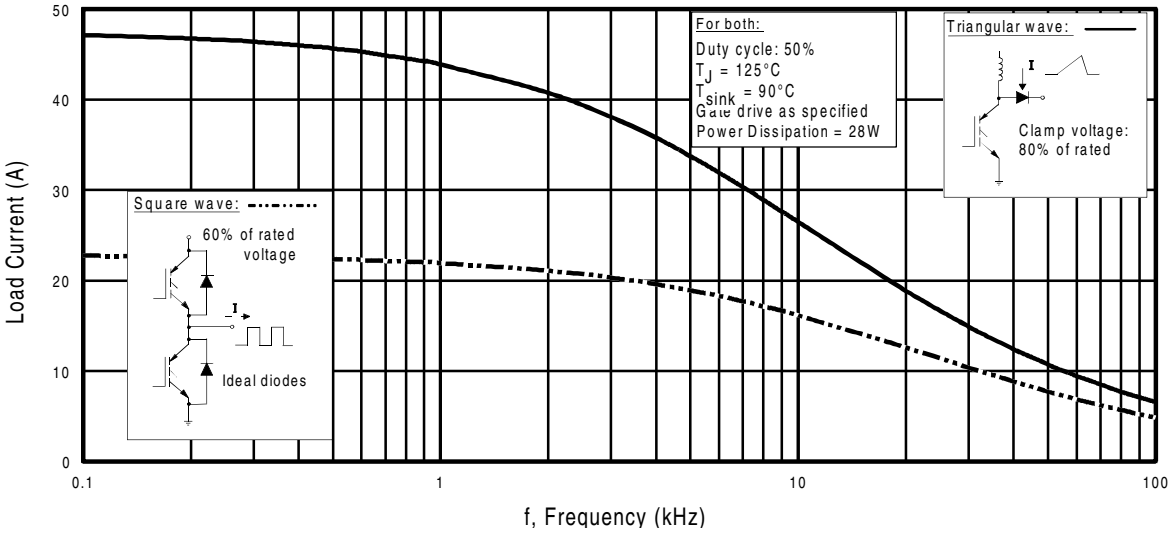


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

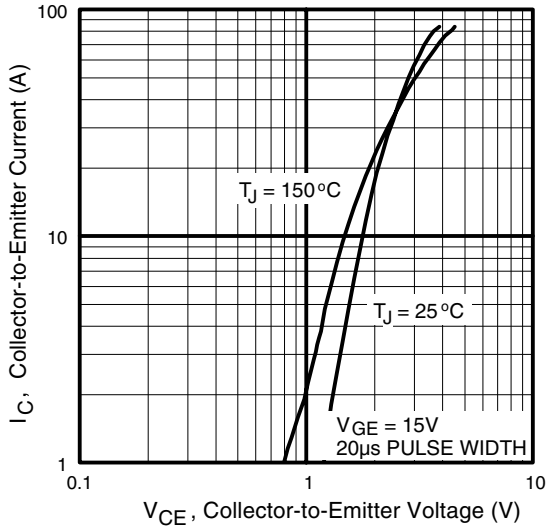


Fig. 2 - Typical Output Characteristics

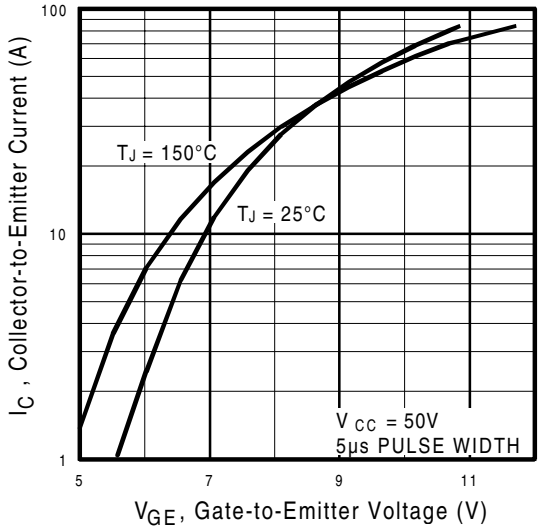


Fig. 3 - Typical Transfer Characteristics

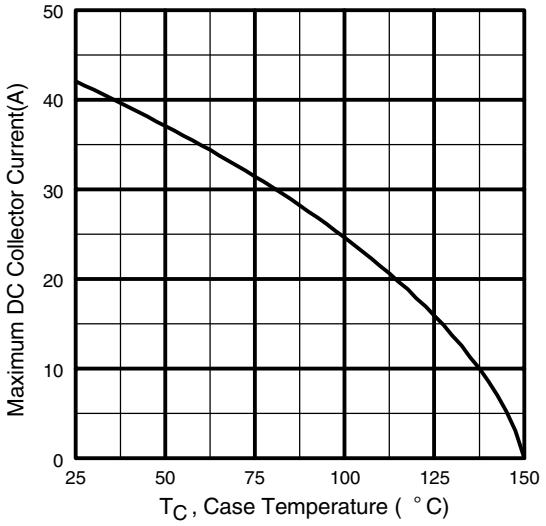


Fig. 4 - Maximum Collector Current vs. Case Temperature

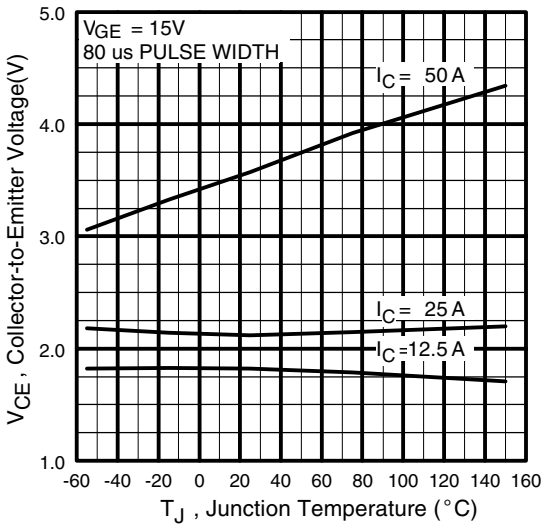


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

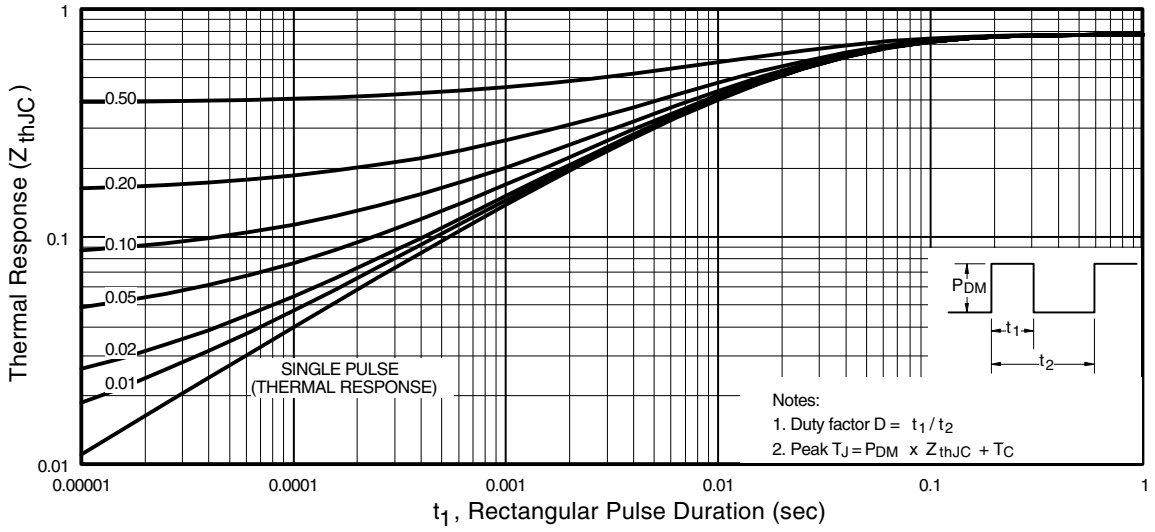


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

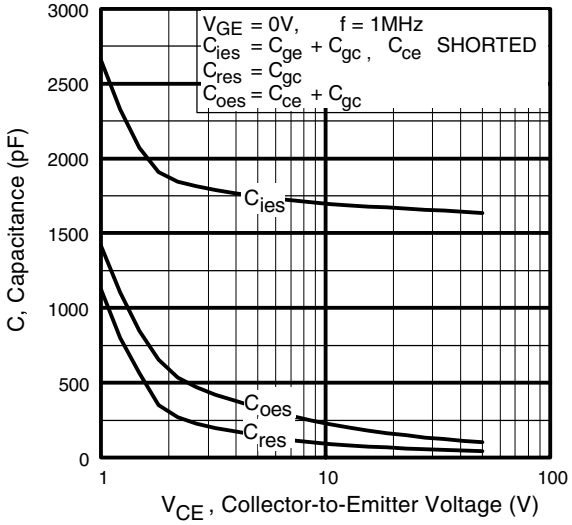


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

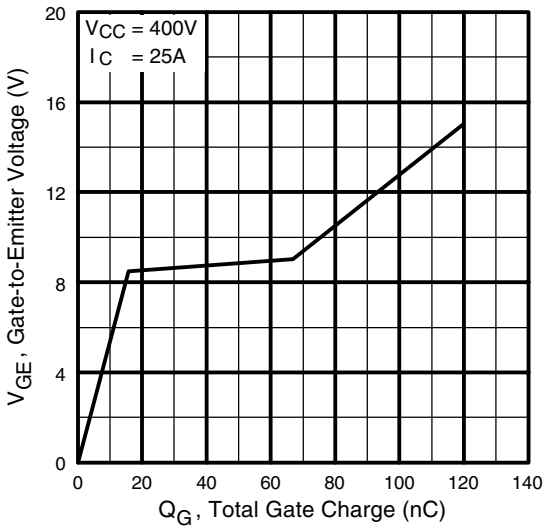


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

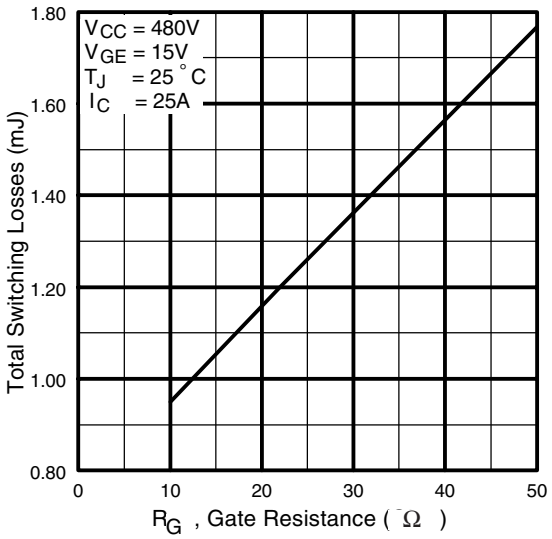


Fig. 9 - Typical Switching Losses vs. Gate Resistance

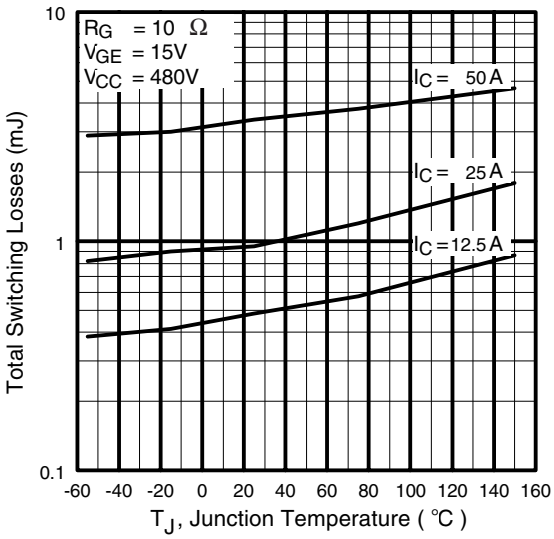


Fig. 10 - Typical Switching Losses vs. Junction Temperature

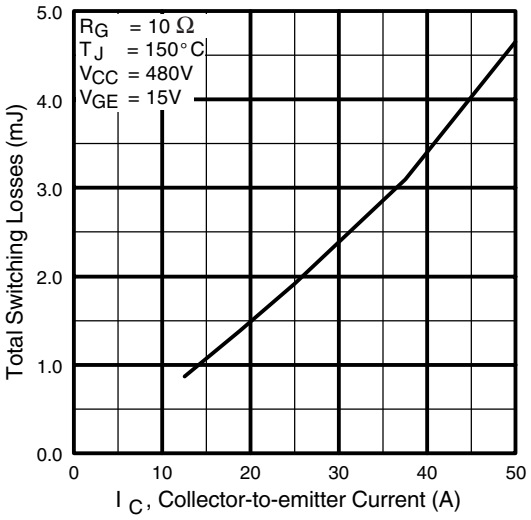


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

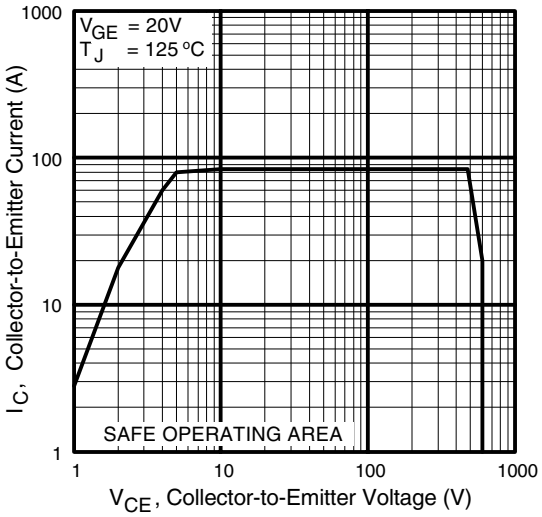


Fig. 12 - Turn-Off SOA

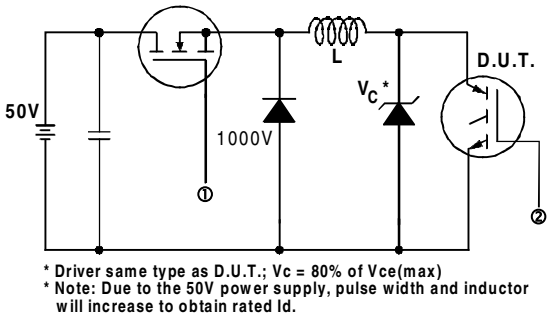


Fig. 13a - Clamped Inductive Load Test Circuit

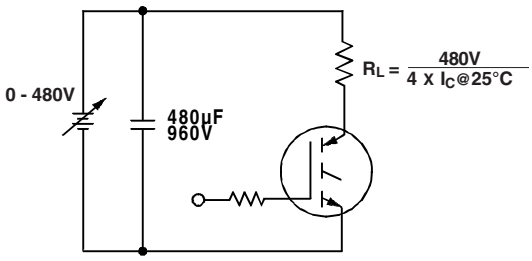


Fig. 13b - Pulsed Collector Current Test Circuit

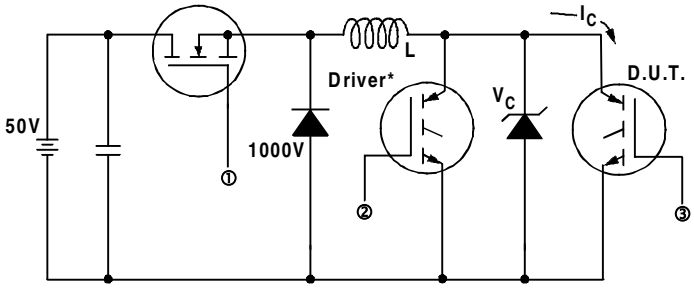


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

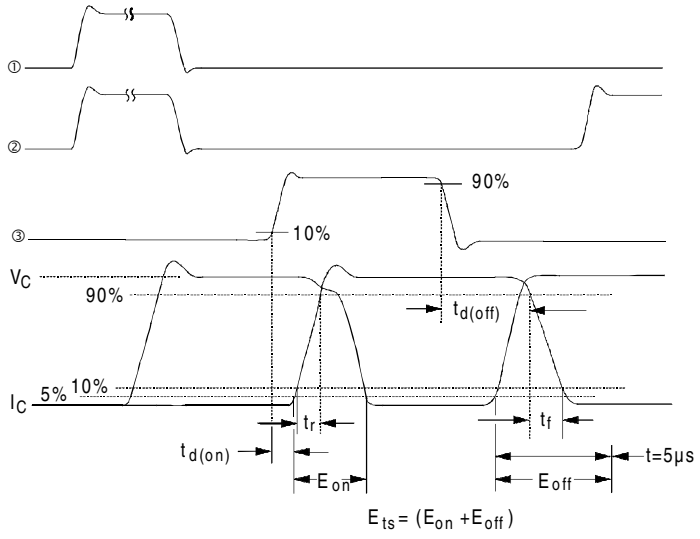
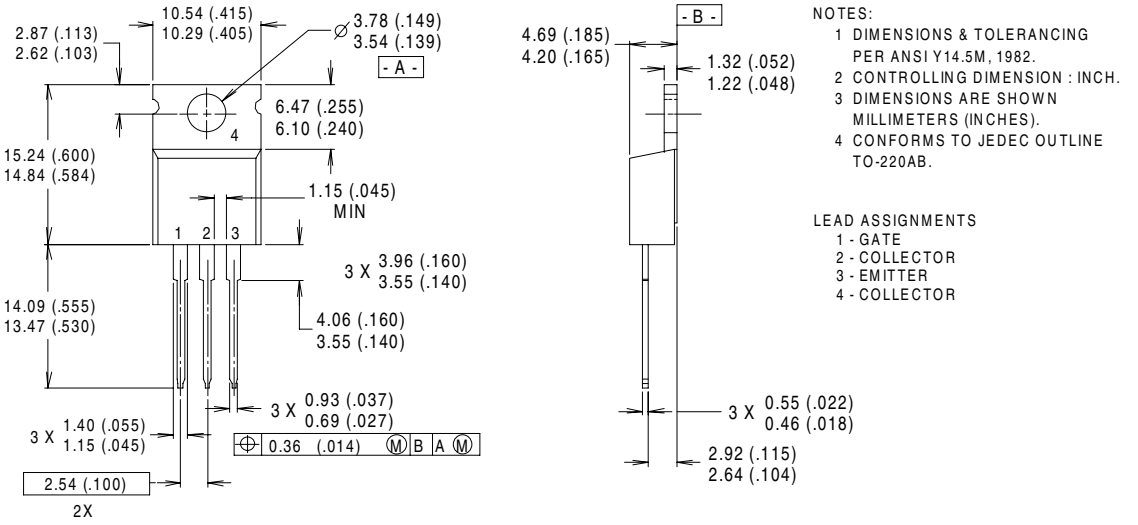


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-220AB



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-220AB.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

International
IOR Rectifier

PD - 9.1585B

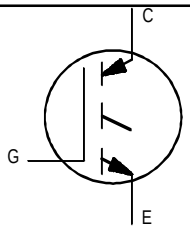
IRG4PC40K

Short Circuit Rated
UltraFast IGBT

INSULATED GATE BIPOLAR TRANSISTOR

Features

- Short Circuit Rated UltraFast: Optimized for high operating frequencies >5.0 kHz , and Short Circuit Rated to 10µs @ 125°C, V_{GE} = 15V
- Generation 4 IGBT design provides higher efficiency than Generation 3
- Industry standard TO-247AC package



n-channel

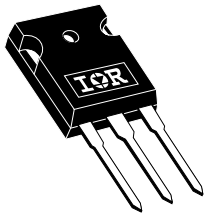
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.1V

@V_{GE} = 15V, I_C = 25A

Benefits

- Generation 4 IGBTs offer highest efficiency available
- IGBTs optimized for specified application conditions



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	42	A
I_C @ T_C = 100°C	Continuous Collector Current	25	
I_{CM}	Pulsed Collector Current ①	84	
I_{LM}	Clamped Inductive Load Current ②	84	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	15	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.77	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.46	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.10	2.6	V	I_C = 25A V_{GE} = 15V
		—	2.70	—		I_C = 42A See Fig.2, 5
		—	2.14	—		I_C = 25A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-13	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	7.0	14	—	S	V_{CE} = 100 V, I_C = 25A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	2000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	120	180	nC	I_C = 25A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	16	24		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	51	77		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	30	—	ns	
t_r	Rise Time	—	15	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	140	210		I_C = 25A, V_{CC} = 480V
t_f	Fall Time	—	140	210		V_{GE} = 15V, R_G = 10Ω
E_{on}	Turn-On Switching Loss	—	0.62	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.33	—		See Fig. 9,10,14
E_{ts}	Total Switching Loss	—	0.95	1.4		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 400V, T_J = 125°C
						V_{GE} = 15V, R_G = 10Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	30	—	ns	T_J = 150°C,
t_r	Rise Time	—	18	—		I_C = 25A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	190	—		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	—	150	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.9	—	mJ	See Fig. 11,14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1600	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	130	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	55	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 10Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

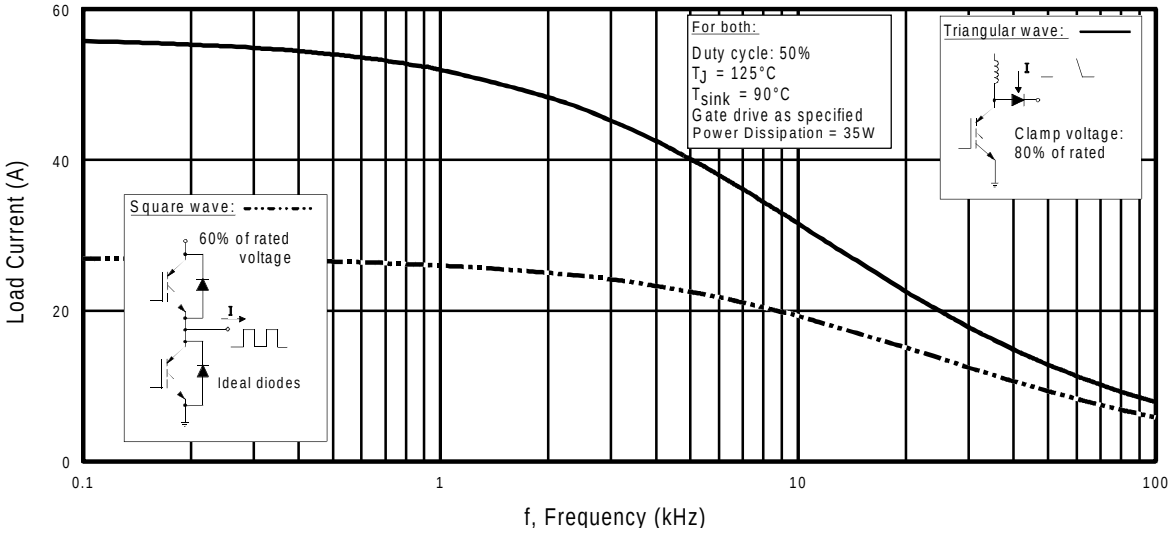


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

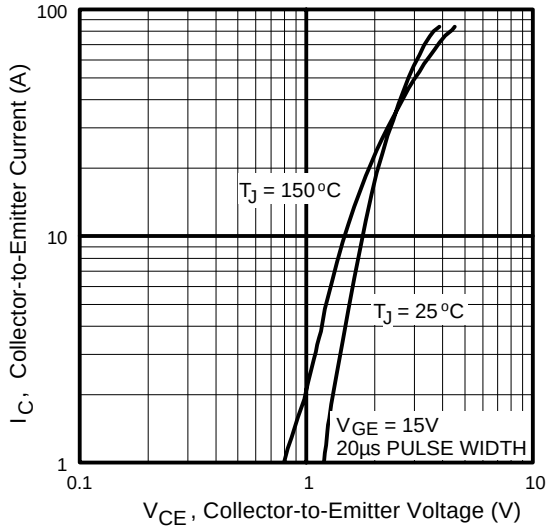


Fig. 2 - Typical Output Characteristics

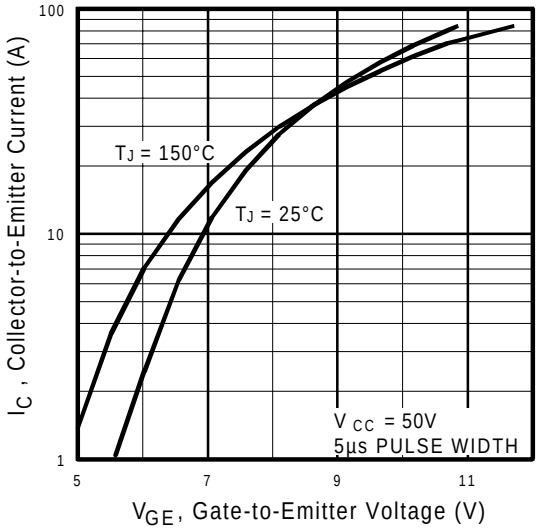


Fig. 3 - Typical Transfer Characteristics

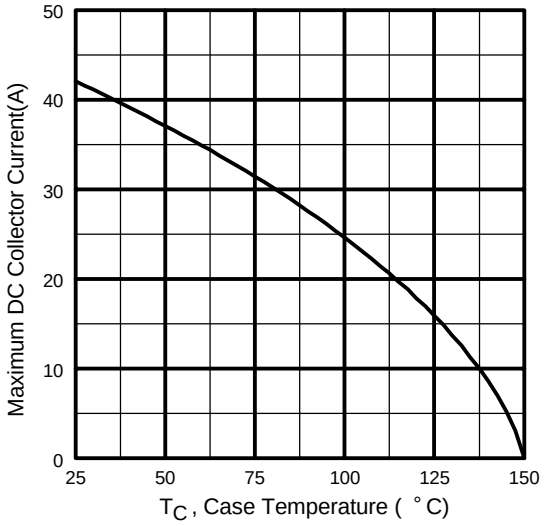


Fig. 4 - Maximum Collector Current vs. Case Temperature

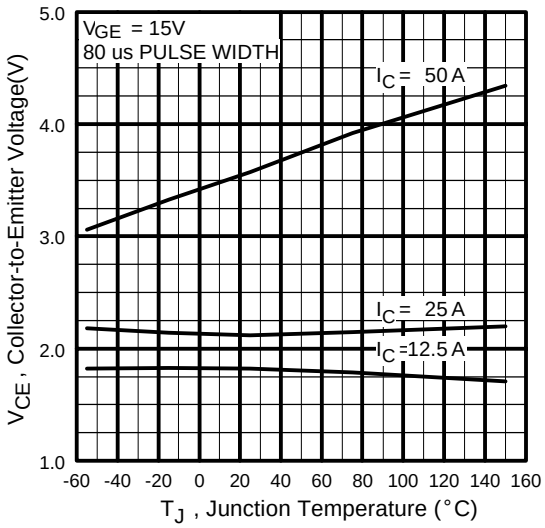


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

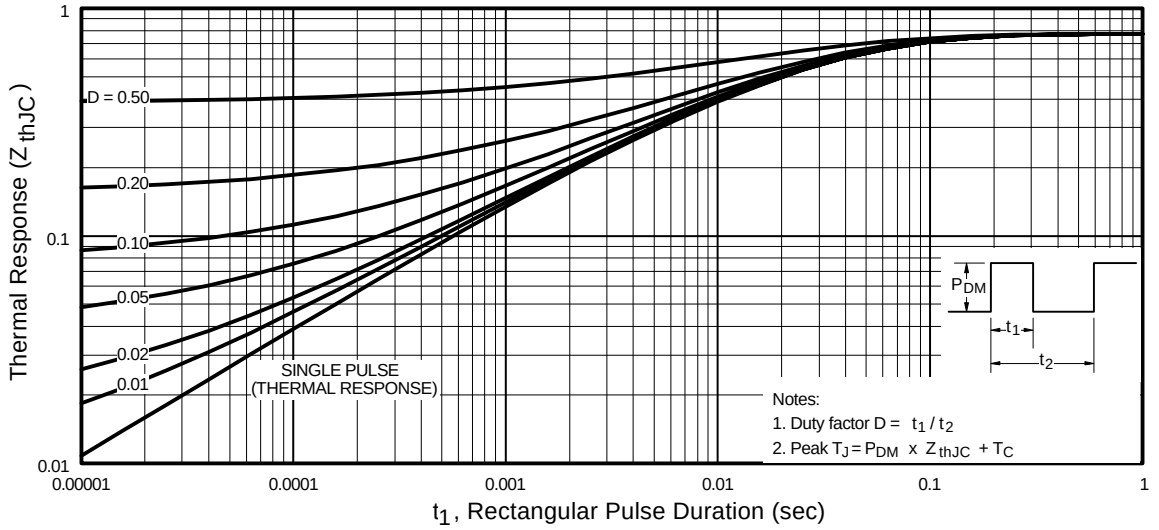


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

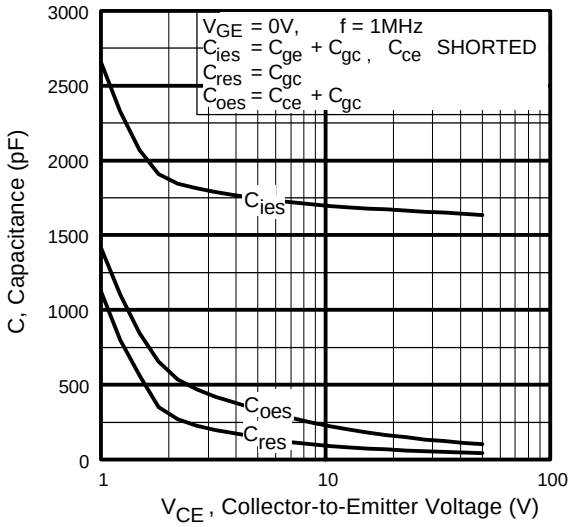


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

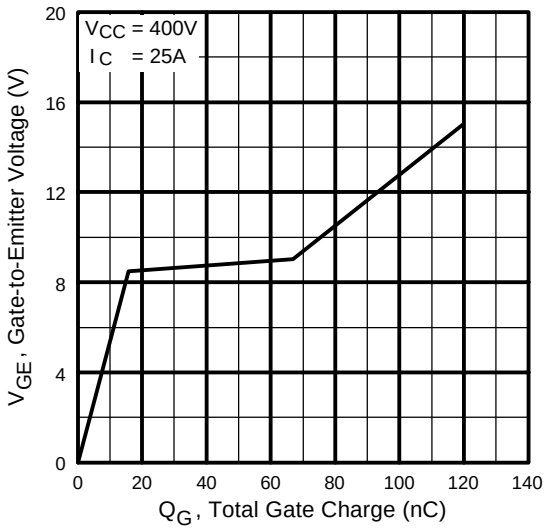


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

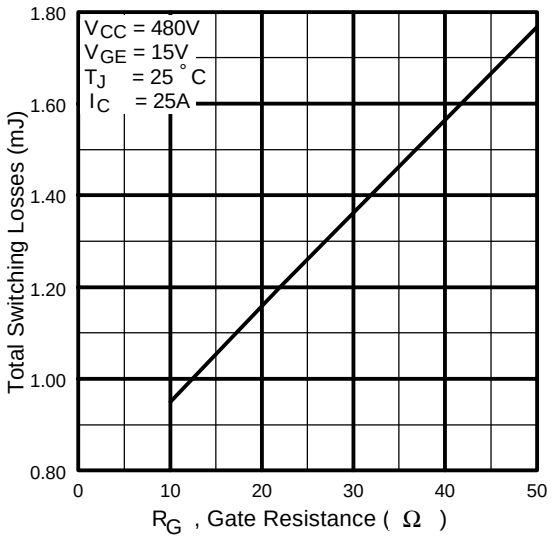


Fig. 9 - Typical Switching Losses vs. Gate Resistance

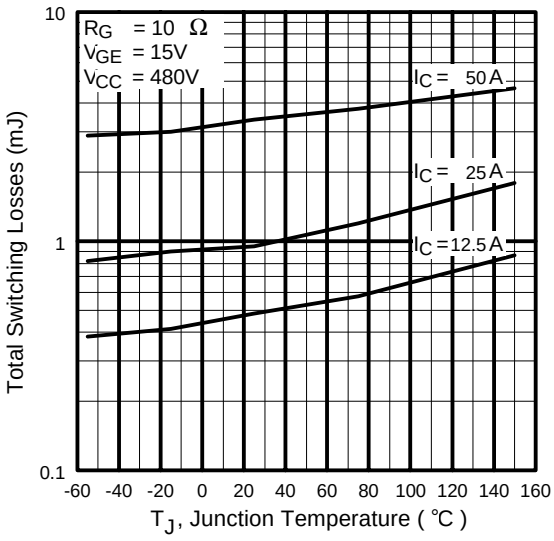


Fig. 10 - Typical Switching Losses vs. Junction Temperature

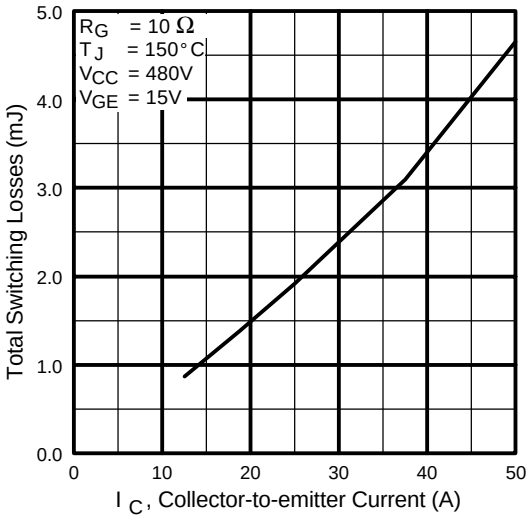


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

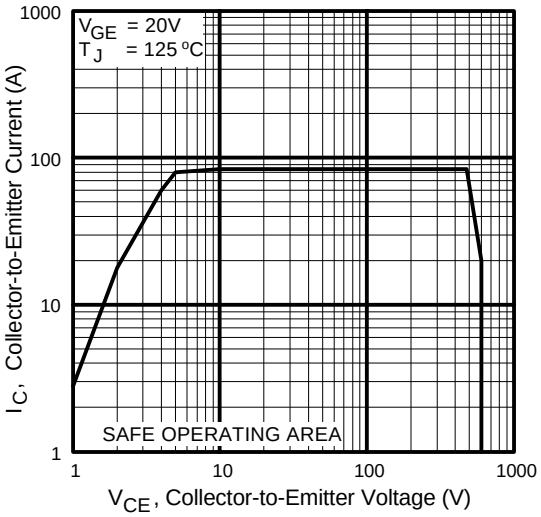


Fig. 12 - Turn-Off SOA

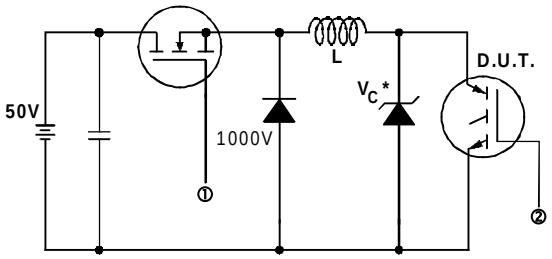


Fig. 13a - Clamped Inductive Load Test Circuit

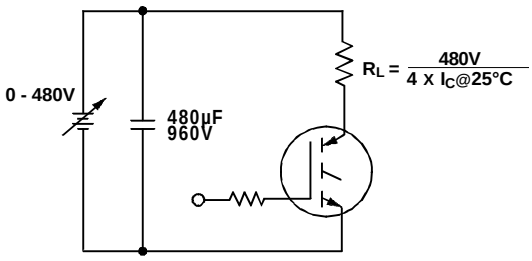


Fig. 13b - Pulsed Collector Current Test Circuit

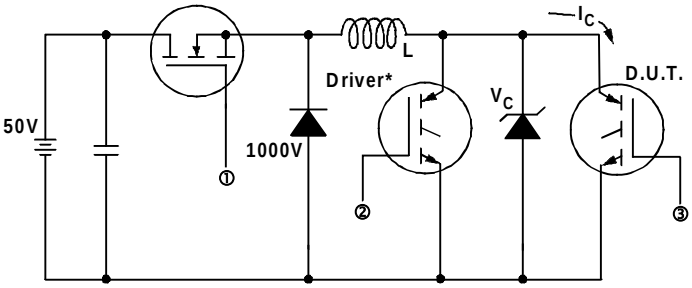


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

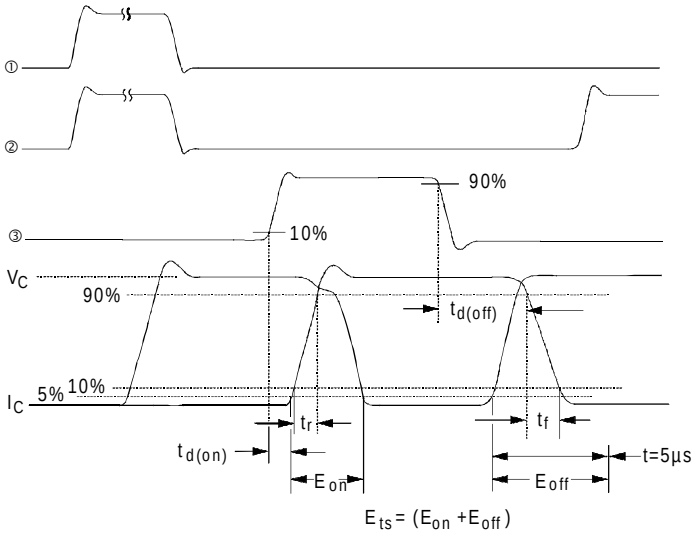
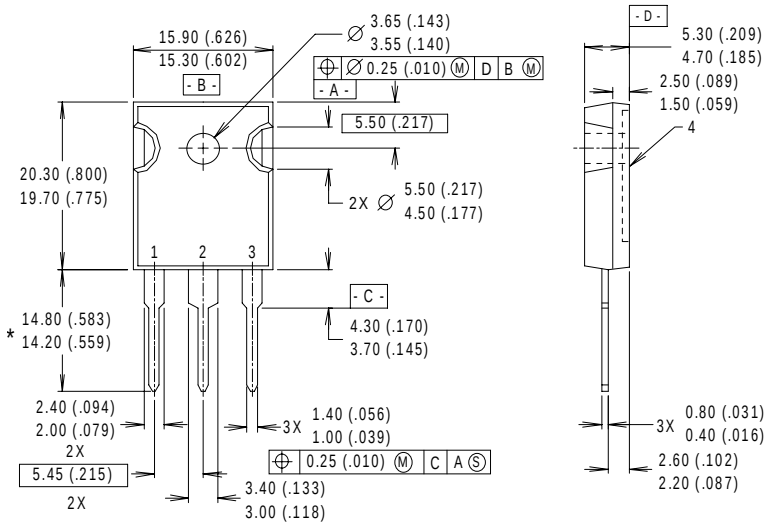


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

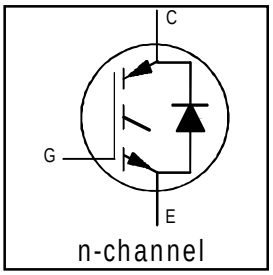
PD -91584A

International
IOR Rectifier

IRG4PC40KD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
UltraFast IGBT



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.1V

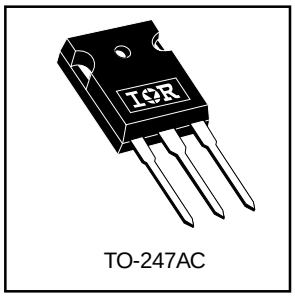
@V_{GE} = 15V, I_C = 25A

Features

- Short Circuit Rated UltraFast: Optimized for high operating frequencies >5.0 kHz , and Short Circuit Rated to 10µs @ 125°C, V_{GE} = 15V
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-247AC package

Benefits

- Generation 4 IGBTs offer highest efficiencies available
- HEXFRED diodes optimized for performance with IGBTs. Minimized recovery characteristics require less/no snubbing
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	42	A
I_C @ T_C = 100°C	Continuous Collector Current	25	
I_{CM}	Pulsed Collector Current ①	84	
I_{LM}	Clamped Inductive Load Current ②	84	
I_F @ T_C = 100°C	Diode Continuous Forward Current	15	
I_{FM}	Diode Maximum Forward Current	84	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	0.77	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	1.7	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	40	
Wt	Weight	—	6 (0.21)	—	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.46	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.10	2.6	V	I_C = 25A, V_{GE} = 15V
		—	2.70	—		I_C = 42A, See Fig. 2, 5
		—	2.14	—		I_C = 25A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-13	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	7.0	14	—	S	V_{CE} = 100V, I_C = 25A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	3500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.3	1.7	V	I_C = 15A, See Fig. 13
		—	1.2	1.6		I_C = 15A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	120	180	nC	I_C = 25A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	16	24		V_{CC} = 400V, See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	51	77		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	53	—	ns	
t_r	Rise Time	—	33	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	110	160		I_C = 25A, V_{CC} = 480V
t_f	Fall Time	—	100	150		V_{GE} = 15V, R_G = 10Ω
E_{on}	Turn-On Switching Loss	—	0.95	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.76	—		See Fig. 9,10,14
E_{ts}	Total Switching Loss	—	1.71	2.3		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 360V, T_J = 125°C
						V_{GE} = 15V, R_G = 10Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	52	—	ns	T_J = 150°C,
t_r	Rise Time	—	37	—		I_C = 25A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	220	—		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	—	140	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	2.67	—	mJ	See Fig. 11,14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1600	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	130	—		V_{CC} = 30V, See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	55	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	42	60	ns	T_J = 25°C, See Fig.
		—	74	120		T_J = 125°C, 14, I_F = 15A
I_{rr}	Diode Peak Reverse Recovery Current	—	4.0	6.0	A	T_J = 25°C, See Fig.
		—	6.5	10		T_J = 125°C, 15, V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	80	180	nC	T_J = 25°C, See Fig.
		—	220	600		T_J = 125°C, 16, di/dt = 200Aµs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	188	—	A/µs	T_J = 25°C, See Fig.
	During t_b	—	160	—		T_J = 125°C, 17

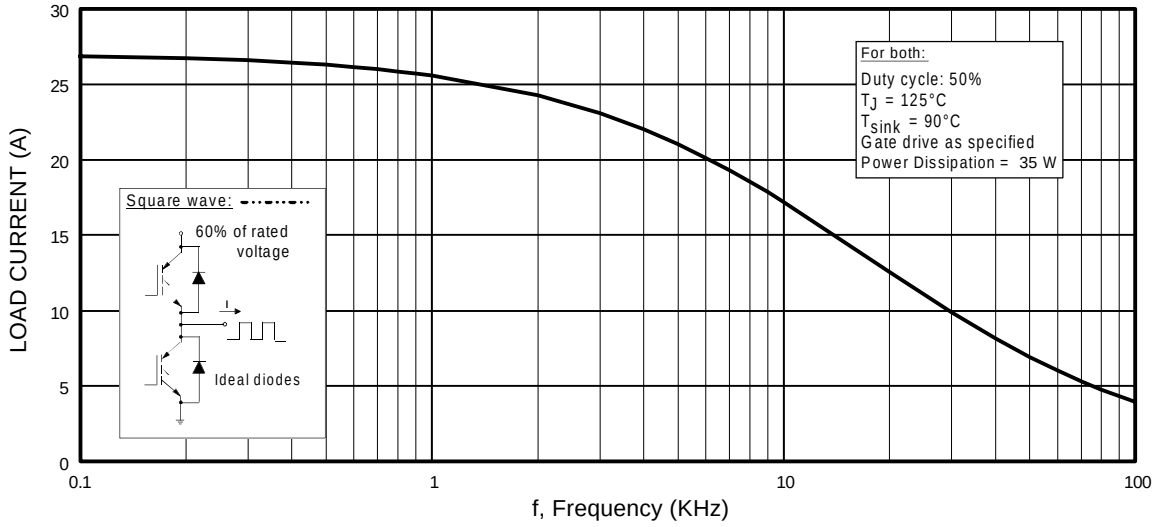


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

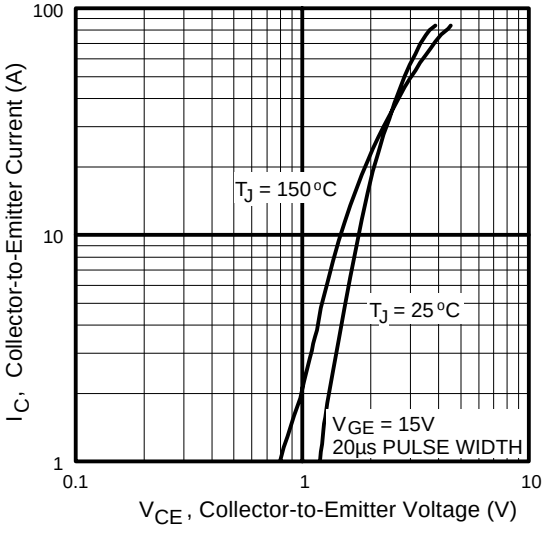


Fig. 2 - Typical Output Characteristics

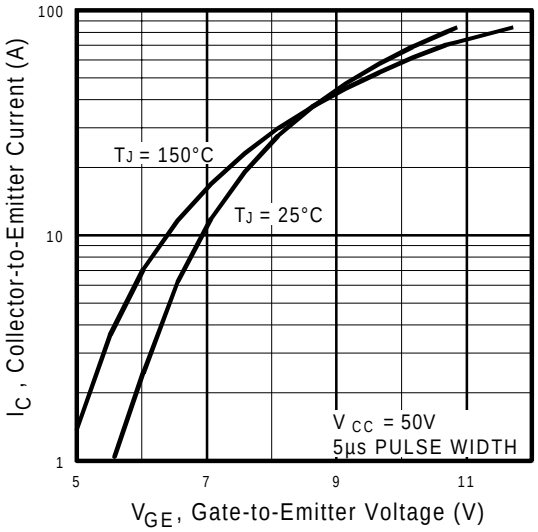


Fig. 3 - Typical Transfer Characteristics

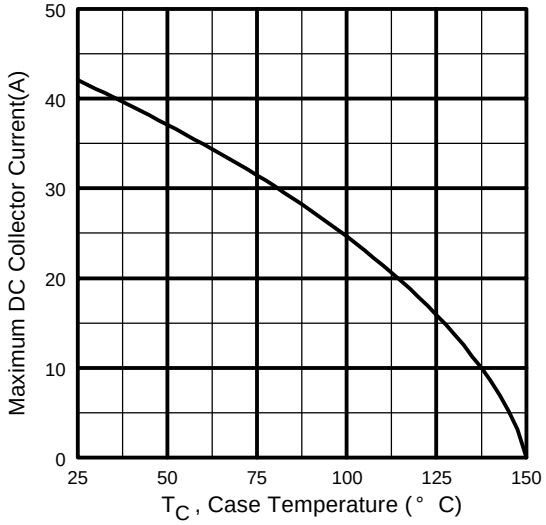


Fig. 4 - Maximum Collector Current vs. Case Temperature

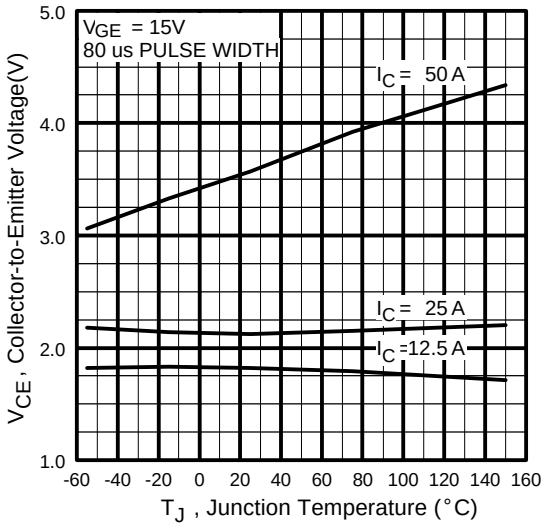


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

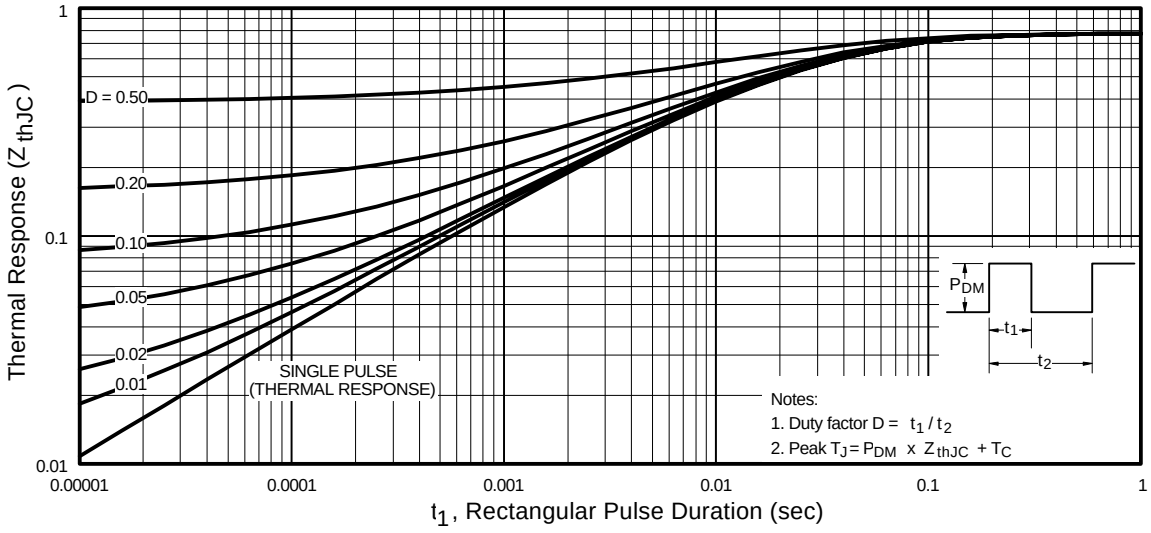


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

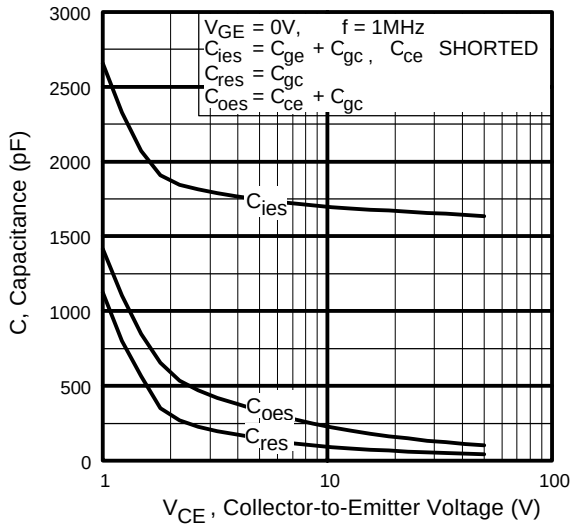


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

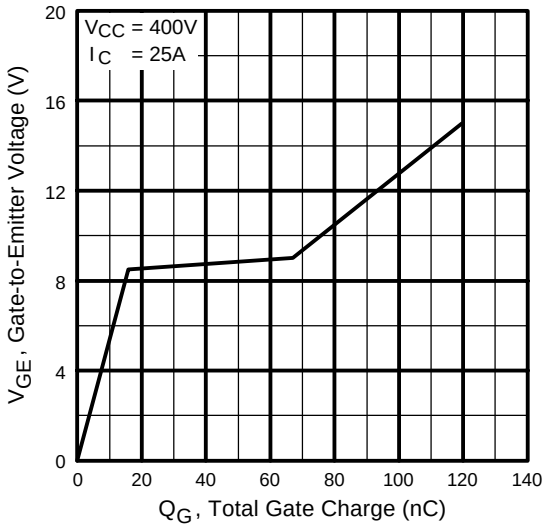


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

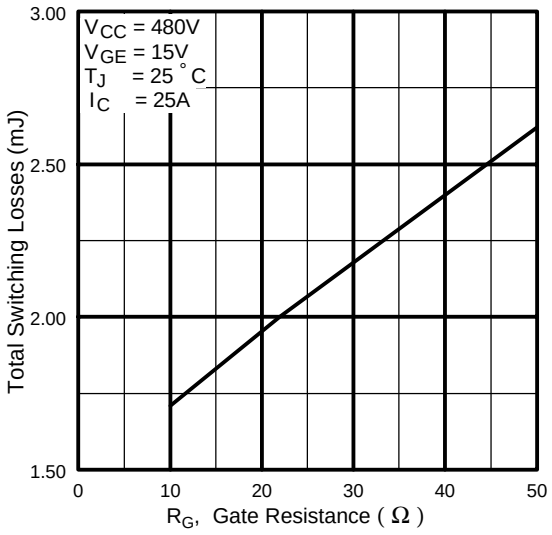


Fig. 9 - Typical Switching Losses vs. Gate Resistance

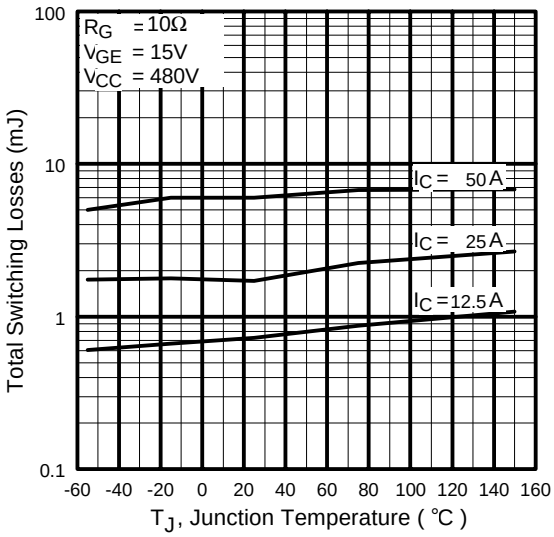


Fig. 10 - Typical Switching Losses vs. Junction Temperature

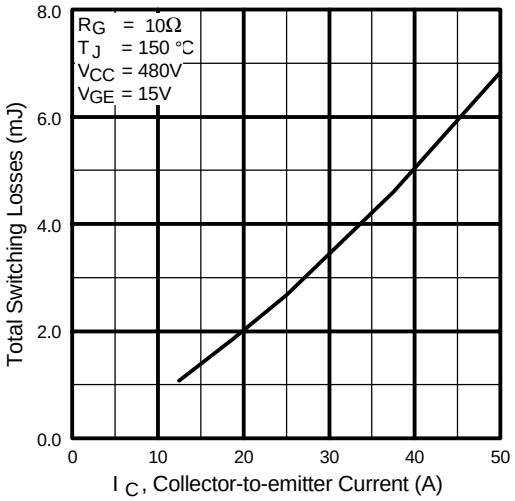


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

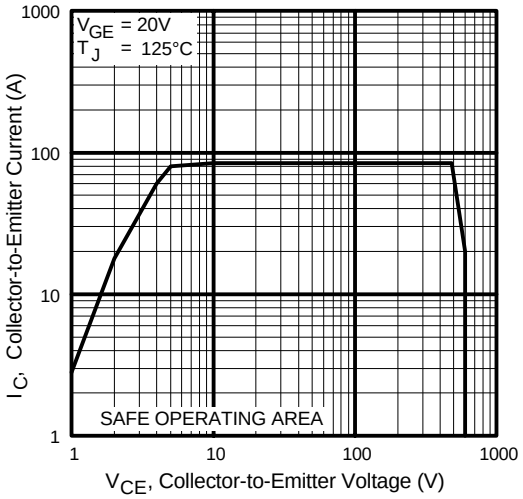


Fig. 12 - Turn-Off SOA

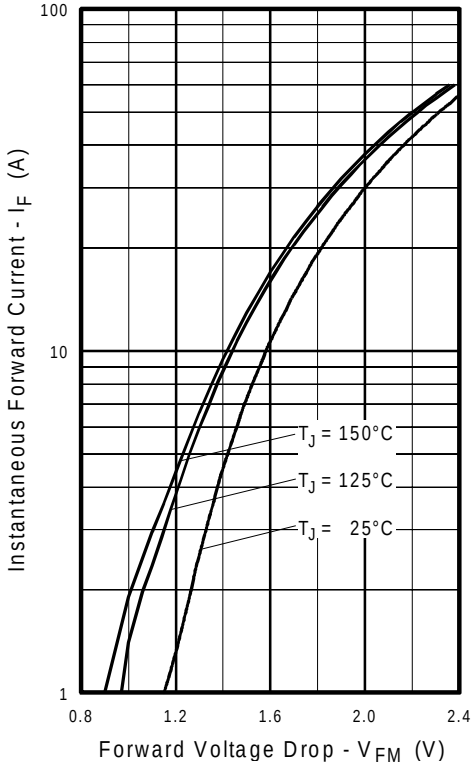


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

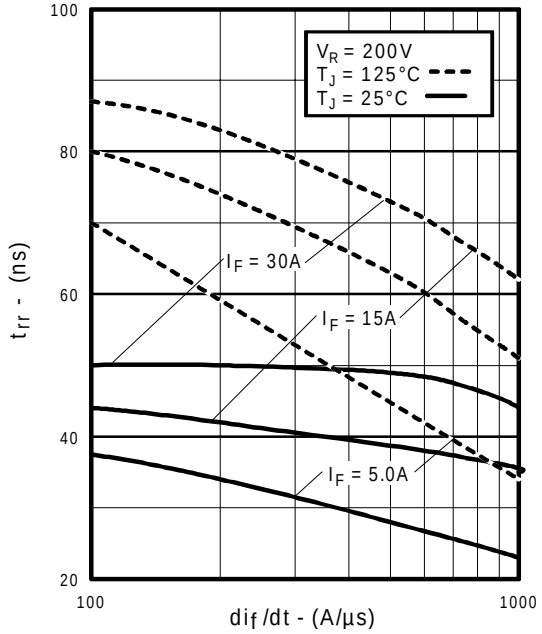


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

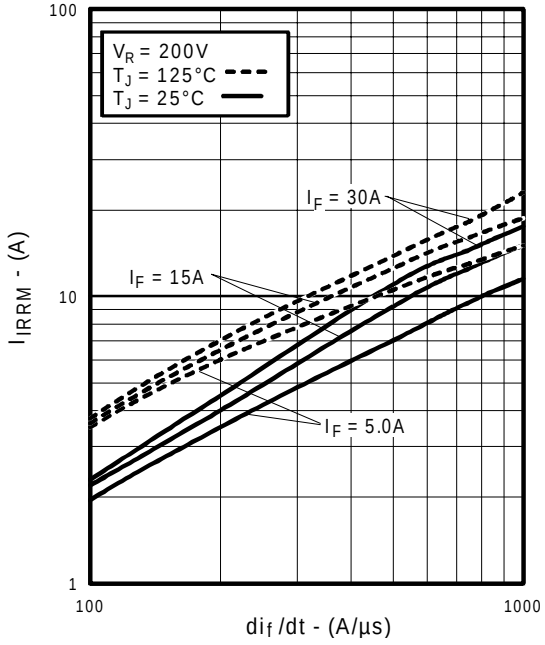


Fig. 15 - Typical Recovery Current vs. di_f/dt

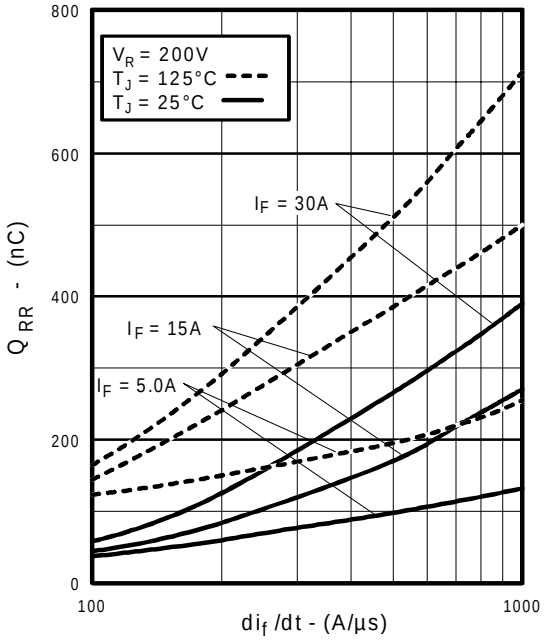


Fig. 16 - Typical Stored Charge vs. di_f/dt

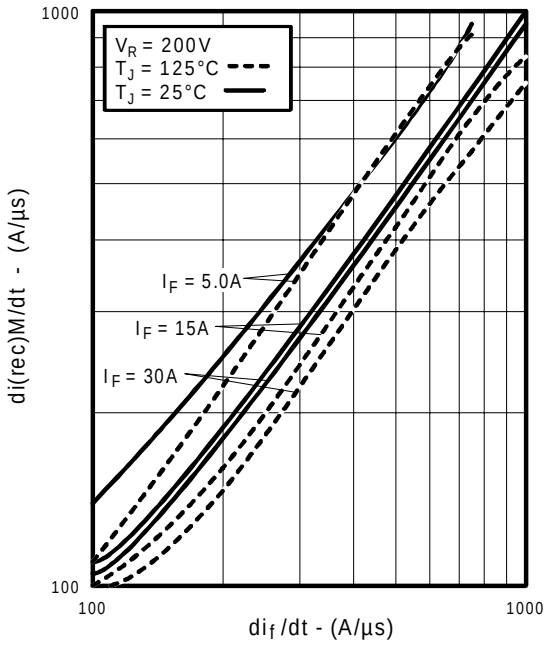


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

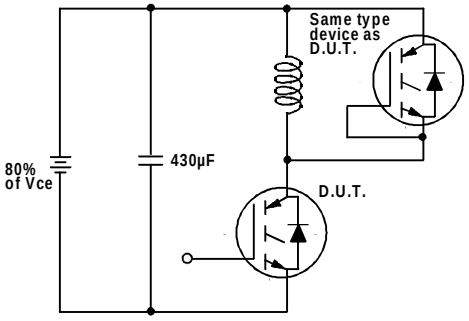


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

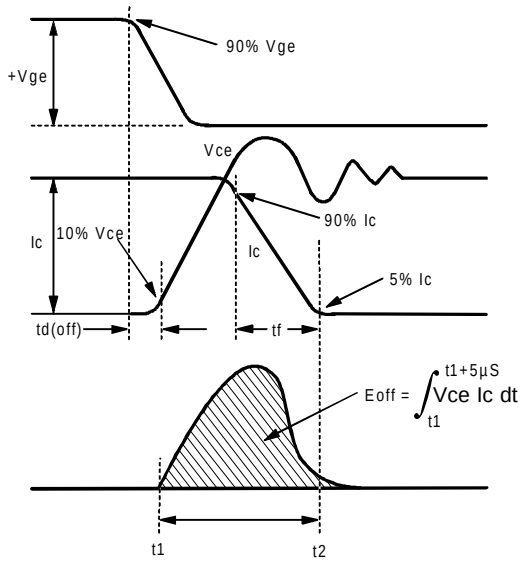


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

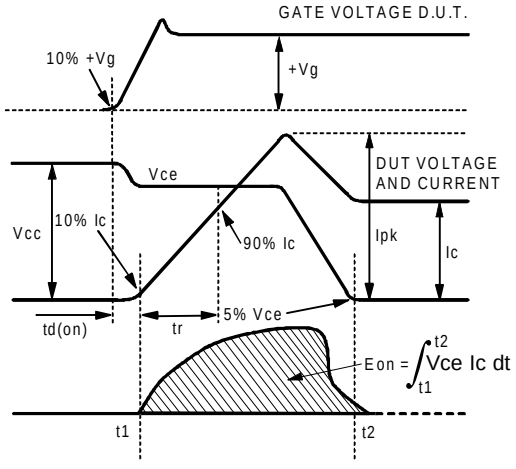


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

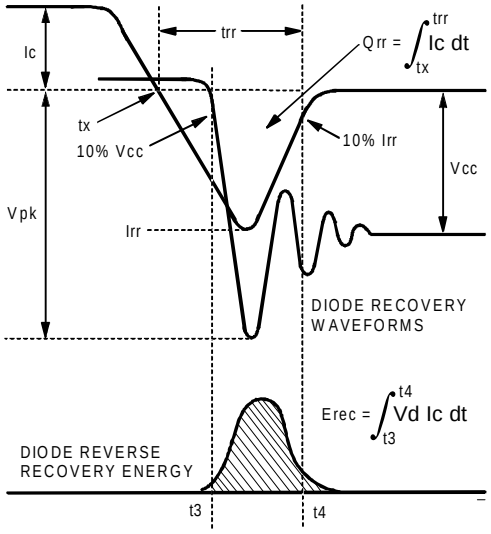


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

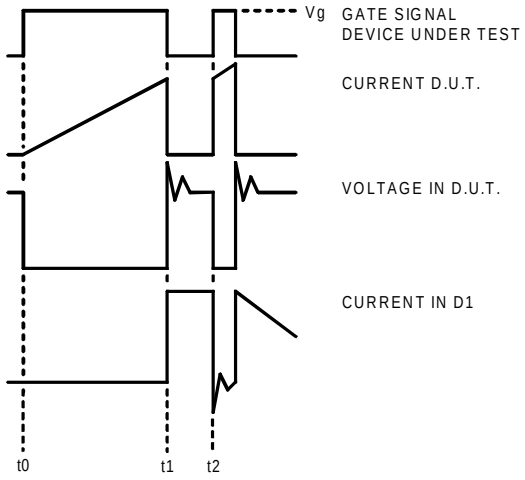


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

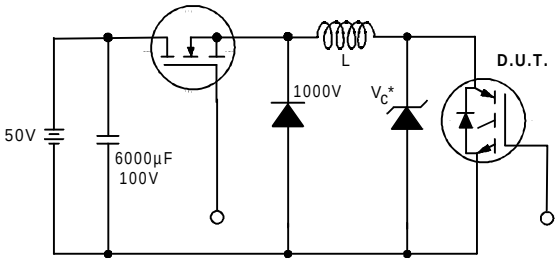


Figure 19. Clamped Inductive Load Test Circuit

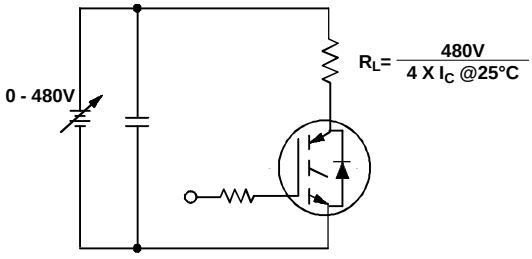


Figure 20. Pulsed Collector Current Test Circuit

Notes:

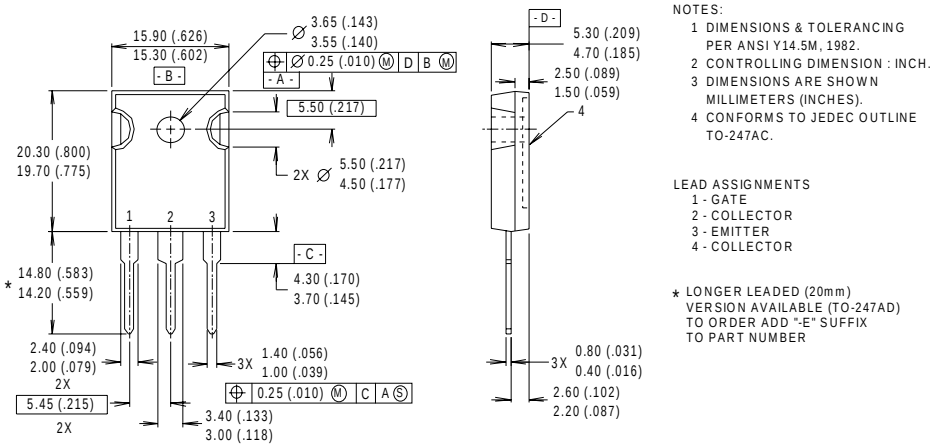
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 10Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD - 91454B

International
IOR Rectifier

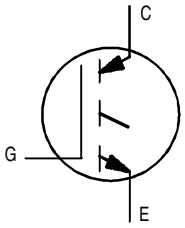
IRG4BC40F

INSULATED GATE BIPOLAR TRANSISTOR

Fast Speed IGBT

Features

- Fast: optimized for medium operating frequencies (1-5 kHz in hard switching, >20 kHz in resonant mode).
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-220AB package



n-channel

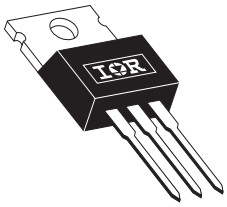
$V_{CES} = 600V$

$V_{CE(on)\ typ.} = 1.50V$

$@V_{GE} = 15V, I_C = 27A$

Benefits

- Generation 4 IGBTs offer highest efficiency available
- IGBTs optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	49	A
I_C @ T_C = 100°C	Continuous Collector Current	27	
I_{CM}	Pulsed Collector Current ①	200	
I_{LM}	Clamped Inductive Load Current ②	200	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	15	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.77	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	80	
Wt	Weight	2.0 (0.07)	—	g (oz)

4/17/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.70	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.50	1.7	V	I_C = 27A V_{GE} = 15V
		—	1.85	—		I_C = 49A See Fig.2, 5
		—	1.56	—		I_C = 27A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-12	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	9.2	12	—	S	V_{CE} = 100V, I_C = 27A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	100	150	nC	I_C = 27A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	15	23		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	35	53		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	26	—	ns	
t_r	Rise Time	—	18	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	240	360		I_C = 27A, V_{CC} = 480V
t_f	Fall Time	—	170	250		V_{GE} = 15V, R_G = 10Ω
E_{on}	Turn-On Switching Loss	—	0.37	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	1.81	—		See Fig. 10, 11, 13, 14
E_{ts}	Total Switching Loss	—	2.18	2.8		
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	T_J = 150°C,
t_r	Rise Time	—	21	—		I_C = 27A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	380	—		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	—	310	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	3.9	—	mJ	See Fig. 13, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	2200	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	140	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	29	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 10Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

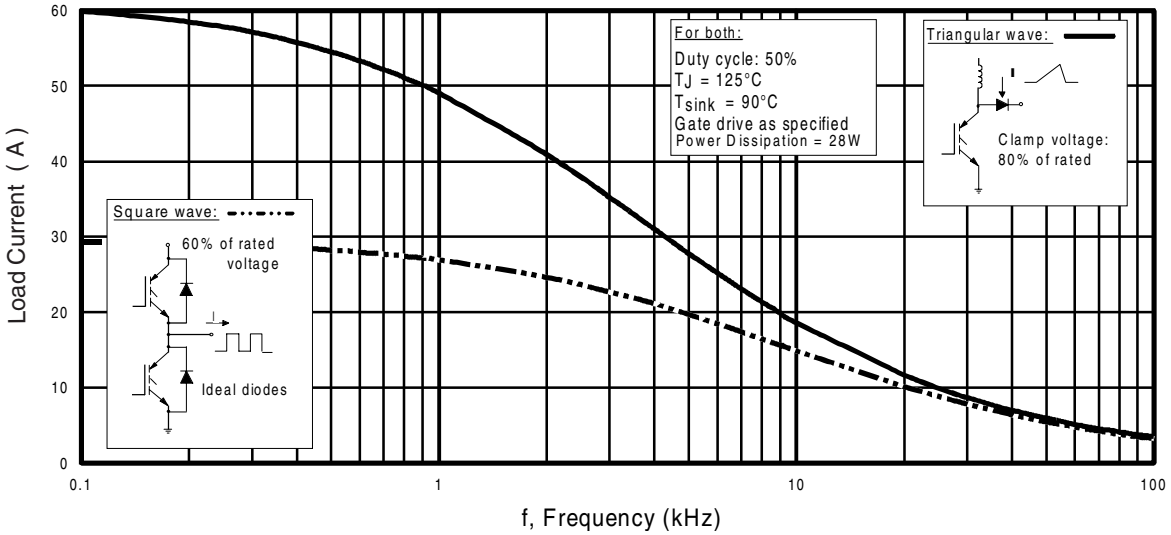


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

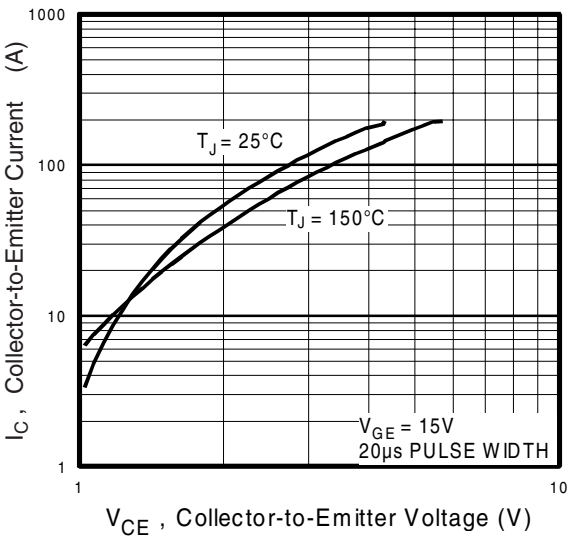


Fig. 2 - Typical Output Characteristics

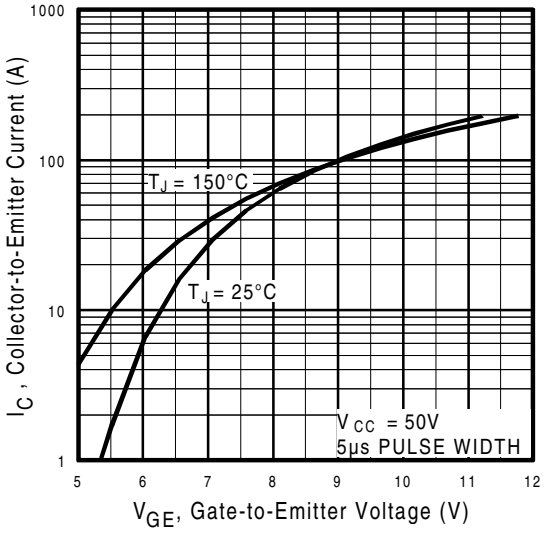


Fig. 3 - Typical Transfer Characteristics

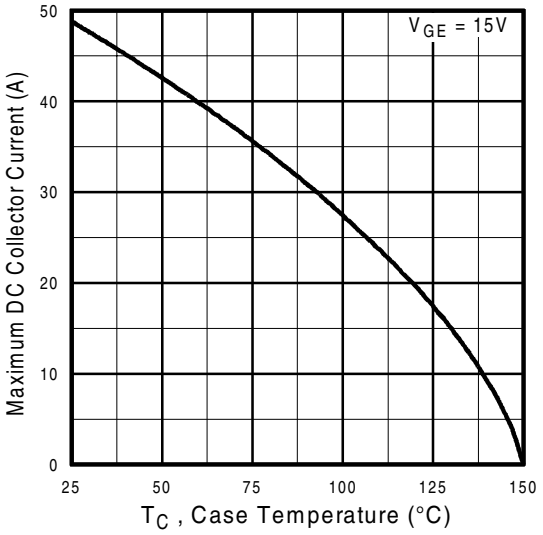


Fig. 4 - Maximum Collector Current vs. Case Temperature

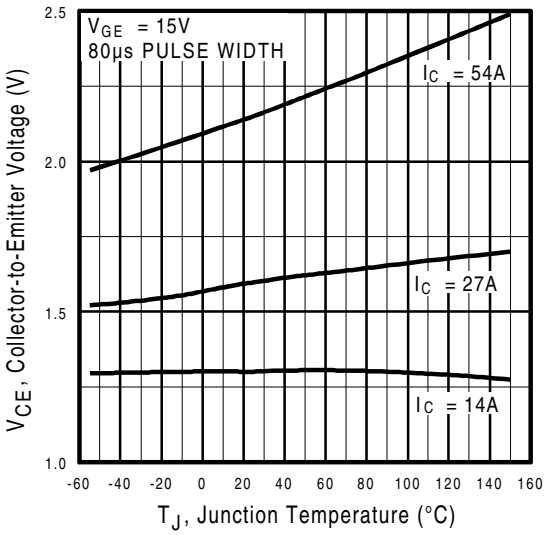


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

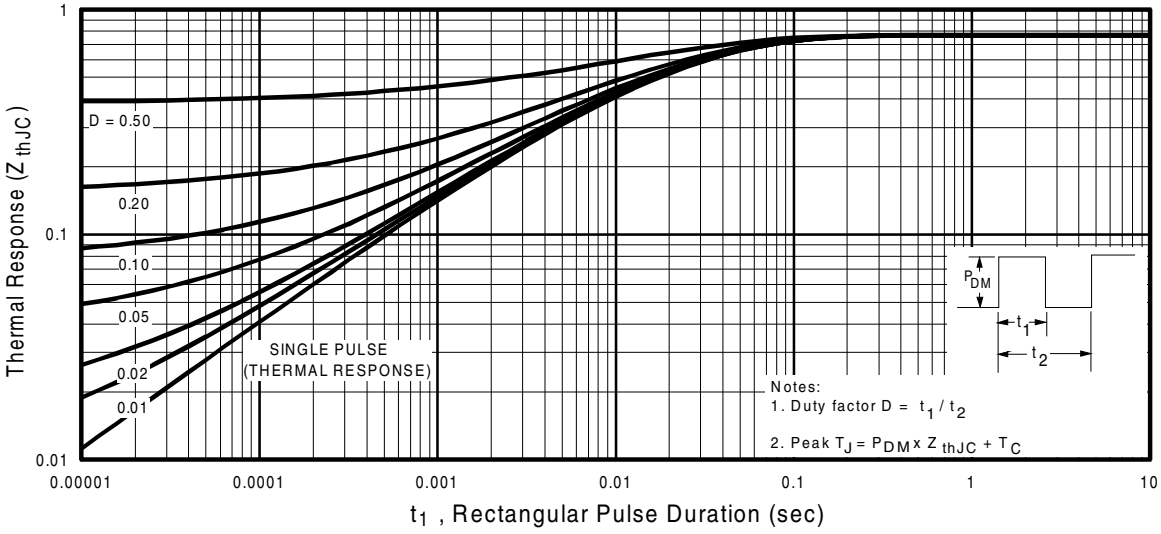


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

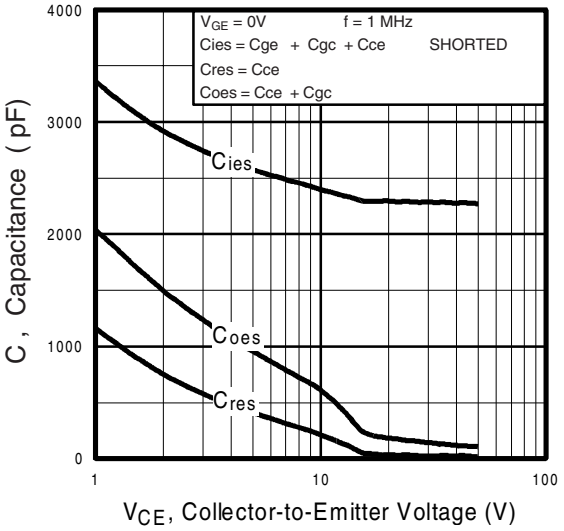


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

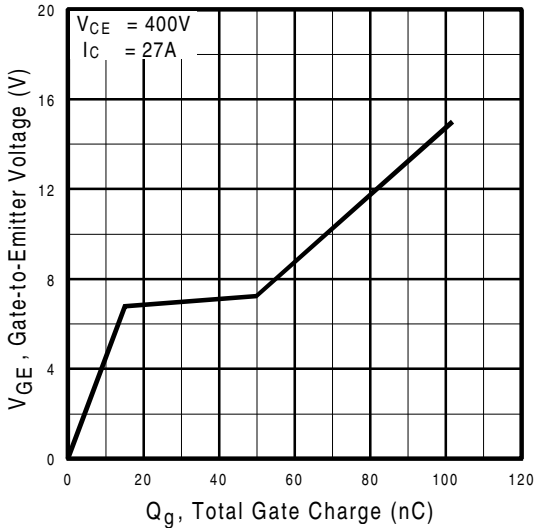


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

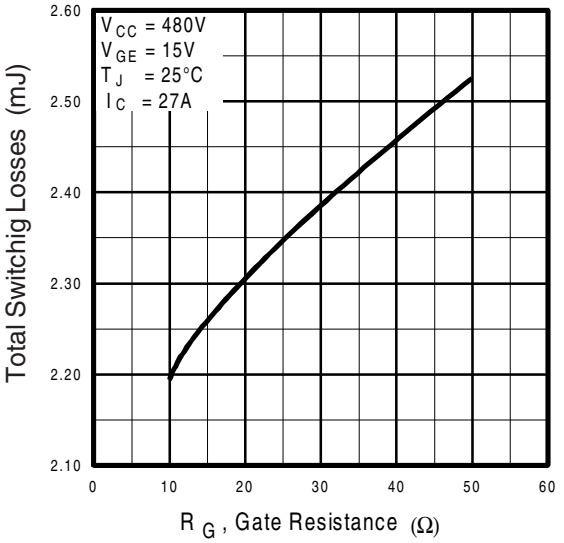


Fig. 9 - Typical Switching Losses vs. Gate Resistance

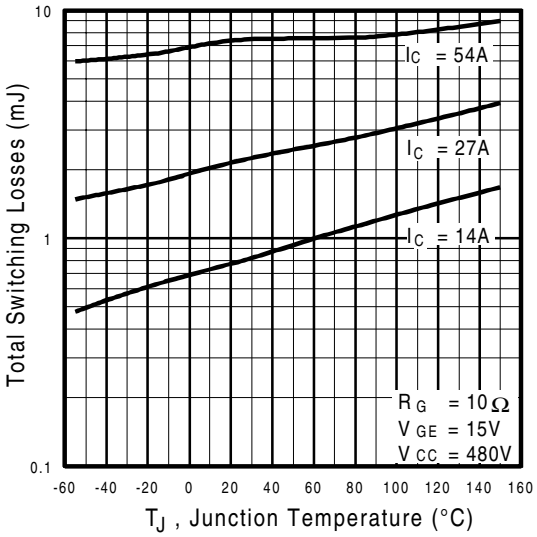


Fig. 10 - Typical Switching Losses vs. Junction Temperature

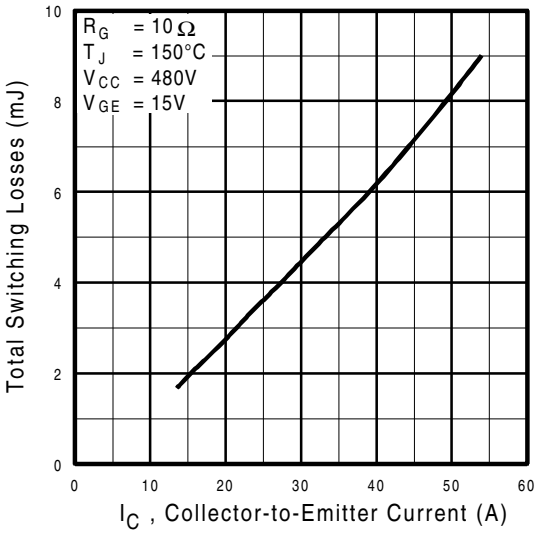


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

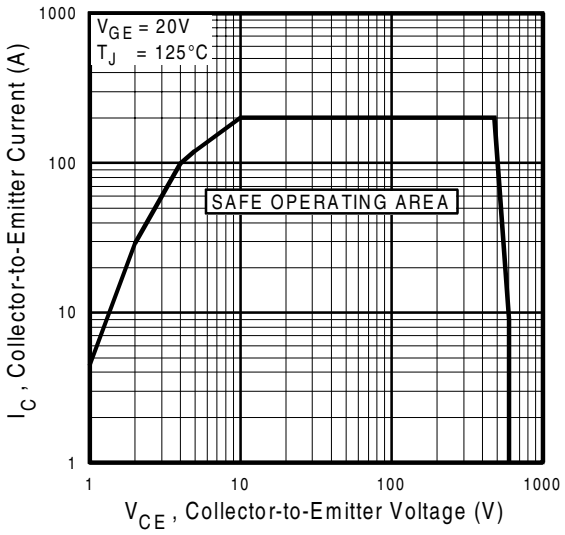


Fig. 12 - Turn-Off SOA

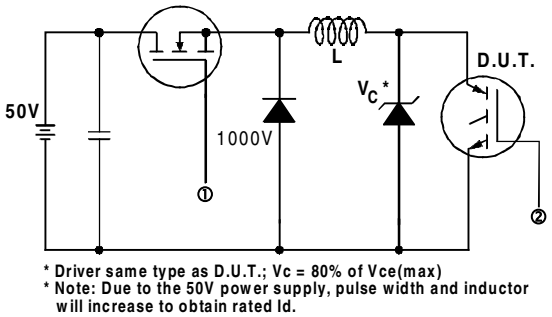


Fig. 13a - Clamped Inductive Load Test Circuit

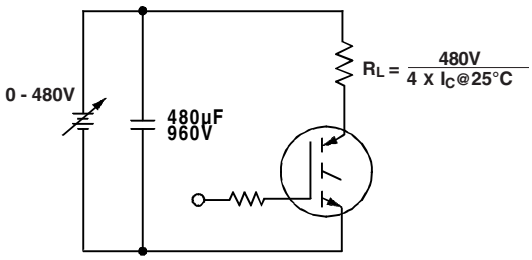


Fig. 13b - Pulsed Collector Current Test Circuit

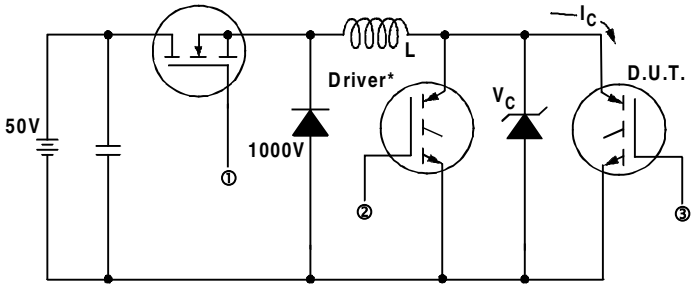


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

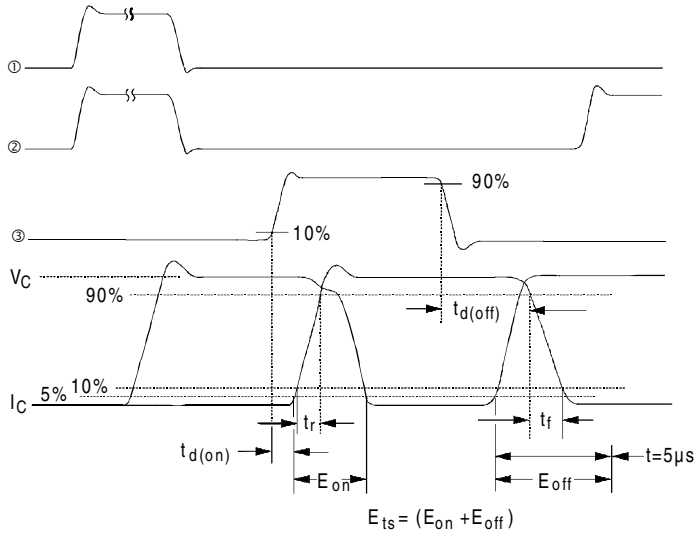
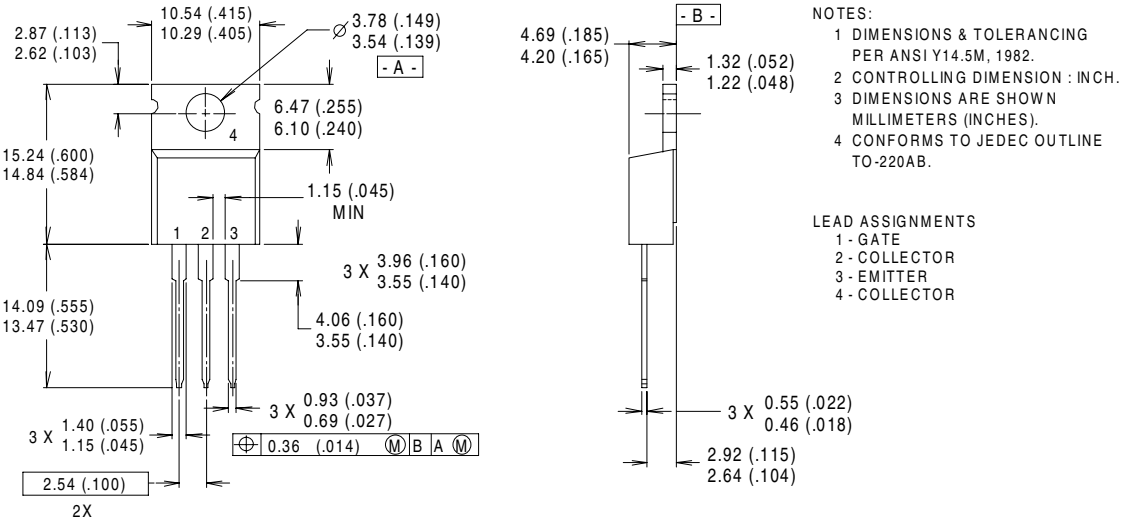


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD 91463B

International
IOR Rectifier

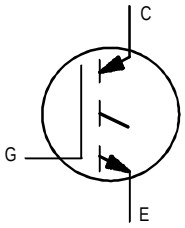
IRG4PC40F

INSULATED GATE BIPOLAR TRANSISTOR

Fast Speed IGBT

Features

- Fast: Optimized for medium operating frequencies (1-5 kHz in hard switching, >20 kHz in resonant mode).
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-247AC package



n-channel

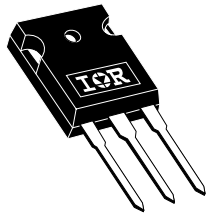
$V_{CES} = 600V$

$V_{CE(on)\ typ.} = 1.50V$

$@V_{GE} = 15V, I_C = 27A$

Benefits

- Generation 4 IGBT's offer highest efficiency available
- IGBT's optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	49	A
I_C @ T_C = 100°C	Continuous Collector Current	27	
I_{CM}	Pulsed Collector Current ①	200	
I_{LM}	Clamped Inductive Load Current ②	200	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	15	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	℃
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.77	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

12/30/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.70	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.50	1.7	V	I_C = 27A V_{GE} = 15V
		—	1.85	—		I_C = 49A See Fig.2, 5
		—	1.56	—		I_C = 27A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-12	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	9.2	12	—	S	V_{CE} = 100V, I_C = 27A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	100	150	nC	I_C = 27A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	15	23		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	35	53		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	26	—	ns	
t_r	Rise Time	—	18	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	240	360		I_C = 27A, V_{CC} = 480V
t_f	Fall Time	—	170	250		V_{GE} = 15V, R_G = 10Ω
E_{on}	Turn-On Switching Loss	—	0.37	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	1.81	—		See Fig. 10, 11, 13, 14
E_{ts}	Total Switching Loss	—	2.18	2.8		
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	T_J = 150°C,
t_r	Rise Time	—	21	—		I_C = 27A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	380	—		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	—	310	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	3.9	—	mJ	See Fig. 13, 14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	2200	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	140	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	29	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 10Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

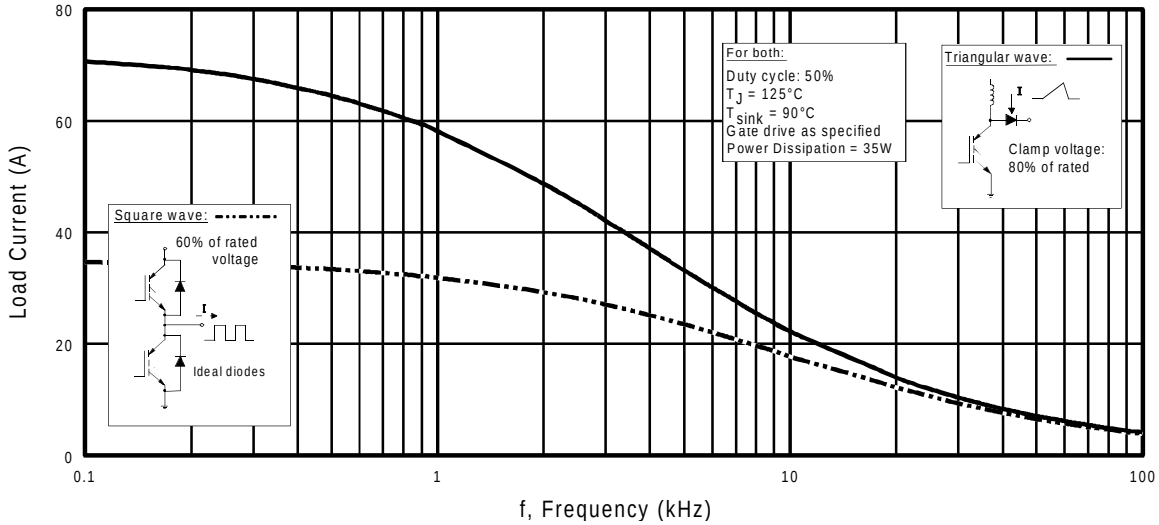


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

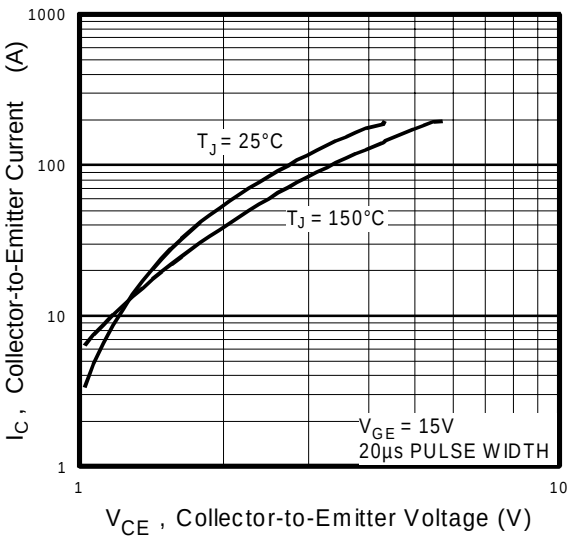


Fig. 2 - Typical Output Characteristics

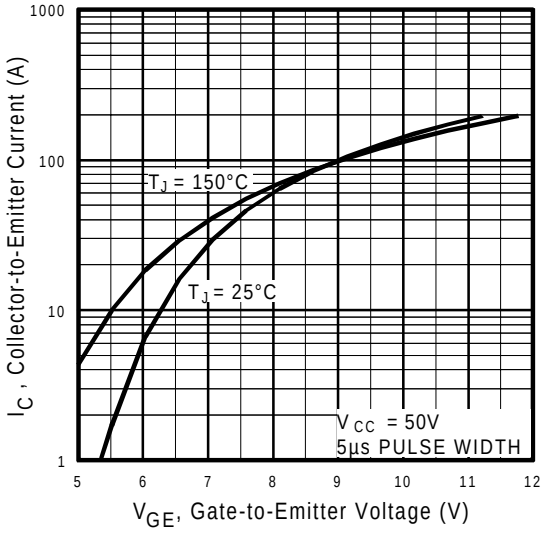


Fig. 3 - Typical Transfer Characteristics

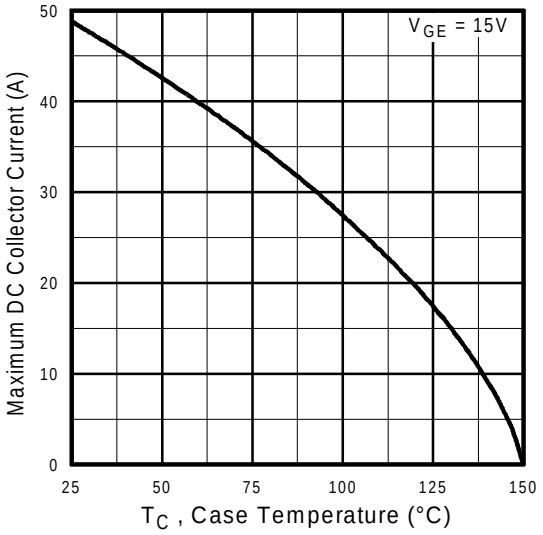


Fig. 4 - Maximum Collector Current vs. Case Temperature

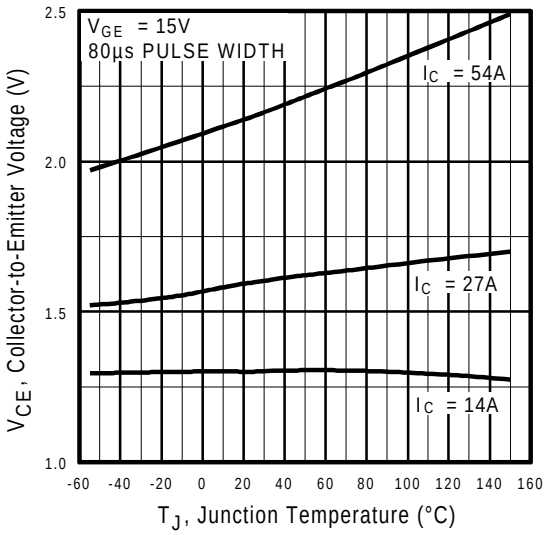


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

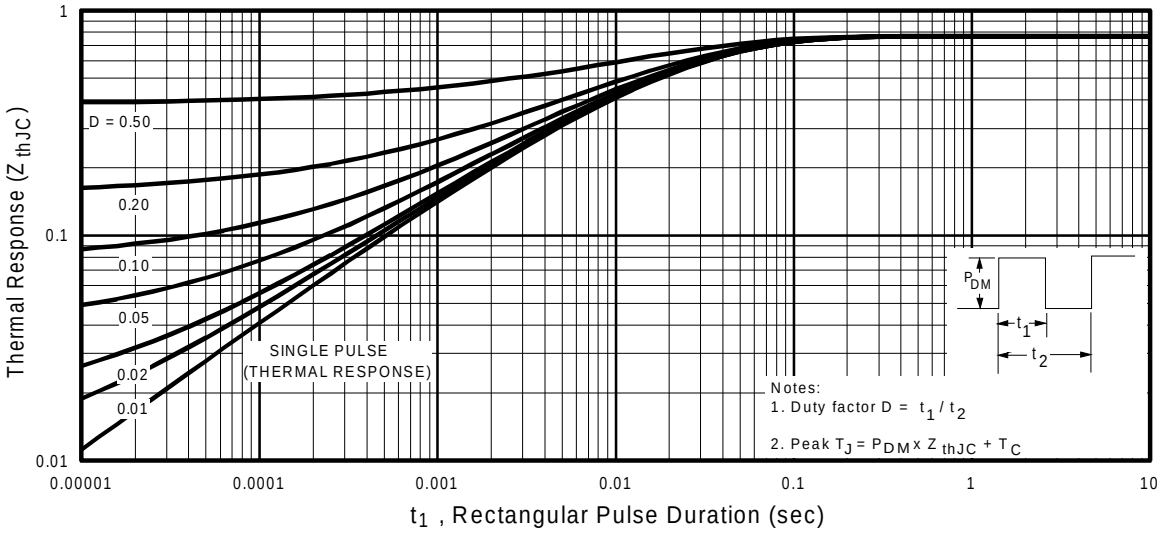


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

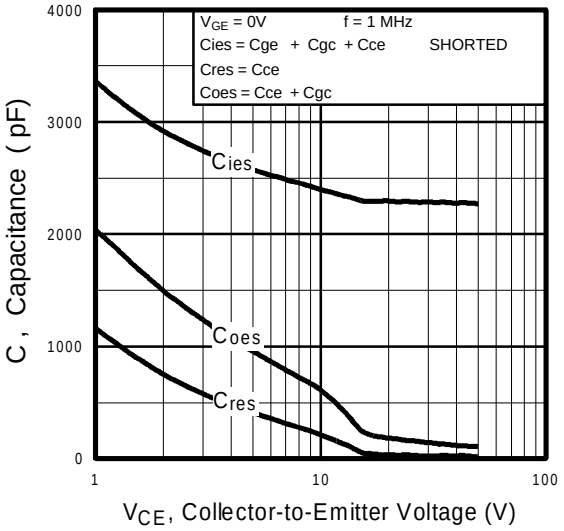


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

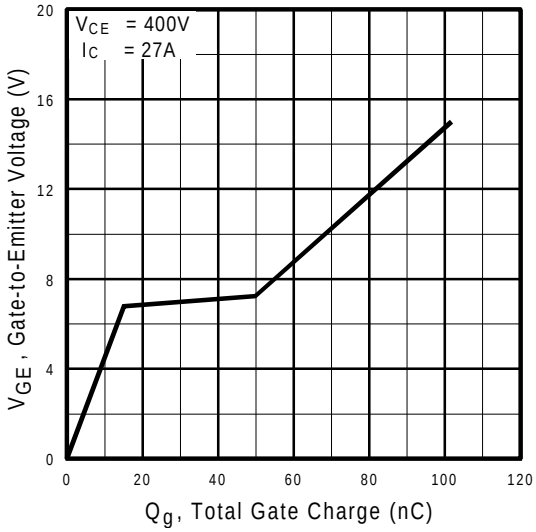


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

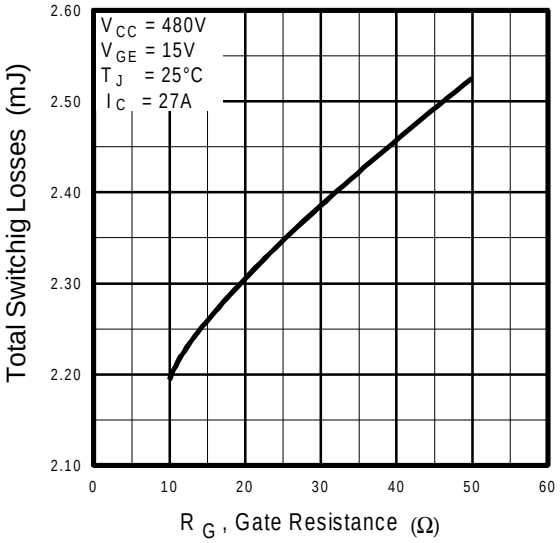


Fig. 9 - Typical Switching Losses vs. Gate Resistance

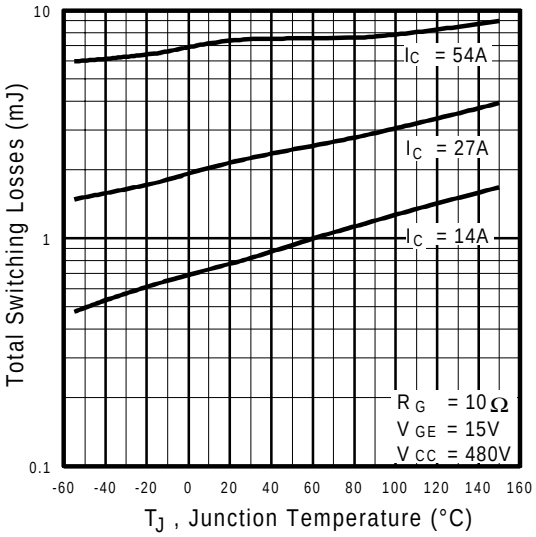


Fig. 10 - Typical Switching Losses vs. Junction Temperature

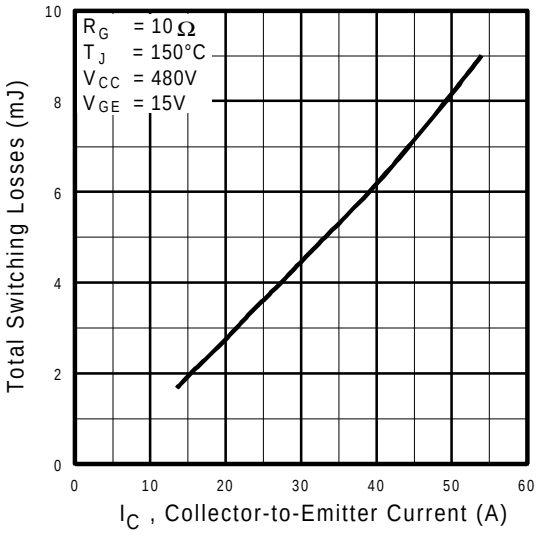


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

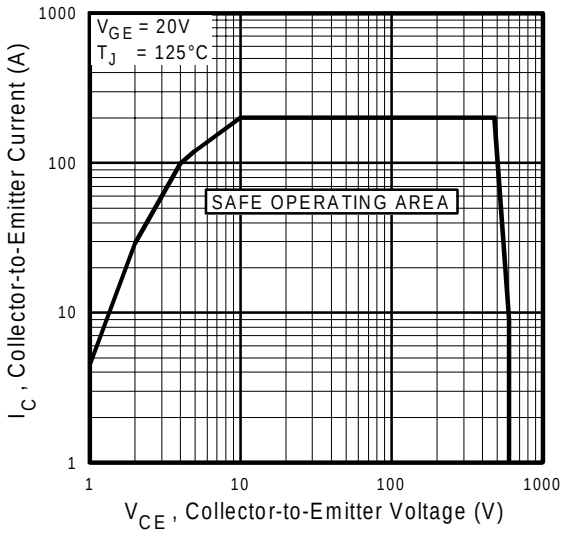


Fig. 12 - Turn-Off SOA

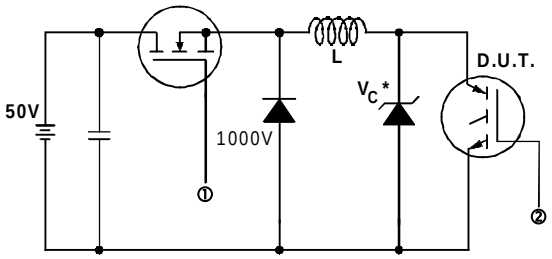


Fig. 13a - Clamped Inductive Load Test Circuit

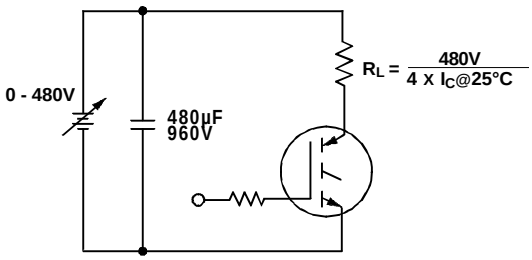


Fig. 13b - Pulsed Collector Current Test Circuit

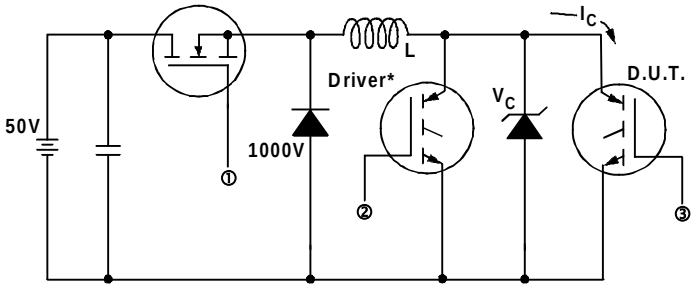


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

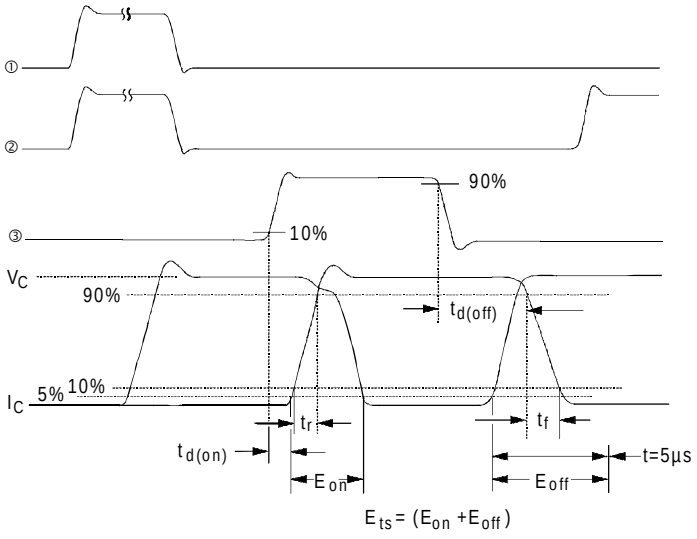
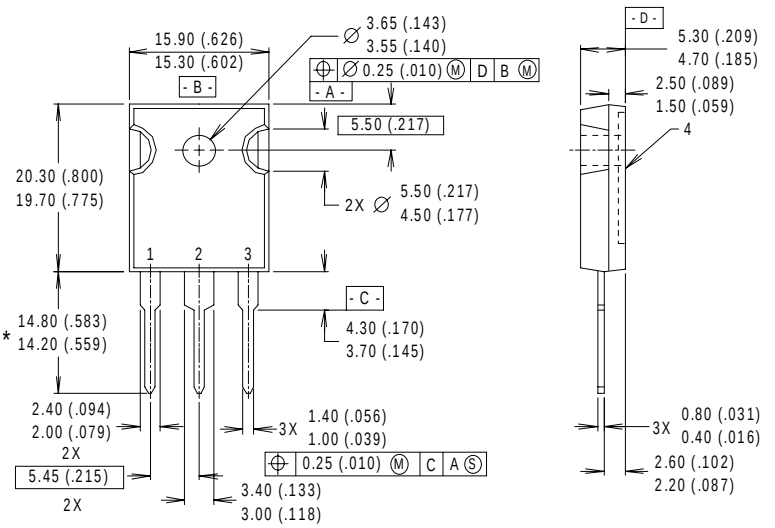


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
Data and specifications subject to change without notice. 12/00

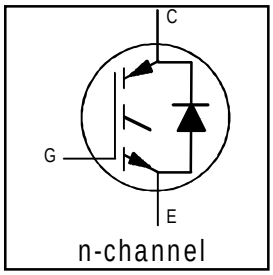
PD 91464B

International
IOR Rectifier

IRG4PC40FD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Fast CoPack IGBT



n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.50V

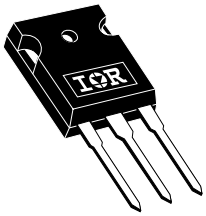
@V_{GE} = 15V, I_C = 27A

Features

- Fast: Optimized for medium operating frequencies (1-5 kHz in hard switching, >20 kHz in resonant mode).
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-247AC package

Benefits

- Generation -4 IGBT's offer highest efficiencies available
- IGBT's optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBT's . Minimized recovery characteristics require less/no snubbing
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	49	A
I_C @ T_C = 100°C	Continuous Collector Current	27	
I_{CM}	Pulsed Collector Current ①	200	
I_{LM}	Clamped Inductive Load Current ②	200	
I_F @ T_C = 100°C	Diode Continuous Forward Current	15	
I_{FM}	Diode Maximum Forward Current	200	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	------	------	0.77	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	------	------	1.7	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	------	0.24	------	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	-----	-----	40	
Wt	Weight	------	6 (0.21)	------	g (oz)

12/30/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	----	----	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	----	0.70	----	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	----	1.50	1.7	V	I_C = 27A V_{GE} = 15V
		----	1.85	----		I_C = 49A See Fig. 2, 5
		----	1.56	----		I_C = 27A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	----	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	----	-12	----	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	9.2	12	----	S	V_{CE} = 100V, I_C = 27A
I_{CES}	Zero Gate Voltage Collector Current	----	----	250	µA	V_{GE} = 0V, V_{CE} = 600V
		----	----	3500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	----	1.3	1.7	V	I_C = 15A See Fig. 13
		----	1.2	1.6		I_C = 15A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	----	----	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	----	100	150		I_C = 27A
Qge	Gate - Emitter Charge (turn-on)	----	15	23	nC	V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	----	35	53		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	----	63	----		T_J = 25°C
t_r	Rise Time	----	32	----	ns	I_C = 27A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	230	350		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	----	170	250		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	----	0.95	----		diode reverse recovery.
E_{off}	Turn-Off Switching Loss	----	2.01	----	mJ	See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	----	2.96	4.0		
$t_{d(on)}$	Turn-On Delay Time	----	63	----		T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	----	33	----	ns	I_C = 27A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	350	----		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	----	310	----		Energy losses include "tail" and
E_{ts}	Total Switching Loss	----	4.7	----	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	----	13	----	nH	Measured 5mm from package
C_{ies}	Input Capacitance	----	2200	----		V_{GE} = 0V
C_{oes}	Output Capacitance	----	140	----	pF	V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	----	29	----		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	----	42	60	ns	T_J = 25°C See Fig.
		----	74	120		T_J = 125°C 14 I_F = 15A
I_{rr}	Diode Peak Reverse Recovery Current	----	4.0	6.0	A	T_J = 25°C See Fig.
		----	6.5	10		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	----	80	180	nC	T_J = 25°C See Fig.
		----	220	600		T_J = 125°C 16 di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	----	188	----	A/µs	T_J = 25°C See Fig.
	During t_b	----	160	----		T_J = 125°C 17

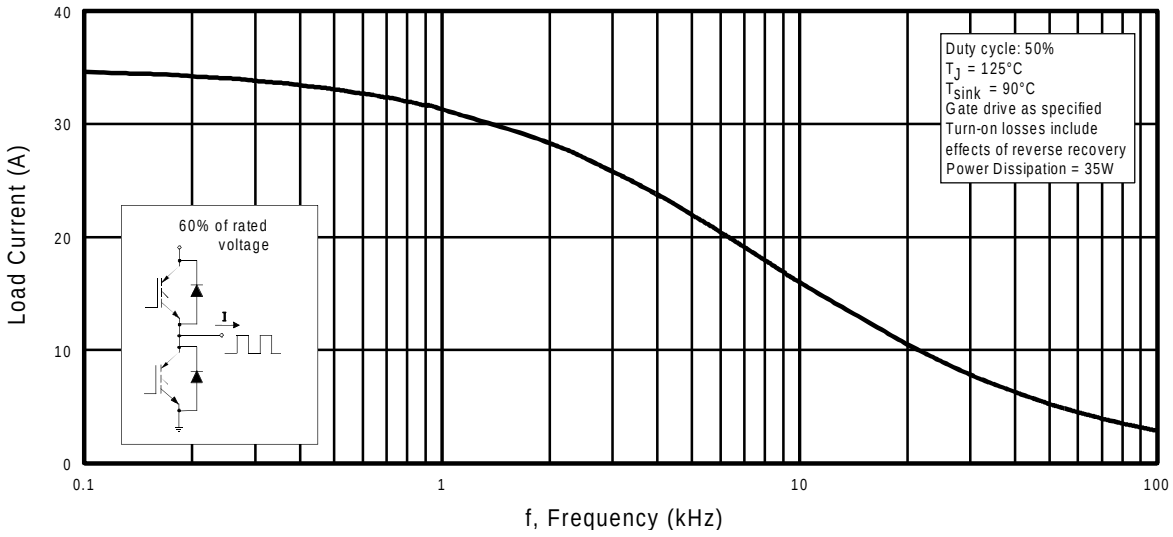


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

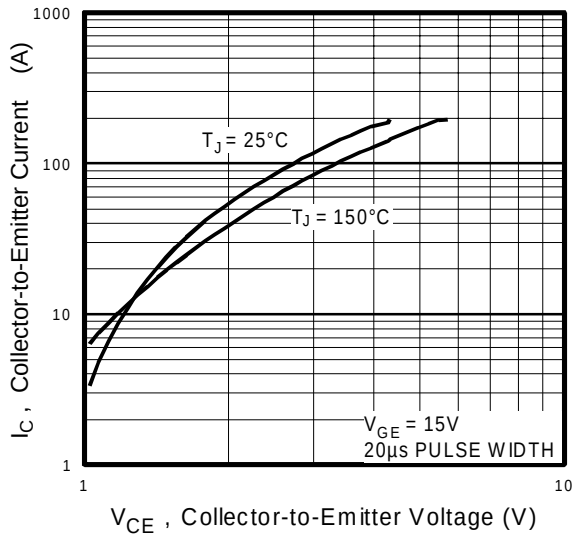


Fig. 2 - Typical Output Characteristics

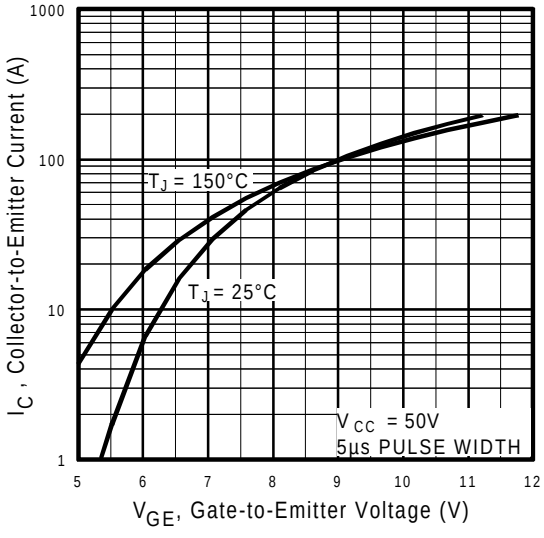


Fig. 3 - Typical Transfer Characteristics

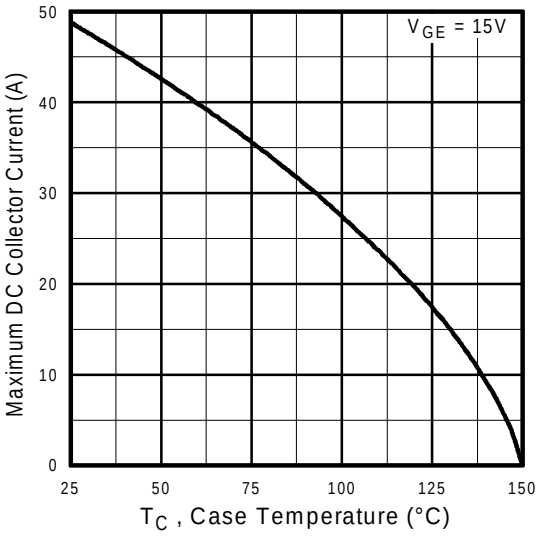


Fig. 4 - Maximum Collector Current vs. Case Temperature

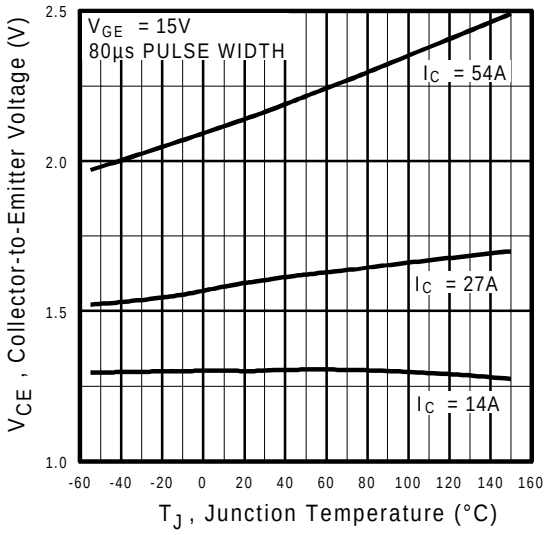


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

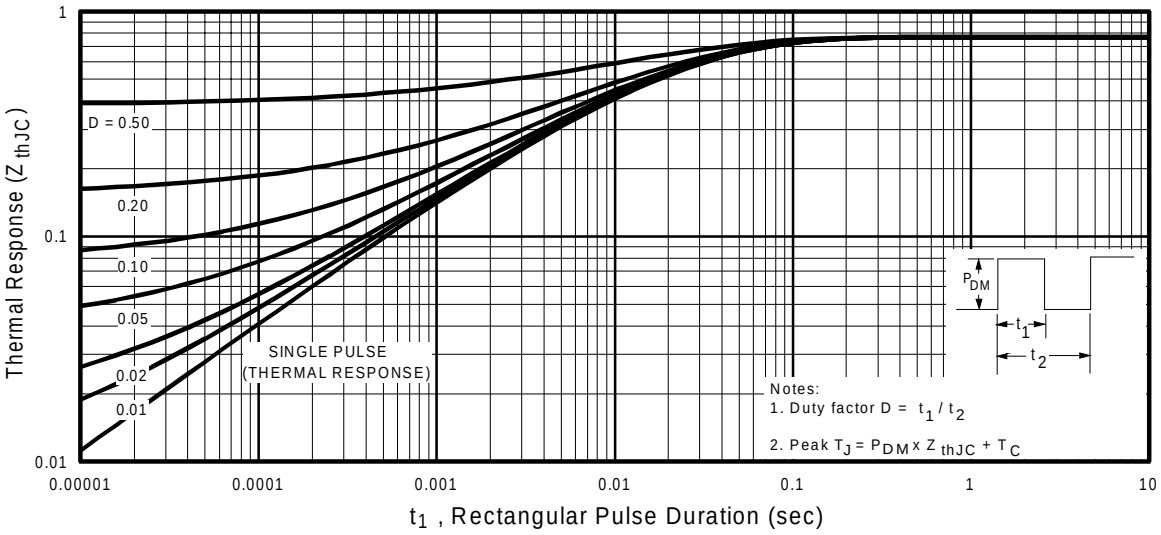


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

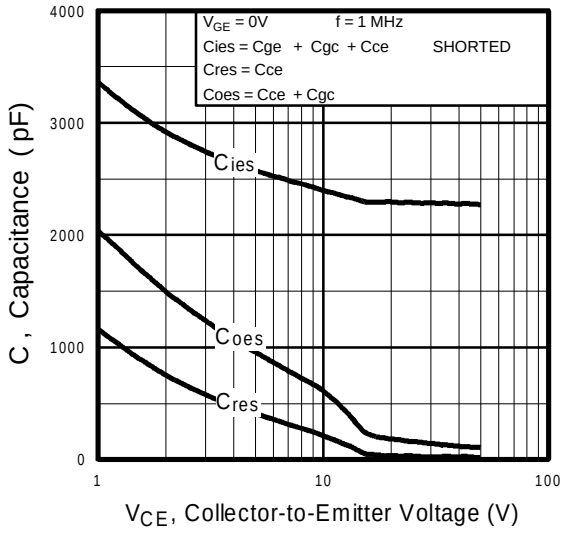


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

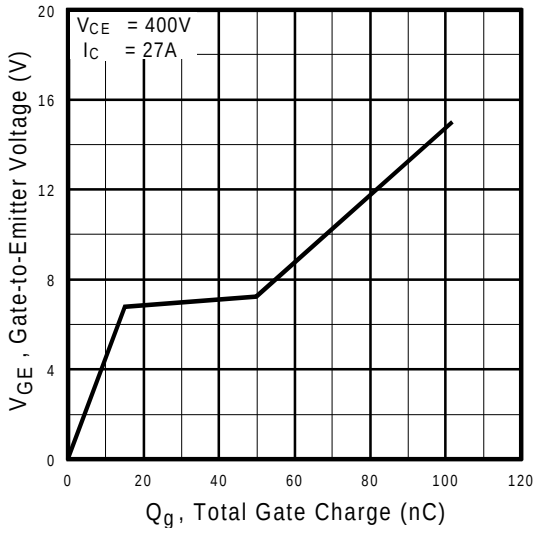


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

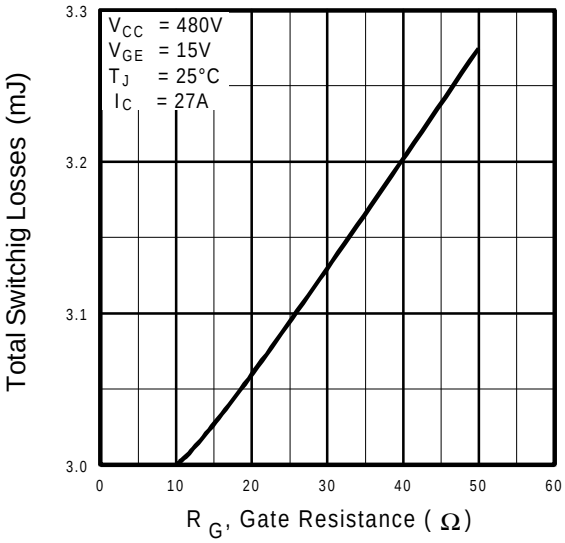


Fig. 9 - Typical Switching Losses vs. Gate Resistance

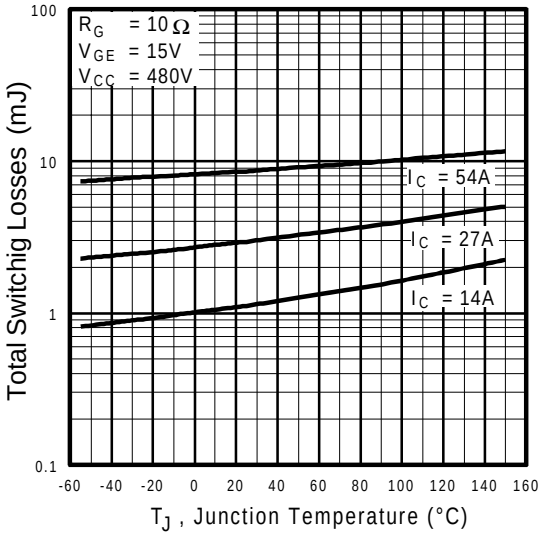


Fig. 10 - Typical Switching Losses vs. Junction Temperature

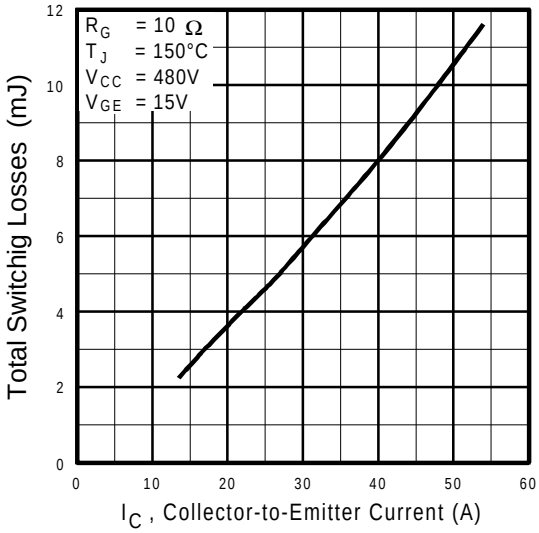


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

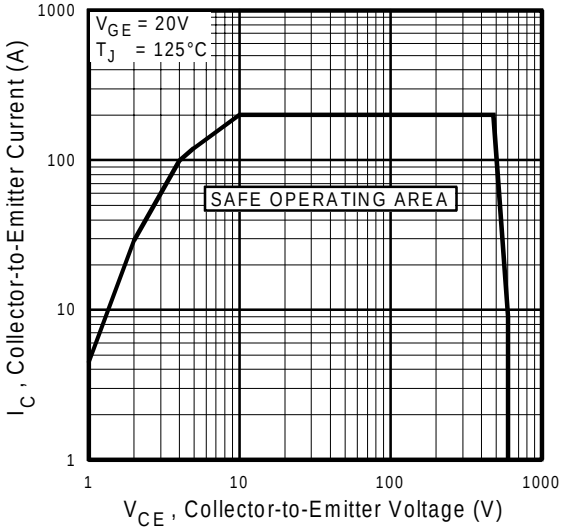


Fig. 12 - Turn-Off SOA

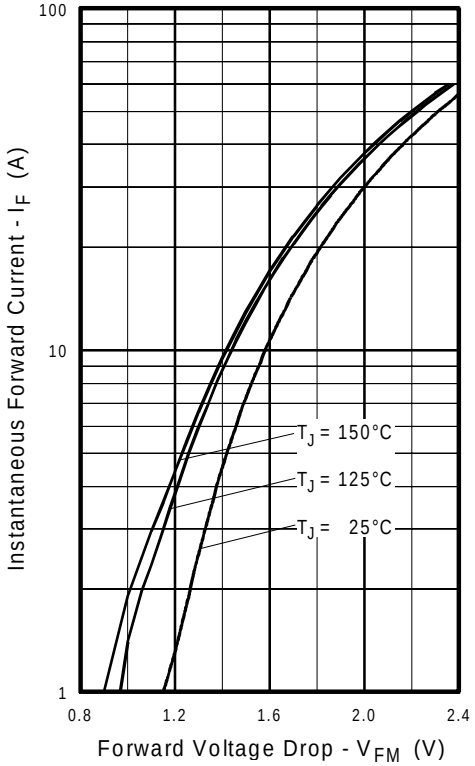


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

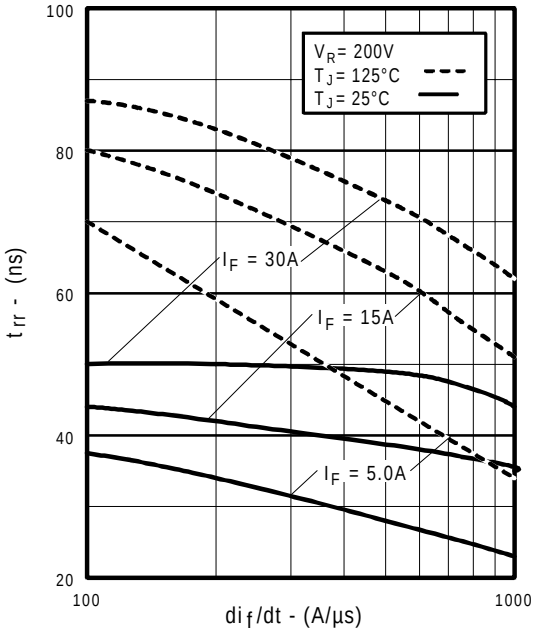


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

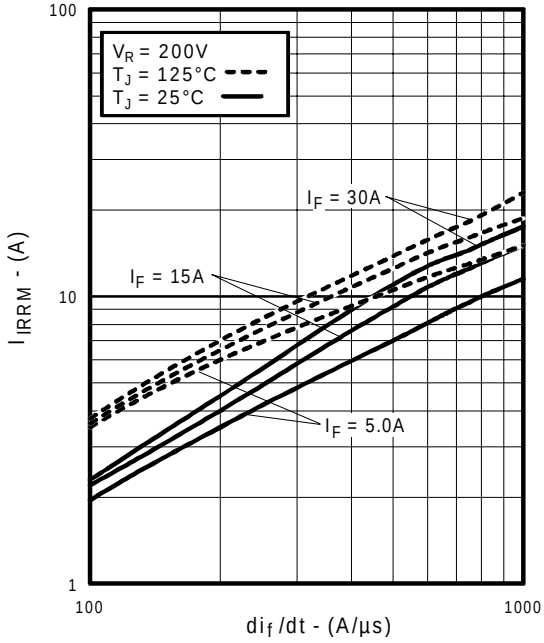


Fig. 15 - Typical Recovery Current vs. di_f/dt

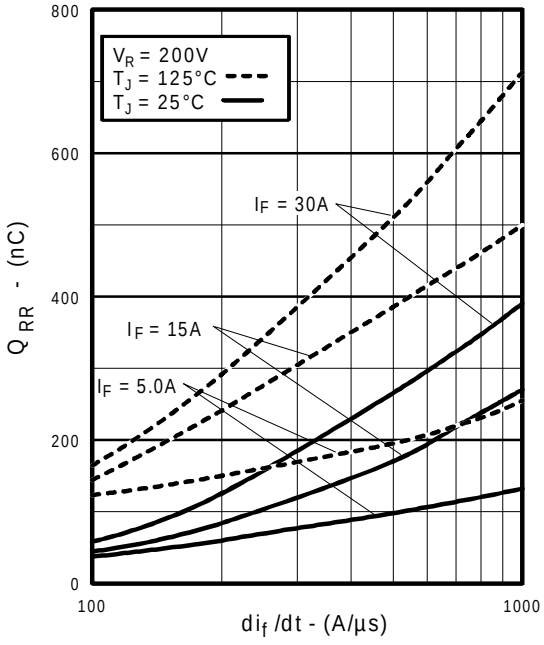


Fig. 16 - Typical Stored Charge vs. di_f/dt

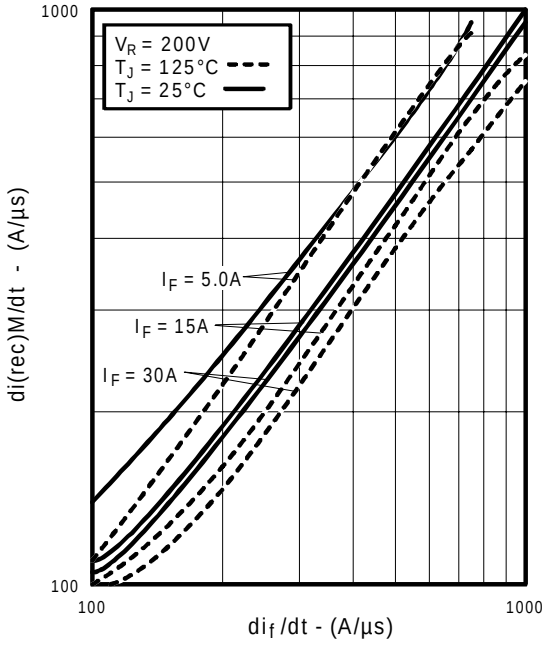


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

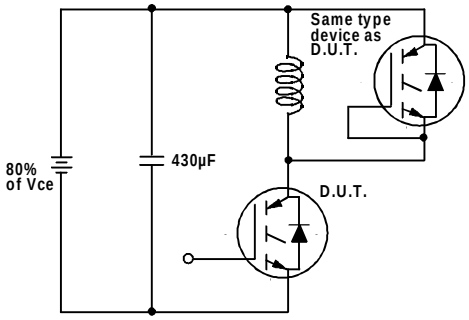


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

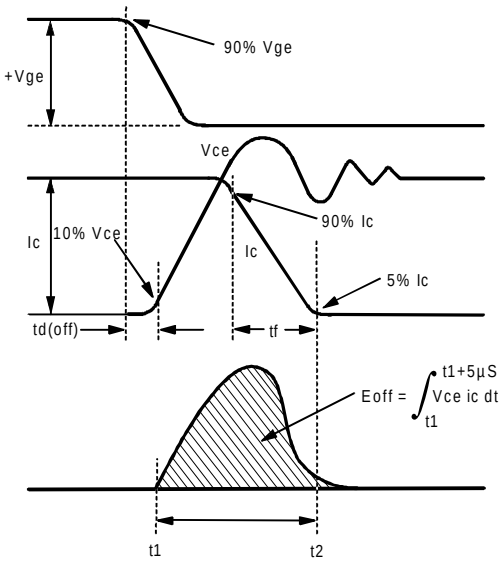


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

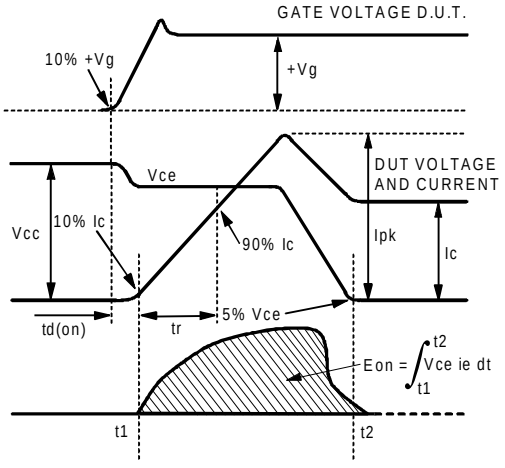


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

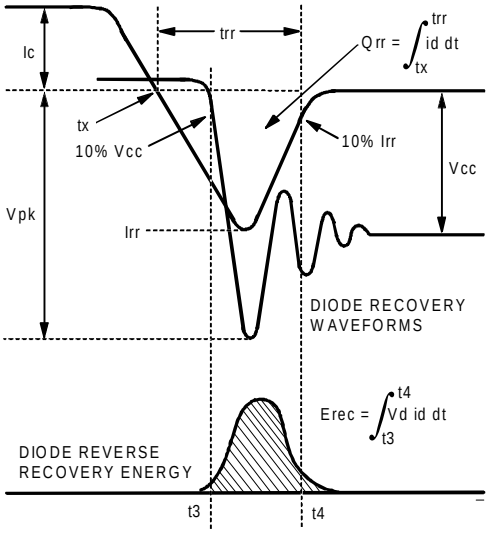


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

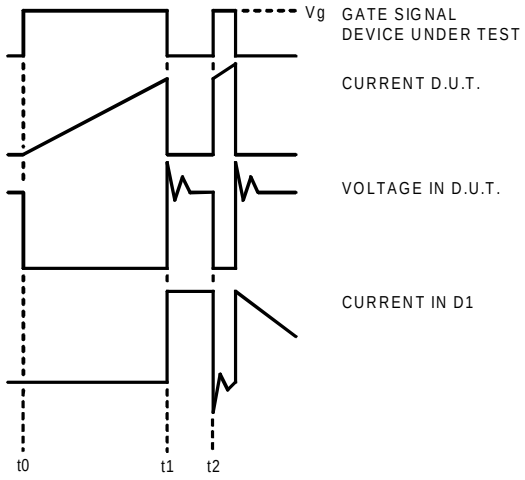


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

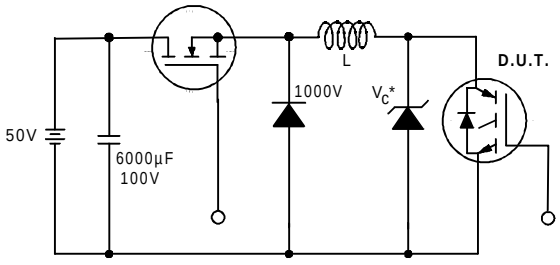


Figure 19. Clamped Inductive Load Test Circuit

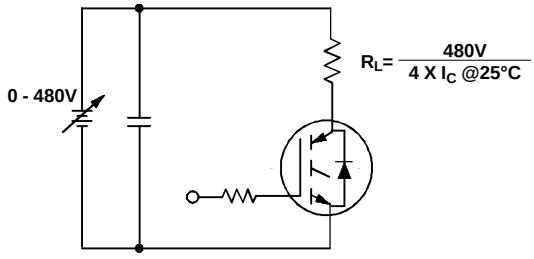


Figure 20. Pulsed Collector Current Test Circuit

Notes:

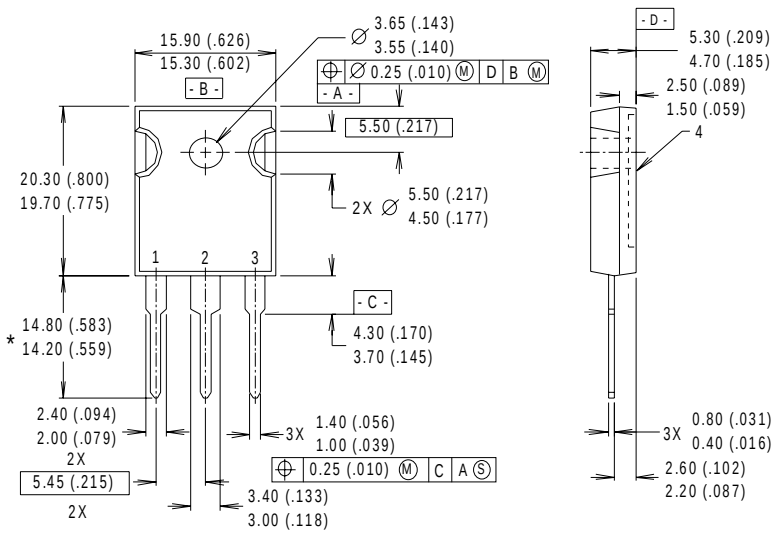
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 10Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
Data and specifications subject to change without notice. 12/00

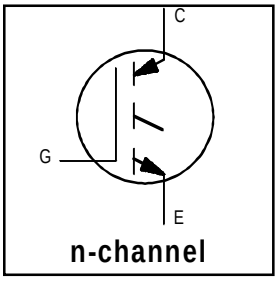
International
IOR Rectifier

PD - 91583B

IRG4PC50K

Short Circuit Rated
UltraFast IGBT

INSULATED GATE BIPOLAR TRANSISTOR



n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.84V

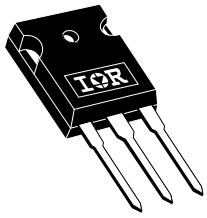
@V_{GE} = 15V, I_C = 30A

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, @360V V_{CE} (start), T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Latest generation design provides tighter parameter distribution and higher efficiency than previous generations

Benefits

- As a Freewheeling Diode we recommend our HEXFRED™ ultrafast, ultrasoft recovery diodes for minimum EMI / Noise and switching losses in the Diode and IGBT
- Latest generation 4 IGBTs offer highest power density motor controls possible
- This part replaces the IRGPC50K and IRGPC50M devices


TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	52	A
I_C @ T_C = 100°C	Continuous Collector Current	30	
I_{CM}	Pulsed Collector Current ①	104	
I_{LM}	Clamped Inductive Load Current ②	104	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	170	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.64	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

4/15/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.47	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.84	2.2	V	I_C = 30A V_{GE} = 15V
		—	2.19	—		I_C = 52A See Fig.2, 5
		—	1.79	—		I_C = 30A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-12	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	17	24	—	S	V_{CE} = 100 V, I_C = 30A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	5000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	200	300	nC	I_C = 30A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	25	38		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	85	130		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	38	—	ns	
t_r	Rise Time	—	34	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	160	240		I_C = 30A, V_{CC} = 480V
t_f	Fall Time	—	79	120		V_{GE} = 15V, R_G = 5.0Ω
E_{on}	Turn-On Switching Loss	—	0.49	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.68	—		See Fig. 9,10,14
E_{ts}	Total Switching Loss	—	1.12	1.4		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 400V, T_J = 125°C
						V_{GE} = 15V, R_G = 10Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	37	—	ns	T_J = 150°C,
t_r	Rise Time	—	35	—		I_C = 30A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	260	—		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	170	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	2.34	—	mJ	See Fig. 11,14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	3200	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	370	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	95	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 5.0Ω

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

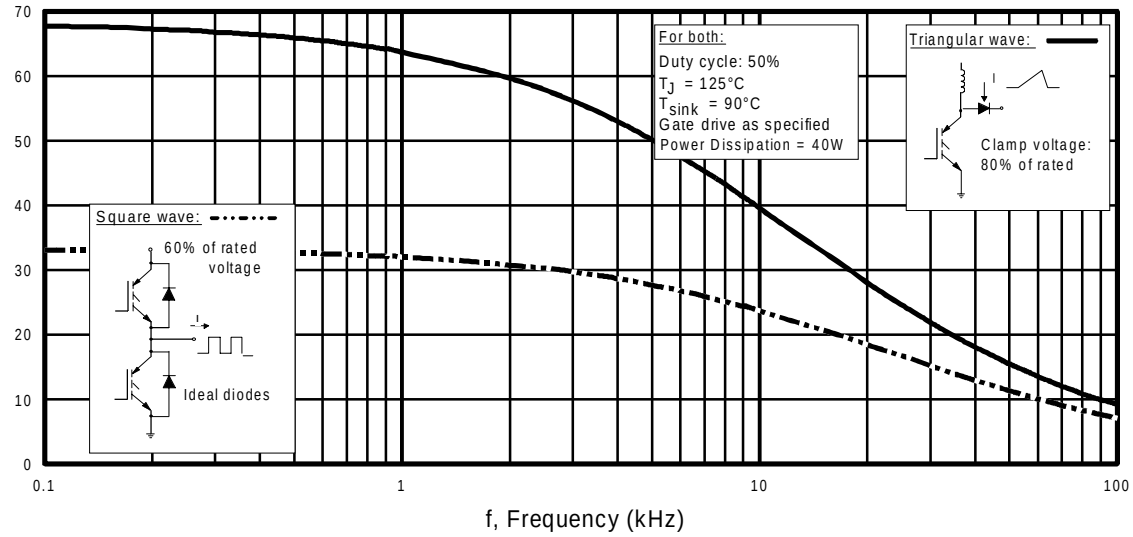


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

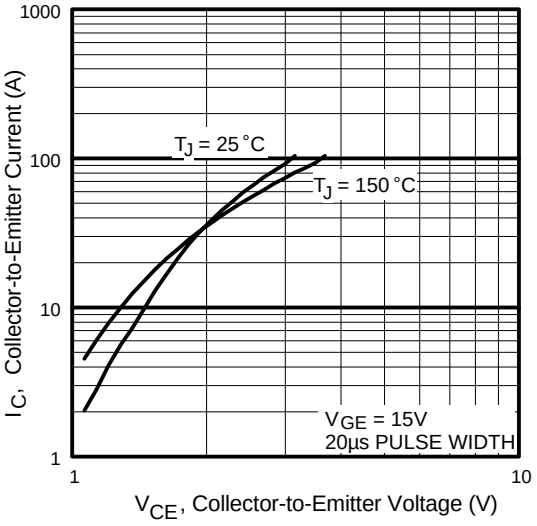


Fig. 2 - Typical Output Characteristics

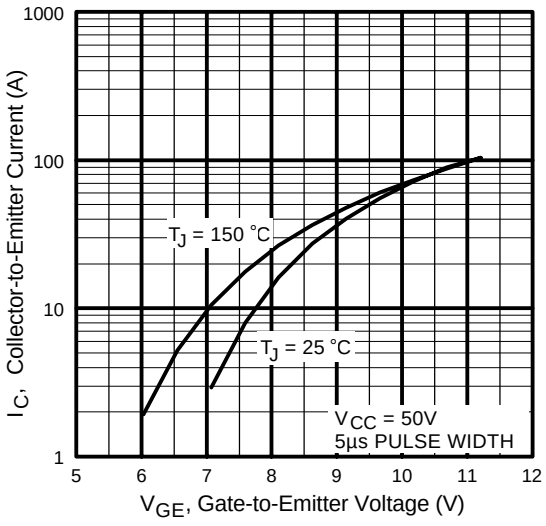


Fig. 3 - Typical Transfer Characteristics

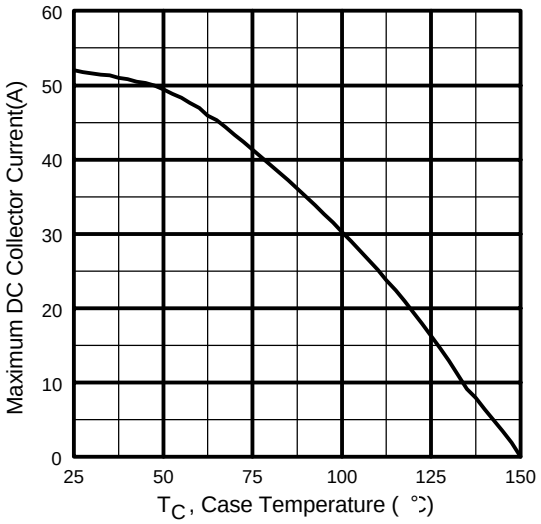


Fig. 4 - Maximum Collector Current vs. Case Temperature

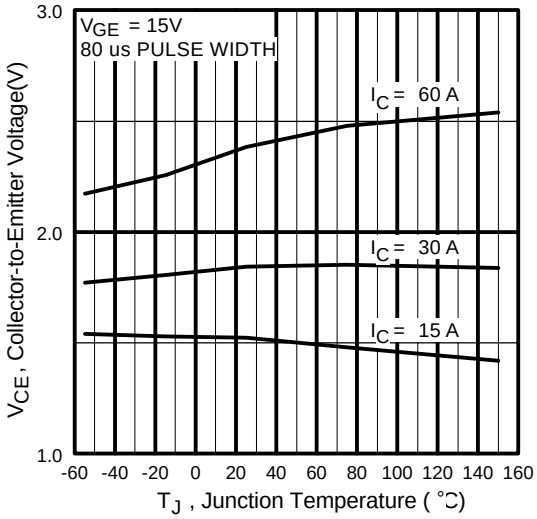


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

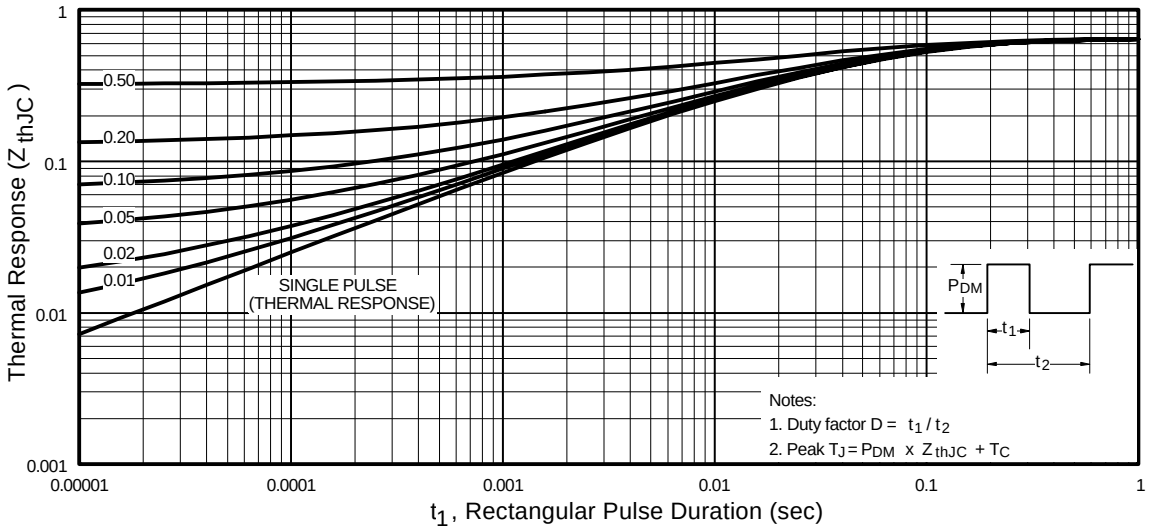


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

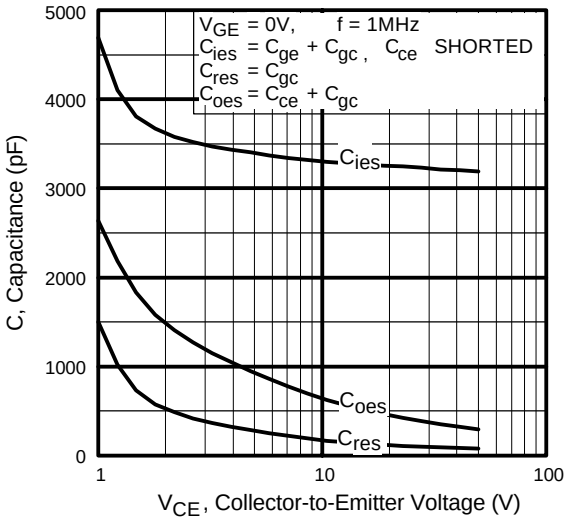


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

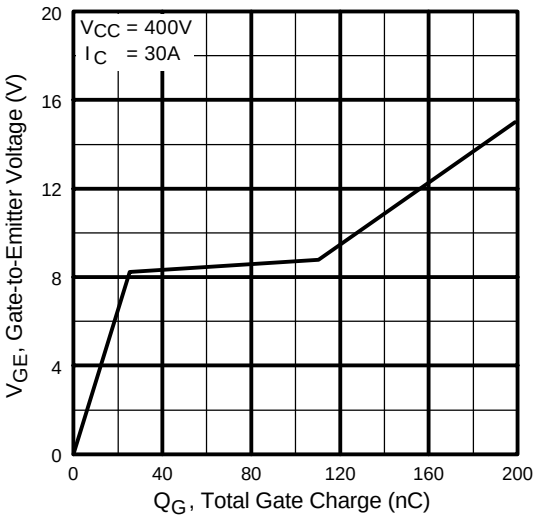


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

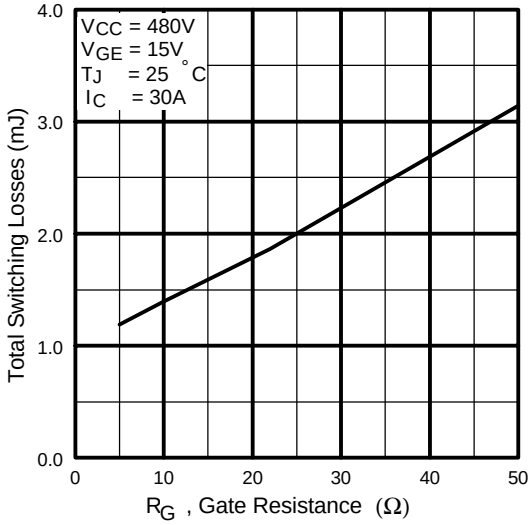


Fig. 9 - Typical Switching Losses vs. Gate Resistance

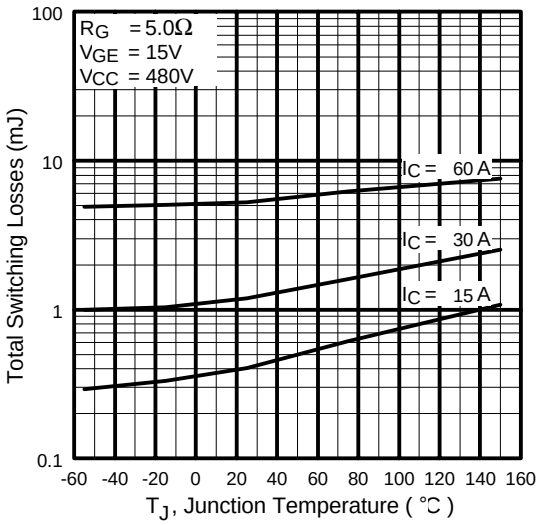


Fig. 10 - Typical Switching Losses vs. Junction Temperature

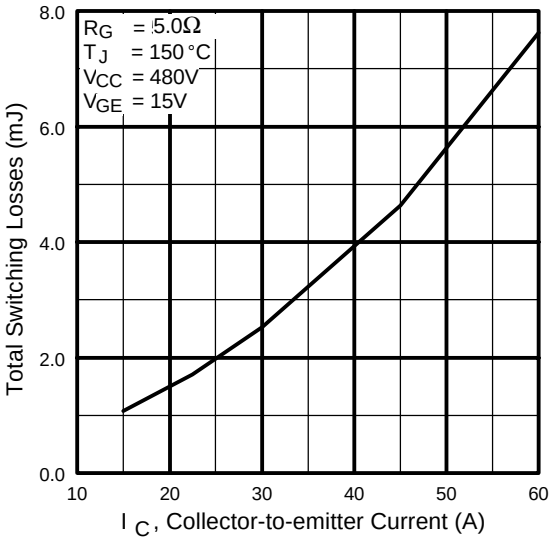


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

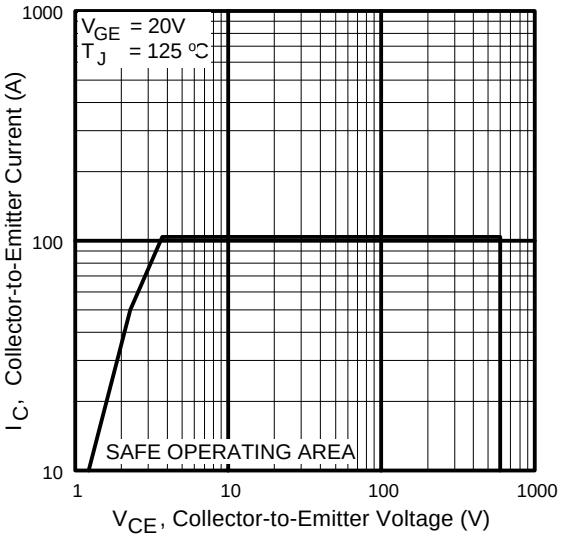


Fig. 12 - Turn-Off SOA

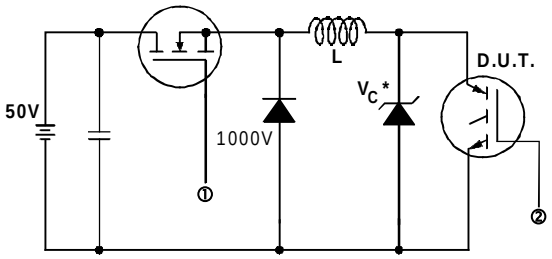


Fig. 13a - Clamped Inductive Load Test Circuit

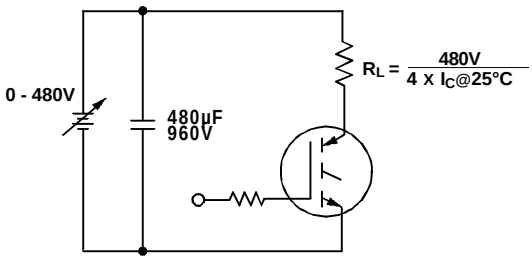


Fig. 13b - Pulsed Collector Current Test Circuit

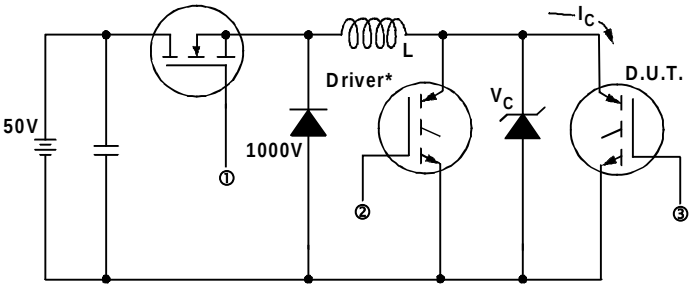


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

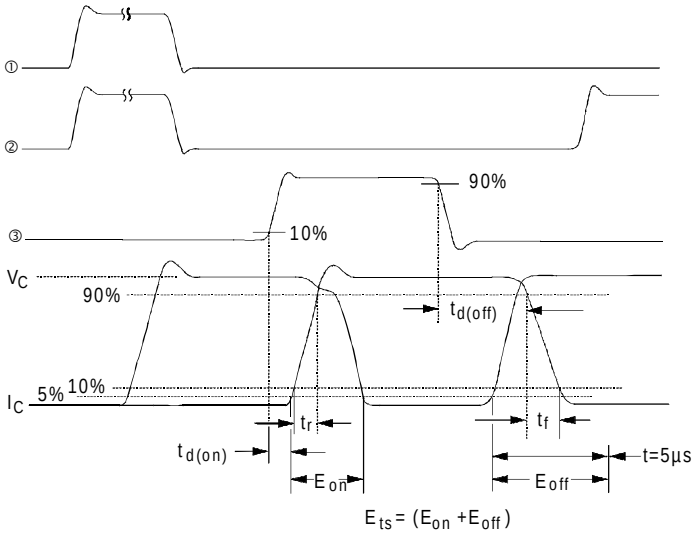
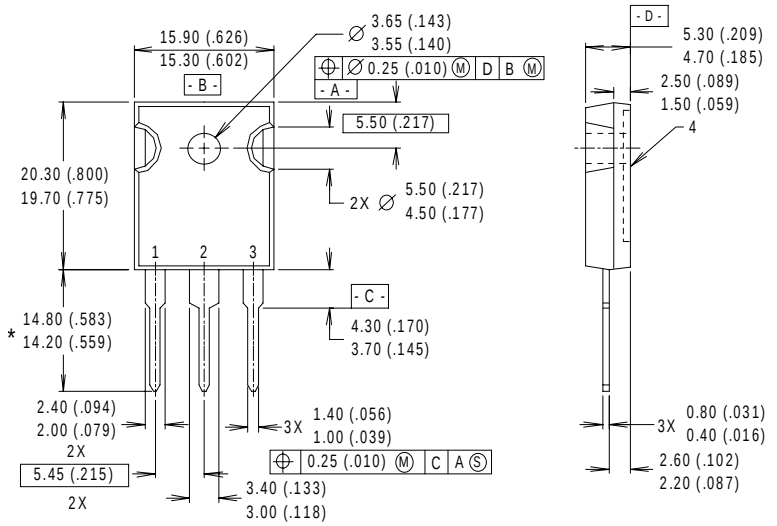


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

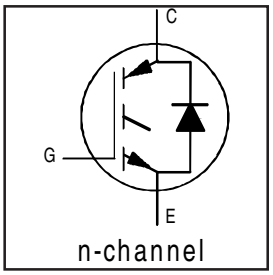
PD- 91575B

International
IOR Rectifier

IRG4PH50KD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
UltraFast IGBT



n-channel

V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.77V

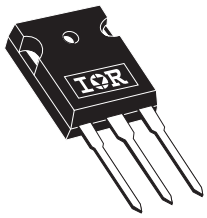
@V_{GE} = 15V, I_C = 24A

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, V_{CC} = 720V , T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Tighter parameter distribution and higher efficiency than previous generations
- IGBT co-packaged with HEXFRED™ ultrafast, ultrasoft recovery antiparallel diodes

Benefits

- Latest generation 4 IGBT's offer highest power density motor controls possible
- HEXFRED™ diodes optimized for performance with IGBTs. Minimized recovery characteristics reduce noise, EMI and switching losses
- This part replaces the IRGPH50KD2 and IRGPH50MD2 products
- For hints see design tip 97003



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	45	A
I_C @ T_C = 100°C	Continuous Collector Current	24	
I_{CM}	Pulsed Collector Current ①	90	
I_{LM}	Clamped Inductive Load Current ②	90	
I_F @ T_C = 100°C	Diode Continuous Forward Current	16	
I_{FM}	Diode Maximum Forward Current	90	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	——	——	0.64	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	——	——	0.83	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	——	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	——	40	
Wt	Weight	——	6 (0.21)	——	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.91	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.77	3.5	V	I_C = 24A V_{GE} = 15V
		—	3.28	—		I_C = 45A See Fig. 2, 5
		—	2.54	—		I_C = 24A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	13	19	—	S	V_{CE} = 100V, I_C = 24A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	6500		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	2.5	3.5	V	I_C = 16A See Fig. 13
		—	2.1	3.0		I_C = 16A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	180	270	nC	I_C = 24A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	25	38		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	70	110		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	87	—	ns	
t_r	Rise Time	—	100	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	140	300		I_C = 24A, V_{CC} = 800V
t_f	Fall Time	—	200	300		V_{GE} = 15V, R_G = 5.0Ω
E_{on}	Turn-On Switching Loss	—	3.83	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	1.90	—		and diode reverse recovery
E_{ts}	Total Switching Loss	—	5.73	7.9		See Fig. 9,10,18
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 720V, T_J = 125°C
						V_{GE} = 15V, R_G = 5.0Ω
$t_{d(on)}$	Turn-On Delay Time	—	67	—	ns	T_J = 150°C, See Fig. 10,11,18
t_r	Rise Time	—	72	—		I_C = 24A, V_{CC} = 800V
$t_{d(off)}$	Turn-Off Delay Time	—	310	—		V_{GE} = 15V, R_G = 5.0Ω,
t_f	Fall Time	—	390	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	8.36	—	mJ	and diode reverse recovery
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	2800	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	140	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	53	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	90	135	ns	T_J = 25°C See Fig.
		—	164	245		T_J = 125°C 14 I_F = 16A
I_{rr}	Diode Peak Reverse Recovery Current	—	5.8	10	A	T_J = 25°C See Fig.
		—	8.3	15		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	260	675	nC	T_J = 25°C See Fig.
		—	680	1838		T_J = 125°C 16 di/dt = 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	120	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	76	—		T_J = 125°C 17

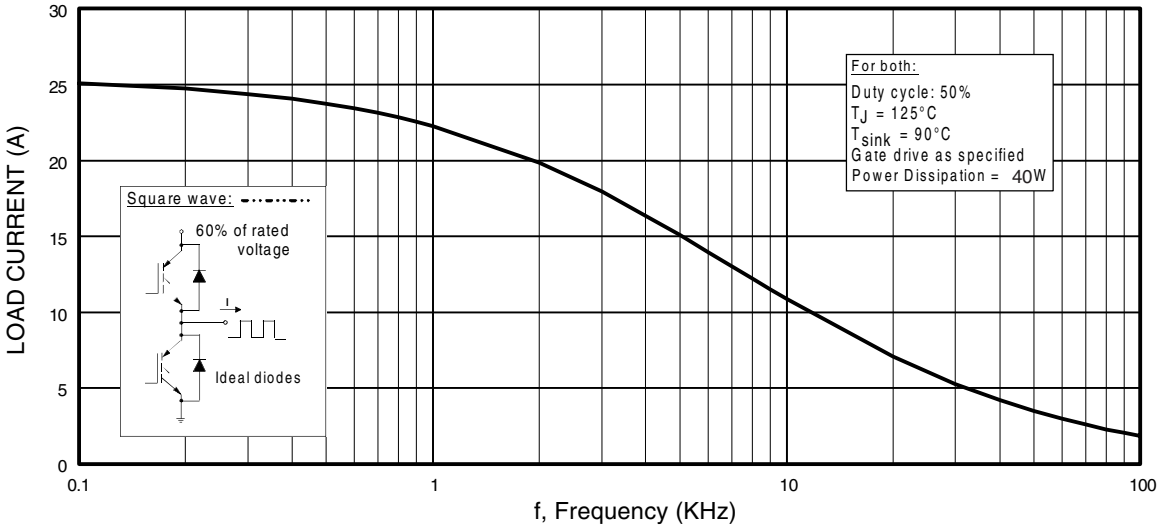


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

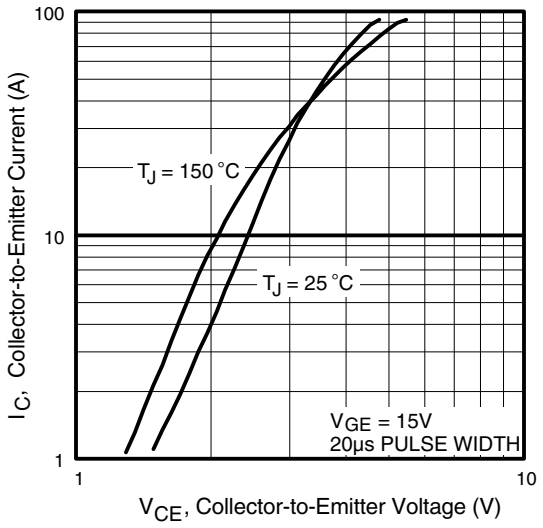


Fig. 2 - Typical Output Characteristics

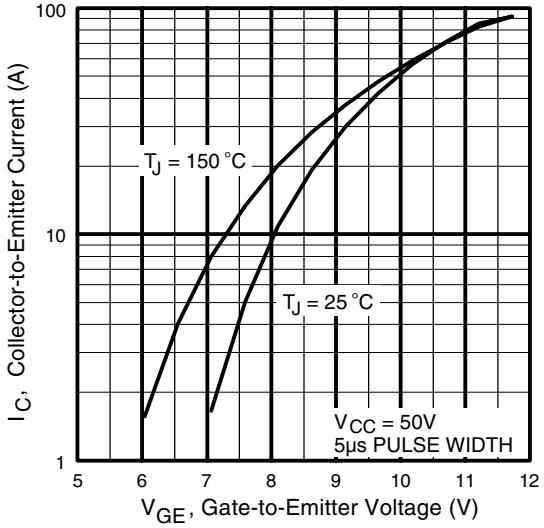


Fig. 3 - Typical Transfer Characteristics

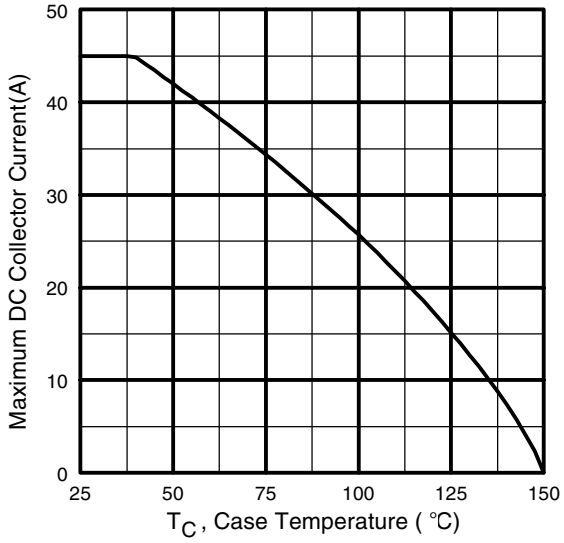


Fig. 4 - Maximum Collector Current vs. Case Temperature

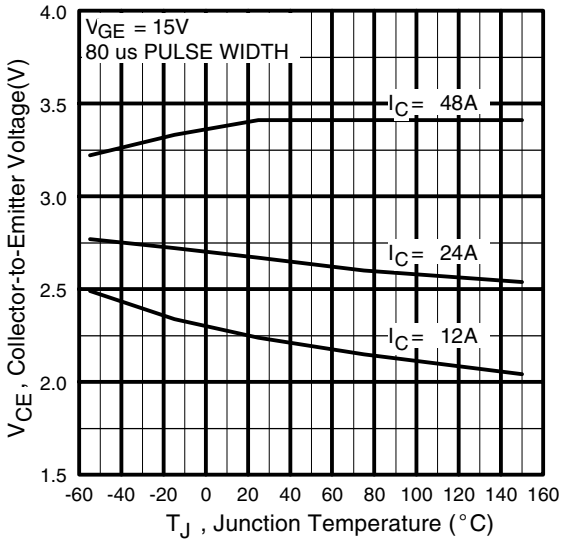


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

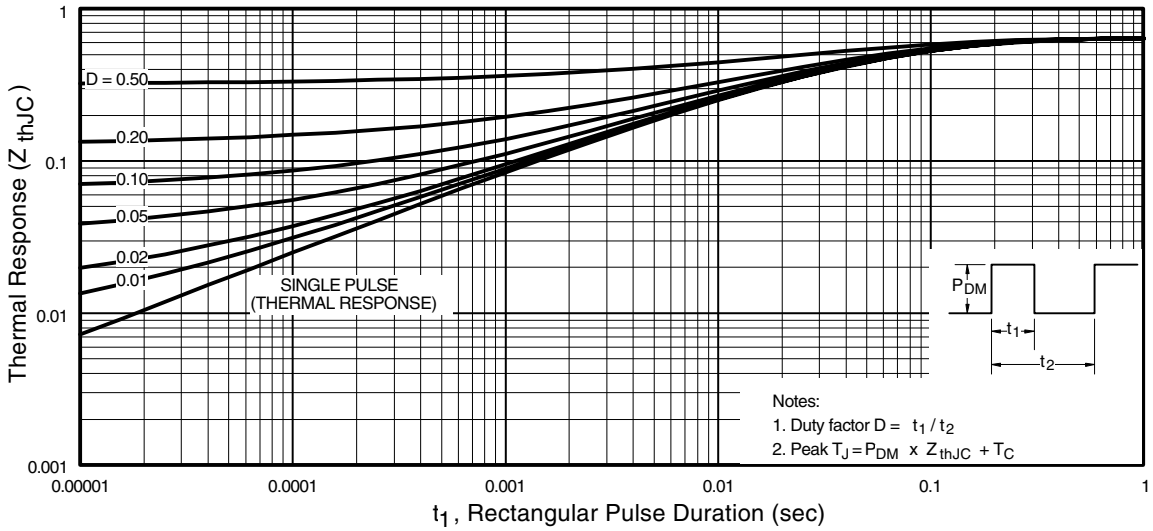


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

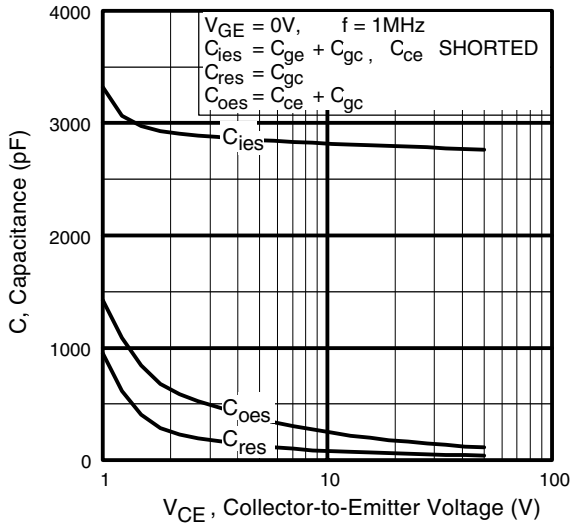


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

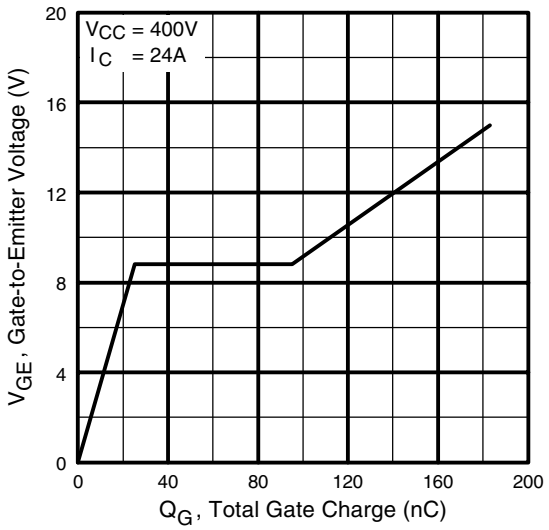


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

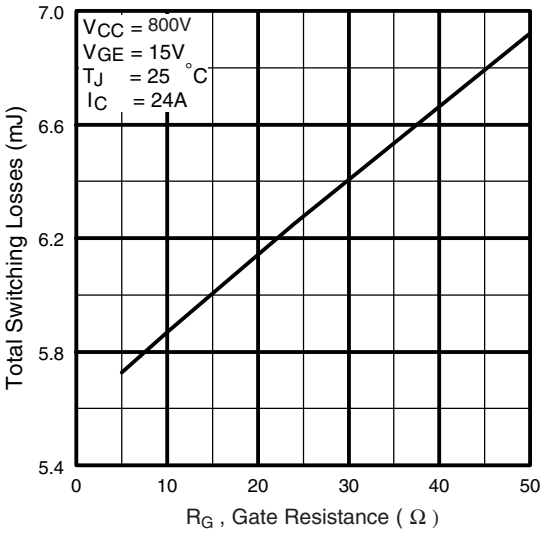


Fig. 9 - Typical Switching Losses vs. Gate Resistance

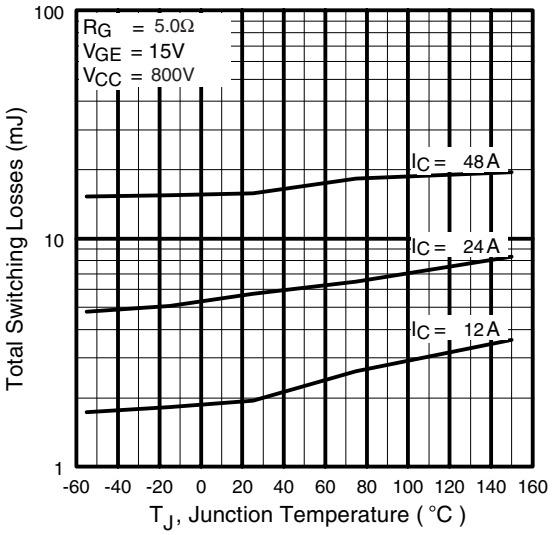


Fig. 10 - Typical Switching Losses vs. Junction Temperature

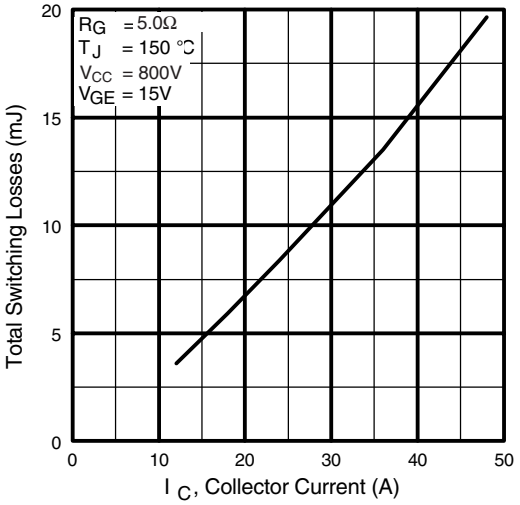


Fig. 11 - Typical Switching Losses vs. Collector Current

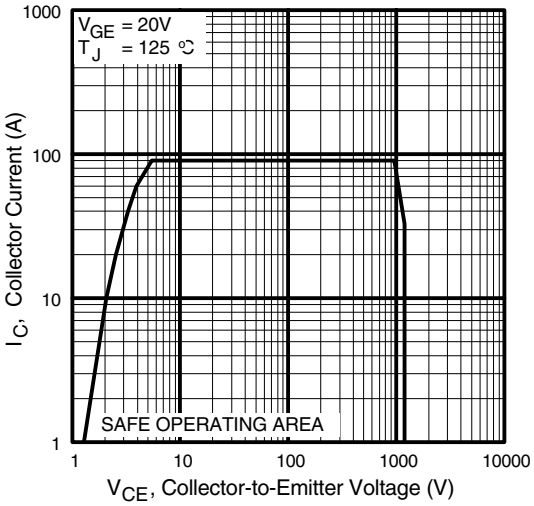


Fig. 12 - Turn-Off SOA

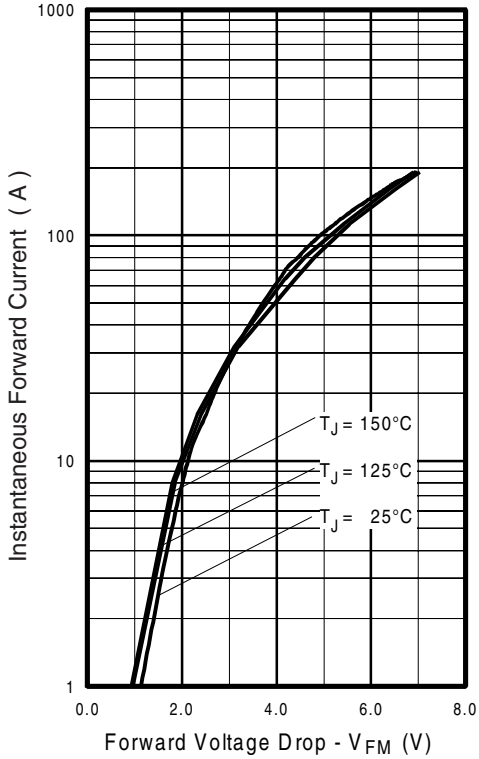


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

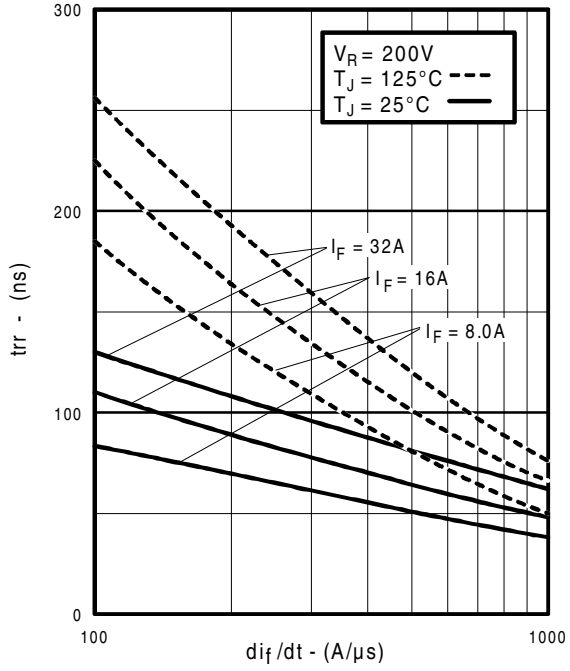


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

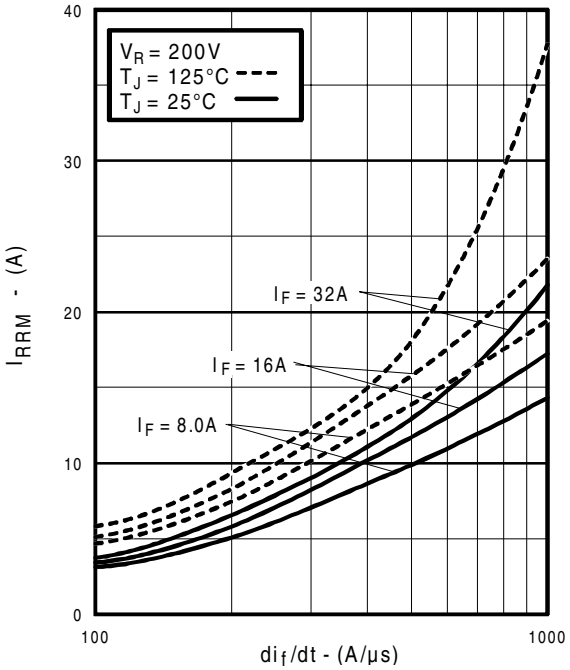


Fig. 15 - Typical Recovery Current vs. di_f/dt

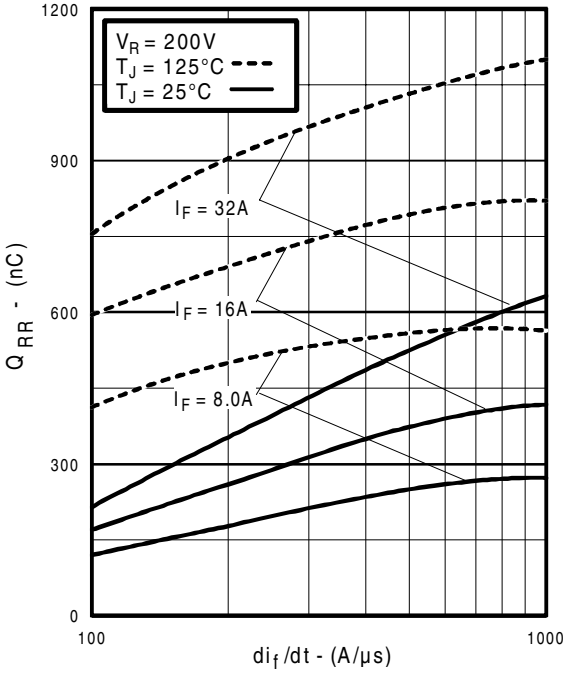


Fig. 16 - Typical Stored Charge vs. di_f/dt

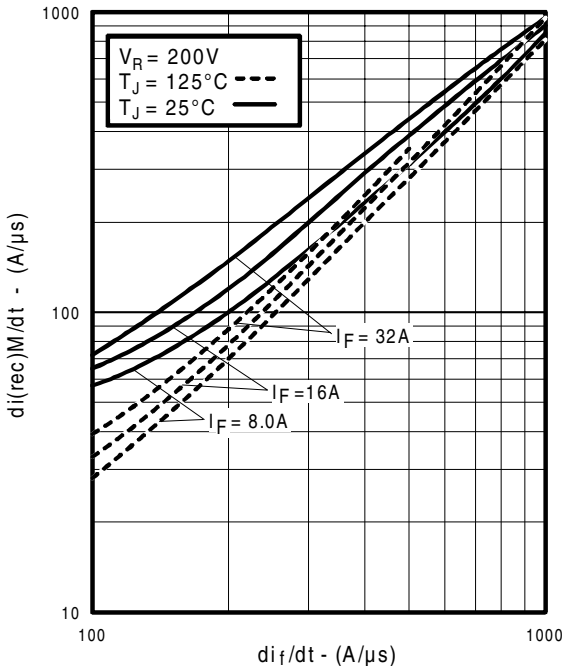


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

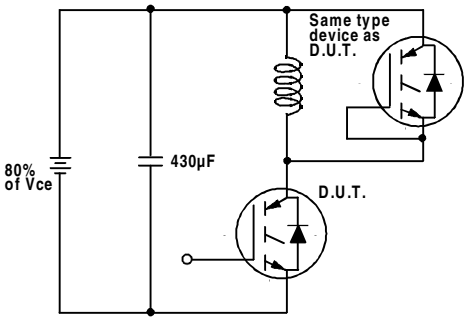


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

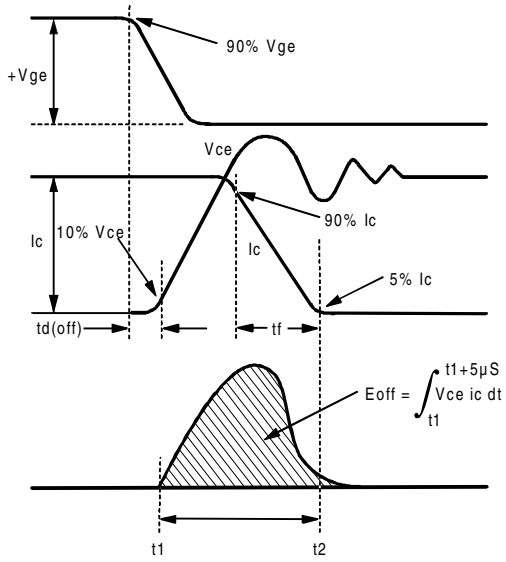


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

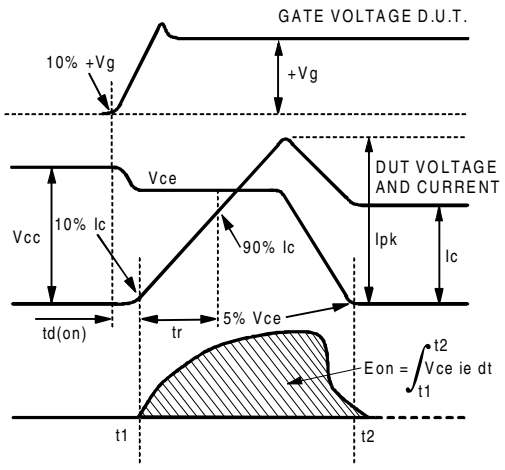


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

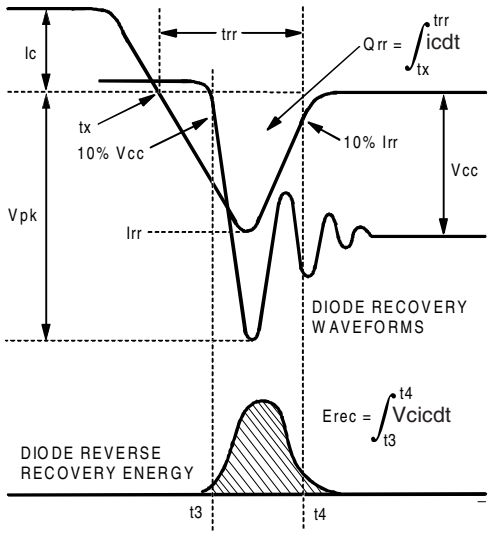


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

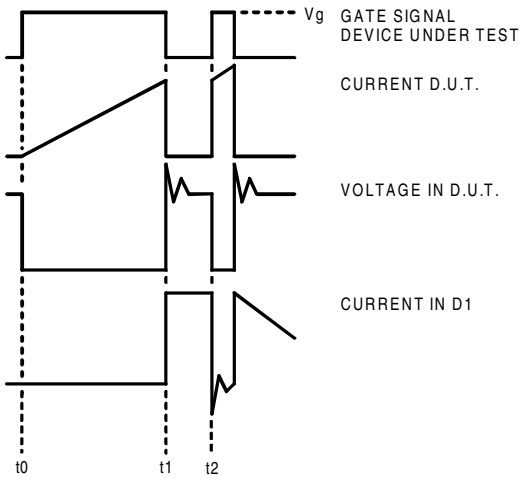


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

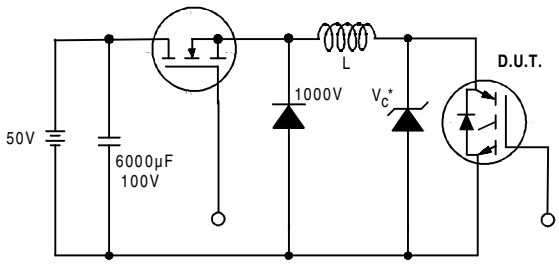


Figure 19. Clamped Inductive Load Test Circuit

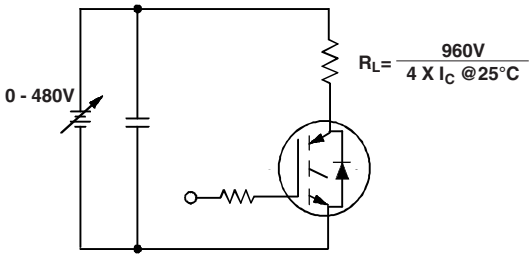


Figure 20. Pulsed Collector Current Test Circuit

Notes:

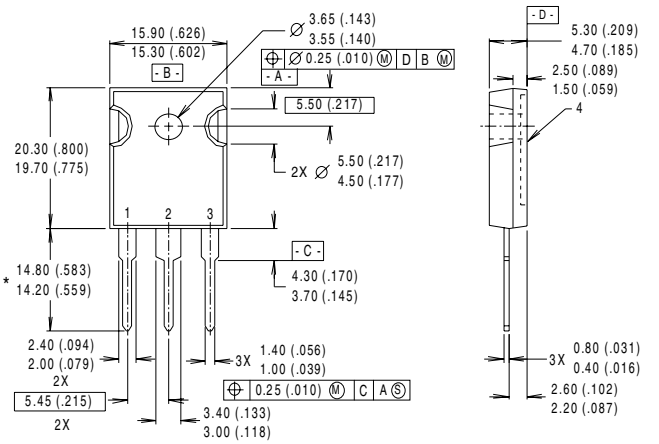
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 5.0Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 7/00

International
IOR Rectifier

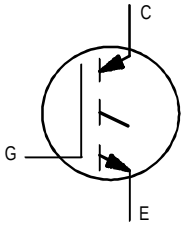
IRG4PC50U

INSULATED GATE BIPOLAR TRANSISTOR

UltraFast Speed IGBT

Features

- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-247AC package



n-channel

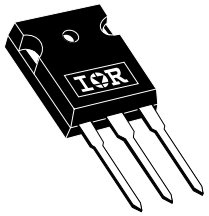
$V_{CES} = 600V$

$V_{CE(on)\ typ.} = 1.65V$

$@V_{GE} = 15V, I_C = 27A$

Benefits

- Generation 4 IGBT's offer highest efficiency available
- IGBT's optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	55	A
I_C @ T_C = 100°C	Continuous Collector Current	27	
I_{CM}	Pulsed Collector Current ①	220	
I_{LM}	Clamped Inductive Load Current ②	220	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	20	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	℃
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	----	0.64	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	----	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	----	40	
Wt	Weight	6 (0.21)	----	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	----	----	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	----	----	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	----	0.60	----	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	----	1.65	2.0	V	I_C = 27A V_{GE} = 15V
		----	2.0	----		I_C = 55A See Fig.2, 5
		----	1.6	----		I_C = 27A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	----	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	----	-13	----	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	16	24	----	S	V_{CE} ≥ 15V, I_C = 27A
I_{CES}	Zero Gate Voltage Collector Current	----	----	250	µA	V_{GE} = 0V, V_{CE} = 600V
		----	----	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		----	----	5000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	----	----	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	----	180	270	nC	I_C = 27A
Q_{ge}	Gate - Emitter Charge (turn-on)	----	25	38		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	----	61	90		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	----	32	----	ns	T_J = 25°C
t_r	Rise Time	----	20	----		I_C = 27A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	170	260		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	----	88	130		Energy losses include "tail"
E_{on}	Turn-On Switching Loss	----	0.12	----	mJ	See Fig. 10, 11, 13, 14
E_{off}	Turn-Off Switching Loss	----	0.54	----		
E_{ts}	Total Switching Loss	----	0.66	0.9		
$t_{d(on)}$	Turn-On Delay Time	----	31	----	ns	T_J = 150°C,
t_r	Rise Time	----	23	----		I_C = 27A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	230	----		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	----	120	----		Energy losses include "tail"
E_{ts}	Total Switching Loss	----	1.6	----	mJ	See Fig. 13, 14
L_E	Internal Emitter Inductance	----	13	----	nH	Measured 5mm from package
C_{ies}	Input Capacitance	----	4000	----	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	----	250	----		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	----	52	----		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 5.0Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

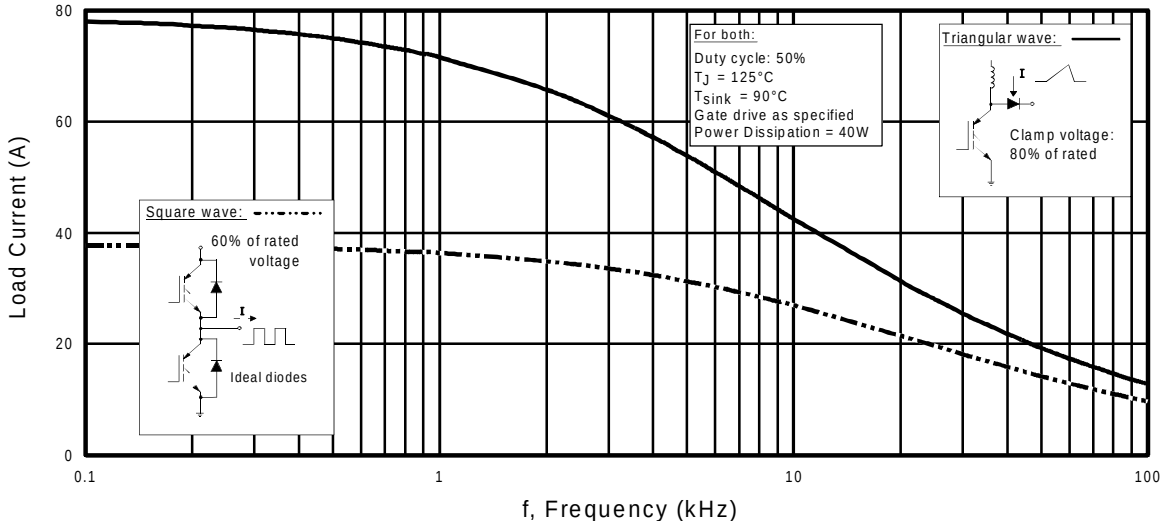


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

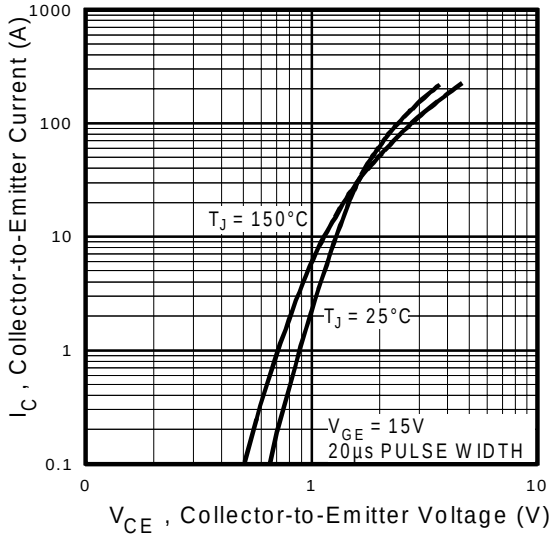


Fig. 2 - Typical Output Characteristics

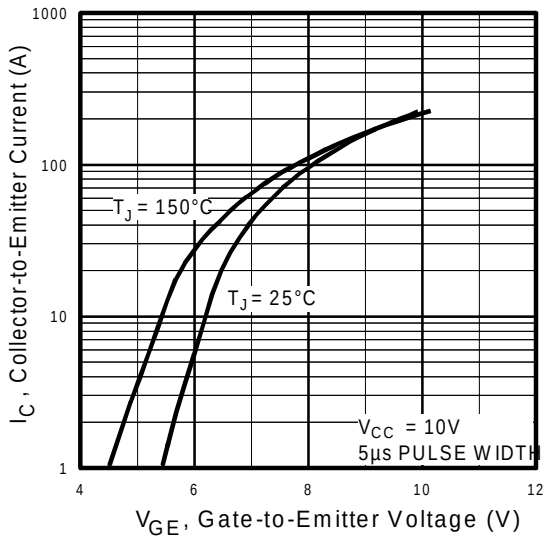


Fig. 3 - Typical Transfer Characteristics

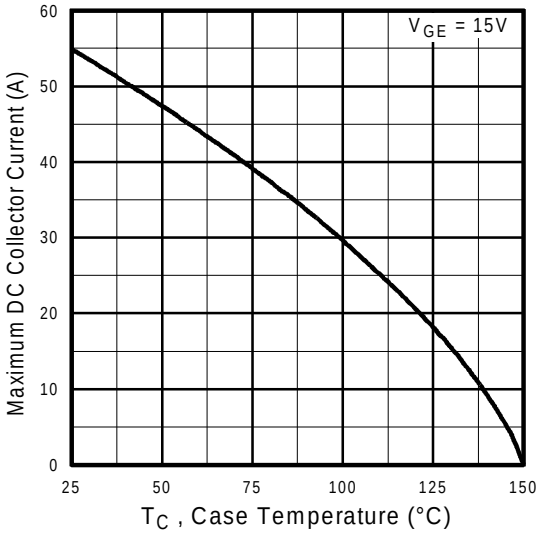


Fig. 4 - Maximum Collector Current vs. Case Temperature

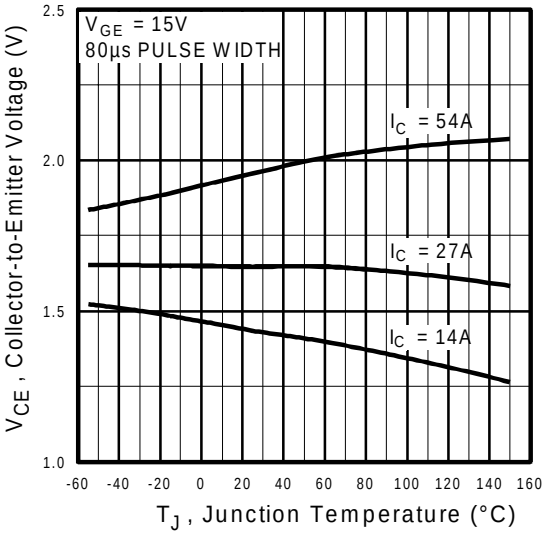


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

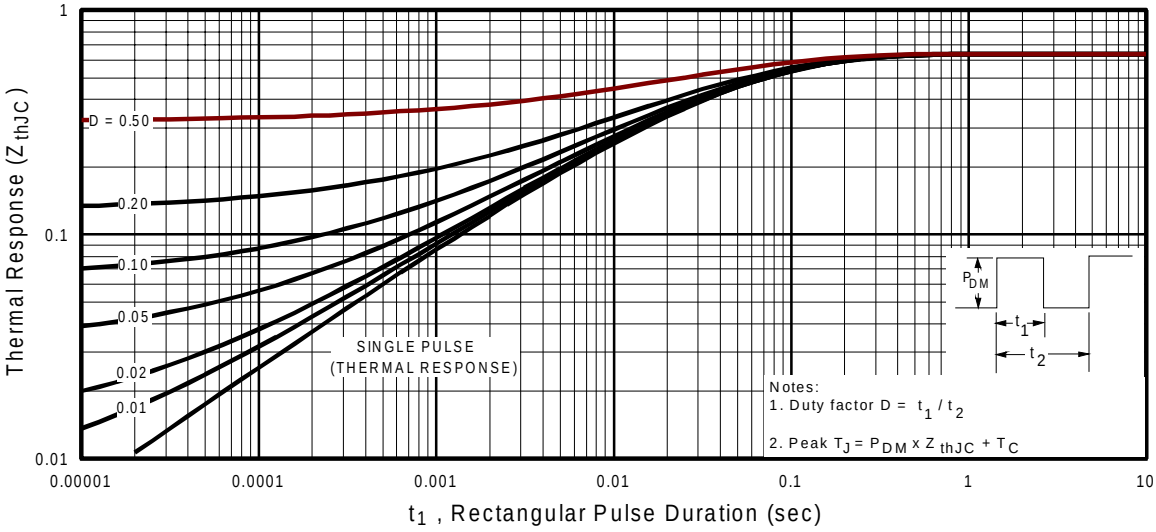


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

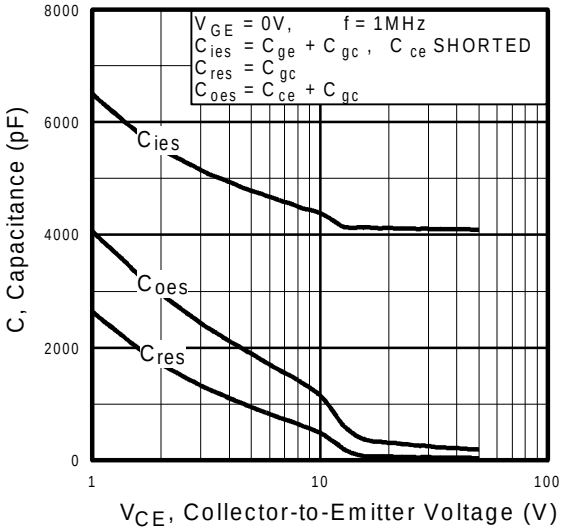


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

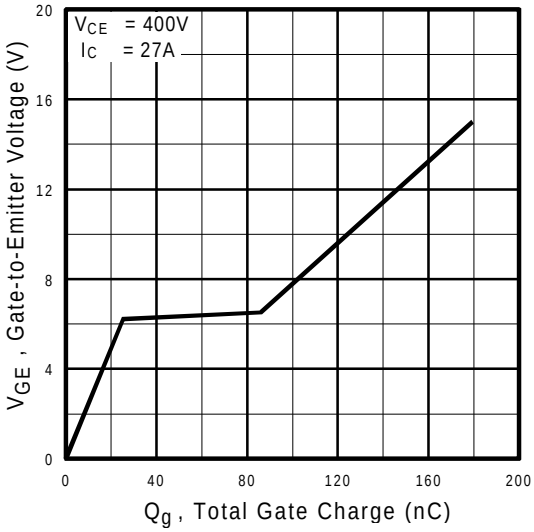


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

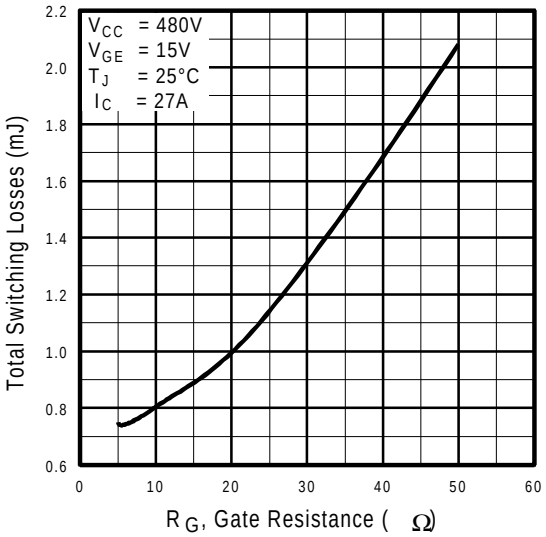


Fig. 9 - Typical Switching Losses vs. Gate Resistance

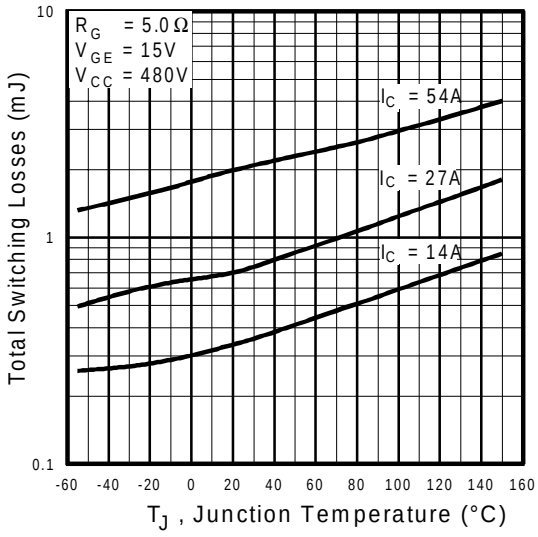


Fig. 10 - Typical Switching Losses vs. Junction Temperature

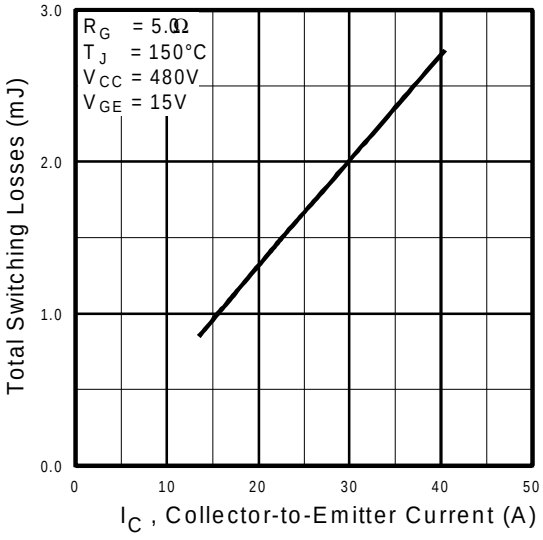


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

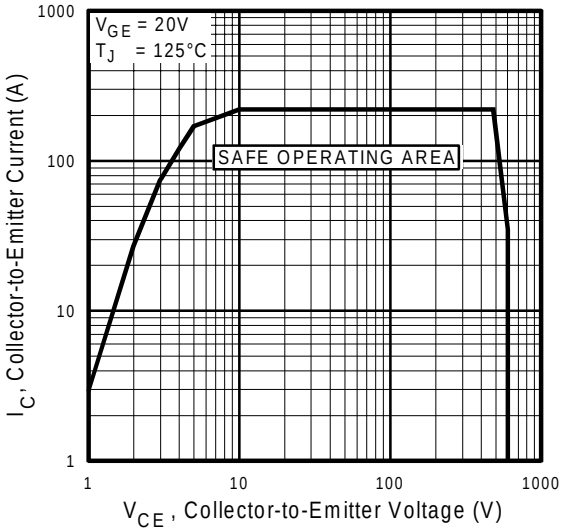


Fig. 12 - Turn-Off SOA

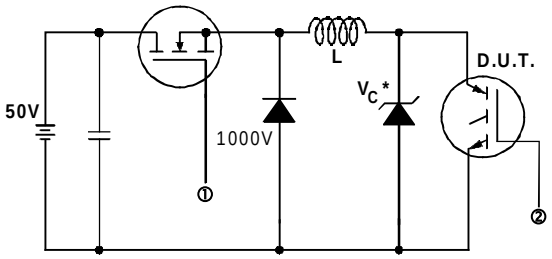


Fig. 13a - Clamped Inductive Load Test Circuit

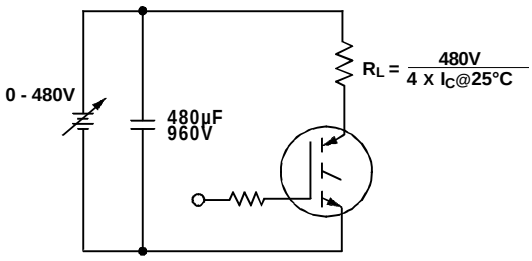


Fig. 13b - Pulsed Collector Current Test Circuit

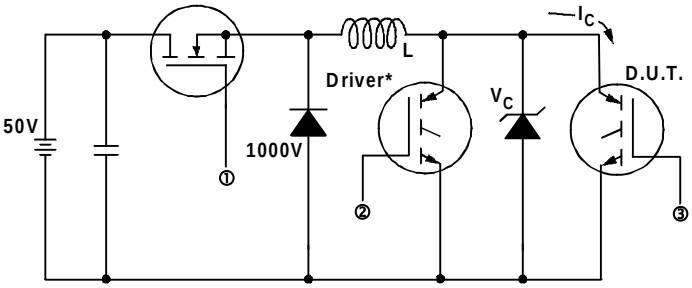


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

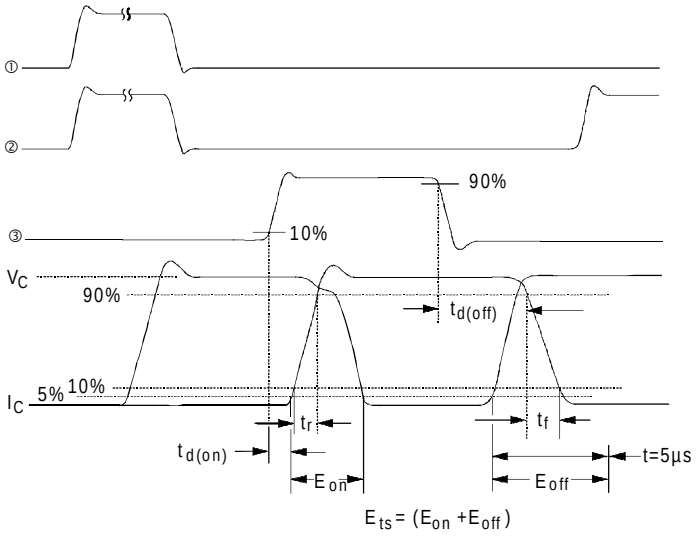
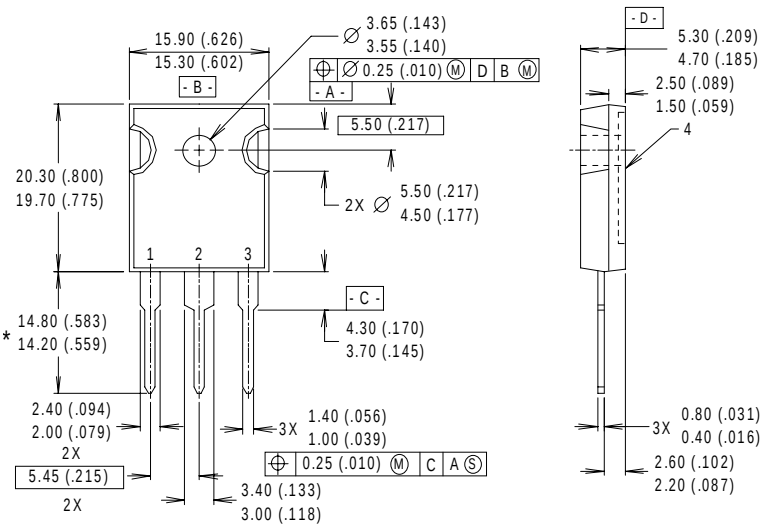


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

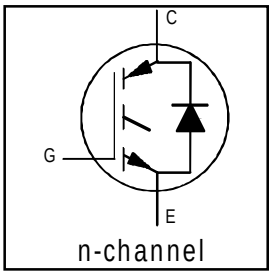
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
Data and specifications subject to change without notice. 12/00

International
IOR Rectifier

IRG4PC50UD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

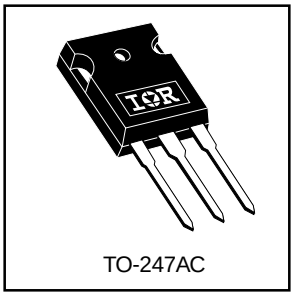
UltraFast CoPack IGBT



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.65V

@V_{GE} = 15V, I_C = 27A



TO-247AC

Features

- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-247AC package

Benefits

- Generation 4 IGBT's offer highest efficiencies available
- IGBT's optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBT's . Minimized recovery characteristics require less/no snubbing
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	55	A
I_C @ T_C = 100°C	Continuous Collector Current	27	
I_{CM}	Pulsed Collector Current ①	220	
I_{LM}	Clamped Inductive Load Current ②	220	
I_F @ T_C = 100°C	Diode Continuous Forward Current	25	
I_{FM}	Diode Maximum Forward Current	220	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	------	------	0.64	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	------	------	0.83	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	------	0.24	------	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	-----	-----	40	
Wt	Weight	------	6 (0.21)	------	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	----	----	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	----	0.60	----	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	----	1.65	2.0	V	I_C = 27A V_{GE} = 15V
		----	2.0	----		I_C = 55A See Fig. 2, 5
		----	1.6	----		I_C = 27A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	----	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	----	-13	----	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	16	24	----	S	V_{CE} = 100V, I_C = 27A
I_{CES}	Zero Gate Voltage Collector Current	----	----	250	µA	V_{GE} = 0V, V_{CE} = 600V
		----	----	6500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	----	1.3	1.7	V	I_C = 25A See Fig. 13
		----	1.2	1.5		I_C = 25A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	----	----	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	----	180	270	nC	I_C = 27A
Qge	Gate - Emitter Charge (turn-on)	----	25	38		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	----	61	90		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	----	46	----	ns	T_J = 25°C
t_r	Rise Time	----	25	----		I_C = 27A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	140	230		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	----	74	110		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	----	0.99	----	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	----	0.59	----		See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	----	1.58	1.9		
$t_{d(on)}$	Turn-On Delay Time	----	44	----	ns	T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	----	27	----		I_C = 27A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	240	----		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	----	130	----		Energy losses include "tail" and
E_{ts}	Total Switching Loss	----	2.3	----	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	----	13	----	nH	Measured 5mm from package
C_{ies}	Input Capacitance	----	4000	----	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	----	250	----		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	----	52	----		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	----	50	75	ns	T_J = 25°C See Fig.
		----	105	160		T_J = 125°C 14 I_F = 25A
I_{rr}	Diode Peak Reverse Recovery Current	----	4.5	10	A	T_J = 25°C See Fig.
		----	8.0	15		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	----	112	375	nC	T_J = 25°C See Fig.
		----	420	1200		T_J = 125°C 16 di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	----	250	----	A/µs	T_J = 25°C
	During t_b	----	160	----		T_J = 125°C

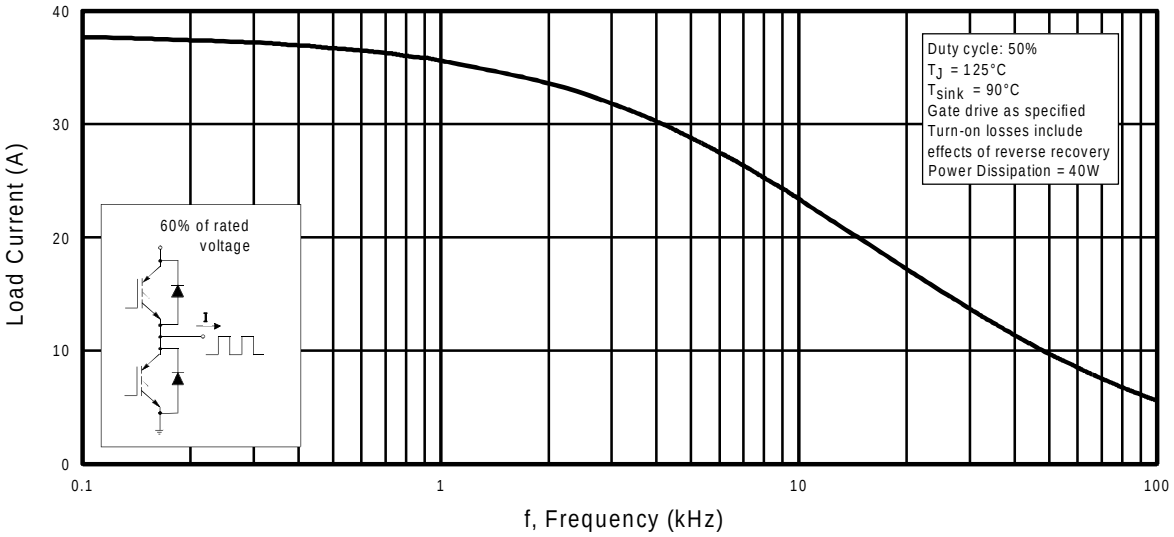


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

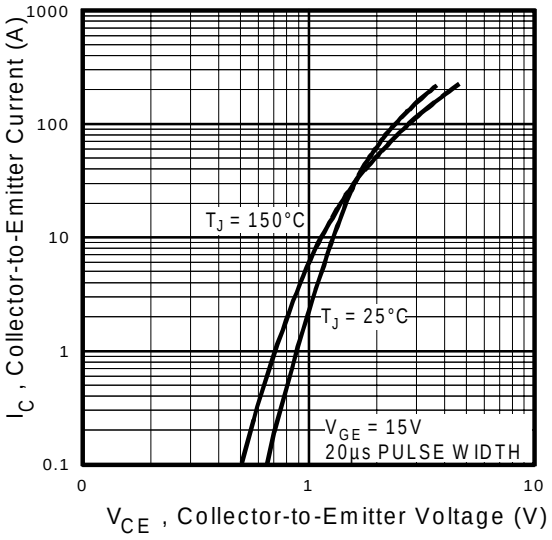


Fig. 2 - Typical Output Characteristics

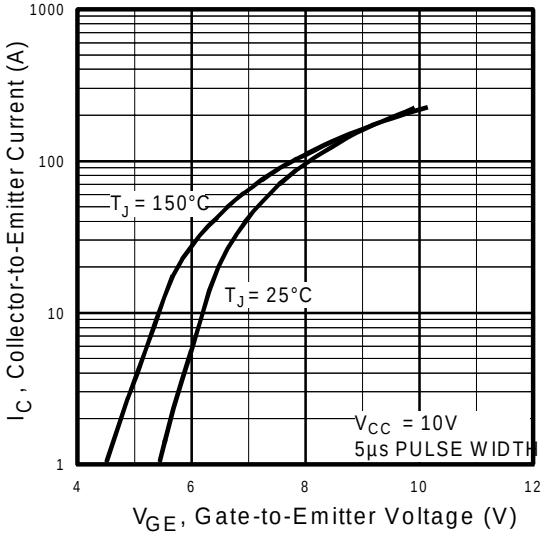


Fig. 3 - Typical Transfer Characteristics

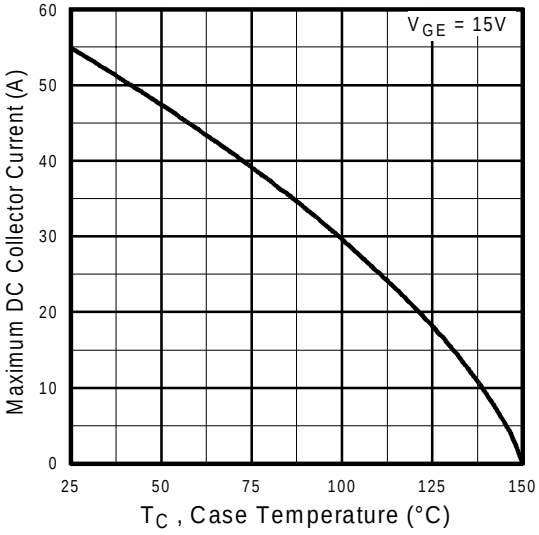


Fig. 4 - Maximum Collector Current vs. Case Temperature

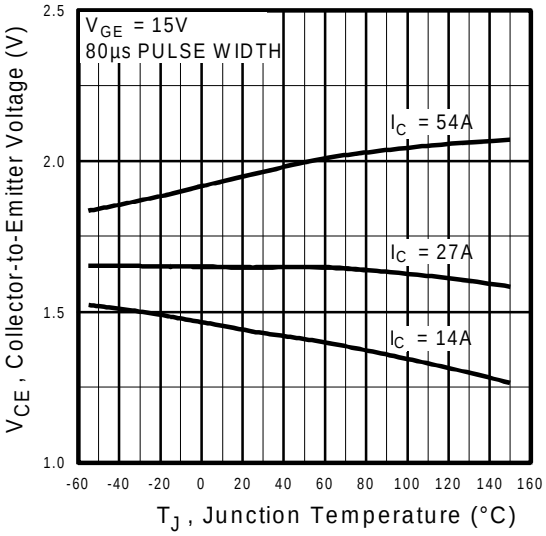


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

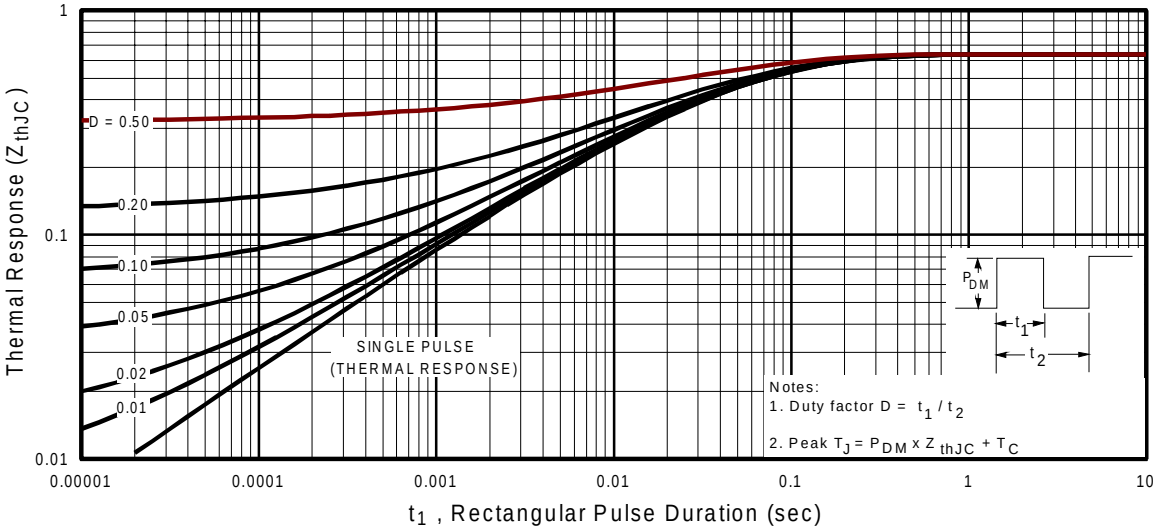


Fig. 6 - Maximum IGBT Effective Transient Thermal Impedance, Junction-to-Case

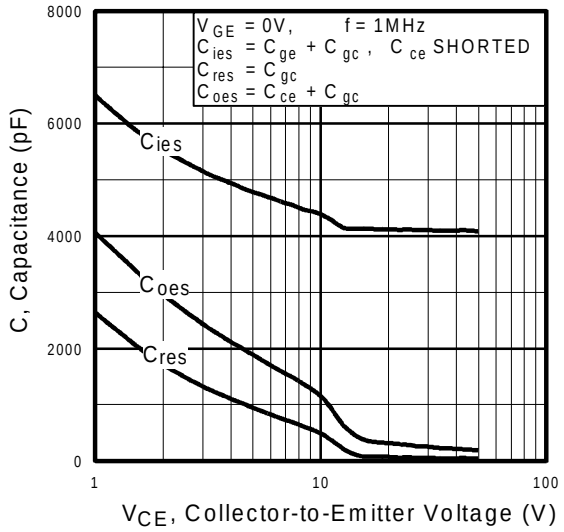


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

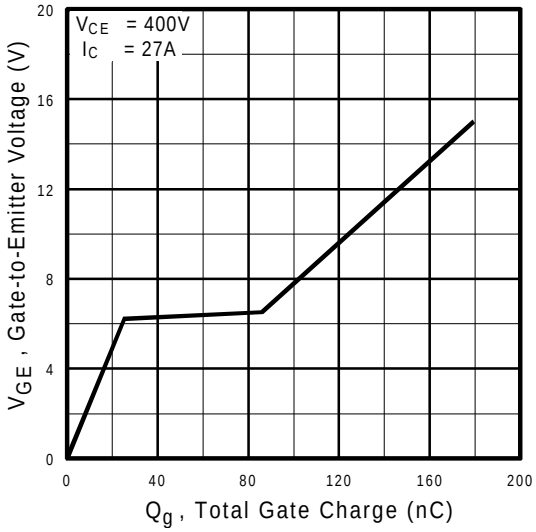


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

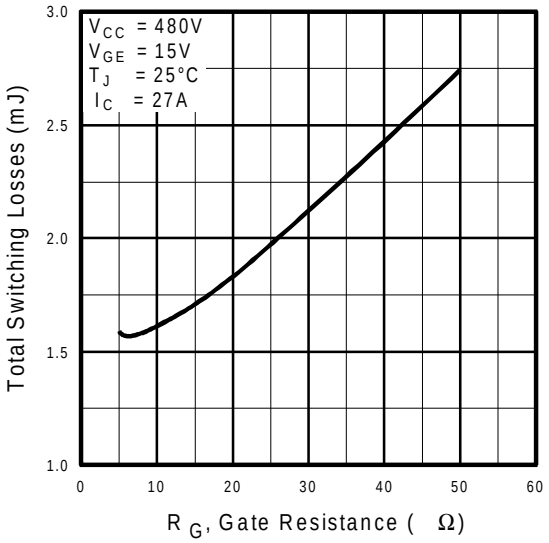


Fig. 9 - Typical Switching Losses vs. Gate Resistance

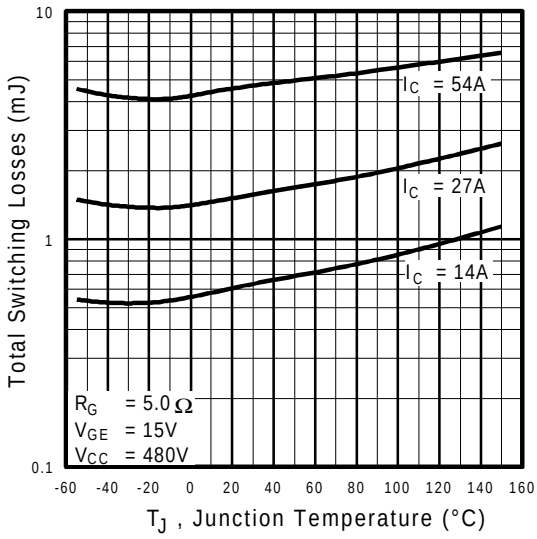


Fig. 10 - Typical Switching Losses vs. Junction Temperature

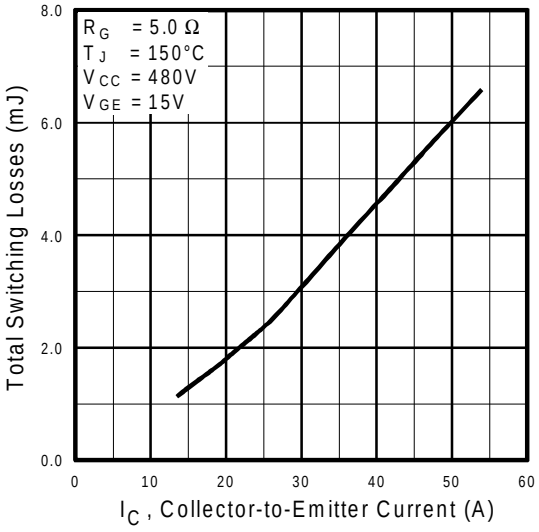


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

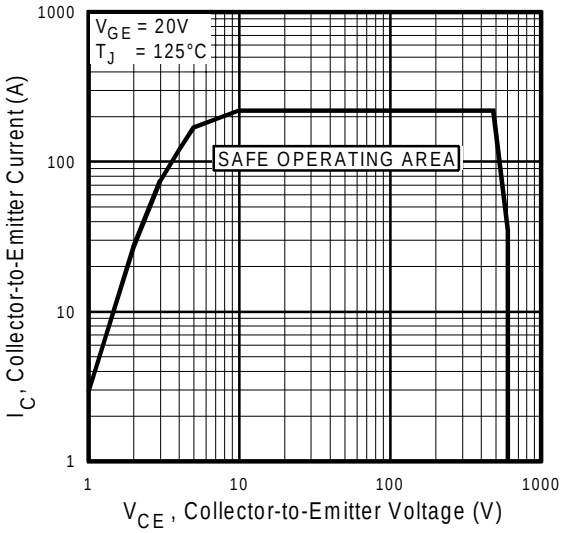


Fig. 12 - Turn-Off SOA

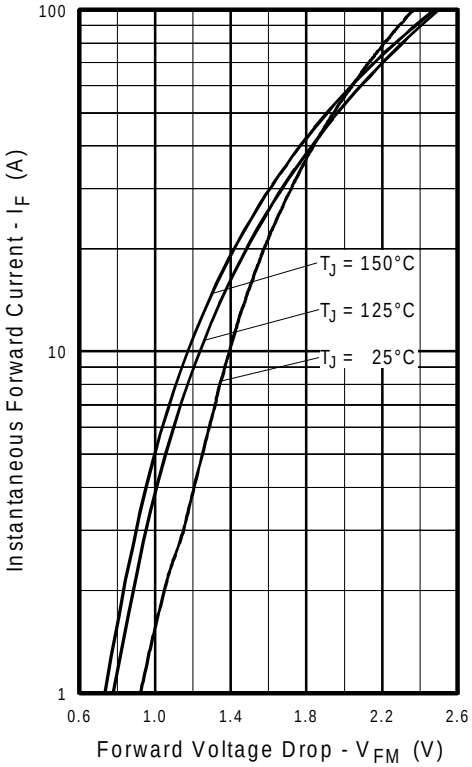


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

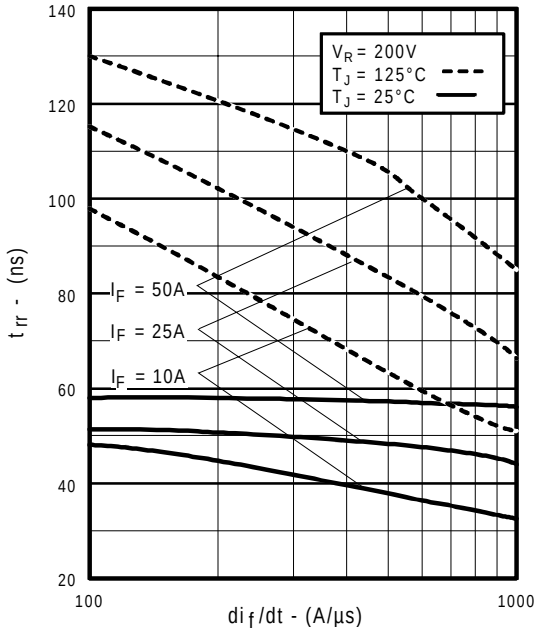


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

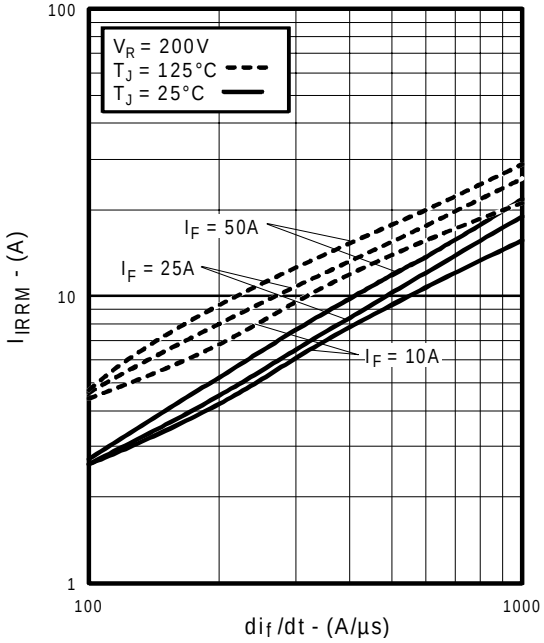


Fig. 15 - Typical Recovery Current vs. di_f/dt

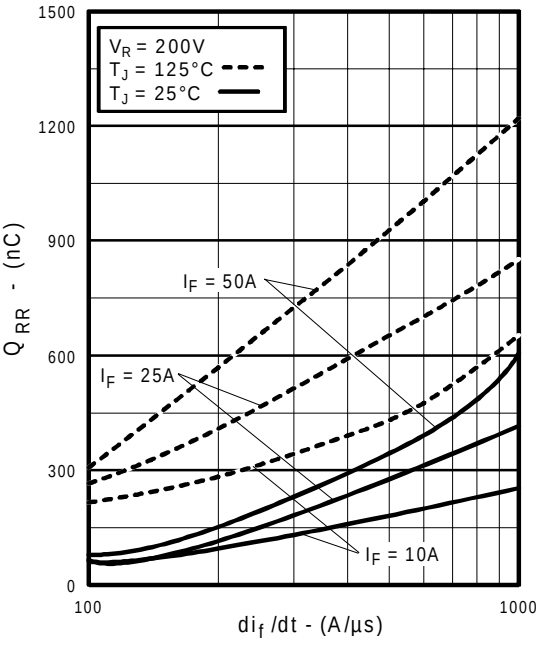


Fig. 16 - Typical Stored Charge vs. di_f/dt

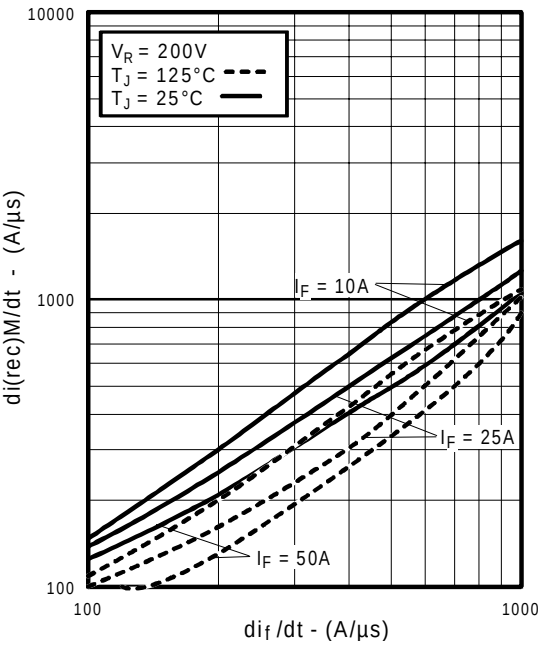


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

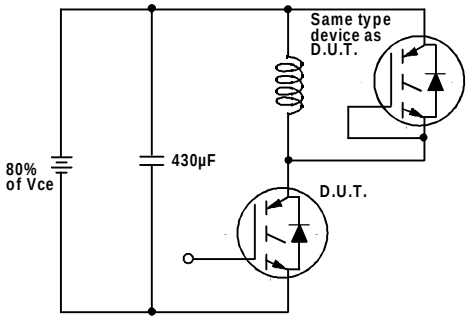


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

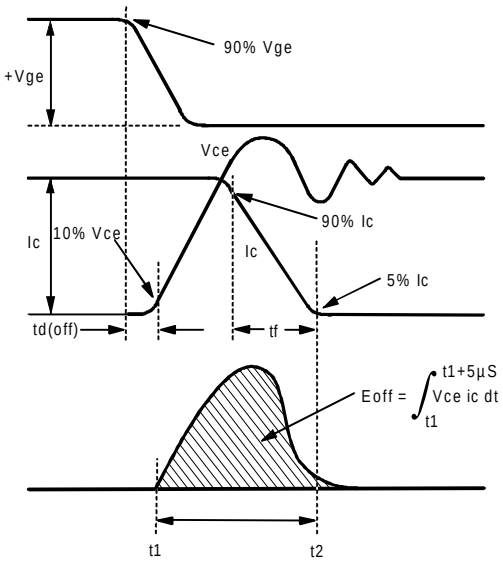


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

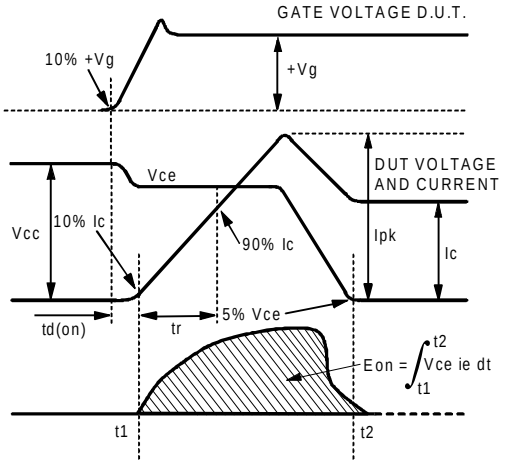


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

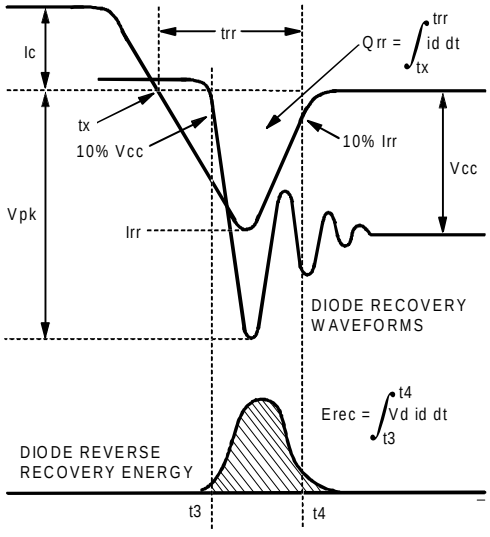


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

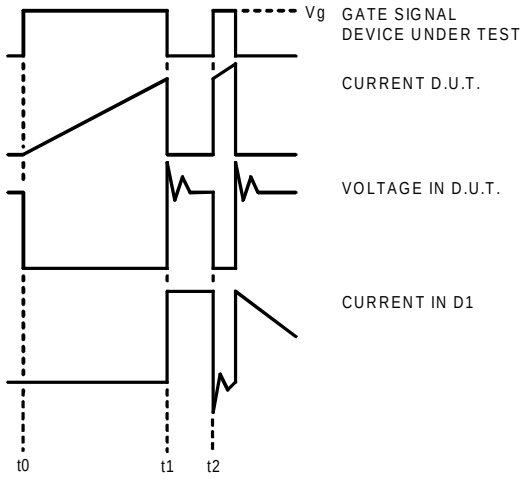


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

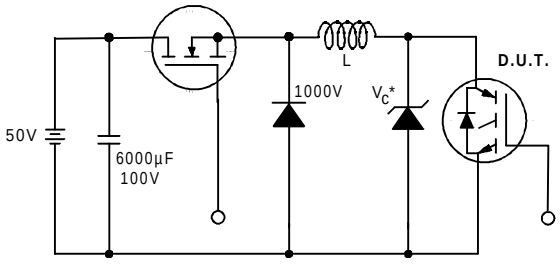


Figure 19. Clamped Inductive Load Test Circuit

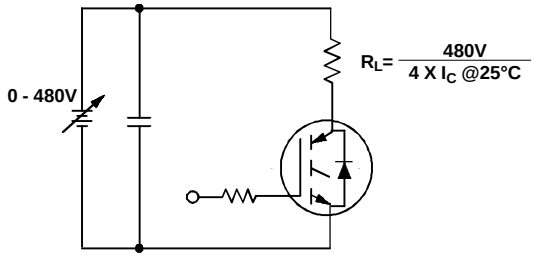


Figure 20. Pulsed Collector Current Test Circuit

Notes:

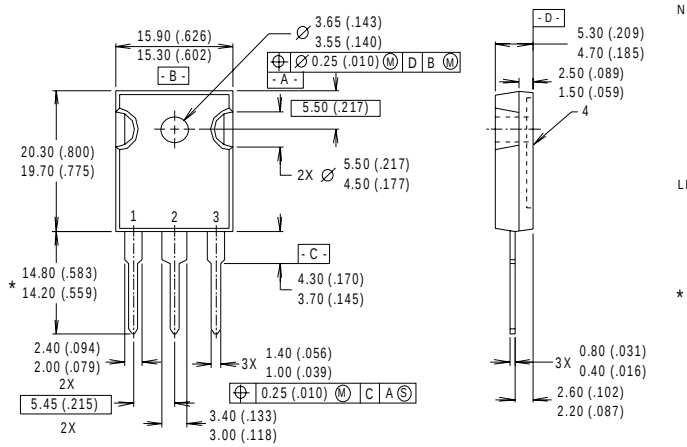
① Repetitive rating: V_{GE} = 20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 5.0Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
Data and specifications subject to change without notice. 12/00

PD - 91455B

International
IOR Rectifier

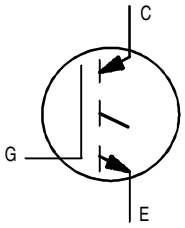
IRG4BC40S

INSULATED GATE BIPOLAR TRANSISTOR

Standard Speed IGBT

Features

- Standard: optimized for minimum saturation voltage and low operating frequencies (< 1kHz)
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-220AB package



n-channel

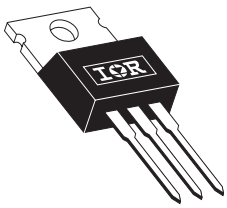
$V_{CES} = 600V$

$V_{CE(on)\ typ.} = 1.32V$

$@V_{GE} = 15V, I_C = 31A$

Benefits

- Generation 4 IGBTs offer highest efficiency available
- IGBTs optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	60	A
I_C @ T_C = 100°C	Continuous Collector Current	31	
I_{CM}	Pulsed Collector Current ①	120	
I_{LM}	Clamped Inductive Load Current ②	120	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	15	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.77	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	80	
Wt	Weight	2.0 (0.07)	—	g (oz)

4/17/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.75	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.32	1.5	V	I_C = 31A V_{GE} = 15V
		—	1.68	—		I_C = 60A See Fig.2, 5
		—	1.32	—		I_C = 31A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-9.3	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	12	21	—	S	V_{CE} = 100V, I_C = 31A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	100	150	nC	I_C = 31A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	14	21		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	34	51		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	22	—	ns	
t_r	Rise Time	—	18	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	650	980		I_C = 31A, V_{CC} = 480V
t_f	Fall Time	—	380	570		V_{GE} = 15V, R_G = 10Ω
E_{on}	Turn-On Switching Loss	—	0.45	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	6.5	—		See Fig. 10, 11, 13, 14
E_{ts}	Total Switching Loss	—	6.95	9.9		
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	T_J = 150°C,
t_r	Rise Time	—	21	—		I_C = 31A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	1000	—		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	—	940	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	12	—	mJ	See Fig. 13, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	2200	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	140	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	26	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 10Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

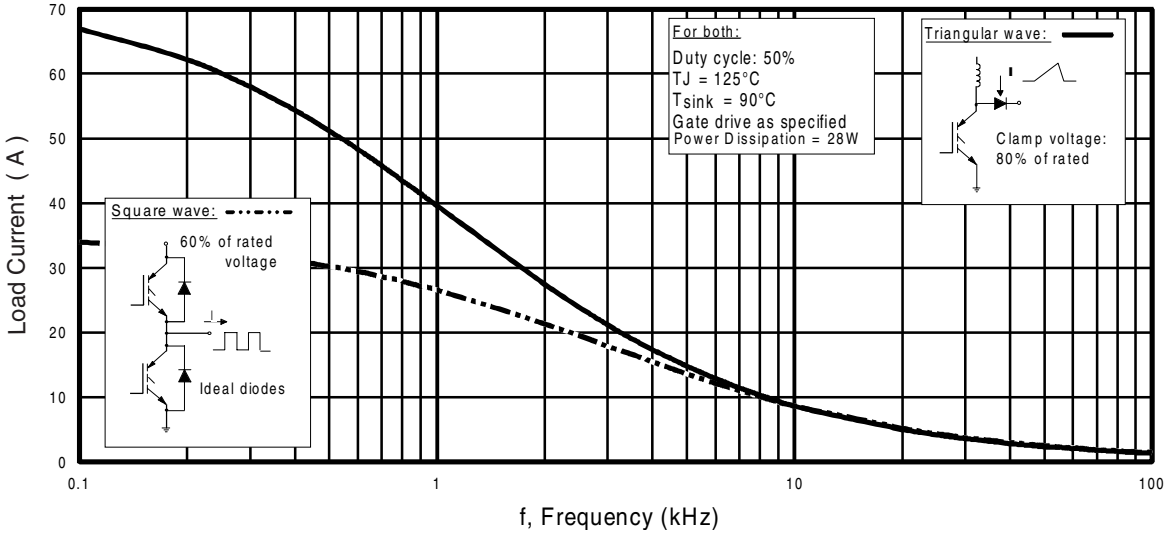


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

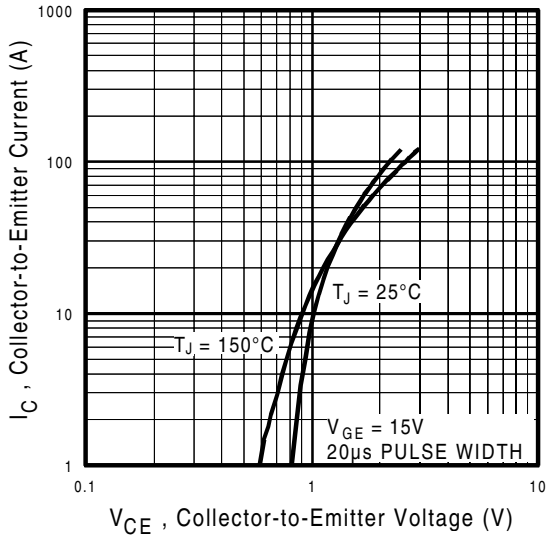


Fig. 2 - Typical Output Characteristics

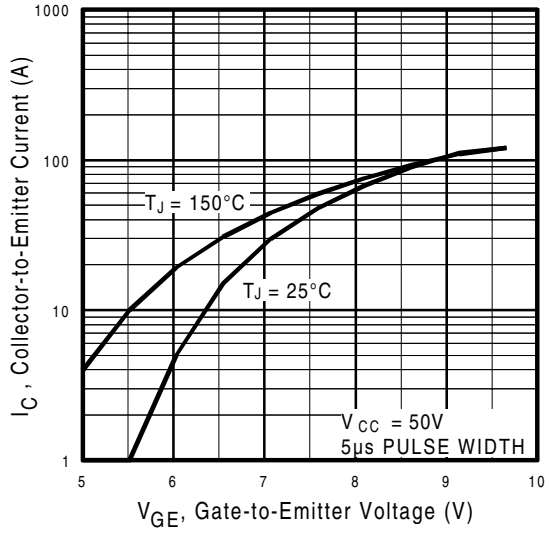


Fig. 3 - Typical Transfer Characteristics

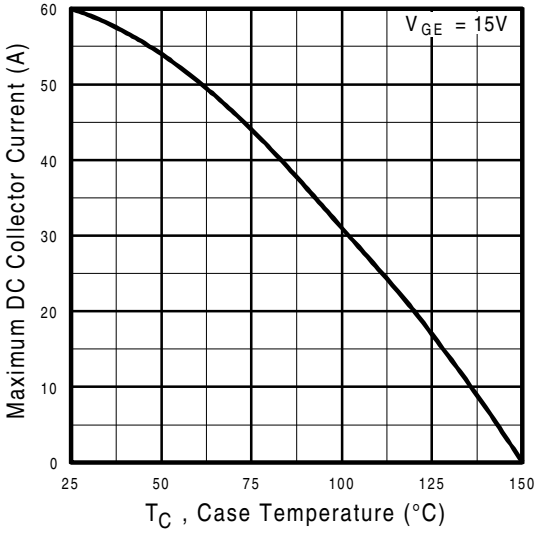


Fig. 4 - Maximum Collector Current vs. Case Temperature

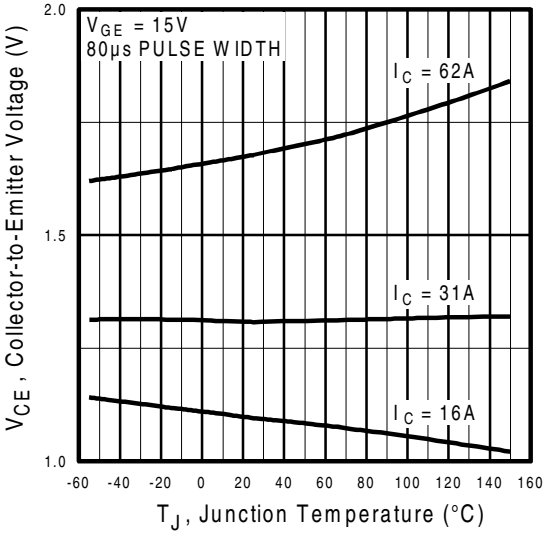


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

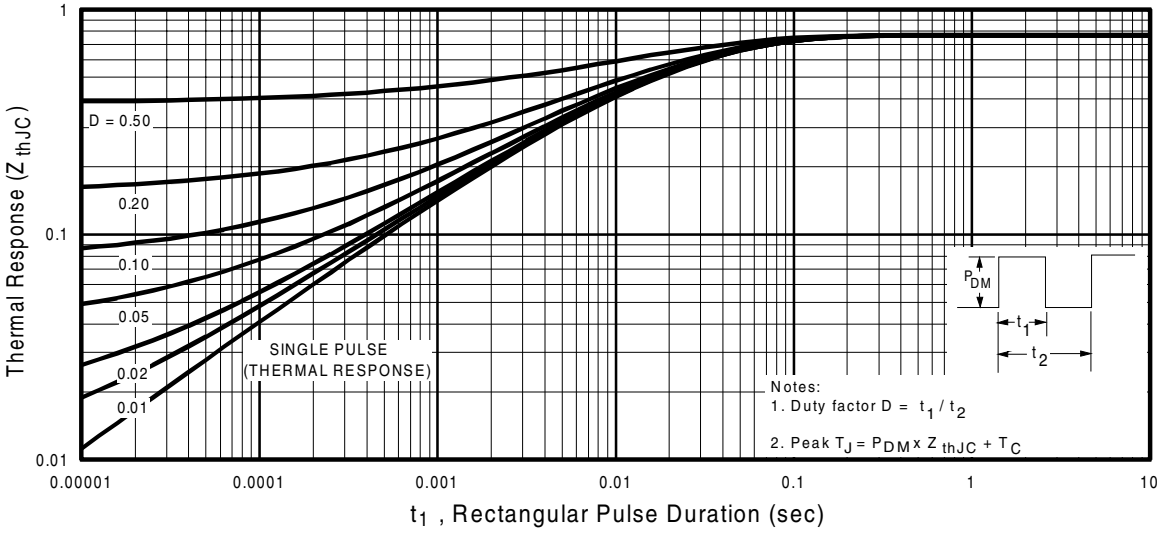


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

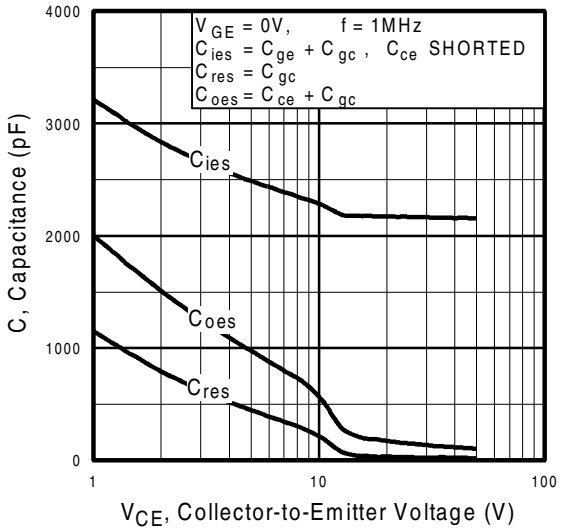


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

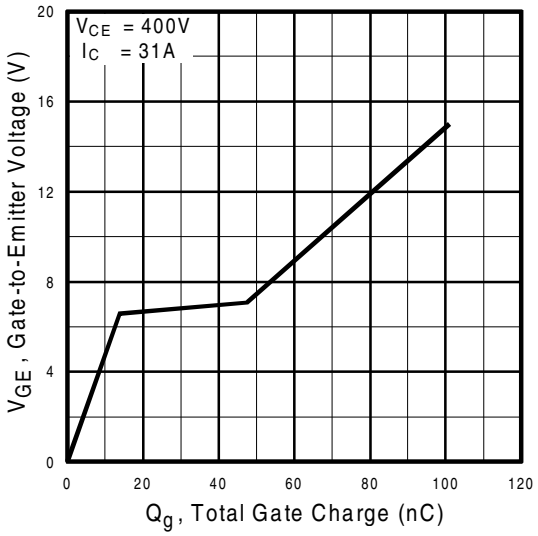


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

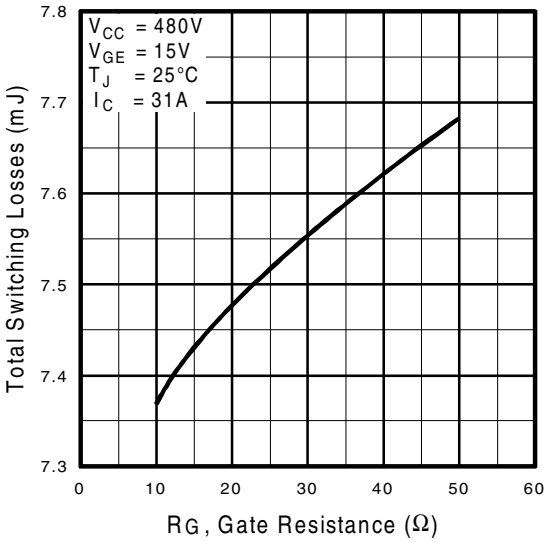


Fig. 9 - Typical Switching Losses vs. Gate Resistance

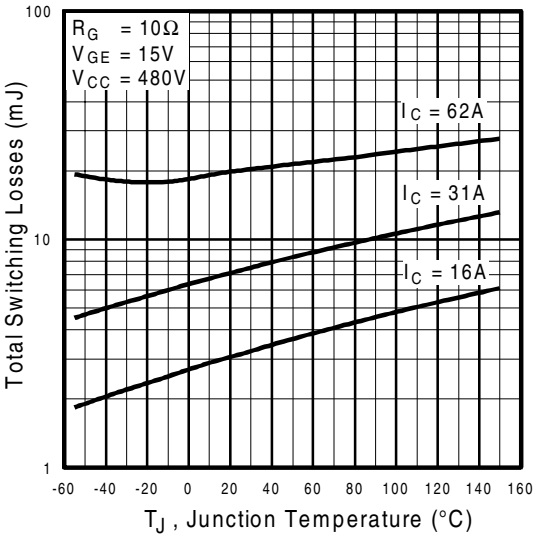


Fig. 10 - Typical Switching Losses vs. Junction Temperature

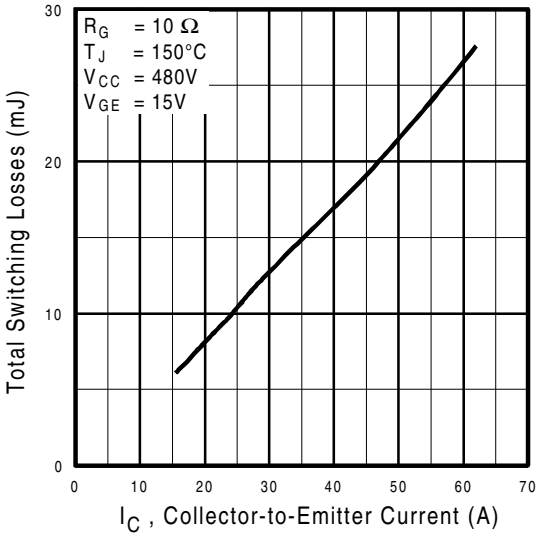


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

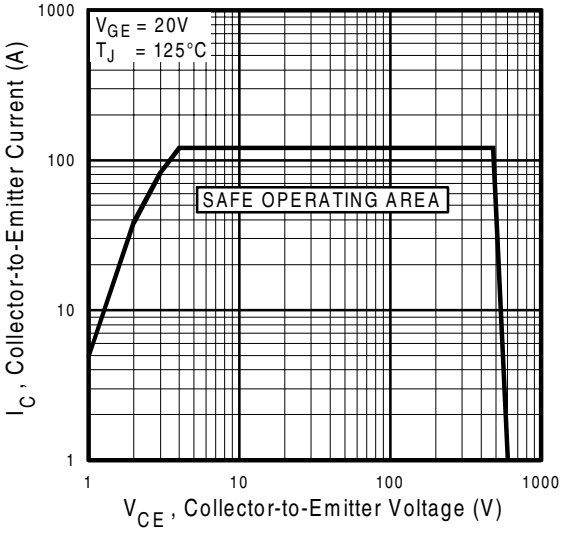


Fig. 12 - Turn-Off SOA

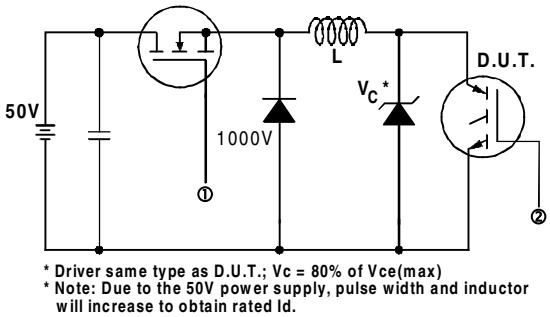


Fig. 13a - Clamped Inductive Load Test Circuit

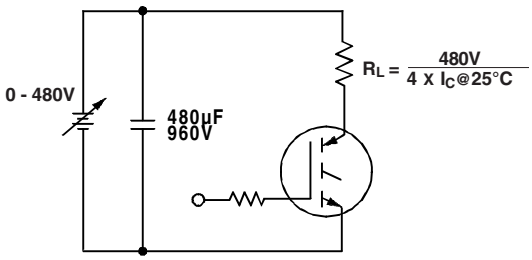


Fig. 13b - Pulsed Collector Current Test Circuit

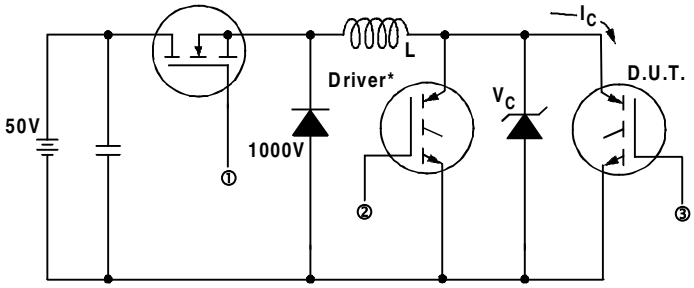


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

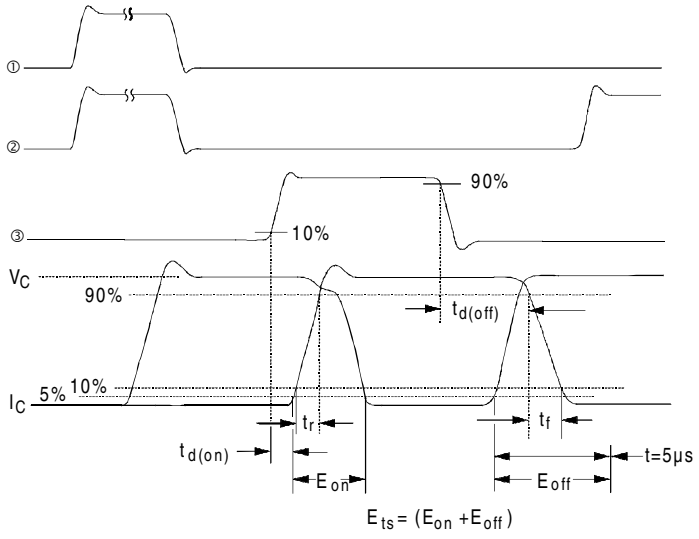
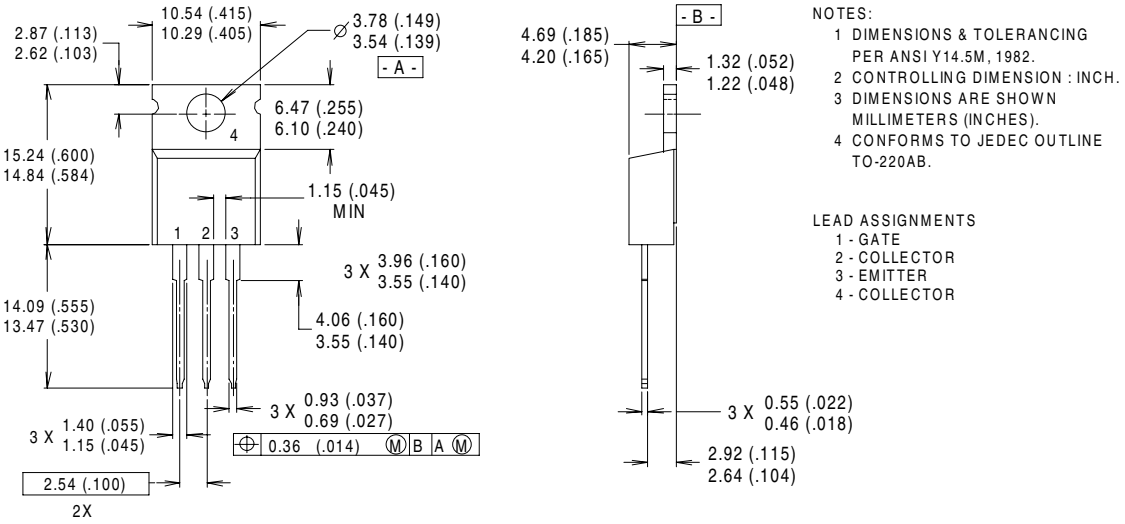


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD 91465B

International
IOR Rectifier

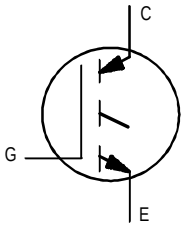
IRG4PC40S

INSULATED GATE BIPOLAR TRANSISTOR

Standard Speed IGBT

Features

- Standard: Optimized for minimum saturation voltage and low operating frequencies (< 1kHz)
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-247AC package



n-channel

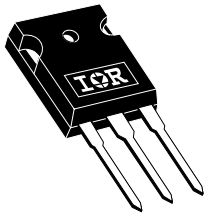
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.32V

@V_{GE} = 15V, I_C = 31A

Benefits

- Generation 4 IGBT's offer highest efficiency available
- IGBT's optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	60	A
I_C @ T_C = 100°C	Continuous Collector Current	31	
I_{CM}	Pulsed Collector Current ①	120	
I_{LM}	Clamped Inductive Load Current ②	120	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	15	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.77	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

12/30/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.75	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.32	1.5	V	I_C = 31A V_{GE} = 15V
		—	1.68	—		I_C = 60A See Fig.2, 5
		—	1.32	—		I_C = 31A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-9.3	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	12	21	—	S	V_{CE} = 100V, I_C = 31A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	100	150	nC	I_C = 31A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	14	21		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	34	51		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	22	—	ns	
t_r	Rise Time	—	18	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	650	980		I_C = 31A, V_{CC} = 480V
t_f	Fall Time	—	380	570		V_{GE} = 15V, R_G = 10Ω
E_{on}	Turn-On Switching Loss	—	0.45	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	6.5	—		See Fig. 10, 11, 13, 14
E_{ts}	Total Switching Loss	—	6.95	9.9		
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	T_J = 150°C,
t_r	Rise Time	—	21	—		I_C = 31A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	1000	—		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	—	940	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	12	—	mJ	See Fig. 13, 14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	2200	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	140	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	26	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 10Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

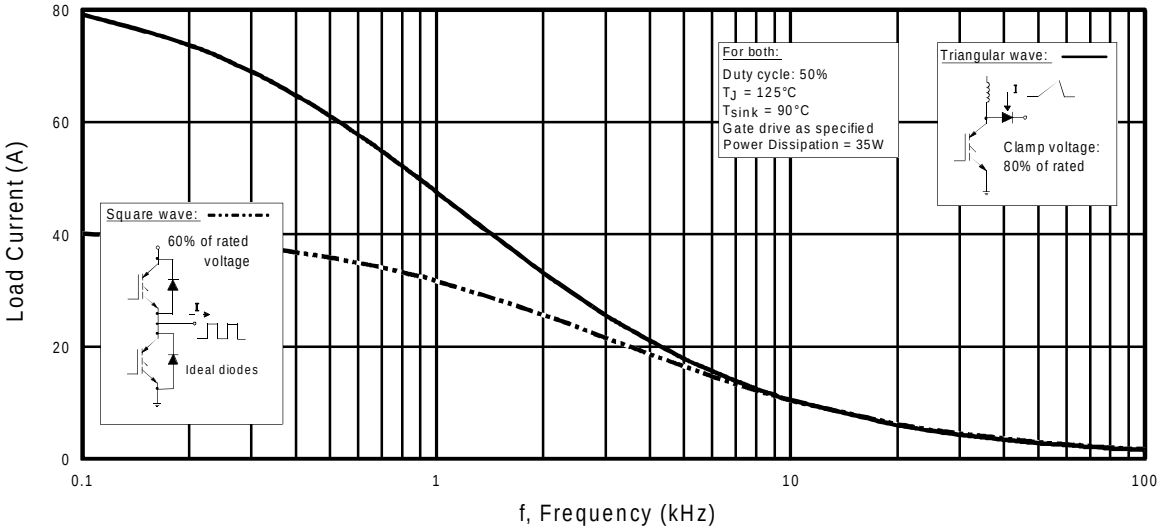


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

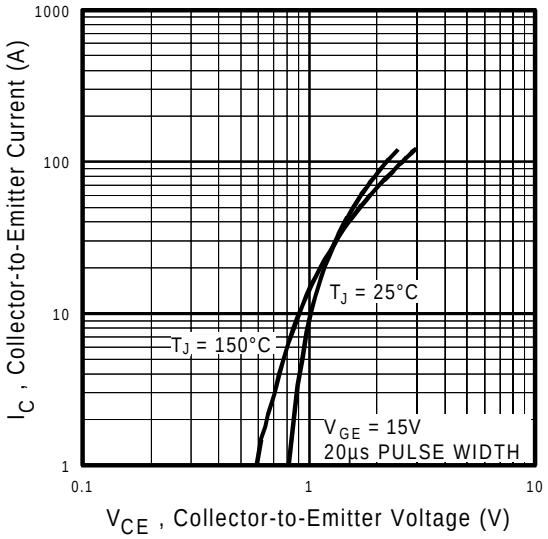


Fig. 2 - Typical Output Characteristics

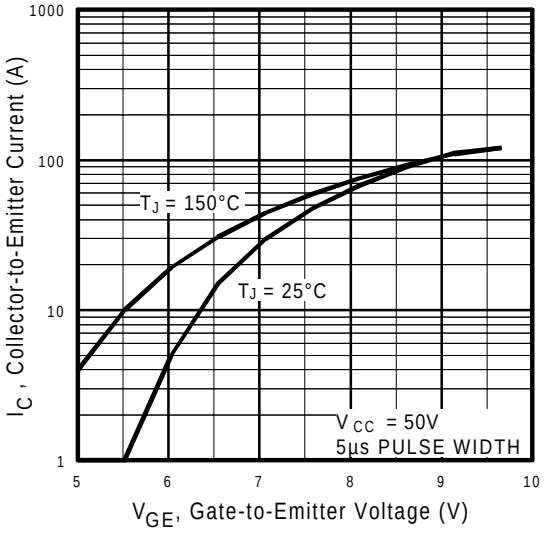


Fig. 3 - Typical Transfer Characteristics

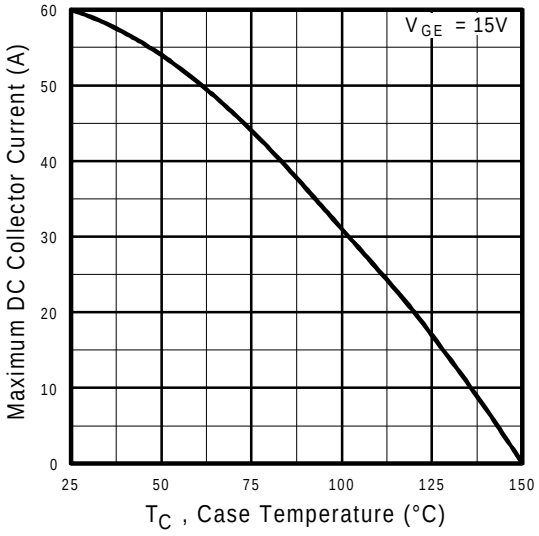


Fig. 4 - Maximum Collector Current vs. Case Temperature

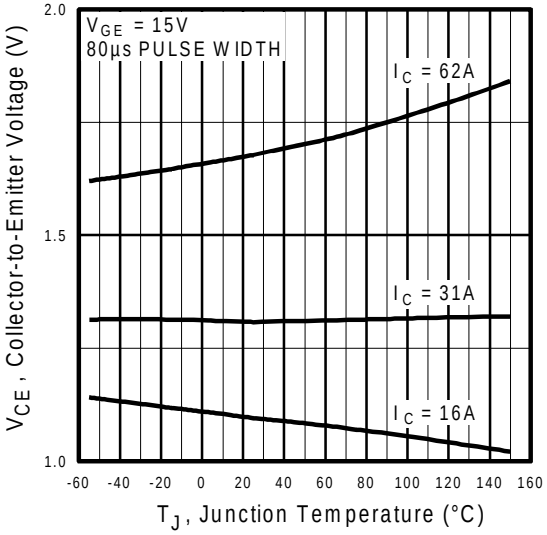


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

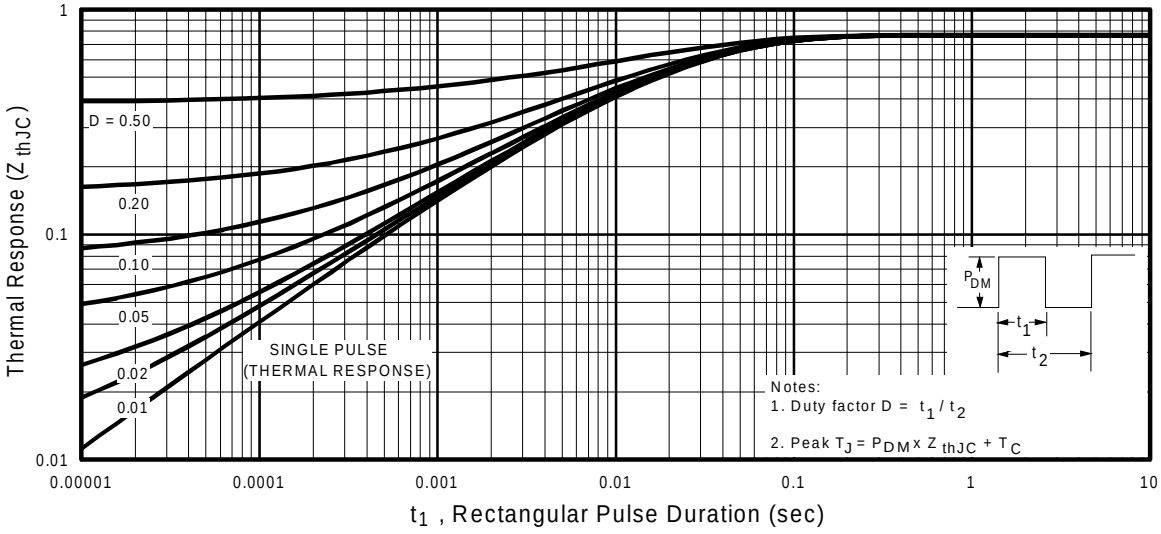


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

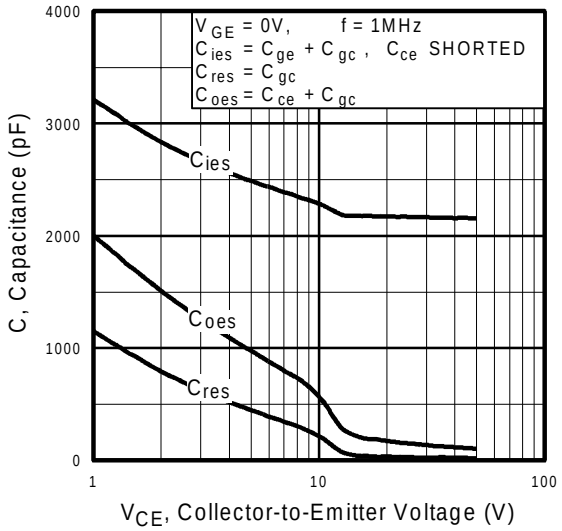


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

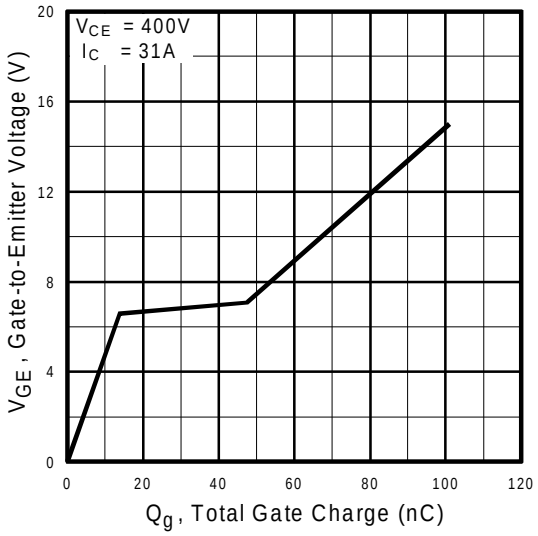


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

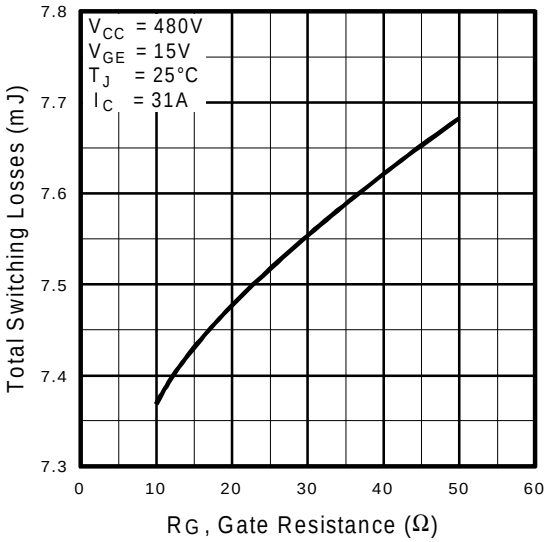


Fig. 9 - Typical Switching Losses vs. Gate Resistance

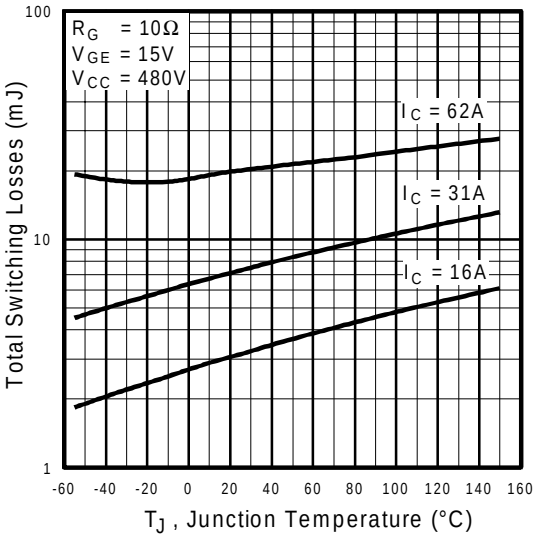


Fig. 10 - Typical Switching Losses vs. Junction Temperature

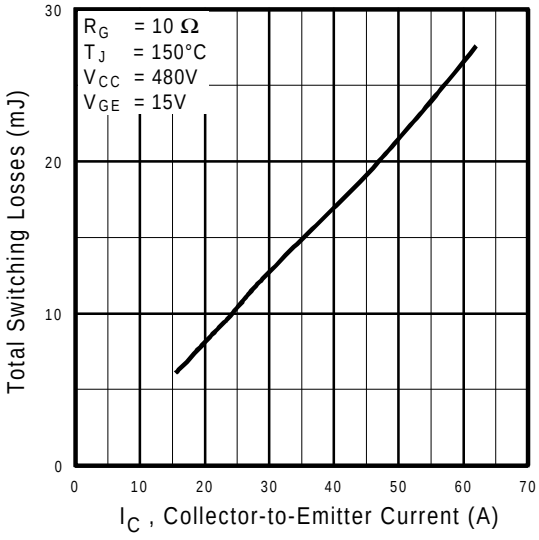


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

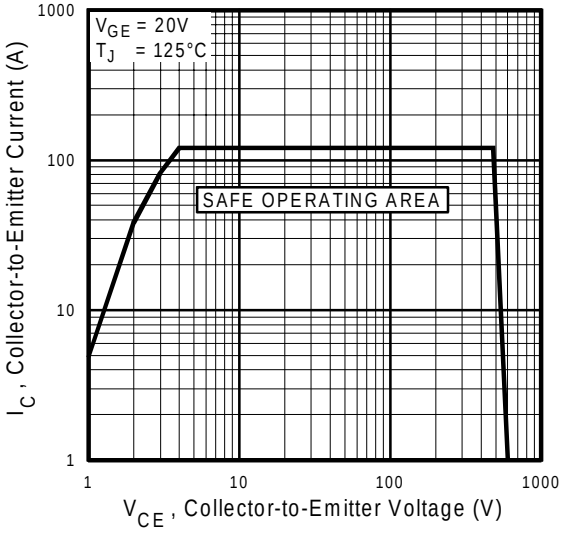


Fig. 12 - Turn-Off SOA

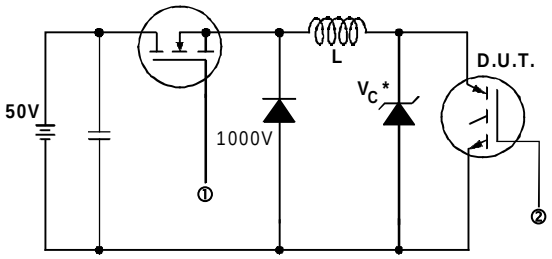


Fig. 13a - Clamped Inductive Load Test Circuit

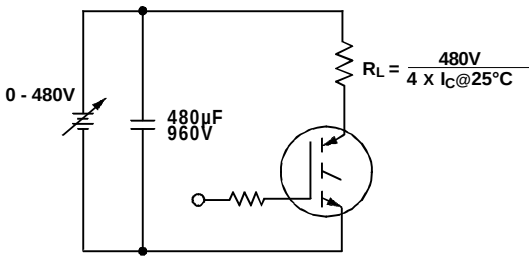


Fig. 13b - Pulsed Collector Current Test Circuit

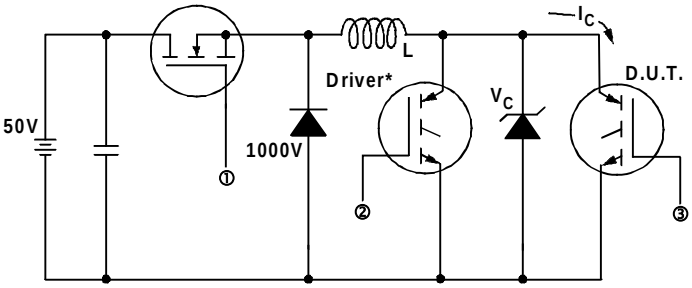


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

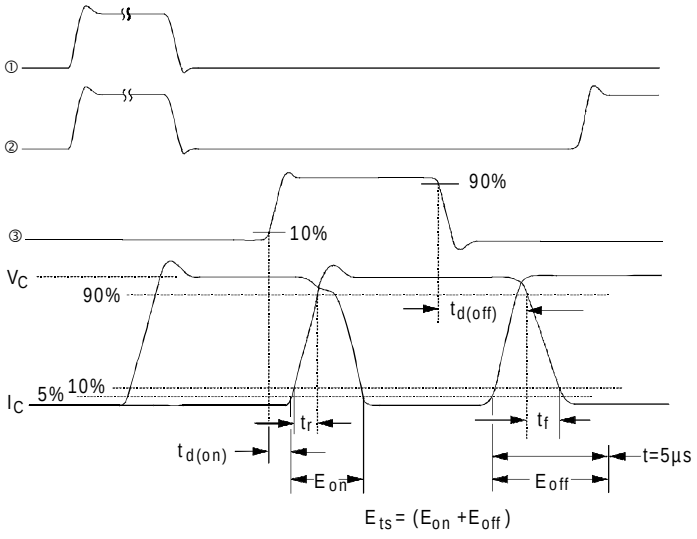
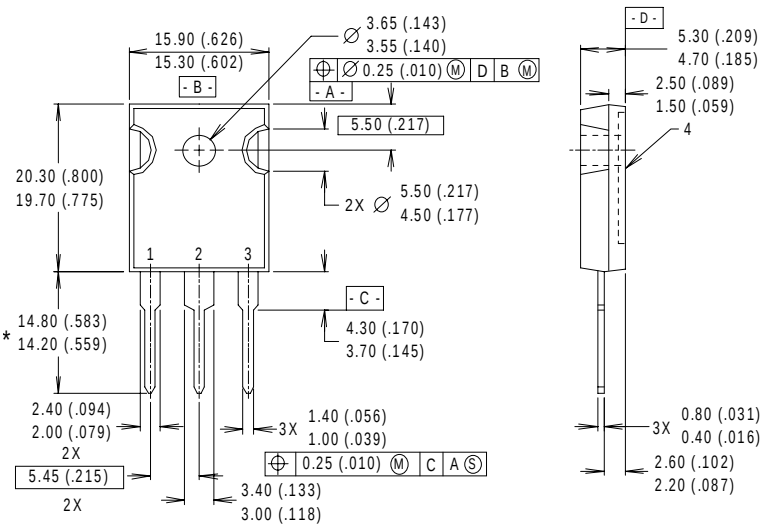


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
Data and specifications subject to change without notice. 12/00

International
IOR Rectifier

PD -93960

IRG4BH20K-S

INSULATED GATE BIPOLAR TRANSISTOR

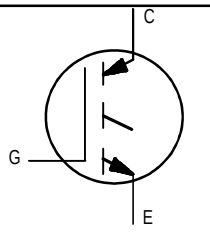
Short Circuit Rated
UltraFast IGBT

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs @ V_{CC} = 720V , T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Latest generation design provides tighter parameter distribution and higher efficiency than previous generations
- Industry standard D^2Pak package

Benefits

- As a Freewheeling Diode we recommend our HEXFRED™ ultrafast, ultrasoft recovery diodes for minimum EMI / Noise and switching losses in the Diode and IGBT
- Latest generation 4 IGBT's offer highest power density motor controls possible



n-channel

V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 3.17V

@V_{GE} = 15V, I_C = 5.0A



D^2Pak

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	11	A
I_C @ T_C = 100°C	Continuous Collector Current	5.0	
I_{CM}	Pulsed Collector Current ①	22	
I_{LM}	Clamped Inductive Load Current ②	22	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	130	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

8/17/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.13	—	V/°C	V_{GE} = 0V, I_C = 2.5mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	3.17	4.3	V	I_C = 5.0A V_{GE} = 15V
		—	4.04	—		I_C = 11A See Fig.2, 5
		—	2.84	—		I_C = 5.0A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.5	—	6.5		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 1mA
g_{fe}	Forward Transconductance ⑤	2.3	3.5	—	S	V_{CE} = 100 V, I_C = 5.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	28	43	nC	I_C = 5.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	4.4	6.6		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	12	18		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	
t_r	Rise Time	—	26	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	93	140		I_C =5.0A, V_{CC} = 960V
t_f	Fall Time	—	270	400		V_{GE} = 15V, R_G = 50Ω
E_{on}	Turn-On Switching Loss	—	0.45	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.44	—		See Fig. 9,10,14
E_{ts}	Total Switching Loss	—	0.89	1.2		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 720V, T_J = 125°C
						V_{GE} = 15V, R_G = 50Ω
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	T_J = 150°C,
t_r	Rise Time	—	28	—		I_C = 5.0A, V_{CC} = 960V
$t_{d(off)}$	Turn-Off Delay Time	—	100	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	620	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.7	—	mJ	See Fig. 10,11,14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Between lead and center of die contact
C_{ies}	Input Capacitance	—	435	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	44	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	8.3	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G =50Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

* When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

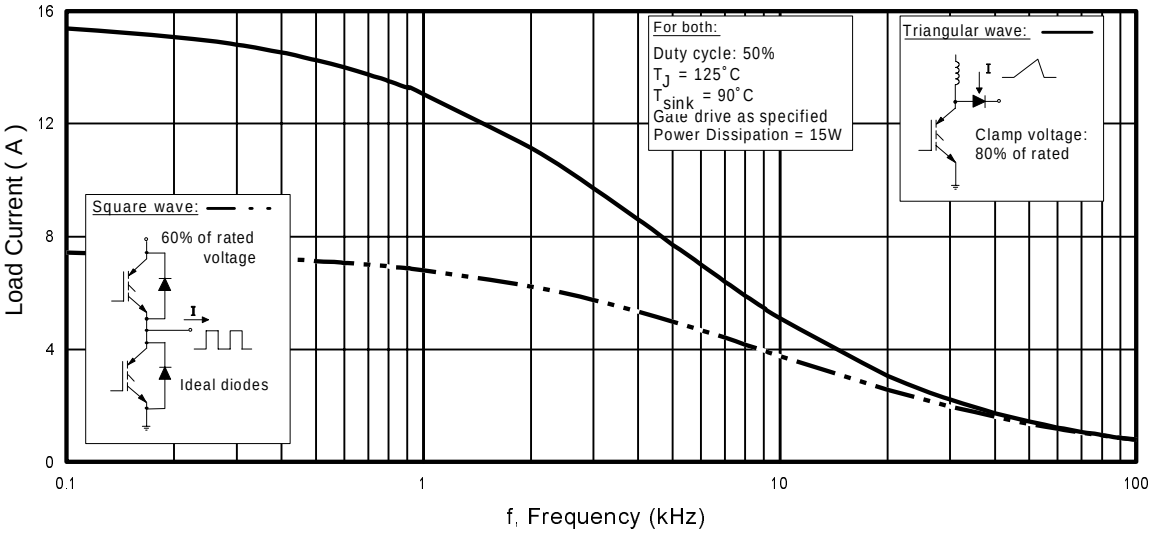


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

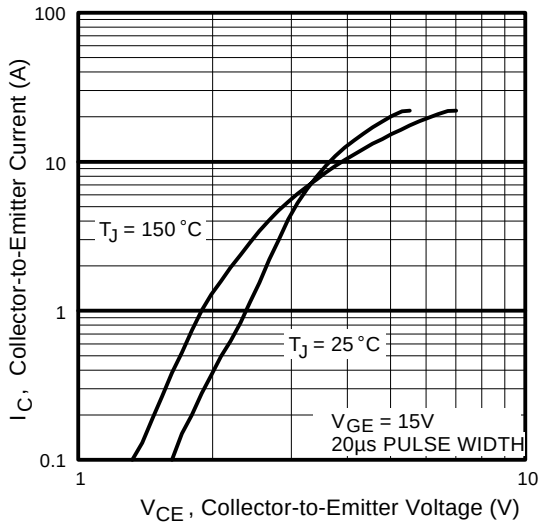


Fig. 2 - Typical Output Characteristics

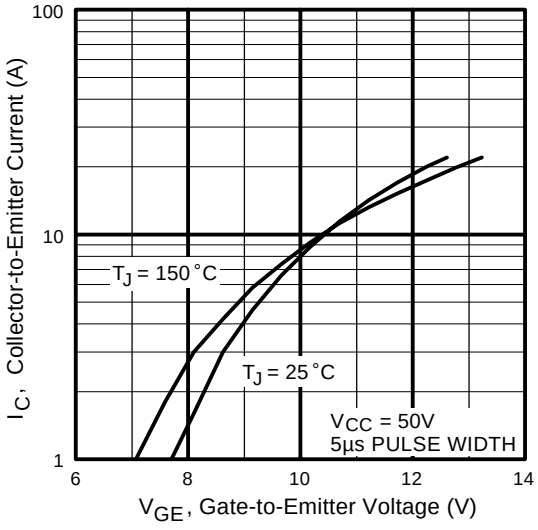


Fig. 3 - Typical Transfer Characteristics

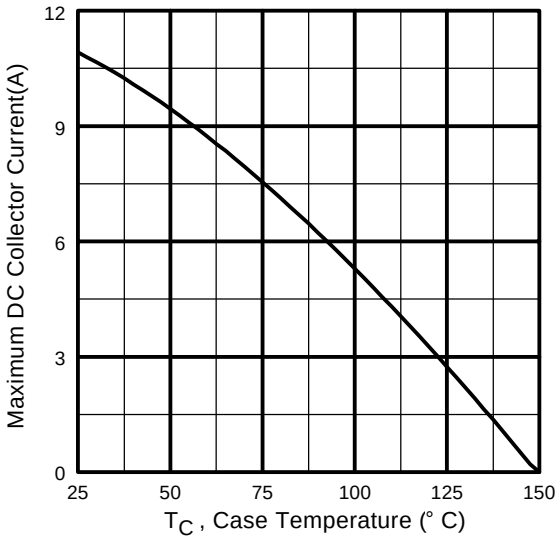


Fig. 4 - Maximum Collector Current vs. Case Temperature

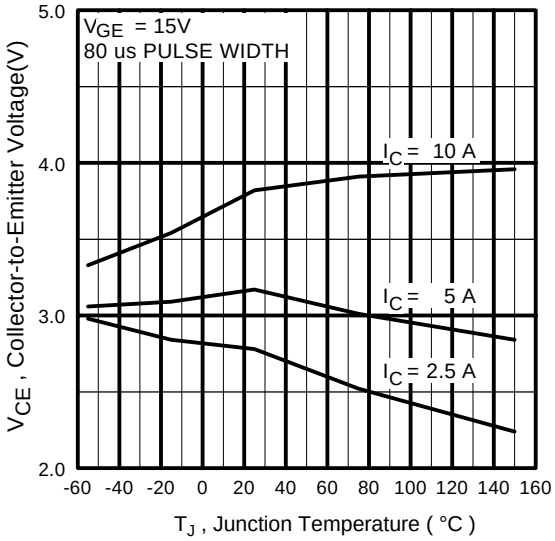


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

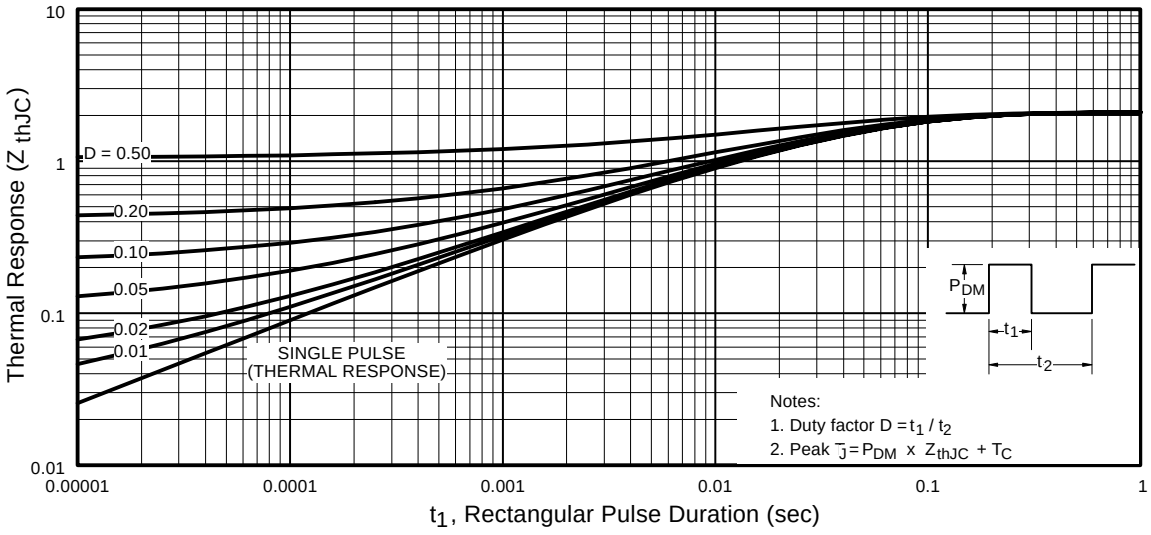


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

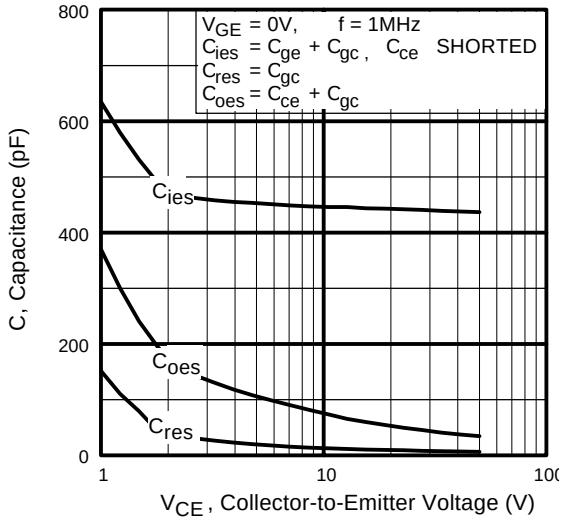


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

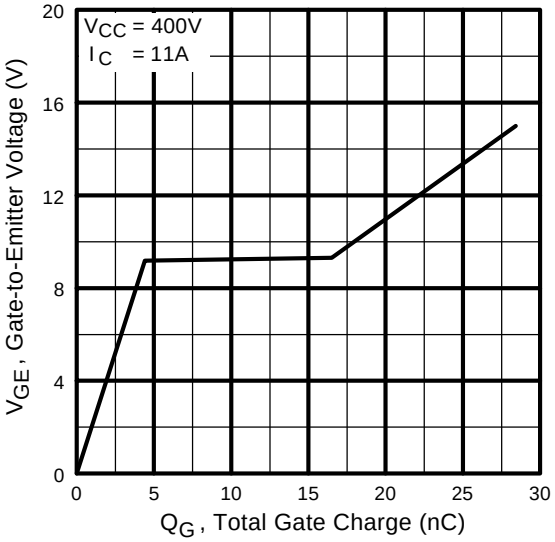


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

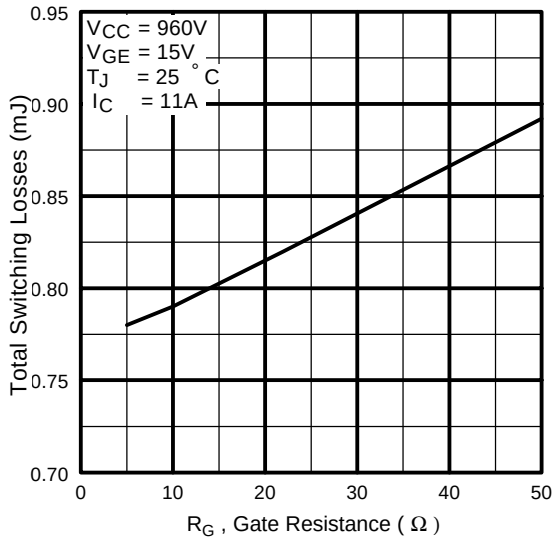


Fig. 9 - Typical Switching Losses vs. Gate Resistance

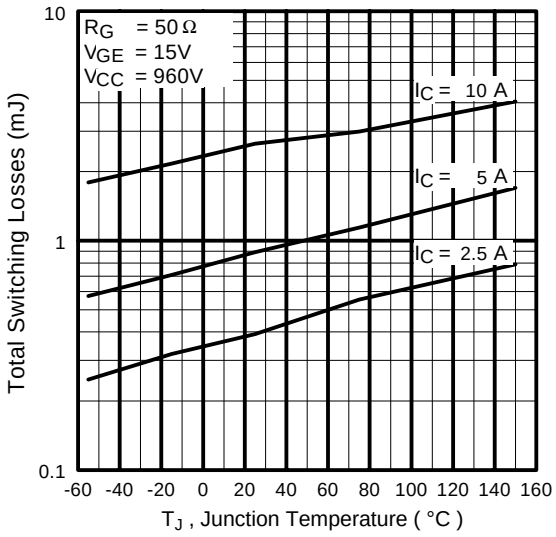


Fig. 10 - Typical Switching Losses vs. Junction Temperature

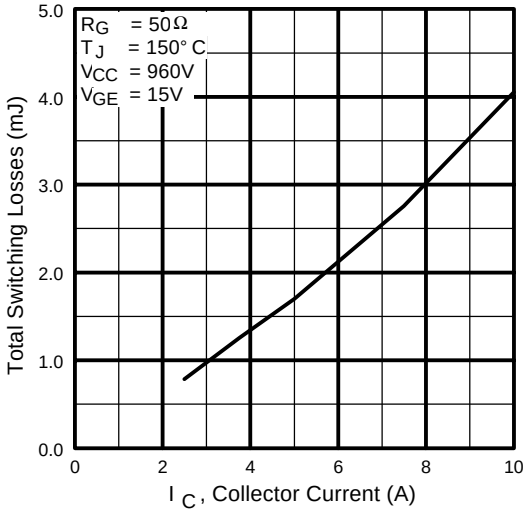


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

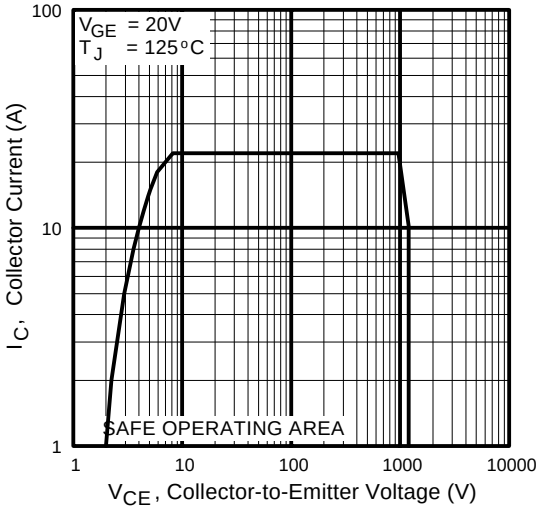


Fig. 12 - Turn-Off SOA

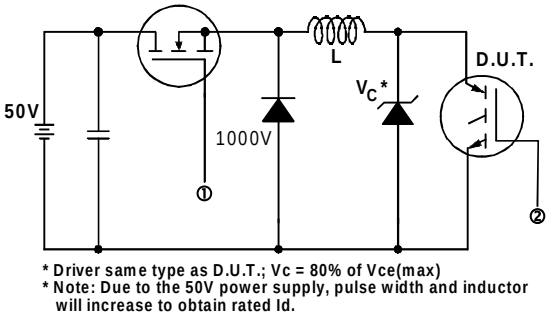


Fig. 13a - Clamped Inductive Load Test Circuit

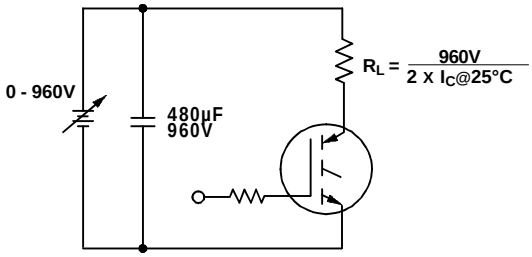


Fig. 13b - Pulsed Collector Current Test Circuit

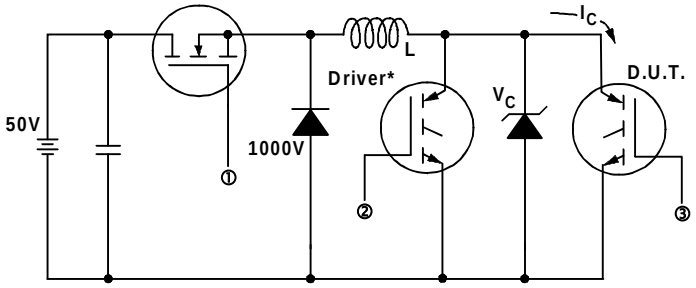


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 960V**

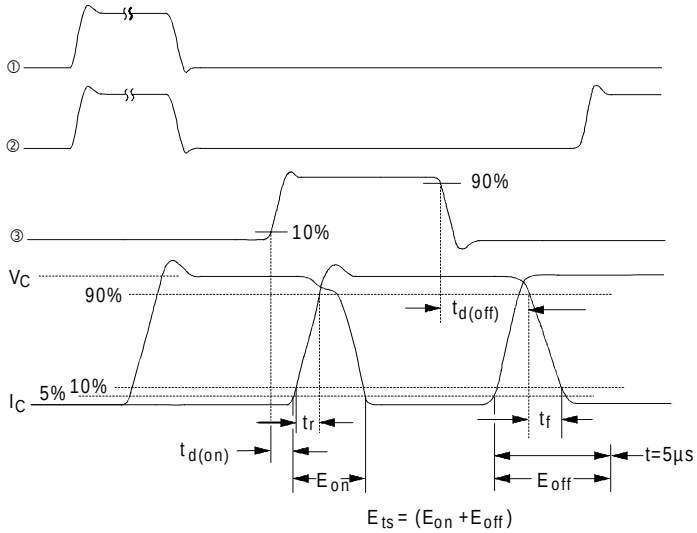
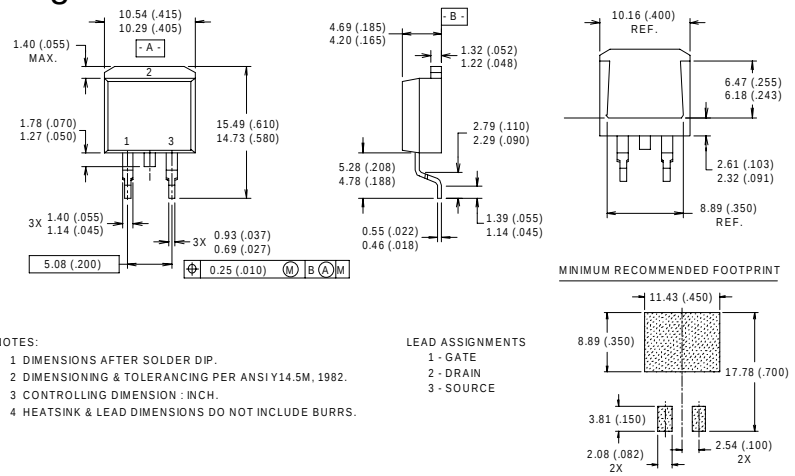


Fig. 14b - Switching Loss Waveforms

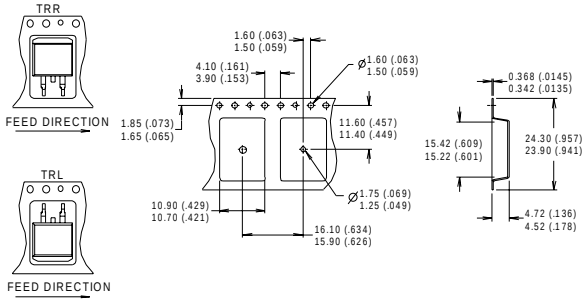
D²Pak Package Outline

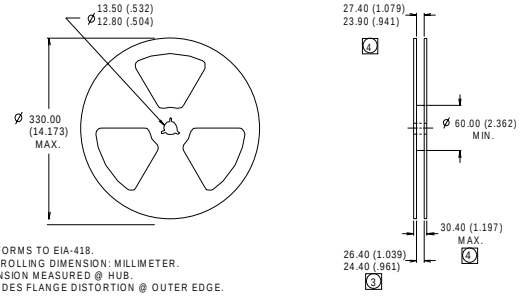


NOTES:
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

D²Pak Tape and Reel





NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
(4) DIMENSION MEASURED @ HUB.
(3) INCLUDES FLANGE DISTORTION @ OUTER EDGE.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTER: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN: 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

Data and specifications subject to change without notice. 8/00

International
IOR Rectifier

PD -91776

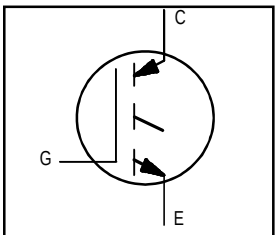
IRG4PH20K

INSULATED GATE BIPOLAR TRANSISTOR

Short Circuit Rated
UltraFast IGBT

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, V_{CC} = 720V , T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Latest generation design provides tighter parameter distribution and higher efficiency than previous generations



n-channel

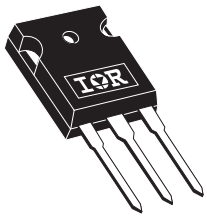
V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 3.17V

@V_{GE} = 15V, I_C = 5.0A

Benefits

- As a Freewheeling Diode we recommend our HEXFRED™ ultrafast, ultrasoft recovery diodes for minimum EMI / Noise and switching losses in the Diode and IGBT
- Latest generation 4 IGBT's offer highest power density motor controls possible



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	11	A
I_C @ T_C = 100°C	Continuous Collector Current	5.0	
I_{CM}	Pulsed Collector Current ①	22	
I_{LM}	Clamped Inductive Load Current ②	22	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	130	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	2.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	40	
Wt	Weight	6 (0.21)	——	g (oz)

6/25/98

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.13	—	V/°C	V_{GE} = 0V, I_C = 2.5mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	3.17	4.3	V	I_C = 5.0A V_{GE} = 15V
		—	4.04	—		I_C = 11A See Fig.2, 5
		—	2.84	—		I_C = 5.0A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.5	—	6.5		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 1mA
g_{fe}	Forward Transconductance ⑤	2.3	3.5	—	S	V_{CE} = 100 V, I_C = 5.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	28	43	nC	I_C = 5.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	4.4	6.6		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	12	18		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	
t_r	Rise Time	—	26	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	93	140		I_C =5.0A, V_{CC} = 960V
t_f	Fall Time	—	270	400		V_{GE} = 15V, R_G = 50Ω
E_{on}	Turn-On Switching Loss	—	0.45	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.44	—		See Fig. 9,10,14
E_{ts}	Total Switching Loss	—	0.89	1.2		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 720V, T_J = 125°C
						V_{GE} = 15V, R_G = 50Ω
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	T_J = 150°C,
t_r	Rise Time	—	28	—		I_C = 5.0A, V_{CC} = 960
$t_{d(off)}$	Turn-Off Delay Time	—	100	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	620	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.7	—	mJ	See Fig. 10,11,14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	435	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	44	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	8.3	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G =50Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

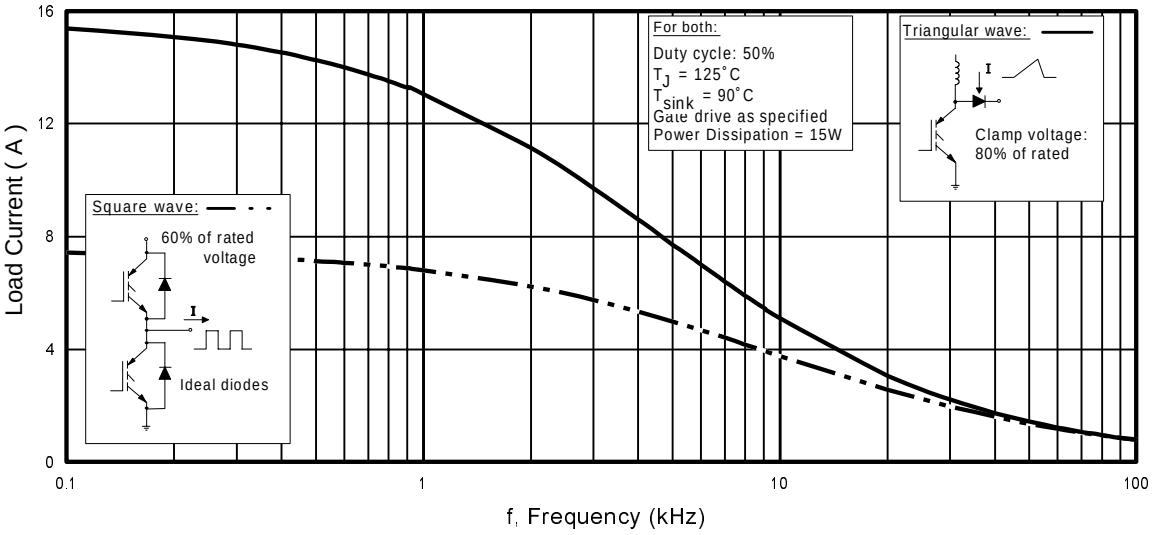


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

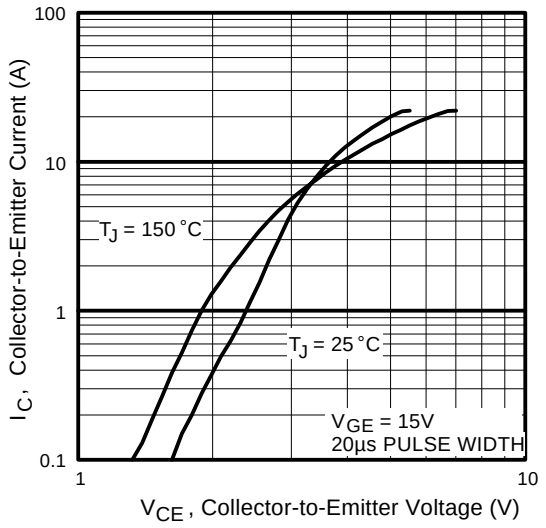


Fig. 2 - Typical Output Characteristics

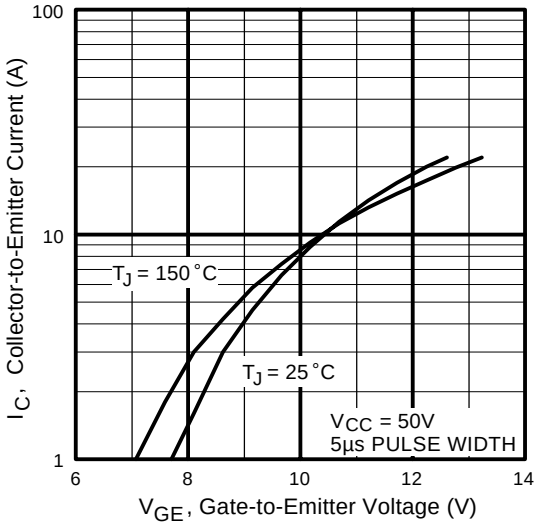


Fig. 3 - Typical Transfer Characteristics

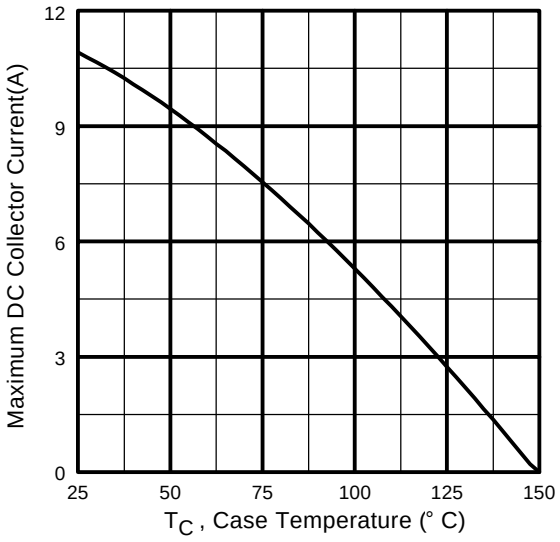


Fig. 4 - Maximum Collector Current vs. Case Temperature

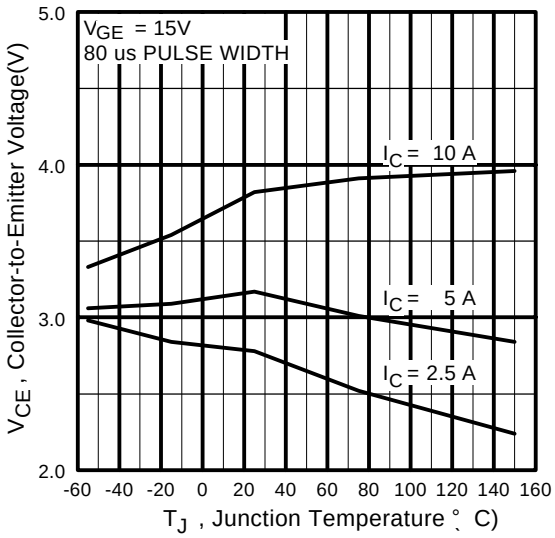


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

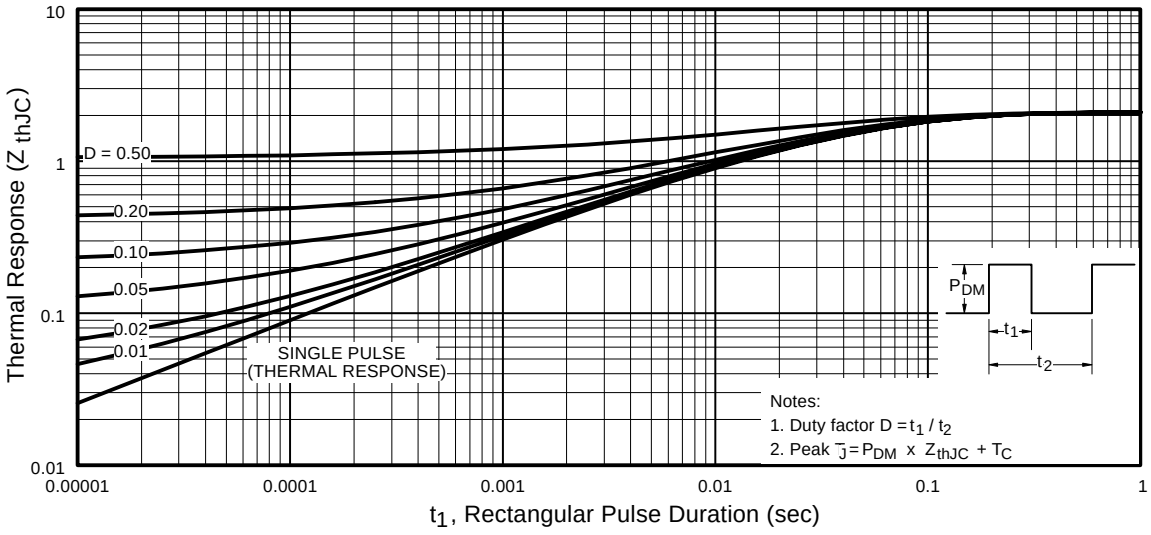


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

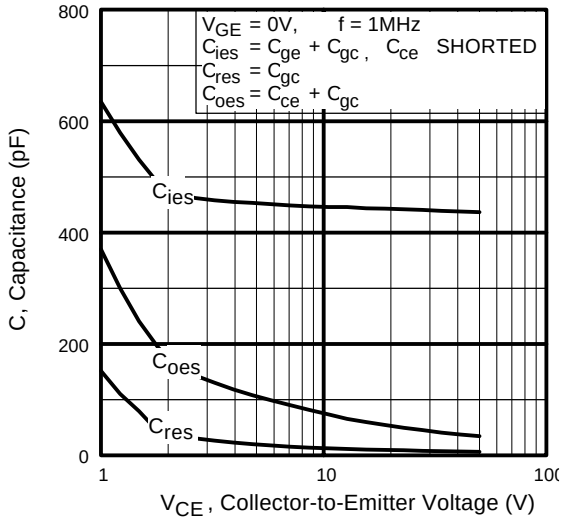


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

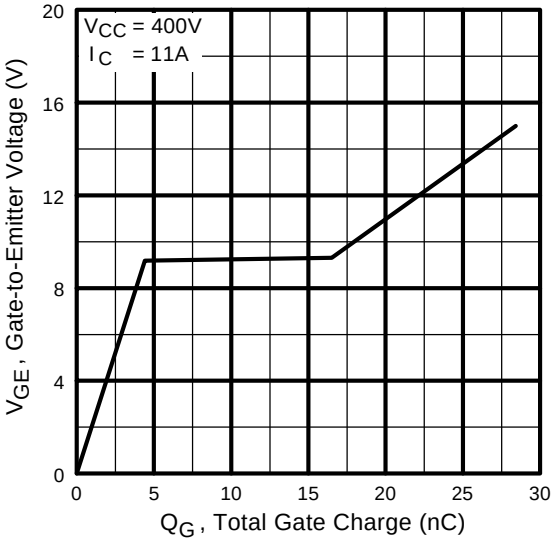


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

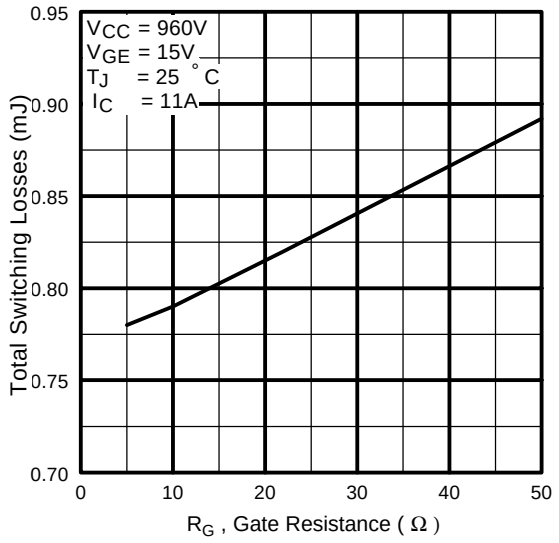


Fig. 9 - Typical Switching Losses vs. Gate Resistance

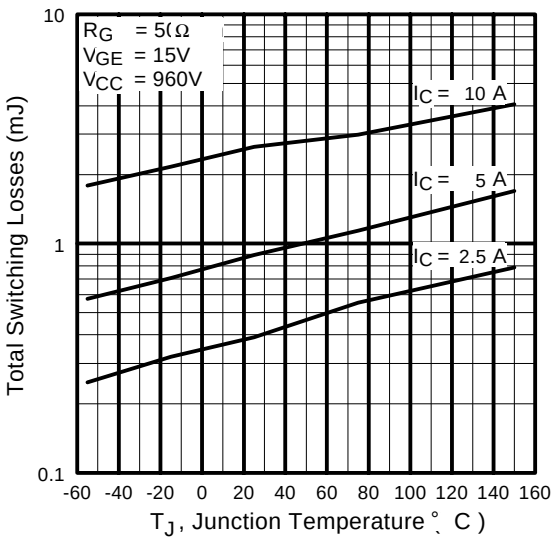


Fig. 10 - Typical Switching Losses vs. Junction Temperature

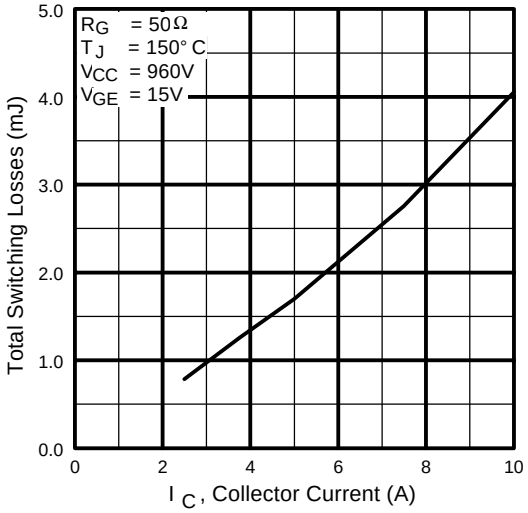


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

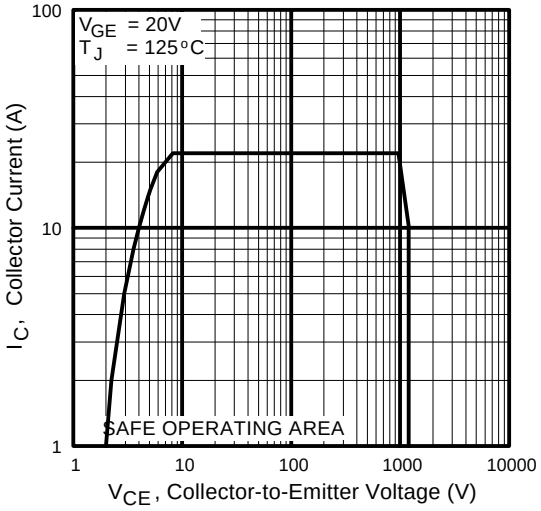


Fig. 12 - Turn-Off SOA

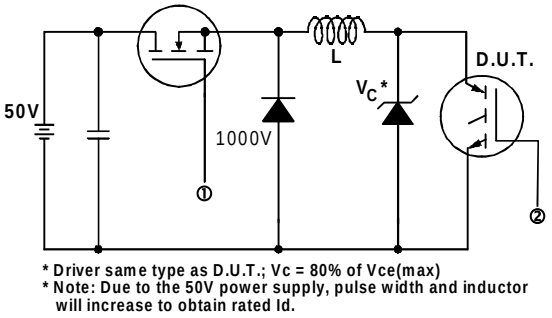


Fig. 13a - Clamped Inductive Load Test Circuit

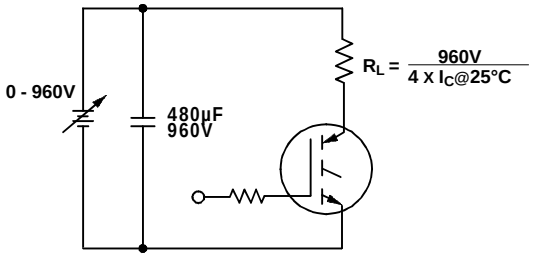


Fig. 13b - Pulsed Collector Current Test Circuit

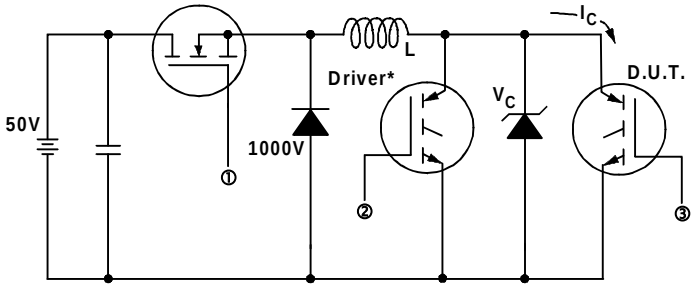


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 960V**

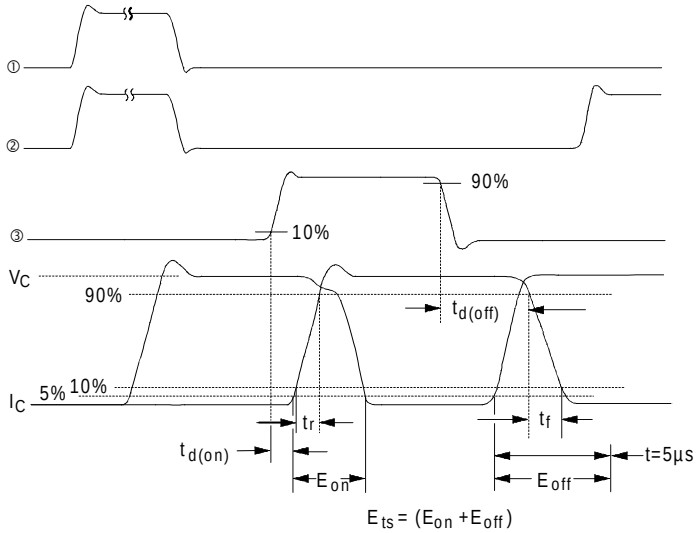
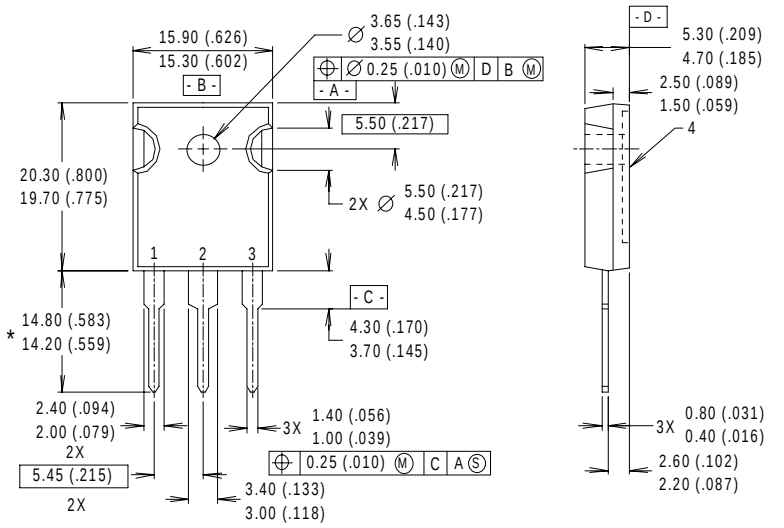


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371
http://www.irf.com/ Data and specifications subject to change without notice.6/98

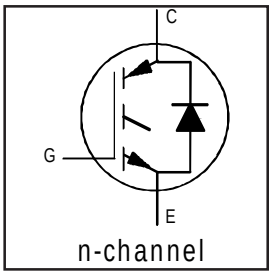
International
IOR Rectifier

PD- 91777

IRG4PH20KD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
UltraFast IGBT



n-channel

V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 3.17V

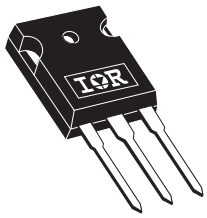
@V_{GE} = 15V, I_C = 5.0A

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, V_{CC} = 720V , T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Tighter parameter distribution and higher efficiency than previous generations
- IGBT co-packaged with HEXFRED™ ultrafast, ultrasoft recovery antiparallel diodes

Benefits

- Latest generation 4 IGBT's offer highest power density motor controls possible
- HEXFRED™ diodes optimized for performance with IGBTs. Minimized recovery characteristics reduce noise, EMI and switching losses



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	11	A
I_C @ T_C = 100°C	Continuous Collector Current	5.0	
I_{CM}	Pulsed Collector Current ①	22	
I_{LM}	Clamped Inductive Load Current ②	22	
I_F @ T_C = 100°C	Diode Continuous Forward Current	5.0	
I_{FM}	Diode Maximum Forward Current	22	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	——	——	2.1	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	——	——	3.5	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	——	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	——	40	
Wt	Weight	——	6 (0.21)	——	g (oz)

6/25/98

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.13	—	V/°C	V_{GE} = 0V, I_C = 2.5mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	3.17	4.3	V	I_C = 5.0A V_{GE} = 15V
		—	4.04	—		I_C = 11A See Fig. 2, 5
		—	2.84	—		I_C = 5.0A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.5	—	6.5		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 1mA
g_{fe}	Forward Transconductance ④	2.3	3.5	—	S	V_{CE} = 100V, I_C = 5.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	1000		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	2.5	2.9	V	I_C = 5.0A See Fig. 13
		—	2.2	2.6		I_C = 5.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	28	43	nC	I_C = 5.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	4.4	6.6		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	12	18		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	50	—	ns	
t_r	Rise Time	—	30	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	100	150		I_C = 5.0A, V_{CC} = 800V
t_f	Fall Time	—	250	380		V_{GE} = 15V, R_G = 50Ω
E_{on}	Turn-On Switching Loss	—	0.62	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.30	—		and diode reverse recovery
E_{ts}	Total Switching Loss	—	0.92	1.2		See Fig. 9,10,18
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 720V, T_J = 125°C
						V_{GE} = 15V, R_G = 50Ω
$t_{d(on)}$	Turn-On Delay Time	—	50	—	ns	T_J = 150°C, See Fig. 10,11,18
t_r	Rise Time	—	30	—		I_C = 5.0A, V_{CC} = 800V
$t_{d(off)}$	Turn-Off Delay Time	—	110	—		V_{GE} = 15V, R_G = 50Ω,
t_f	Fall Time	—	620	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.6	—	mJ	and diode reverse recovery
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	435	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	44	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	8.3	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	51	77	ns	T_J = 25°C See Fig.
		—	68	102		T_J = 125°C 14 I_F = 5.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	6.0	9.0	A	T_J = 25°C See Fig.
		—	7.0	11		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	183	274	nC	T_J = 25°C See Fig.
		—	285	427		T_J = 125°C 16 di/dt = 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	380	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	307	—		T_J = 125°C 17

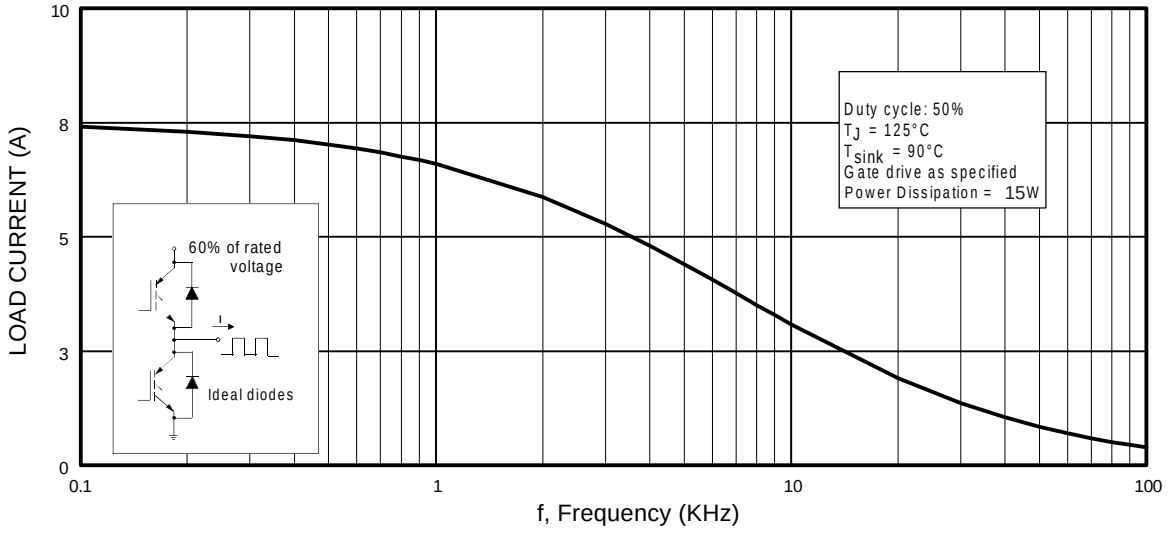


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

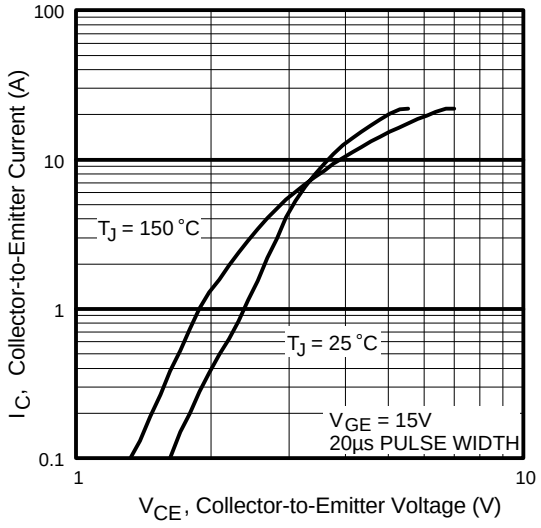


Fig. 2 - Typical Output Characteristics

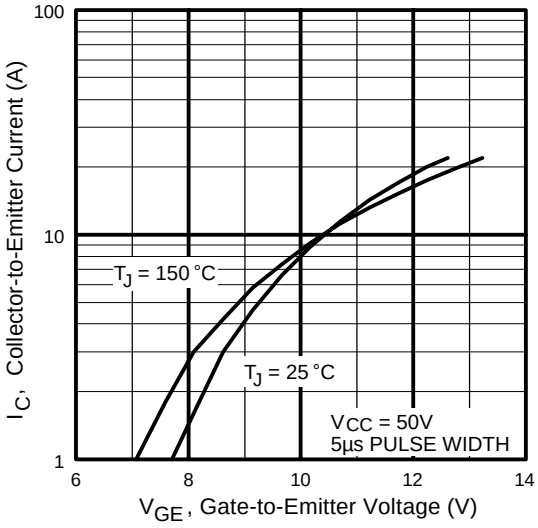


Fig. 3 - Typical Transfer Characteristics

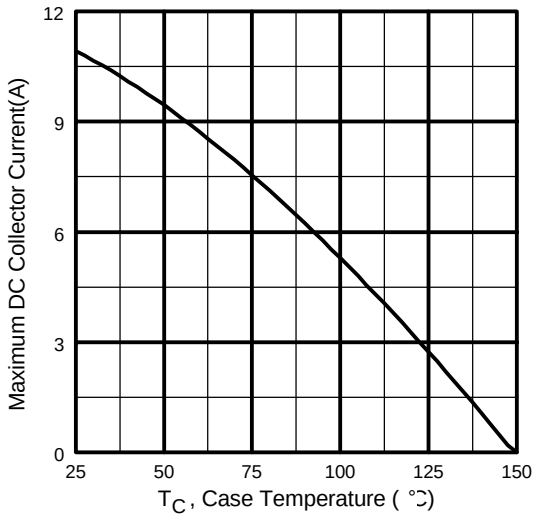


Fig. 4 - Maximum Collector Current vs. Case Temperature

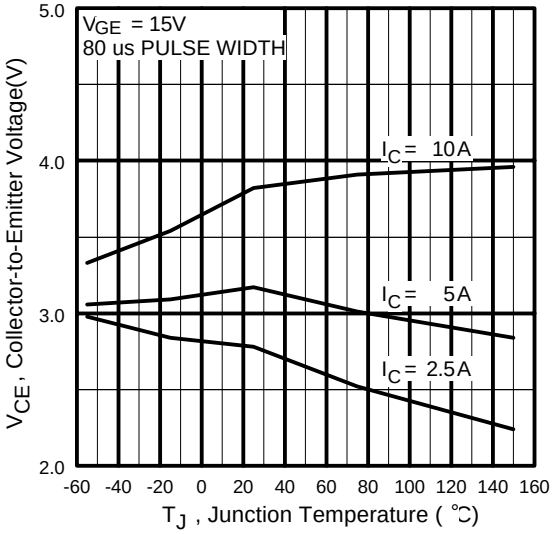


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

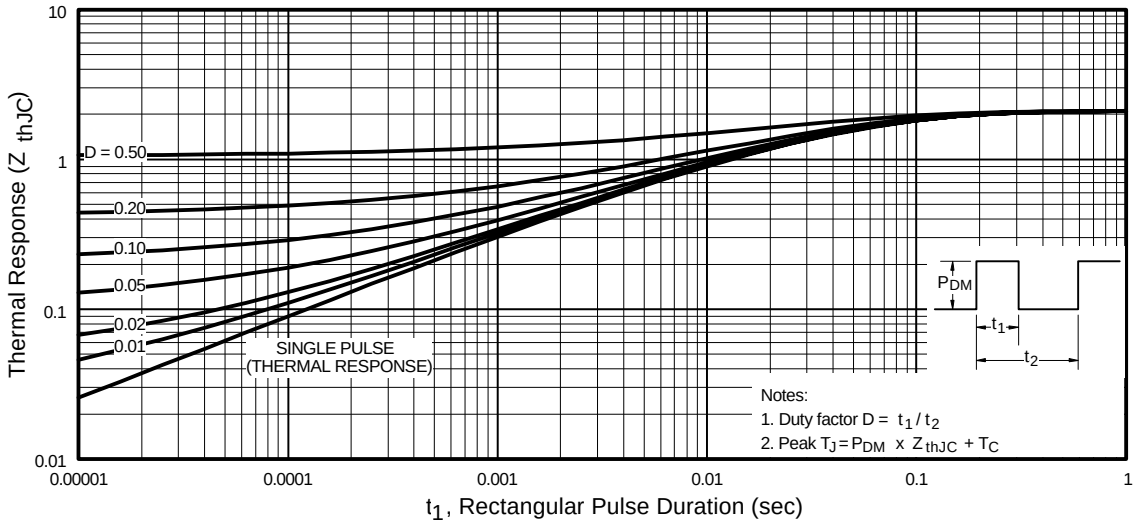


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

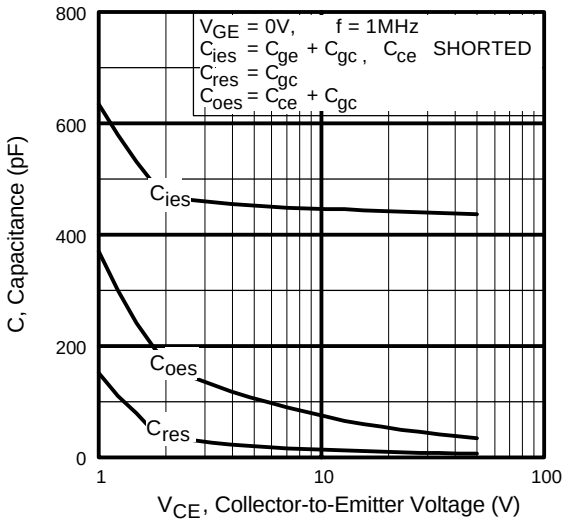


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

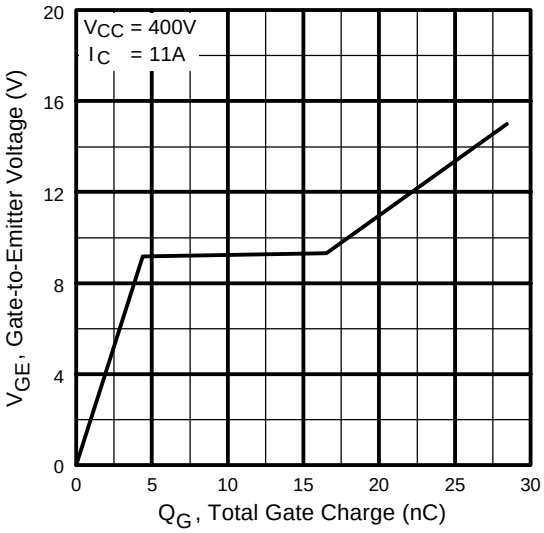


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

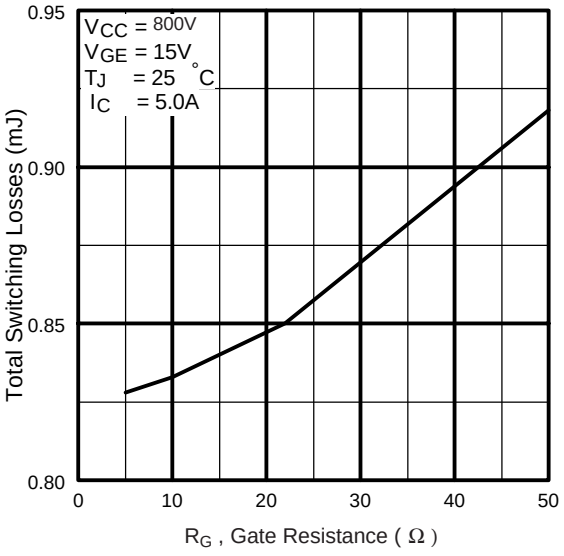


Fig. 9 - Typical Switching Losses vs. Gate Resistance

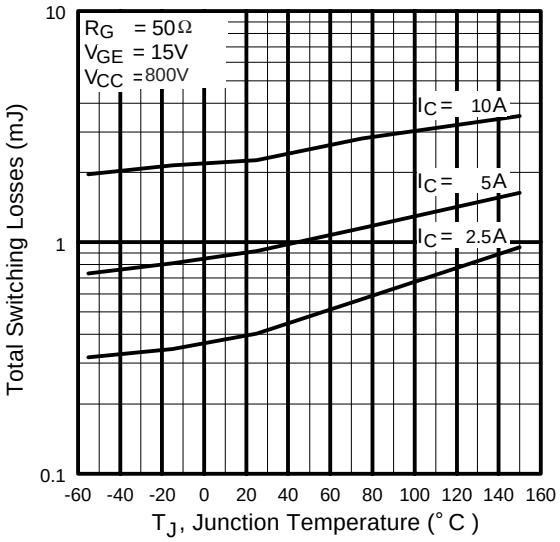


Fig. 10 - Typical Switching Losses vs. Junction Temperature

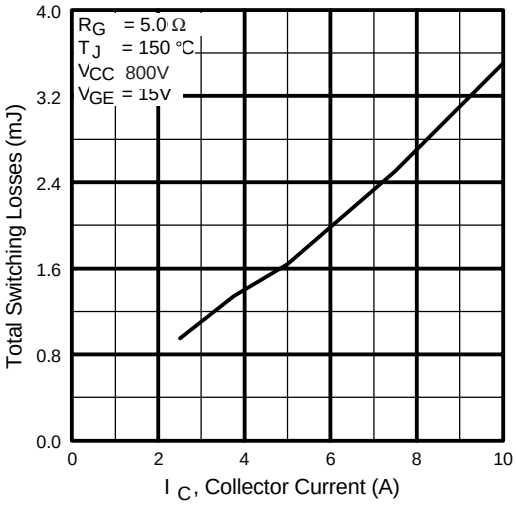


Fig. 11 - Typical Switching Losses vs. Collector Current

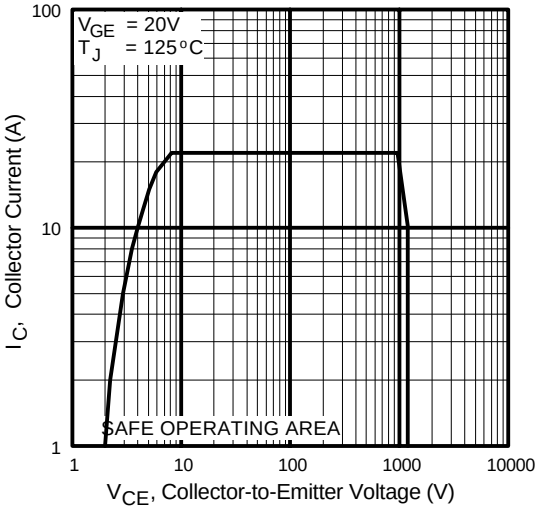


Fig. 12 - Turn-Off SOA

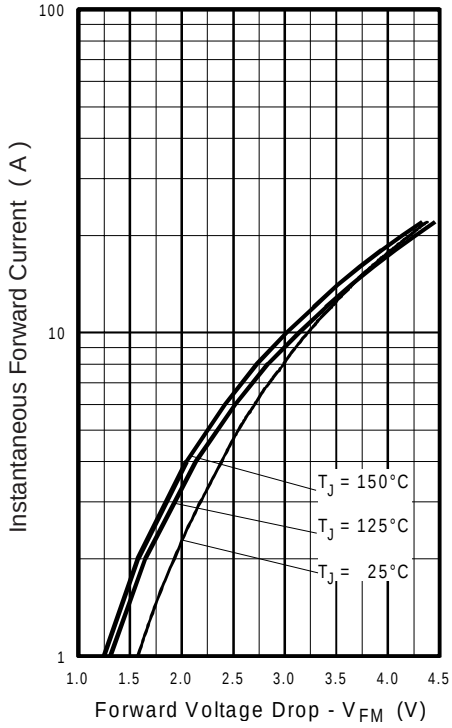


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

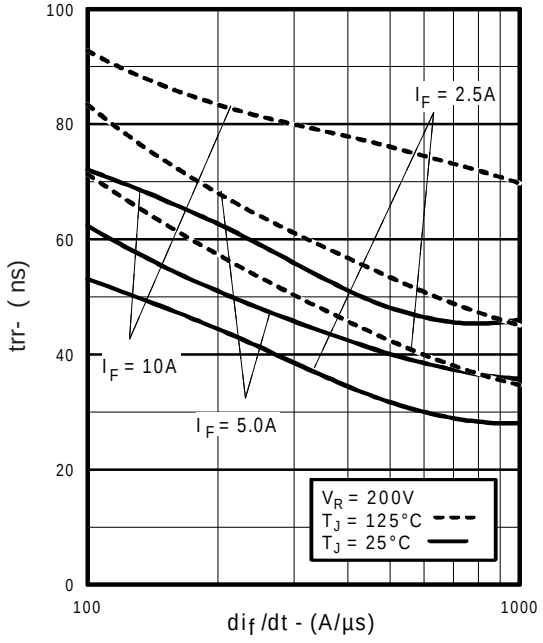


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

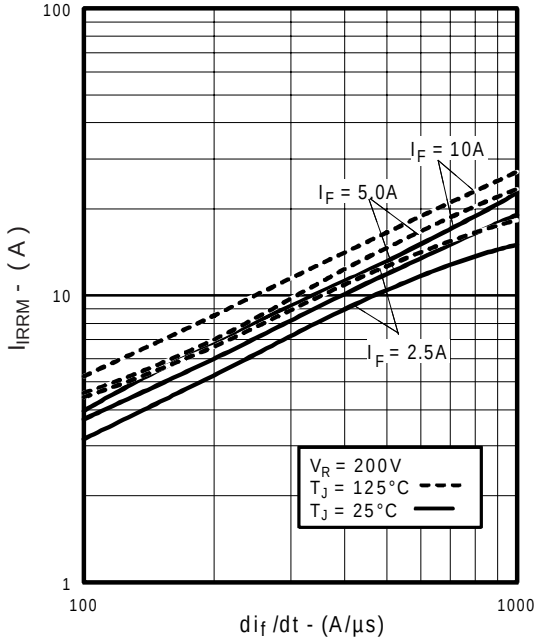


Fig. 15 - Typical Recovery Current vs. di_f/dt

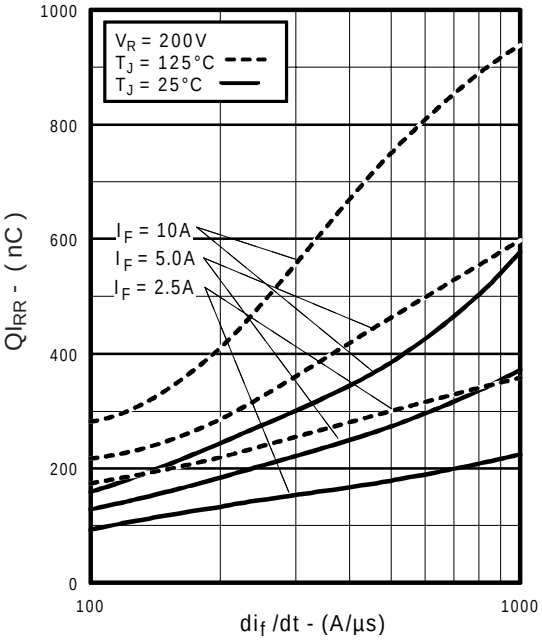


Fig. 16 - Typical Stored Charge vs. di_f/dt

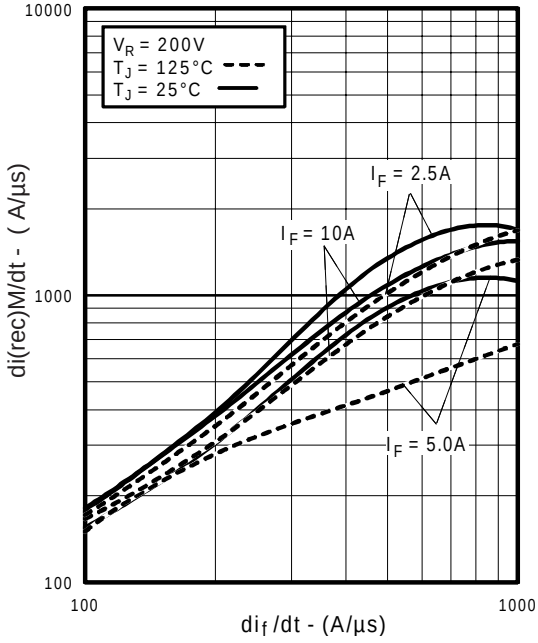


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

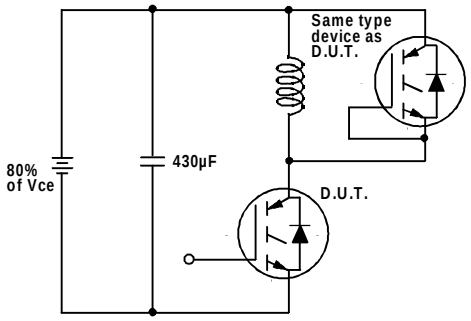


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

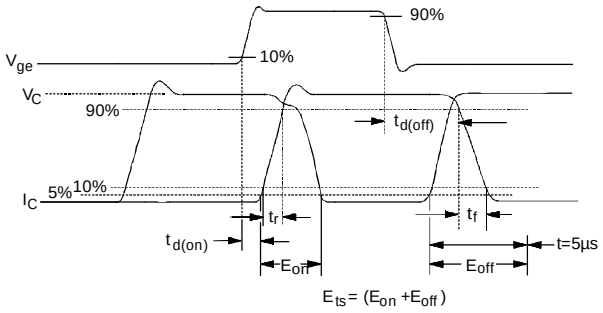


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

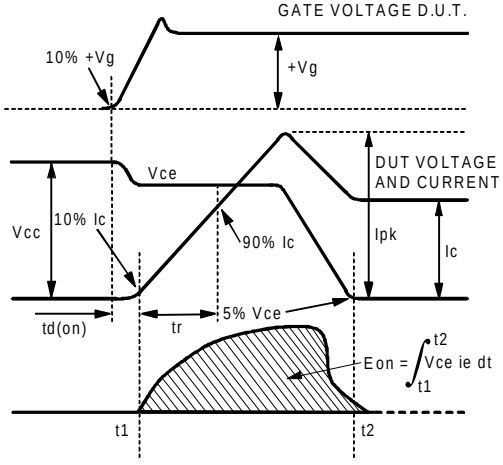


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

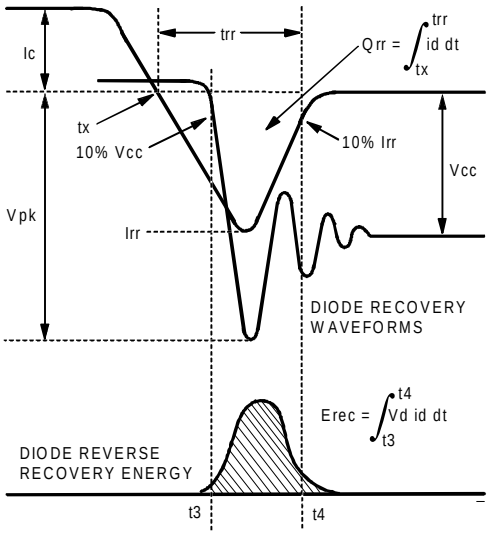


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

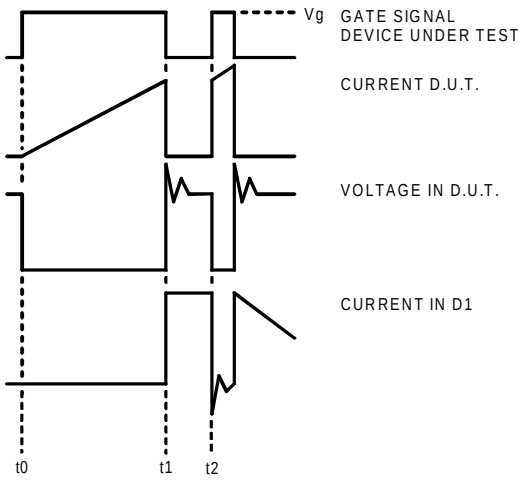


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

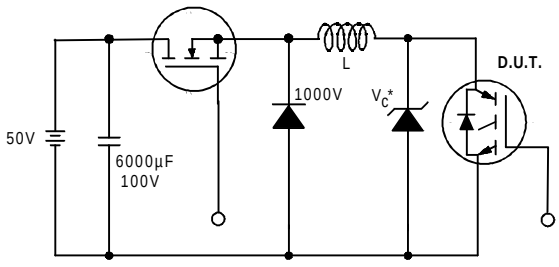


Figure 19. Clamped Inductive Load Test Circuit

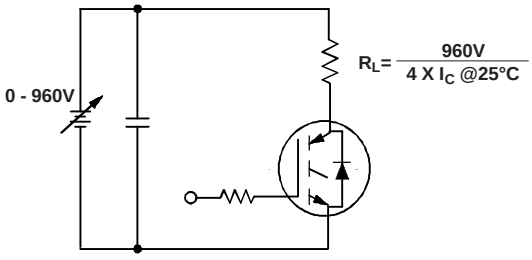


Figure 20. Pulsed Collector Current Test Circuit

Notes:

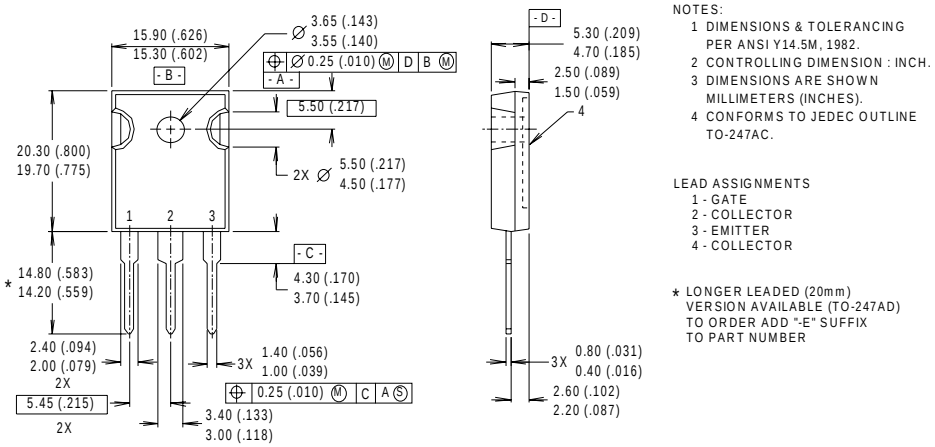
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 5.0Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline - TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371

International
IOR Rectifier

PD -93961

IRG4BH20K-L

INSULATED GATE BIPOLAR TRANSISTOR

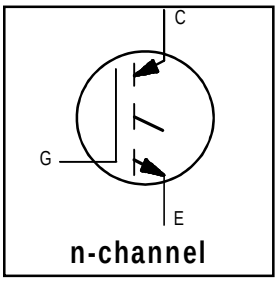
Short Circuit Rated
UltraFast IGBT

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, V_{CC} = 720V , T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Latest generation design provides tighter parameter distribution and higher efficiency than previous generations
- Industry standard TO-262 package

Benefits

- As a Freewheeling Diode we recommend our HEXFRED™ ultrafast, ultrasoft recovery diodes for minimum EMI / Noise and switching losses in the Diode and IGBT
- Latest generation 4 IGBT's offer highest power density motor controls possible



n-channel

V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 3.17V

@V_{GE} = 15V, I_C = 5.0A



TO-262

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	11	A
I_C @ T_C = 100°C	Continuous Collector Current	5.0	
I_{CM}	Pulsed Collector Current ①	22	
I_{LM}	Clamped Inductive Load Current ②	22	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	130	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

8/17/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.13	—	V/°C	V_{GE} = 0V, I_C = 2.5mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	3.17	4.3	V	I_C = 5.0A V_{GE} = 15V
		—	4.04	—		I_C = 11A See Fig.2, 5
		—	2.84	—		I_C = 5.0A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.5	—	6.5		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 1mA
g_{fe}	Forward Transconductance ⑤	2.3	3.5	—	S	V_{CE} = 100 V, I_C = 5.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	28	43	nC	I_C = 5.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	4.4	6.6		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	12	18		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	
t_r	Rise Time	—	26	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	93	140		I_C =5.0A, V_{CC} = 960V
t_f	Fall Time	—	270	400		V_{GE} = 15V, R_G = 50Ω
E_{on}	Turn-On Switching Loss	—	0.45	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.44	—		See Fig. 9,10,14
E_{ts}	Total Switching Loss	—	0.89	1.2		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 720V, T_J = 125°C
						V_{GE} = 15V, R_G = 50Ω
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	T_J = 150°C,
t_r	Rise Time	—	28	—		I_C = 5.0A, V_{CC} = 960V
$t_{d(off)}$	Turn-Off Delay Time	—	100	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	620	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.7	—	mJ	See Fig. 10,11,14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	435	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	44	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	8.3	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G =50Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

* When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

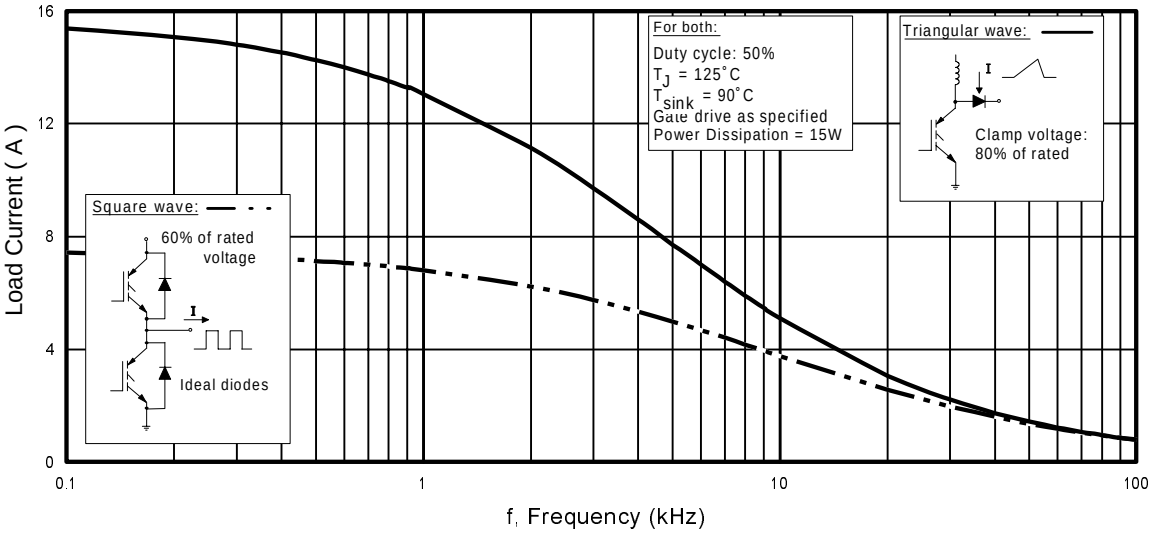


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

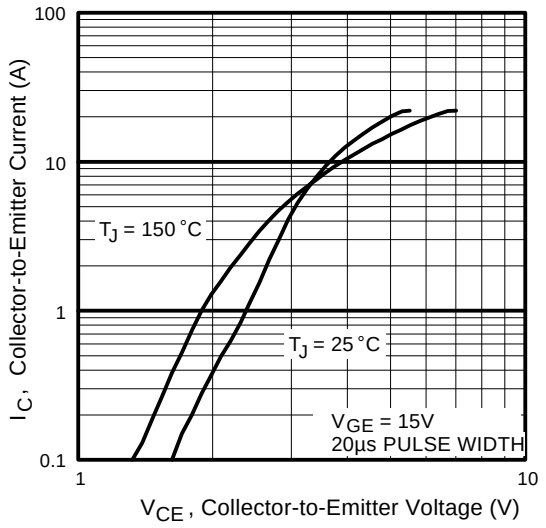


Fig. 2 - Typical Output Characteristics

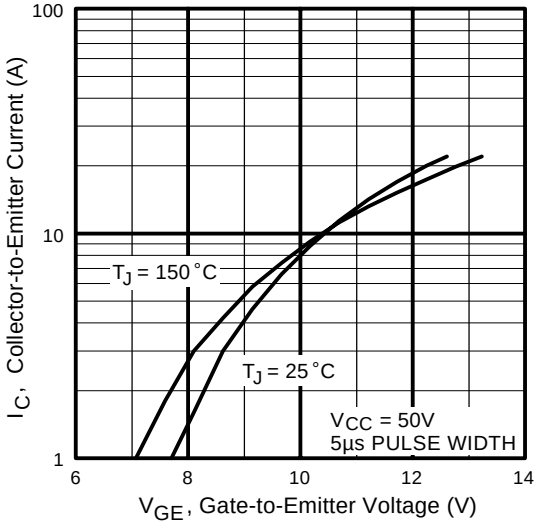


Fig. 3 - Typical Transfer Characteristics

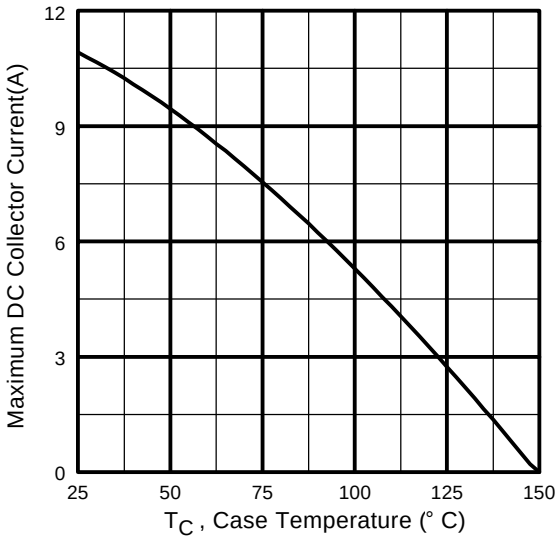


Fig. 4 - Maximum Collector Current vs. Case Temperature

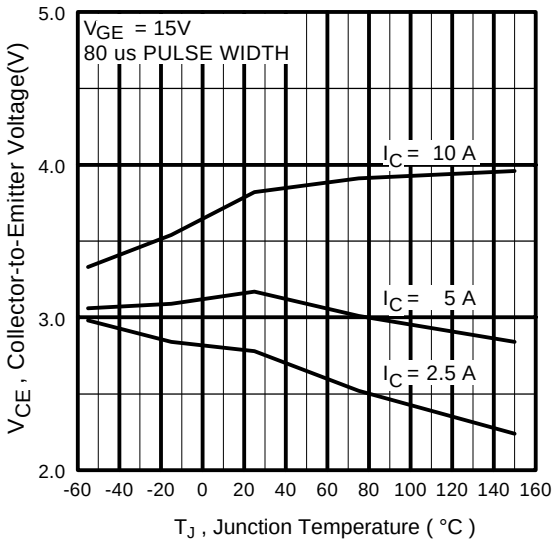


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

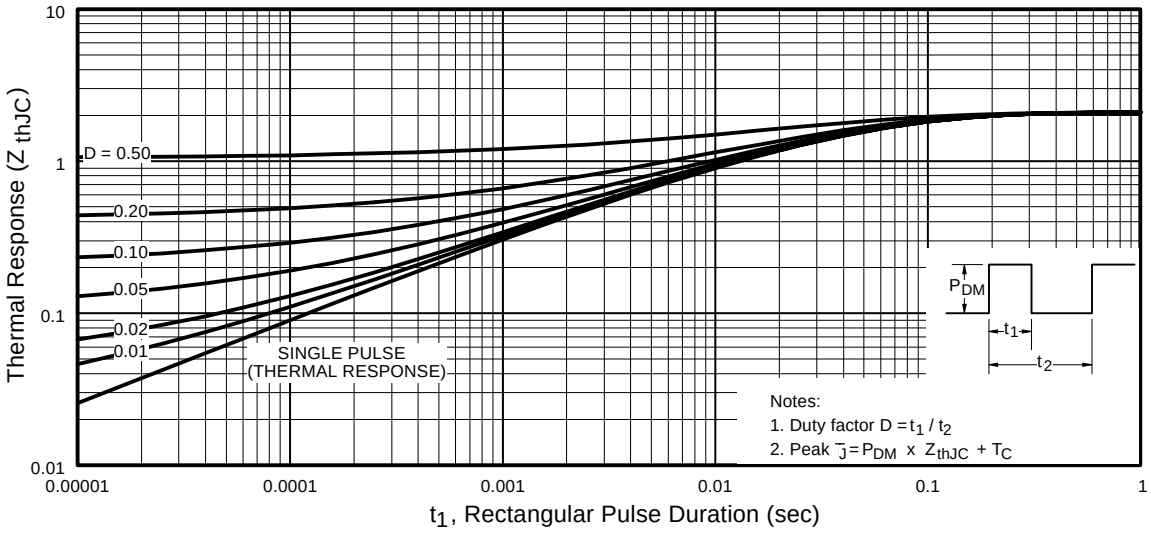


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

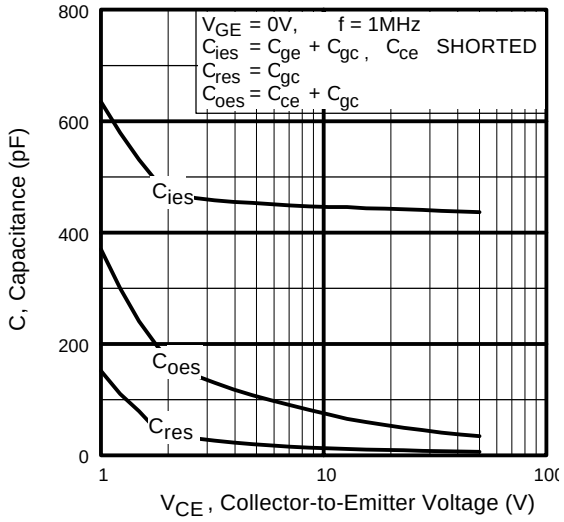


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

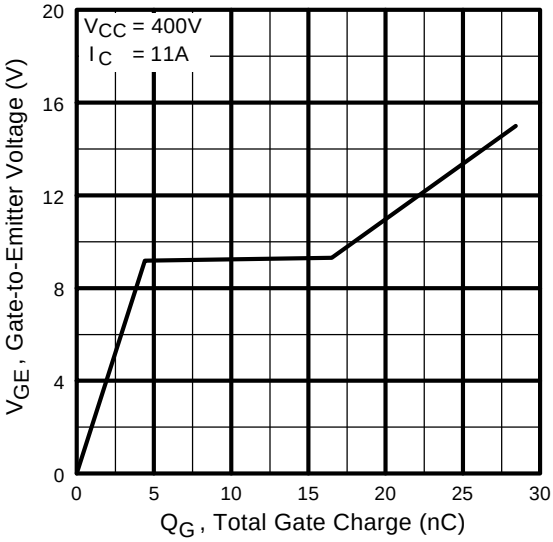


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

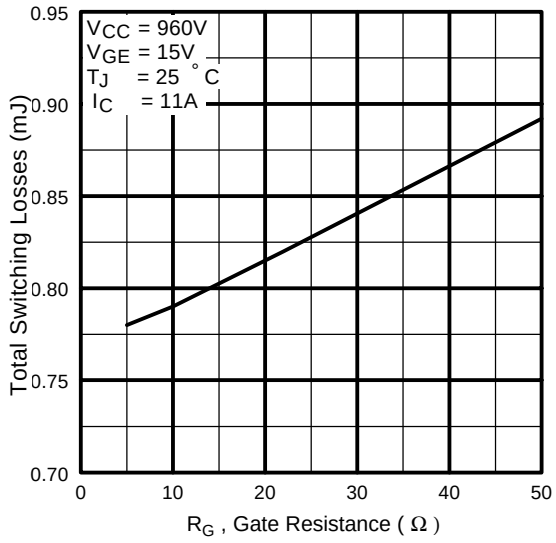


Fig. 9 - Typical Switching Losses vs. Gate Resistance

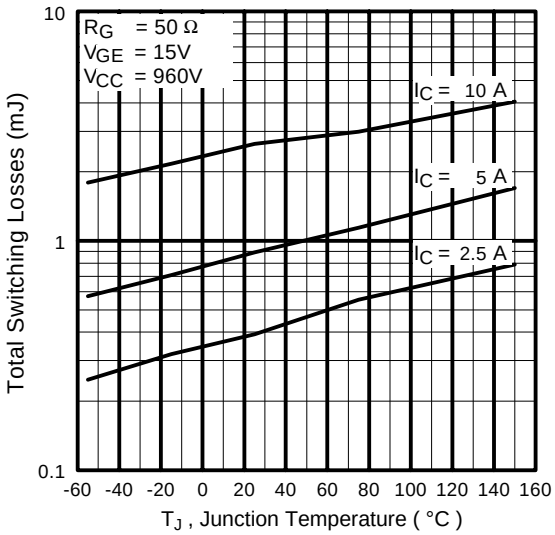


Fig. 10 - Typical Switching Losses vs. Junction Temperature

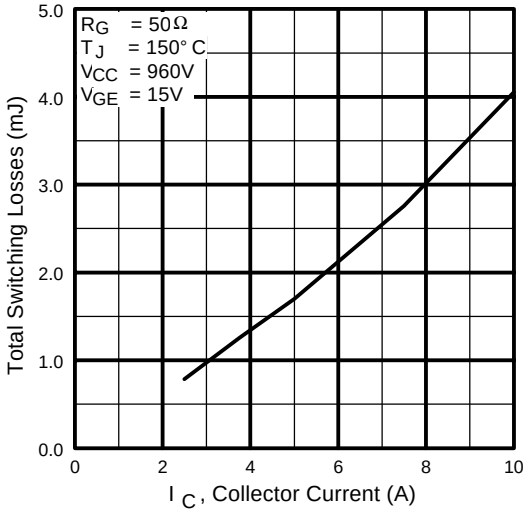


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

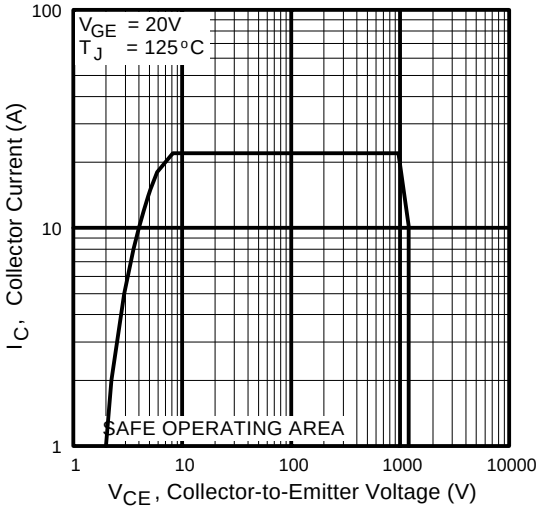


Fig. 12 - Turn-Off SOA

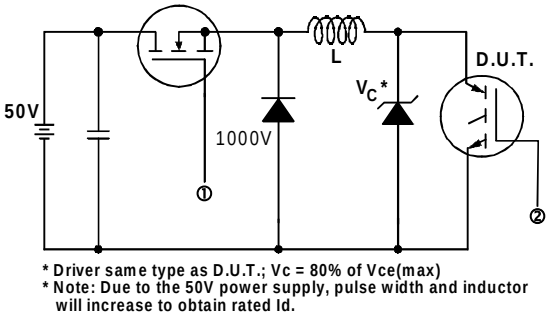


Fig. 13a - Clamped Inductive Load Test Circuit

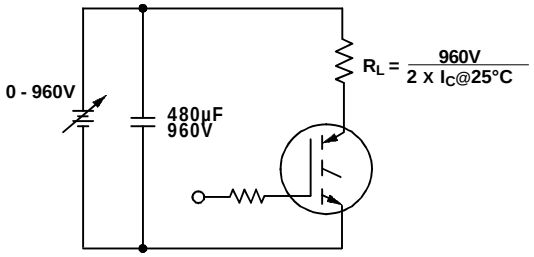


Fig. 13b - Pulsed Collector Current Test Circuit

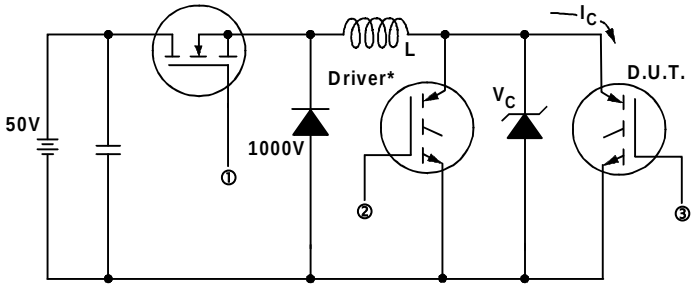


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 960V**

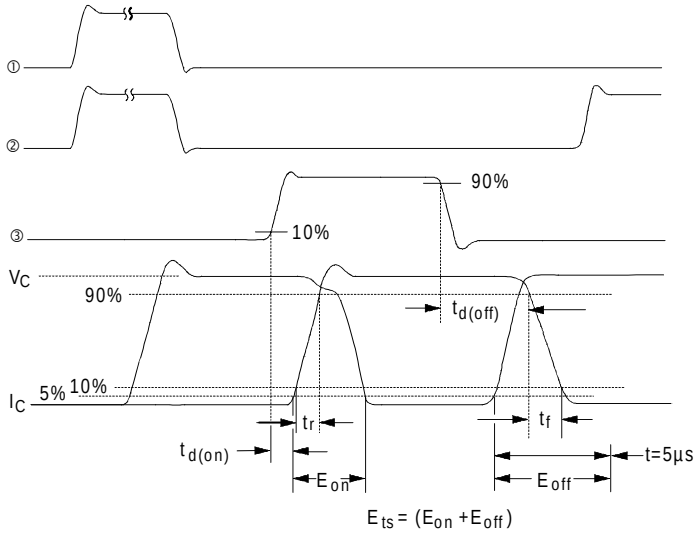
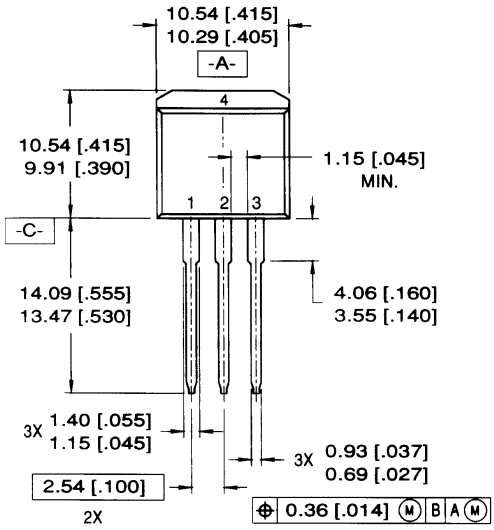


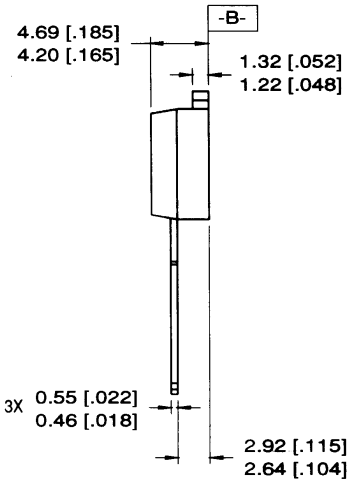
Fig. 14b - Switching Loss Waveforms

TO-262 Package Details



LEAD ASSIGNMENTS

1 = GATE 3 = SOURCE
2 = DRAIN 4 = DRAIN



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

Data and specifications subject to change without notice. 8/00

International
IOR Rectifier

PD -91580A

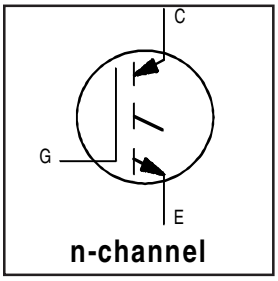
IRG4PH30K

INSULATED GATE BIPOLAR TRANSISTOR

Short Circuit Rated
UltraFast IGBT

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, V_{CC} = 720V , T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Latest generation design provides tighter parameter distribution and higher efficiency than previous generations



n-channel

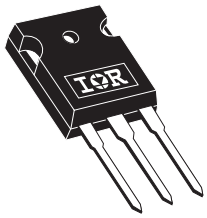
V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 3.10V

@V_{GE} = 15V, I_C = 10A

Benefits

- As a Freewheeling Diode we recommend our HEXFRED™ ultrafast, ultrasoft recovery diodes for minimum EMI / Noise and switching losses in the Diode and IGBT
- Latest generation 4 IGBT's offer highest power density motor controls possible
- This part replaces the IRGPH30K and IRGPH30M devices


TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	20	A
I_C @ T_C = 100°C	Continuous Collector Current	10	
I_{CM}	Pulsed Collector Current ①	40	
I_{LM}	Clamped Inductive Load Current ②	40	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	121	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

2/7/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.19	—	V/°C	V_{GE} = 0V, I_C = 2.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	3.10	4.2	V	I_C = 10A V_{GE} = 15V
		—	3.90	—		I_C = 20A See Fig.2, 5
		—	3.01	—		I_C = 10A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-12	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	4.3	6.5	—	S	V_{CE} = 100 V, I_C = 10A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	2000		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	53	80	nC	I_C = 10A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	9.0	14		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	21	32		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	28	—	ns	
t_r	Rise Time	—	23	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	200	300		I_C =10A, V_{CC} = 960V
t_f	Fall Time	—	110	170		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.64	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.92	—		See Fig. 9,10,14
E_{ts}	Total Switching Loss	—	1.56	2.4		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 720V, T_J = 125°C
						V_{GE} = 15V, R_G = 23Ω
$t_{d(on)}$	Turn-On Delay Time	—	27	—	ns	T_J = 150°C,
t_r	Rise Time	—	26	—		I_C = 10A, V_{CC} = 960V
$t_{d(off)}$	Turn-Off Delay Time	—	310	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	330	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	3.18	—	mJ	See Fig. 10,11,14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	800	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	60	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	14	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G =23Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

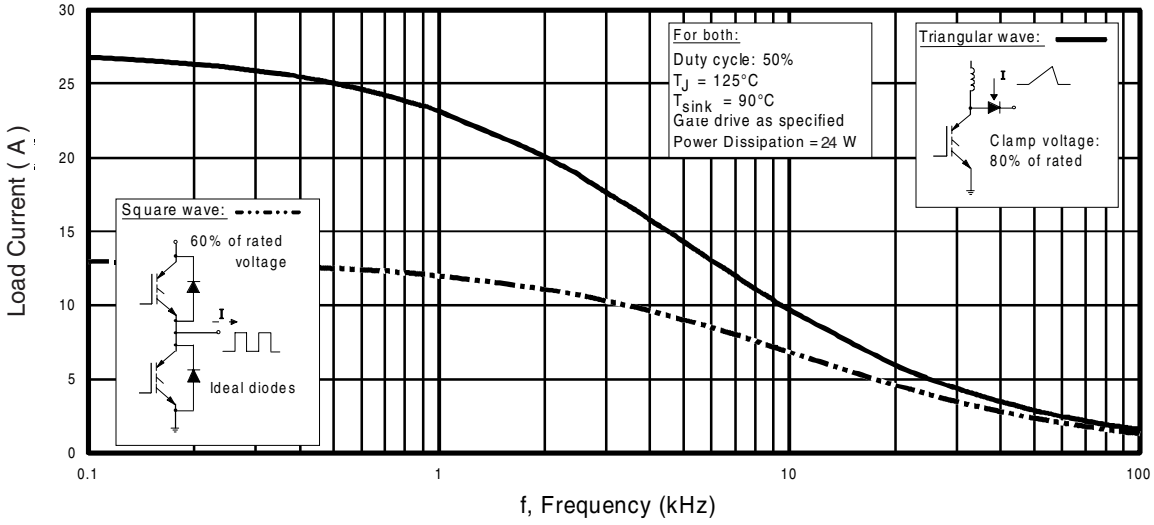


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

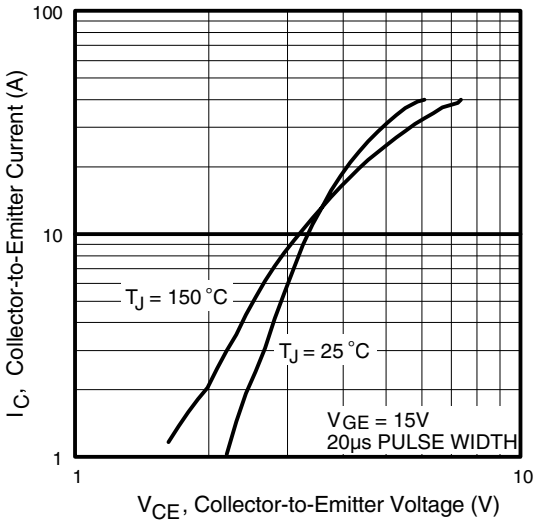


Fig. 2 - Typical Output Characteristics

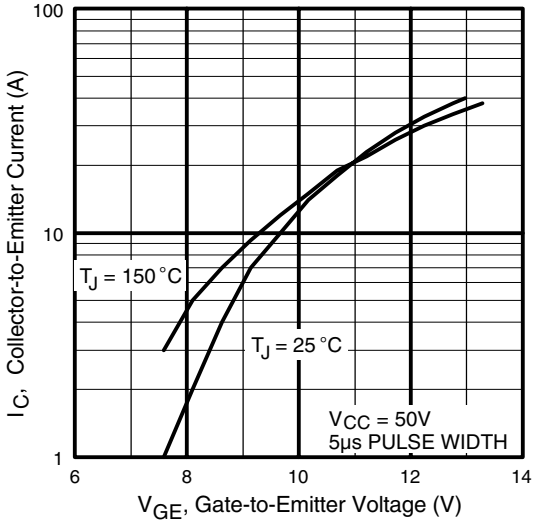


Fig. 3 - Typical Transfer Characteristics

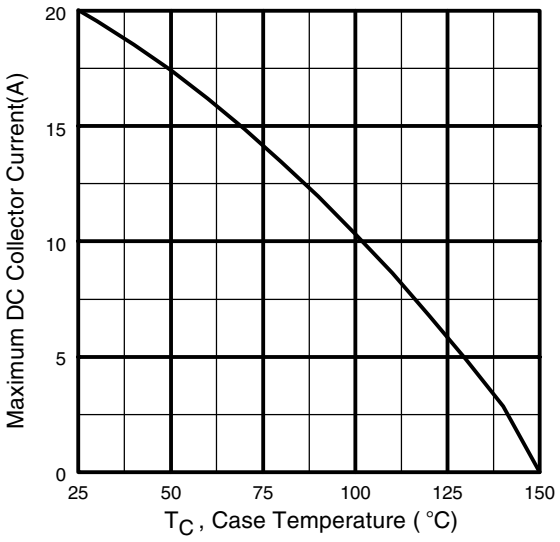


Fig. 4 - Maximum Collector Current vs. Case Temperature

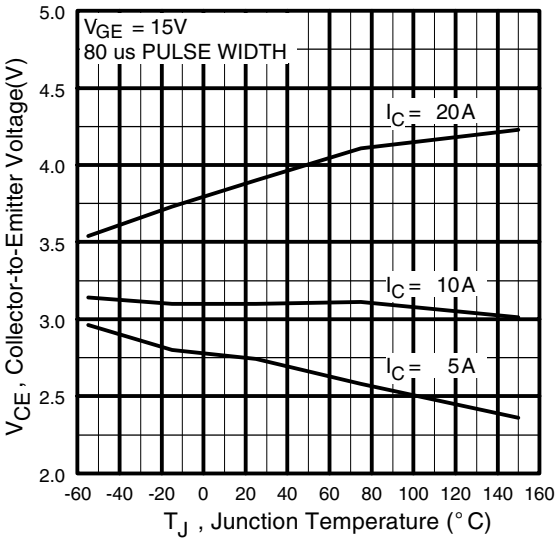


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

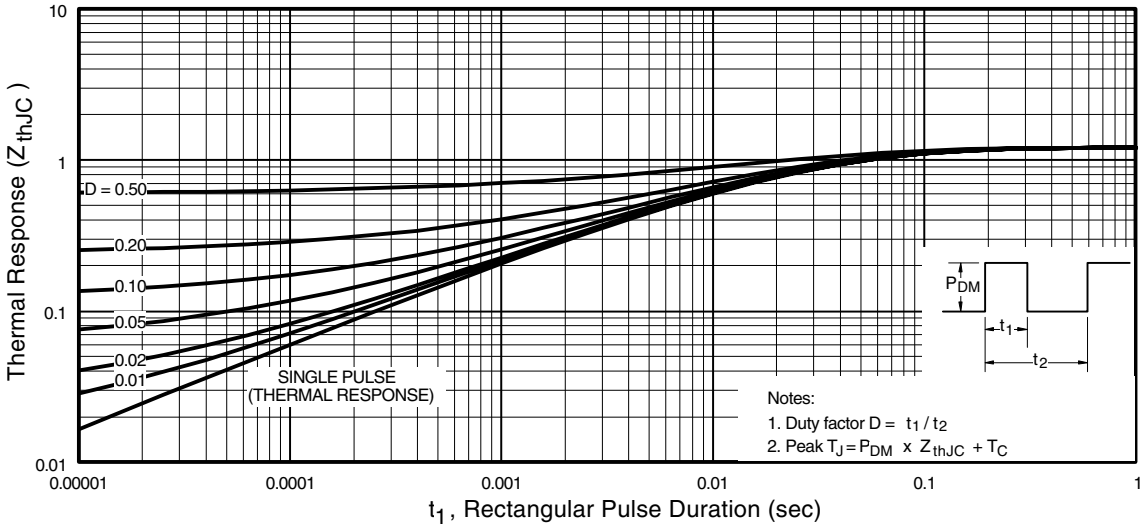


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

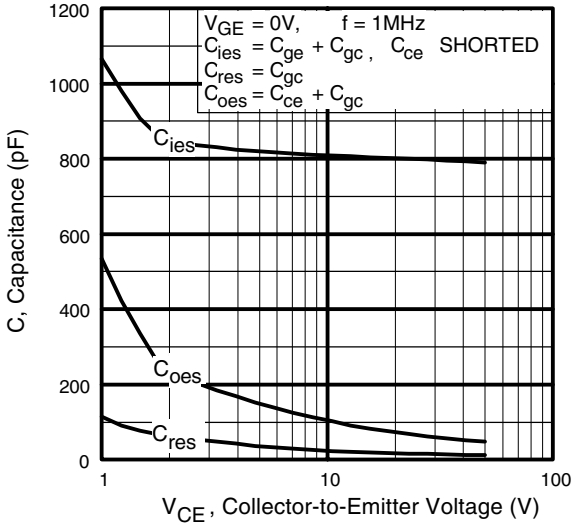


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

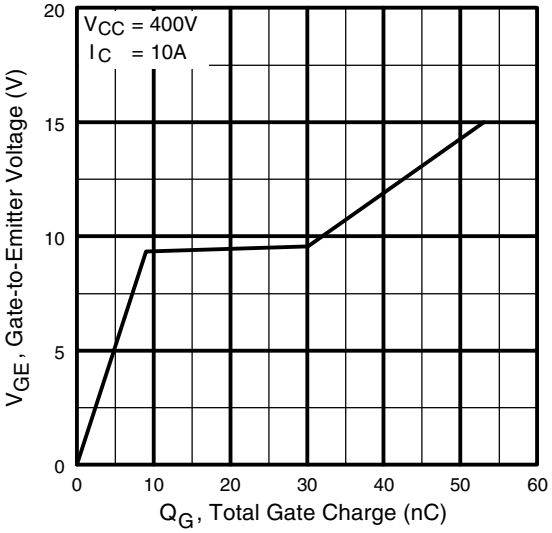


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

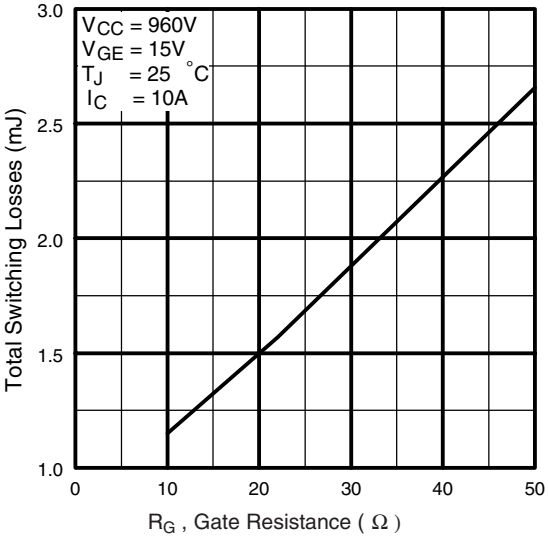


Fig. 9 - Typical Switching Losses vs. Gate Resistance

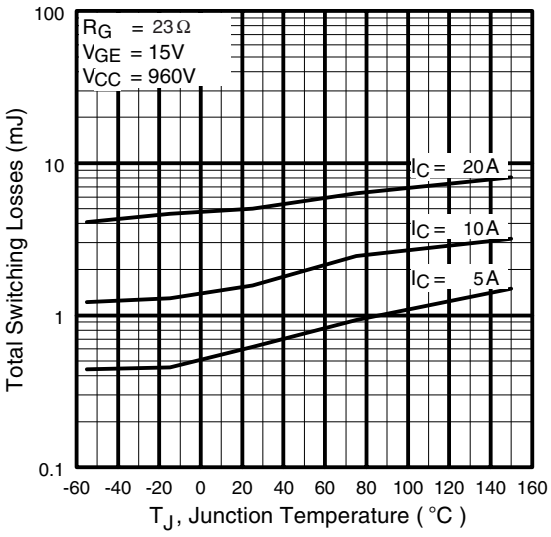


Fig. 10 - Typical Switching Losses vs. Junction Temperature

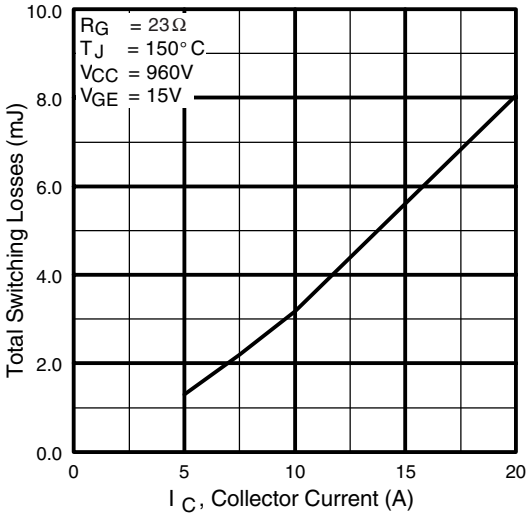


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

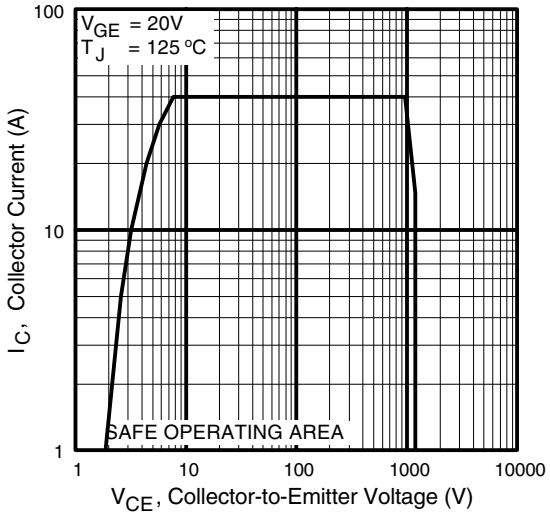


Fig. 12 - Turn-Off SOA

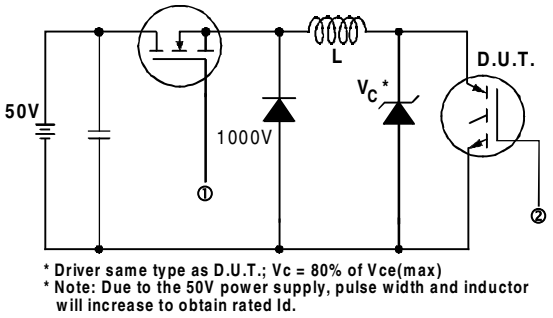


Fig. 13a - Clamped Inductive Load Test Circuit

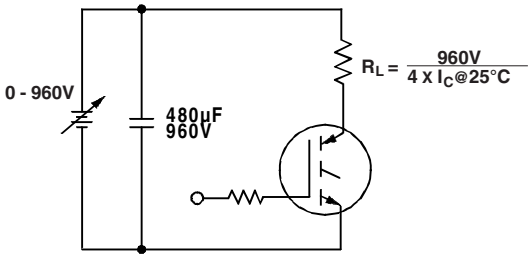


Fig. 13b - Pulsed Collector Current Test Circuit

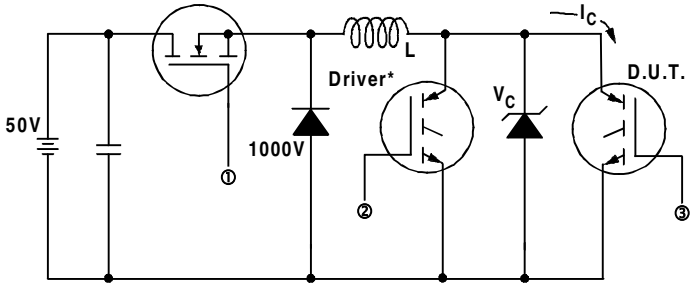


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 960V**

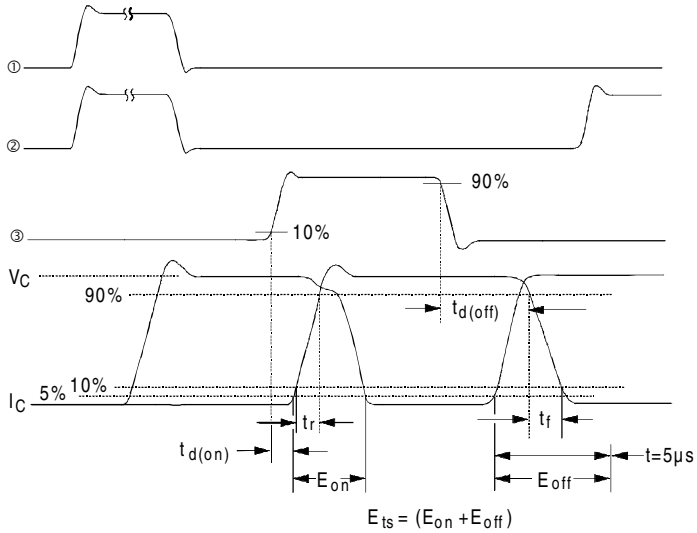
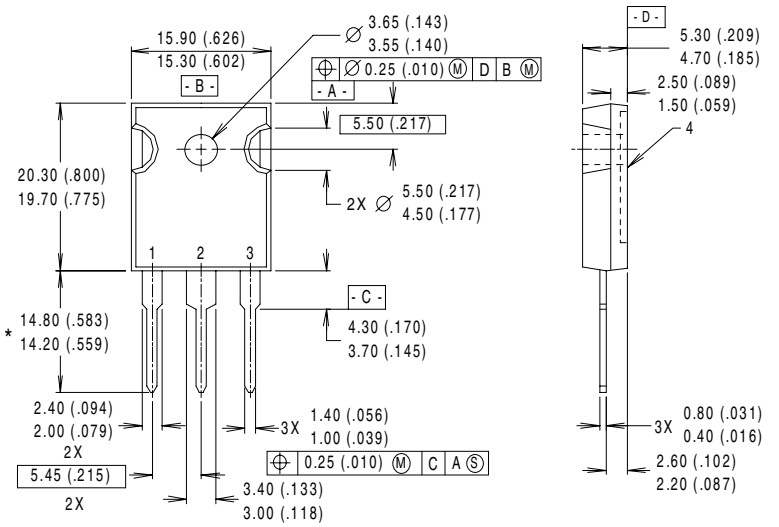


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 6/00

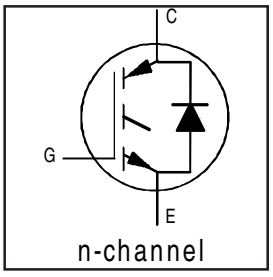
PD- 91579A

International
IOR Rectifier

IRG4PH30KD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
UltraFast IGBT



n-channel

V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 3.10V

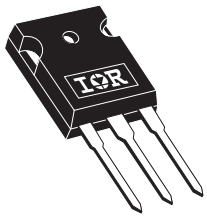
@V_{GE} = 15V, I_C = 10A

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, V_{CC} = 720V , T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Tighter parameter distribution and higher efficiency than previous generations
- IGBT co-packaged with HEXFRED™ ultrafast, ultrasoft recovery antiparallel diodes

Benefits

- Latest generation 4 IGBT's offer highest power density motor controls possible
- HEXFRED™ diodes optimized for performance with IGBTs. Minimized recovery characteristics reduce noise, EMI and switching losses
- This part replaces IRGPH30MD2 products
- For hints see design tip 97003


TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	20	A
I_C @ T_C = 100°C	Continuous Collector Current	10	
I_{CM}	Pulsed Collector Current ①	40	
I_{LM}	Clamped Inductive Load Current ②	40	
I_F @ T_C = 100°C	Diode Continuous Forward Current	10	
I_{FM}	Diode Maximum Forward Current	40	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	——	——	1.2	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	——	——	2.5	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	——	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	——	40	
Wt	Weight	——	6 (0.21)	——	g (oz)

2/7/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.19	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	3.10	4.2	V	I_C = 10A V_{GE} = 15V
		—	3.90	—		I_C = 20A See Fig. 2, 5
		—	3.01	—		I_C = 10A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-12	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	4.3	6.5	—	S	V_{CE} = 100V, I_C = 10A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	3500		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	3.4	3.8	V	I_C = 10A See Fig. 13
		—	3.3	3.7		I_C = 10A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	53	80	nC	I_C = 10A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	9.0	14		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	21	32		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	39	—	ns	
t_r	Rise Time	—	84	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	220	340		I_C = 10A, V_{CC} = 800V
t_f	Fall Time	—	90	140		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.95	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	1.15	—		and diode reverse recovery
E_{ts}	Total Switching Loss	—	2.10	2.6		See Fig. 9,10,18
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 720V, T_J = 125°C
						V_{GE} = 15V, R_G = 5.0Ω
$t_{d(on)}$	Turn-On Delay Time	—	42	—	ns	T_J = 150°C, See Fig. 10,11,18
t_r	Rise Time	—	79	—		I_C = 10A, V_{CC} = 800V
$t_{d(off)}$	Turn-Off Delay Time	—	540	—		V_{GE} = 15V, R_G = 23Ω,
t_f	Fall Time	—	97	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	3.5	—	mJ	and diode reverse recovery
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	800	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	60	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	14	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	50	76	ns	T_J = 25°C See Fig.
		—	72	110		T_J = 125°C 14 I_F = 10A
I_{rr}	Diode Peak Reverse Recovery Current	—	4.4	7.0	A	T_J = 25°C See Fig.
		—	5.9	8.8		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	130	200	nC	T_J = 25°C See Fig.
		—	250	380		T_J = 125°C 16 di/dt = 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	210	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	180	—		T_J = 125°C 17

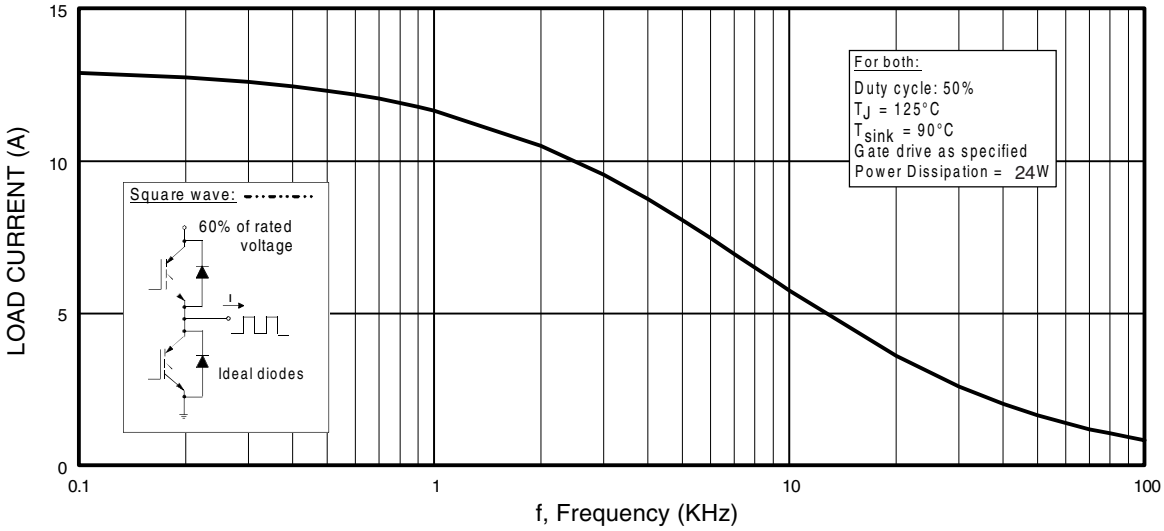


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

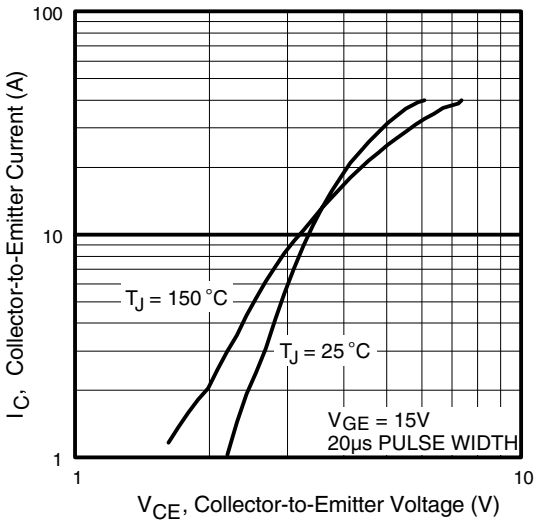


Fig. 2 - Typical Output Characteristics

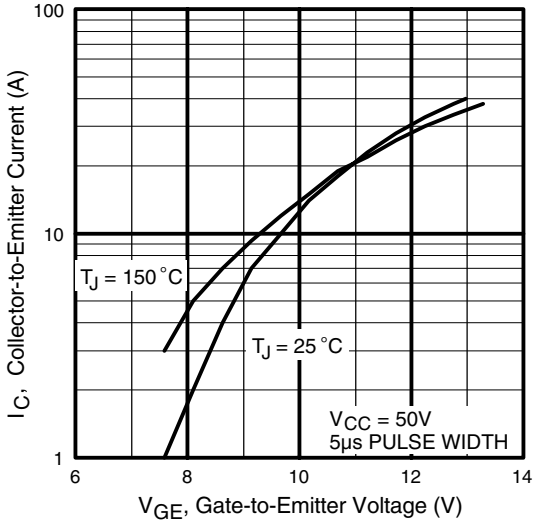


Fig. 3 - Typical Transfer Characteristics

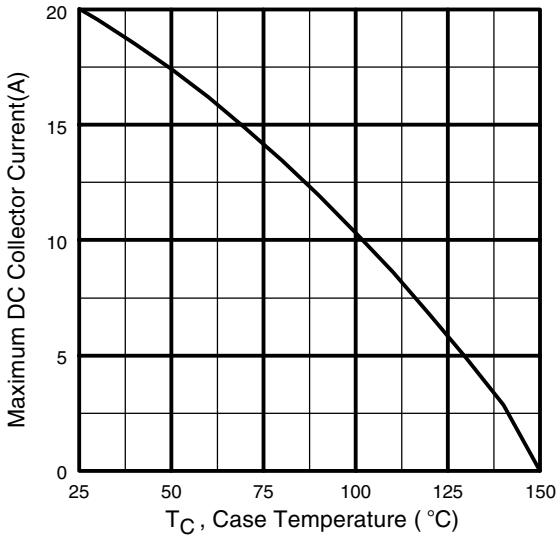


Fig. 4 - Maximum Collector Current vs. Case Temperature

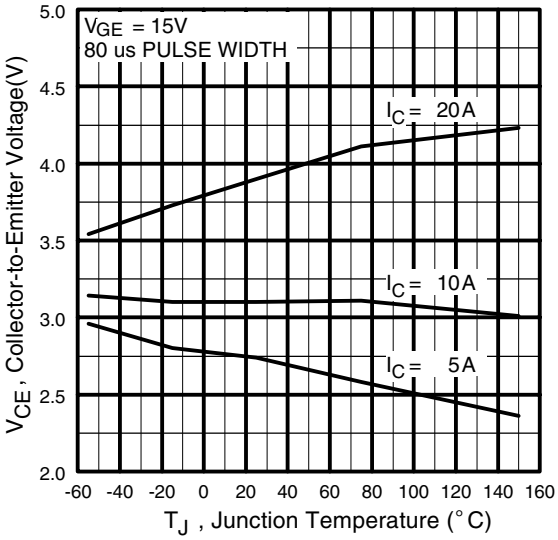


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

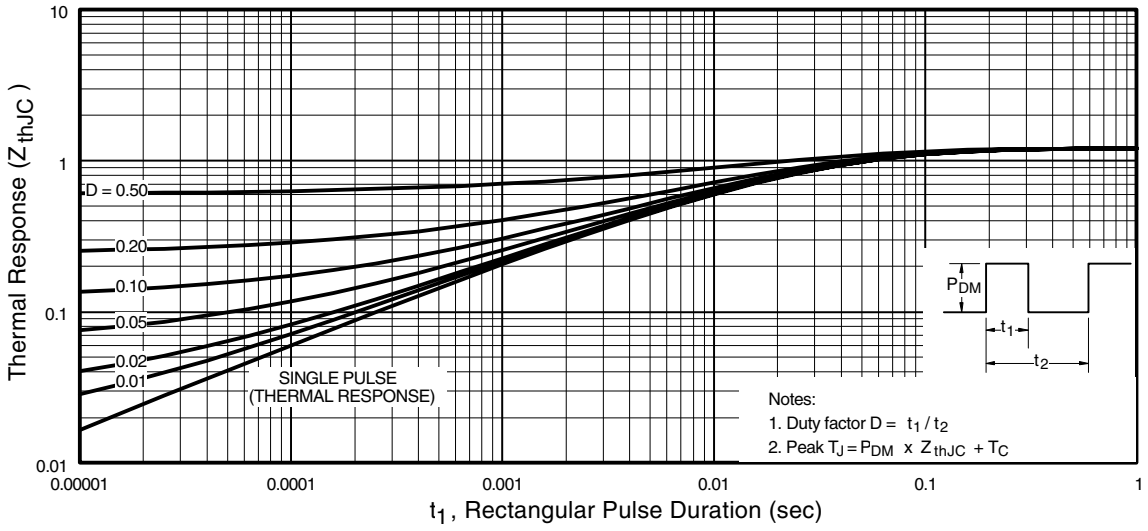


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

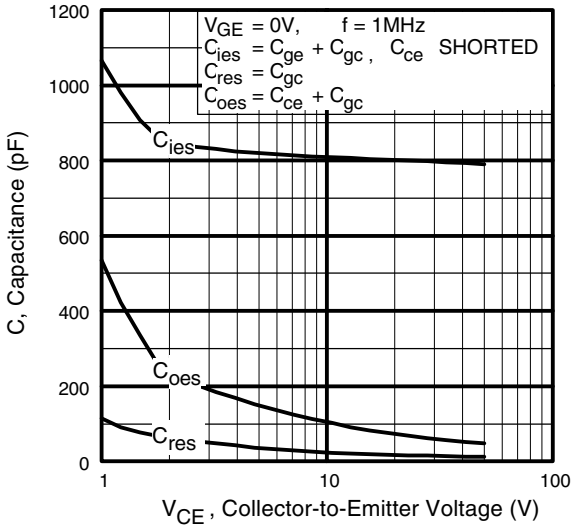


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

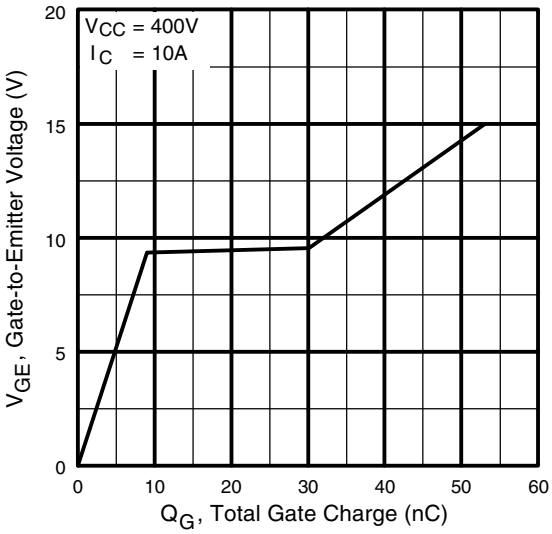


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

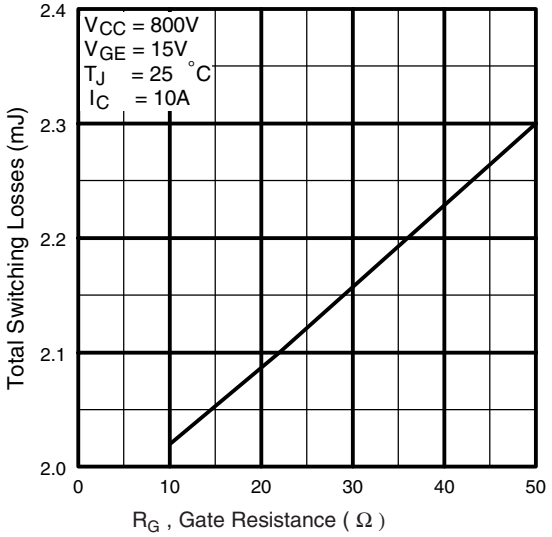


Fig. 9 - Typical Switching Losses vs. Gate Resistance

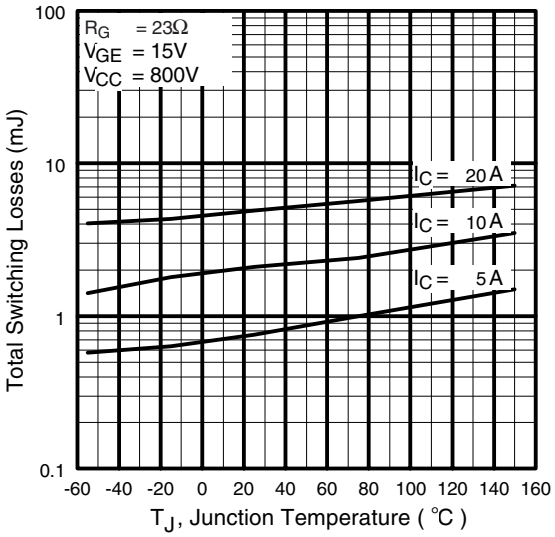


Fig. 10 - Typical Switching Losses vs. Junction Temperature

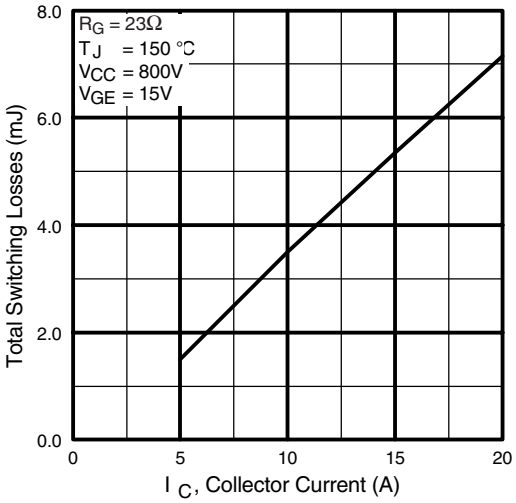


Fig. 11 - Typical Switching Losses vs. Collector Current

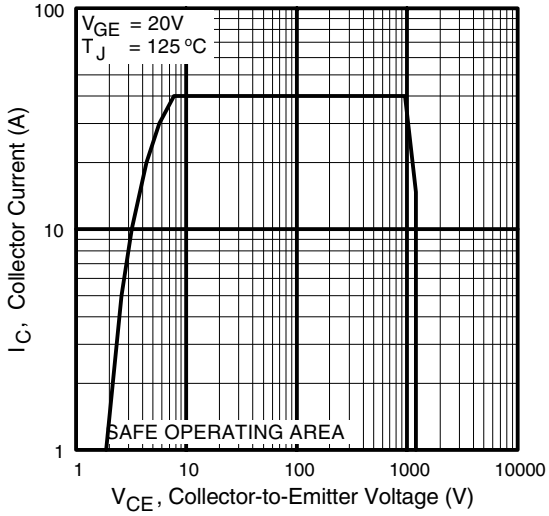


Fig. 12 - Turn-Off SOA

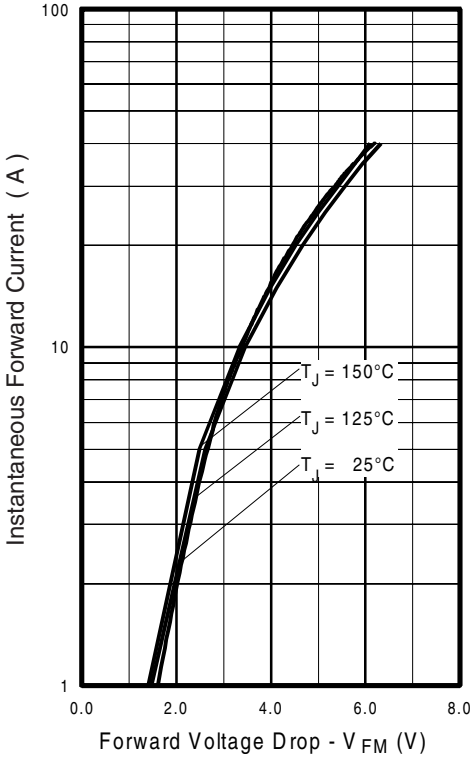


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

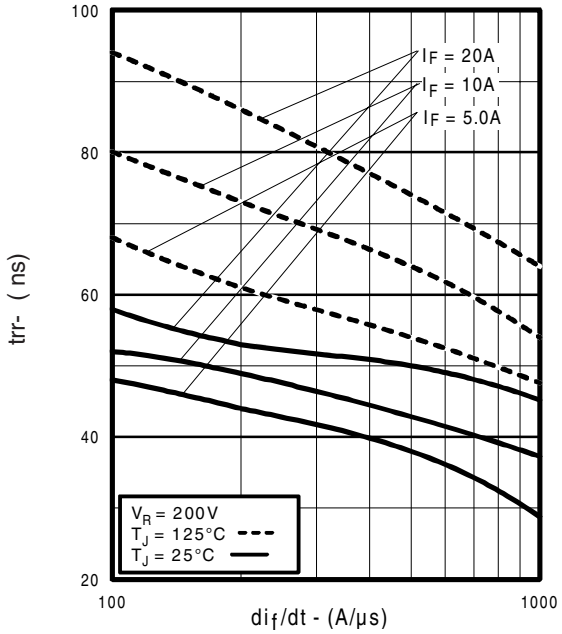


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

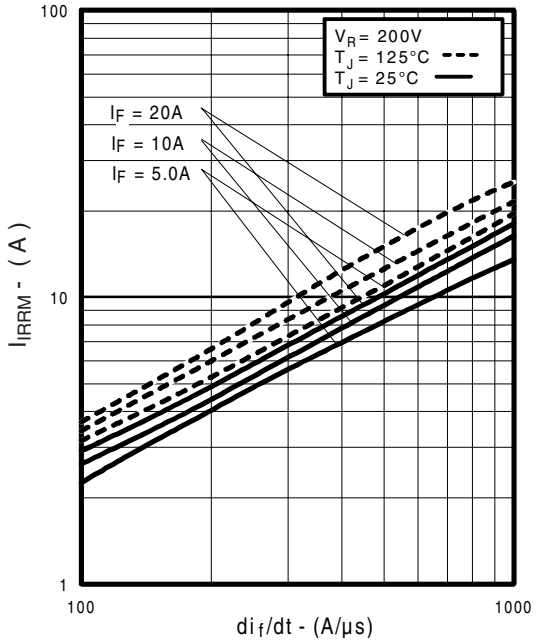


Fig. 15 - Typical Recovery Current vs. di_f/dt

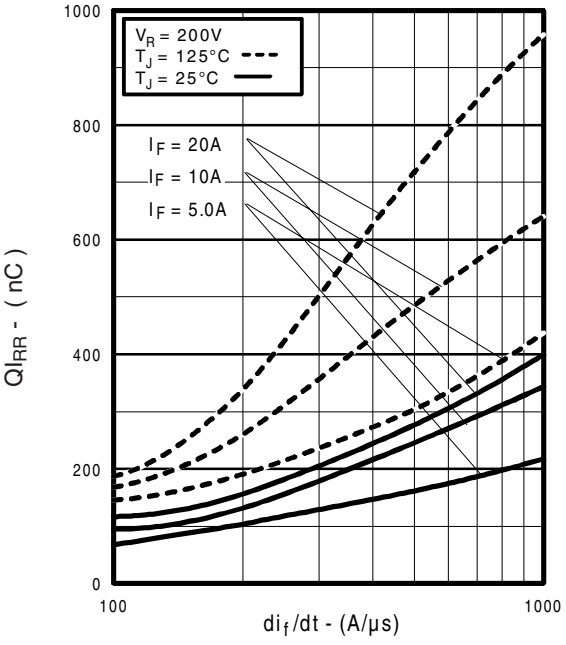


Fig. 16 - Typical Stored Charge vs. di_f/dt

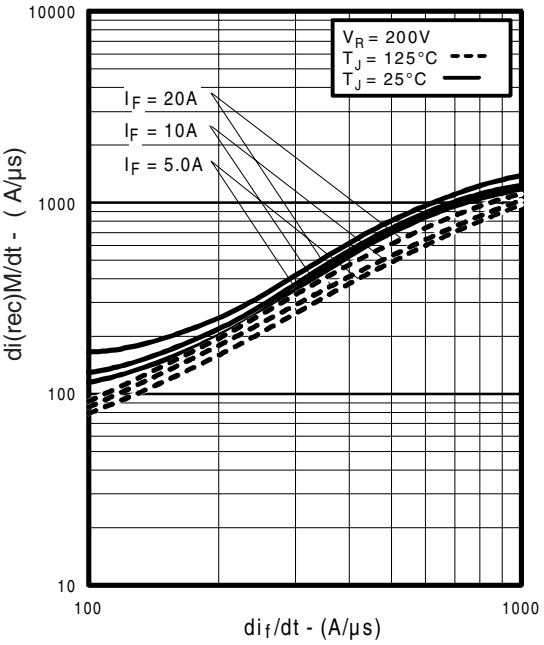


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

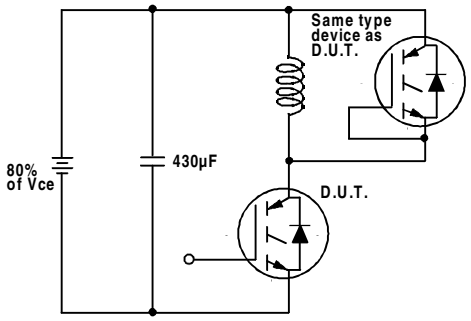


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

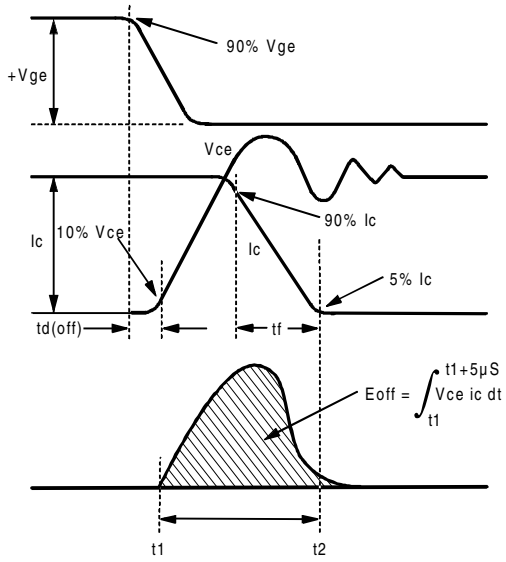


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

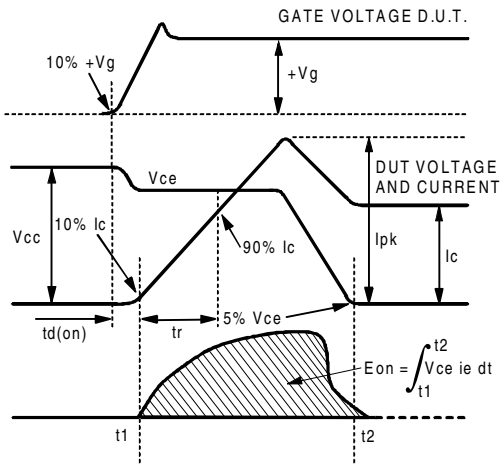


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

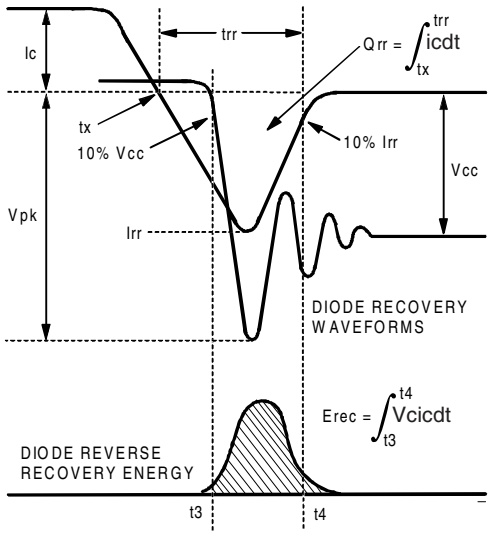


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

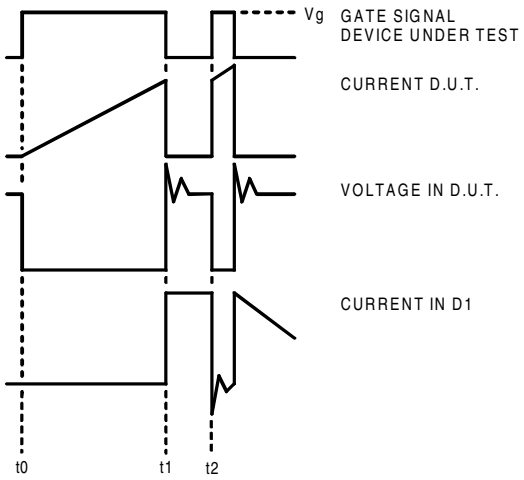


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

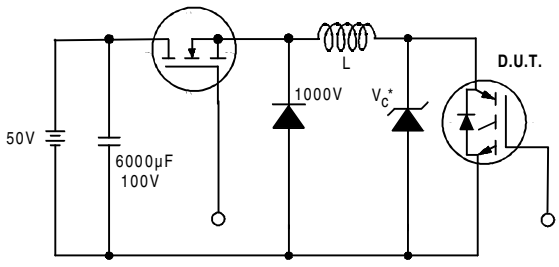


Figure 19. Clamped Inductive Load Test Circuit

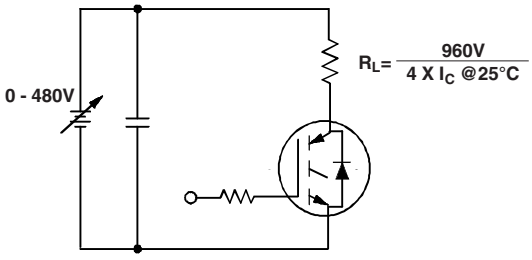


Figure 20. Pulsed Collector Current Test Circuit

Notes:

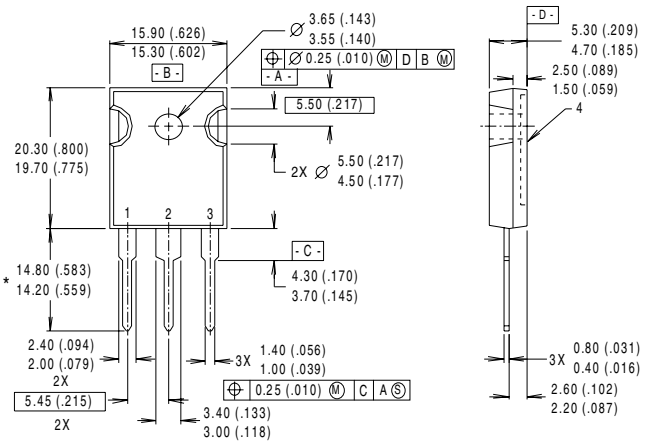
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 23Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 6/00

International
IOR Rectifier

PD - 91578B

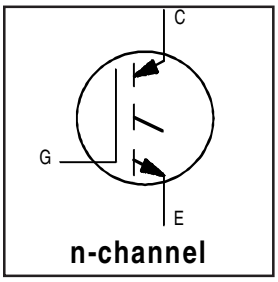
IRG4PH40K

Short Circuit Rated
UltraFast IGBT

INSULATED GATE BIPOLAR TRANSISTOR

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, V_{CC} = 720V , T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Latest generation design provides tighter parameter distribution and higher efficiency than previous generations



n-channel

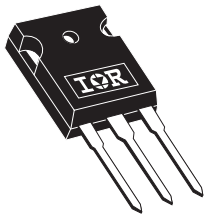
V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.74V

@V_{GE} = 15V, I_C = 15A

Benefits

- As a Freewheeling Diode we recommend our HEXFRED™ ultrafast, ultrasoft recovery diodes for minimum EMI / Noise and switching losses in the Diode and IGBT
- Latest generation 4 IGBT's offer highest power density motor controls possible
- This part replaces the IRGPH40K and IRGPH40M devices



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	30	A
I_C @ T_C = 100°C	Continuous Collector Current	15	
I_{CM}	Pulsed Collector Current ①	60	
I_{LM}	Clamped Inductive Load Current ②	60	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	180	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.77	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

2/7/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.37	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.54	—	V	I_C = 10A
		—	2.74	3.4		I_C = 15A V_{GE} = 15V
		—	3.29	—		I_C = 30A See Fig.2, 5
		—	2.53	—		I_C = 15A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-3.3	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	8.0	12	—	S	V_{CE} = 100 V, I_C = 15A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	3000		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	94	140	nC	I_C = 15A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	14	22		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	37	55		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	30	—	ns	
t_r	Rise Time	—	22	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	200	300		I_C = 15A, V_{CC} = 960V
t_f	Fall Time	—	150	230		V_{GE} = 15V, R_G = 10Ω
E_{on}	Turn-On Switching Loss	—	0.73	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	1.66	—		See Fig. 9,10,14
E_{ts}	Total Switching Loss	—	2.39	2.9		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 720V, T_J = 125°C V_{GE} = 15V, R_G = 10Ω
$t_{d(on)}$	Turn-On Delay Time	—	29	—	ns	T_J = 150°C,
t_r	Rise Time	—	24	—		I_C = 15A, V_{CC} = 960V
$t_{d(off)}$	Turn-Off Delay Time	—	870	—		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	—	330	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	4.93	—	mJ	See Fig. 10,11,14
E_{on}	Turn-On Switching Loss	—	0.37	—	mJ	T_J = 25°C, V_{GE} = 15V, R_G = 10Ω
E_{off}	Turn-Off Switching Loss	—	0.89	—		I_C = 10A, V_{CC} = 960V
E_{ts}	Total Switching Loss	—	1.26	—		Energy losses include "tail"
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1600	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	77	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	26	—		f = 1.0MHz

Details of note ① through ⑤ are on the last page

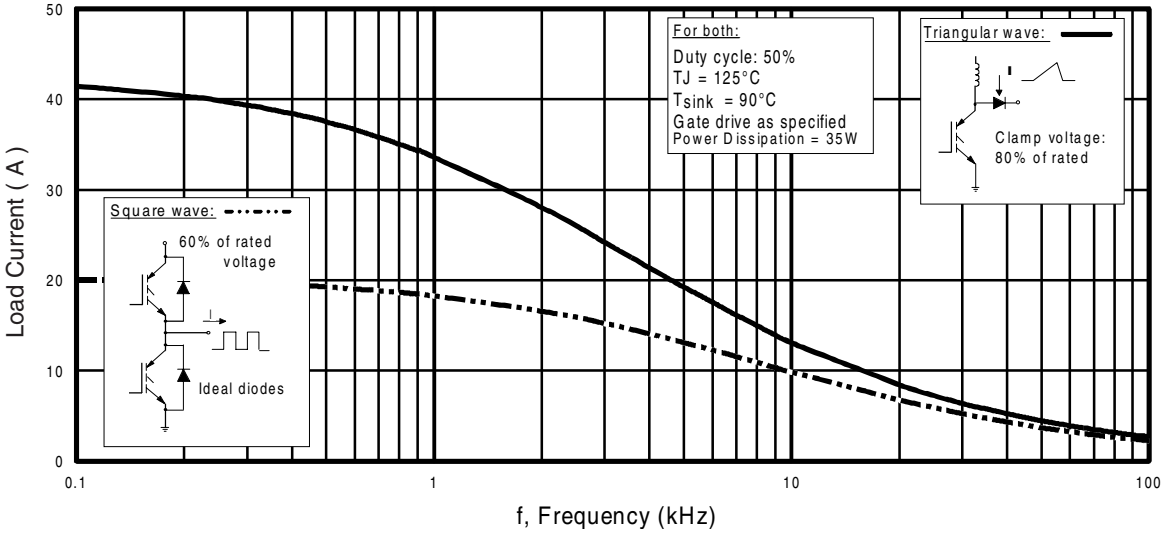


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

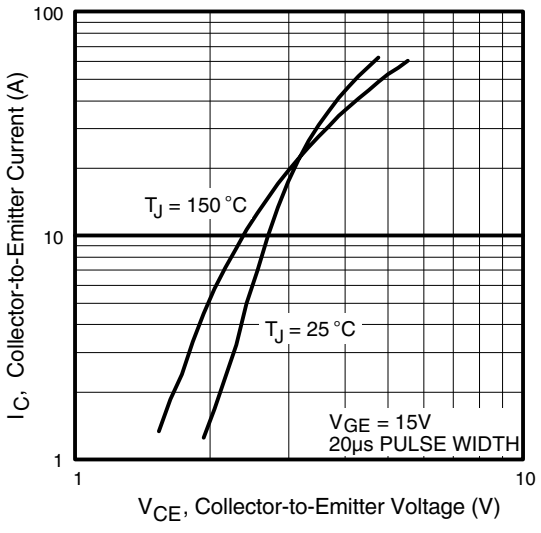


Fig. 2 - Typical Output Characteristics

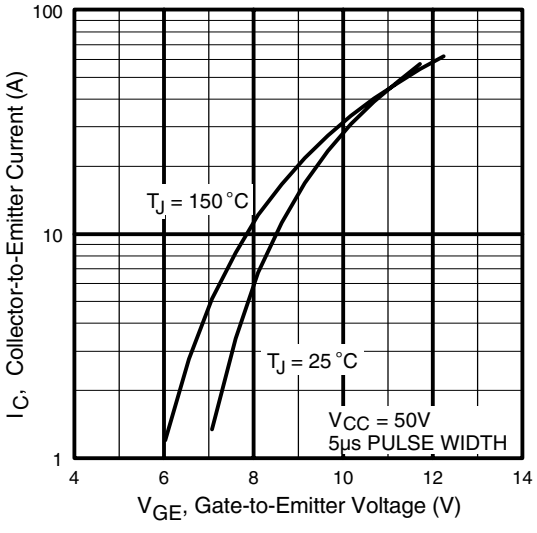


Fig. 3 - Typical Transfer Characteristics

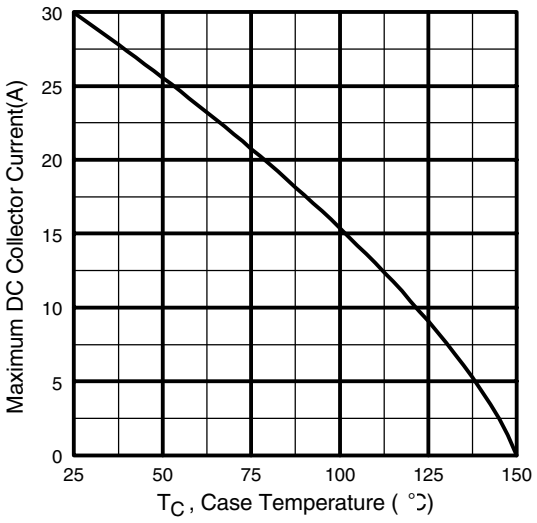


Fig. 4 - Maximum Collector Current vs. Case Temperature

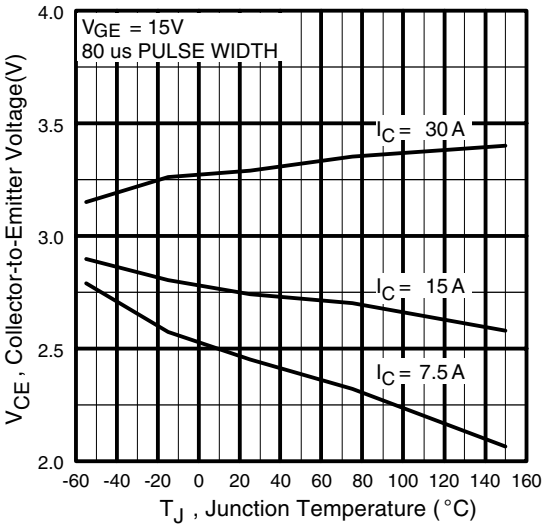


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

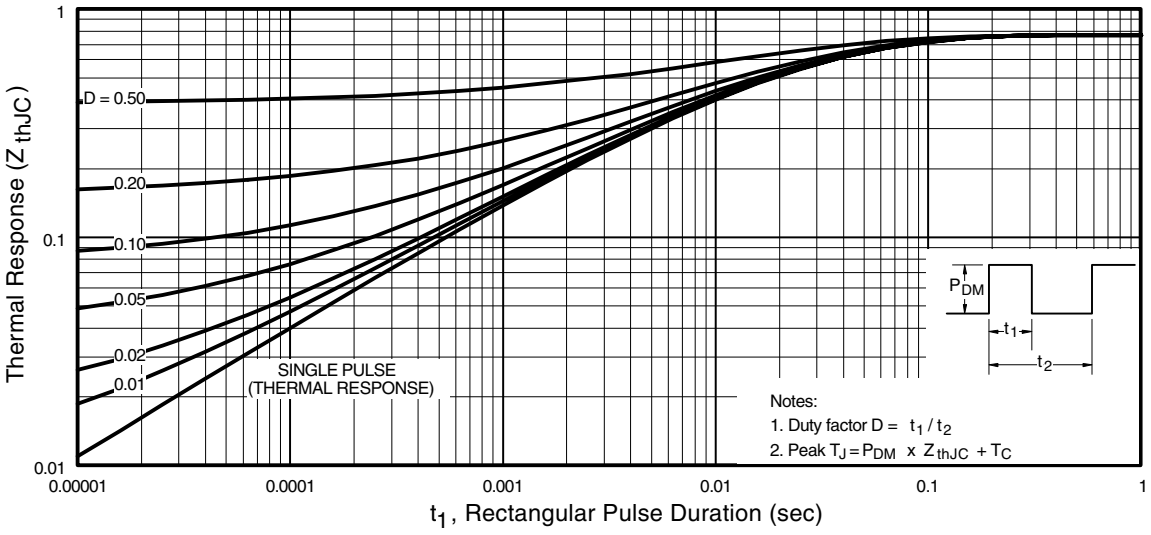


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

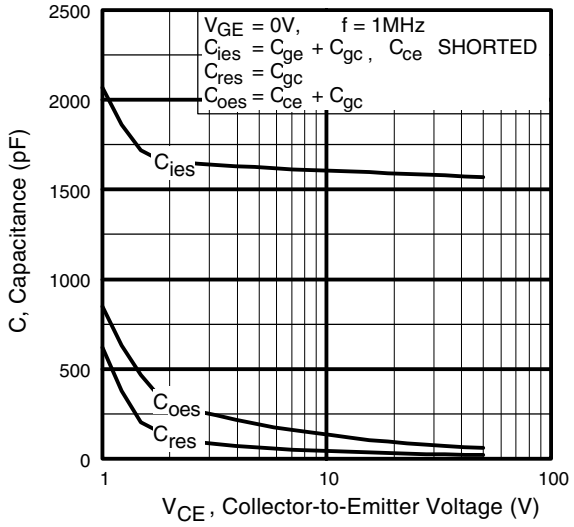


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

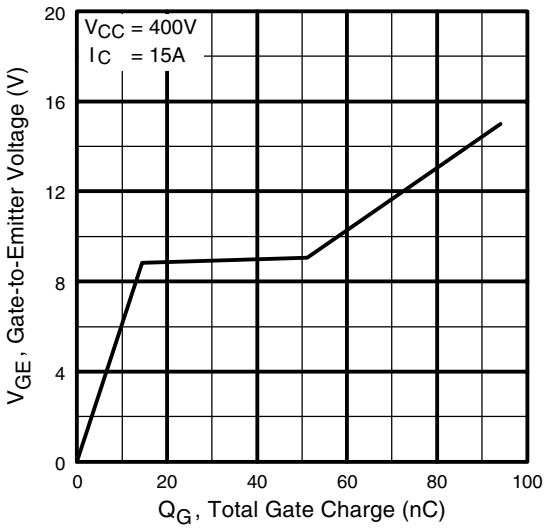


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

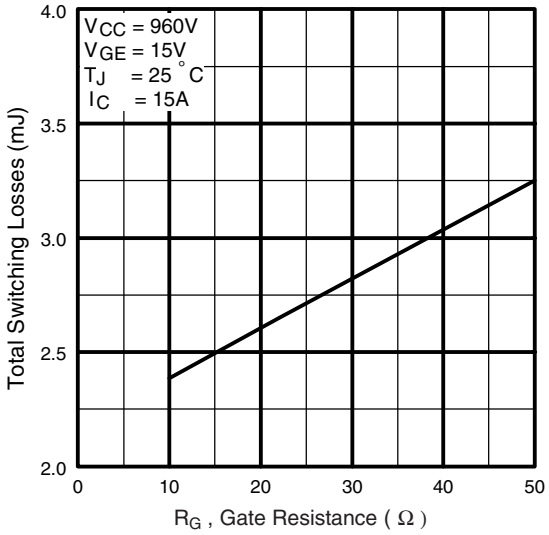


Fig. 9 - Typical Switching Losses vs. Gate Resistance

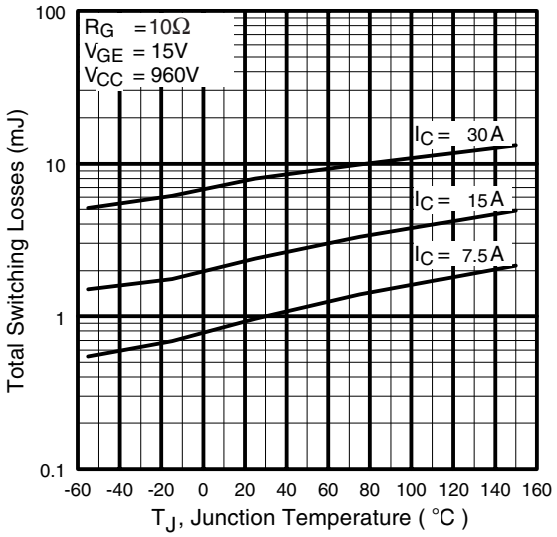


Fig. 10 - Typical Switching Losses vs. Junction Temperature

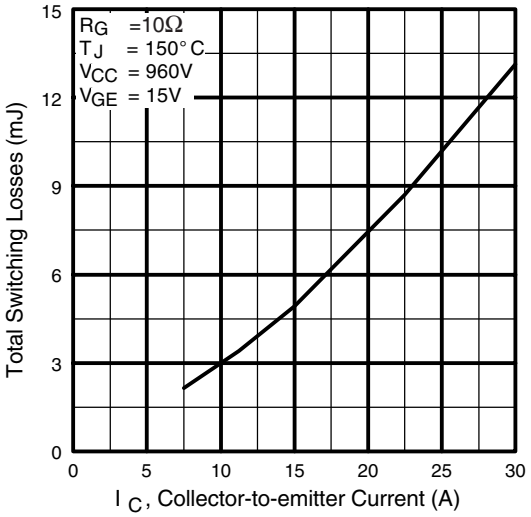


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

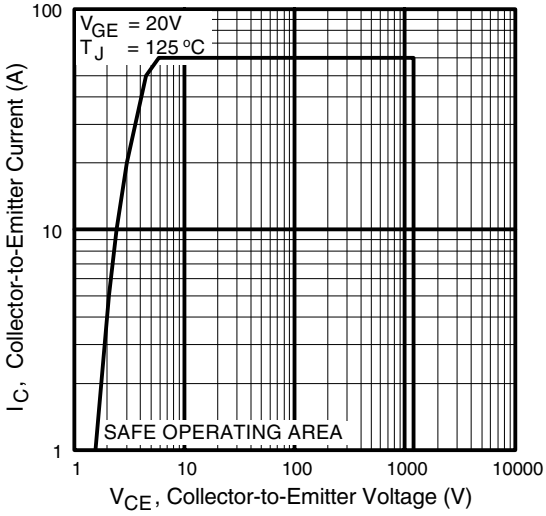


Fig. 12 - Turn-Off SOA

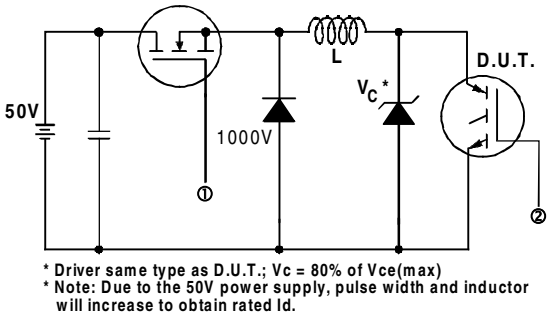


Fig. 13a - Clamped Inductive Load Test Circuit

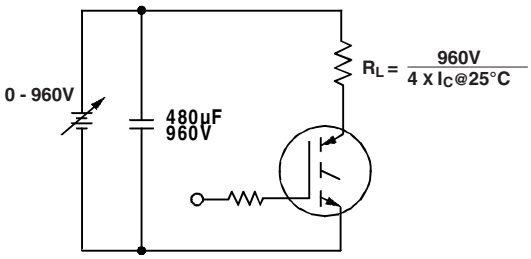


Fig. 13b - Pulsed Collector Current Test Circuit

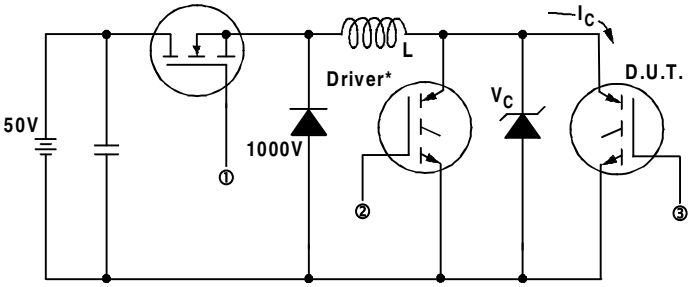


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 960V**

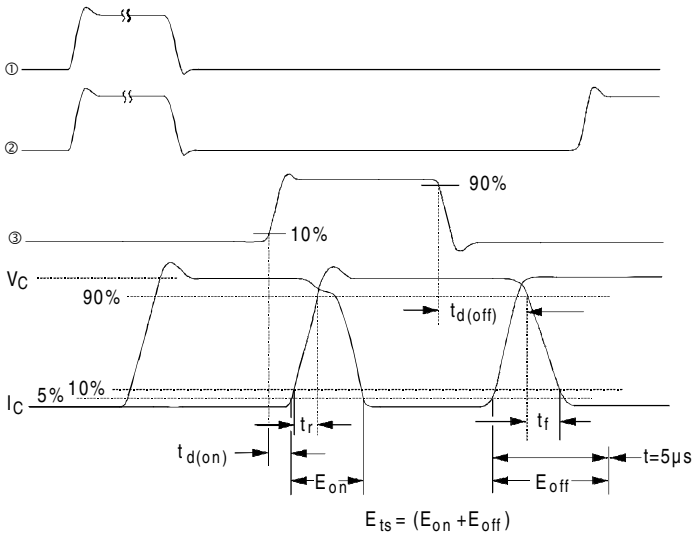


Fig. 14b - Switching Loss Waveforms

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

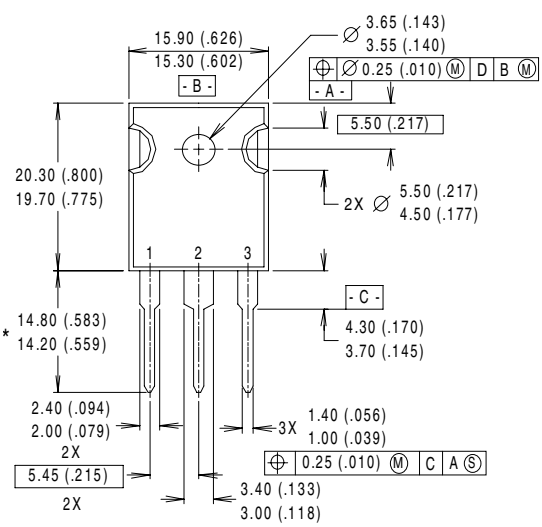
② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 10Ω, (See fig. 13a)

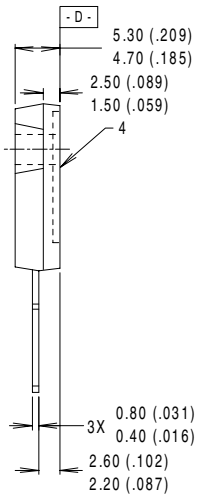
③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

Case Outline and Dimensions — TO-247AC





NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 6/00

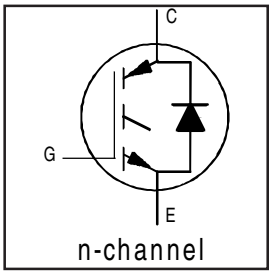
PD- 91577B

International
IOR Rectifier

IRG4PH40KD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
UltraFast IGBT



V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.74V

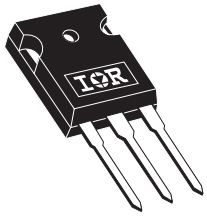
@V_{GE} = 15V, I_C = 15A

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, V_{CC} = 720V , T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Tighter parameter distribution and higher efficiency than previous generations
- IGBT co-packaged with HEXFRED™ ultrafast, ultrasoft recovery antiparallel diodes

Benefits

- Latest generation 4 IGBT's offer highest power density motor controls possible
- HEXFRED™ diodes optimized for performance with IGBTs. Minimized recovery characteristics reduce noise, EMI and switching losses
- This part replaces the IRGPH40KD2 and IRGPH40MD2 products
- For hints see design tip 97003



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	30	A
I_C @ T_C = 100°C	Continuous Collector Current	15	
I_{CM}	Pulsed Collector Current ①	60	
I_{LM}	Clamped Inductive Load Current ②	60	
I_F @ T_C = 100°C	Diode Continuous Forward Current	8.0	
I_{FM}	Diode Maximum Forward Current	130	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	0.77	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	1.7	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	40	
Wt	Weight	—	6 (0.21)	—	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.37	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.74	3.4	V	I_C = 15A V_{GE} = 15V
		—	3.29	—		I_C = 30A See Fig. 2, 5
		—	2.53	—		I_C = 15A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-3.3	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	8.0	12	—	S	V_{CE} = 100V, I_C = 15A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	3000		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	2.6	3.3	V	I_C = 8.0A See Fig. 13
		—	2.4	3.1		I_C = 8.0A, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	94	140	nC	I_C = 15A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	14	22		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	37	55		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	50	—	ns	
t_r	Rise Time	—	31	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	96	140		I_C = 15A, V_{CC} = 800V
t_f	Fall Time	—	220	330		V_{GE} = 15V, R_G = 10Ω
E_{on}	Turn-On Switching Loss	—	1.31	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	1.12	—		and diode reverse recovery
E_{ts}	Total Switching Loss	—	2.43	2.8		See Fig. 9,10,18
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 720V, T_J = 125°C
						V_{GE} = 15V, R_G = 10Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	49	—	ns	T_J = 150°C, See Fig. 10,11,18
t_r	Rise Time	—	33	—		I_C = 15A, V_{CC} = 800V
$t_{d(off)}$	Turn-Off Delay Time	—	290	—		V_{GE} = 15V, R_G = 10Ω,
t_f	Fall Time	—	440	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	5.1	—	mJ	and diode reverse recovery
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1600	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	77	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	26	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	63	95	ns	T_J = 25°C See Fig. 14 I_F = 8.0A
		—	106	160		T_J = 125°C
I_{rr}	Diode Peak Reverse Recovery Current	—	4.5	8.0	A	T_J = 25°C See Fig. 15 V_R = 200V
		—	6.2	11		T_J = 125°C
Q_{rr}	Diode Reverse Recovery Charge	—	140	380	nC	T_J = 25°C See Fig. 16 di/dt = 200Aµs
		—	335	880		T_J = 125°C
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	133	—	A/µs	T_J = 25°C See Fig. 17
	During t_b	—	85	—		T_J = 125°C

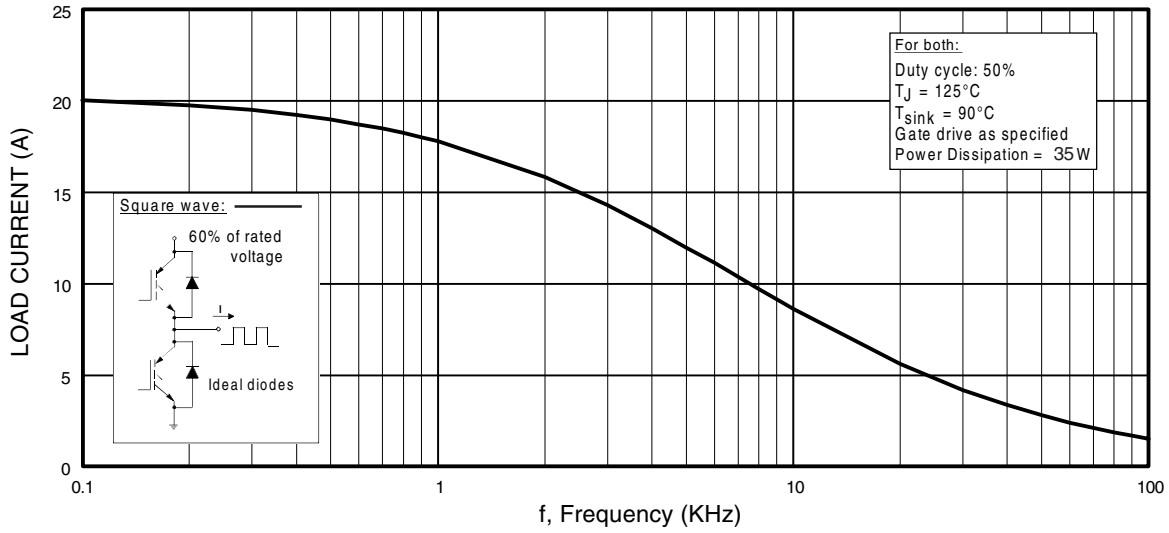


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

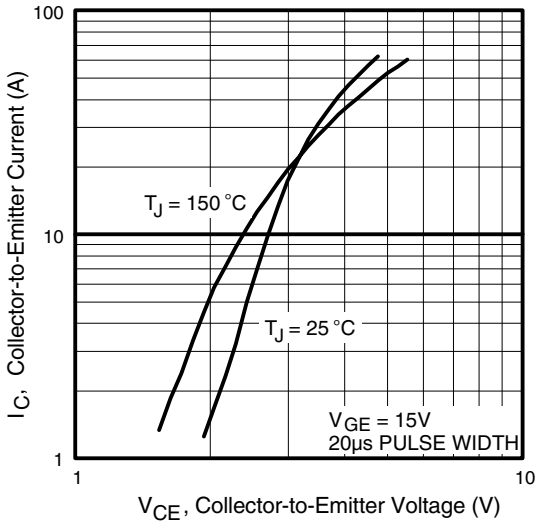


Fig. 2 - Typical Output Characteristics

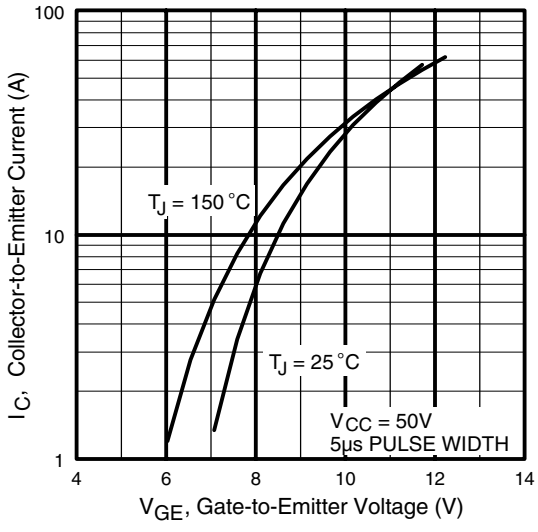


Fig. 3 - Typical Transfer Characteristics

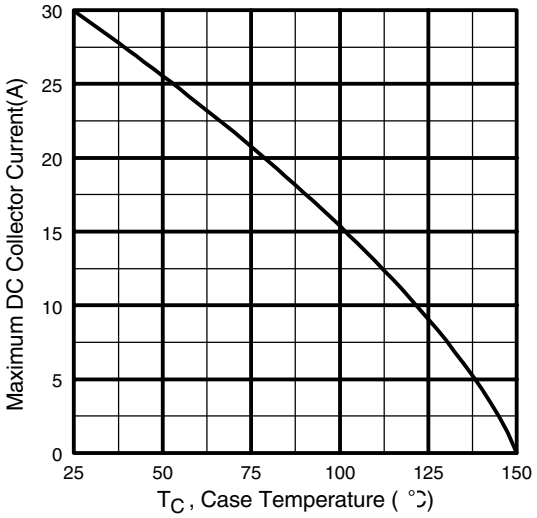


Fig. 4 - Maximum Collector Current vs. Case Temperature

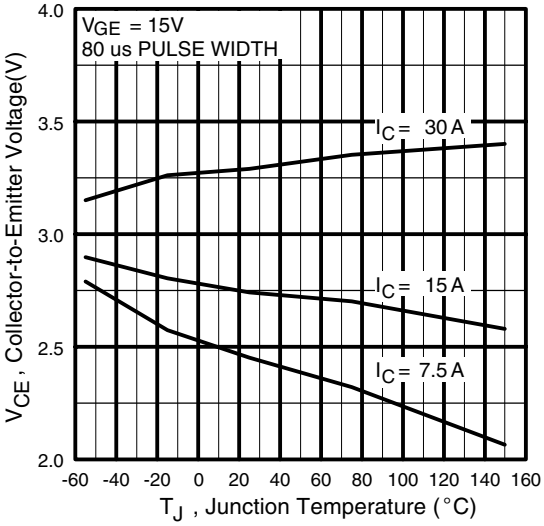


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

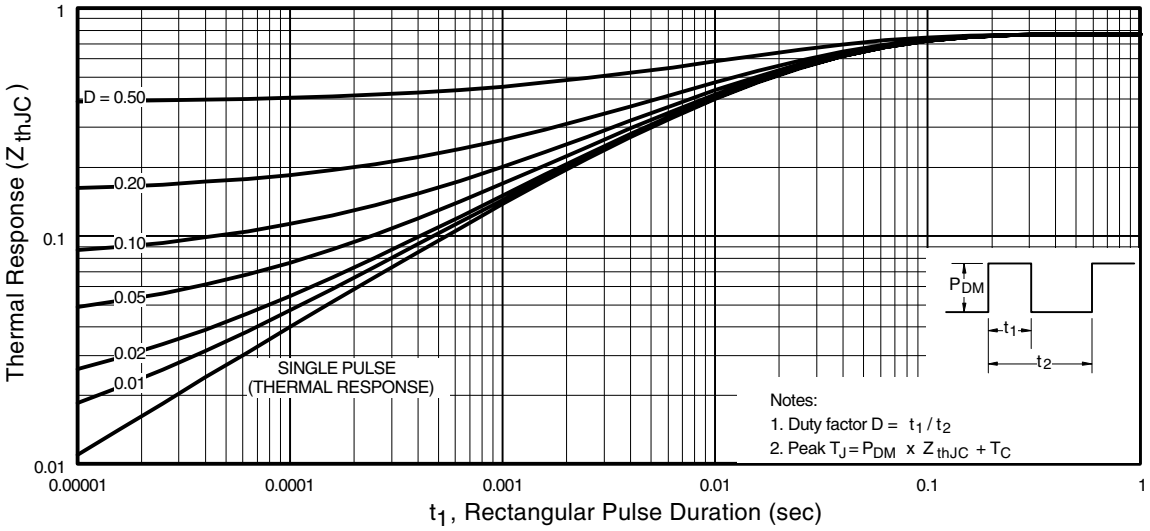


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

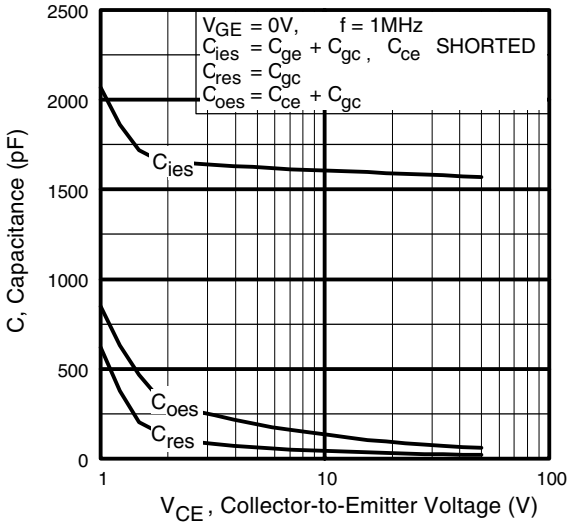


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

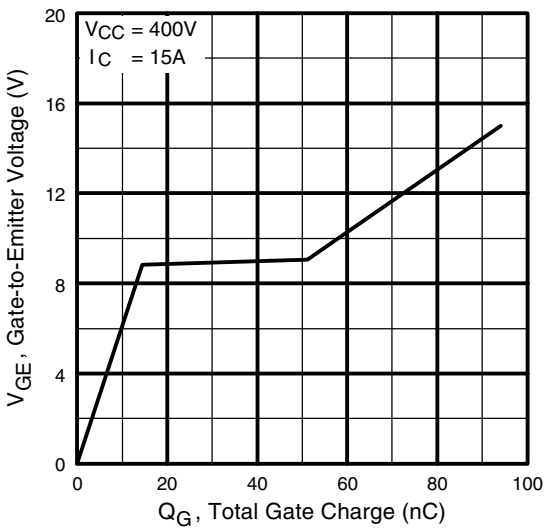


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

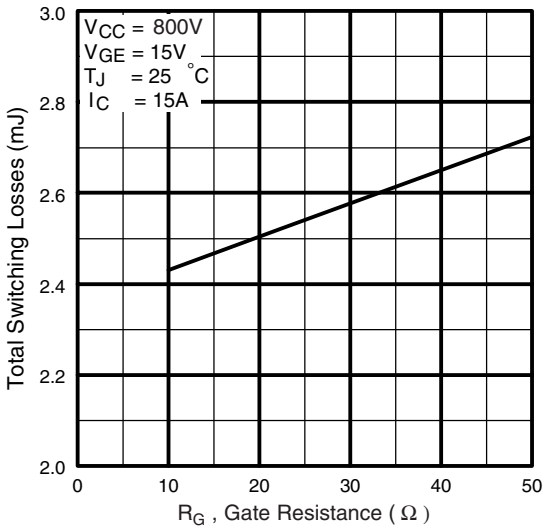


Fig. 9 - Typical Switching Losses vs. Gate Resistance

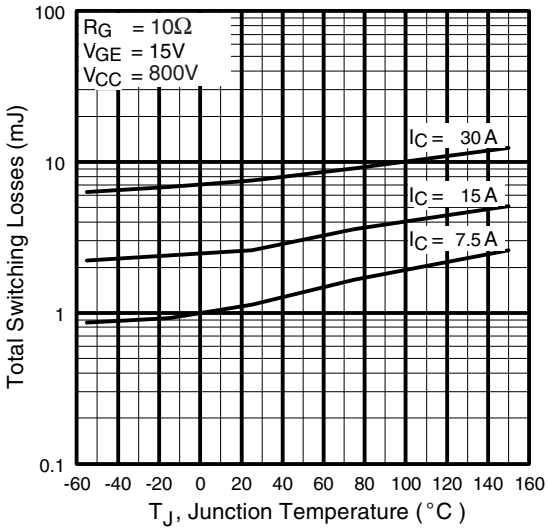


Fig. 10 - Typical Switching Losses vs. Junction Temperature

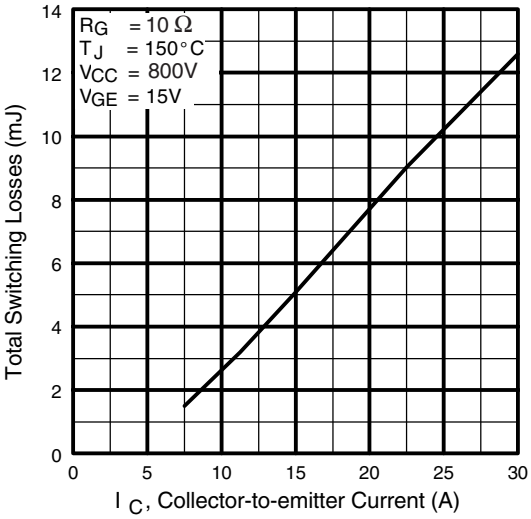


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

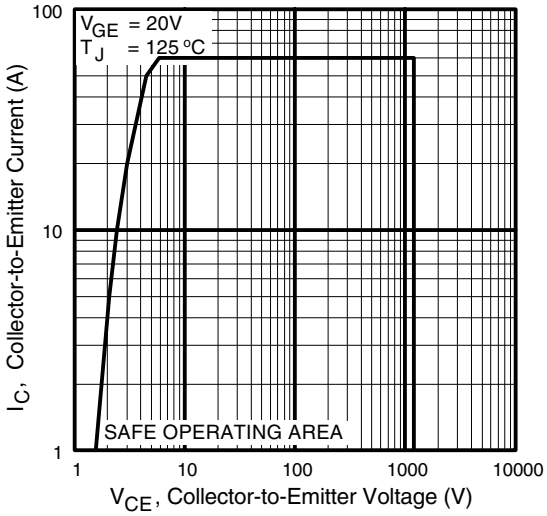


Fig. 12 - Turn-Off SOA

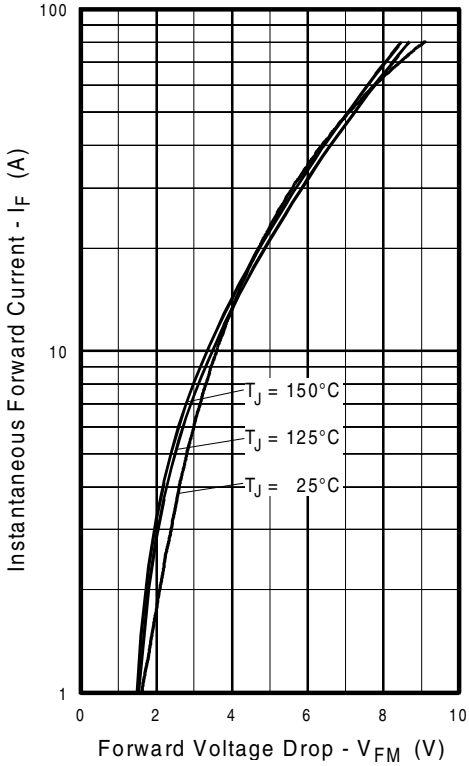


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

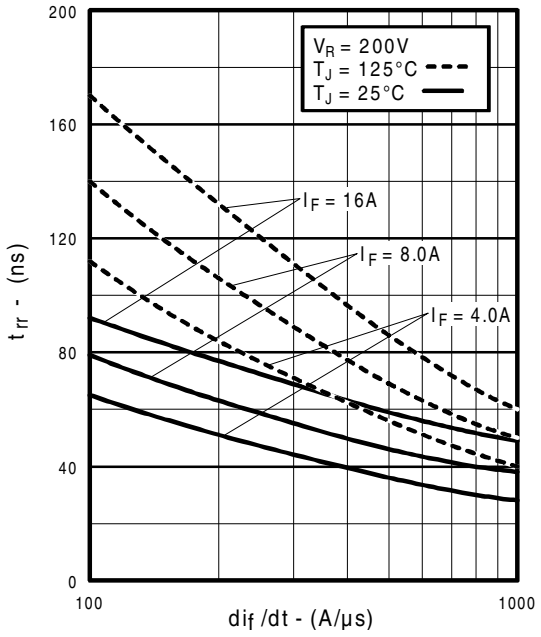


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

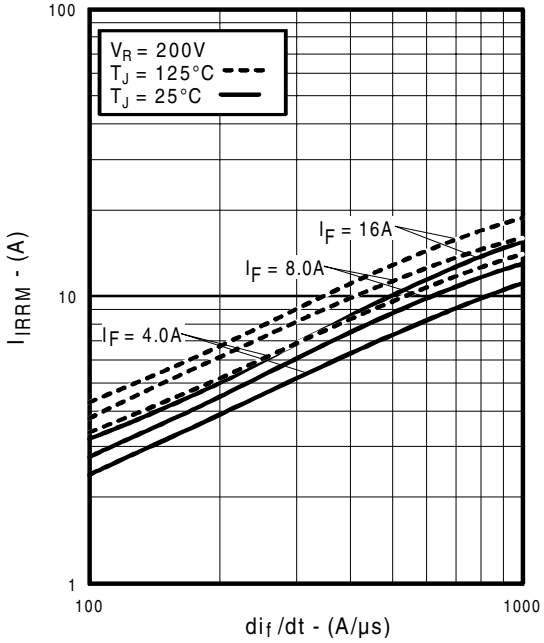


Fig. 15 - Typical Recovery Current vs. di_f/dt

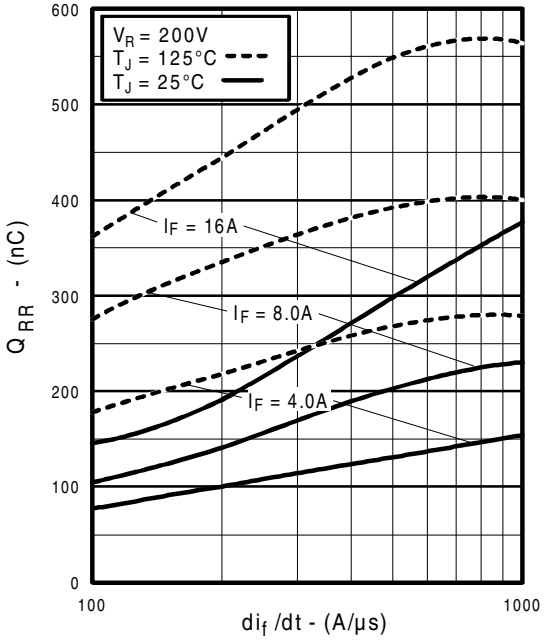


Fig. 16 - Typical Stored Charge vs. di_f/dt

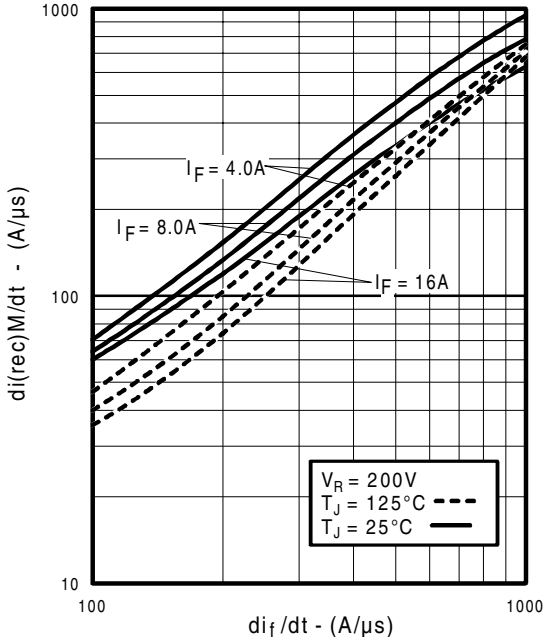


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

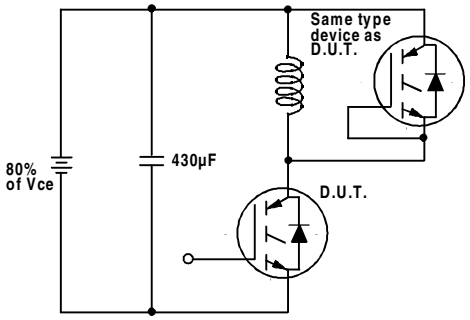


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

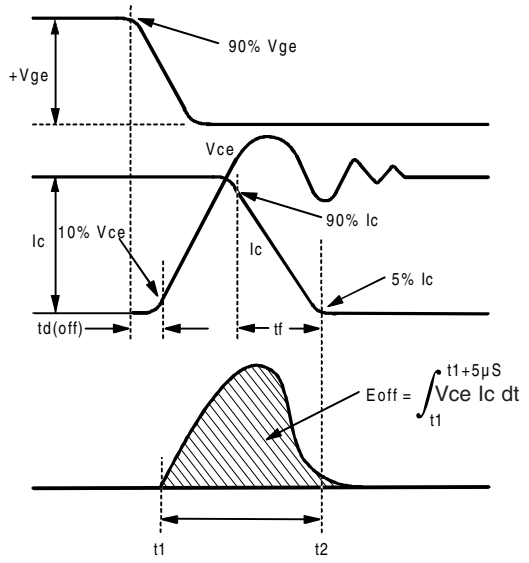


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

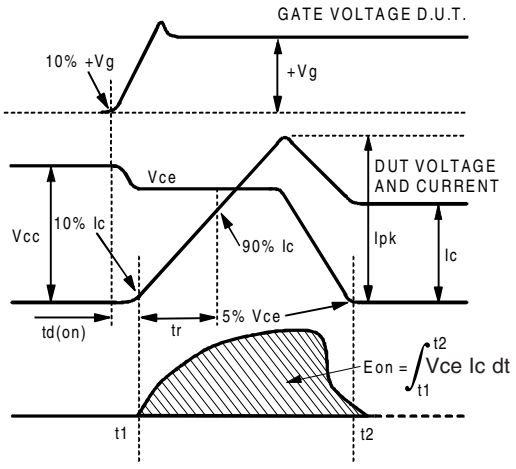


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

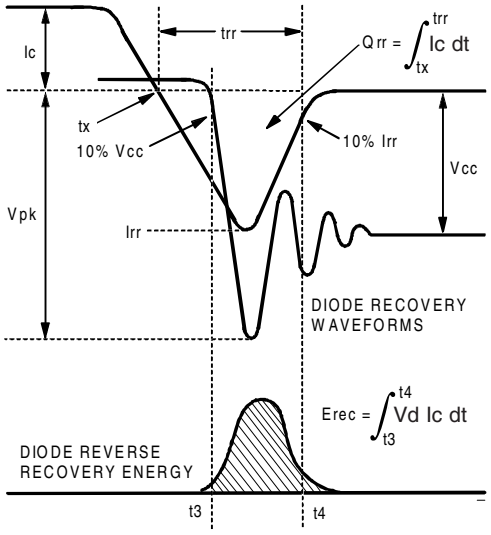


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

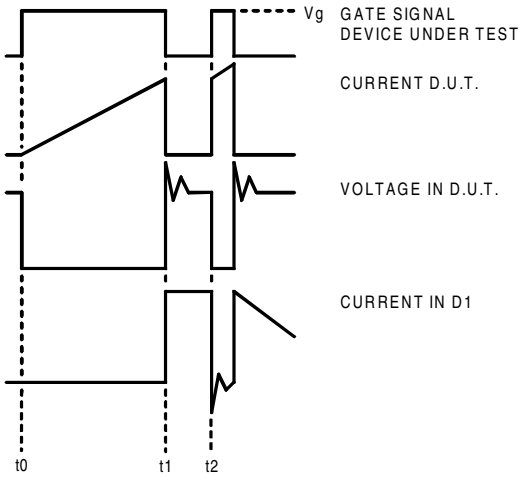


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

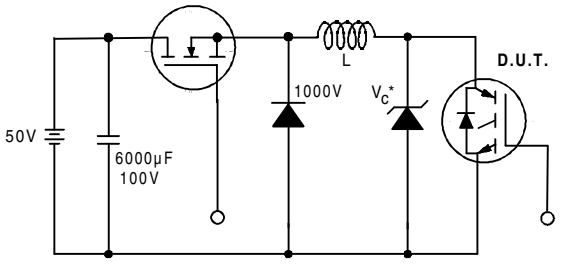


Figure 19. Clamped Inductive Load Test Circuit

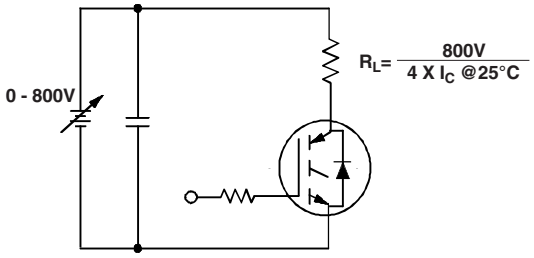


Figure 20. Pulsed Collector Current Test Circuit

Notes:

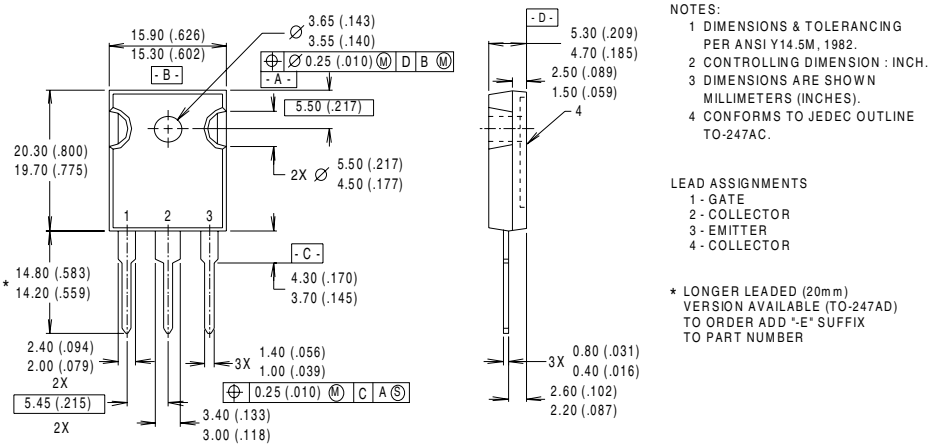
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 10Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 6/00

PD - 91612C

International
IOR Rectifier

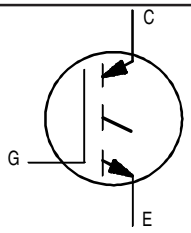
IRG4PH40U

INSULATED GATE BIPOLAR TRANSISTOR

Ultra Fast Speed IGBT

Features

- UltraFast: Optimized for high operating frequencies up to 40 kHz in hard switching, >200 kHz in resonant mode
- New IGBT design provides tighter parameter distribution and higher efficiency than previous generations
- Optimized for power conversion; SMPS, UPS and welding
- Industry standard TO-247AC package



n-channel

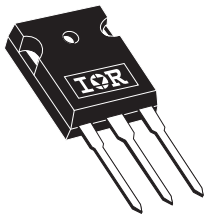
V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.43V

@V_{GE} = 15V, I_C = 21A

Benefits

- Higher switching frequency capability than competitive IGBTs
- Highest efficiency available
- Much lower conduction losses than MOSFETs
- More efficient than short circuit rated IGBTs



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	41	A
I_C @ T_C = 100°C	Continuous Collector Current	21	
I_{CM}	Pulsed Collector Current ①	82	
I_{LM}	Clamped Inductive Load Current ②	82	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	270	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.77	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.43	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.43	3.1	V	I_C = 21A V_{GE} = 15V
		—	2.97	—		I_C = 41A See Fig.2, 5
		—	2.47	—		I_C = 21A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	16	24	—	S	V_{CE} = 100V, I_C = 21A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	5000		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	86	130	nC	I_C = 21A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	13	20		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	29	44		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	
t_r	Rise Time	—	24	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	220	330		I_C = 21A, V_{CC} = 960V
t_f	Fall Time	—	180	270		V_{GE} = 15V, R_G = 10Ω
E_{on}	Turn-On Switching Loss	—	1.04	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	3.40	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	4.44	5.2		
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	T_J = 150°C,
t_r	Rise Time	—	25	—		I_C = 21A, V_{CC} = 960V
$t_{d(off)}$	Turn-Off Delay Time	—	310	—		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	—	380	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	7.39	—	mJ	See Fig. 11, 14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1800	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	120	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	18	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 10Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

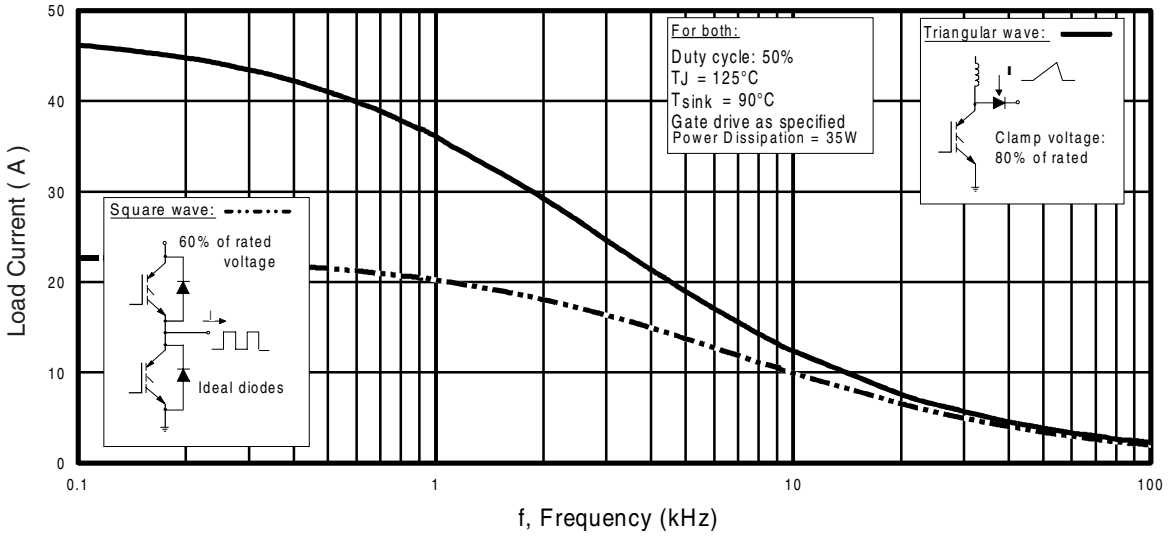


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

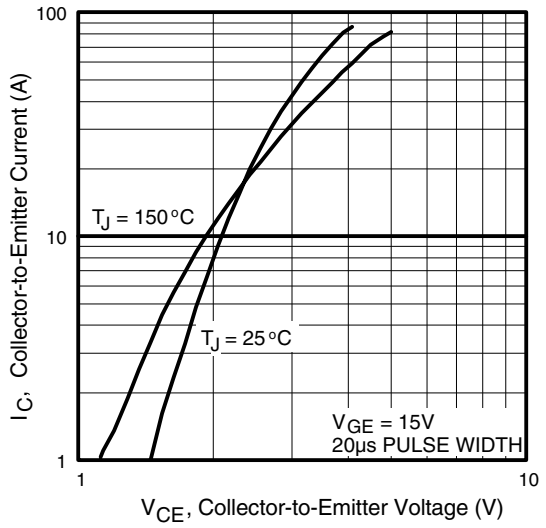


Fig. 2 - Typical Output Characteristics

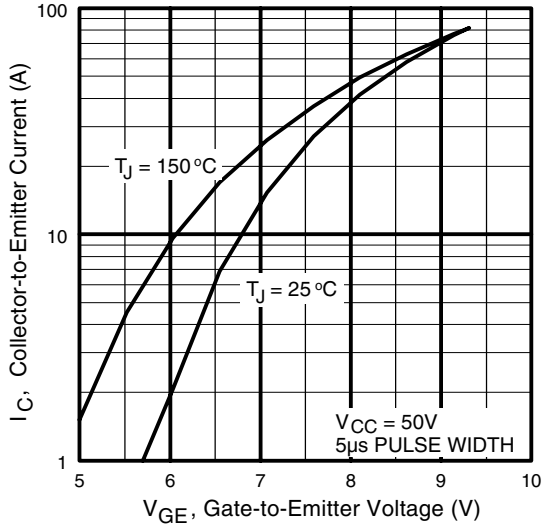


Fig. 3 - Typical Transfer Characteristics

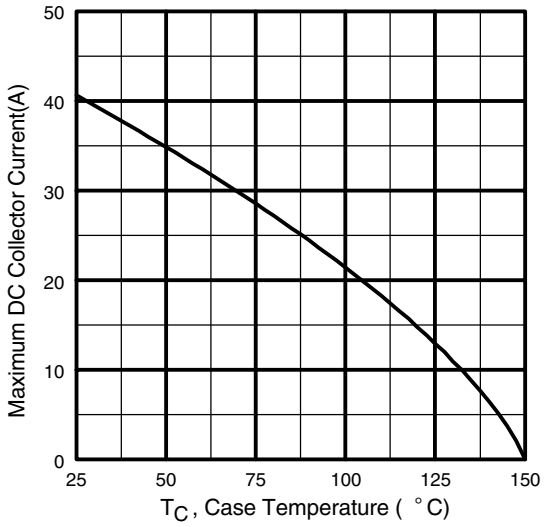


Fig. 4 - Maximum Collector Current vs. Case Temperature

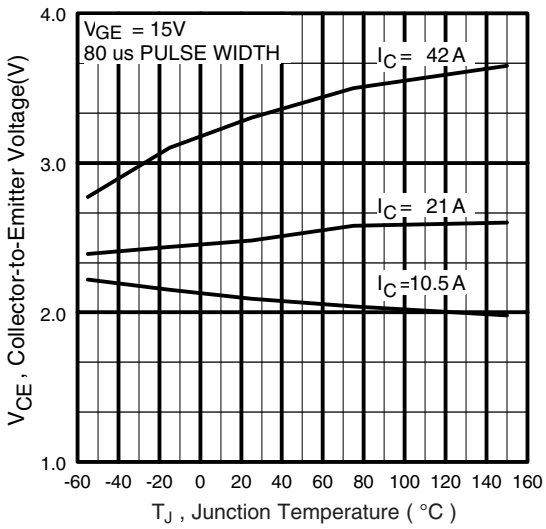


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

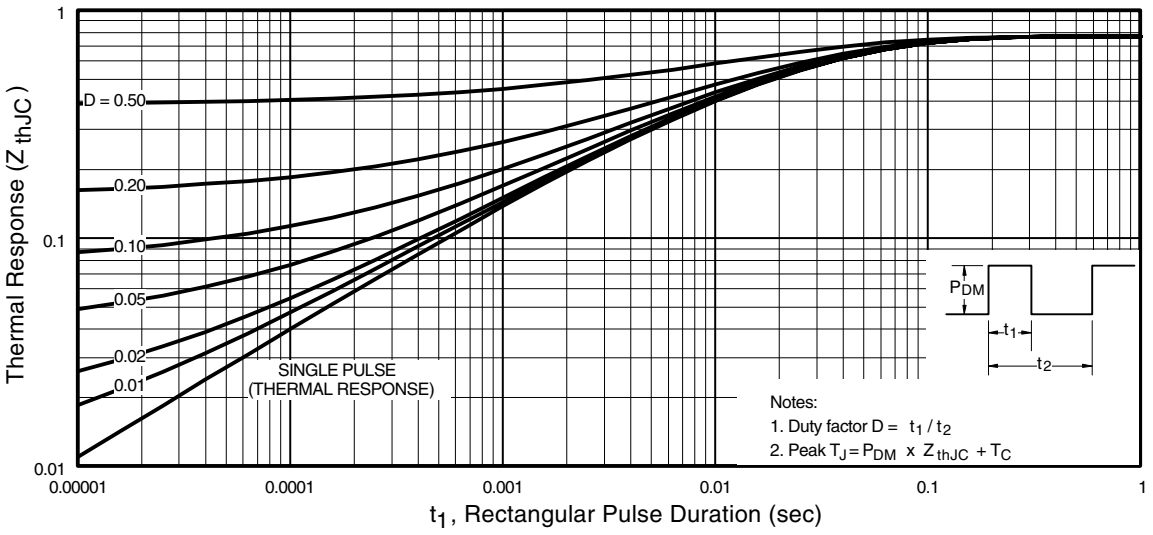


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

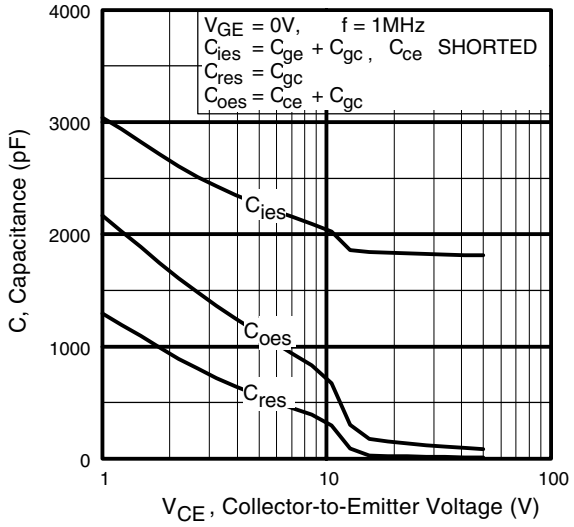


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

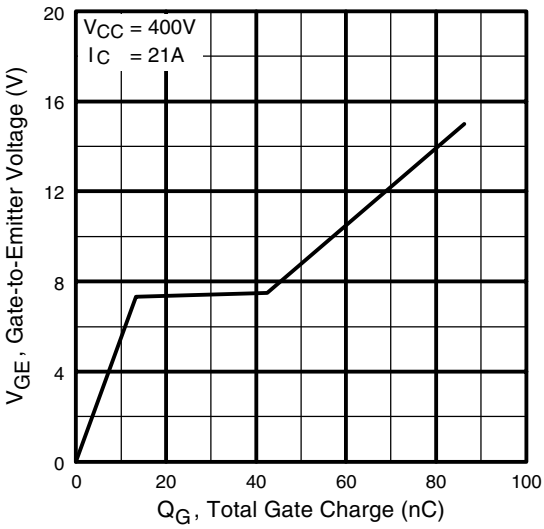


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

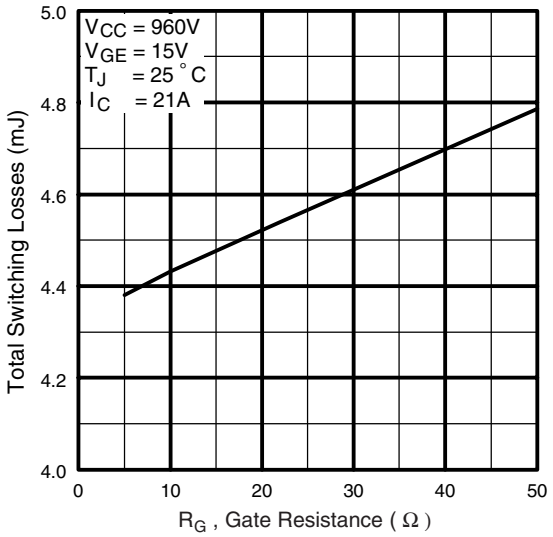


Fig. 9 - Typical Switching Losses vs. Gate Resistance

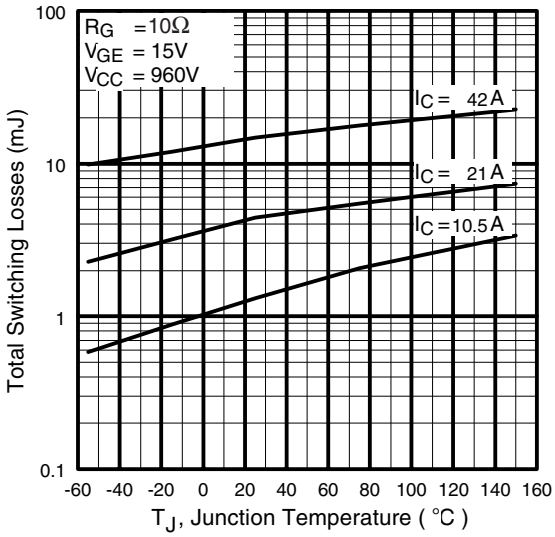


Fig. 10 - Typical Switching Losses vs. Junction Temperature

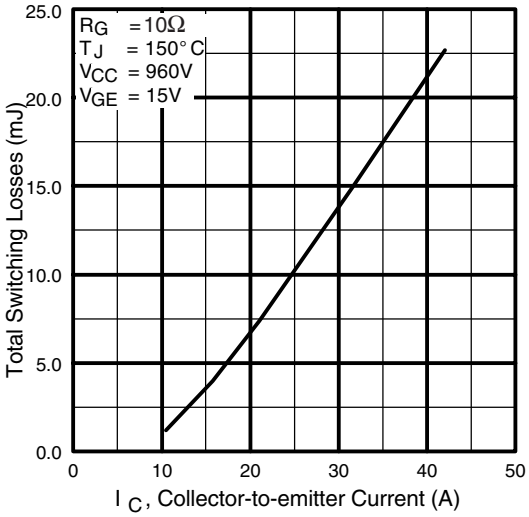


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

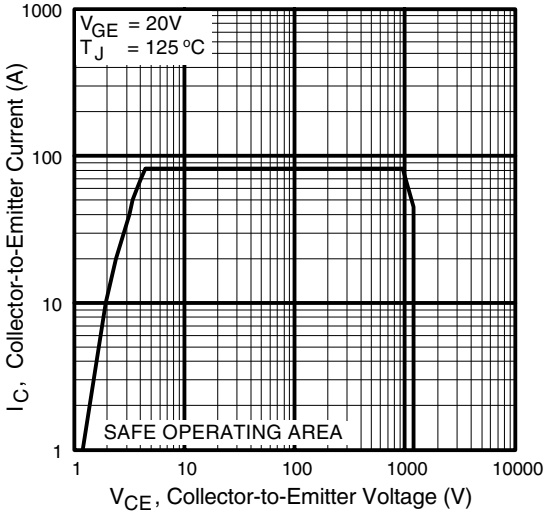


Fig. 12 - Turn-Off SOA

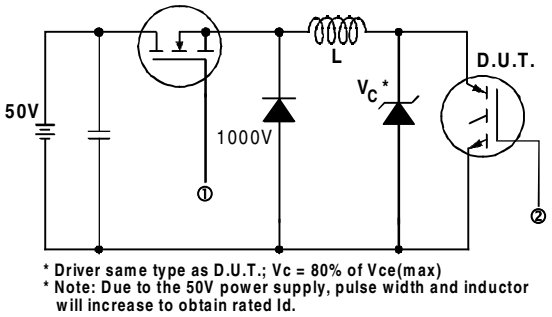


Fig. 13a - Clamped Inductive Load Test Circuit

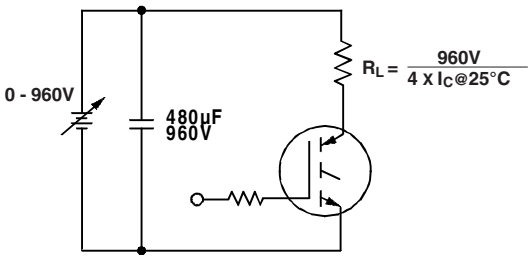


Fig. 13b - Pulsed Collector Current Test Circuit

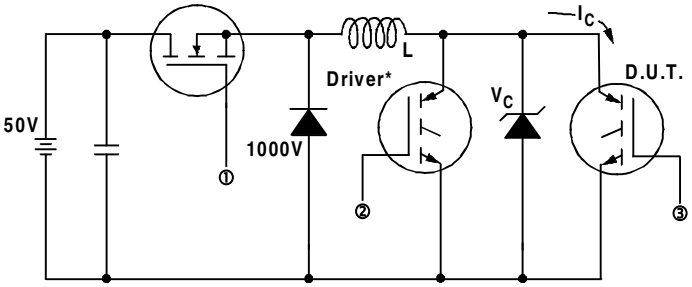


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 960V**

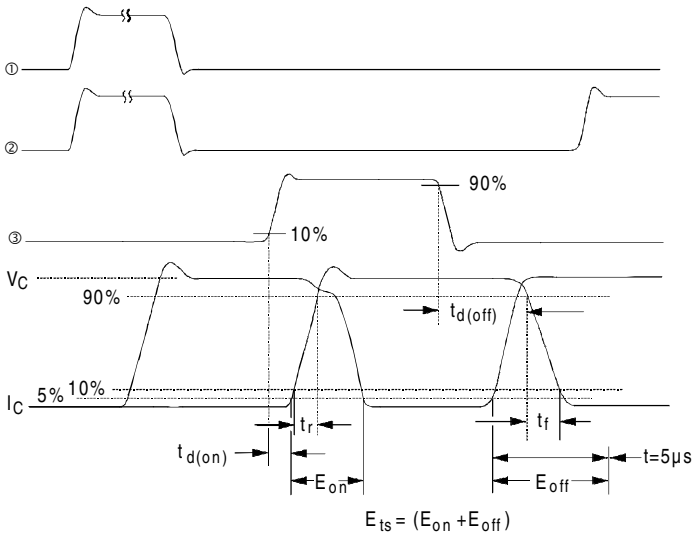
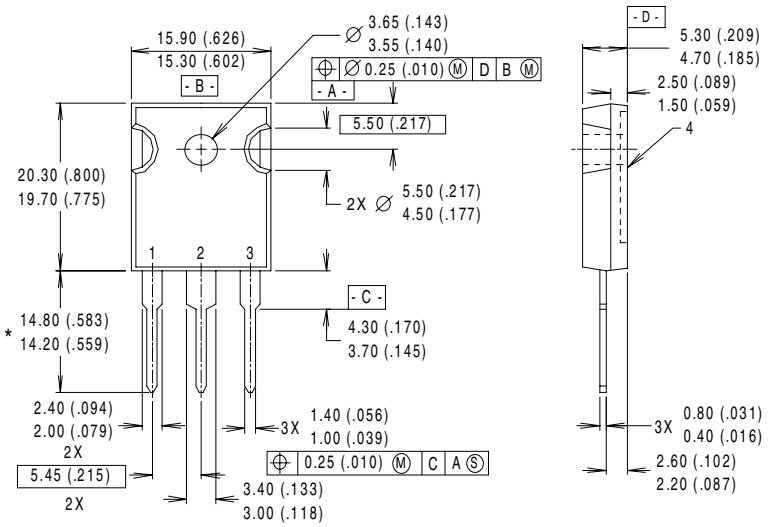


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 7/00

PD- 91621B

International
IOR Rectifier

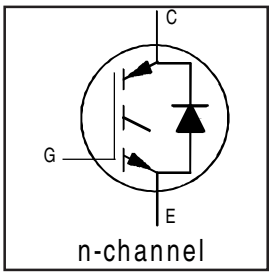
IRG4PH40UD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

UltraFast CoPack IGBT

Features

- UltraFast: Optimized for high operating frequencies up to 40 kHz in hard switching, >200 kHz in resonant mode
- New IGBT design provides tighter parameter distribution and higher efficiency than previous generations
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-247AC package

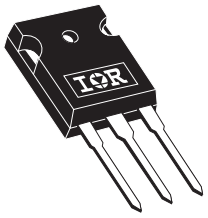


n-channel

V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.43V

@V_{GE} = 15V, I_C = 21A



TO-247AC

Benefits

- Higher switching frequency capability than competitive IGBTs
- Highest efficiency available
- HEXFRED diodes optimized for performance with IGBT's . Minimized recovery characteristics require less/no snubbing

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	41	A
I_C @ T_C = 100°C	Continuous Collector Current	21	
I_{CM}	Pulsed Collector Current ①	82	
I_{LM}	Clamped Inductive Load Current ②	82	
I_F @ T_C = 100°C	Diode Continuous Forward Current	8.0	
I_{FM}	Diode Maximum Forward Current	130	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	0.77	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	1.7	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	40	
Wt	Weight	—	6 (0.21)	—	g (oz)

7/7/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.43	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.43	3.1	V	I_C = 21A V_{GE} = 15V
		—	2.97	—		I_C = 41A See Fig. 2, 5
		—	2.47	—		I_C = 21A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	16	24	—	S	V_{CE} = 100V, I_C = 21A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	5000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	2.6	3.3	V	I_C = 8.0A See Fig. 13
		—	2.4	3.1		I_C = 8.0A, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	86	130		I_C = 21A
Qge	Gate - Emitter Charge (turn-on)	—	13	20	nC	V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	29	44		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	46	—		T_J = 25°C
t_r	Rise Time	—	35	—	ns	I_C = 21A, V_{CC} = 800V
$t_{d(off)}$	Turn-Off Delay Time	—	97	150		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	—	240	360		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	1.80	—		diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	1.93	—	mJ	See Fig. 9, 10, 18
E_{ts}	Total Switching Loss	—	3.73	4.6		
$t_{d(on)}$	Turn-On Delay Time	—	42	—		T_J = 150°C, See Fig. 11, 18
t_r	Rise Time	—	32	—	ns	I_C = 21A, V_{CC} = 800V
$t_{d(off)}$	Turn-Off Delay Time	—	240	—		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	—	510	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	7.04	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1800	—		V_{GE} = 0V
C_{oes}	Output Capacitance	—	120	—	pF	V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	18	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	63	95	ns	T_J = 25°C See Fig.
		—	106	160		T_J = 125°C 14 I_F = 8.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	4.5	8.0	A	T_J = 25°C See Fig.
		—	6.2	11		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	140	380	nC	T_J = 25°C See Fig.
		—	335	880		T_J = 125°C 16 di/dt = 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	133	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	85	—		T_J = 125°C 17

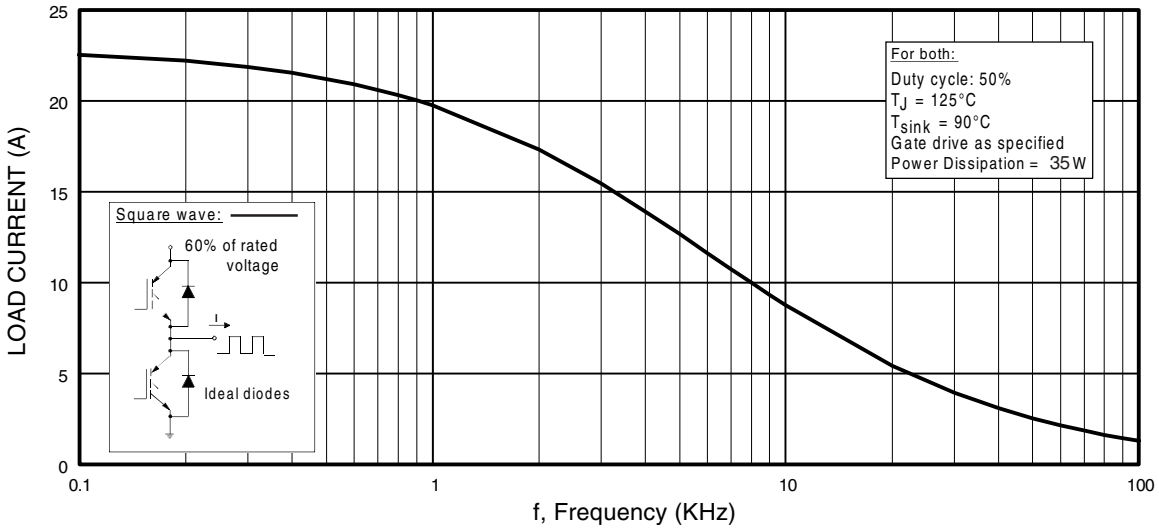


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

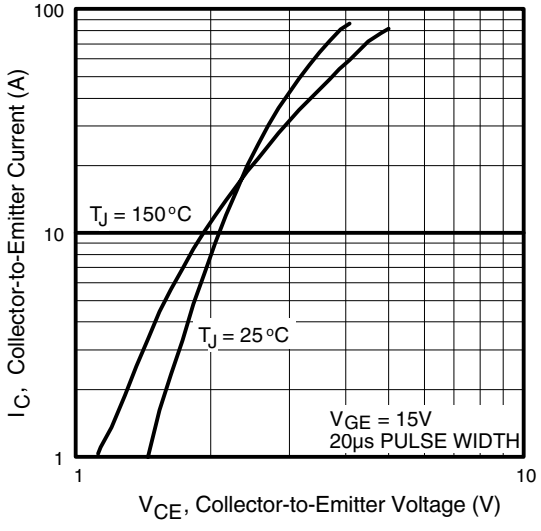


Fig. 2 - Typical Output Characteristics

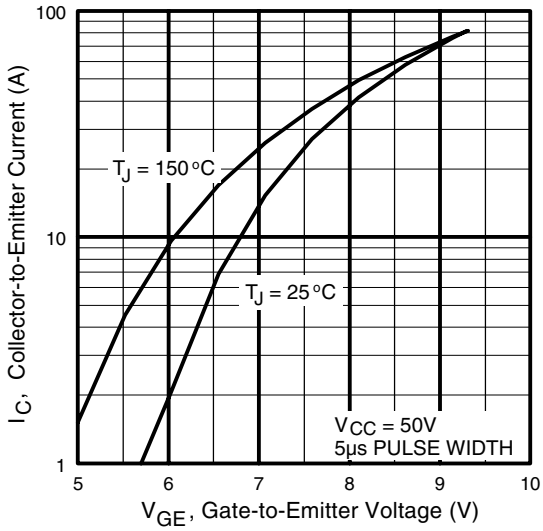


Fig. 3 - Typical Transfer Characteristics

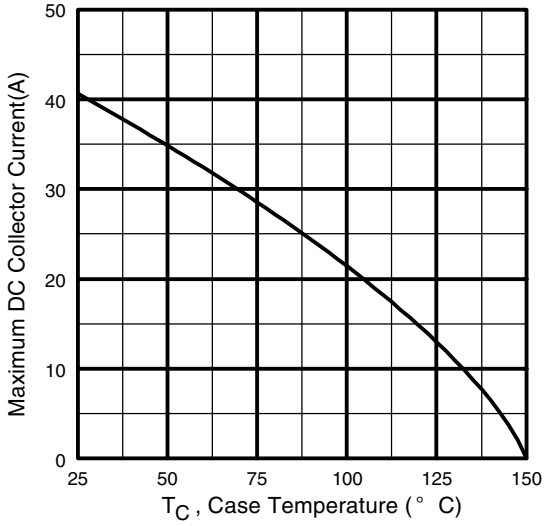


Fig. 4 - Maximum Collector Current vs. Case Temperature

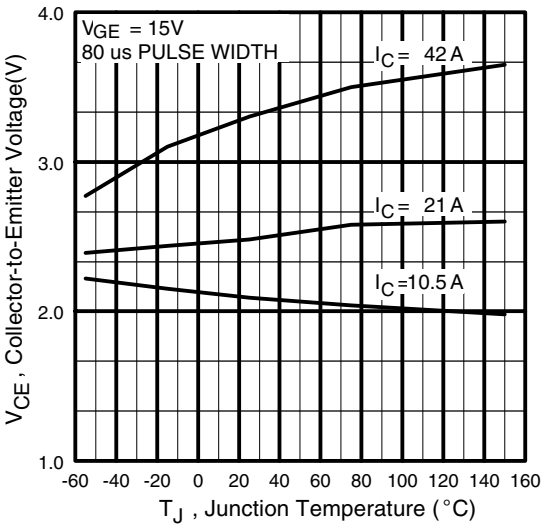


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

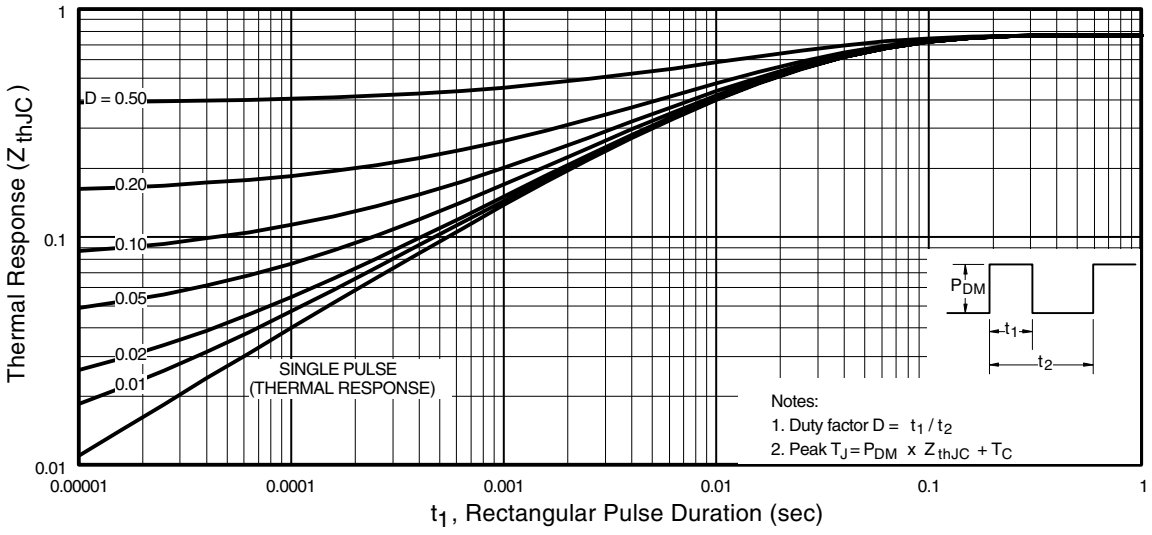


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

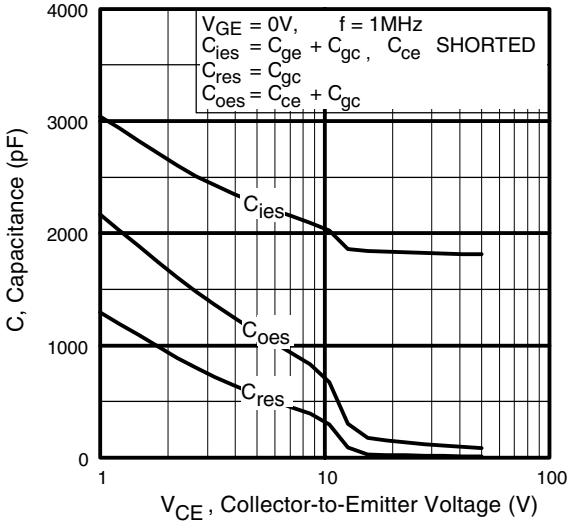


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

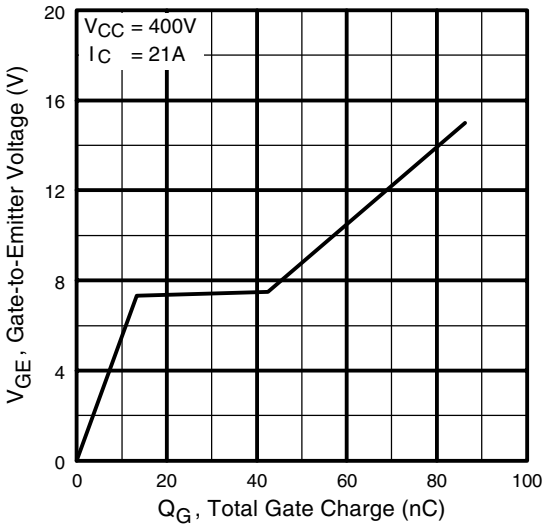


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

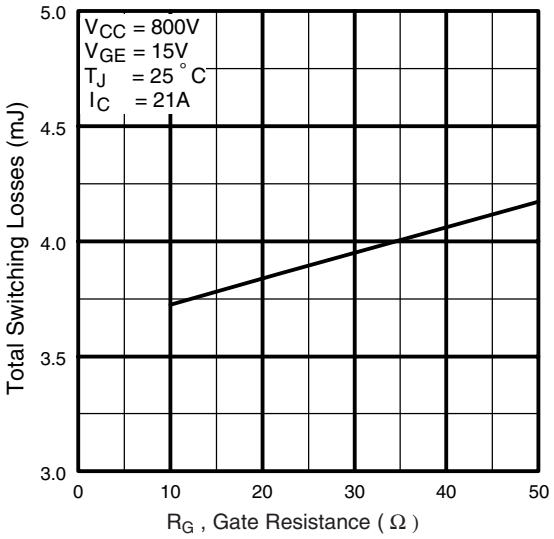


Fig. 9 - Typical Switching Losses vs. Gate Resistance

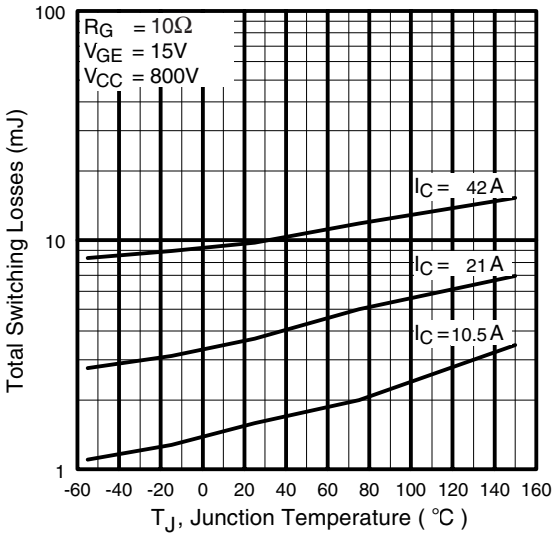


Fig. 10 - Typical Switching Losses vs. Junction Temperature

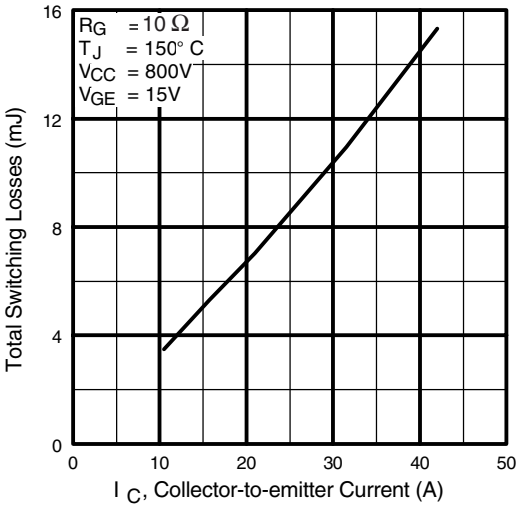


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

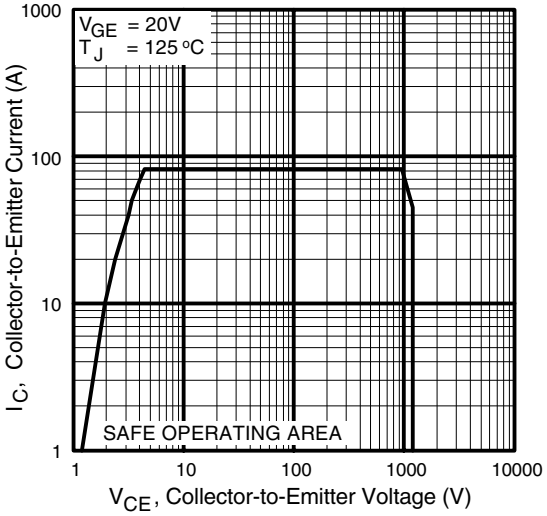


Fig. 12 - Turn-Off SOA

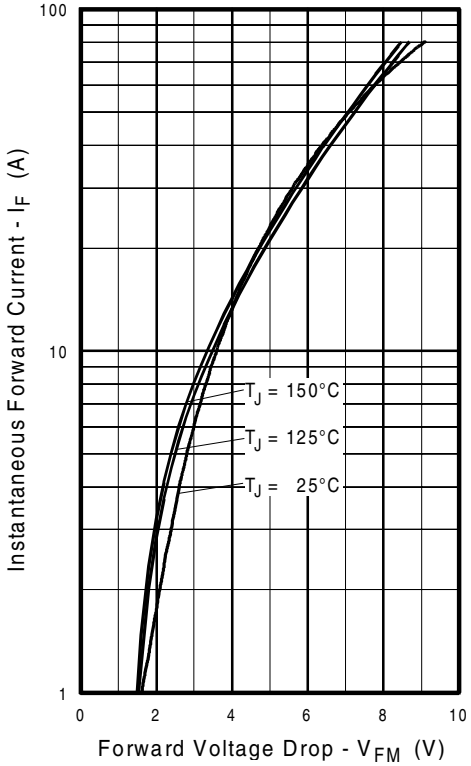


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

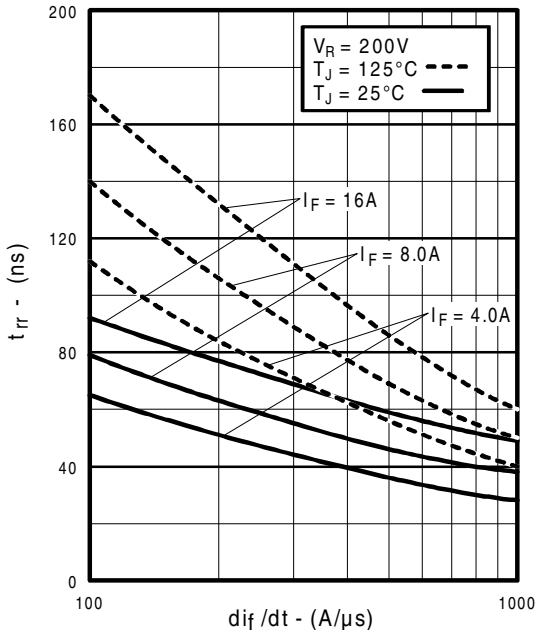


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

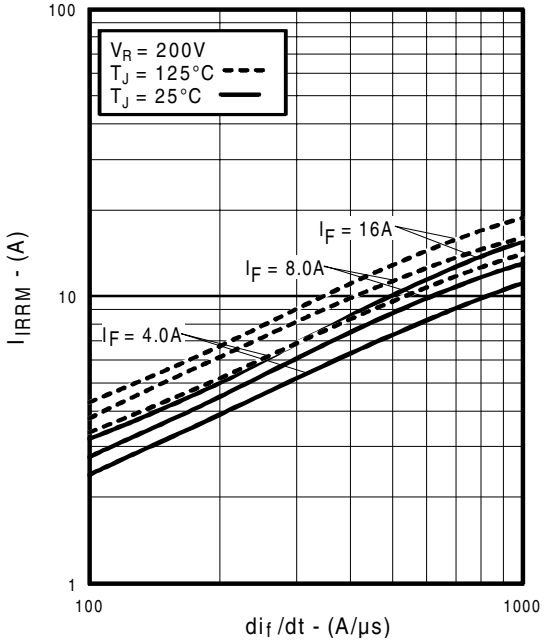


Fig. 15 - Typical Recovery Current vs. di_f/dt

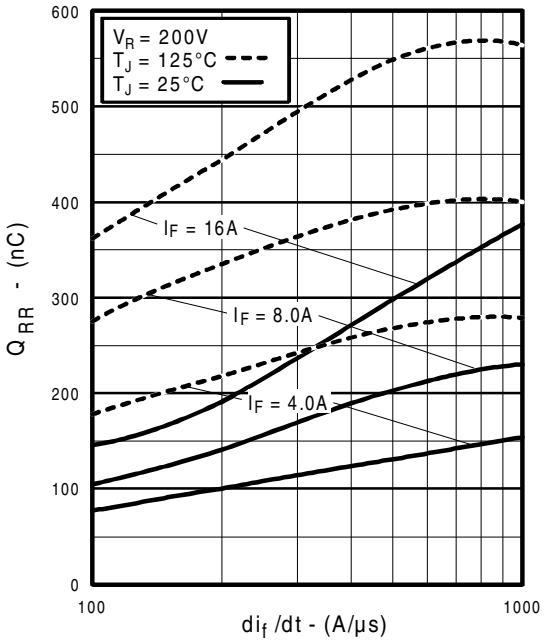


Fig. 16 - Typical Stored Charge vs. di_f/dt

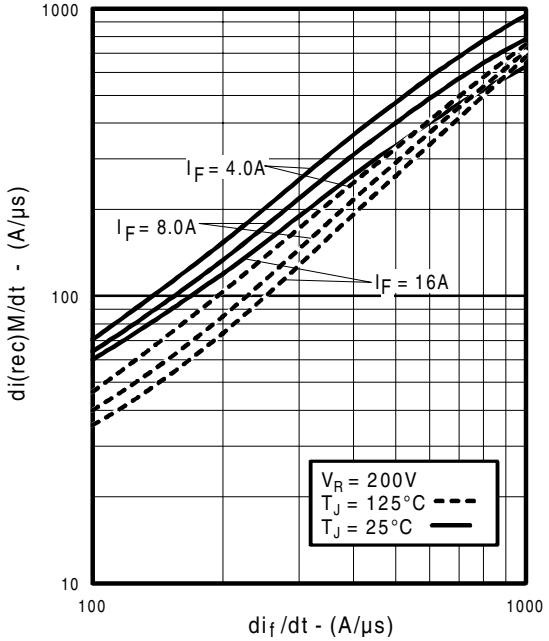


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

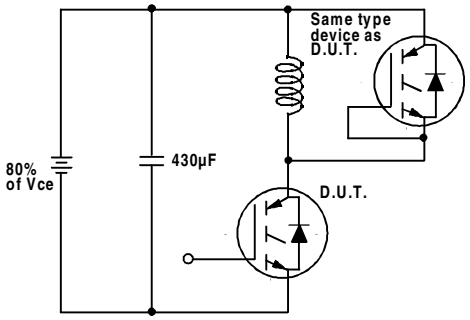


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

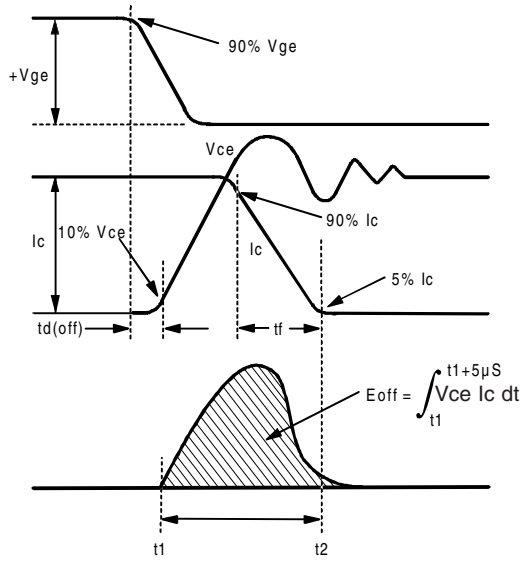


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

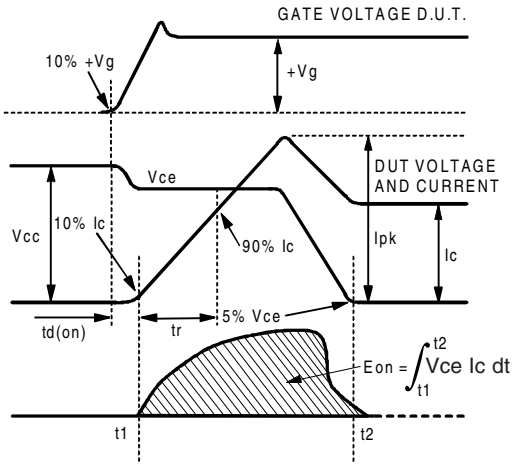


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

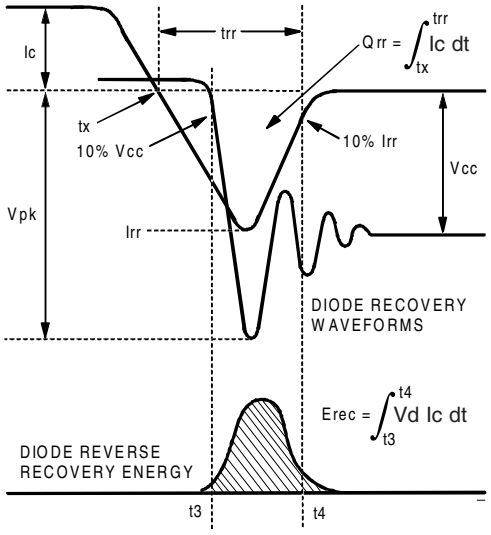


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

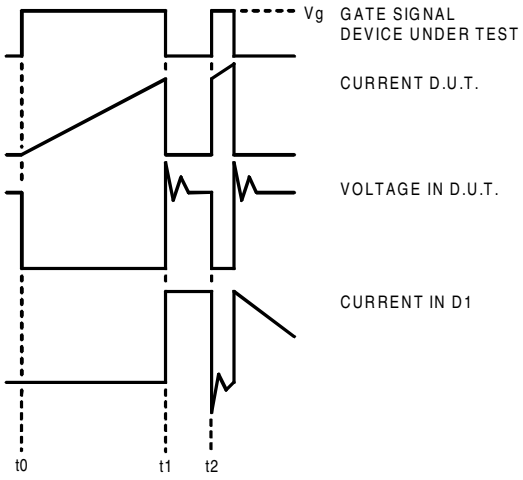


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

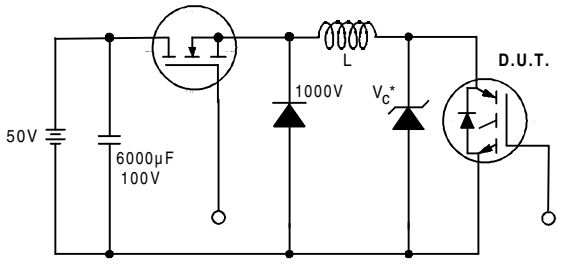


Figure 19. Clamped Inductive Load Test Circuit

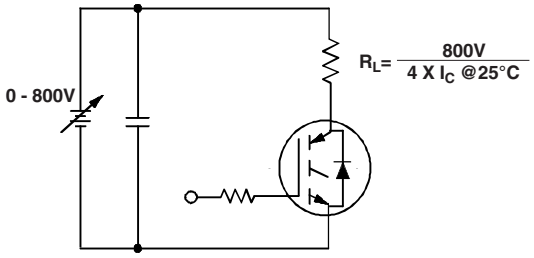


Figure 20. Pulsed Collector Current Test Circuit

Notes:

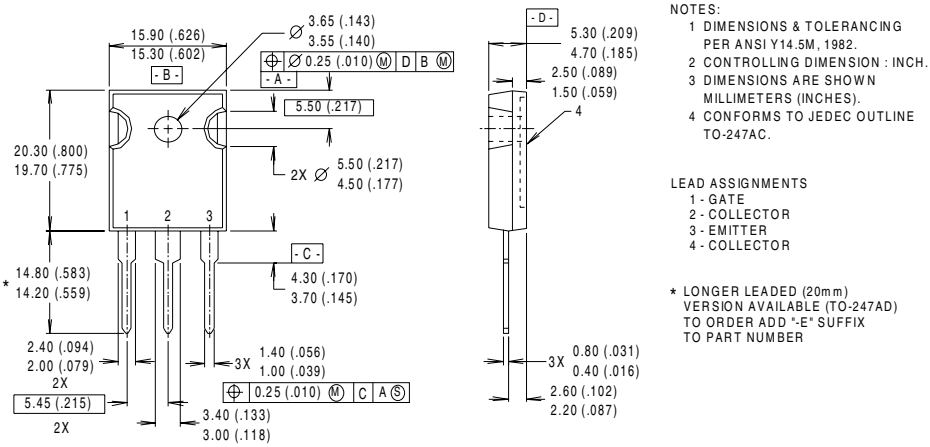
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 10Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
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IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
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IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 7/00

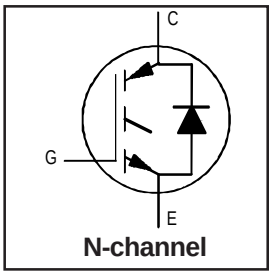
International
IOR Rectifier

PD - 93765

IRG4IBC10UD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

UltraFast Co-Pack IGBT



N-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.15V

@V_{GE} = 15V, I_C = 5.0A

$t_{f(typ.)}$ = 140ns

Features

- UltraFast: Optimized for high operating up to 80 kHz in hard switching, > 200 kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than previous generation
- IGBT co-packaged with HEXFRED® ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-220 Full-Pak

Benefits

- Generation 4 IGBTs offer highest efficiencies available
- IGBTs optimized for specific application conditions
- HEXFRED® diodes optimized for performance with IGBTs Minimized recovery characteristics require less/no snubbing


TO-220 Full-Pak

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	6.8	A
I_C @ T_C = 100°C	Continuous Collector Current	3.9	
I_{CM}	Pulsed Collector Current ①	27	
I_{LM}	Clamped Inductive Load Current ②	27	
I_F @ T_C = 100°C	Diode Continuous Forward Current	3.9	
I_{FM}	Diode Maximum Forward Current	27	
V_{ISOL}	RMS Isolated Voltage, Terminal to case, t=1min	2500	V
V_{GE}	Gate-to-Emitter Voltage	± 20	
P_D @ T_C = 25°C	Maximum Power Dissipation	25	W
P_D @ T_C = 100°C	Maximum Power Dissipation	10	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	5.0	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	9.0	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	65	
Wt	Weight	2.1 (0.075)	—	g (oz)

10/27/99

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage ③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$DV_{(BR)CES}/DT_J$	Temperature Coeff. of Breakdown Voltage	—	0.54	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.15	2.6	V	I_C = 5.0A V_{GE} = 15V
		—	2.61	—		I_C = 8.5A See Fig. 2, 5
		—	2.30	—		I_C = 5.0A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage ④	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$DV_{GE(th)}/DT_J$	Temperature Coeff. of Threshold Voltage	—	-8.7	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance	2.8	4.2	—	S	V_{CE} = 100V, I_C = 5.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.5	1.8	V	I_C = 4.0A See Fig. 13
		—	1.4	1.7		I_C = 4.0A, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	15	22	nC	I_C = 5.0A
Qge	Gate - Emitter Charge (turn-on)	—	2.6	4.0		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	5.8	8.7		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	40	—	ns	T_J = 25°C
t_r	Rise Time	—	16	—		I_C = 5.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	87	130		V_{GE} = 15V, R_G = 100W
t_f	Fall Time	—	140	210		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	0.14	—	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	0.12	—		See Fig. 9, 10, 18
E_{ts}	Total Switching Loss	—	0.26	0.33		
$t_{d(on)}$	Turn-On Delay Time	—	38	—	ns	T_J = 150°C, See Fig. 11, 18
t_r	Rise Time	—	18	—		I_C = 5.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	95	—		V_{GE} = 15V, R_G = 100W
t_f	Fall Time	—	250	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	0.45	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	270	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	21	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	3.5	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	28	42	ns	T_J = 25°C See Fig. 14 I_F = 4.0A
		—	38	57		T_J = 125°C
I_{rr}	Diode Peak Reverse Recovery Current	—	2.9	5.2	A	T_J = 25°C See Fig. 15 V_R = 200V
		—	3.7	6.7		T_J = 125°C
Q_{rr}	Diode Reverse Recovery Charge	—	40	60	nC	T_J = 25°C See Fig. 16 di/dt = 200A/µs
		—	70	105		T_J = 125°C
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	280	—	A/µs	T_J = 25°C See Fig. 17
	During t_b	—	235	—		T_J = 125°C

Details of note ① through ④ are on the last page

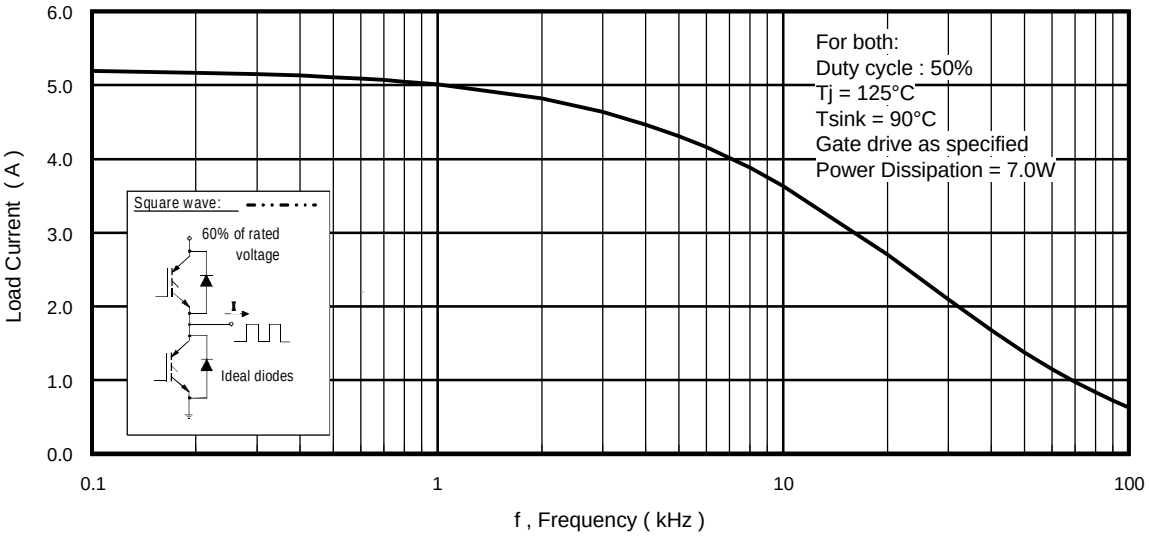


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

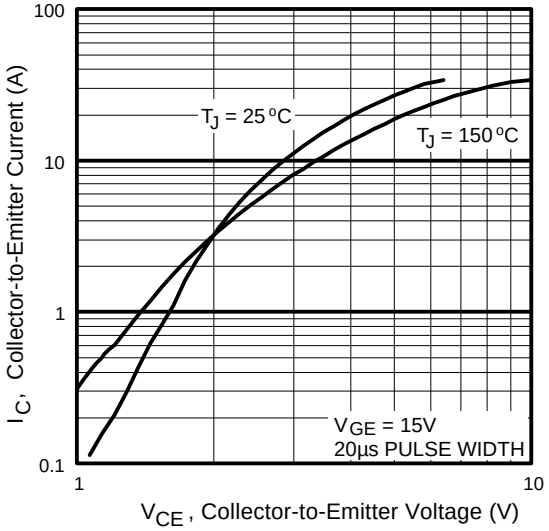


Fig. 2 - Typical Output Characteristics

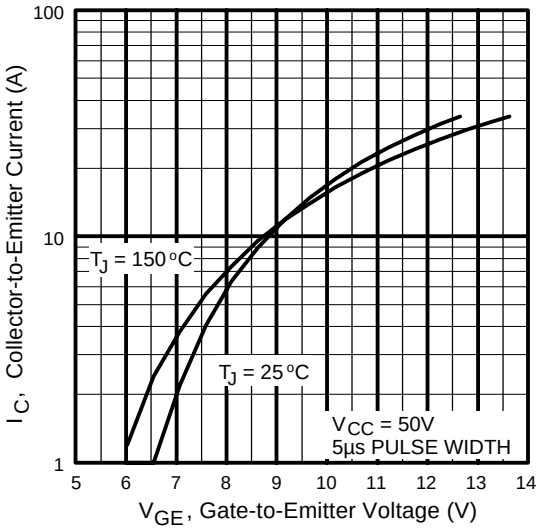


Fig. 3 - Typical Transfer Characteristics

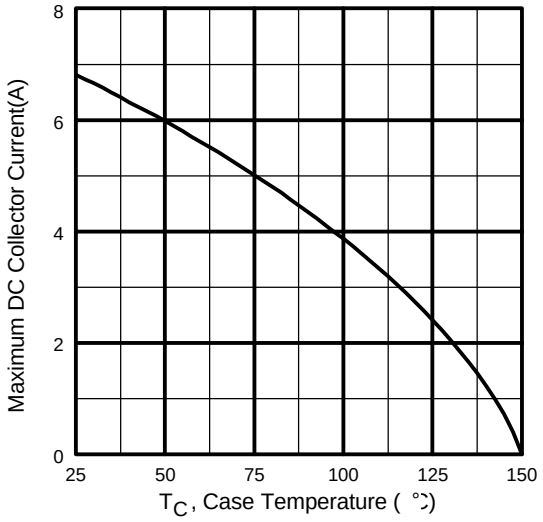


Fig. 4 - Maximum Collector Current vs. Case Temperature

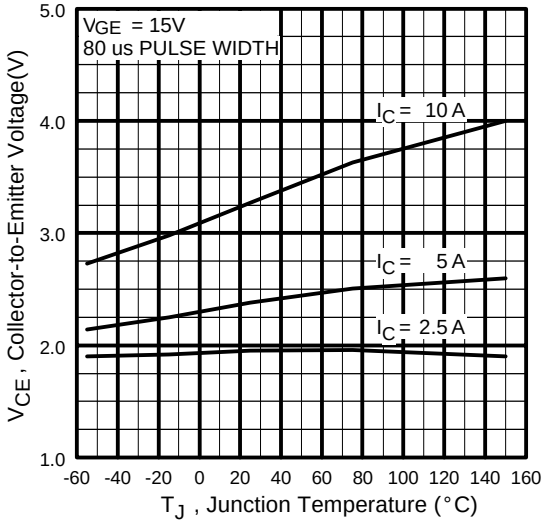


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

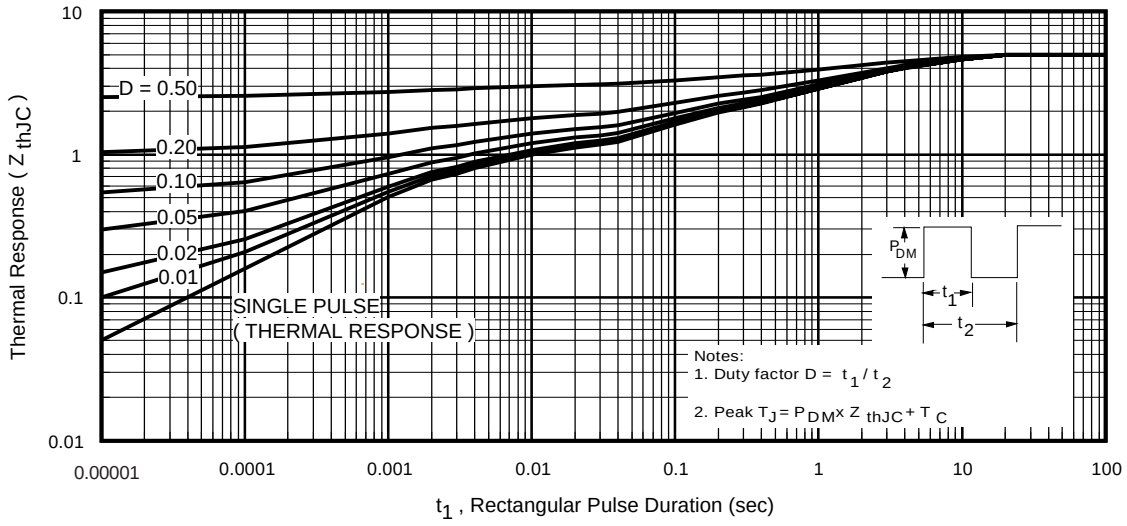


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

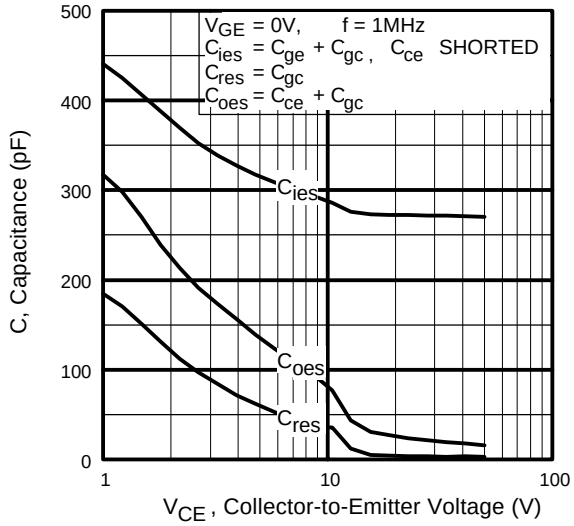


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

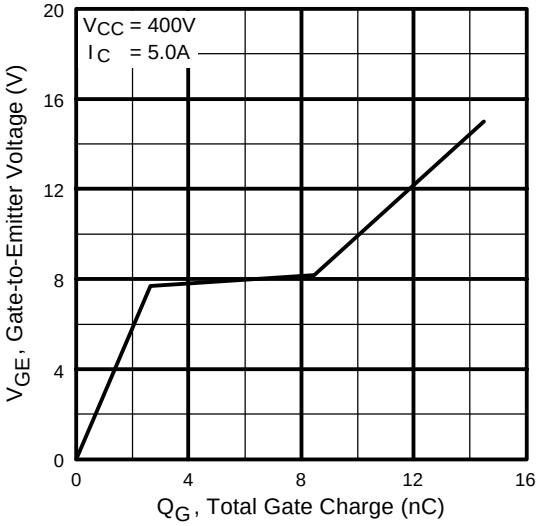


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

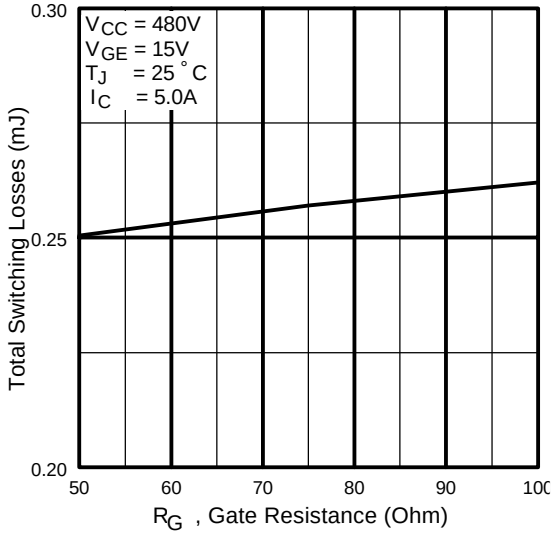


Fig. 9 - Typical Switching Losses vs. Gate Resistance

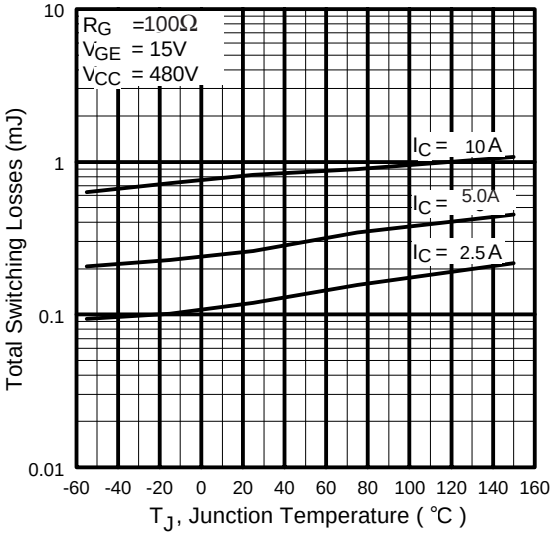


Fig. 10 - Typical Switching Losses vs. Junction Temperature

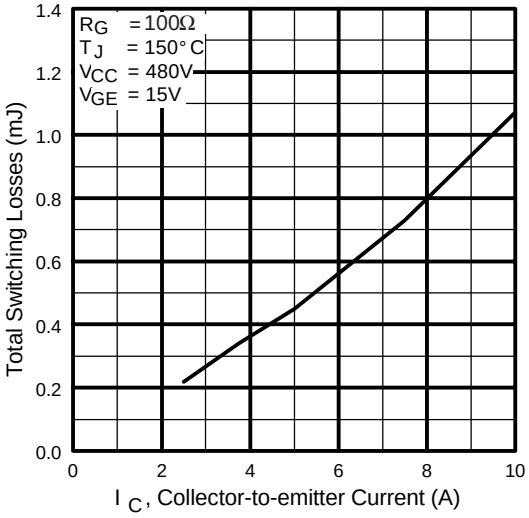


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

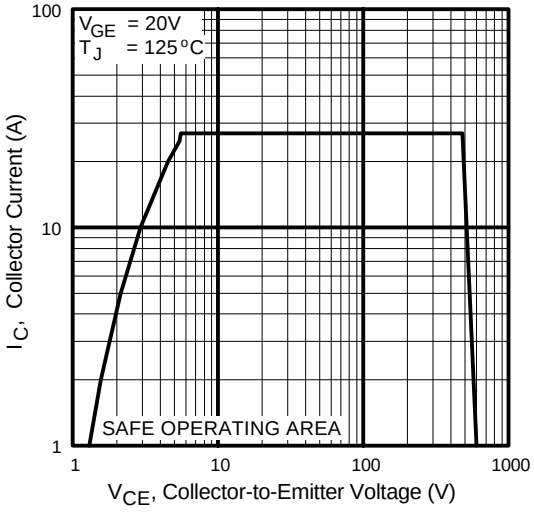


Fig. 12 - Turn-Off SOA

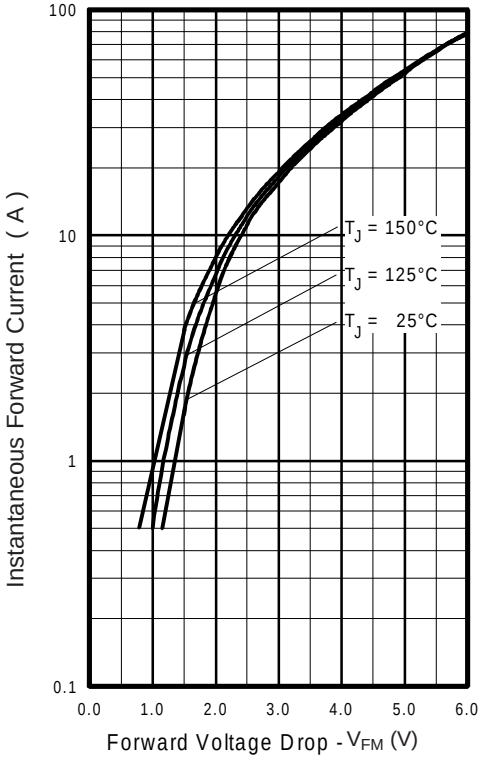


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

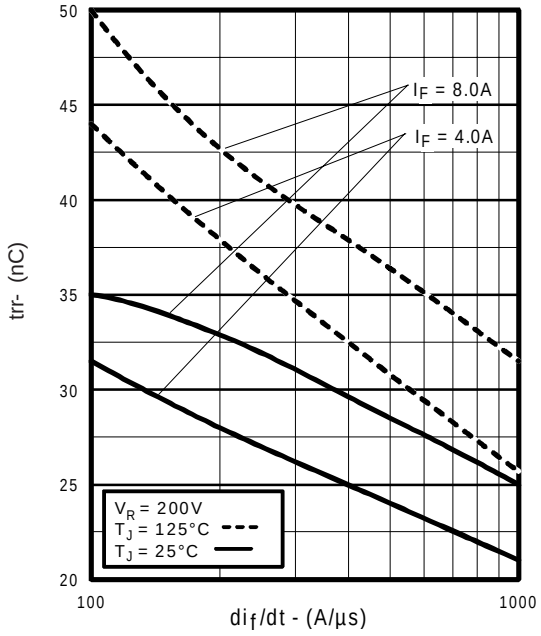


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

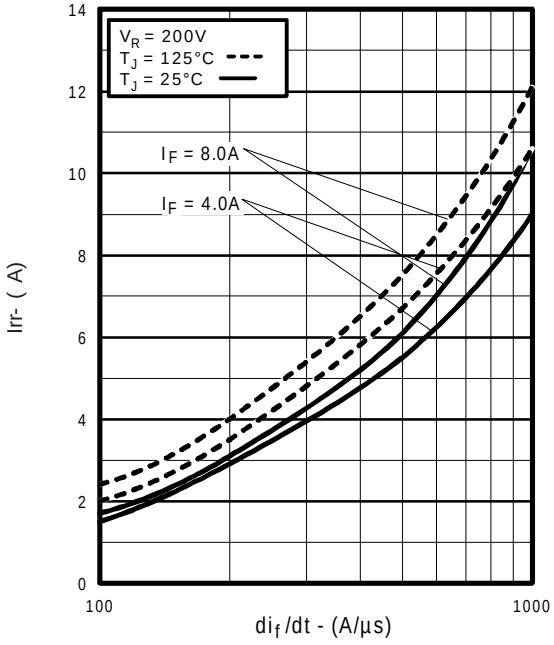


Fig. 15 - Typical Recovery Current vs. di_f/dt

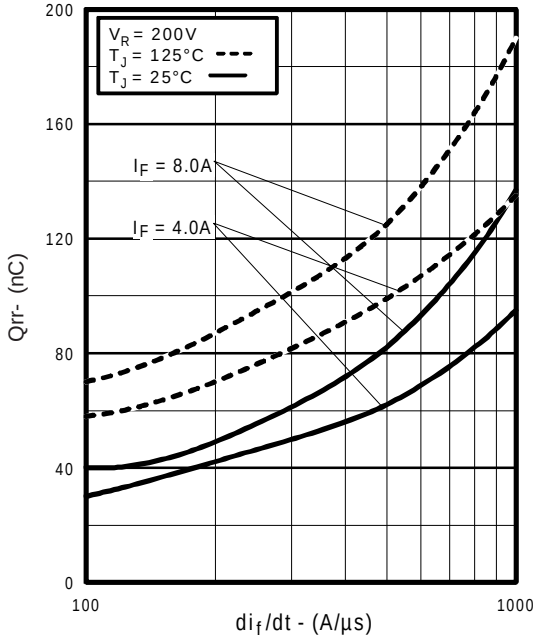


Fig. 16 - Typical Stored Charge vs. di_f/dt

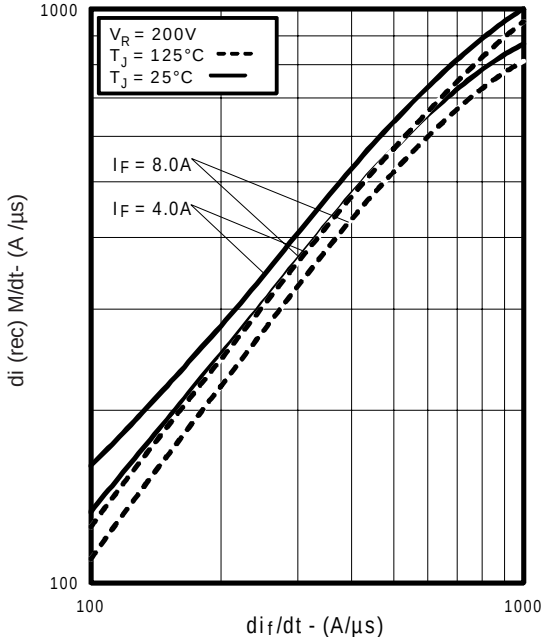


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

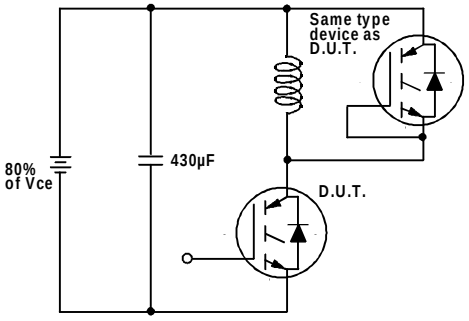


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

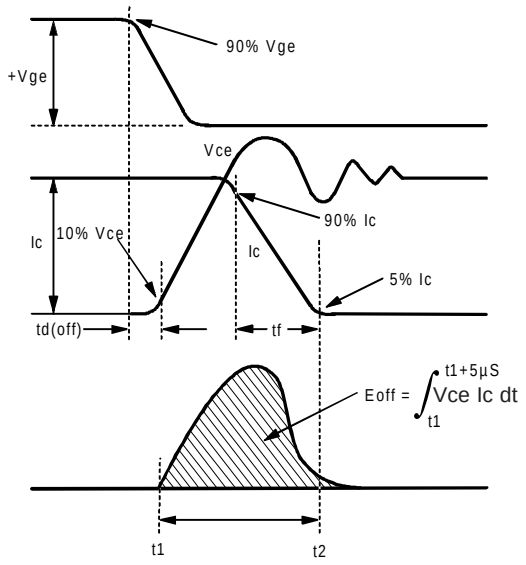


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

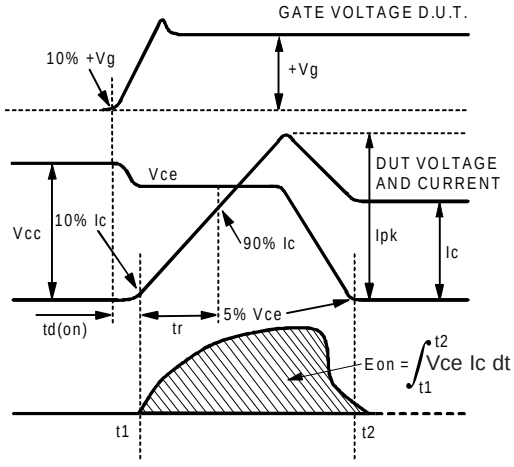


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

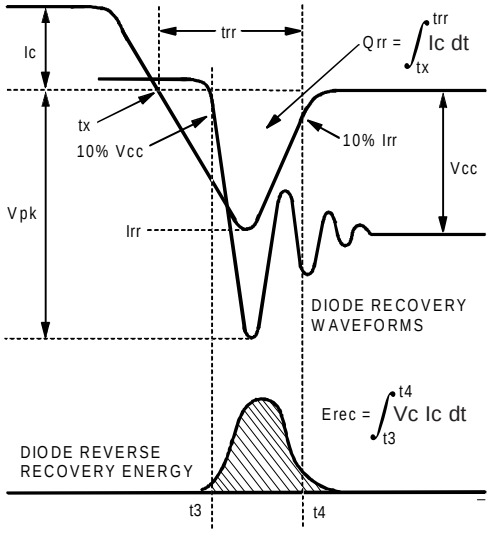


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

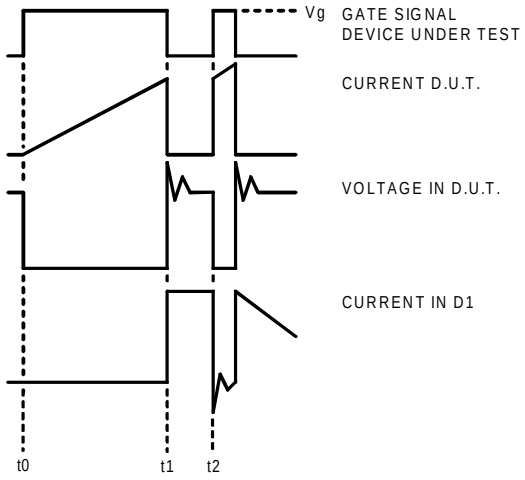


Fig. 18e - Macro Waveforms for Figure 18a's Test Circuit

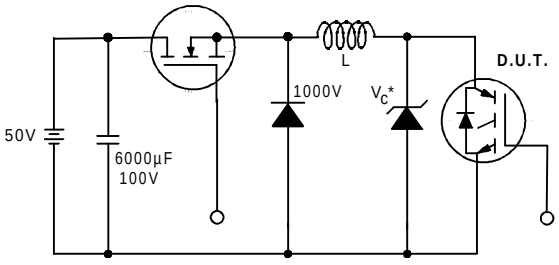


Fig. 19 - Clamped Inductive Load Test Circuit

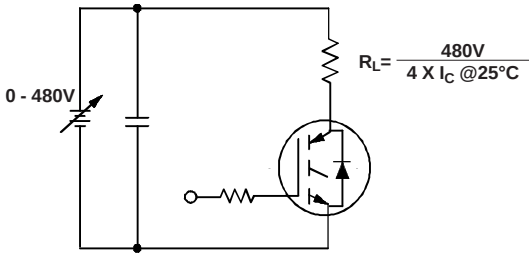
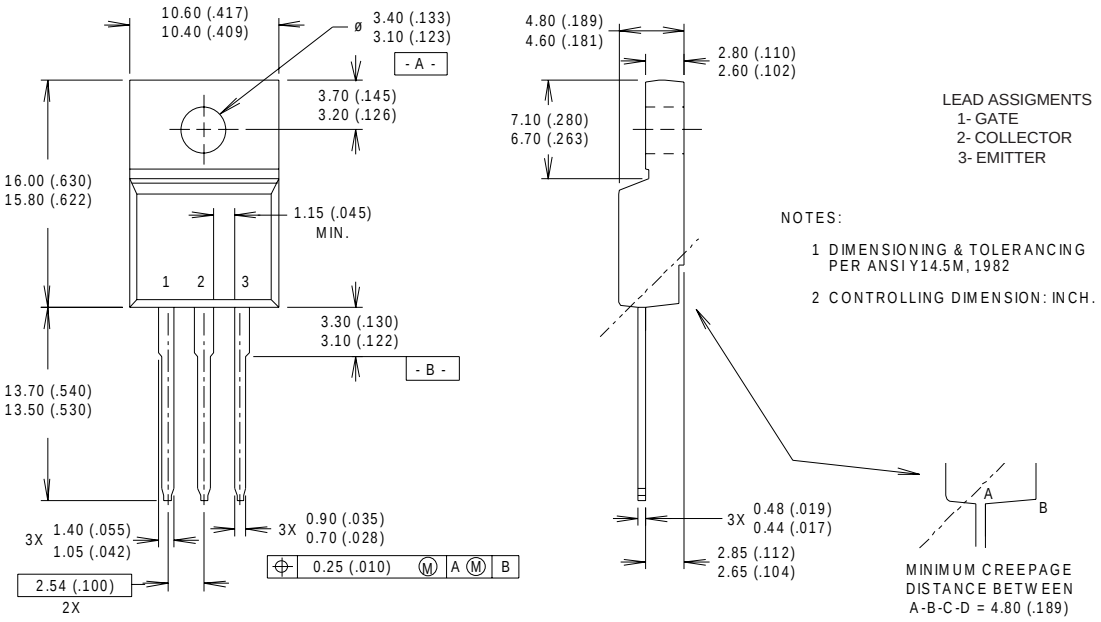


Fig. 20 - Pulsed Collector Current Test Circuit

TO-220 Full-Pak Package Outline



Notes

① Repetitive rating: V_{GE}=20V; Pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 100Ω (figure 19)

③ Pulse width ≤ 80µs, duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

International
IOR Rectifier

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IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936

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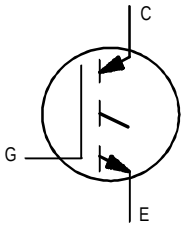
IRG4RC10U

INSULATED GATE BIPOLAR TRANSISTOR

UltraFast Speed IGBT

Features

- UltraFast: Optimized for high operating frequencies (8-40 kHz in hard switching, >200 kHz in resonant mode)
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than previous generation
- Industry standard TO-252AA package



n-channel

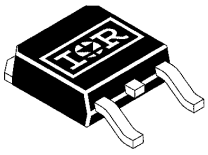
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.15V

@V_{GE} = 15V, I_C = 5.0A

Benefits

- Generation 4 IGBT's offer highest efficiency available
- IGBT's optimized for specified application conditions



D-PAK
TO-252AA

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	8.5	A
I_C @ T_C = 100°C	Continuous Collector Current	5.0	
I_{CM}	Pulsed Collector Current ①	34	
I_{LM}	Clamped Inductive Load Current ②	34	
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	110	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	38	W
P_D @ T_C = 100°C	Maximum Power Dissipation	15	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	3.3	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	——	50	
Wt	Weight	0.3 (0.01)	——	g (oz)

* When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	14	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.54	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.15	2.6	V	I_C = 5.0A V_{GE} = 15V
		—	2.61	—		I_C = 8.5A See Fig.2, 5
		—	2.30	—		I_C = 5.0A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-8.7	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	2.8	4.2	—	S	V_{CE} = 100V, I_C = 5.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	15	22	nC	I_C = 5.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	2.6	4.0		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	5.8	8.7		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	19	—	ns	
t_r	Rise Time	—	11	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	116	240		I_C = 5.0A, V_{CC} = 480V
t_f	Fall Time	—	81	180		V_{GE} = 15V, R_G = 100Ω
E_{on}	Turn-On Switching Loss	—	0.08	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.16	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	0.24	0.36		
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	T_J = 150°C,
t_r	Rise Time	—	14	—		I_C = 5.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	180	—		V_{GE} = 15V, R_G = 100Ω
t_f	Fall Time	—	150	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.36	—	mJ	See Fig. 11, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	270	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	21	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	3.5	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 100Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

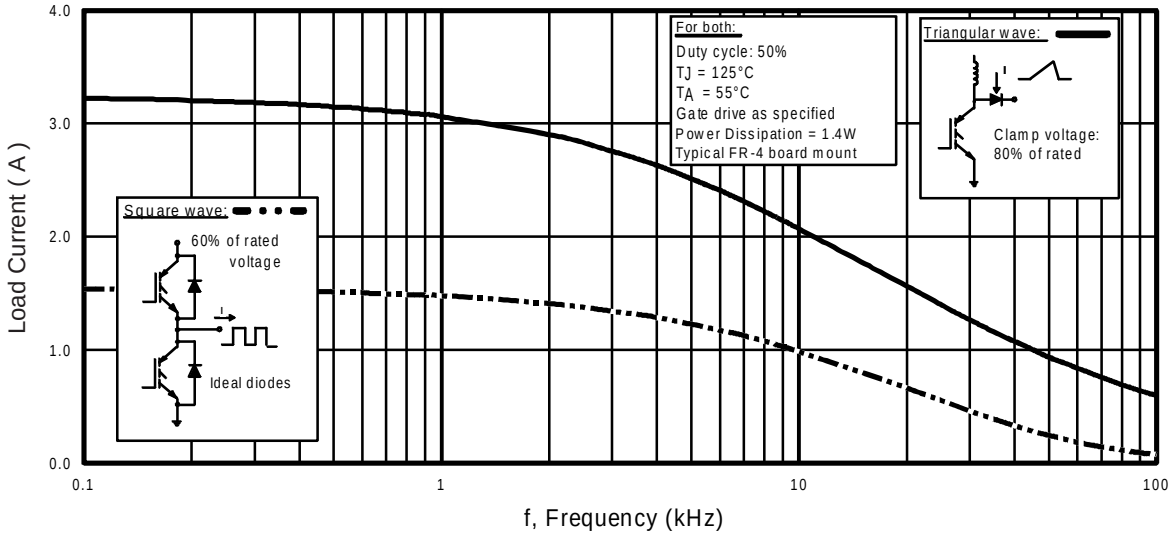


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

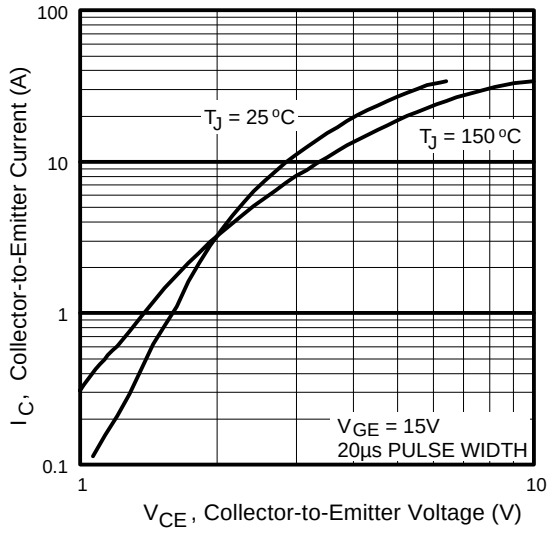


Fig. 2 - Typical Output Characteristics

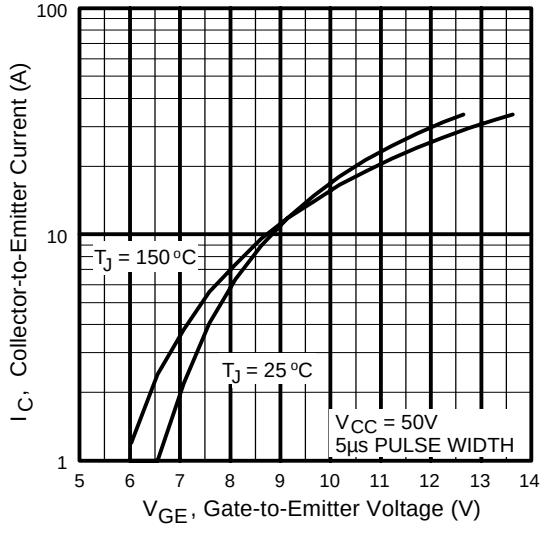


Fig. 3 - Typical Transfer Characteristics

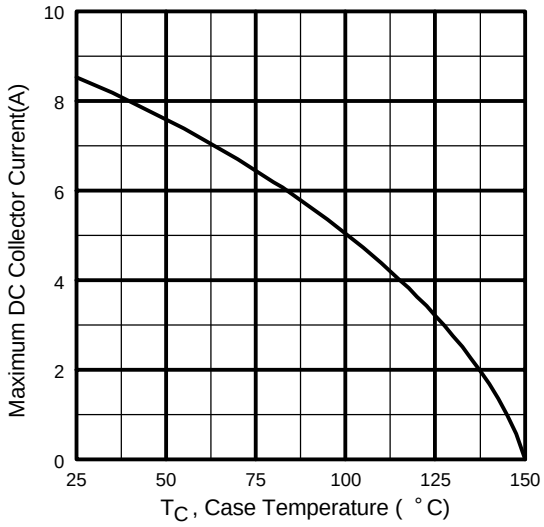


Fig. 4 - Maximum Collector Current vs. Case Temperature

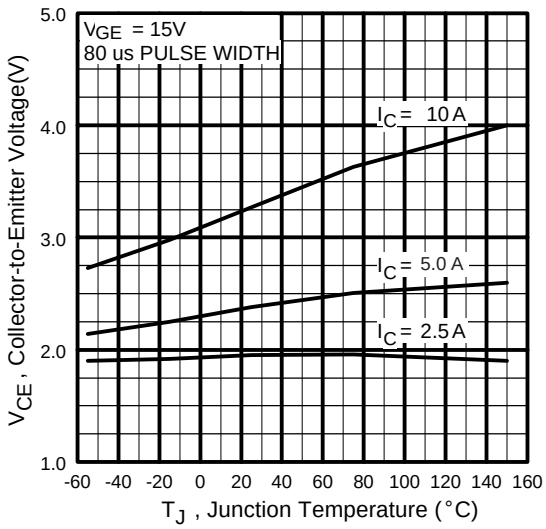


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

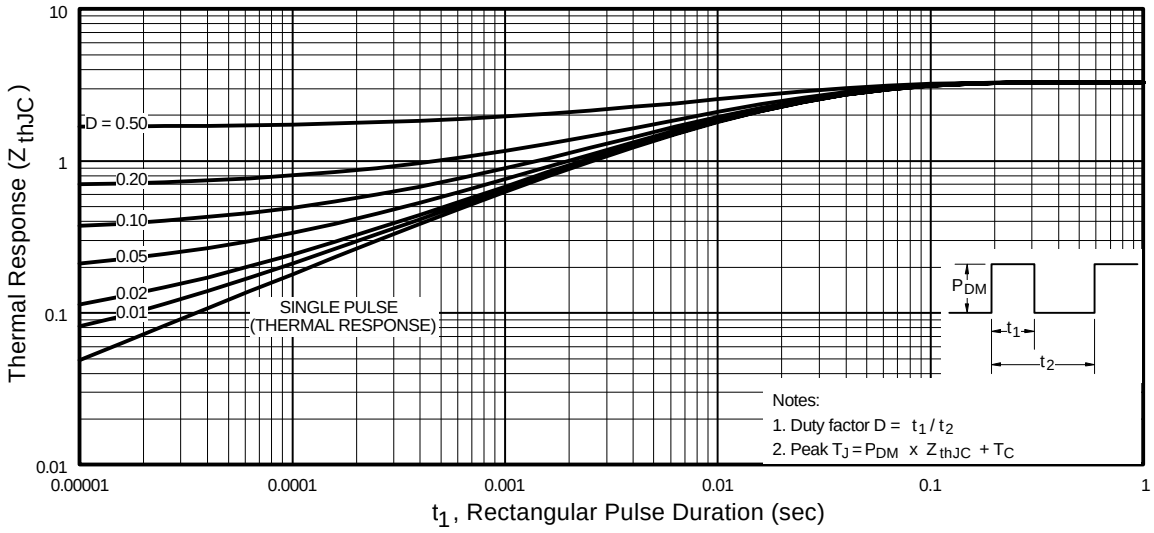


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

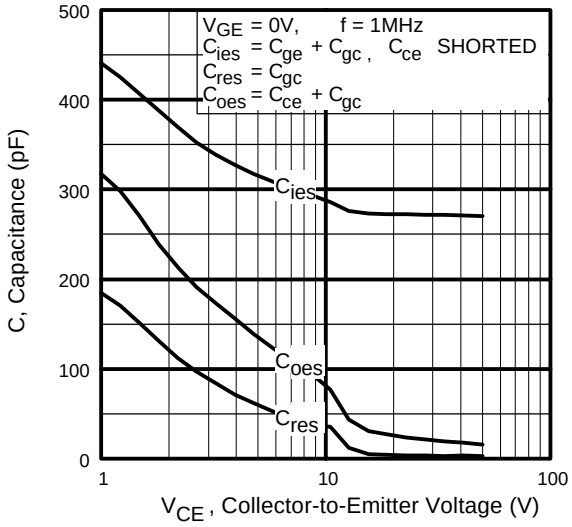


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

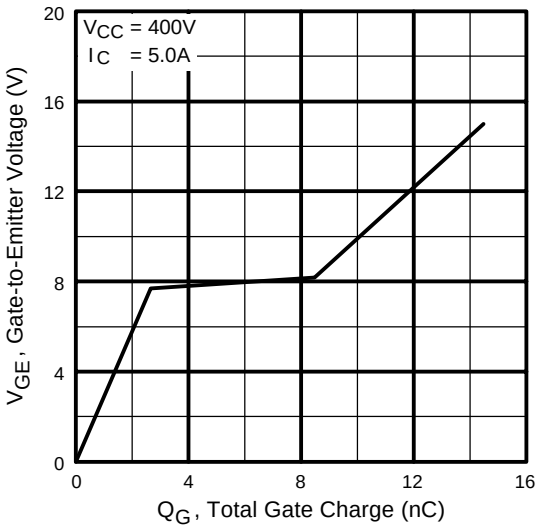


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

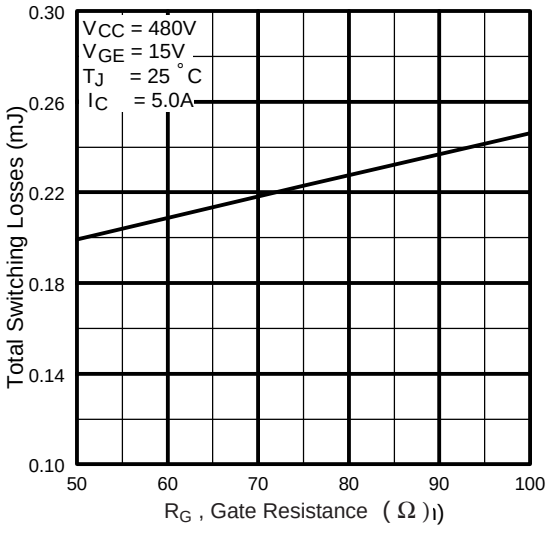


Fig. 9 - Typical Switching Losses vs. Gate Resistance

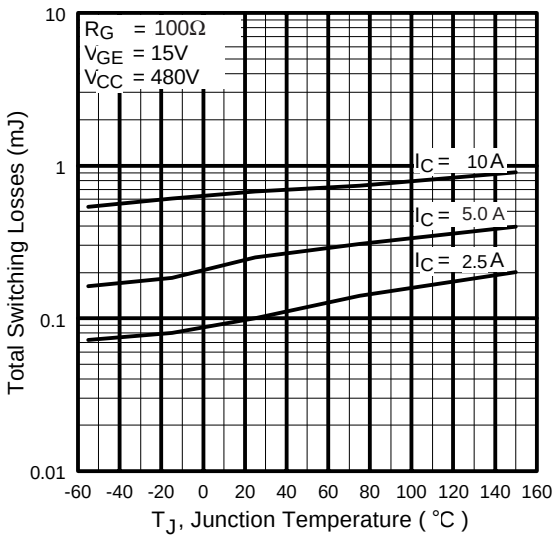


Fig. 10 - Typical Switching Losses vs. Junction Temperature

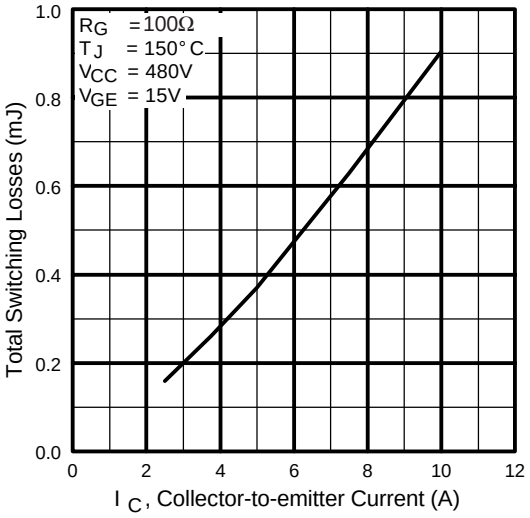


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

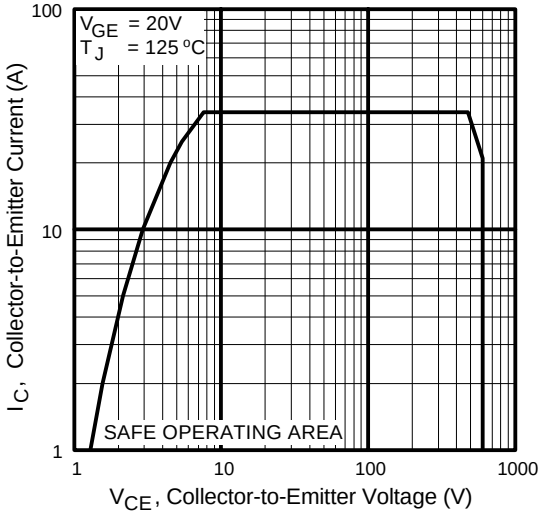


Fig. 12 - Turn-Off SOA

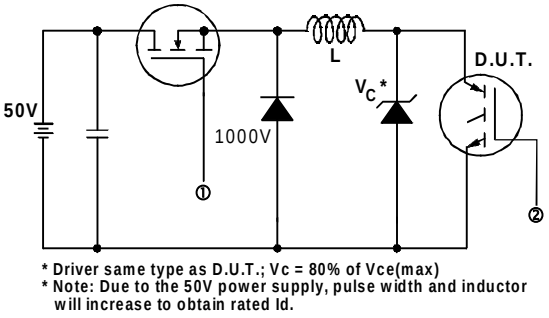


Fig. 13a - Clamped Inductive Load Test Circuit

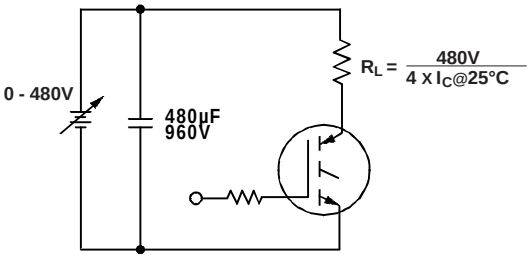


Fig. 13b - Pulsed Collector Current Test Circuit

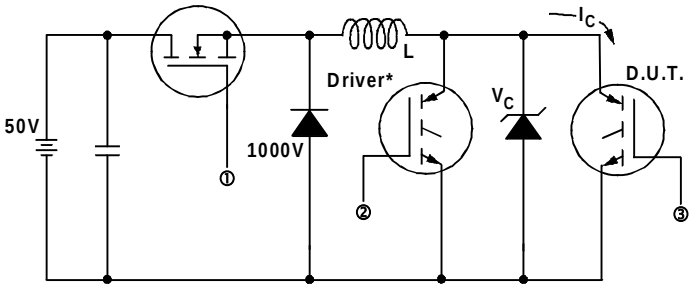


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

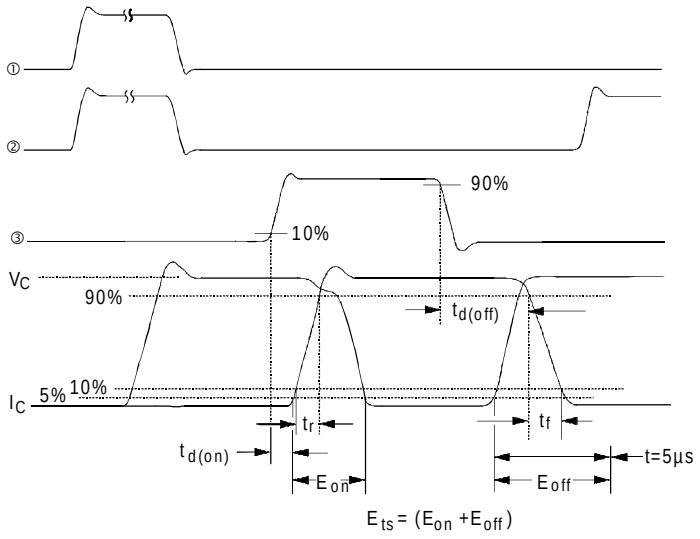
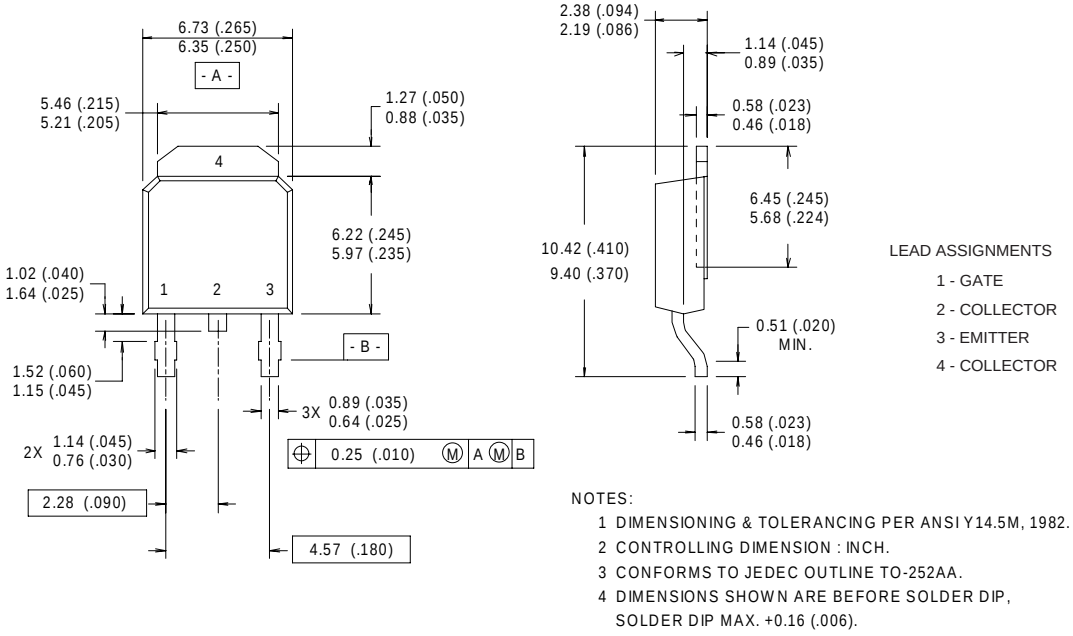


Fig. 14b - Switching Loss Waveforms

Package Outline

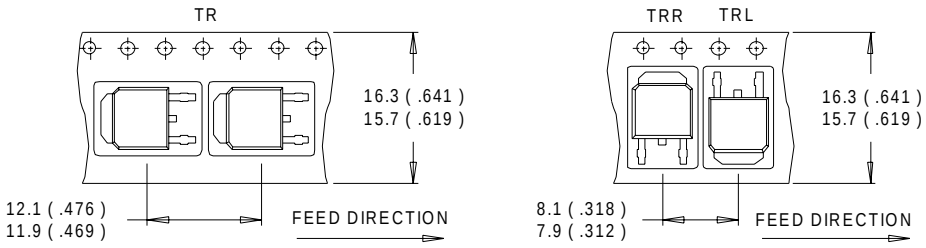
TO-252AA Outline
Dimensions are shown in millimeters (inches)



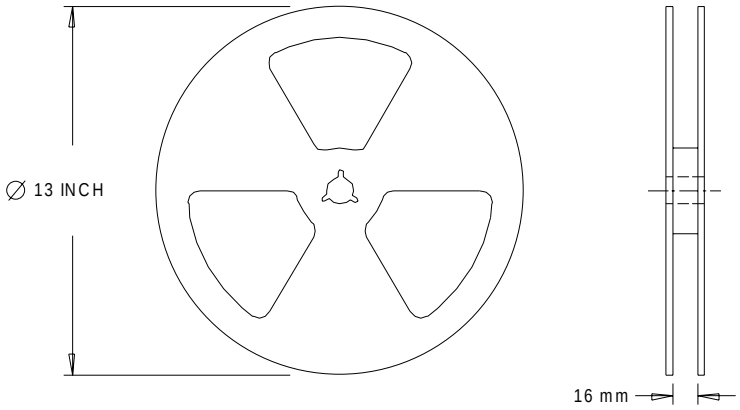
NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

Tape & Reel Information

TO-252AA



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936
http://www.irf.com/ Data and specifications subject to change without notice. 12/98

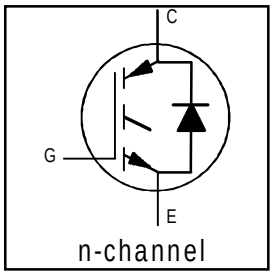
PD 91677B

International
IOR Rectifier

IRG4BC10UD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

UltraFast CoPack IGBT

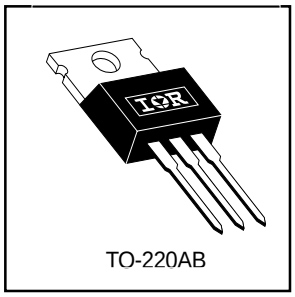


V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.15V

@V_{GE} = 15V, I_C = 5.0A

t_f (typ.) = 140ns



TO-220AB

Features

- UltraFast: Optimized for high operating up to 80 kHz in hard switching, >200 kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than previous Generation
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-220AB package

Benefits

- Generation 4 IGBT's offer highest efficiencies available
- IGBT's optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBT's . Minimized recovery characteristics require less/no snubbing

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	8.5	A
I_C @ T_C = 100°C	Continuous Collector Current	5.0	
I_{CM}	Pulsed Collector Current ①	34	
I_{LM}	Clamped Inductive Load Current ②	34	
I_F @ T_C = 100°C	Diode Continuous Forward Current	4.0	
I_{FM}	Diode Maximum Forward Current	16	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	38	W
P_D @ T_C = 100°C	Maximum Power Dissipation	15	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	3.3	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	7.0	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	80	
Wt	Weight	—	2 (0.07)	—	g (oz)

12/30/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.54	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.15	2.6	V	I_C = 5.0A V_{GE} = 15V
		—	2.61	—		I_C = 8.5A See Fig. 2, 5
		—	2.30	—		I_C = 5.0A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-8.7	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	2.8	4.2	—	S	V_{CE} = 100V, I_C = 5.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.5	1.8	V	I_C = 4.0A See Fig. 13
		—	1.4	1.7		I_C = 4.0A, T_J = 125°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	15	22	nC	I_C = 5.0A
Qge	Gate - Emitter Charge (turn-on)	—	2.6	4.0		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	5.8	8.7		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	40	—	ns	T_J = 25°C
t_r	Rise Time	—	16	—		I_C = 5.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	87	130		V_{GE} = 15V, R_G = 100Ω
t_f	Fall Time	—	140	210		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	0.14	—	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	0.12	—		See Fig. 9, 10, 18
E_{ts}	Total Switching Loss	—	0.26	0.33		
$t_{d(on)}$	Turn-On Delay Time	—	38	—	ns	T_J = 150°C, See Fig. 11, 18
t_r	Rise Time	—	18	—		I_C = 5.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	95	—		V_{GE} = 15V, R_G = 100Ω
t_f	Fall Time	—	250	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	0.45	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	270	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	21	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	3.5	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	28	42	ns	T_J = 25°C See Fig.
		—	38	57		T_J = 125°C 14 I_F = 4.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	2.9	5.2	A	T_J = 25°C See Fig.
		—	3.7	6.7		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	40	60	nC	T_J = 25°C See Fig.
		—	70	105		T_J = 125°C 16 di/dt = 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	280	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	235	—		T_J = 125°C 17

Details of note ① through ④ are on the last page

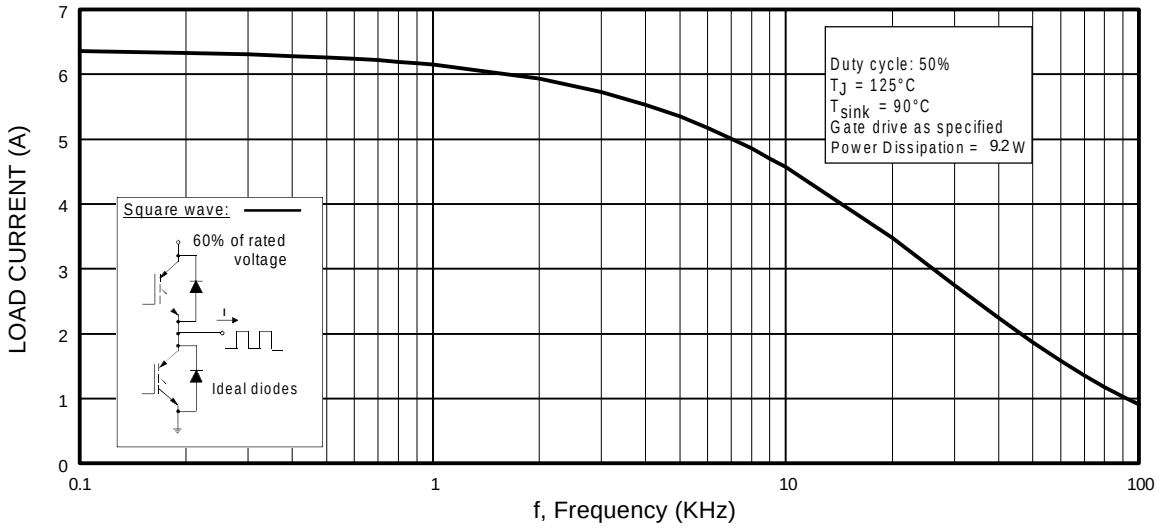


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

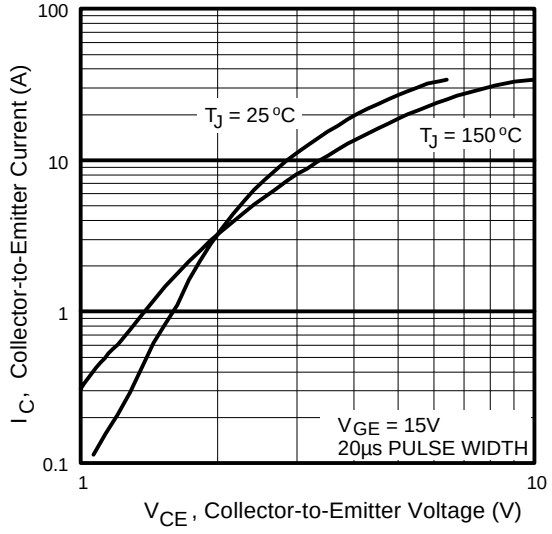


Fig. 2 - Typical Output Characteristics

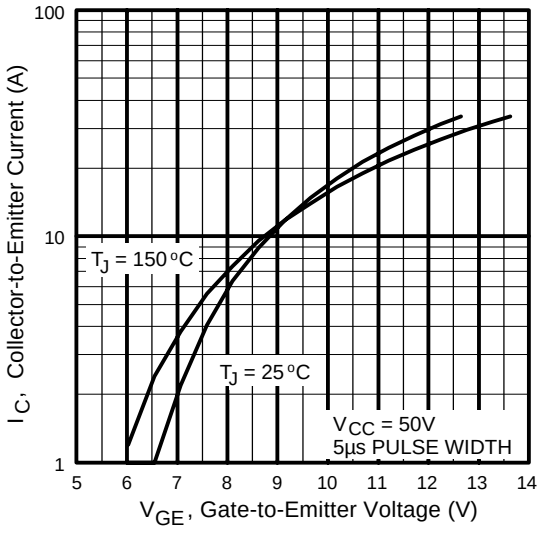


Fig. 3 - Typical Transfer Characteristics

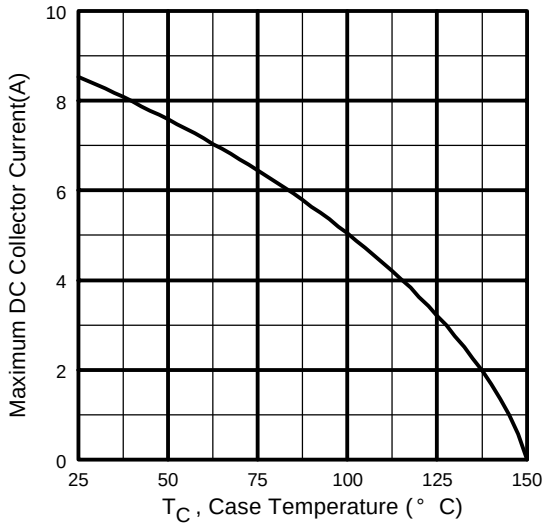


Fig. 4 - Maximum Collector Current vs. Case Temperature

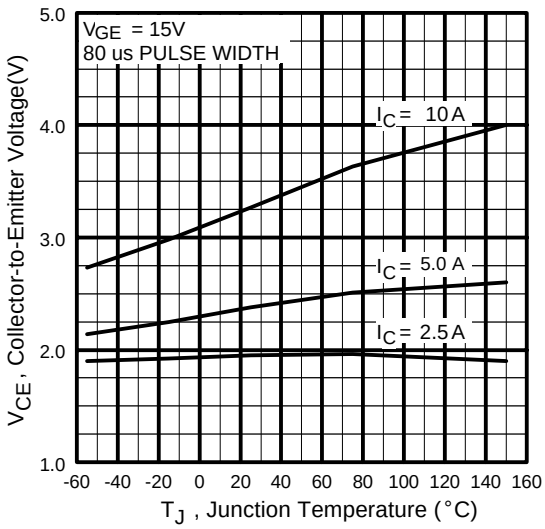


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

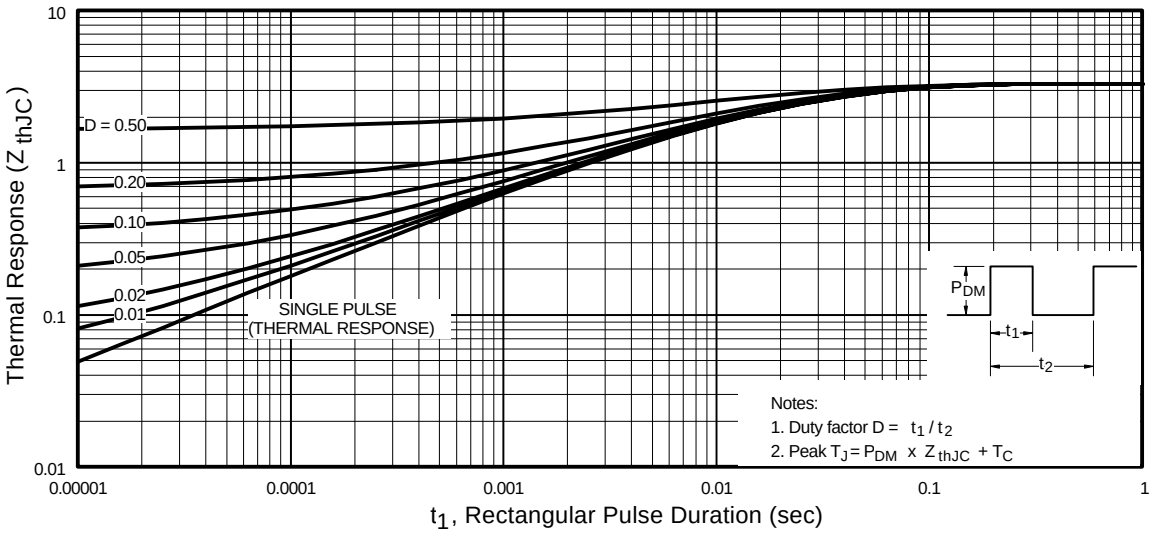


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

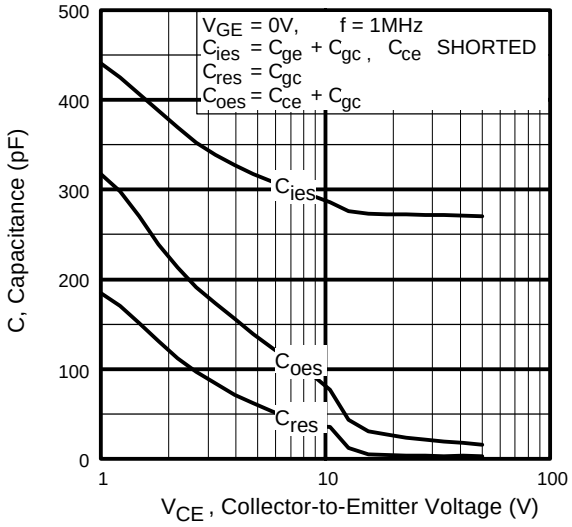


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

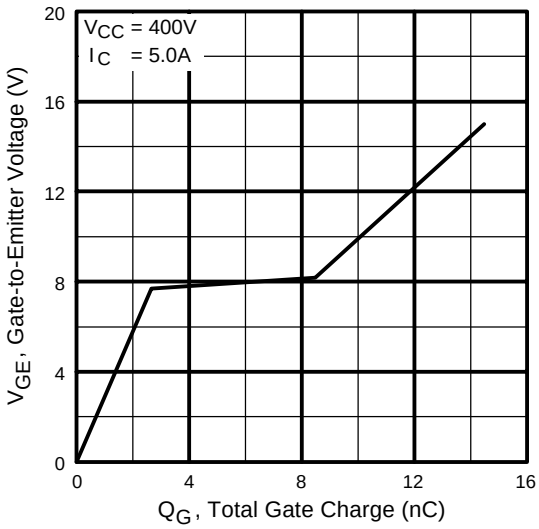


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

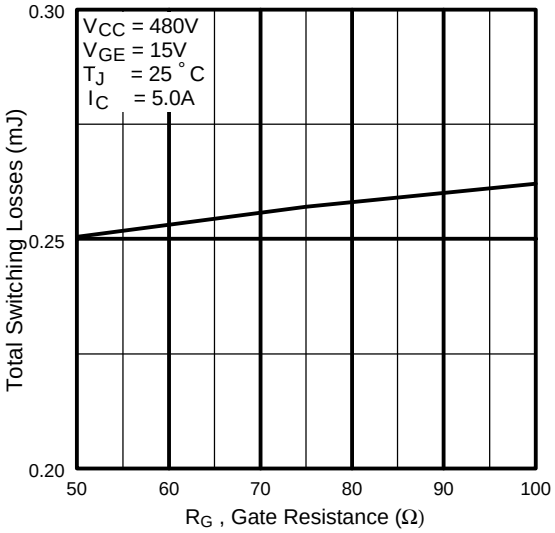


Fig. 9 - Typical Switching Losses vs. Gate Resistance

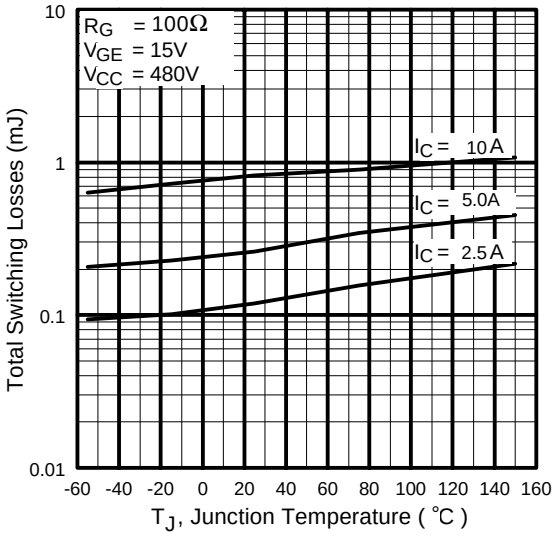


Fig. 10 - Typical Switching Losses vs. Junction Temperature

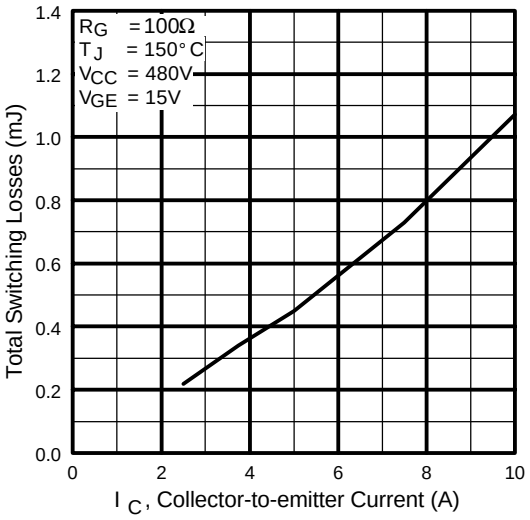


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

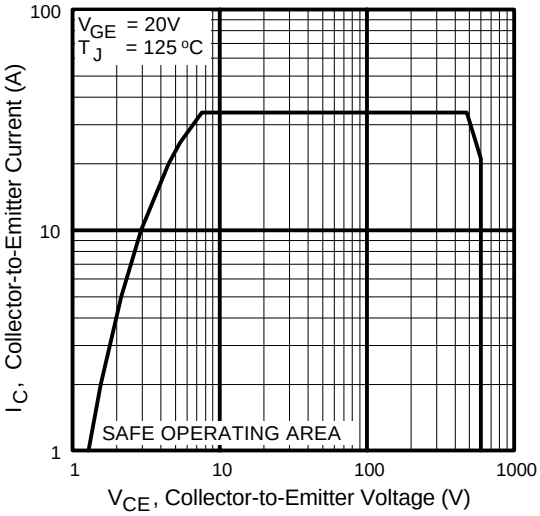


Fig. 12 - Turn-Off SOA

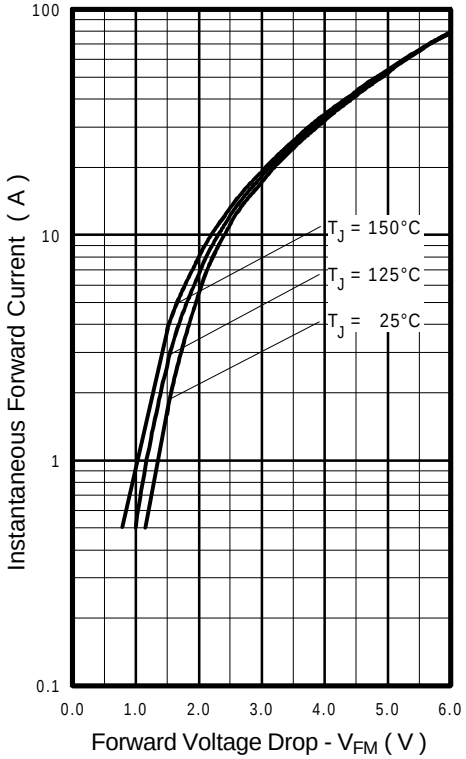


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

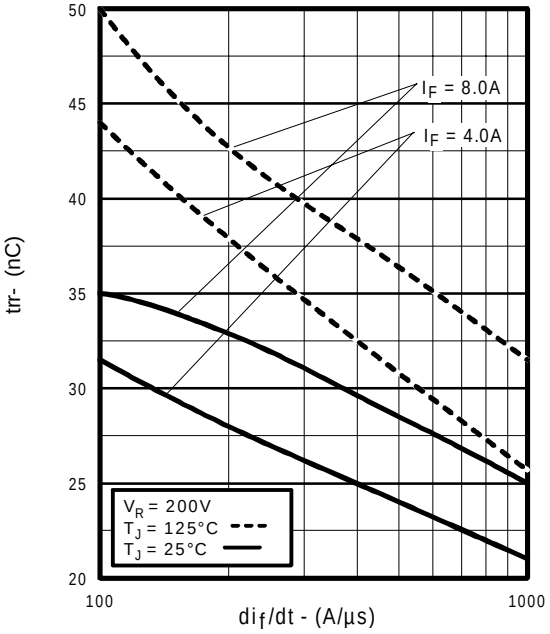


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

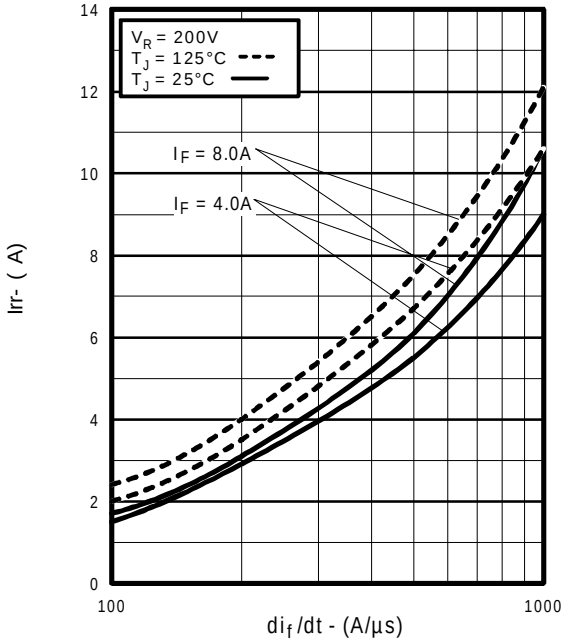


Fig. 15 - Typical Recovery Current vs. di_f/dt

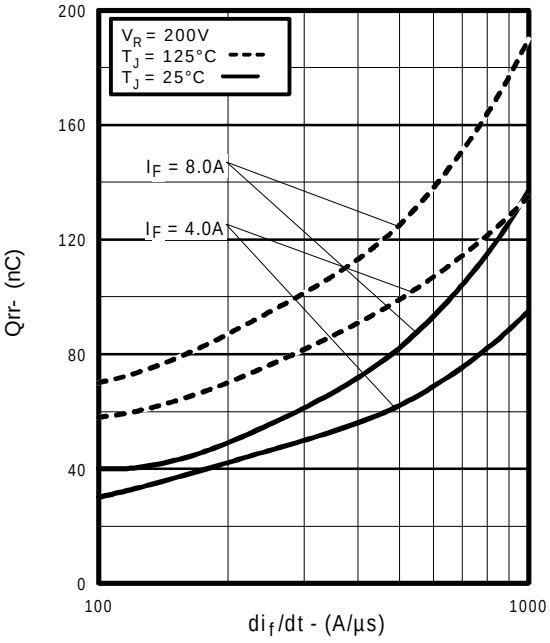


Fig. 16 - Typical Stored Charge vs. di_f/dt

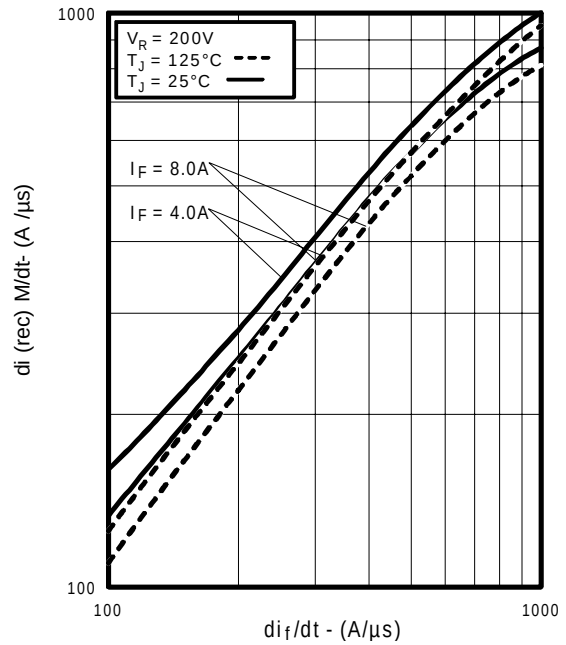


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt,

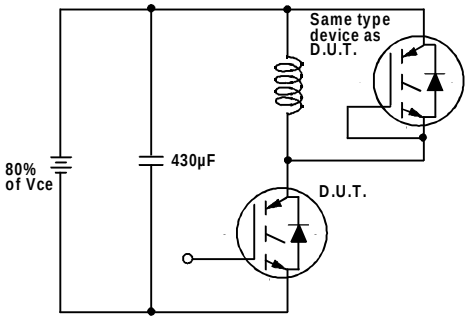


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

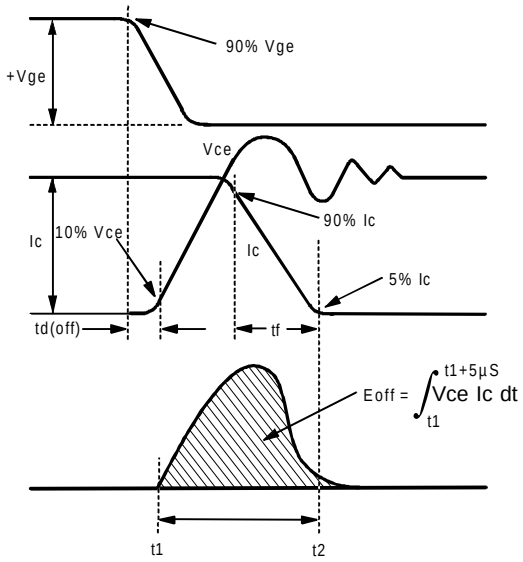


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

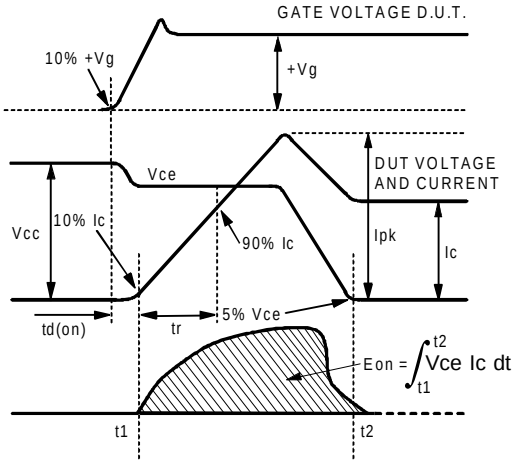


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

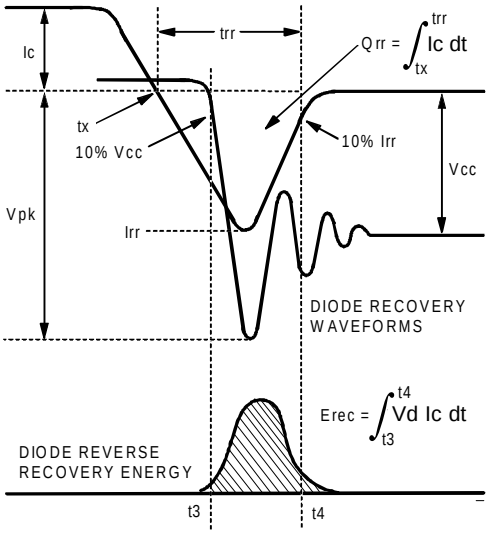


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

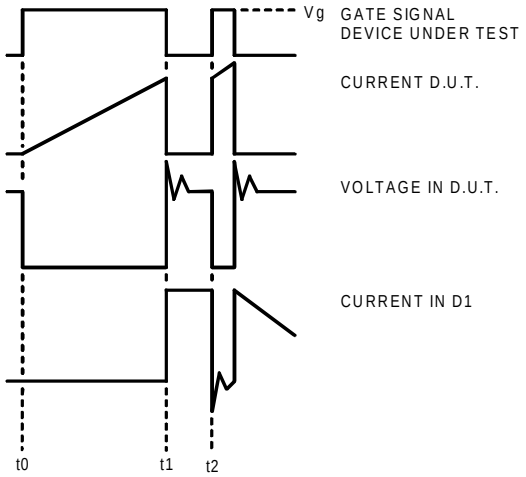


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

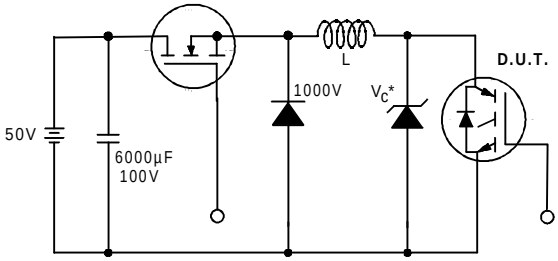


Figure 19. Clamped Inductive Load Test Circuit

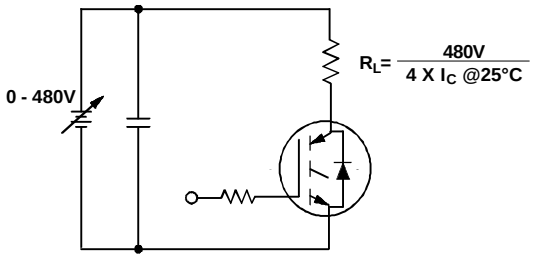


Figure 20. Pulsed Collector Current Test Circuit

Notes:

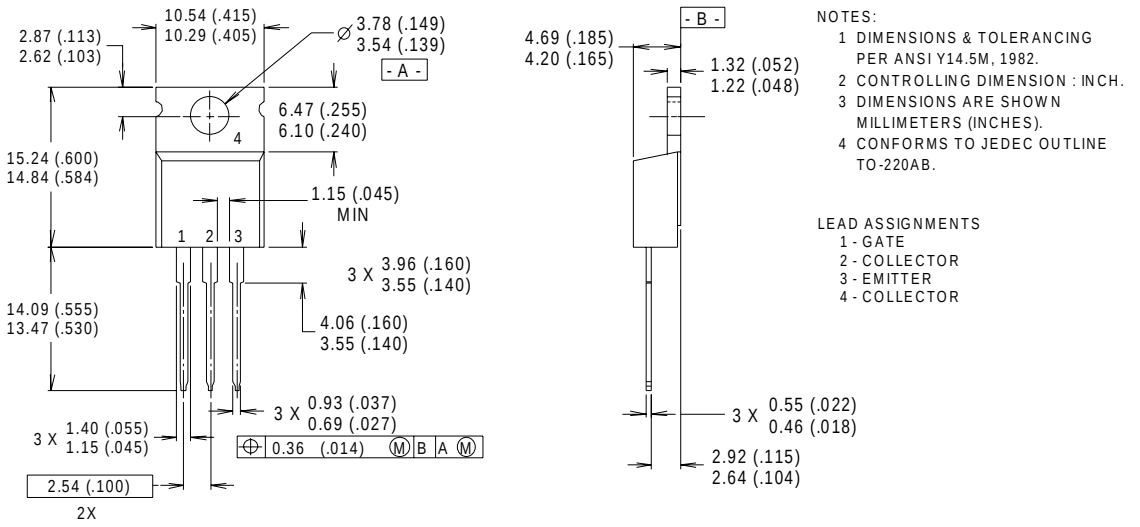
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 100Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline and Dimensions — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB

Dimensions in Millimeters and (Inches)

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.

Data and specifications subject to change without notice. 12/00

International
IOR Rectifier

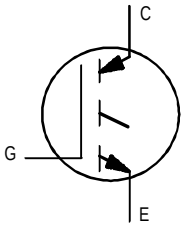
IRG4RC10K

INSULATED GATE BIPOLAR TRANSISTOR

Short Circuit Rated
UltraFast IGBT

Features

- Short Circuit Rated UltraFast: Optimized for high operating frequencies >5.0 kHz , and Short Circuit Rated to 10µs @ 125°C, V_{GE} = 15V
- Generation 4 IGBT design provides higher efficiency than Generation 3
- Industry standard TO-252AA package



n-channel

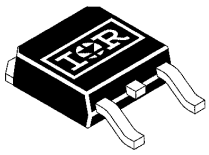
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.39V

@V_{GE} = 15V, I_C = 5.0A

Benefits

- Generation 4 IGBT's offer highest efficiency available
- IGBT's optimized for specified application conditions



D-PAK
TO-252AA

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	9.0	A
I_C @ T_C = 100°C	Continuous Collector Current	5.0	
I_{CM}	Pulsed Collector Current ①	18	
I_{LM}	Clamped Inductive Load Current ②	18	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	34	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	38	W
P_D @ T_C = 100°C	Maximum Power Dissipation	15	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	3.3	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	——	50	
Wt	Weight	0.3 (0.01)	——	g (oz)

* When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.58	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.39	2.62	V	I_C = 5.0A V_{GE} = 15V
		—	3.25	—		I_C = 9.0A See Fig.2, 5
		—	2.63	—		I_C = 5.0A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.5		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	1.2	1.8	—	S	V_{CE} = 50 V, I_C = 5.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	19	29	nC	I_C = 5.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	2.9	4.3		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	9.8	15		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	T_J = 25°C
t_r	Rise Time	—	24	—		I_C = 5.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	51	77		V_{GE} = 15V, R_G = 100Ω
t_f	Fall Time	—	190	290		Energy losses include "tail"
E_{on}	Turn-On Switching Loss	—	0.16	—	mJ	See Fig. 9,10,14
E_{off}	Turn-Off Switching Loss	—	0.10	—		
E_{ts}	Total Switching Loss	—	0.26	0.32		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 400V, T_J = 125°C
						V_{GE} = 15V, R_G = 100Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	T_J = 150°C,
t_r	Rise Time	—	27	—		I_C = 5.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	67	—		V_{GE} = 15V, R_G = 100Ω
t_f	Fall Time	—	350	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.47	—	mJ	See Fig. 10,11,14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	220	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	29	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	7.5	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 100Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

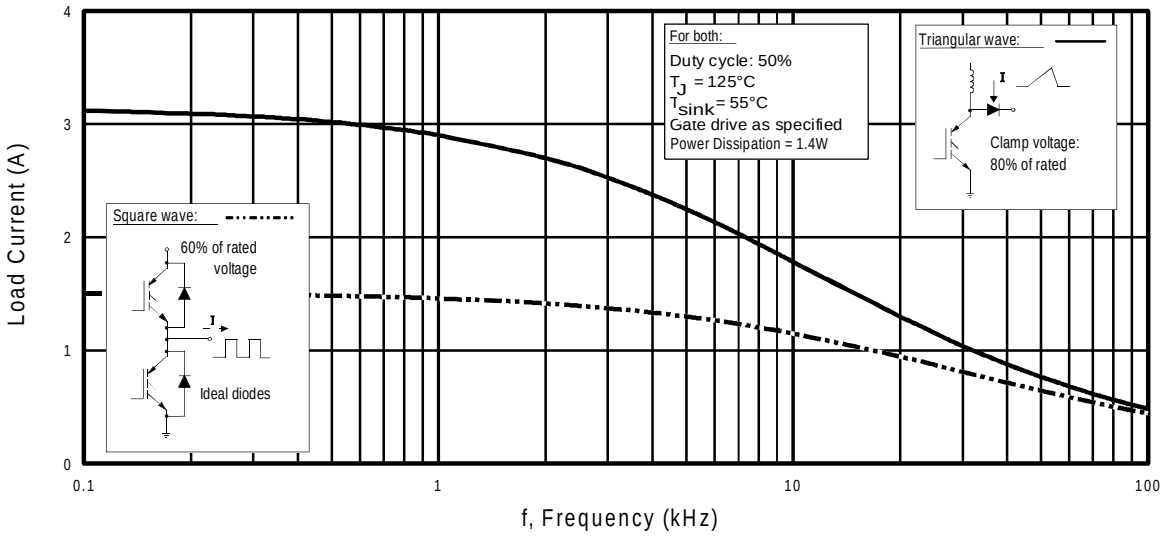


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

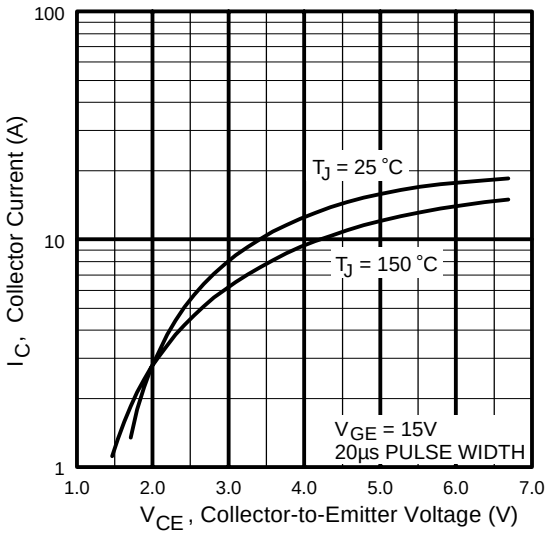


Fig. 2 - Typical Output Characteristics

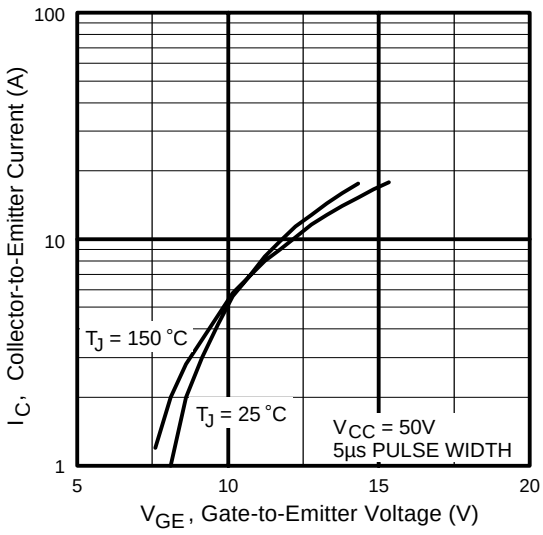


Fig. 3 - Typical Transfer Characteristics

5µs PULSE WIDTH

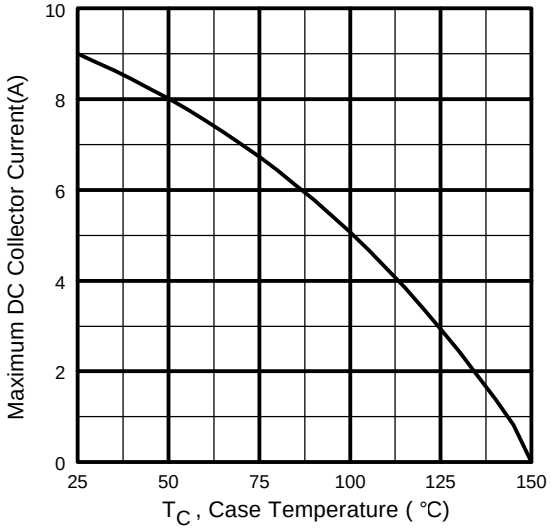


Fig. 4 - Maximum Collector Current vs. Case Temperature

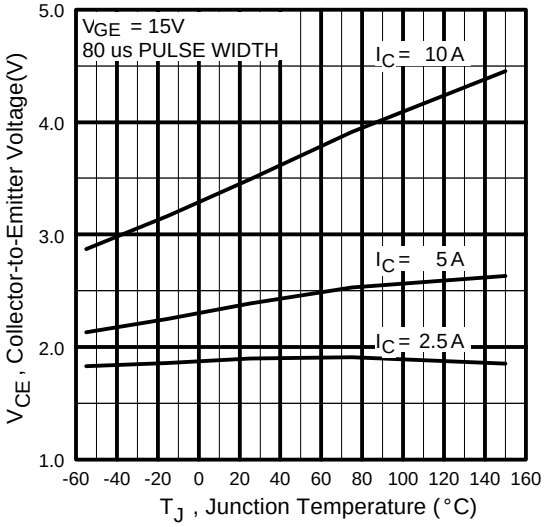


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

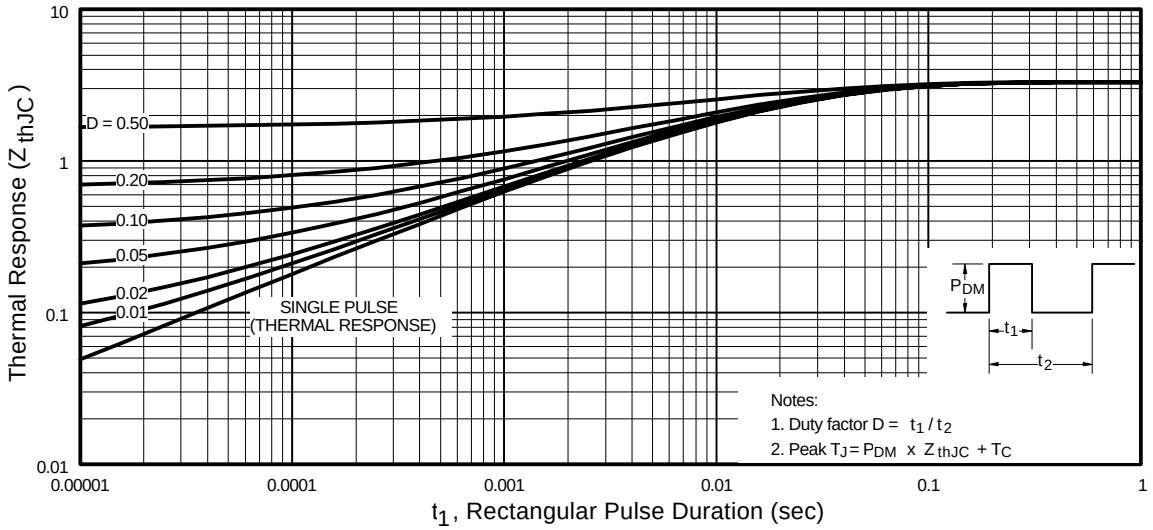


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

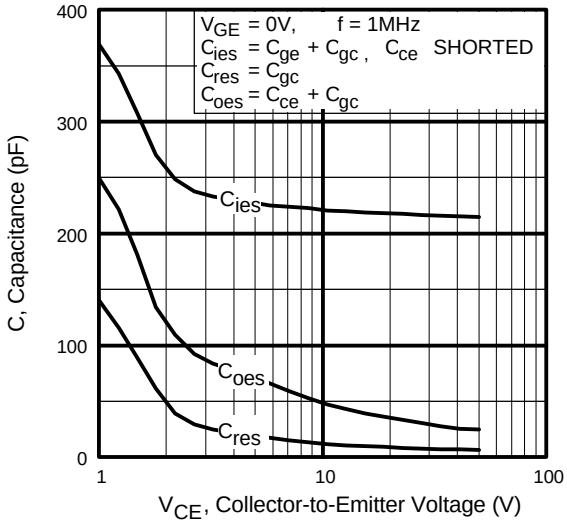


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

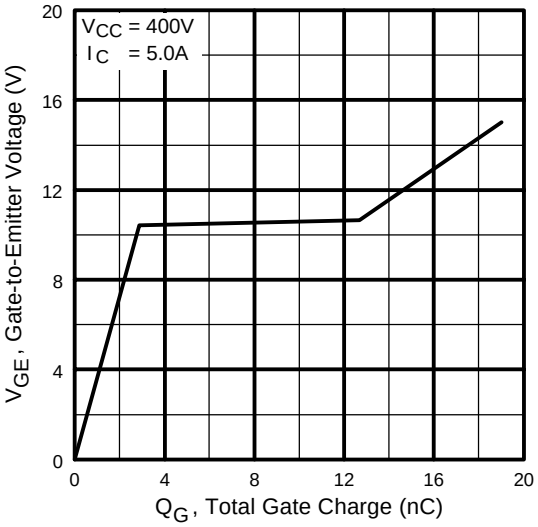


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

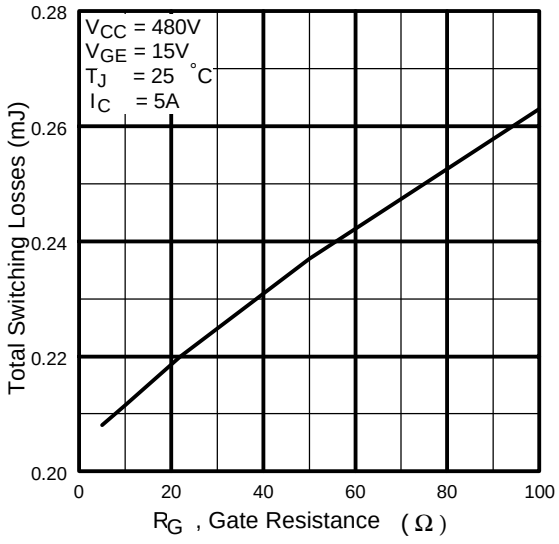


Fig. 9 - Typical Switching Losses vs. Gate Resistance

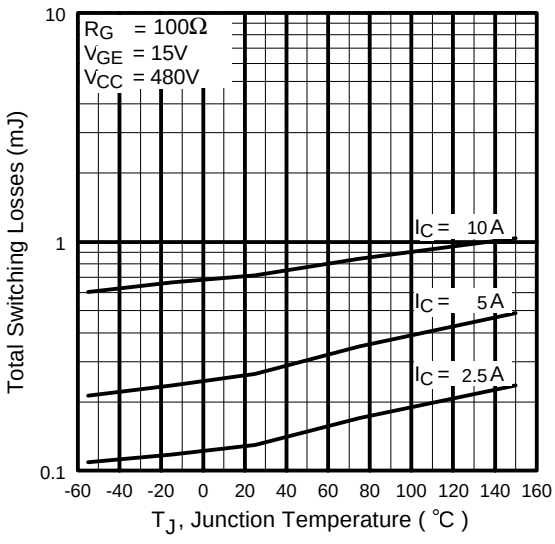


Fig. 10 - Typical Switching Losses vs. Junction Temperature

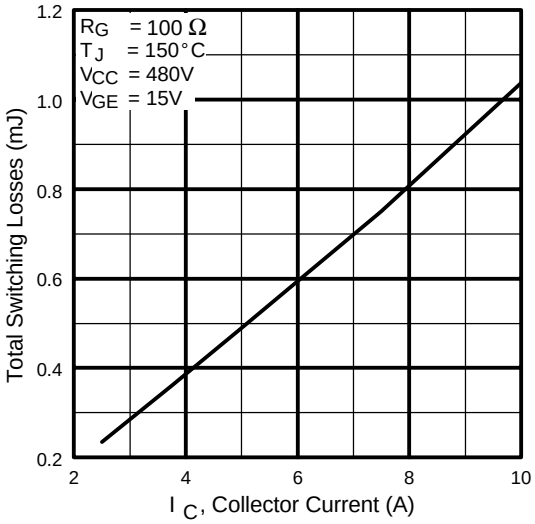


Fig. 11 - Typical Switching Losses vs. Collector Current

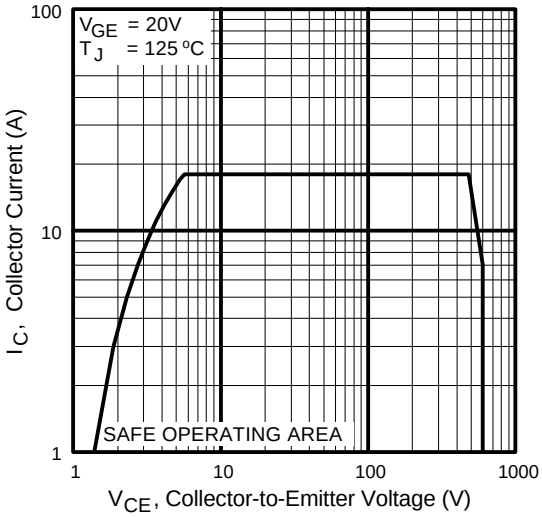


Fig. 12 - Turn-Off SOA

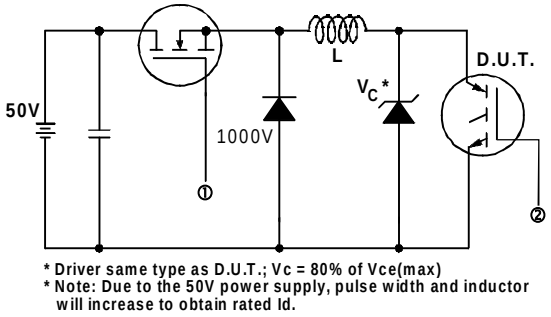


Fig. 13a - Clamped Inductive Load Test Circuit

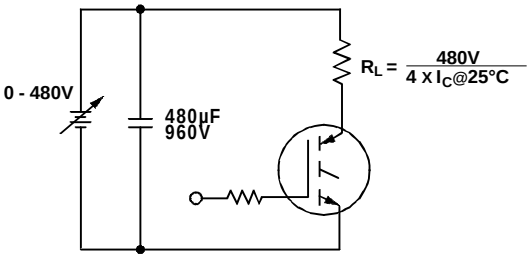


Fig. 13b - Pulsed Collector Current Test Circuit

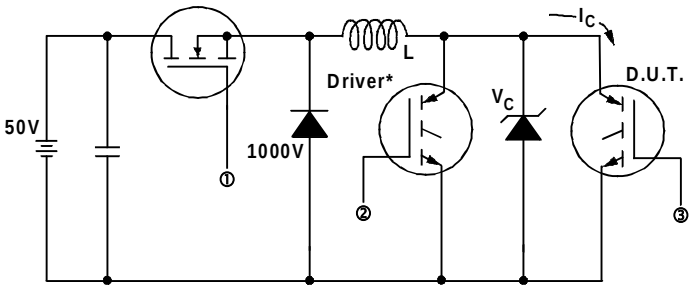


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

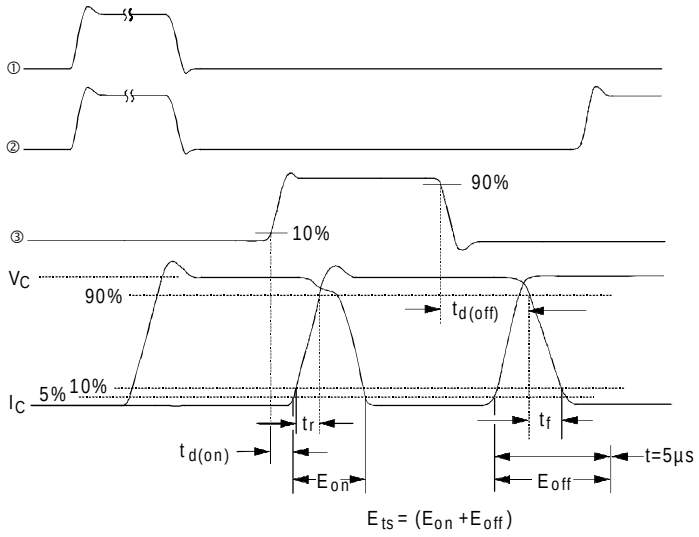
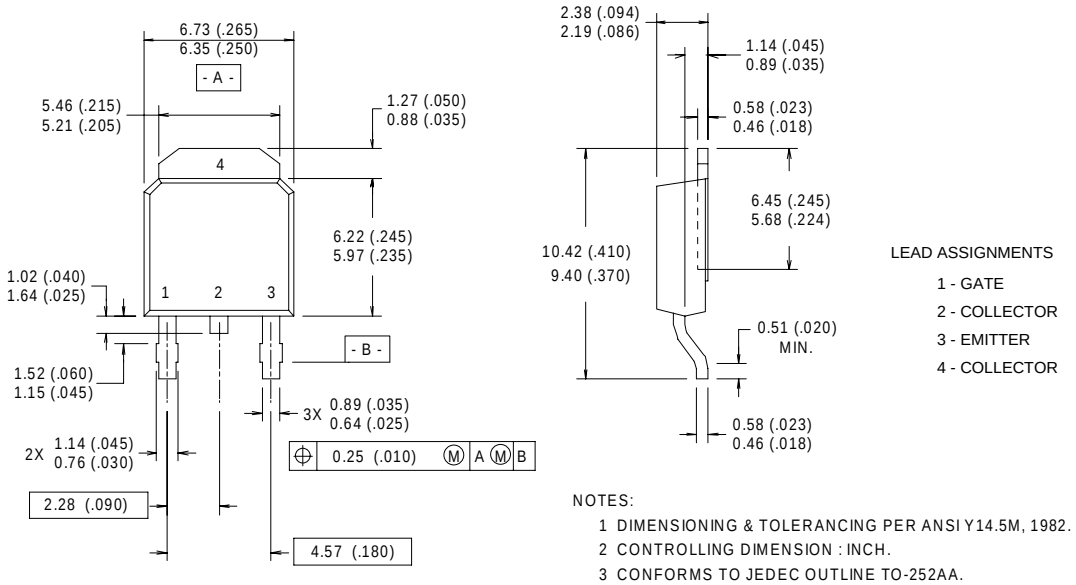


Fig. 14b - Switching Loss Waveforms

Package Outline

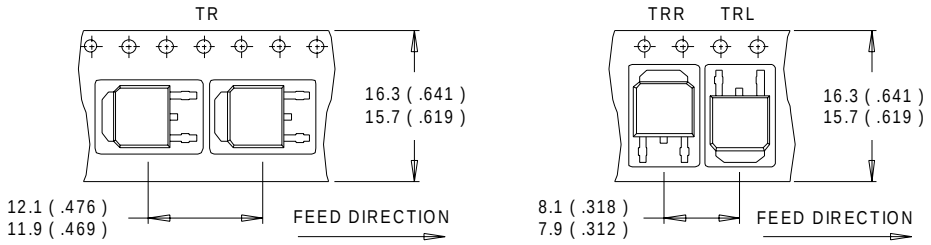
TO-252AA Outline
Dimensions are shown in millimeters (inches)



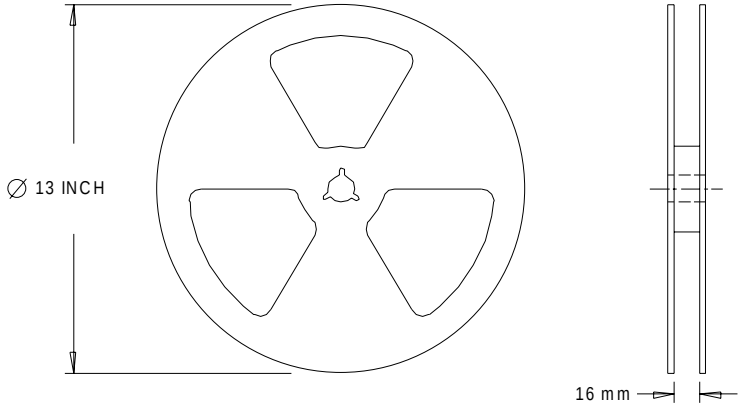
NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

Tape & Reel Information

TO-252AA



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.

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PD - 91733A

International
IOR Rectifier

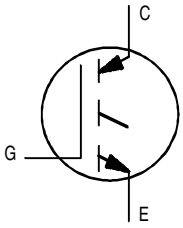
IRG4BC10K

Short Circuit Rated
UltraFast IGBT

INSULATED GATE BIPOLAR TRANSISTOR

Features

- Short Circuit Rated UltraFast: Optimized for high operating frequencies >5.0 kHz , and Short Circuit Rated to 10µs @ 125°C, V_{GE} = 15V
- Generation 4 IGBT design provides higher efficiency than Generation 3
- Industry standard TO-220AB package



n-channel

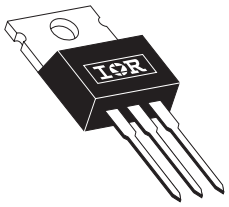
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.39V

@V_{GE} = 15V, I_C = 5.0A

Benefits

- Generation 4 IGBTs offer highest efficiency available
- IGBTs optimized for specified application conditions



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	9.0	A
I_C @ T_C = 100°C	Continuous Collector Current	5.0	
I_{CM}	Pulsed Collector Current ①	18	
I_{LM}	Clamped Inductive Load Current ②	18	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	34	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	38	W
P_D @ T_C = 100°C	Maximum Power Dissipation	15	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	3.3	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	80	
Wt	Weight	2.0 (0.07)	—	g (oz)

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.58	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.39	2.62	V	I_C = 5.0A V_{GE} = 15V
		—	3.25	—		I_C = 9.0A See Fig.2, 5
		—	2.63	—		I_C = 5.0A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.5		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	1.2	1.8	—	S	V_{CE} = 50 V, I_C = 5.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	19	29	nC	I_C = 5.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	2.9	4.3		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	9.8	15		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	T_J = 25°C
t_r	Rise Time	—	24	—		I_C = 5.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	51	77		V_{GE} = 15V, R_G = 100Ω
t_f	Fall Time	—	190	290		Energy losses include "tail"
E_{on}	Turn-On Switching Loss	—	0.16	—	mJ	See Fig. 9,10,14
E_{off}	Turn-Off Switching Loss	—	0.10	—		
E_{ts}	Total Switching Loss	—	0.26	0.32		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 400V, T_J = 125°C
						V_{GE} = 15V, R_G = 100Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	T_J = 150°C,
t_r	Rise Time	—	27	—		I_C = 5.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	67	—		V_{GE} = 15V, R_G = 100Ω
t_f	Fall Time	—	350	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.47	—	mJ	See Fig. 10,11,14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	220	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	29	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	7.5	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 100Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

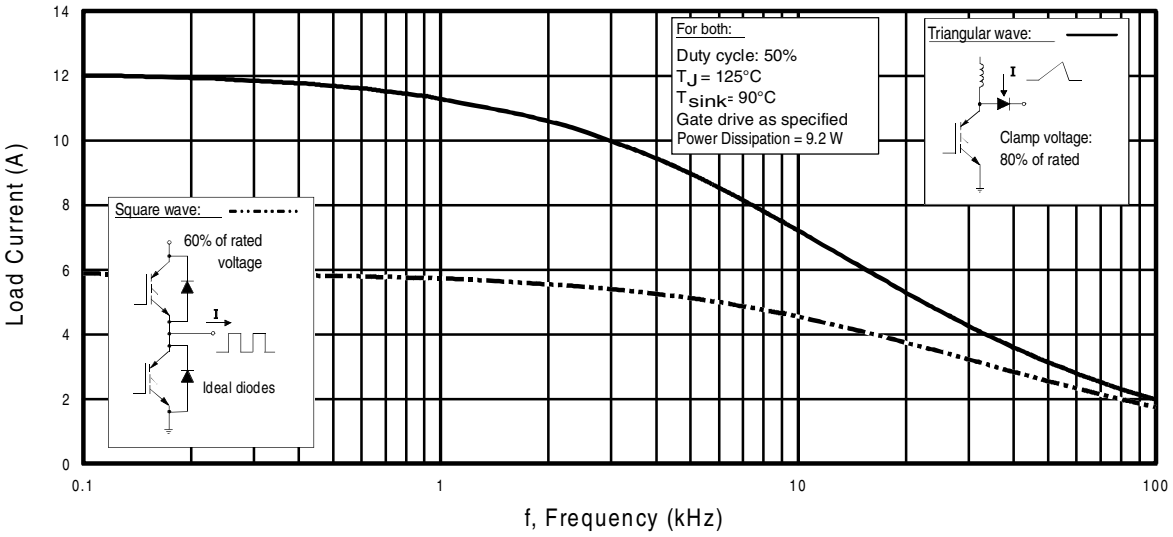


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

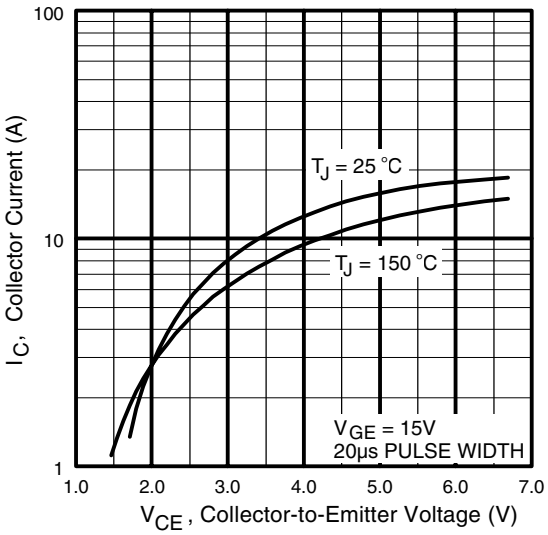


Fig. 2 - Typical Output Characteristics

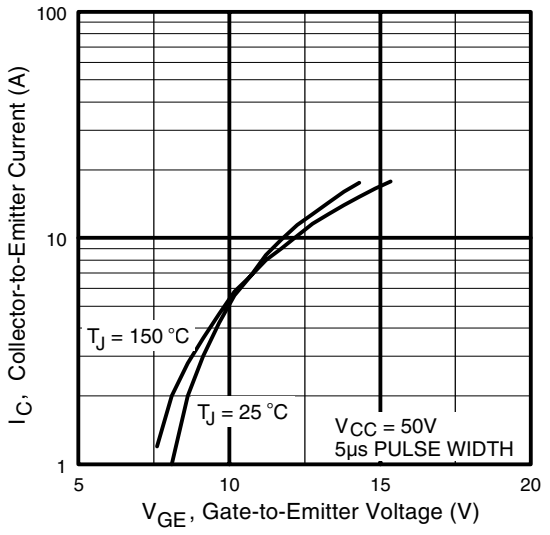


Fig. 3 - Typical Transfer Characteristics

5µs PULSE WIDTH

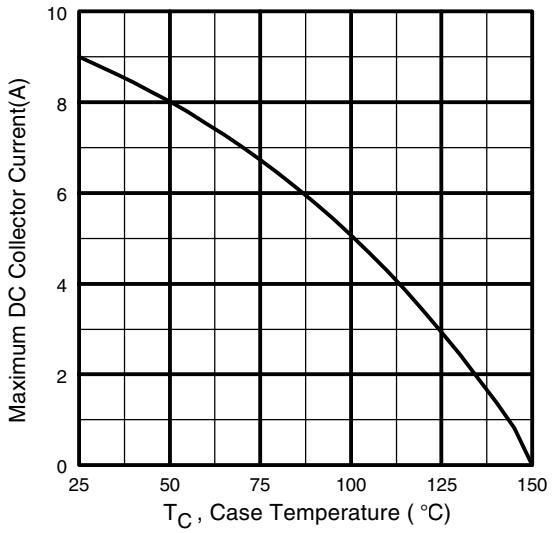


Fig. 4 - Maximum Collector Current vs. Case Temperature

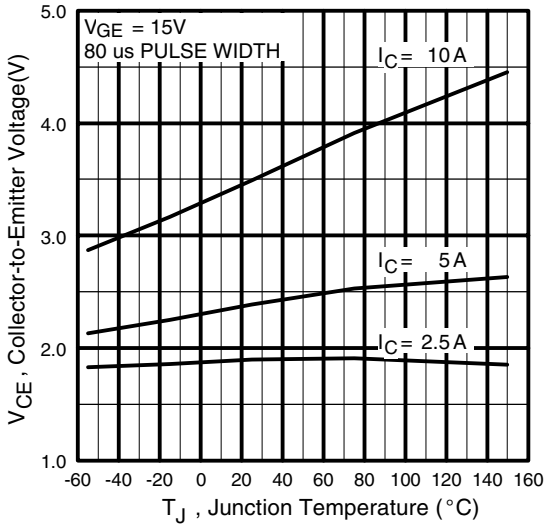


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

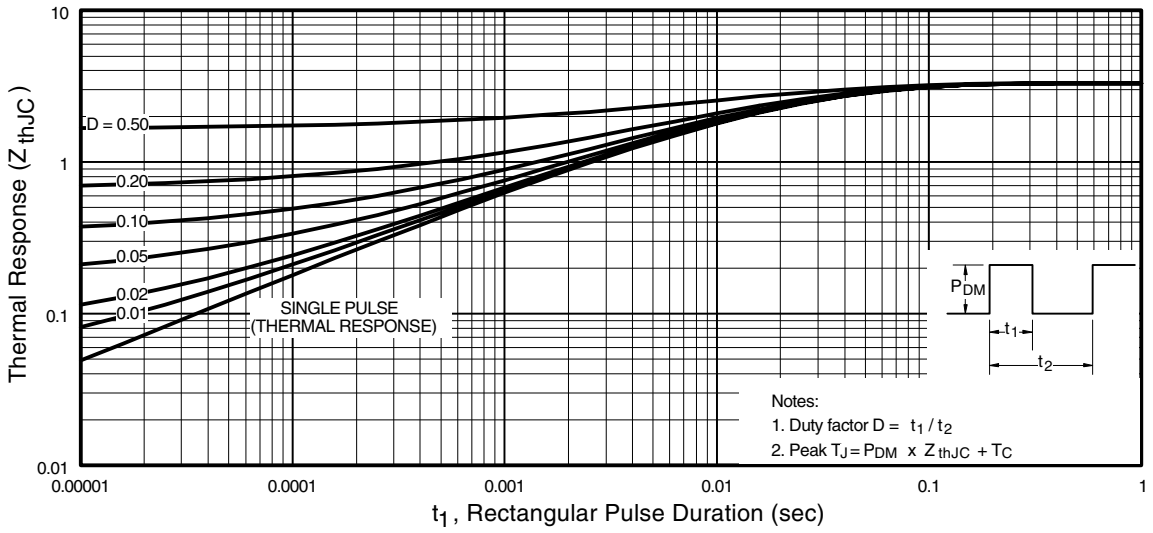


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

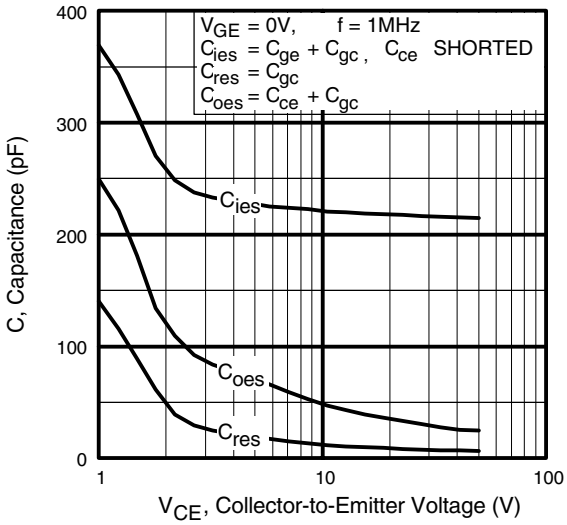


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

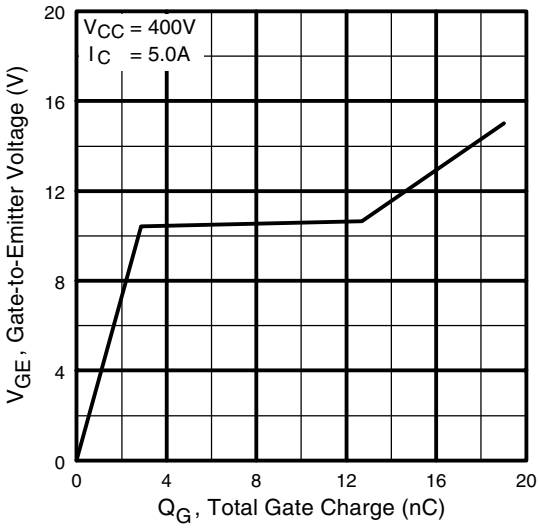


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

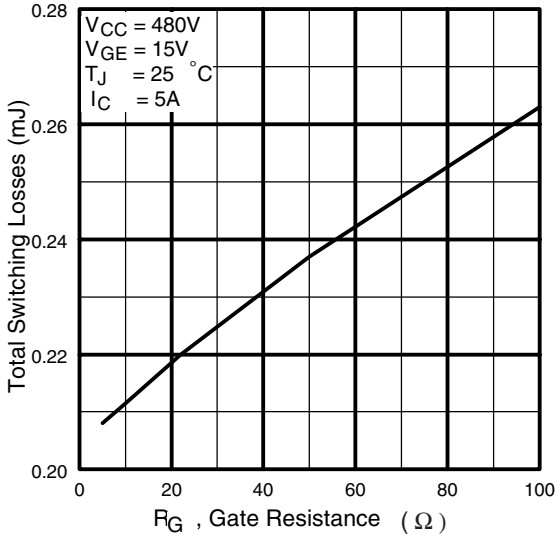


Fig. 9 - Typical Switching Losses vs. Gate Resistance

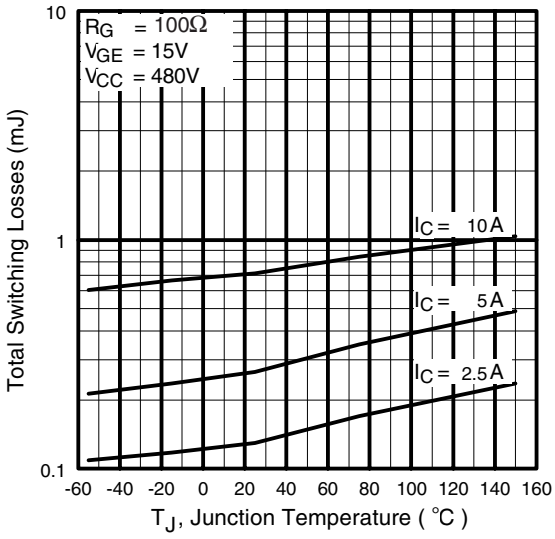


Fig. 10 - Typical Switching Losses vs. Junction Temperature

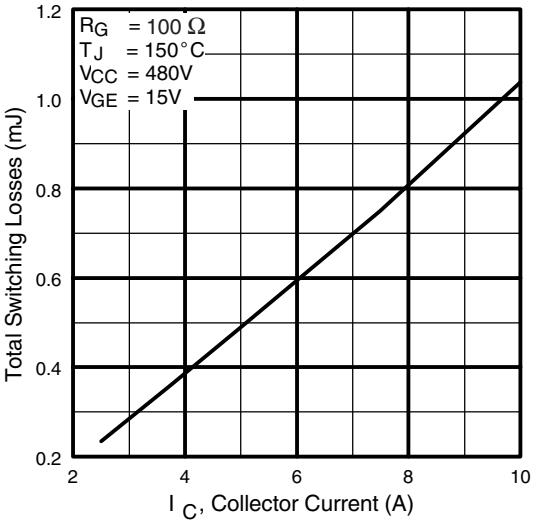


Fig. 11 - Typical Switching Losses vs. Collector Current

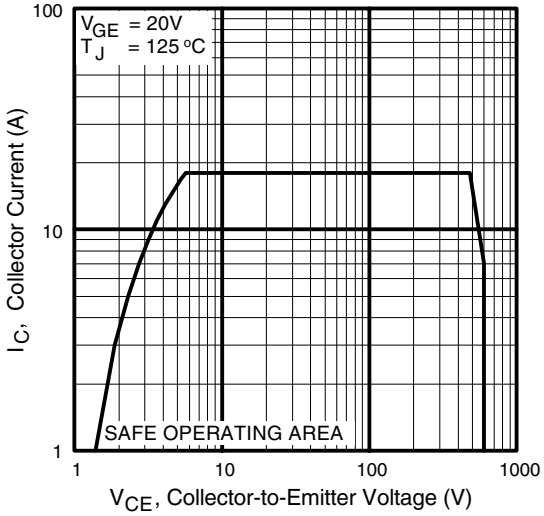


Fig. 12 - Turn-Off SOA

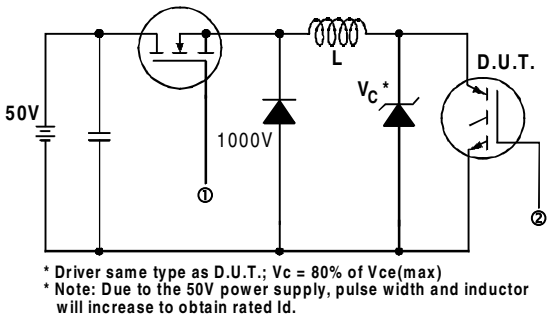


Fig. 13a - Clamped Inductive Load Test Circuit

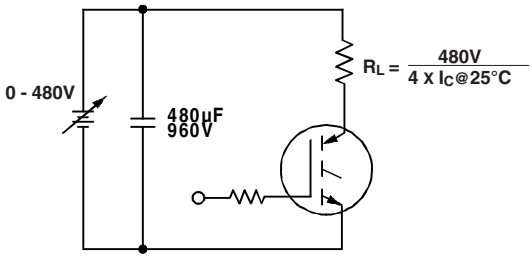


Fig. 13b - Pulsed Collector Current Test Circuit

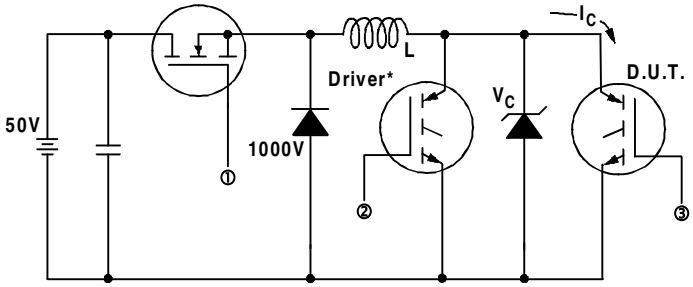


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

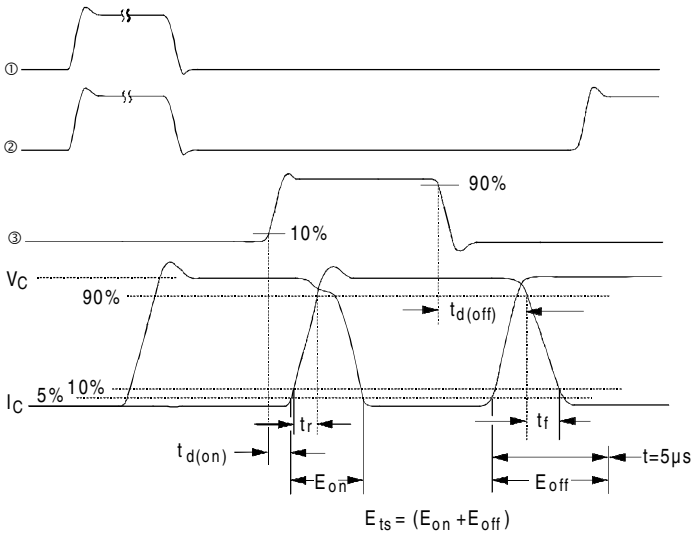
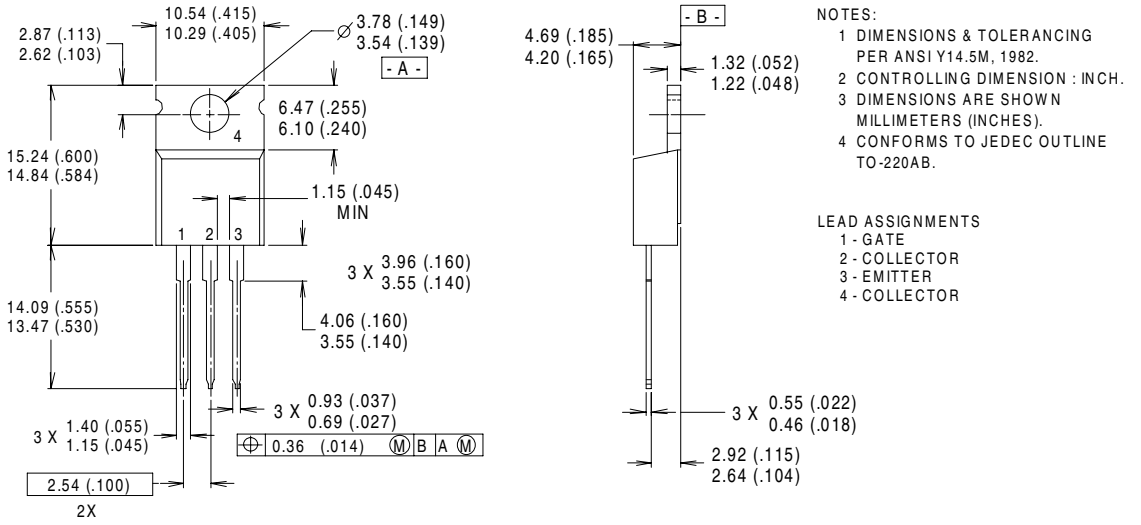


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

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PD -91734B

International
IOR Rectifier

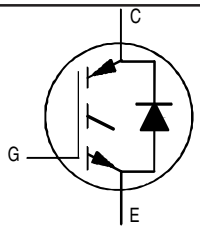
IRG4BC10KD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
UltraFast IGBT

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, @360V V_{CE} (start), T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Tighter parameter distribution and higher efficiency than previous generations
- IGBT co-packaged with HEXFRED™ ultrafast, ultrasoft recovery antiparallel diodes

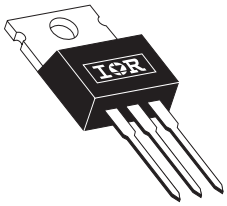


n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.39V

@V_{GE} = 15V, I_C = 5.0A


TO-220AB

Benefits

- Latest generation 4 IGBTs offer highest power density motor controls possible
- HEXFRED™ diodes optimized for performance with IGBTs. Minimized recovery characteristics reduce noise, EMI and switching losses

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	9.0	A
I_C @ T_C = 100°C	Continuous Collector Current	5.0	
I_{CM}	Pulsed Collector Current ①	18	
I_{LM}	Clamped Inductive Load Current ②	18	
I_F @ T_C = 100°C	Diode Continuous Forward Current	4.0	
I_{FM}	Diode Maximum Forward Current	16	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	38	W
P_D @ T_C = 100°C	Maximum Power Dissipation	15	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	——	——	3.3	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	——	——	7.0	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	——	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	——	80	
Wt	Weight	——	2 (0.07)	——	g (oz)

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage*f*	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.58	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.39	2.62	V	I_C = 5.0A V_{GE} = 15V
		—	3.25	—		I_C = 9.0A See Fig. 2, 5
		—	2.63	—		I_C = 5.0A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.5		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance „	1.2	1.8	—	S	V_{CE} = 50V, I_C = 5.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.5	1.8	V	I_C = 4.0A See Fig. 13
		—	1.4	1.7		I_C = 4.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	19	29	nC	I_C = 5.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	2.9	4.3		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	9.8	15		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	49	—	ns	
t_r	Rise Time	—	28	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	97	150		I_C = 5.0A, V_{CC} = 480V
t_f	Fall Time	—	140	210		V_{GE} = 15V, R_G = 100Ω
E_{on}	Turn-On Switching Loss	—	0.25	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.14	—		and diode reverse recovery
E_{ts}	Total Switching Loss	—	0.39	0.48		See Fig. 9,10,14
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 360V, T_J = 125°C
						V_{GE} = 15V, R_G = 100Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	46	—	ns	T_J = 150°C, See Fig. 10,11,14
t_r	Rise Time	—	32	—		I_C = 5.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	100	—		V_{GE} = 15V, R_G = 100Ω
t_f	Fall Time	—	310	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.56	—	mJ	and diode reverse recovery
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	220	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	29	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	7.5	—		*f* = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	28	42	ns	T_J = 25°C See Fig.
		—	38	57		T_J = 125°C 14 I_F = 4.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	2.9	5.2	A	T_J = 25°C See Fig.
		—	3.7	6.7		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	40	60	nC	T_J = 25°C See Fig.
		—	70	105		T_J = 125°C 16 di/dt = 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	280	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	235	—		T_J = 125°C 17

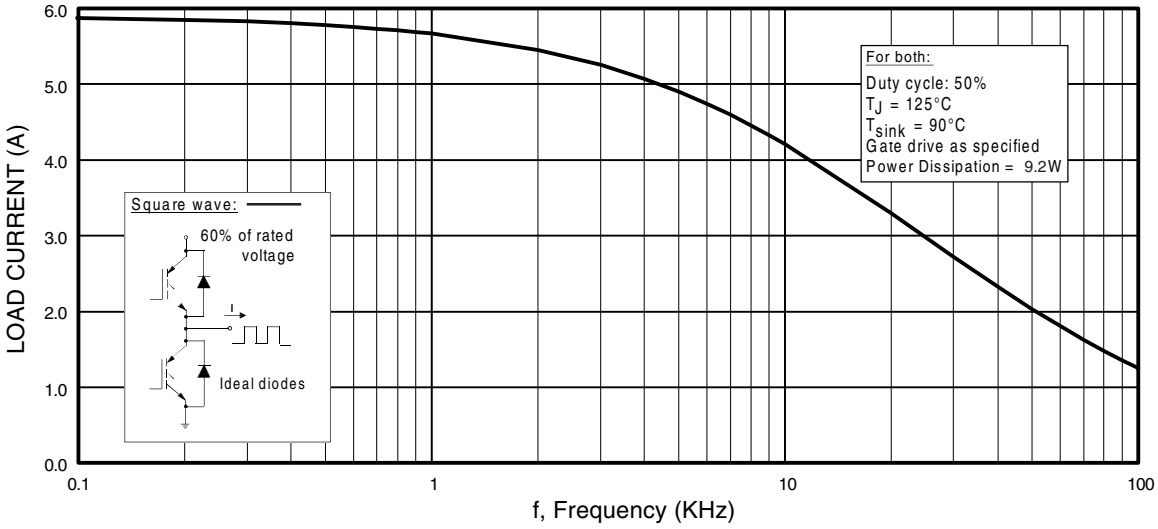


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

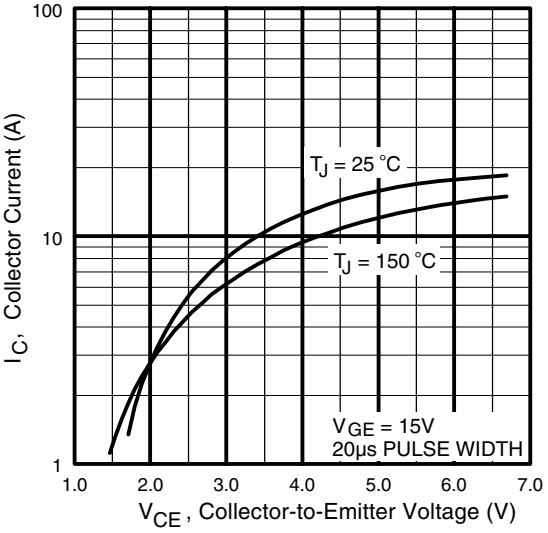


Fig. 2 - Typical Output Characteristics

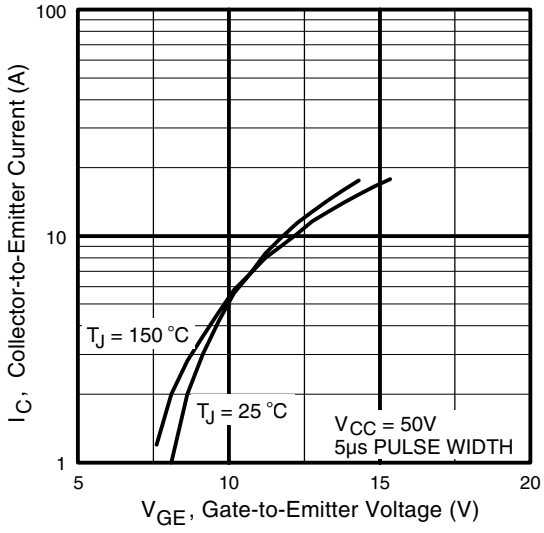


Fig. 3 - Typical Transfer Characteristics

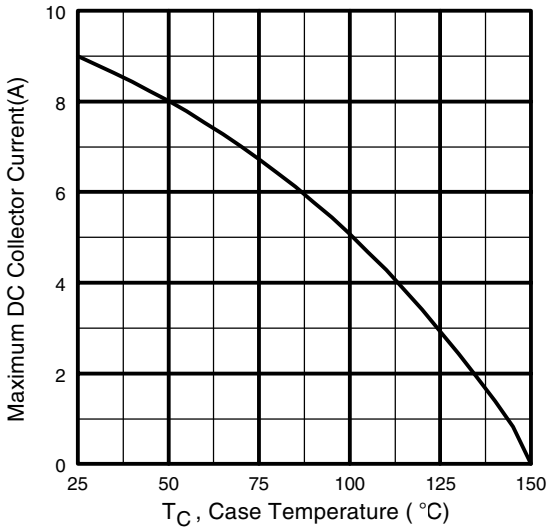


Fig. 4 - Maximum Collector Current vs. Case Temperature

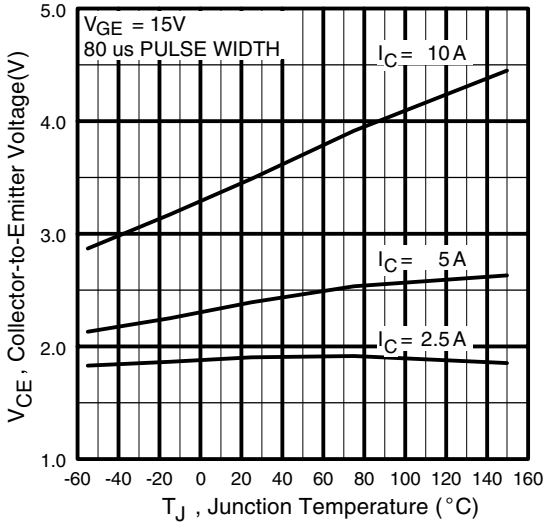


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

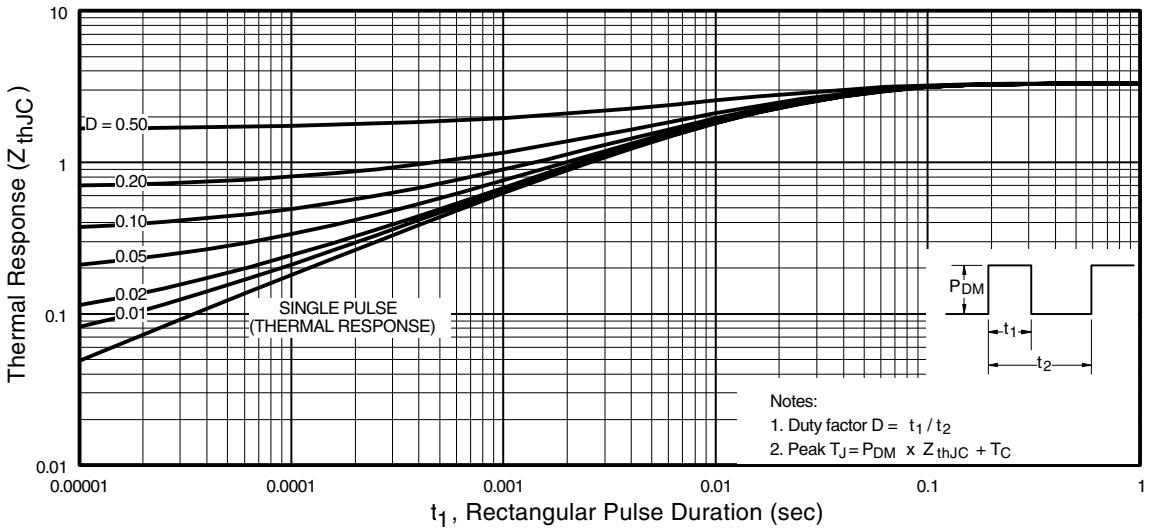


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

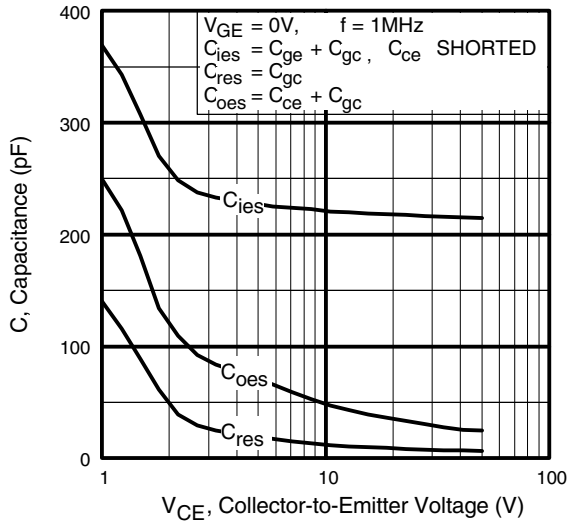


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

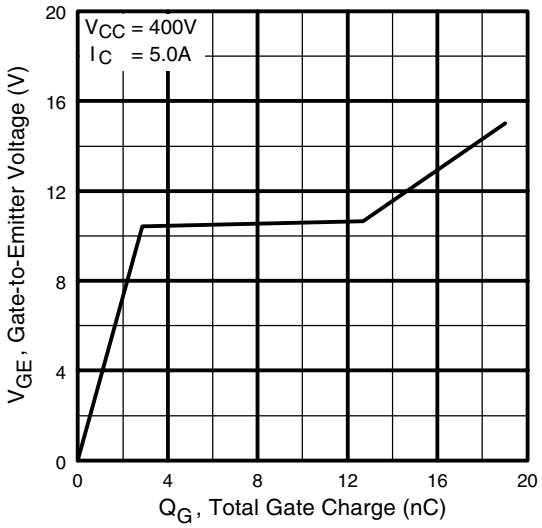


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

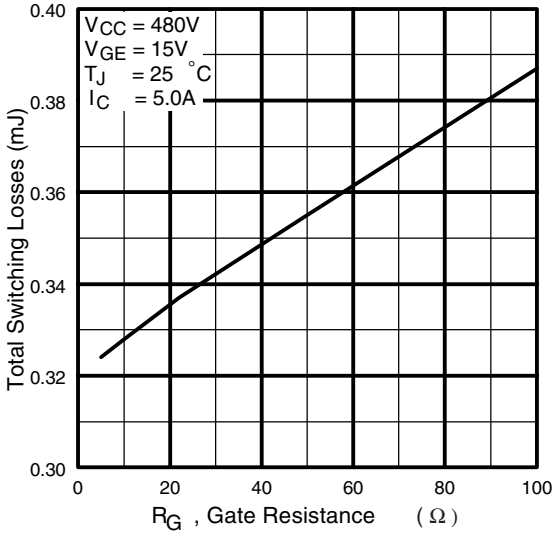


Fig. 9 - Typical Switching Losses vs. Gate Resistance

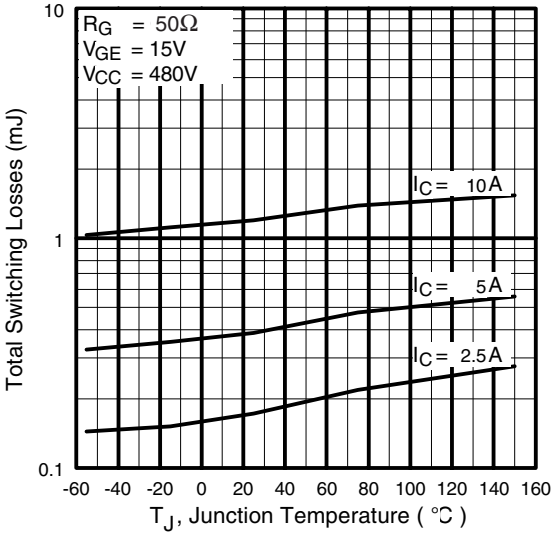


Fig. 10 - Typical Switching Losses vs. Junction Temperature

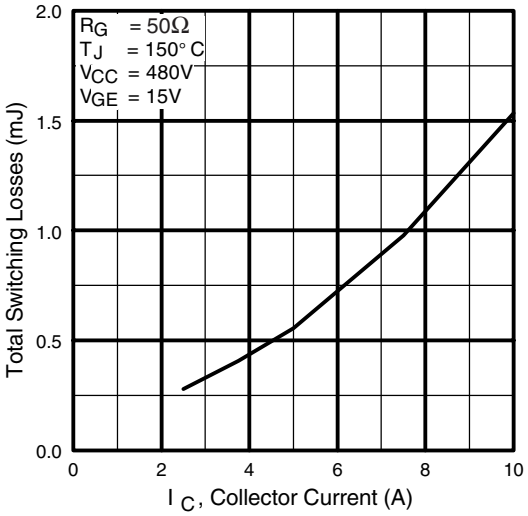


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

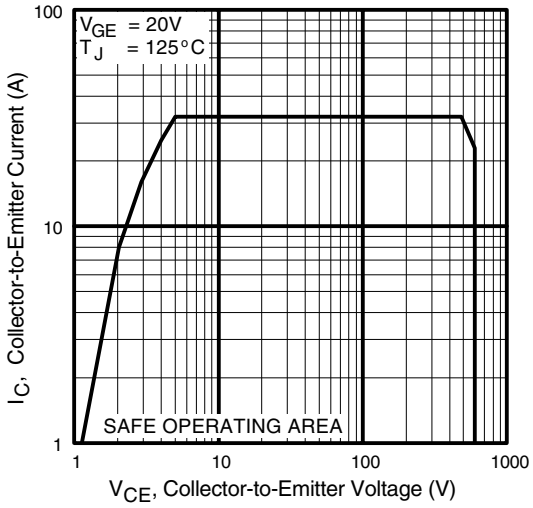


Fig. 12 - Turn-Off SOA

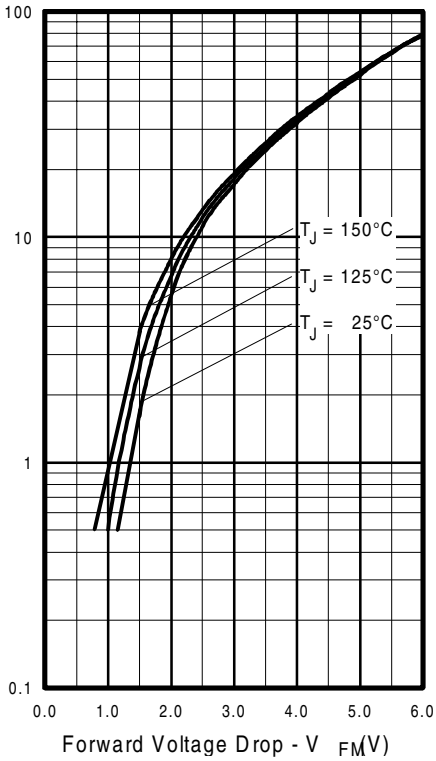


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

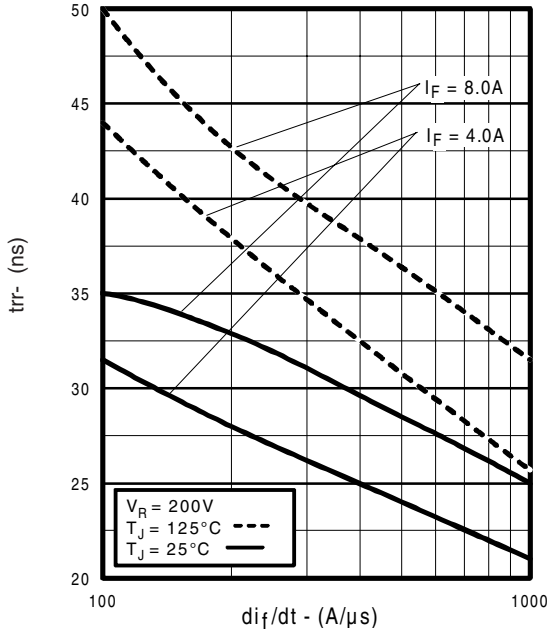


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

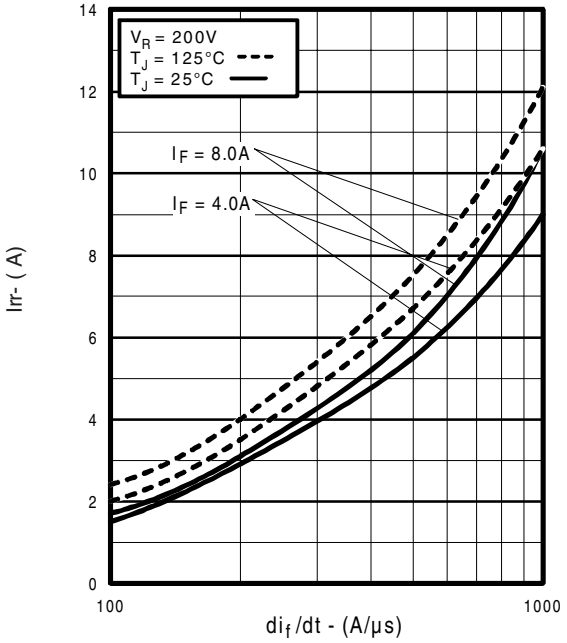


Fig. 15 - Typical Recovery Current vs. di_f/dt

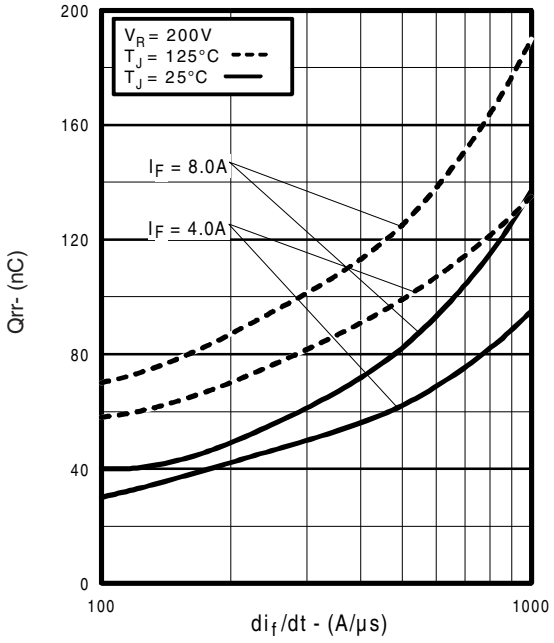


Fig. 16 - Typical Stored Charge vs. di_f/dt

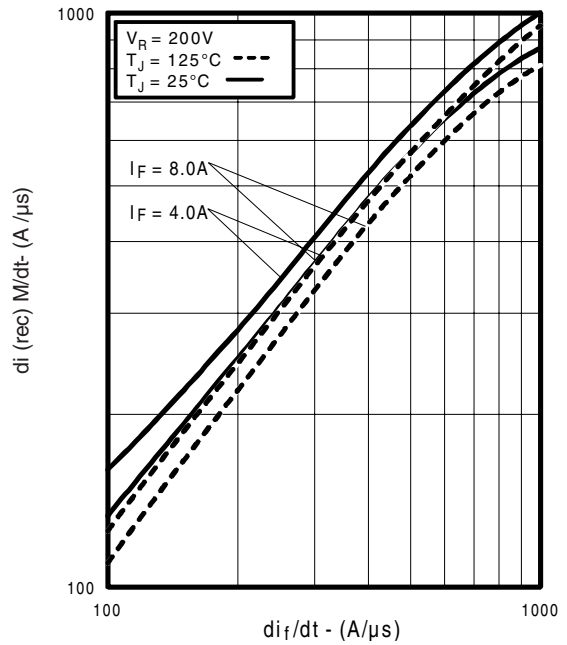


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt,

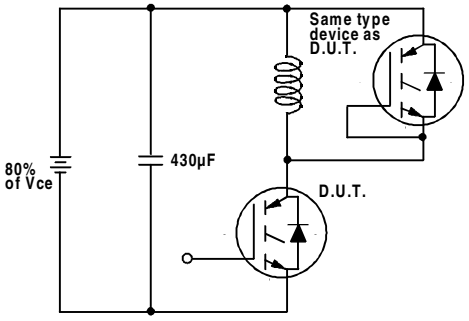


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

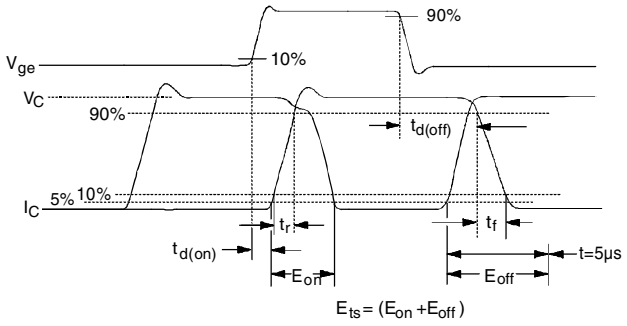


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

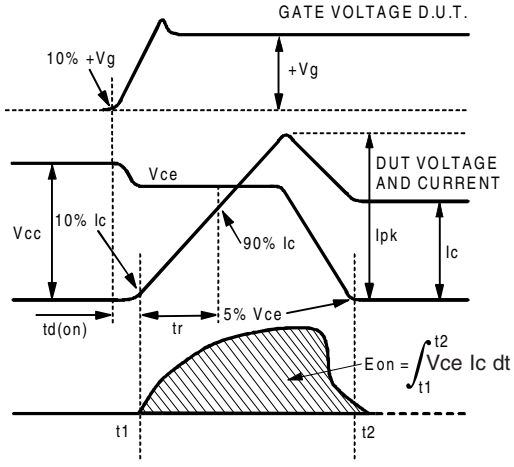


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

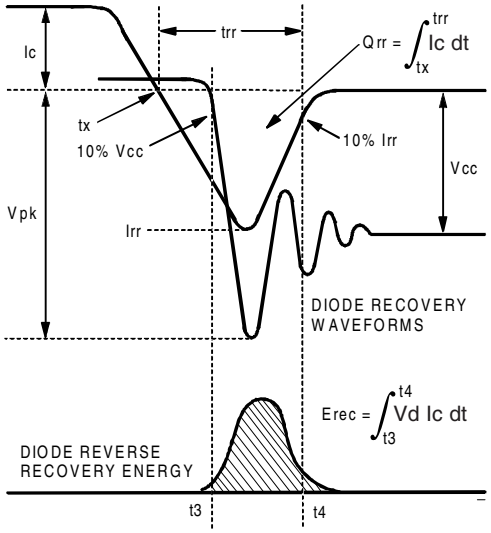


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

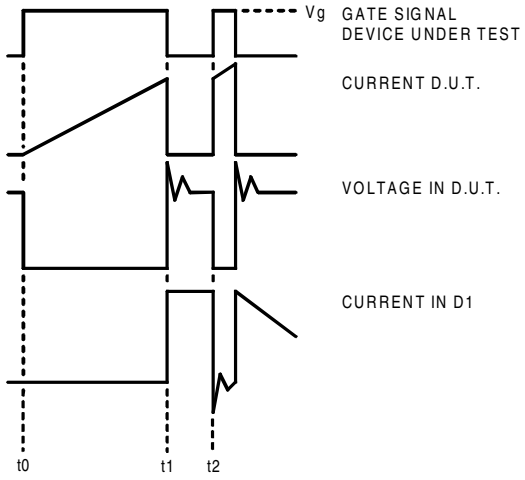


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

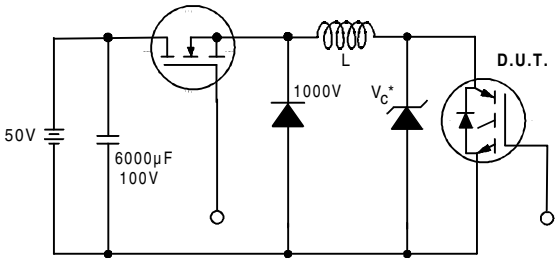


Figure 19. Clamped Inductive Load Test Circuit

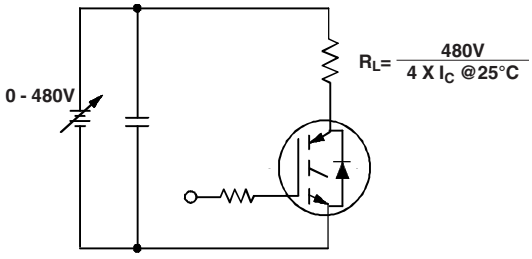


Figure 20. Pulsed Collector Current Test Circuit

Notes:

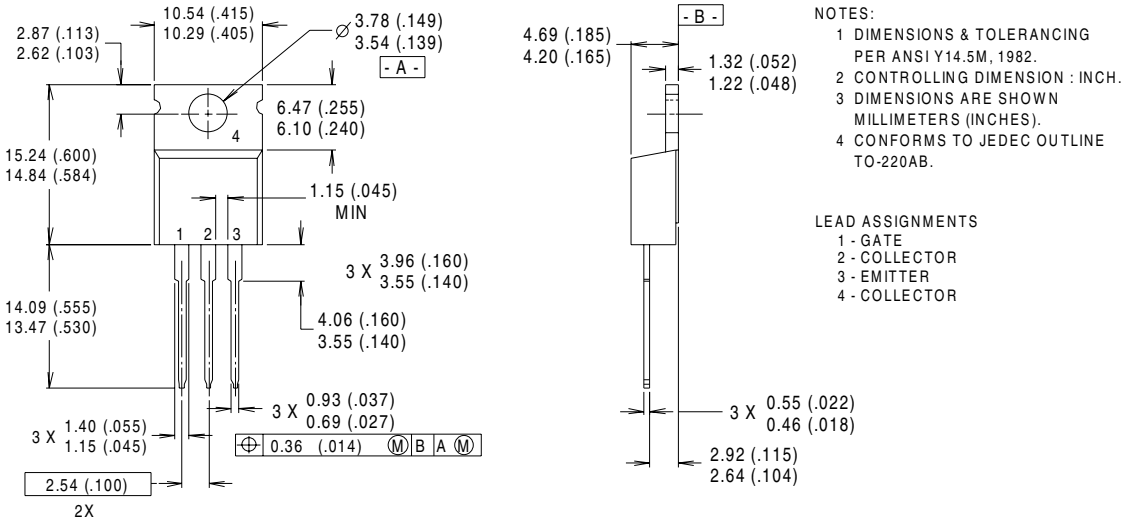
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 100Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-220AB



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-220AB.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

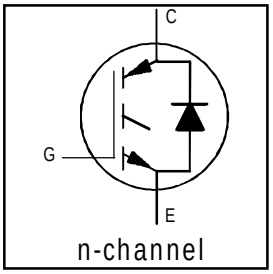
PD - 94083A

International
IOR Rectifier

IRG4BC15UD-S
IRG4BC15UD-L

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

UltraFast CoPack IGBT



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.02V

@V_{GE} = 15V, I_C = 7.8A

Features

- UltraFast: Optimized for high frequencies from10 to 30 kHz in hard switching
- IGBT Co-packaged with ultra-soft-recovery antiparallel diode
- Industry standard D^2Pak & TO-262 packages

Benefits

- Best Value for Appliance and Industrial Applications
- High noise immune "Positive Only" gate drive- Negative bias gate drive not necessary
- For Low EMI designs- requires little or no snubbing
- Single Package switch for bridge circuit applications
- Compatible with high voltage Gate Driver IC's
- Allows simpler gate drive



D^2Pak
IRG4BC15UD-S



TO-262
IRG4BC15UD-L

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	14	A
I_C @ T_C = 100°C	Continuous Collector Current	7.8	
I_{CM}	Pulsed Collector Current ①	42	
I_{LM}	Clamped Inductive Load Current ②	42	
I_F @ T_C = 100°C	Diode Continuous Forward Current	4.0	
I_{FM}	Diode Maximum Forward Current	16	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	49	W
P_D @ T_C = 100°C	Maximum Power Dissipation	19	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	——	——	2.7	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	——	——	7.0	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	——	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount ⑤	——	——	80	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state)⑥	——	——	40	
Wt	Weight	——	2 (0.07)	——	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.63	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.02	2.4	V	I_C = 7.8A V_{GE} = 15V
		—	2.56	—		I_C = 14A
		—	2.21	—		I_C = 7.8A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	4.1	6.2	—	S	V_{CE} = 100V, I_C = 7.8A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1400		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.5	1.8	V	I_C = 4.0A
		—	1.4	1.7		I_C = 4.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	23	35	nC	I_C = 7.8A
Qge	Gate - Emitter Charge (turn-on)	—	4.0	6.0		V_{CC} = 400V
Q_{gc}	Gate - Collector Charge (turn-on)	—	9.6	14		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	T_J = 25°C
t_r	Rise Time	—	20	—		I_C = 7.8A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	160	240		V_{GE} = 15V, R_G = 75Ω
t_f	Fall Time	—	83	120		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	0.24	—	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	0.26	—		
E_{ts}	Total Switching Loss	—	0.50	0.63		
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	T_J = 150°C,
t_r	Rise Time	—	21	—		I_C = 7.8A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	180	—		V_{GE} = 15V, R_G = 75Ω
t_f	Fall Time	—	220	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	0.76	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	410	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	37	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	5.3	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	28	42	ns	T_J = 25°C
		—	38	57		T_J = 125°C I_F = 4.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	2.9	5.2	A	T_J = 25°C
		—	3.7	6.7		T_J = 125°C V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	40	60	nC	T_J = 25°C
		—	70	110		T_J = 125°C di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	280	—	A/µs	T_J = 25°C
	During t_b	—	240	—		T_J = 125°C

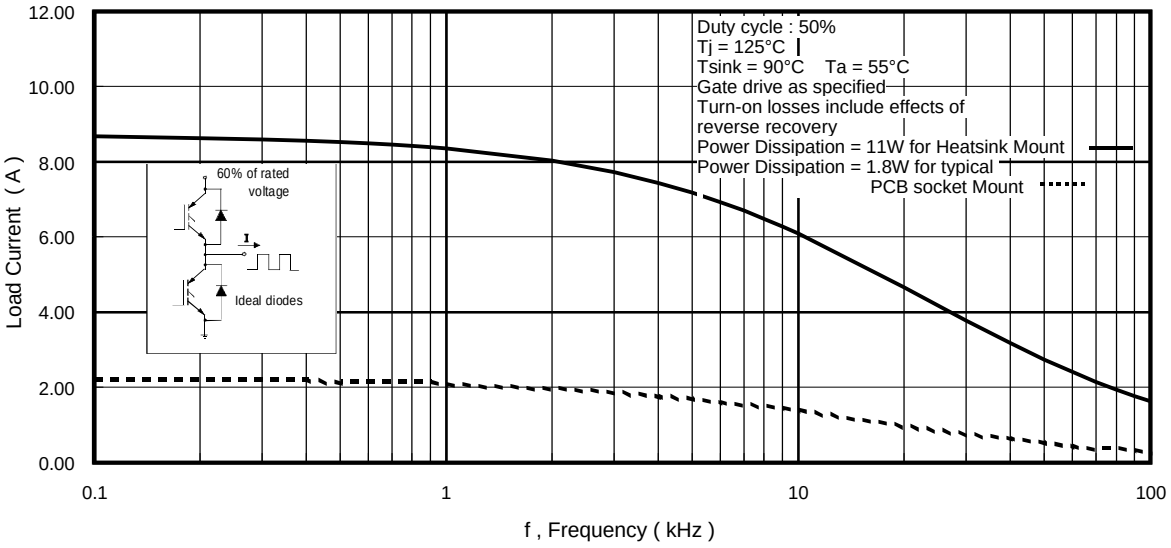


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

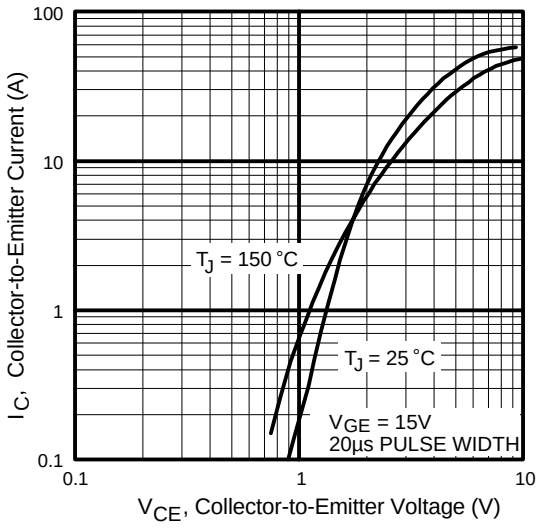


Fig. 2 - Typical Output Characteristics

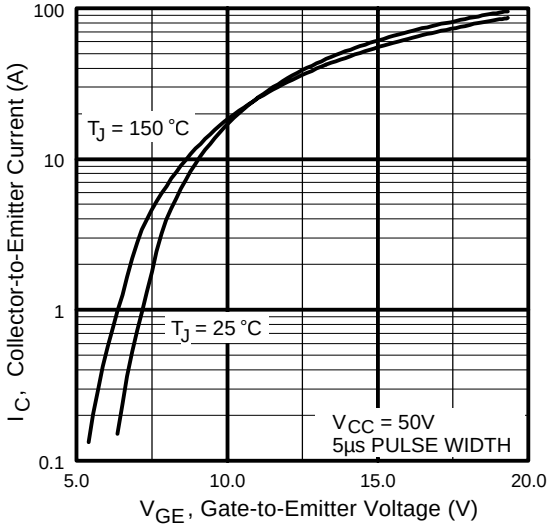


Fig. 3 - Typical Transfer Characteristics

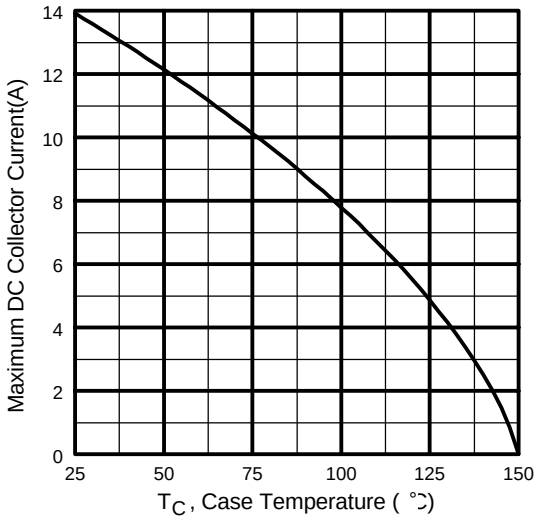


Fig. 4 - Maximum Collector Current vs. Case Temperature

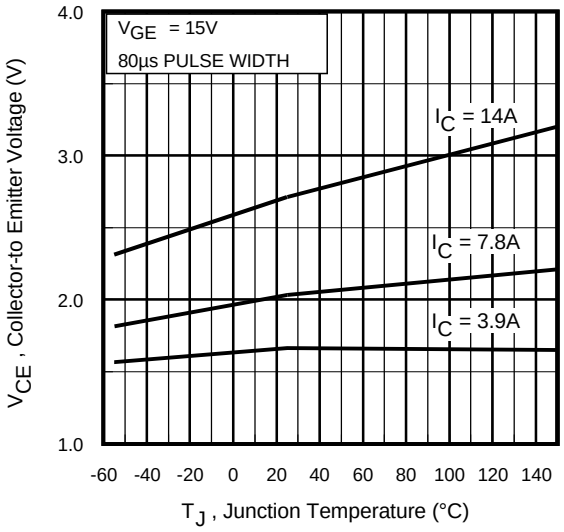


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

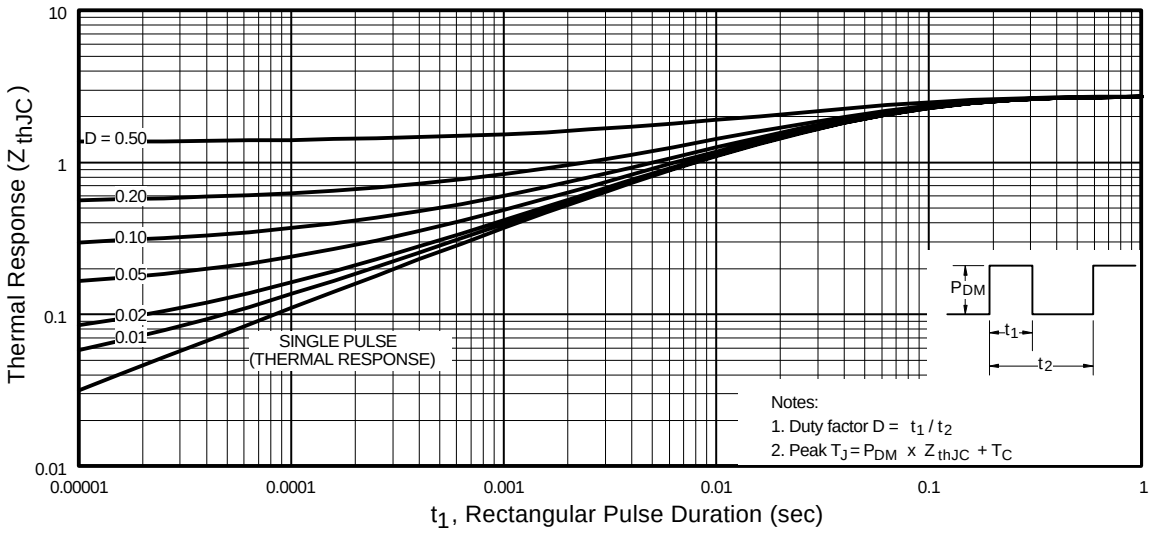


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

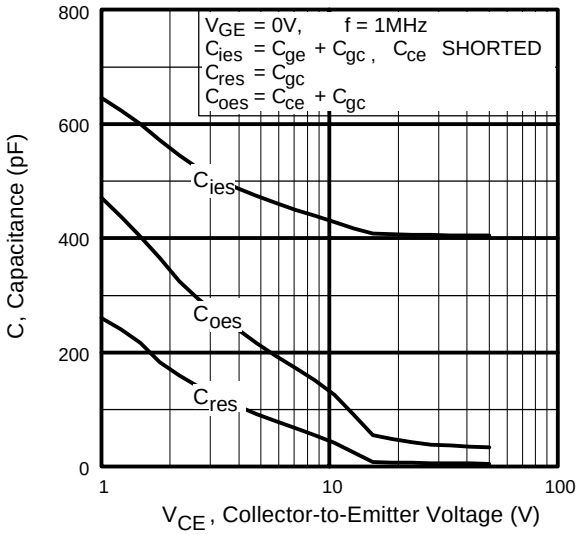


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

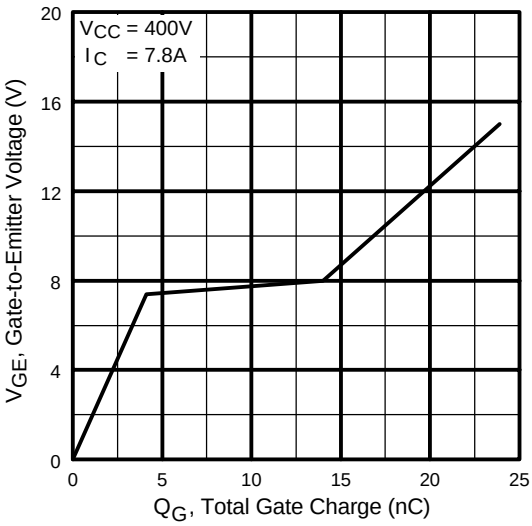


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

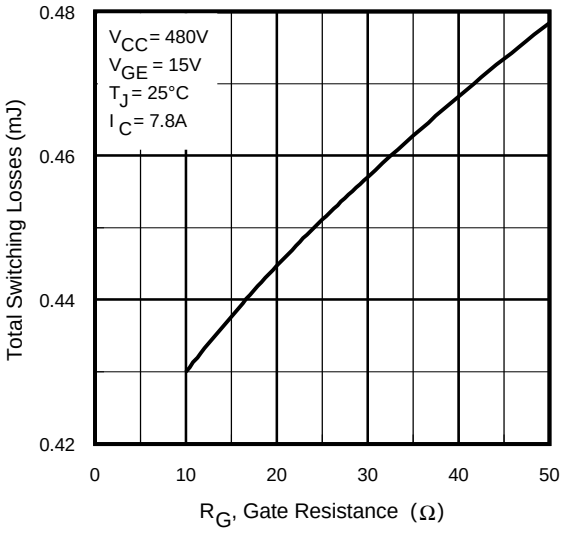


Fig. 9 - Typical Switching Losses vs. Gate Resistance

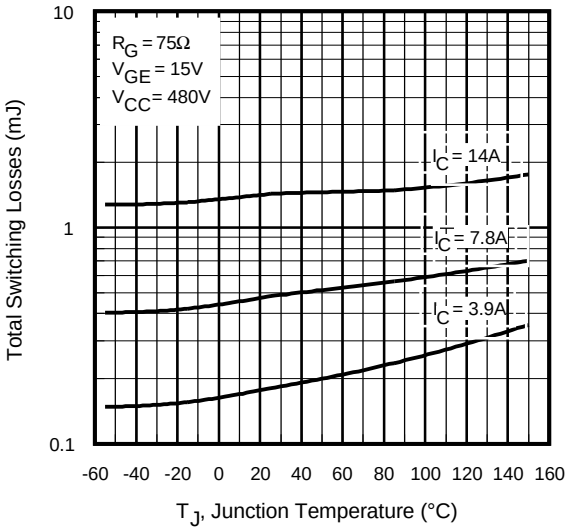


Fig. 10 - Typical Switching Losses vs. Junction Temperature

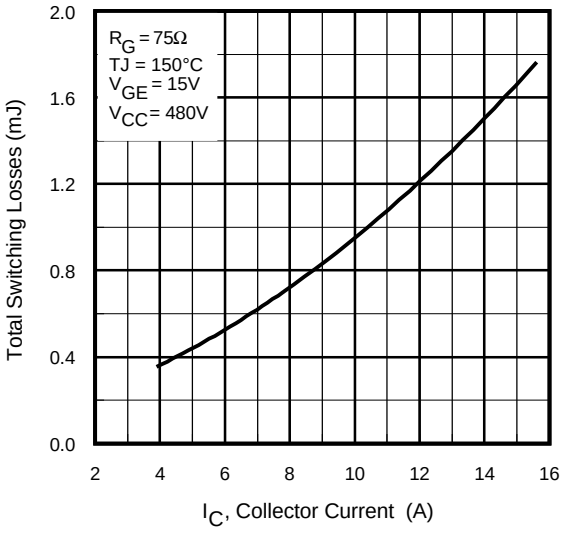


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

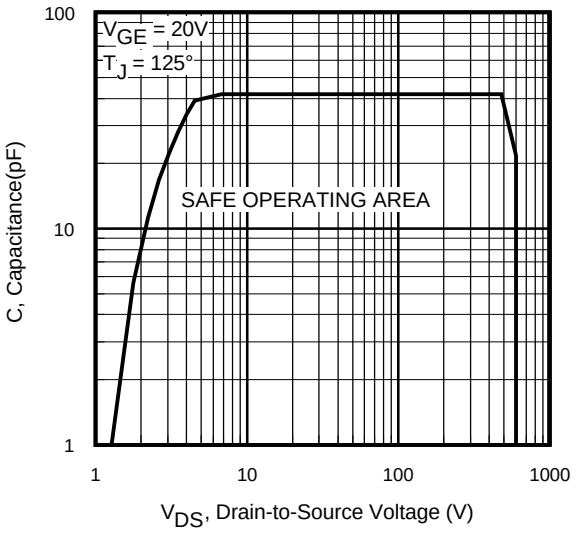


Fig. 12 - Turn-Off SOA

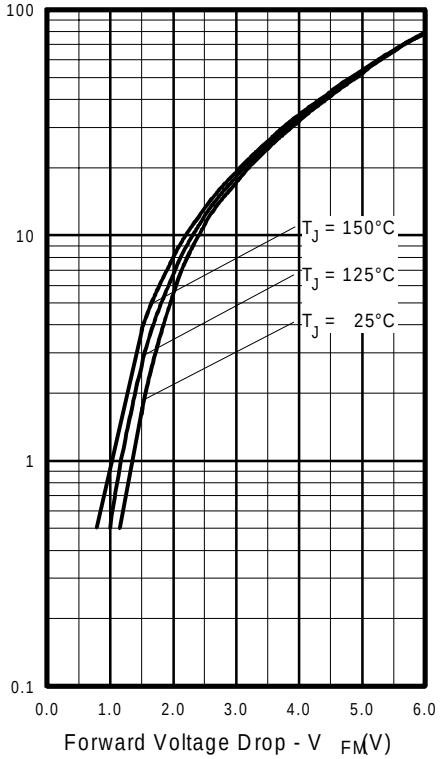


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

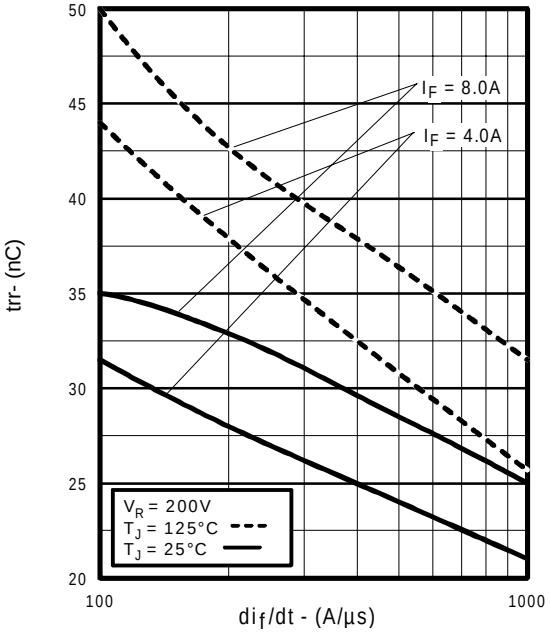


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

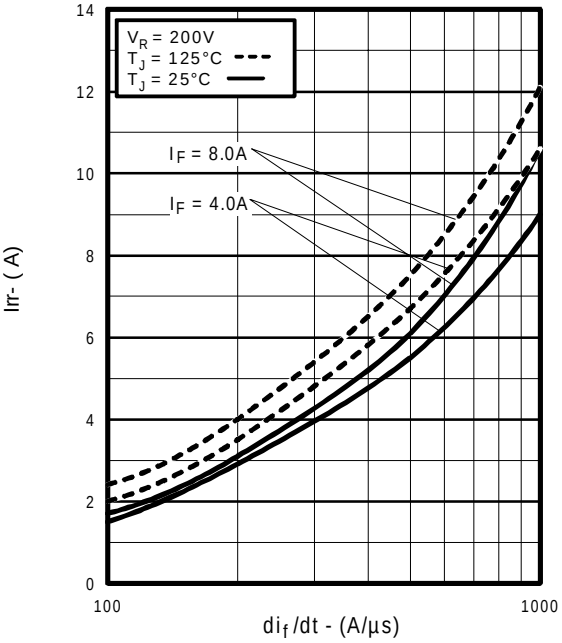


Fig. 15 - Typical Recovery Current vs. di_f/dt

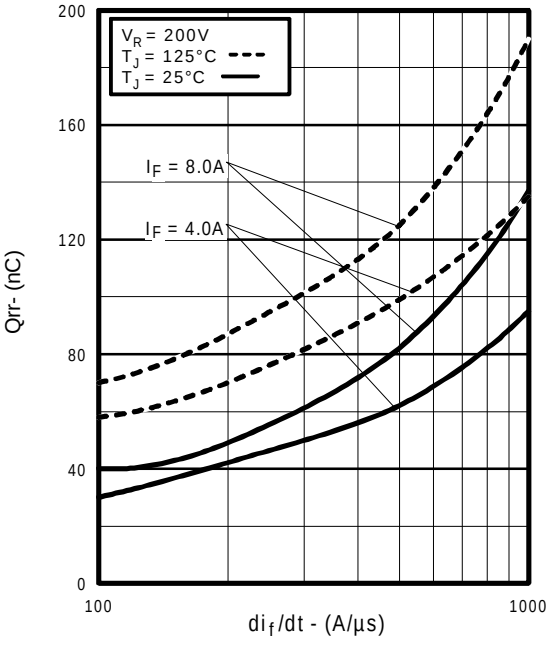


Fig. 16 - Typical Stored Charge vs. di_f/dt

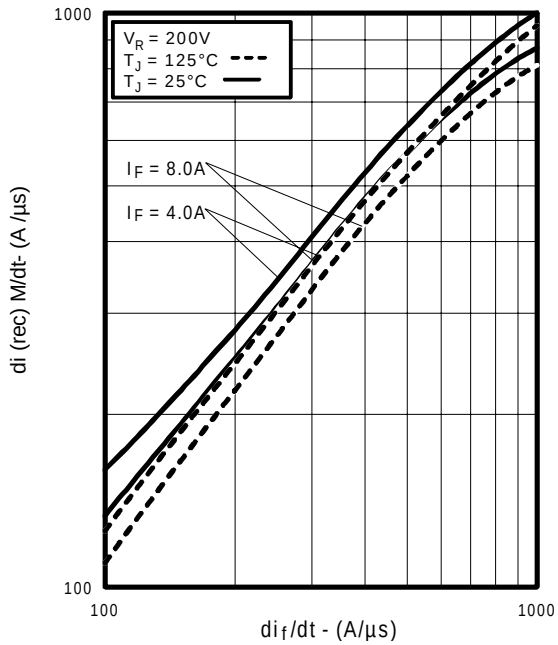


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt,

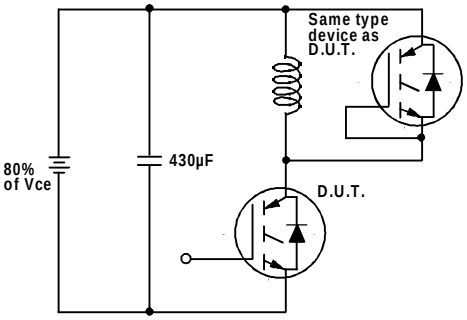


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

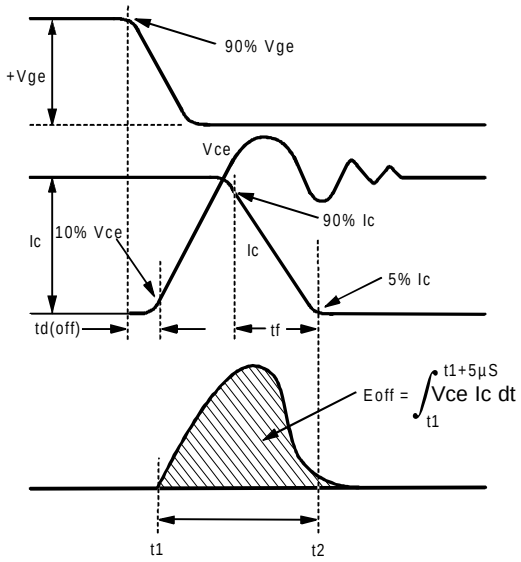


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

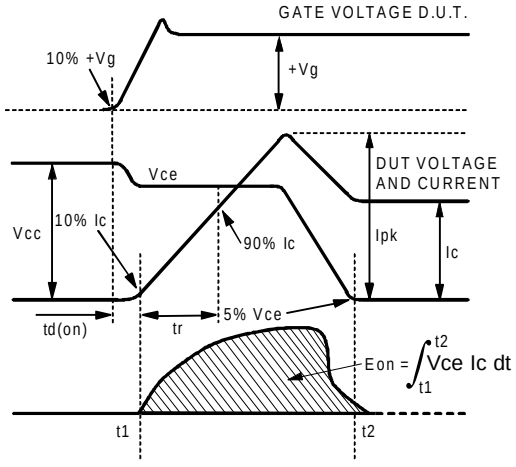


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

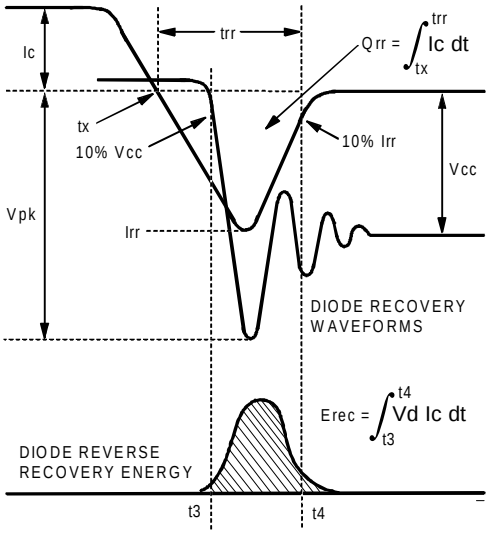


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

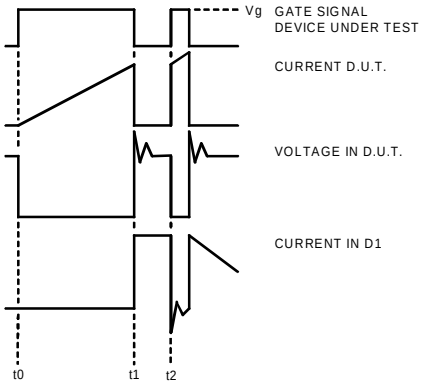


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

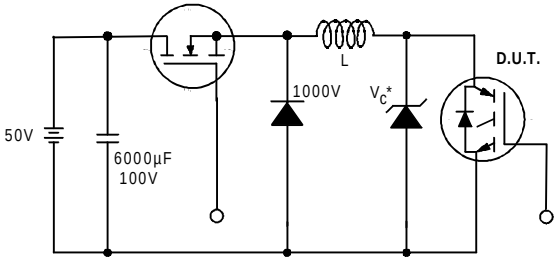


Figure 19. Clamped Inductive Load Test Circuit

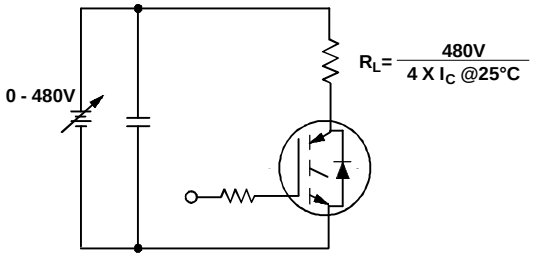
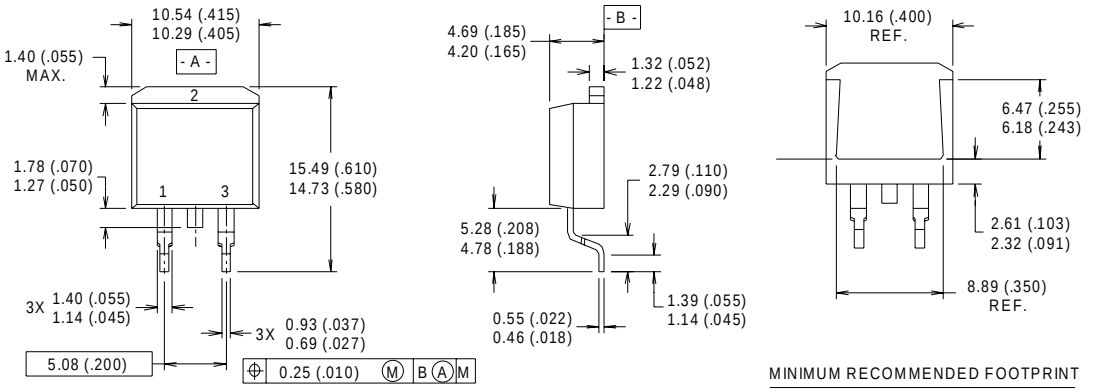


Figure 20. Pulsed Collector Current Test Circuit

D²Pak Package Outline



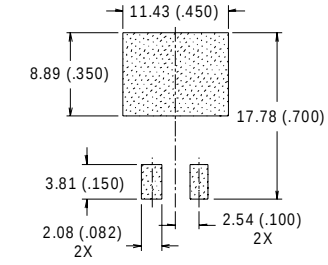
NOTES:

1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

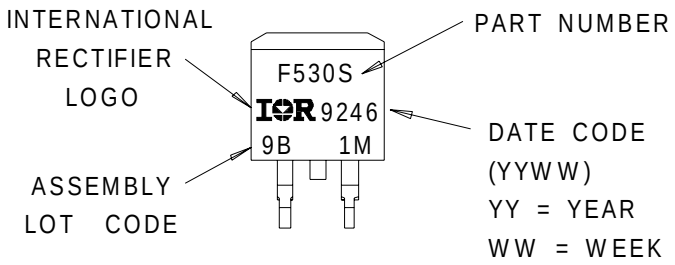
LEAD ASSIGNMENTS

1 - GATE
2 - DRAIN
3 - SOURCE

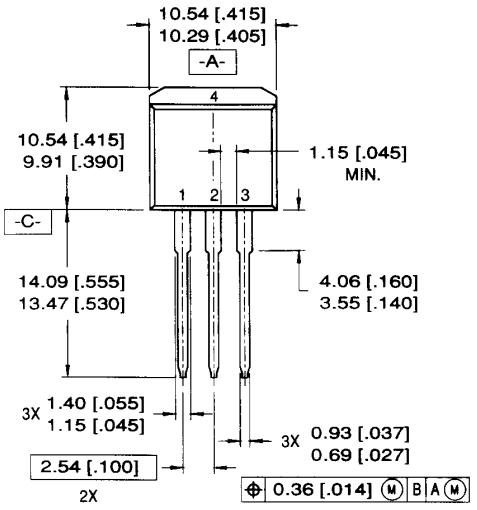
MINIMUM RECOMMENDED FOOTPRINT



D²Pak Part Marking Information

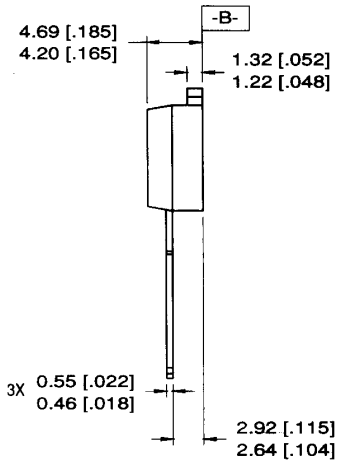


TO-262 Package Outline



LEAD ASSIGNMENTS

1 = GATE 3 = SOURCE
2 = DRAIN 4 = DRAIN

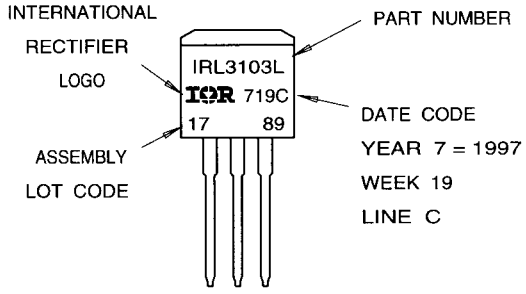


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

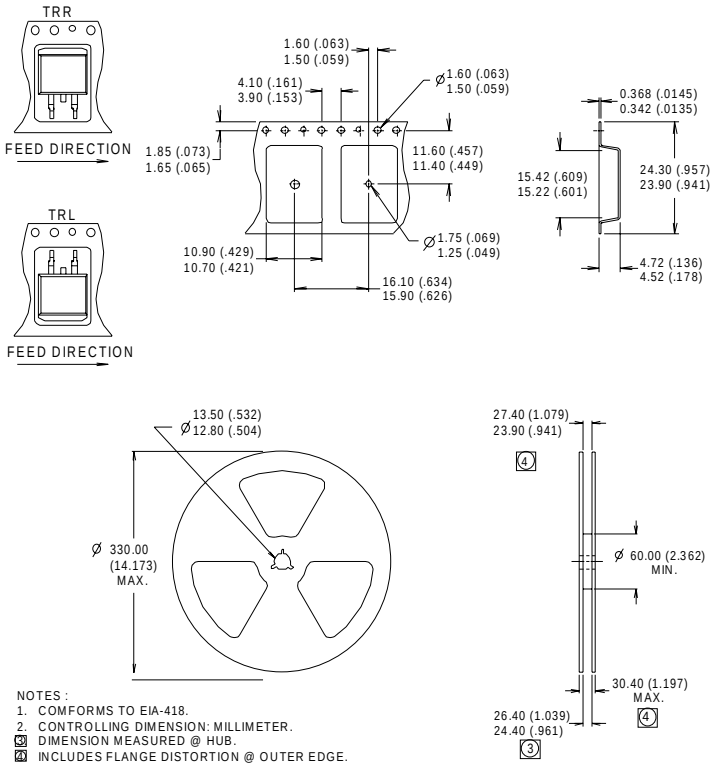
EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



IRG4BC15UD-S/L

International
IOR Rectifier

D²Pak Tape & Reel Information



NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
③ DIMENSION MEASURED @ HUB.
④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Notes:

① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature.

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 75Ω

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

⑤ This only applies to TO-262 package.

⑥ This applies to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.06/01

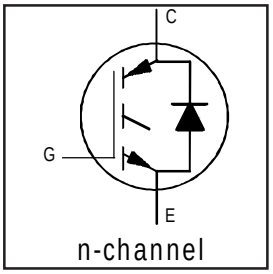
PD - 94082A

International
IOR Rectifier

IRG4BC15UD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

UltraFast CoPack IGBT



n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.02V

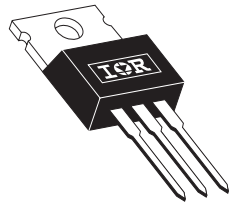
@V_{GE} = 15V, I_C = 7.8A

Features

- UltraFast: Optimized for high frequencies from10 to 30 kHz in hard switching
- IGBT Co-packaged with ultra-soft-recovery antiparallel diode
- Industry standard TO-220AB package

Benefits

- Best Value for Appliance and Industrial Applications
- High noise immune "Positive Only" gate drive- Negative bias gate drive not necessary
- For Low EMI designs- requires little or no snubbing
- Single Package switch for bridge circuit applications
- Compatible with high voltage Gate Driver IC's
- Allows simpler gate drive


TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	14	A
I_C @ T_C = 100°C	Continuous Collector Current	7.8	
I_{CM}	Pulsed Collector Current ①	42	
I_{LM}	Clamped Inductive Load Current ②	42	
I_F @ T_C = 100°C	Diode Continuous Forward Current	4.0	
I_{FM}	Diode Maximum Forward Current	16	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	49	W
P_D @ T_C = 100°C	Maximum Power Dissipation	19	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	2.7	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	7.0	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	80	
Wt	Weight	—	2 (0.07)	—	g (oz)

03/20/01

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.63	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.02	2.4	V	I_C = 7.8A V_{GE} = 15V
		—	2.56	—		I_C = 14A
		—	2.21	—		I_C = 7.8A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	4.1	6.2	—	S	V_{CE} = 100V, I_C = 7.8A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1400		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.5	1.8	V	I_C = 4.0A
		—	1.4	1.7		I_C = 4.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	23	35	nC	I_C = 7.8A
Qge	Gate - Emitter Charge (turn-on)	—	4.0	6.0		V_{CC} = 400V
Q_{gc}	Gate - Collector Charge (turn-on)	—	9.6	14		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	T_J = 25°C
t_r	Rise Time	—	20	—		I_C = 7.8A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	160	240		V_{GE} = 15V, R_G = 75Ω
t_f	Fall Time	—	83	120		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	0.24	—	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	0.26	—		
E_{ts}	Total Switching Loss	—	0.50	0.63		
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	T_J = 150°C,
t_r	Rise Time	—	21	—		I_C = 7.8A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	180	—		V_{GE} = 15V, R_G = 75Ω
t_f	Fall Time	—	220	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	0.76	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	410	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	37	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	5.3	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	28	42	ns	T_J = 25°C
		—	38	57		T_J = 125°C I_F = 4.0A
$_{rr}$	Diode Peak Reverse Recovery Current	—	2.9	5.2	A	T_J = 25°C
		—	3.7	6.7		T_J = 125°C V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	40	60	nC	T_J = 25°C
		—	70	110		T_J = 125°C di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	280	—	A/µs	T_J = 25°C
	During t_b	—	240	—		T_J = 125°C

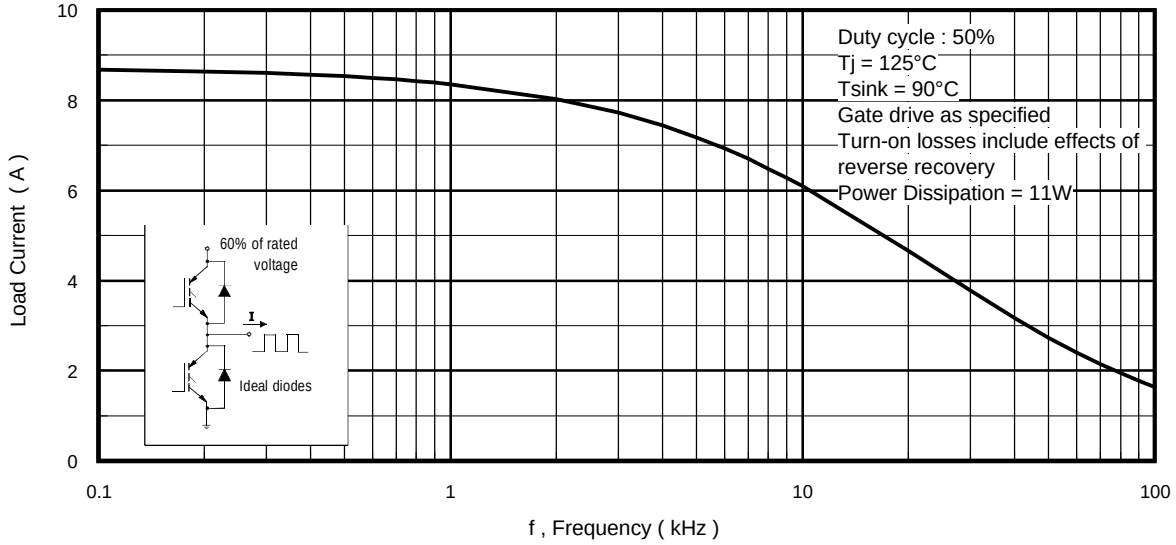


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

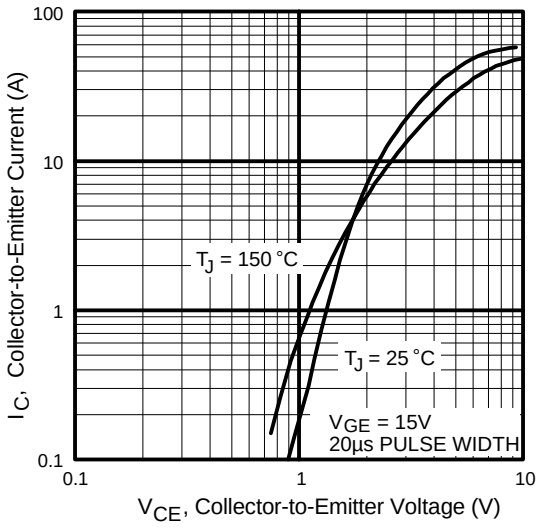


Fig. 2 - Typical Output Characteristics

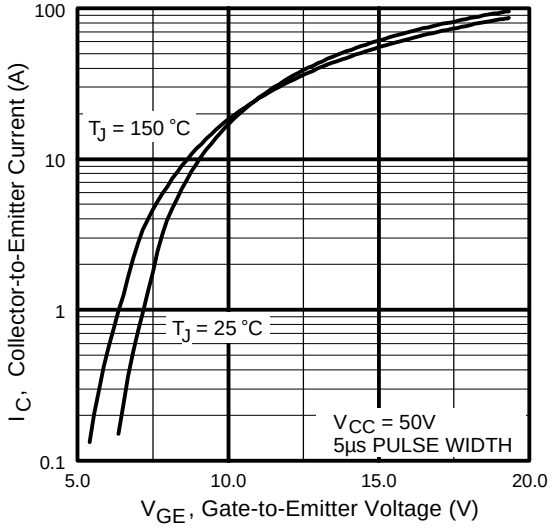


Fig. 3 - Typical Transfer Characteristics

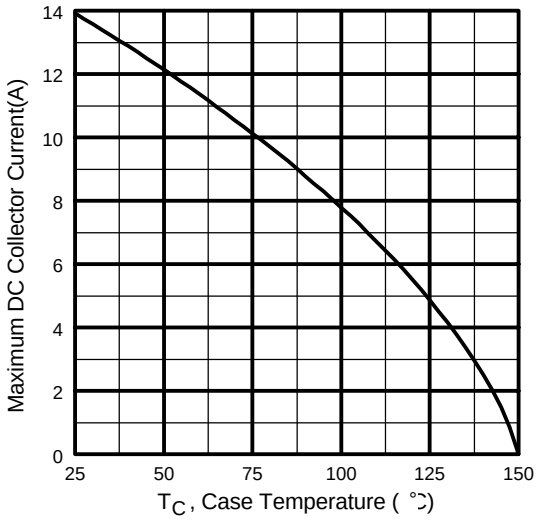


Fig. 4 - Maximum Collector Current vs. Case Temperature

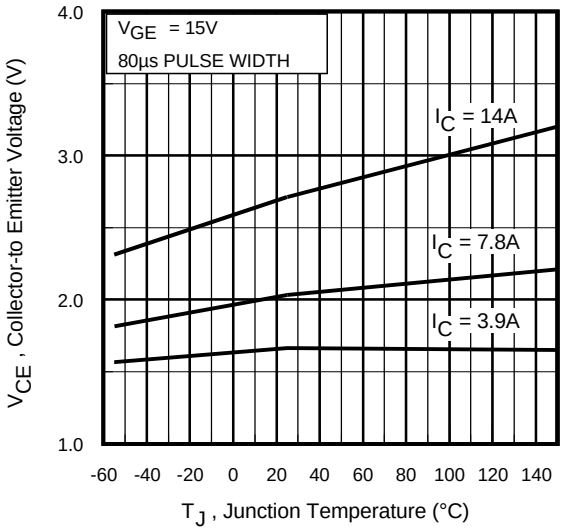


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

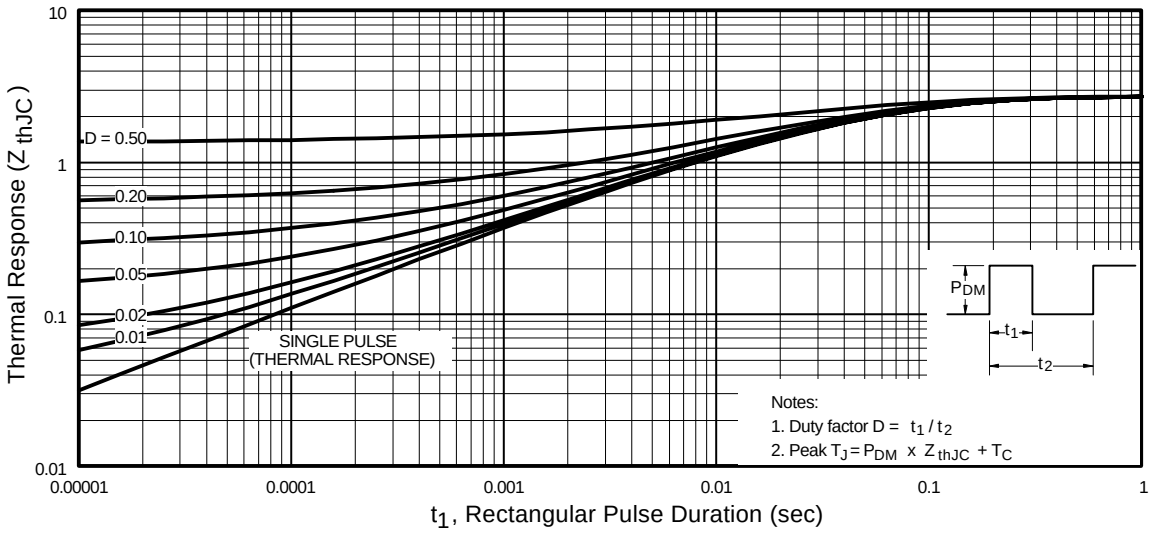


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

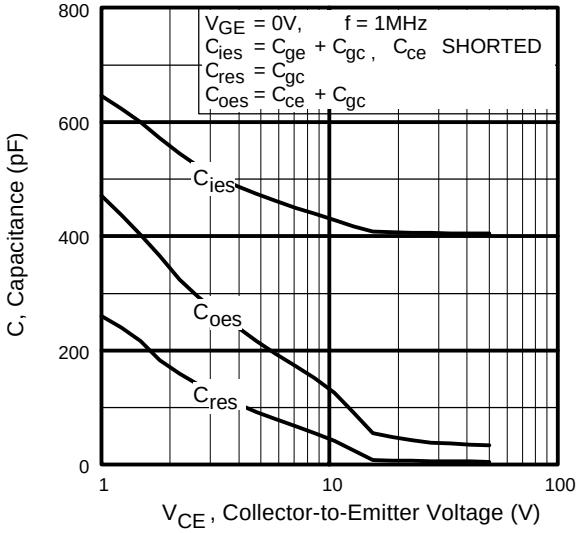


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

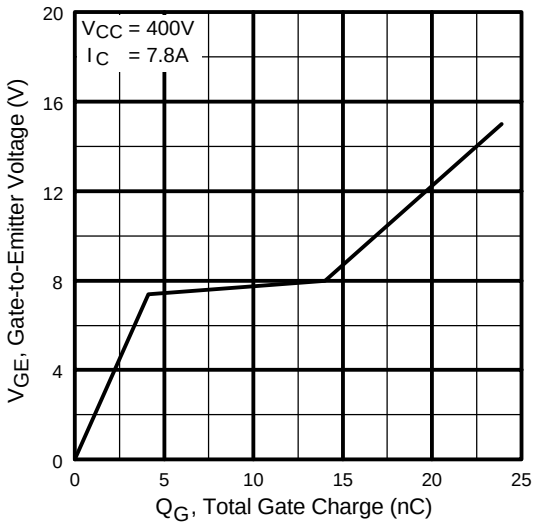


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

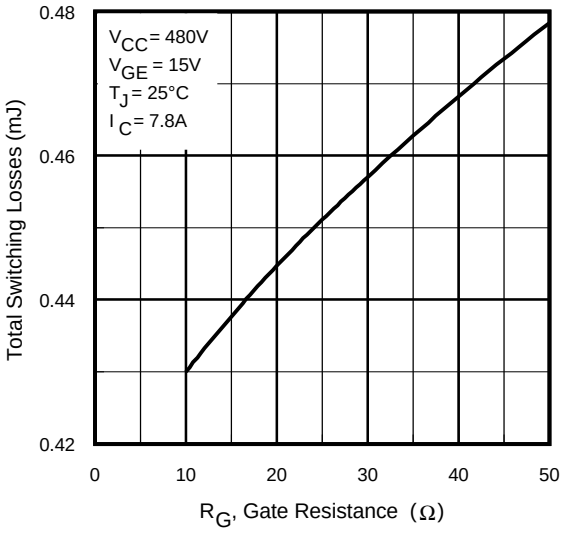


Fig. 9 - Typical Switching Losses vs. Gate Resistance

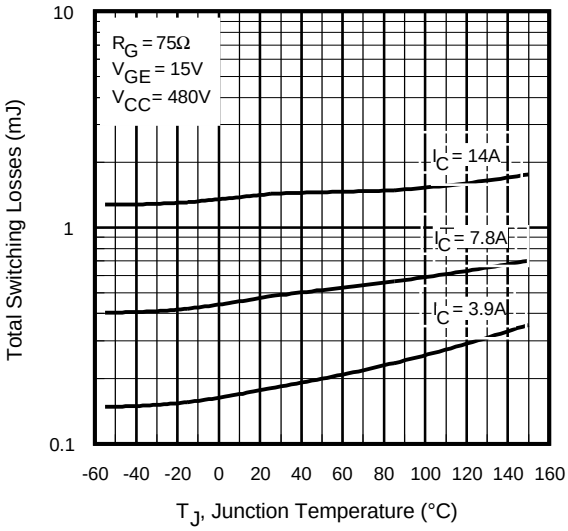


Fig. 10 - Typical Switching Losses vs. Junction Temperature

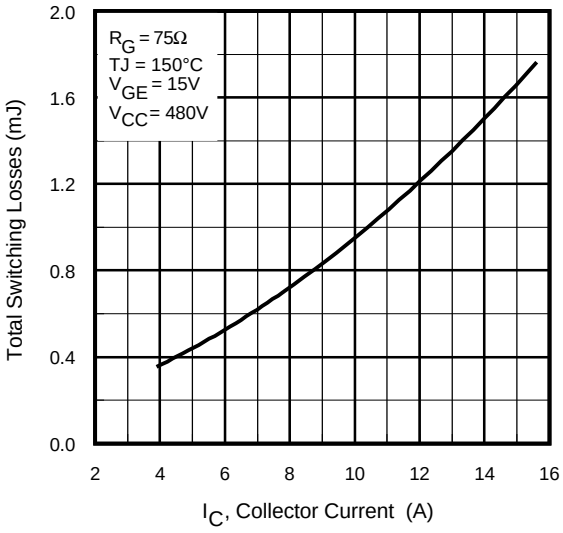


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

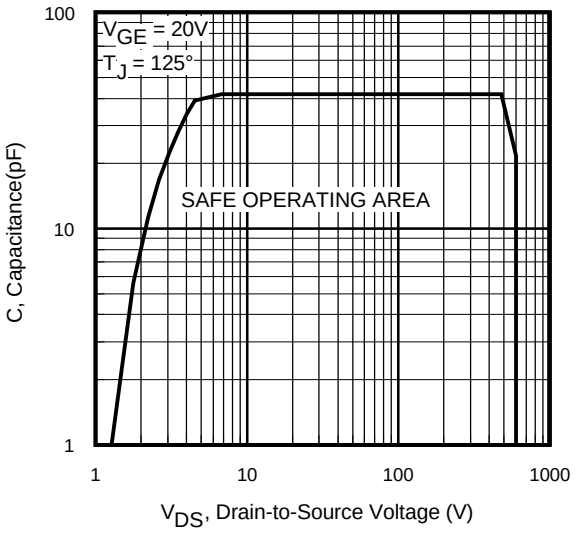


Fig. 12 - Turn-Off SOA

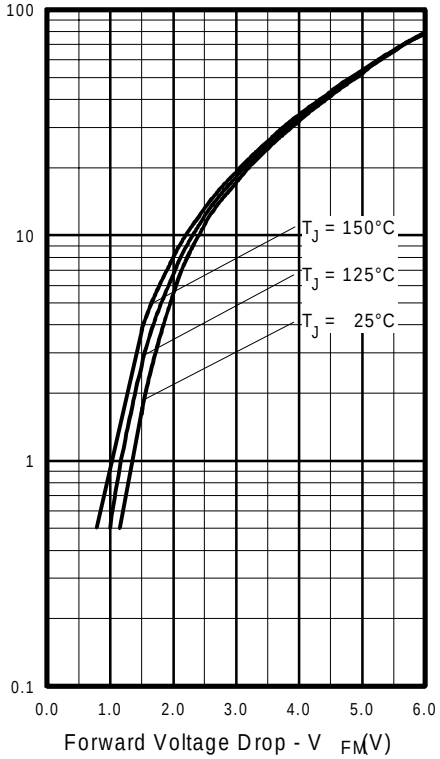


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

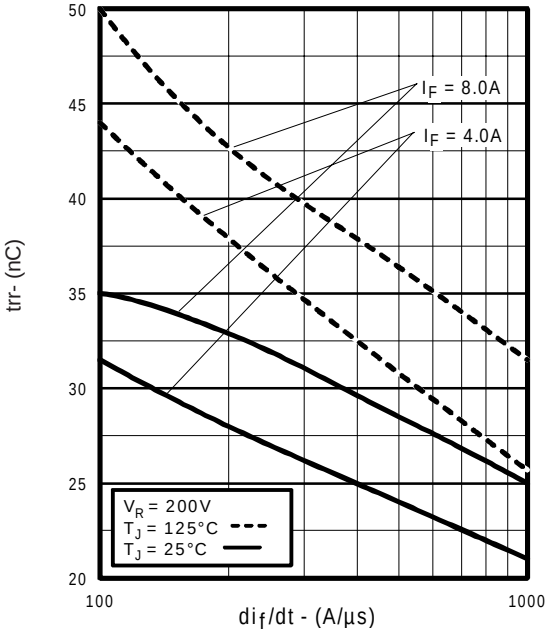


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

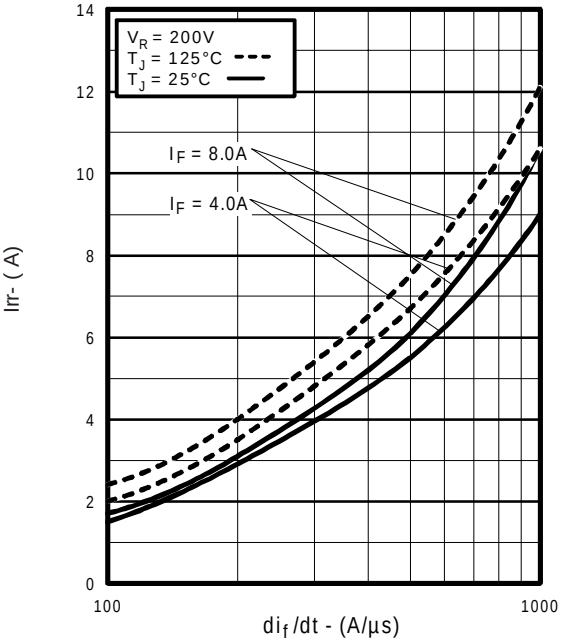


Fig. 15 - Typical Recovery Current vs. di_f/dt

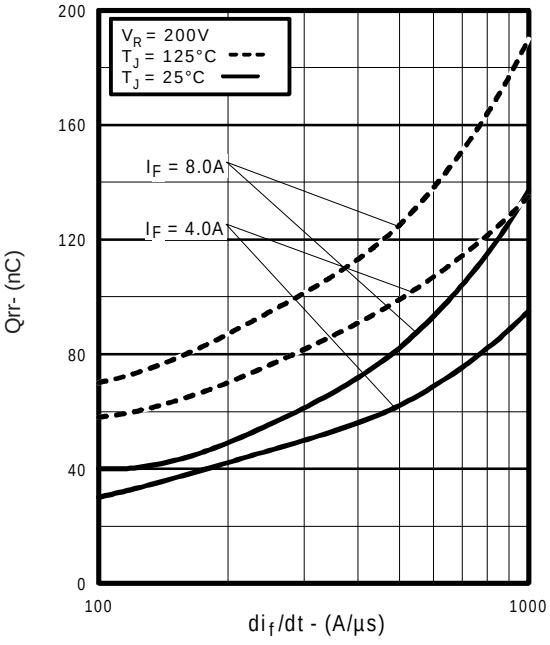


Fig. 16 - Typical Stored Charge vs. di_f/dt

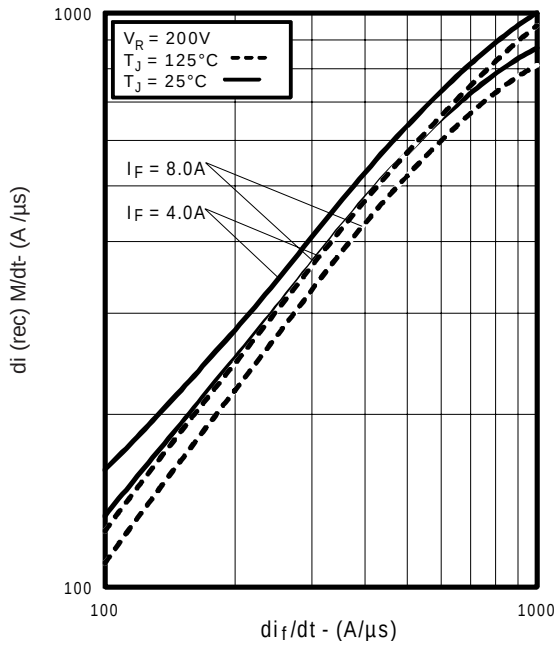


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt,

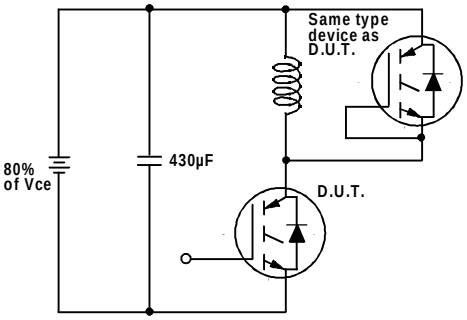


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

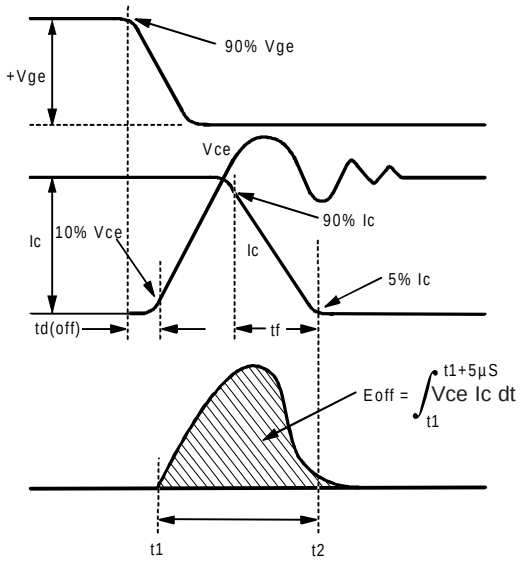


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

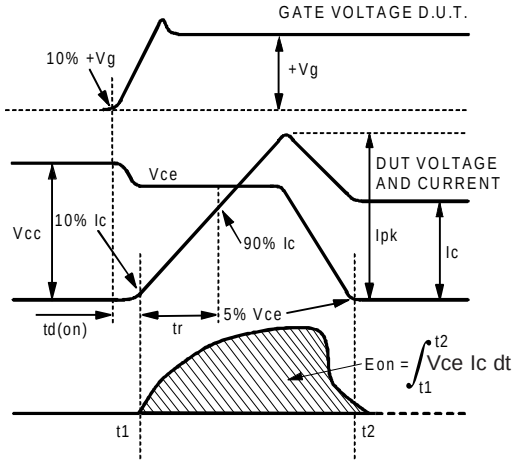


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

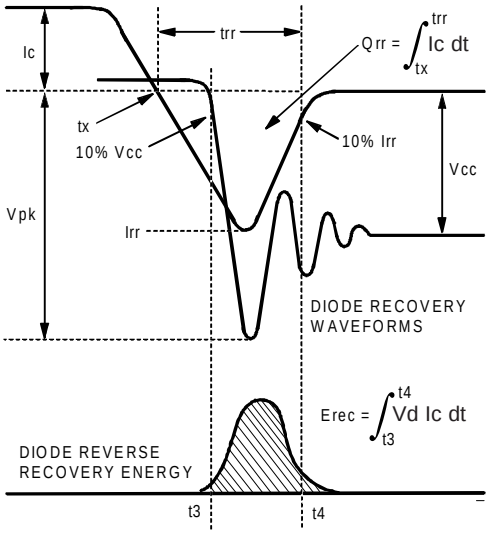


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

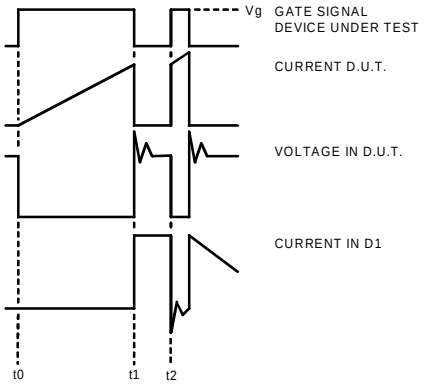


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

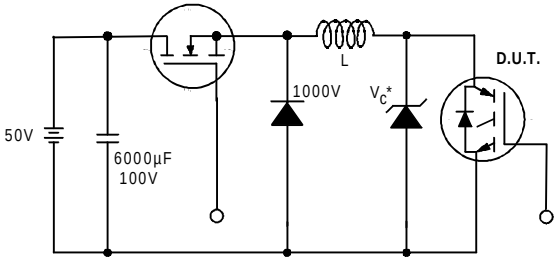


Figure 19. Clamped Inductive Load Test Circuit

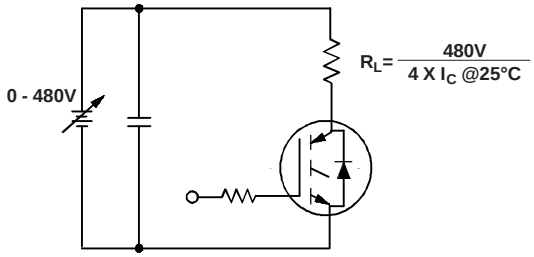


Figure 20. Pulsed Collector Current Test Circuit

Notes:

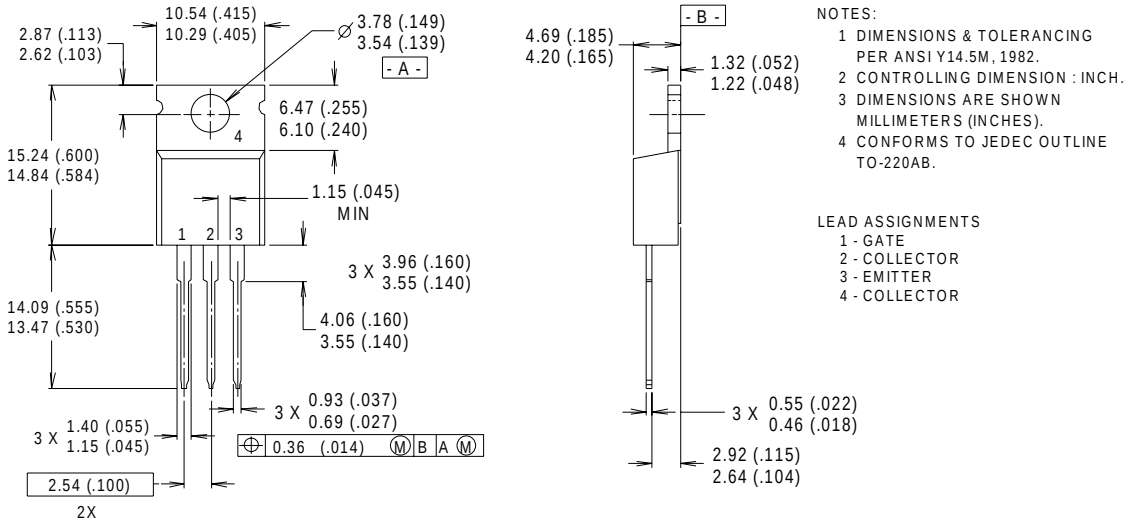
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 75Ω

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-220AB



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-220AB.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.03/01

PD -91752A

International
IOR Rectifier

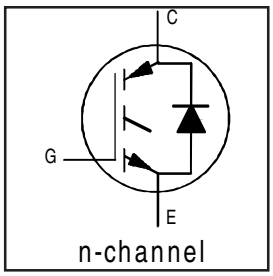
IRG4IBC20UD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

UltraFast CoPack IGBT

Features

- 2.5kV, 60s insulation voltage ⑤
- 4.8 mm creapage distance to heatsink
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- IGBT co-packaged with HEXFRED™ ultrafast, ultrasoft recovery antiparallel diodes
- Tighter parameter distribution
- Industry standard Isolated TO-220 Fullpak™ outline

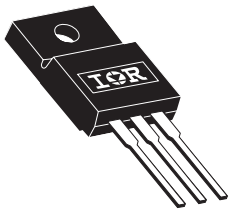


n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.85V

@V_{GE} = 15V, I_C = 6.5A



TO-220 FULLPAK

Benefits

- Simplified assembly
- Highest efficiency and power density
- HEXFRED™ antiparallel Diode minimizes switching losses and EMI

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	11.4	A
I_C @ T_C = 100°C	Continuous Collector Current	6.0	
I_{CM}	Pulsed Collector Current ①	52	
I_{LM}	Clamped Inductive Load Current ②	52	
I_F @ T_C = 100°C	Diode Continuous Forward Current	6.5	
I_{FM}	Diode Maximum Forward Current	52	
Visol	RMS Isolation Voltage, Terminal to Case⑤	2500	V
V_{GE}	Gate-to-Emitter Voltage	± 20	
P_D @ T_C = 25°C	Maximum Power Dissipation	34	W
P_D @ T_C = 100°C	Maximum Power Dissipation	14	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	——	3.7	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	——	5.1	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	65	
Wt	Weight	2.0 (0.07)	——	g (oz)

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.69	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.85	2.1	V	I_C = 6.5A, V_{GE} = 15V
		—	2.27	—		I_C = 13A, See Fig. 2, 5
		—	1.87	—		I_C = 6.5A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	1.4	4.3	—	S	V_{CE} = 100V, I_C = 6.5A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1700		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 8.0A, See Fig. 13
		—	1.3	1.6		I_C = 8.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	27	41		I_C = 6.5A
Qge	Gate - Emitter Charge (turn-on)	—	4.5	6.8	nC	V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	10	16		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	39	—		T_J = 25°C
t_r	Rise Time	—	15	—	ns	I_C = 6.5A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	93	140		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	110	170		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	0.16	—		diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	0.13	—	mJ	See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	—	0.29	0.3		
$t_{d(on)}$	Turn-On Delay Time	—	38	—		T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	—	17	—	ns	I_C = 6.5A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	100	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	220	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	0.49	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	530	—		V_{GE} = 0V
C_{oes}	Output Capacitance	—	39	—	pF	V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	7.4	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	37	55	ns	T_J = 25°C See Fig.
		—	55	90		T_J = 125°C 14 I_F = 8.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	5.0	A	T_J = 25°C See Fig.
		—	4.5	8.0		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	65	138	nC	T_J = 25°C See Fig.
		—	124	360		T_J = 125°C 16 di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	240	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	210	—		T_J = 125°C 17

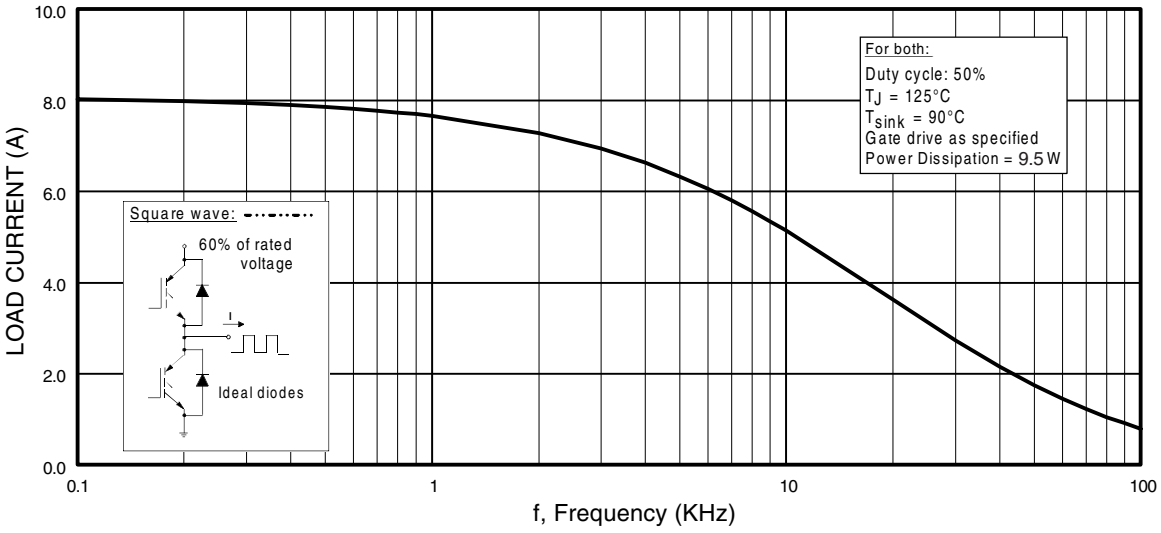


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

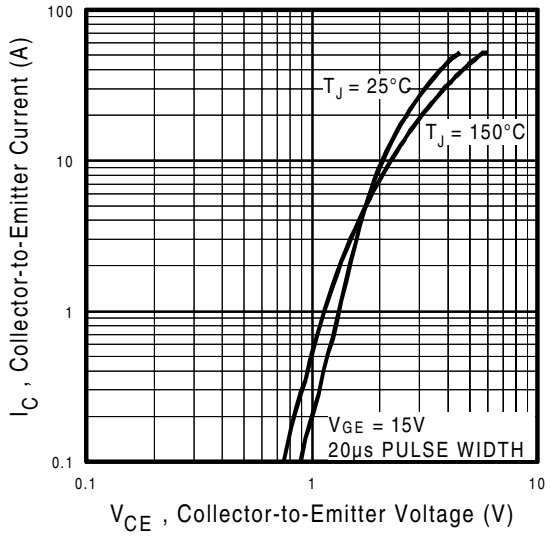


Fig. 2 - Typical Output Characteristics

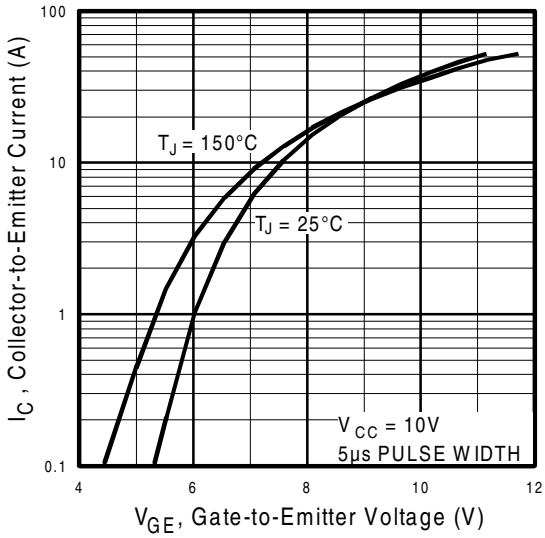


Fig. 3 - Typical Transfer Characteristics

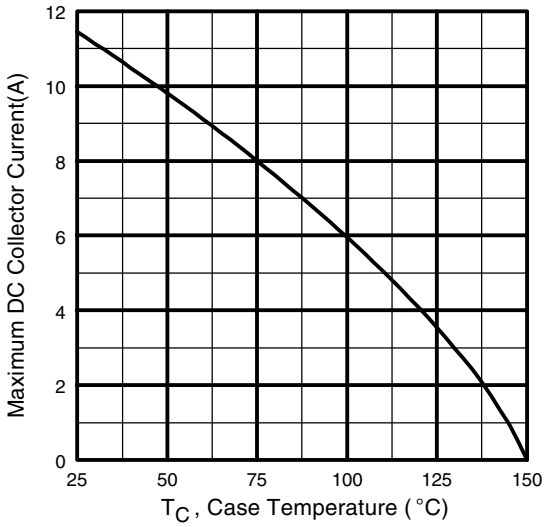


Fig. 4 - Maximum Collector Current vs. Case Temperature

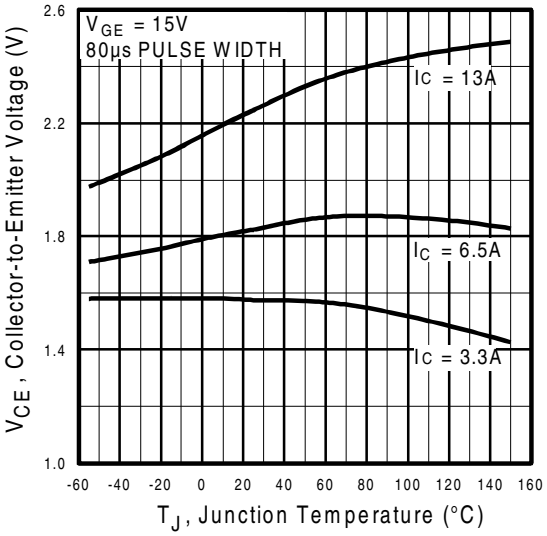


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

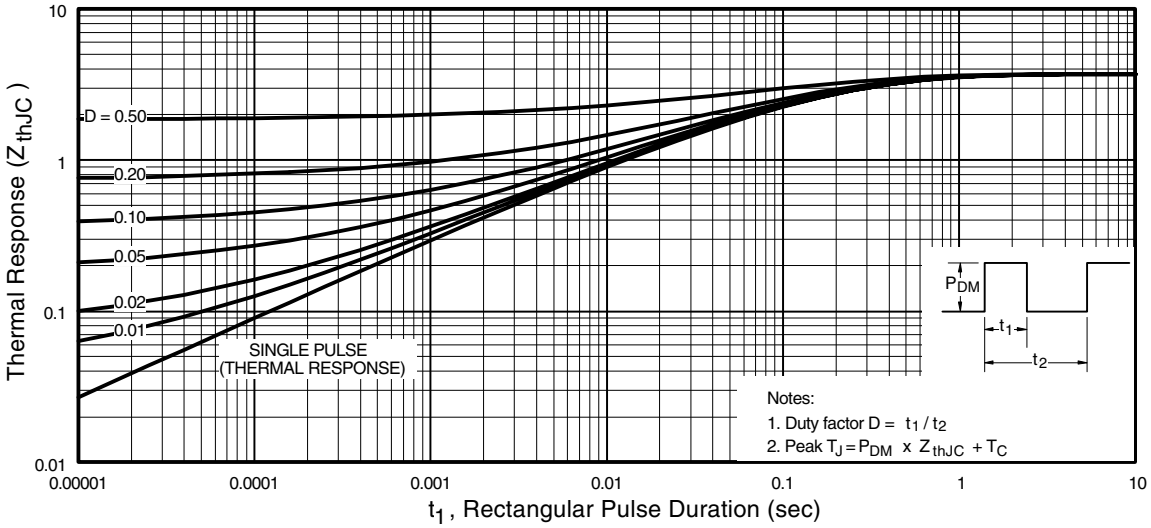


Fig. 6 - Maximum IGBT Effective Transient Thermal Impedance, Junction-to-Case

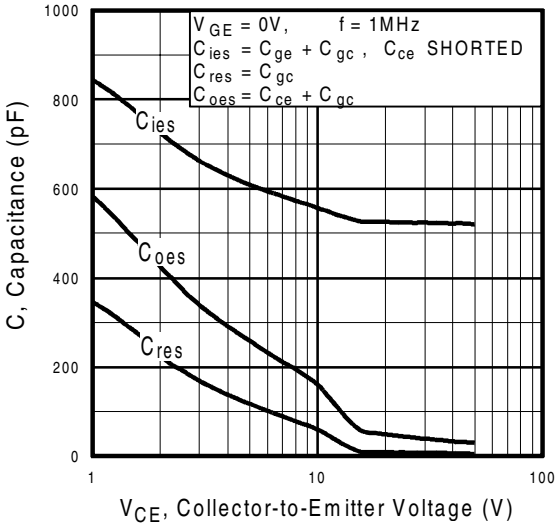


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

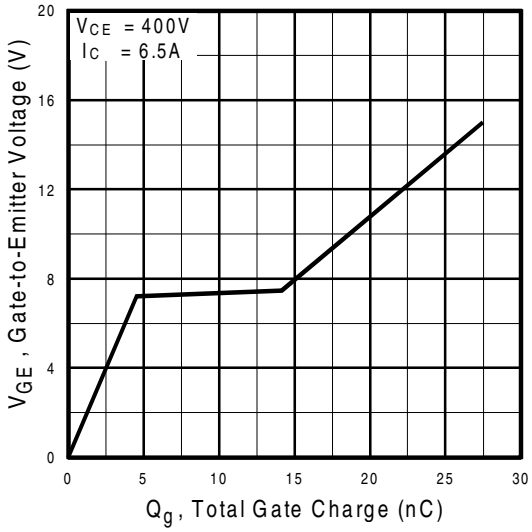


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

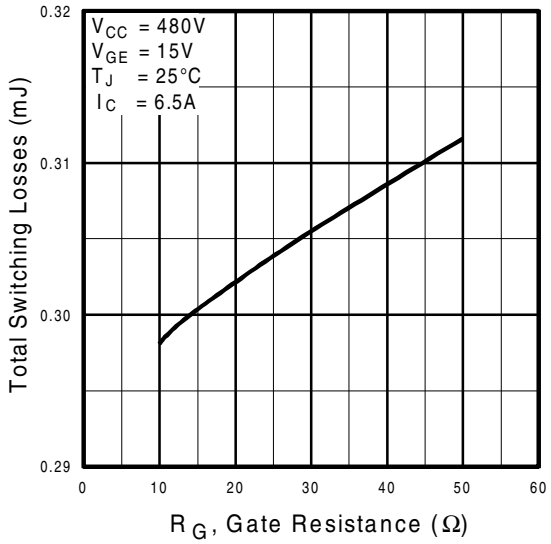


Fig. 9 - Typical Switching Losses vs. Gate Resistance

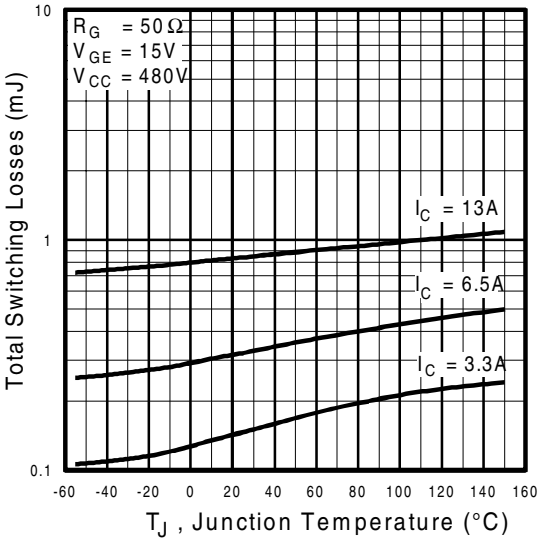


Fig. 10 - Typical Switching Losses vs. Junction Temperature

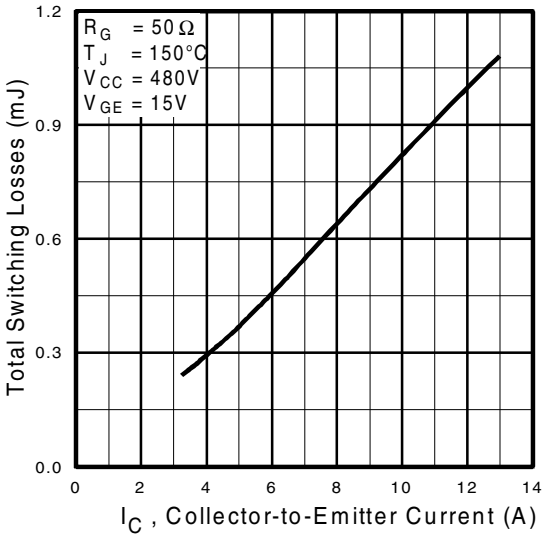


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

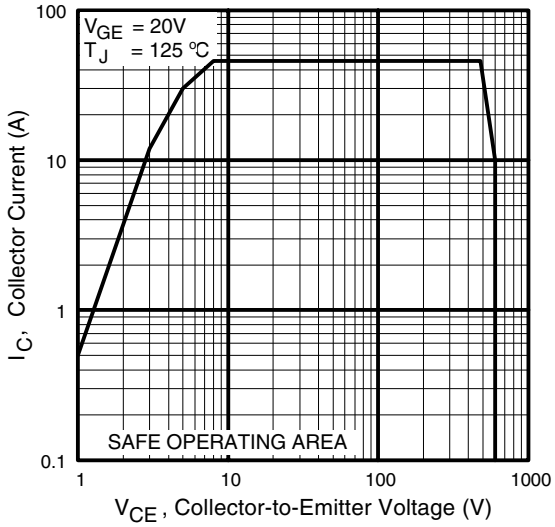


Fig. 12 - Turn-Off SOA

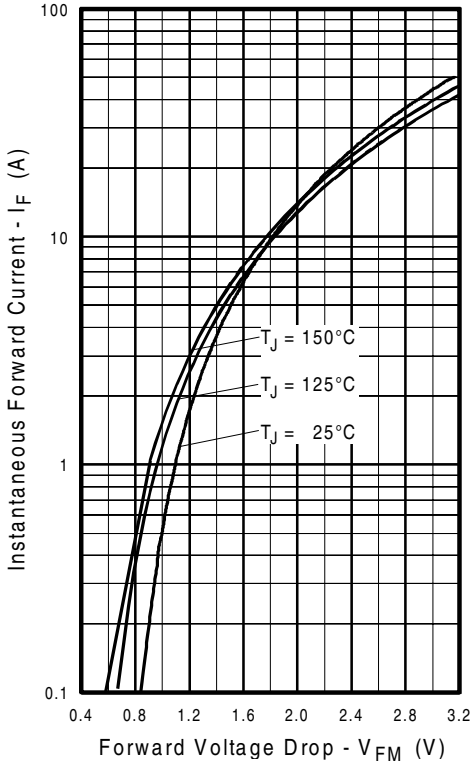


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

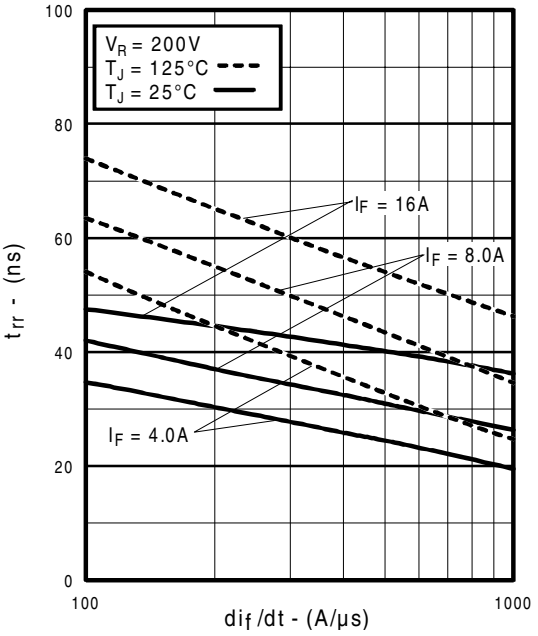


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

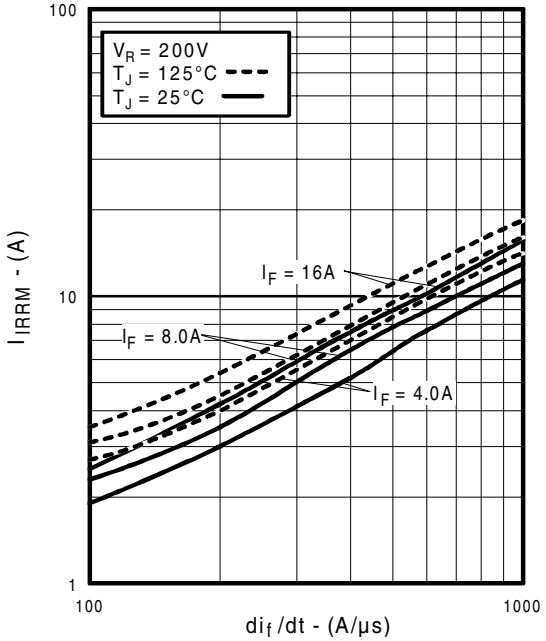


Fig. 15 - Typical Recovery Current vs. di_f/dt

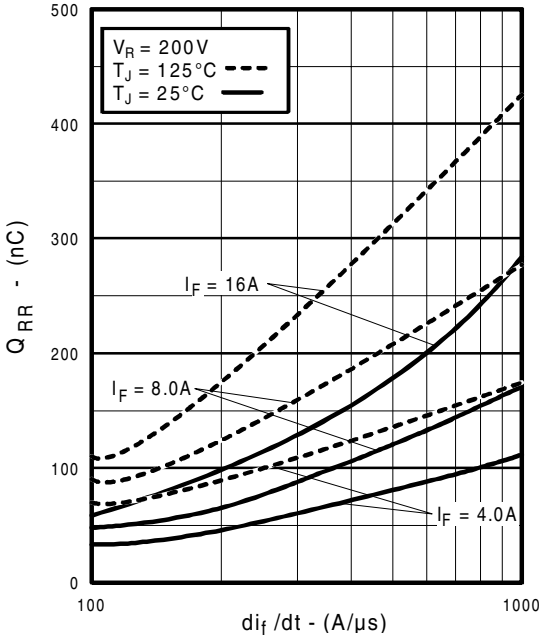


Fig. 16 - Typical Stored Charge vs. di_f/dt

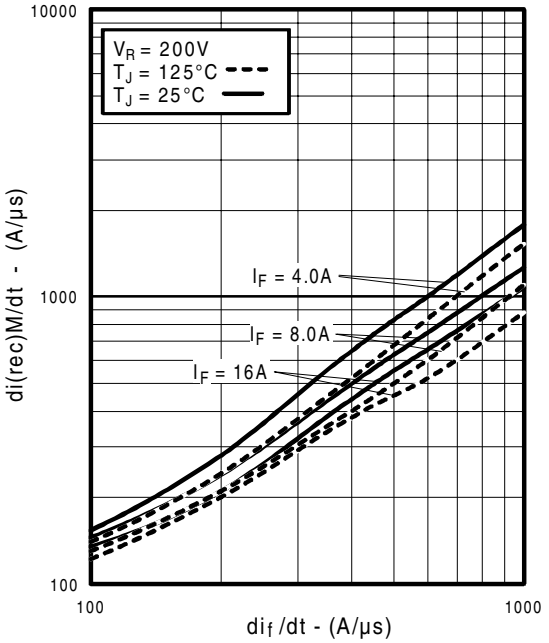


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

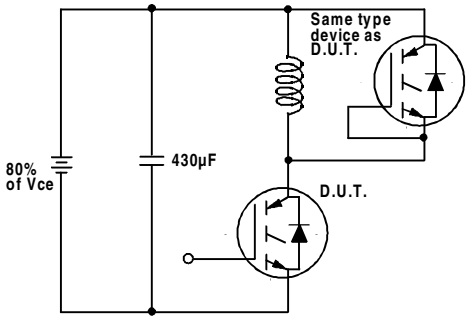


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

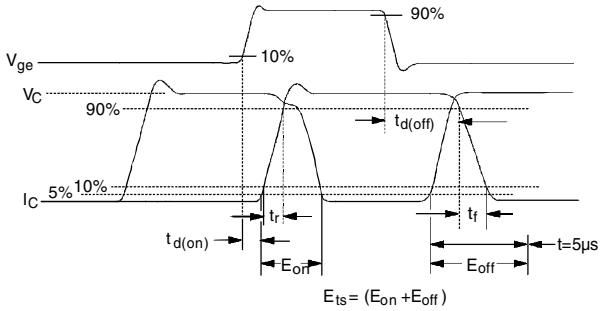


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

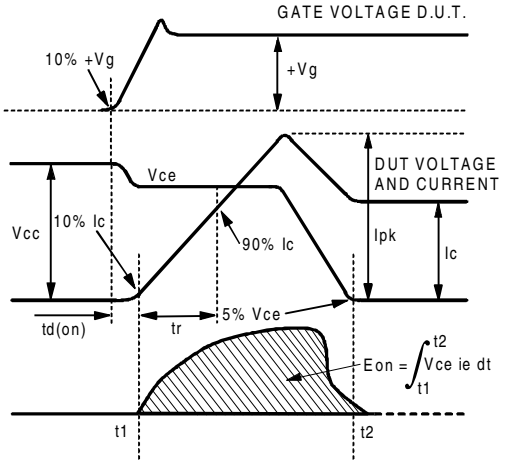


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

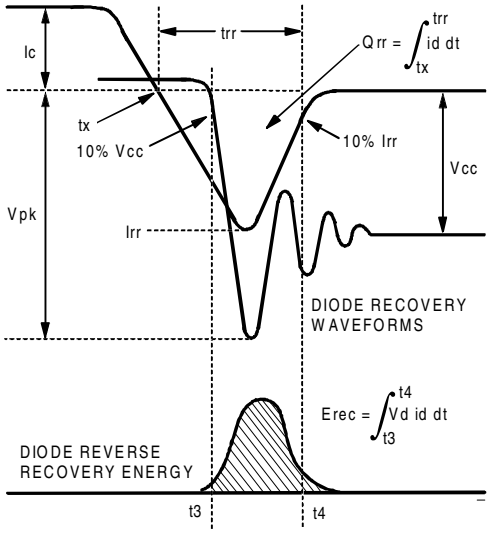


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

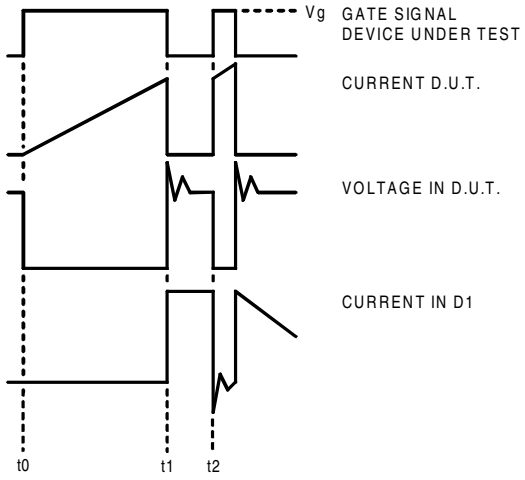


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

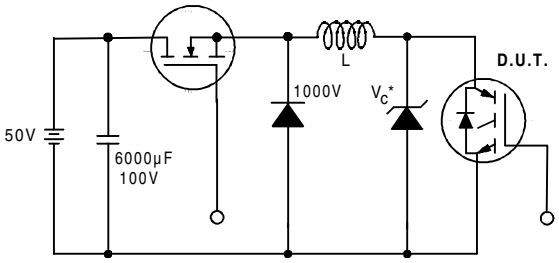


Figure 19. Clamped Inductive Load Test Circuit

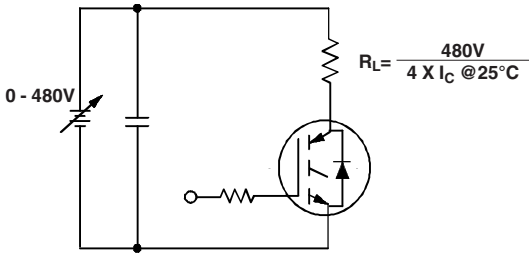


Figure 20. Pulsed Collector Current Test Circuit

Notes:

① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

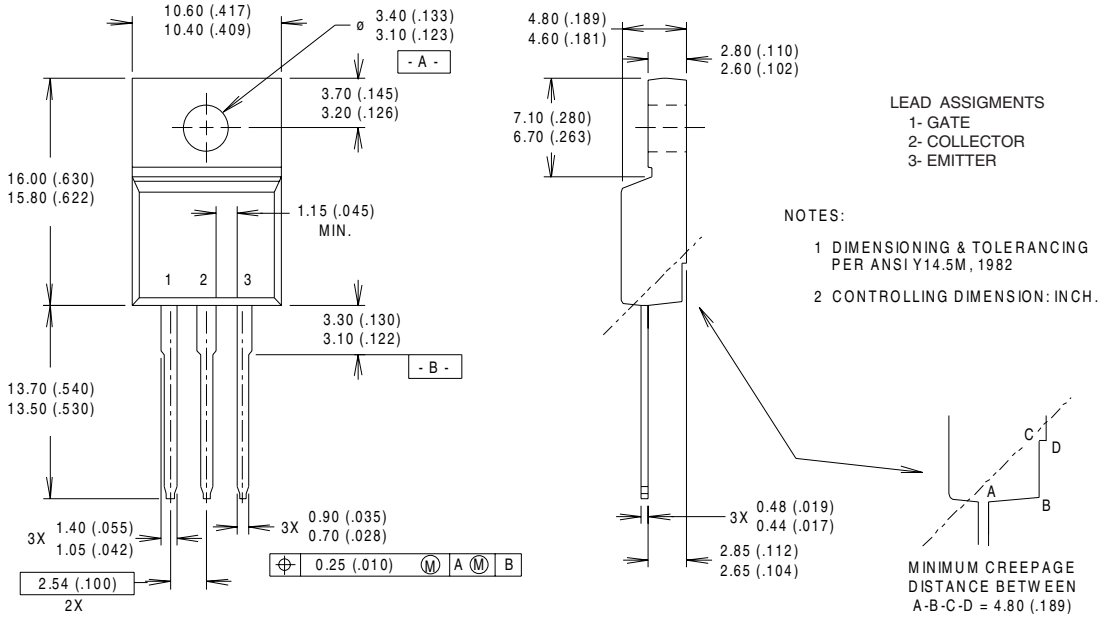
② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 50Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

⑤ t = 60s, f = 60Hz

Case Outline — TO-220 FULLPAK



International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD -91689A

International
IOR Rectifier

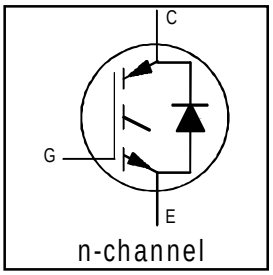
IRG4IBC20KD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
UltraFast IGBT

Features

- High switching speed optimized for up to 25kHz with low $V_{CE(on)}$
- Short Circuit Rating 10µs @ 125°C, V_{GE} = 15V
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than previous generation
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-220 FULLPAK



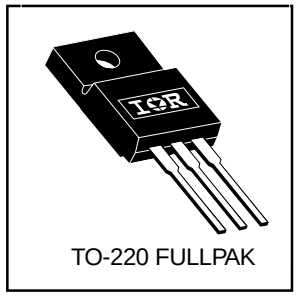
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.27V

@V_{GE} = 15V, I_C = 6.3A

Benefits

- Generation 4 IGBTs offer highest efficiencies available maximizing the power density of the system
- IGBTs optimized for specific application conditions
- HEXFRED™ diodes optimized for performance with IGBTs. Minimized recovery characteristics reduce noise EMI
- Designed to exceed the power handling capability of equivalent industry-standard IGBTs



TO-220 FULLPAK

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	11.5	A
I_C @ T_C = 100°C	Continuous Collector Current	6.3	
I_{CM}	Pulsed Collector Current ①	23	
I_{LM}	Clamped Inductive Load Current ②	24	
I_F @ T_C = 100°C	Diode Continuous Forward Current	6.3	
I_{FM}	Diode Maximum Forward Current	24	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{ISOL}	RMS Isolation Voltage, Terminal to Case, t = 1 min	2500	V
V_{GE}	Gate-to-Emitter Voltage	± 20	
P_D @ T_C = 25°C	Maximum Power Dissipation	34	W
P_D @ T_C = 100°C	Maximum Power Dissipation	14	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	3.7	°C/W
$R_{\theta CS}$	Junction-to-Case - Diode	—	5.5	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	65	
Wt	Weight	2.0 (0.07)	—	g (oz)

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.49	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.27	2.8	V	I_C = 9.0A V_{GE} = 15V
		—	3.01	—		I_C = 16A See Fig. 2, 5
		—	2.43	—		I_C = 9.0A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	2.9	4.3	—	S	V_{CE} = 100V, I_C = 9.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 8.0A See Fig. 13
		—	1.3	1.6		I_C = 8.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	34	51	nC	I_C = 9.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	4.9	7.4		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	14	21		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	54	—	ns	
t_r	Rise Time	—	34	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	180	270		I_C = 9.0A, V_{CC} = 480V
t_f	Fall Time	—	72	110		V_{GE} = 15V, R_G = 50Ω
E_{on}	Turn-On Switching Loss	—	0.34	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.30	—		and diode reverse recovery
E_{ts}	Total Switching Loss	—	0.64	0.96		See Fig. 9,10,14
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 360V, T_J = 125°C
						V_{GE} = 15V, R_G = 50Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	51	—	ns	T_J = 150°C, See Fig. 10,11,14
t_r	Rise Time	—	37	—		I_C = 9.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	220	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	160	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.85	—	mJ	and diode reverse recovery
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	450	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	61	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	14	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	37	55	ns	T_J = 25°C See Fig.
		—	55	90		T_J = 125°C 14 I_F = 8.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	5.0	A	T_J = 25°C See Fig.
		—	4.5	8.0		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	65	138	nC	T_J = 25°C See Fig.
		—	124	360		T_J = 125°C 16 di/dt = 200Aµs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	240	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	210	—		T_J = 125°C 17

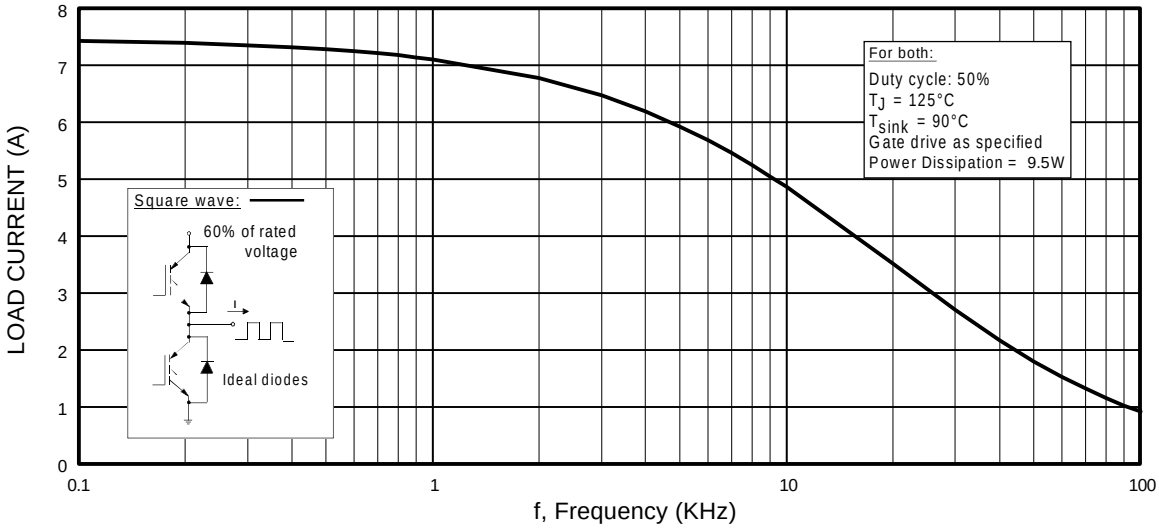


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

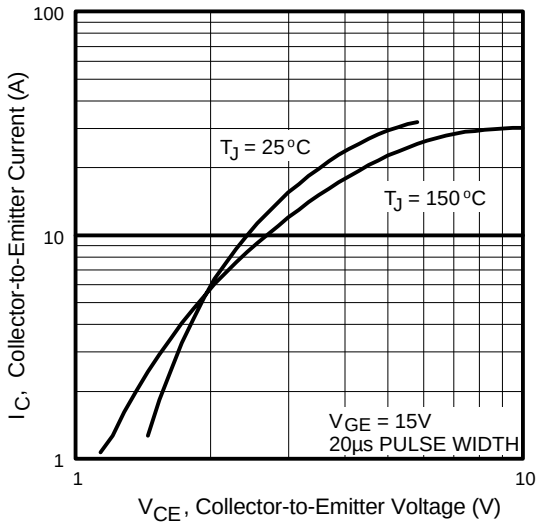


Fig. 2 - Typical Output Characteristics

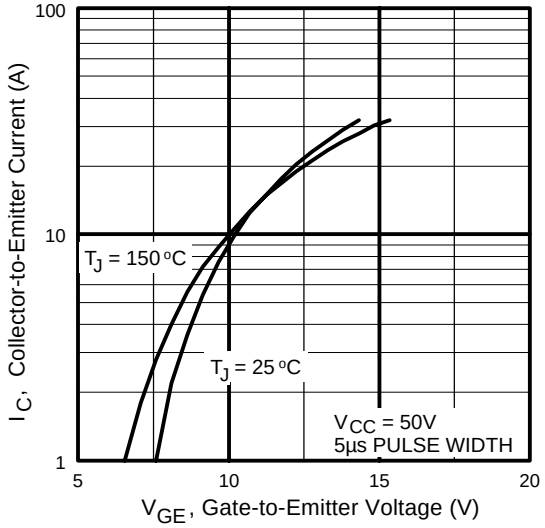


Fig. 3 - Typical Transfer Characteristics

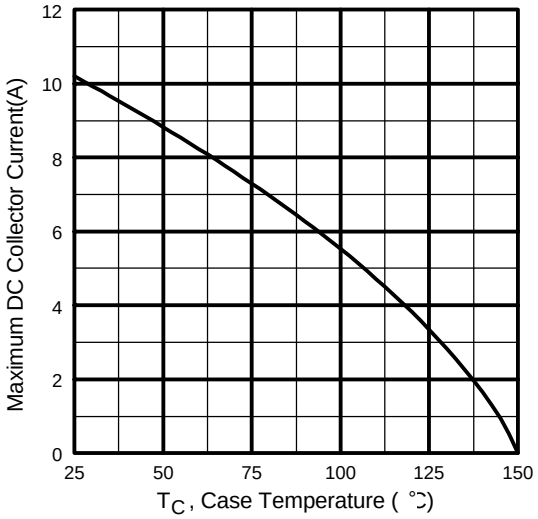


Fig. 4 - Maximum Collector Current vs. Case Temperature

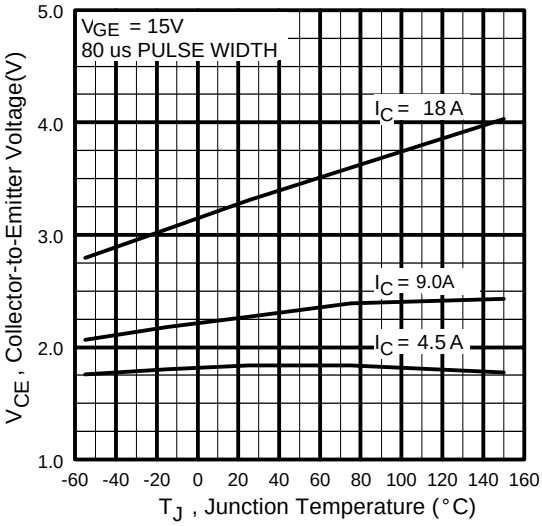


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

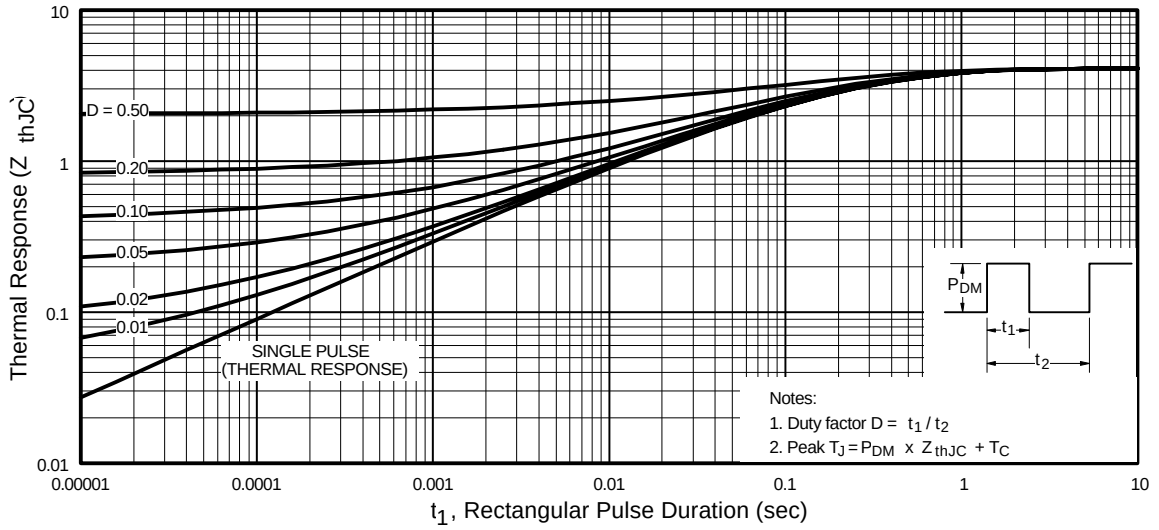


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

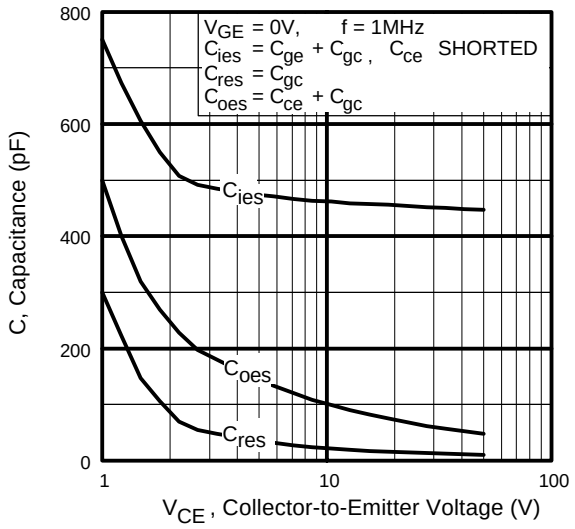


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

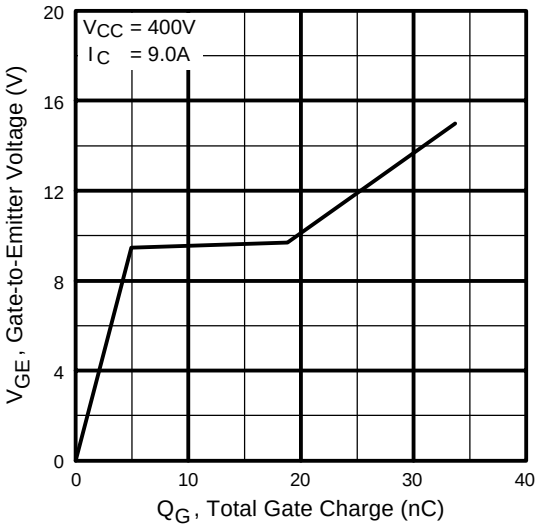


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

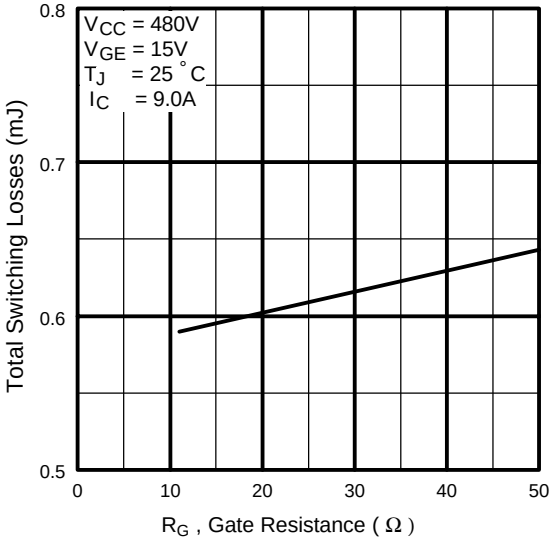


Fig. 9 - Typical Switching Losses vs. Gate Resistance

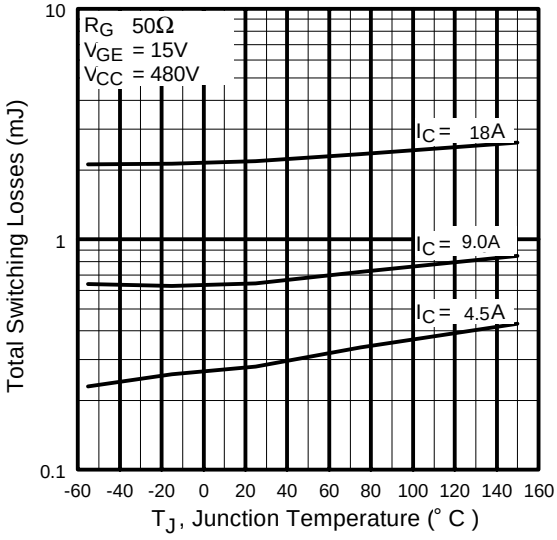


Fig. 10 - Typical Switching Losses vs. Junction Temperature

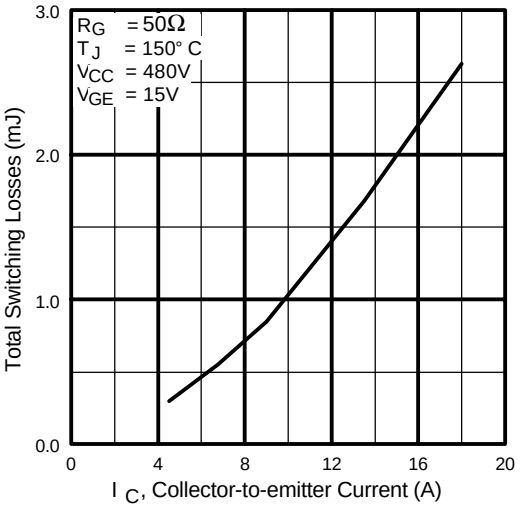


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

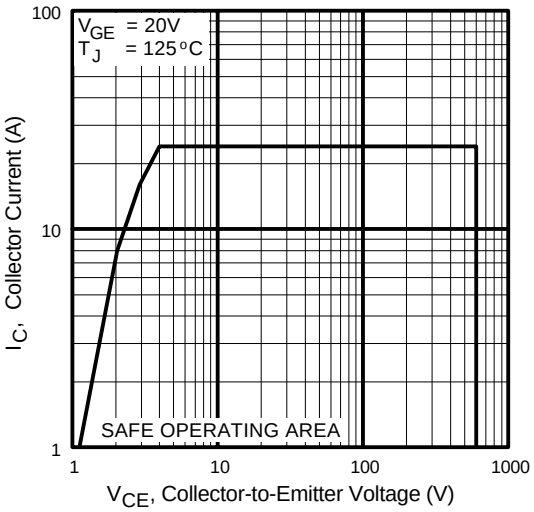


Fig. 12 - Turn-Off SOA

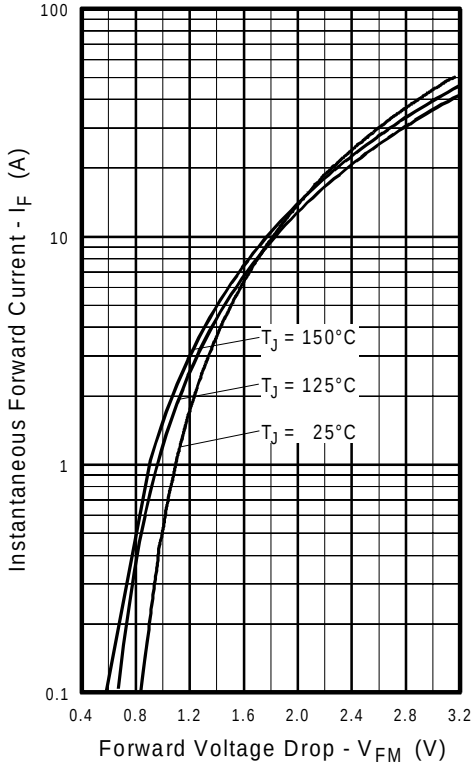


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

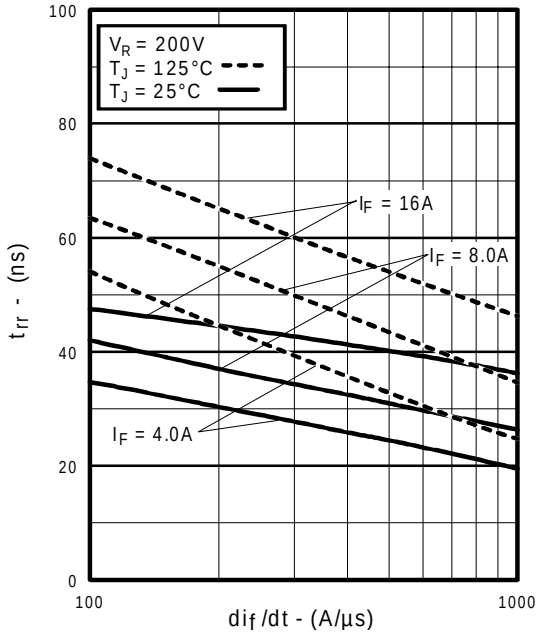


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

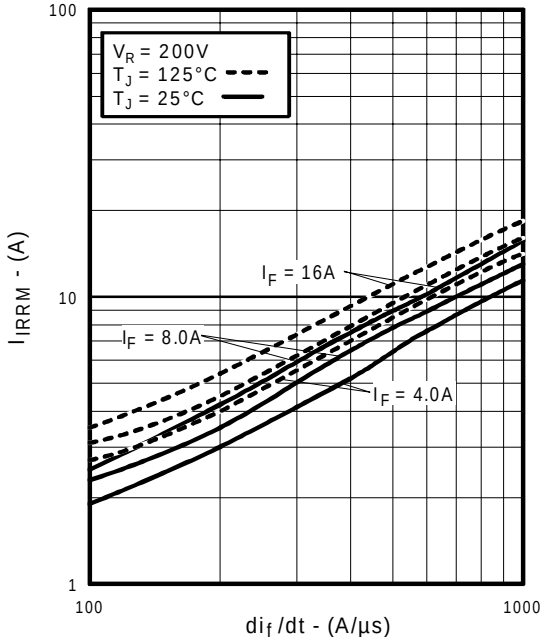


Fig. 15 - Typical Recovery Current vs. di_f/dt

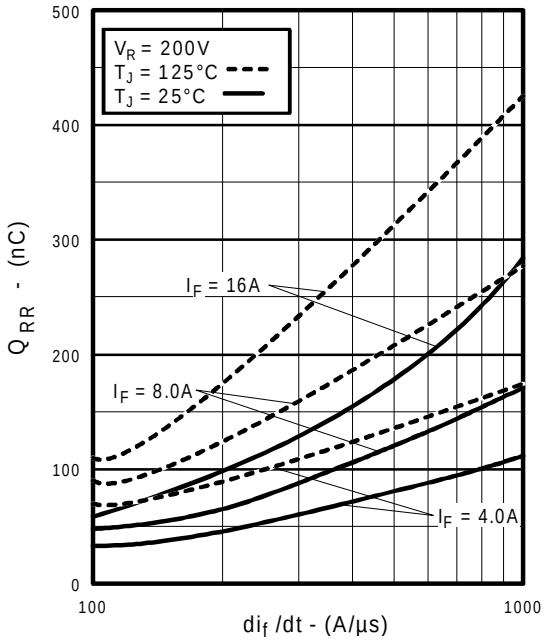


Fig. 16 - Typical Stored Charge vs. di_f/dt

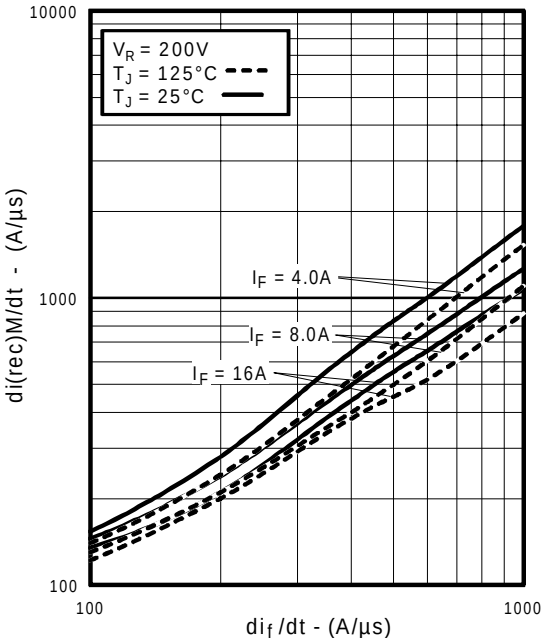


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

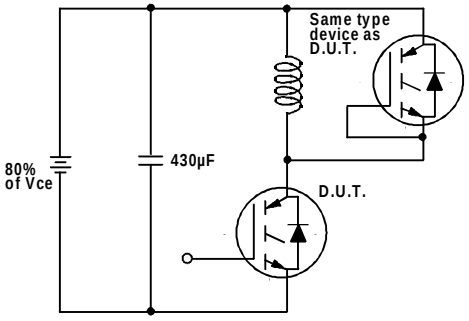


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

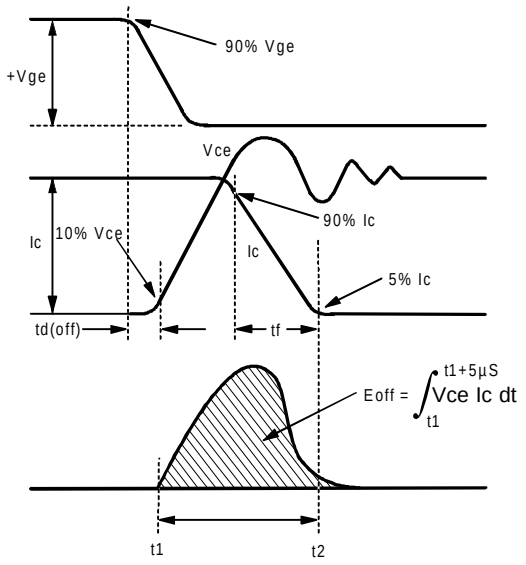


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

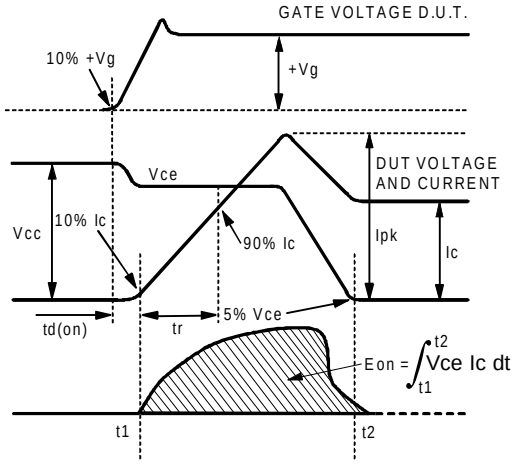


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

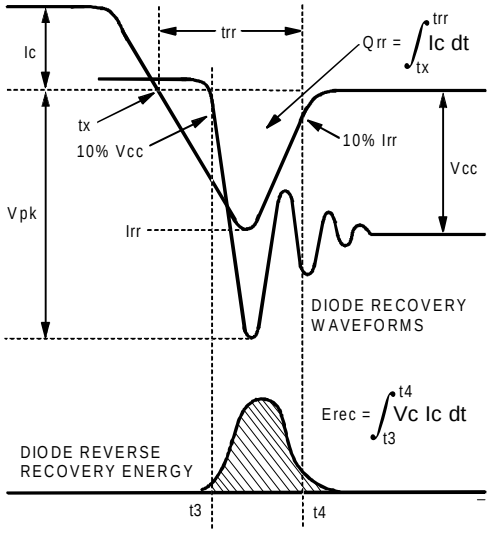


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

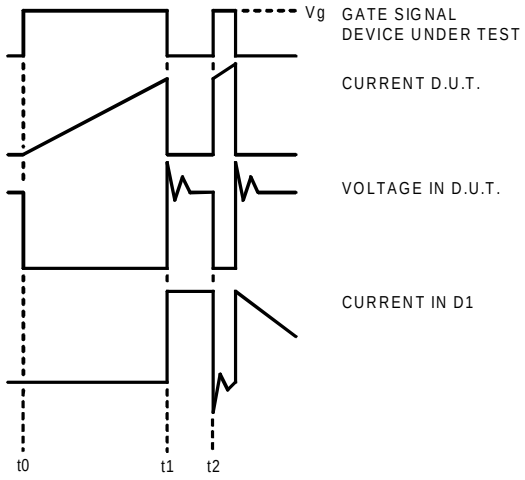


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

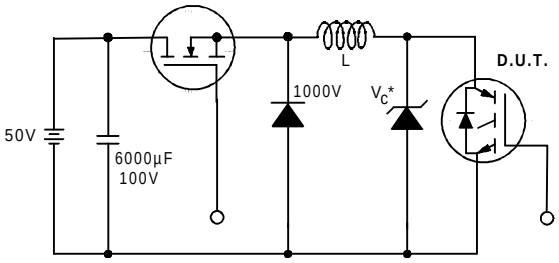


Figure 19. Clamped Inductive Load Test Circuit

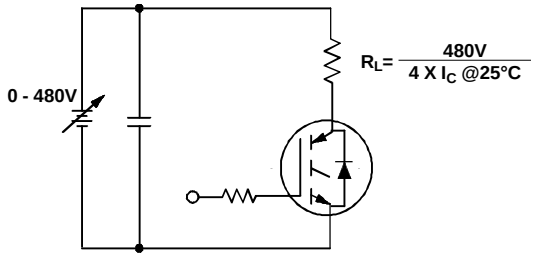


Figure 20. Pulsed Collector Current Test Circuit

Notes:

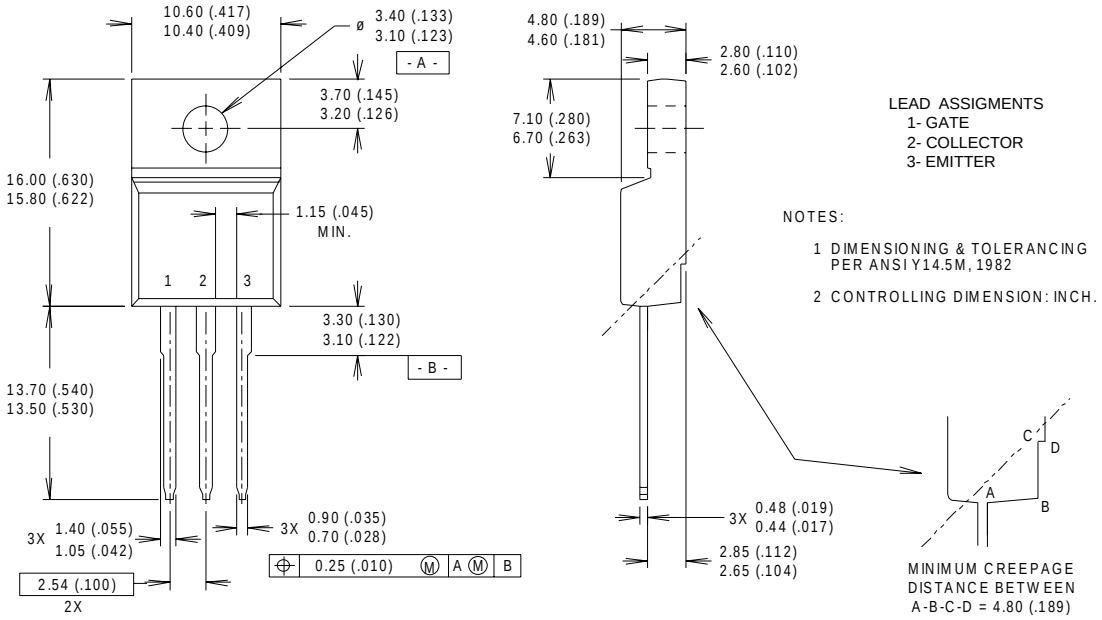
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 50Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-220 FULLPAK



International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 10/00

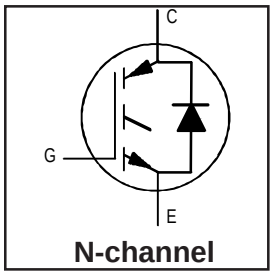
PD- 94077

International
IOR Rectifier

IRG4BC20UD-S

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

UltraFast CoPack IGBT



N-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.85V

@V_{GE} = 15V, I_C = 6.5A

Features

- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard D²Pak package

Benefits

- Generation 4 IGBTs offers highest efficiencies available
- Optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBTs . Minimized recovery characteristics require less/no snubbing
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs



D²Pak

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	13	A
I_C @ T_C = 100°C	Continuous Collector Current	6.5	
I_{CM}	Pulsed Collector Current ①	52	
I_{LM}	Clamped Inductive Load Current ②	52	
I_F @ T_C = 100°C	Diode Continuous Forward Current	7.0	
I_{FM}	Diode Maximum Forward Current	52	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	1.44	—	g (oz)

1/12/01

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.69	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.85	2.1	V	I_C = 6.5A V_{GE} = 15V
		—	2.27	—		I_C = 13A See Fig. 2, 5
		—	1.87	—		I_C = 6.5A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	1.4	4.3	—	S	V_{CE} = 100V, I_C = 6.5A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1700		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 8.0A See Fig. 13
		—	1.3	1.6		I_C = 8.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	27	41		I_C = 6.5A
Qge	Gate - Emitter Charge (turn-on)	—	4.5	6.8	nC	V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	10	16		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	39	—		T_J = 25°C
t_r	Rise Time	—	15	—	ns	I_C = 6.5A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	93	140		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	110	170		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	0.16	—		diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	0.13	—	mJ	See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	—	0.29	0.3		
$t_{d(on)}$	Turn-On Delay Time	—	38	—		T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	—	17	—	ns	I_C = 6.5A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	100	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	220	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	0.49	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	530	—		V_{GE} = 0V
C_{oes}	Output Capacitance	—	39	—	pF	V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	7.4	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	37	55	ns	T_J = 25°C See Fig.
		—	55	90		T_J = 125°C 14 I_F = 8.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	5.0	A	T_J = 25°C See Fig.
		—	4.5	8.0		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	65	138	nC	T_J = 25°C See Fig.
		—	124	360		T_J = 125°C 16 di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	240	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	210	—		T_J = 125°C 17

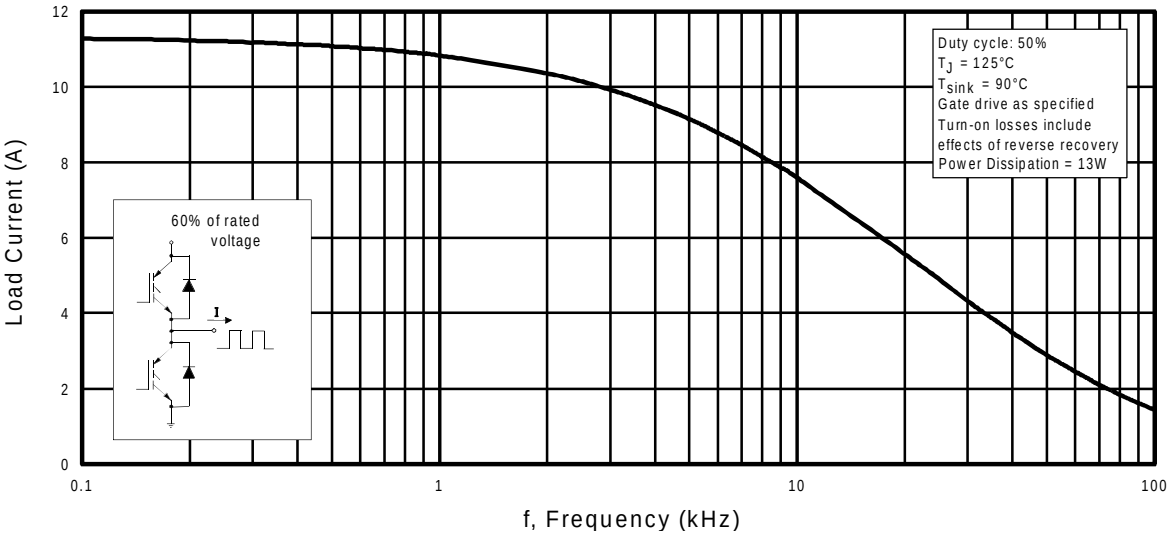


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

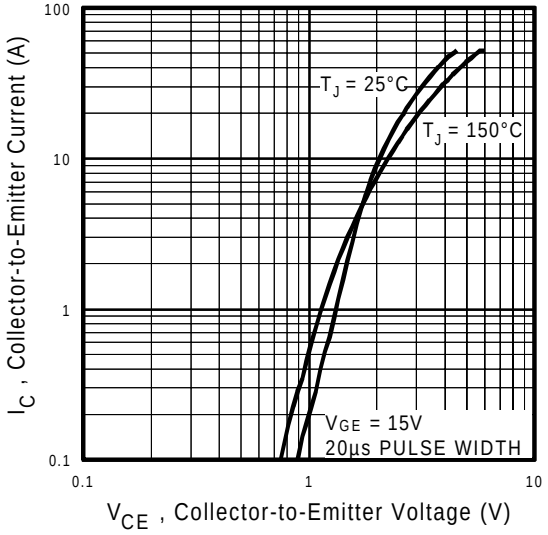


Fig. 2 - Typical Output Characteristics

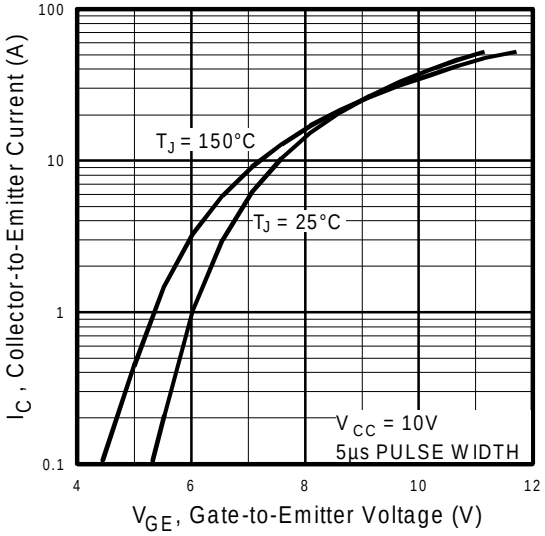


Fig. 3 - Typical Transfer Characteristics

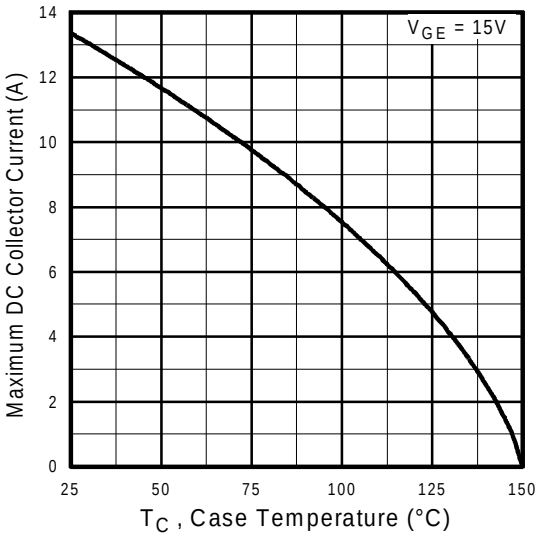


Fig. 4 - Maximum Collector Current vs. Case Temperature

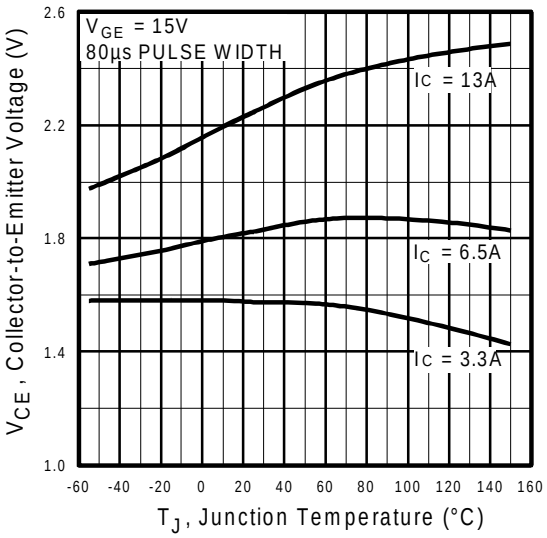


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

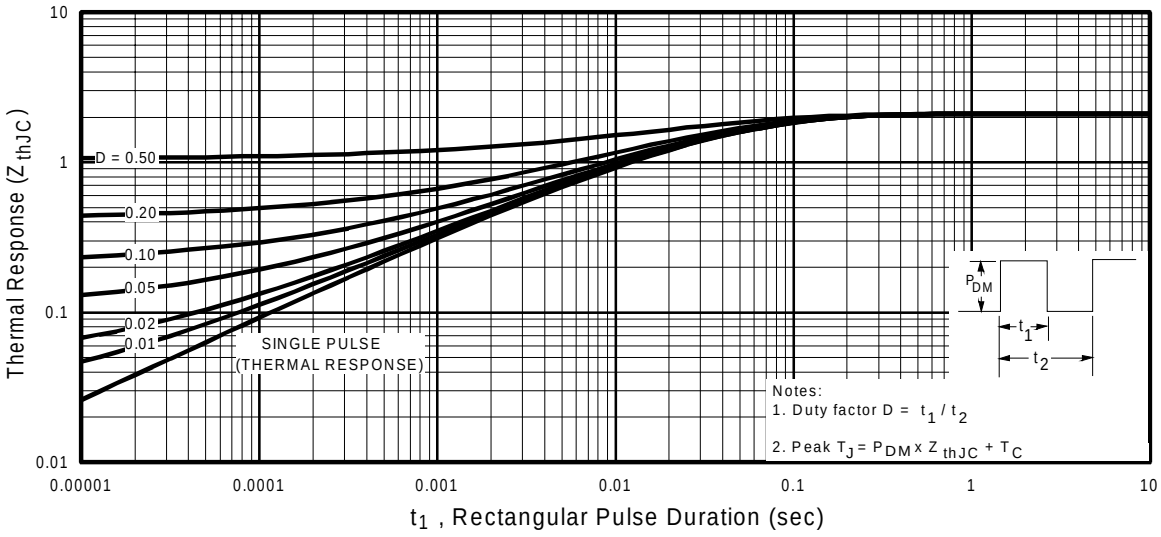


Fig. 6 - Maximum IGBT Effective Transient Thermal Impedance, Junction-to-Case

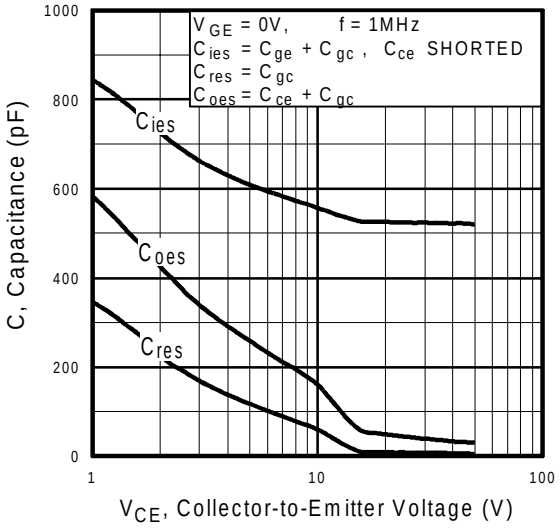


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

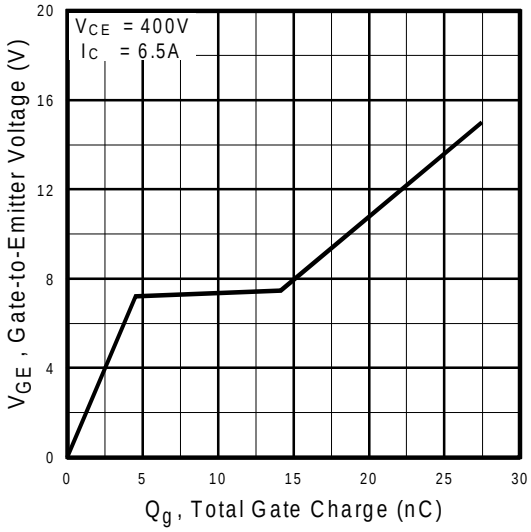


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

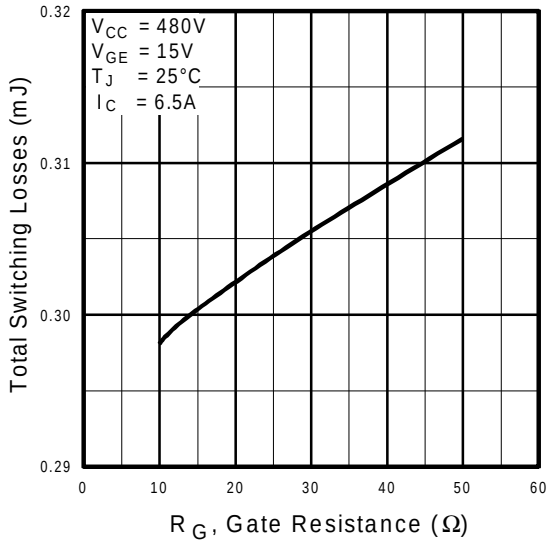


Fig. 9 - Typical Switching Losses vs. Gate Resistance

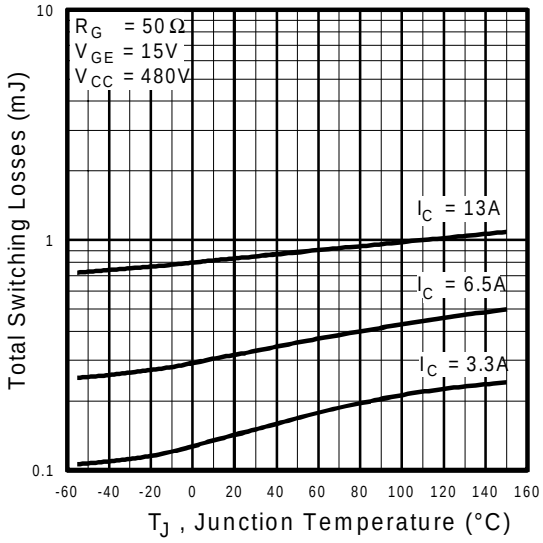


Fig. 10 - Typical Switching Losses vs. Junction Temperature

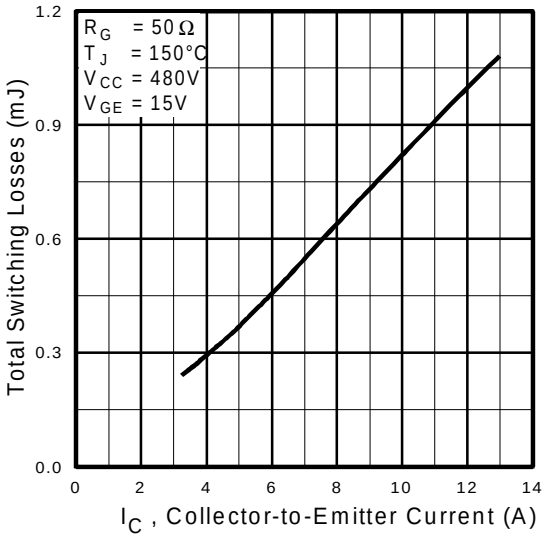


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

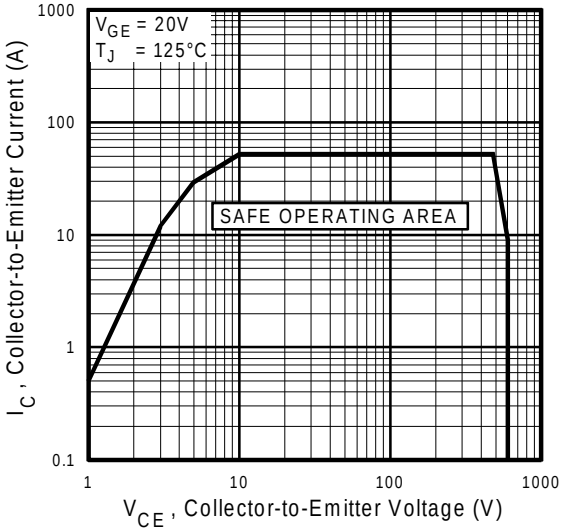


Fig. 12 - Turn-Off SOA

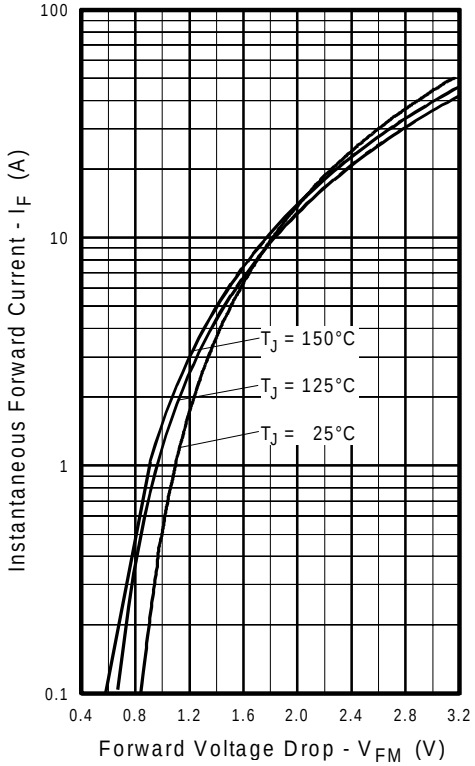


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

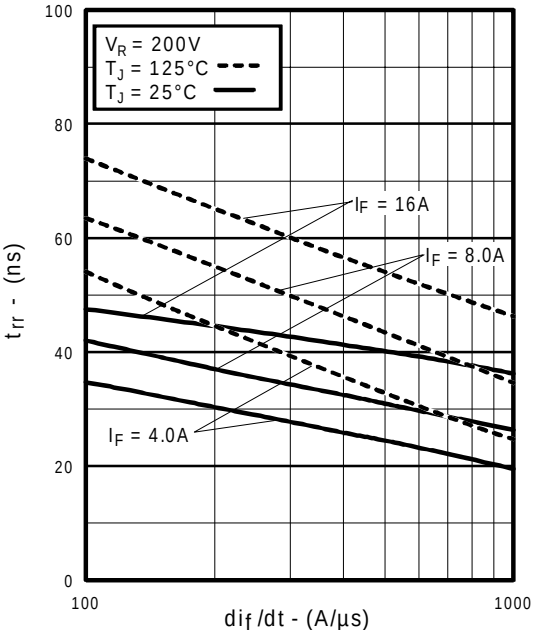


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

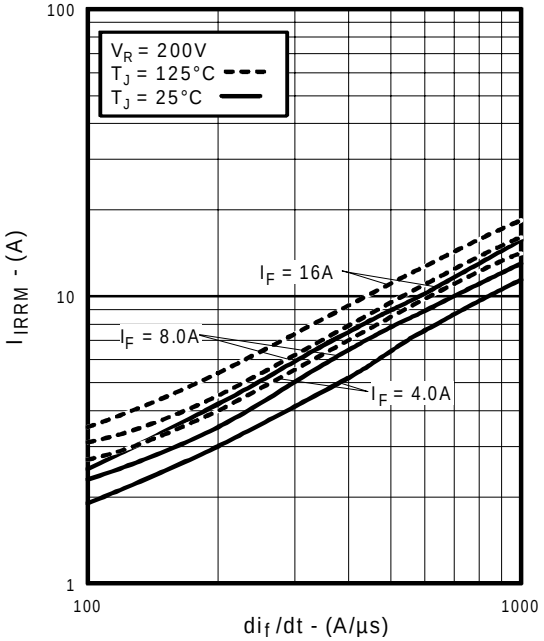


Fig. 15 - Typical Recovery Current vs. di_f/dt

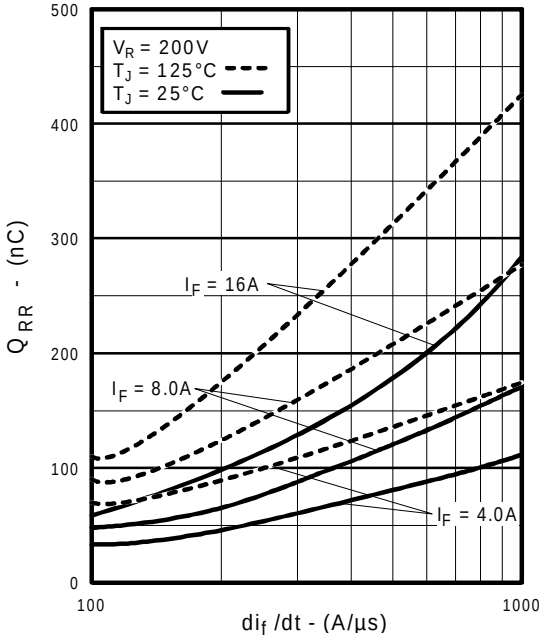


Fig. 16 - Typical Stored Charge vs. di_f/dt

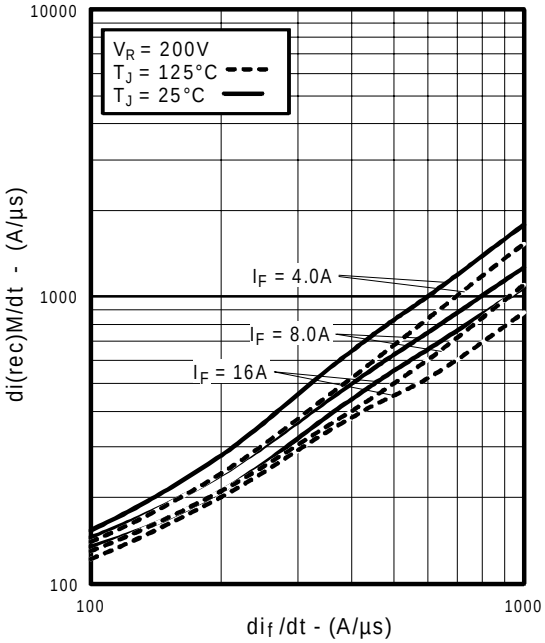


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

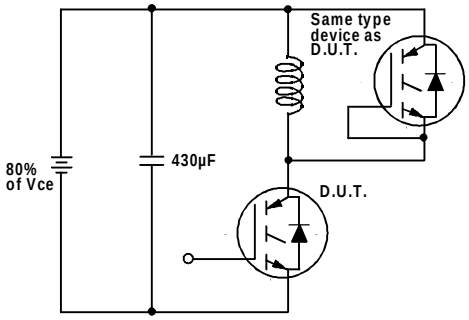


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

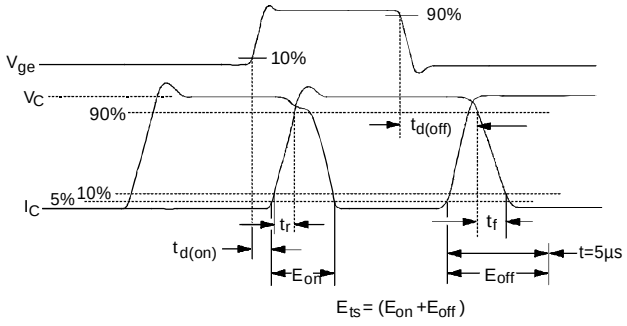


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

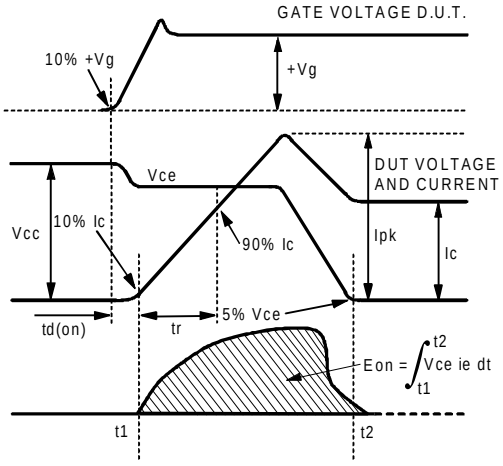


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

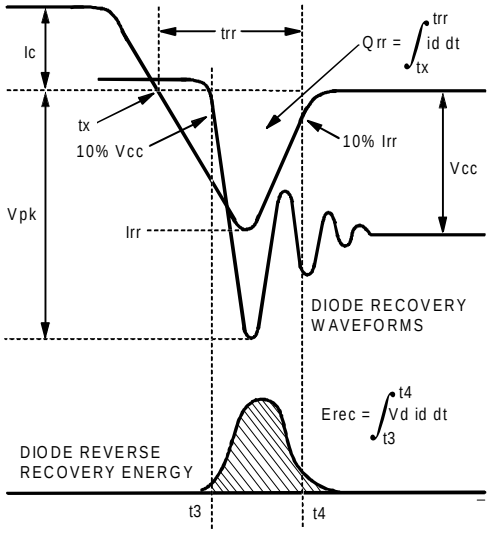


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

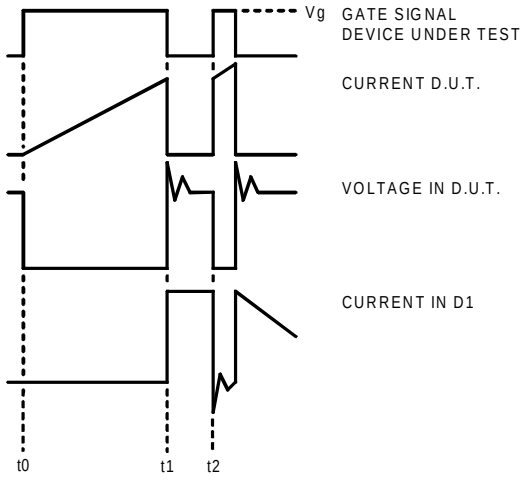


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

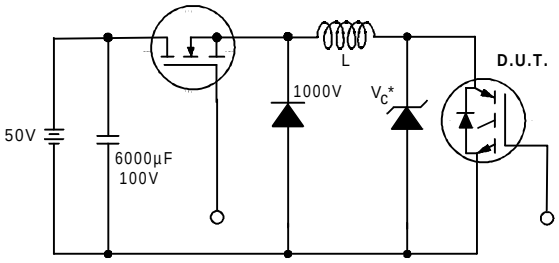


Figure 19. Clamped Inductive Load Test Circuit

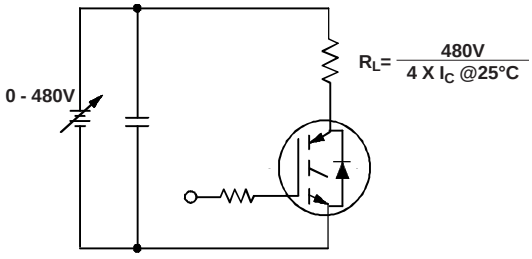
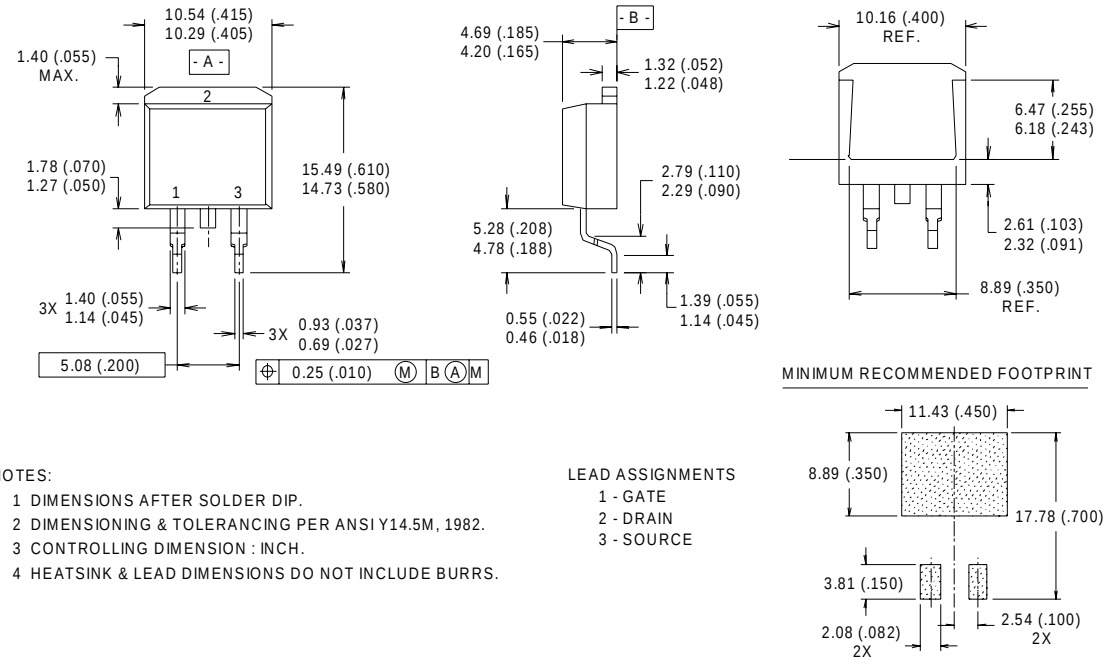


Figure 20. Pulsed Collector Current Test Circuit

D²Pak Package Outline



NOTES:

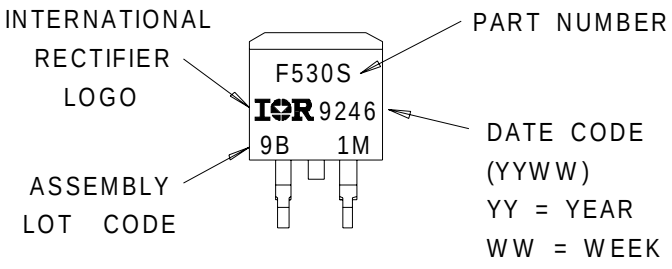
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

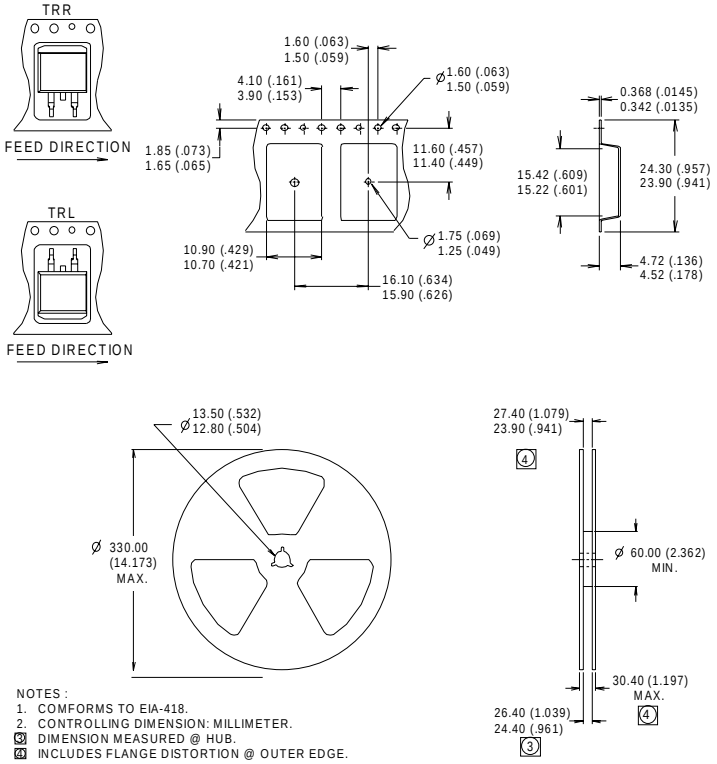
1 - GATE
2 - DRAIN
3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT

D²Pak Part Marking Information



D²Pak Tape & Reel Information



NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Notes:

① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (Figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 50Ω (Figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.1/01

PD - 91448D

International
IOR Rectifier

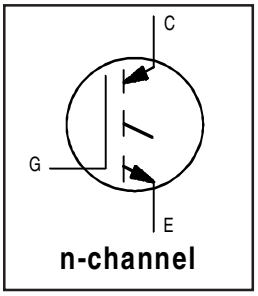
IRG4BC20U

INSULATED GATE BIPOLAR TRANSISTOR

UltraFast Speed IGBT

Features

- UltraFast: optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-220AB package



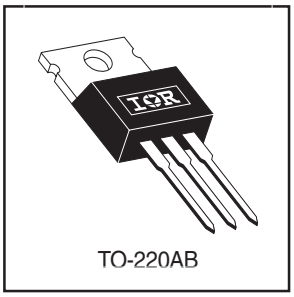
$V_{CES} = 600V$

$V_{CE(on)\ typ.} = 1.85V$

$@V_{GE} = 15V, I_C = 6.5A$

Benefits

- Generation 4 IGBTs offer highest efficiency available
- IGBTs optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ $T_C = 25°C$	Continuous Collector Current	13	A
I_C @ $T_C = 100°C$	Continuous Collector Current	6.5	
I_{CM}	Pulsed Collector Current ①	52	
I_{LM}	Clamped Inductive Load Current ②	52	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	5.0	mJ
P_D @ $T_C = 25°C$	Maximum Power Dissipation	60	W
P_D @ $T_C = 100°C$	Maximum Power Dissipation	24	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	80	
Wt	Weight	2.0 (0.07)	—	g (oz)

4/17/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.69	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.85	2.1	V	I_C = 6.5A V_{GE} = 15V
		—	2.27	—		I_C = 13A See Fig.2, 5
		—	1.87	—		I_C = 6.5A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	1.4	4.3	—	S	V_{CE} = 100V, I_C = 6.5A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	27	41	nC	I_C = 6.5A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	4.5	6.8		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	10	16		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	
t_r	Rise Time	—	13	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	86	130		I_C = 6.5A, V_{CC} = 480V
t_f	Fall Time	—	120	180		V_{GE} = 15V, R_G = 50Ω
E_{on}	Turn-On Switching Loss	—	0.10	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.12	—		See Fig. 10, 11, 13, 14
E_{ts}	Total Switching Loss	—	0.22	0.4		
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	T_J = 150°C,
t_r	Rise Time	—	14	—		I_C = 6.5A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	190	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	140	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.42	—	mJ	See Fig. 13, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	530	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	39	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	7.4	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 50Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

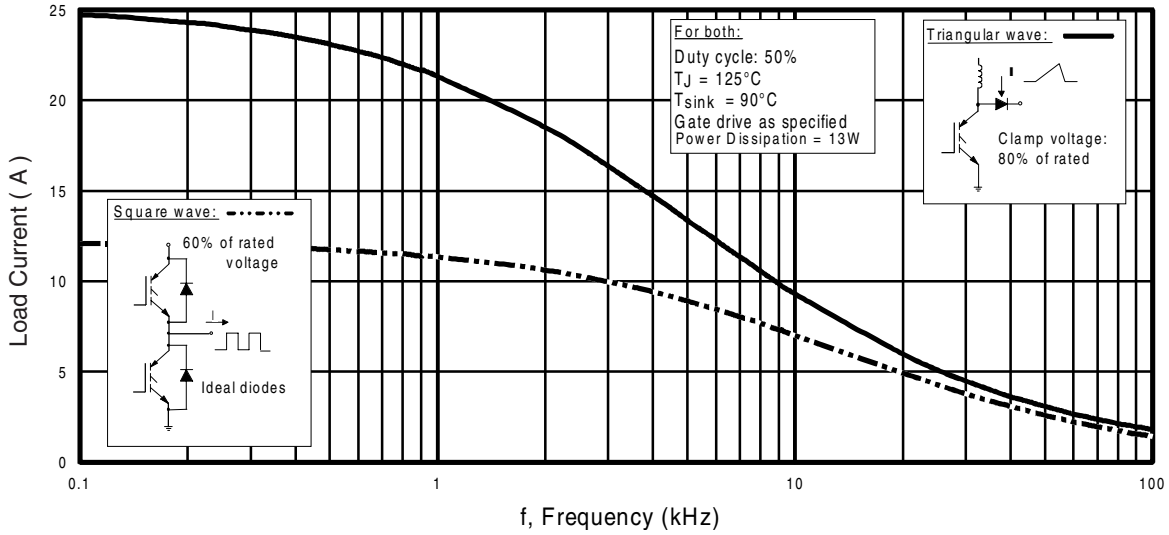


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

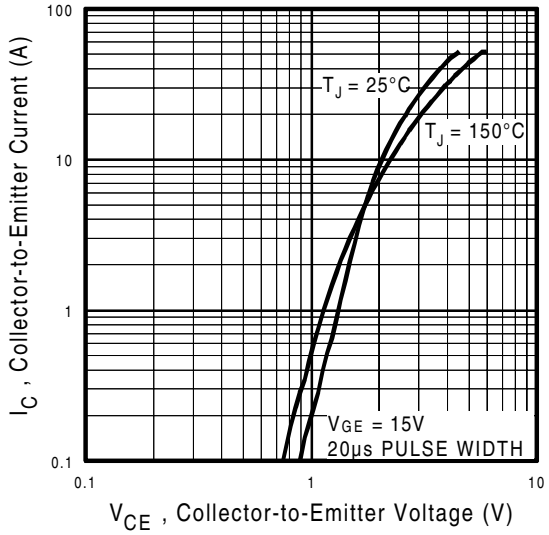


Fig. 2 - Typical Output Characteristics

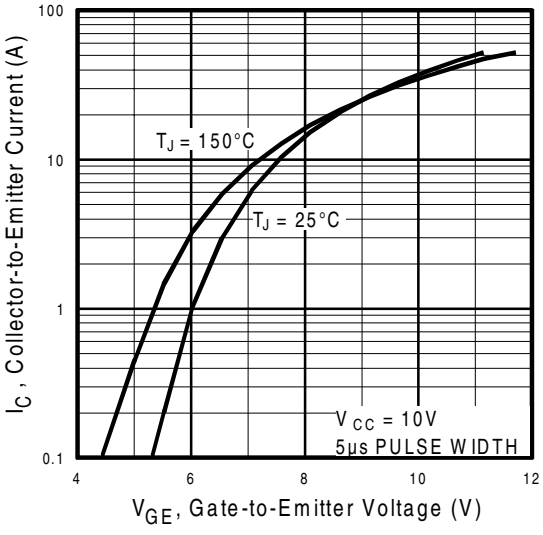


Fig. 3 - Typical Transfer Characteristics

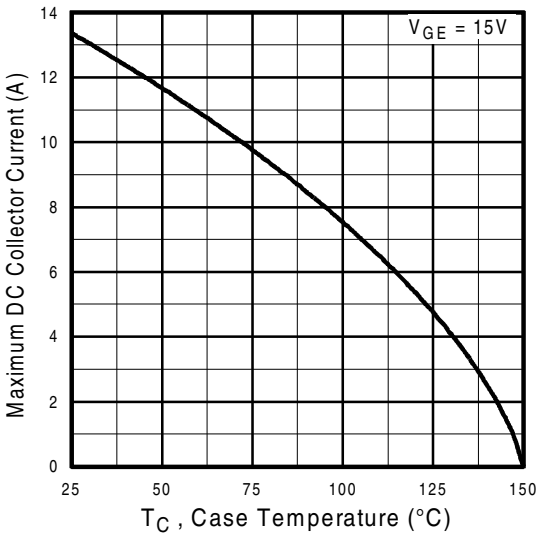


Fig. 4 - Maximum Collector Current vs. Case Temperature

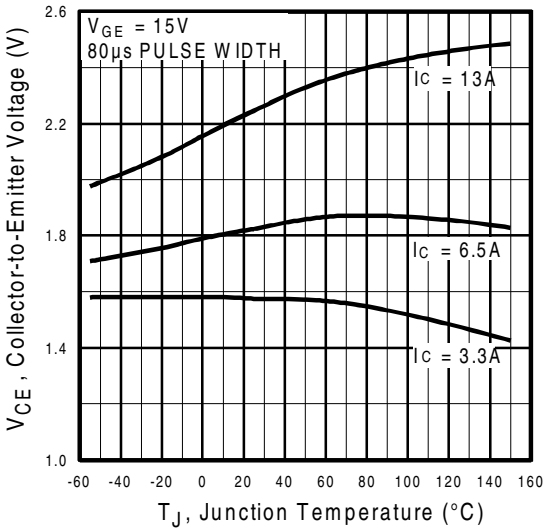


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

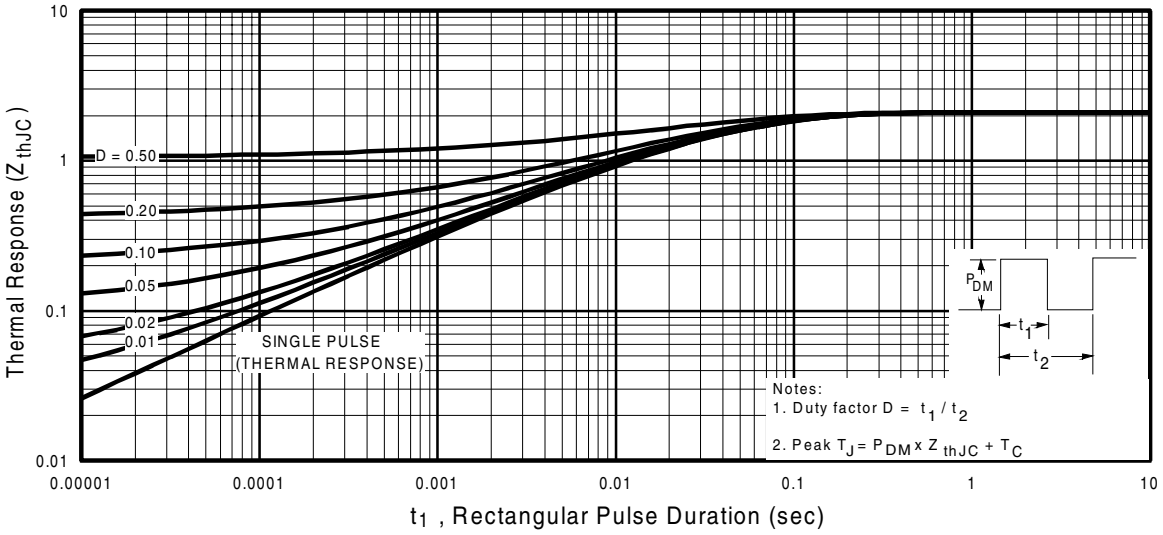


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

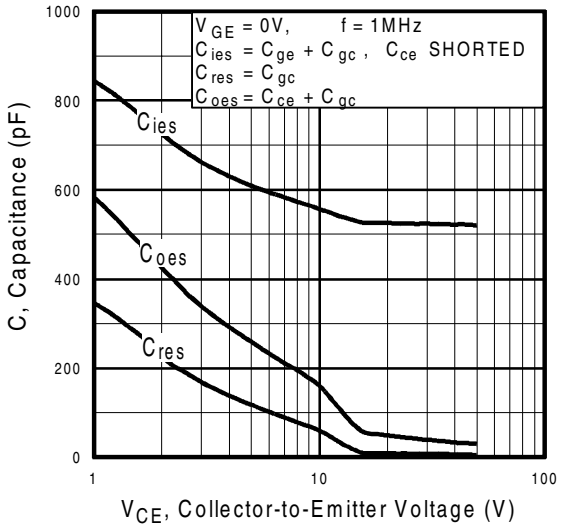


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

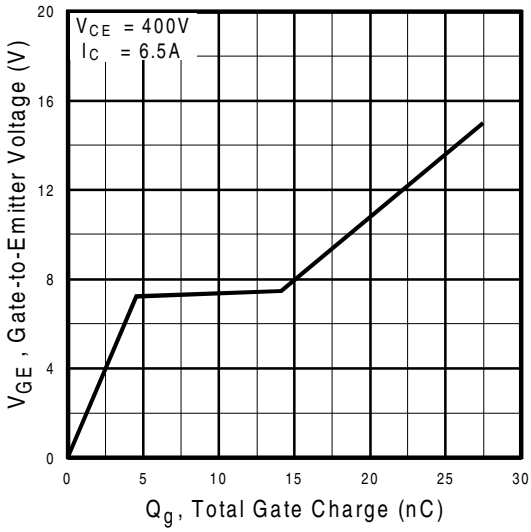


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

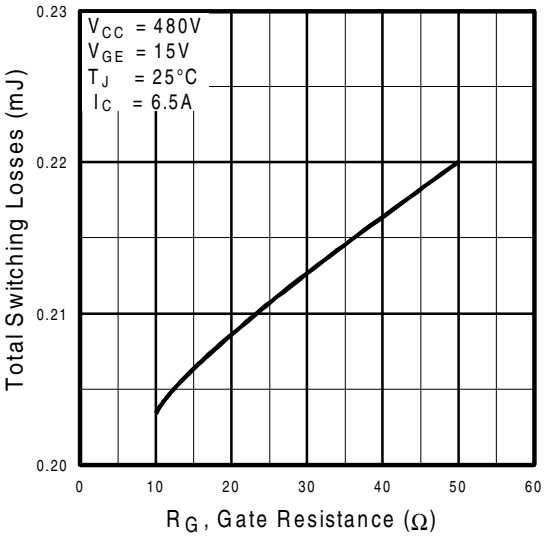


Fig. 9 - Typical Switching Losses vs. Gate Resistance

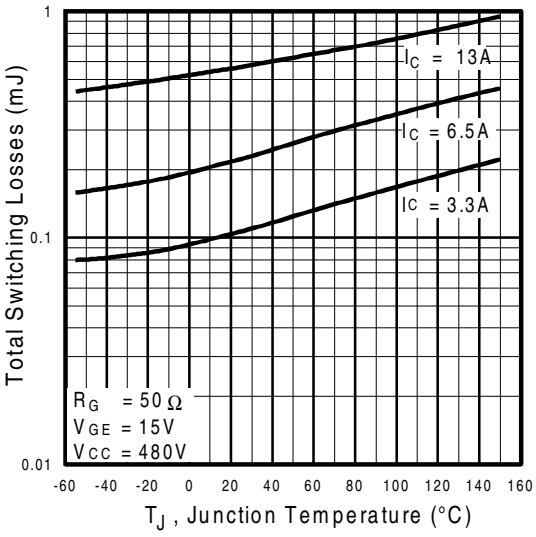


Fig. 10 - Typical Switching Losses vs. Junction Temperature

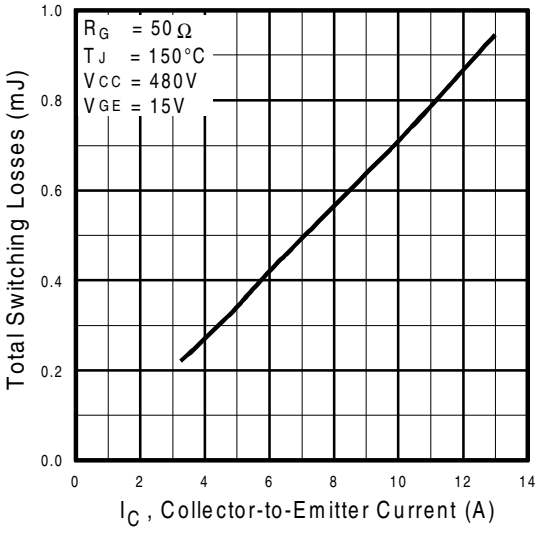


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

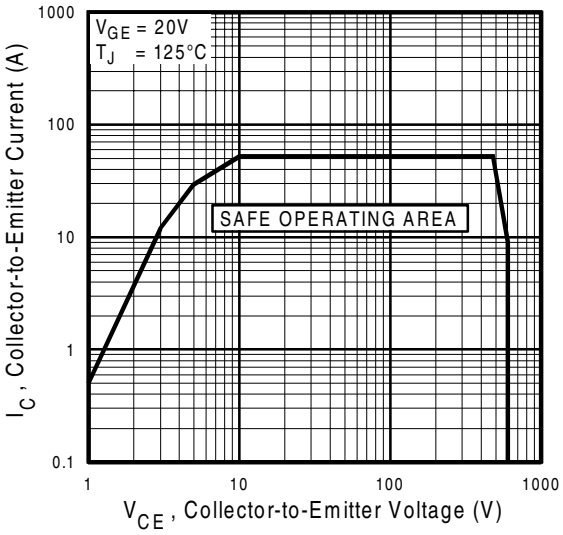


Fig. 12 - Turn-Off SOA

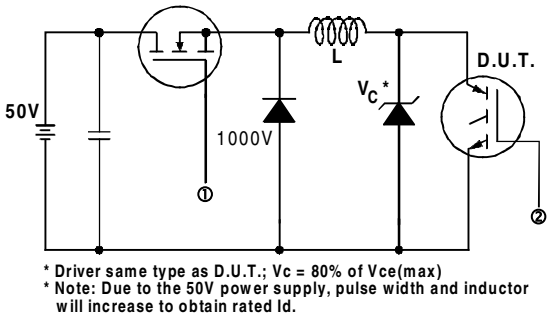


Fig. 13a - Clamped Inductive Load Test Circuit

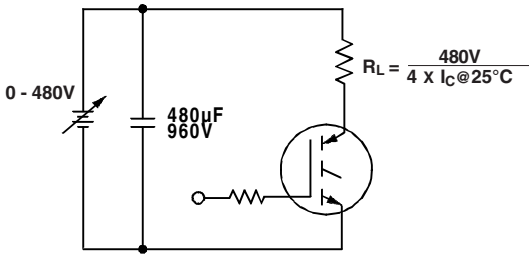


Fig. 13b - Pulsed Collector Current Test Circuit

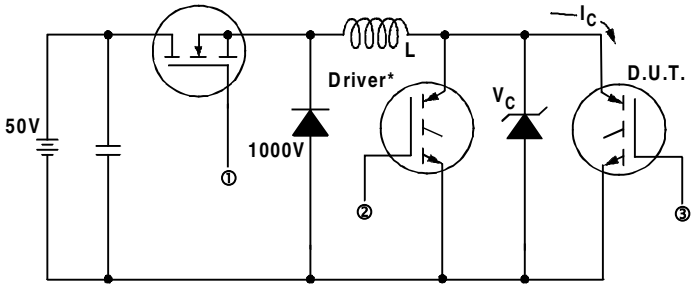


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

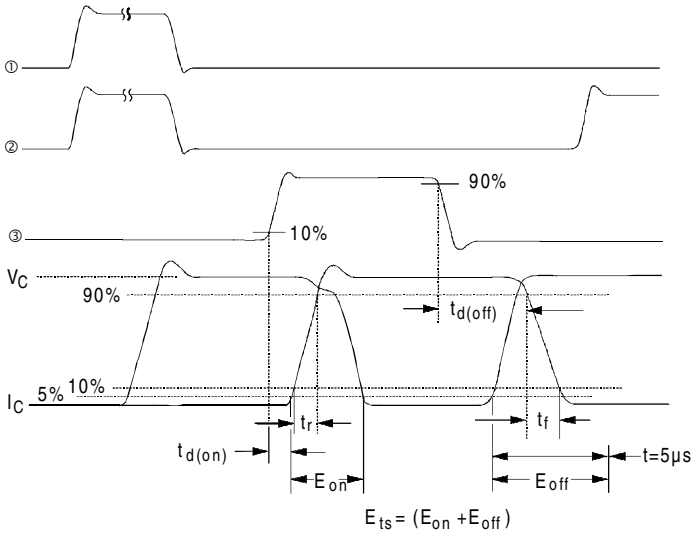
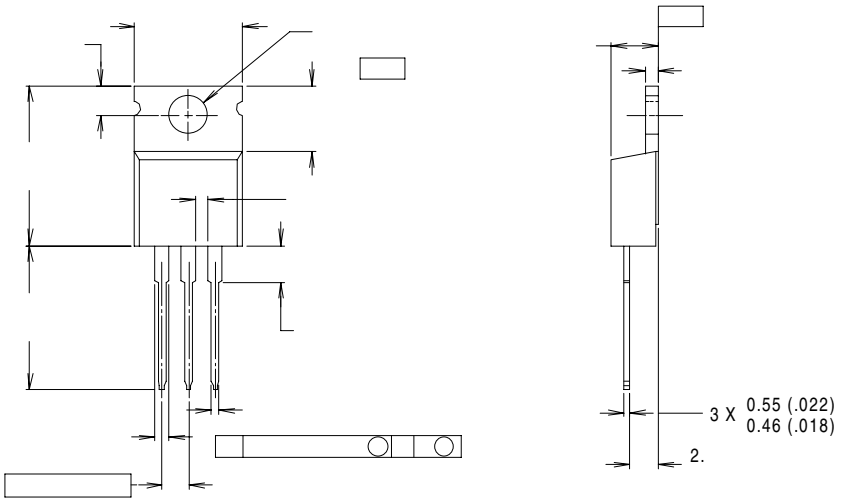


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-220AB



International
IOR Rectifier

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IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD 91449B

International
IOR Rectifier

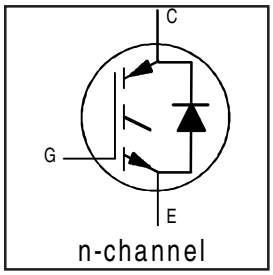
IRG4BC20UD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

UltraFast CoPack IGBT

Features

- UltraFast: optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- IGBT co-packaged with HEXFRED® ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-220AB package

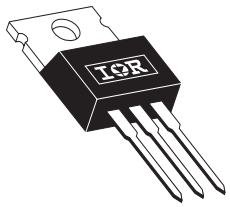


n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.85V

@V_{GE} = 15V, I_C = 6.5A



TO-220AB

Benefits

- Generation -4 IGBTs offer highest efficiencies available
- IGBTs optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBTs. Minimized recovery characteristics require less/no snubbing
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	13	A
I_C @ T_C = 100°C	Continuous Collector Current	6.5	
I_{CM}	Pulsed Collector Current ①	52	
I_{LM}	Clamped Inductive Load Current ②	52	
I_F @ T_C = 100°C	Diode Continuous Forward Current	7.0	
I_{FM}	Diode Maximum Forward Current	52	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	------	------	2.1	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	------	------	3.5	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	------	0.50	------	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	-----	-----	80	
Wt	Weight	------	2 (0.07)	------	g (oz)

3/21/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	----	----	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	----	0.69	----	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	----	1.85	2.1	V	I_C = 6.5A V_{GE} = 15V
		----	2.27	----		I_C = 13A See Fig. 2, 5
		----	1.87	----		I_C = 6.5A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	----	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	----	-11	----	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	1.4	4.3	----	S	V_{CE} = 100V, I_C = 6.5A
I_{CES}	Zero Gate Voltage Collector Current	----	----	250	µA	V_{GE} = 0V, V_{CE} = 600V
		----	----	1700		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	----	1.4	1.7	V	I_C = 8.0A See Fig. 13
		----	1.3	1.6		I_C = 8.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	----	----	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	----	27	41	nC	I_C = 6.5A
Qge	Gate - Emitter Charge (turn-on)	----	4.5	6.8		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	----	10	16		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	----	39	----	ns	T_J = 25°C
t_r	Rise Time	----	15	----		I_C = 6.5A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	93	140		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	----	110	170		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	----	0.16	----	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	----	0.13	----		See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	----	0.29	0.3		
$t_{d(on)}$	Turn-On Delay Time	----	38	----	ns	T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	----	17	----		I_C = 6.5A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	100	----		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	----	220	----		Energy losses include "tail" and
E_{ts}	Total Switching Loss	----	0.49	----	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	----	7.5	----	nH	Measured 5mm from package
C_{ies}	Input Capacitance	----	530	----	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	----	39	----		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	----	7.4	----		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	----	37	55	ns	T_J = 25°C See Fig.
		----	55	90		T_J = 125°C 14 I_F = 8.0A
I_{rr}	Diode Peak Reverse Recovery Current	----	3.5	5.0	A	T_J = 25°C See Fig.
		----	4.5	8.0		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	----	65	138	nC	T_J = 25°C See Fig.
		----	124	360		T_J = 125°C 16 di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	----	240	----	A/µs	T_J = 25°C See Fig.
	During t_b	----	210	----		T_J = 125°C 17

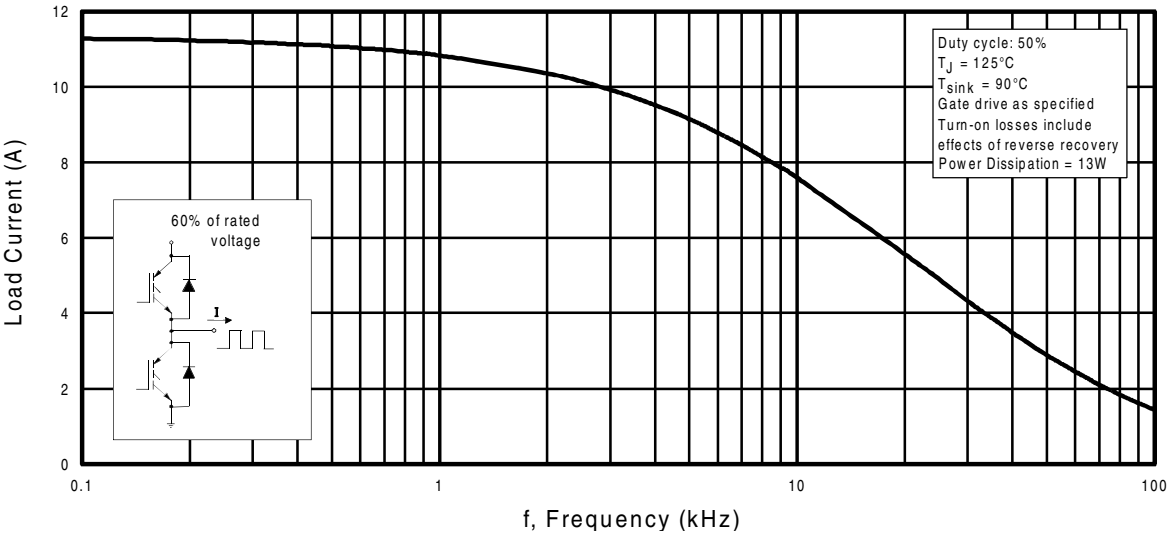


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

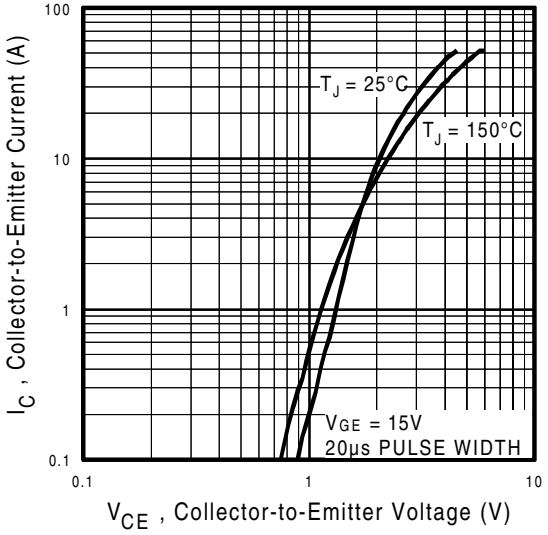


Fig. 2 - Typical Output Characteristics

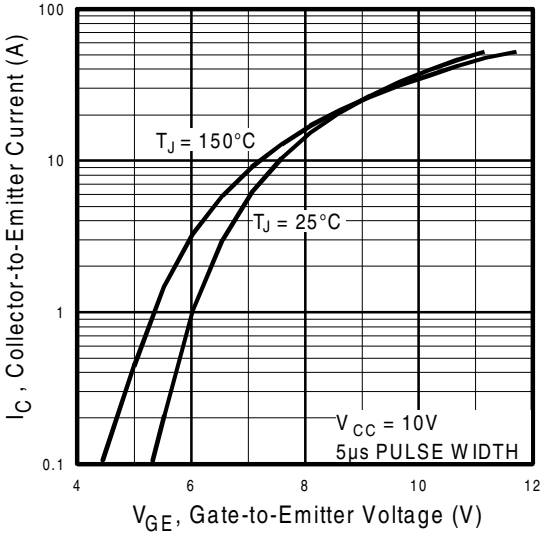


Fig. 3 - Typical Transfer Characteristics

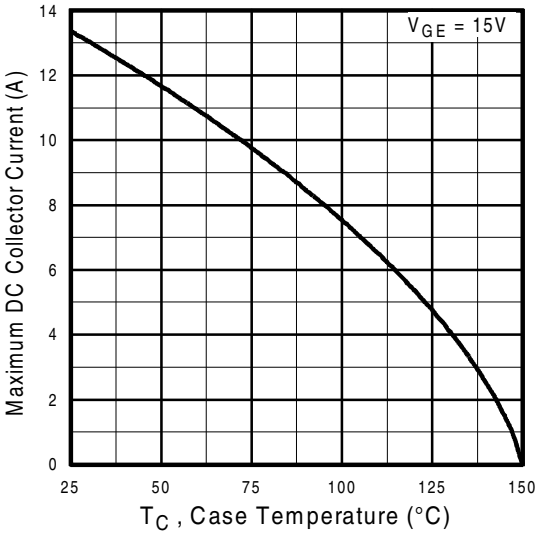


Fig. 4 - Maximum Collector Current vs. Case Temperature

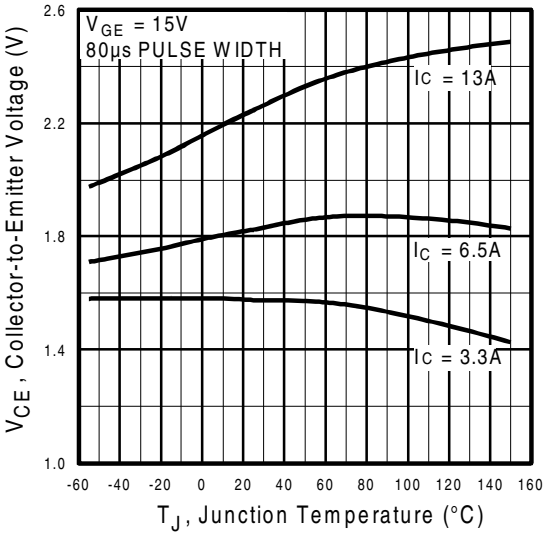


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

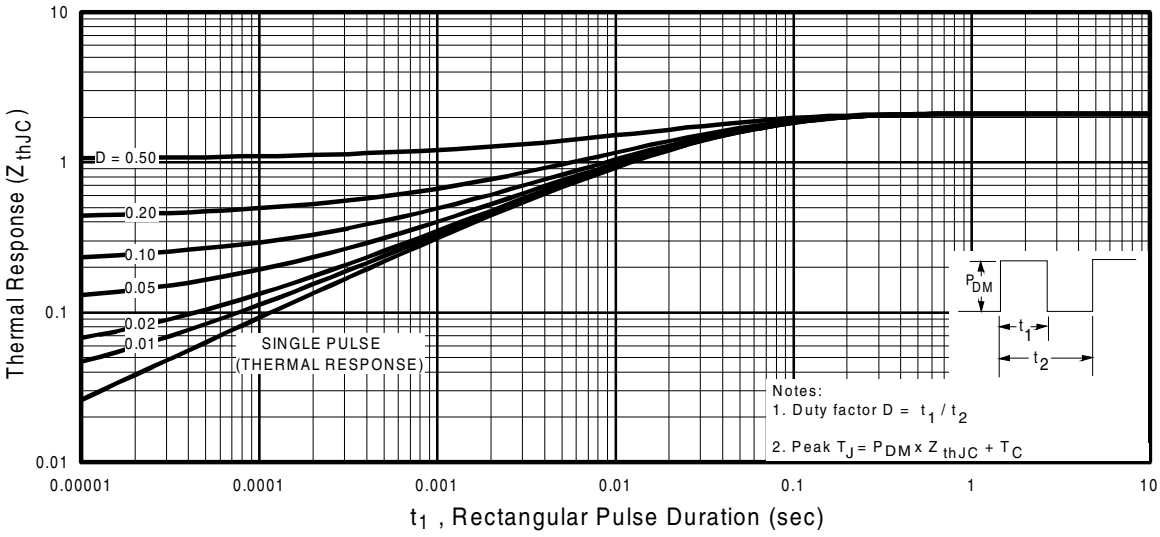


Fig. 6 - Maximum IGBT Effective Transient Thermal Impedance, Junction-to-Case

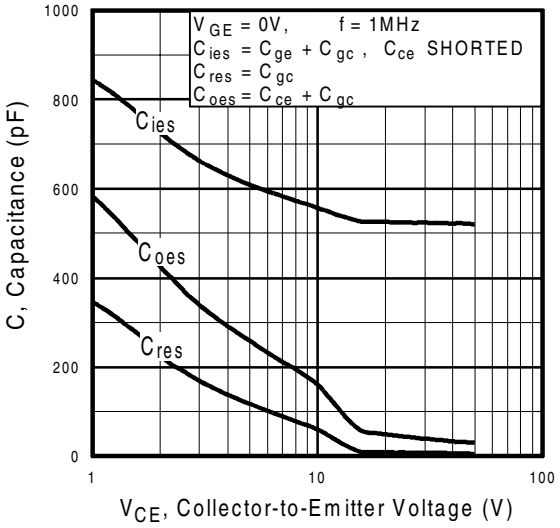


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

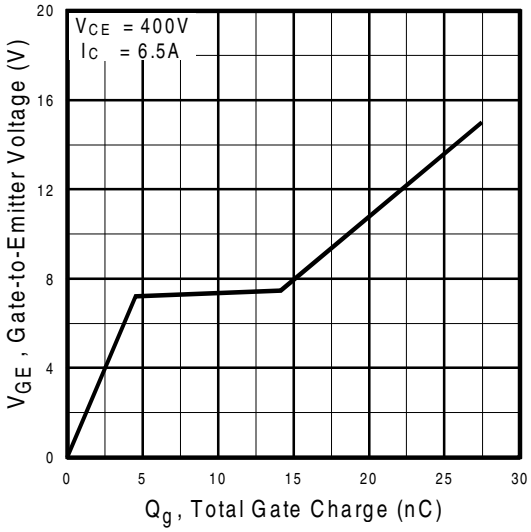


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

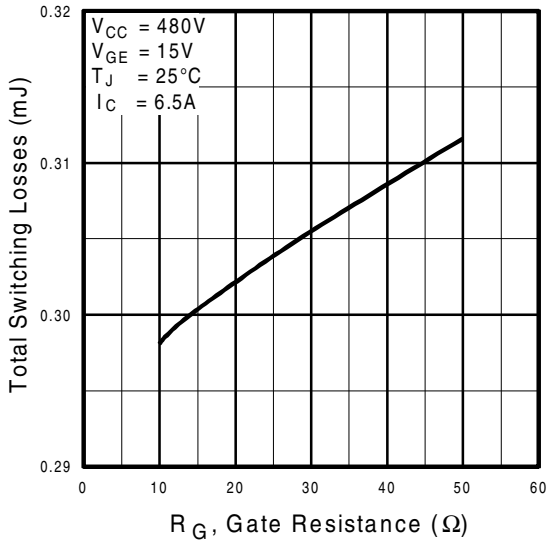


Fig. 9 - Typical Switching Losses vs. Gate Resistance

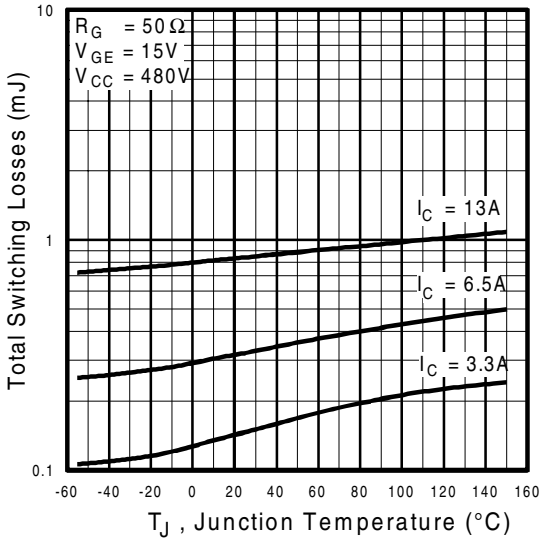


Fig. 10 - Typical Switching Losses vs. Junction Temperature

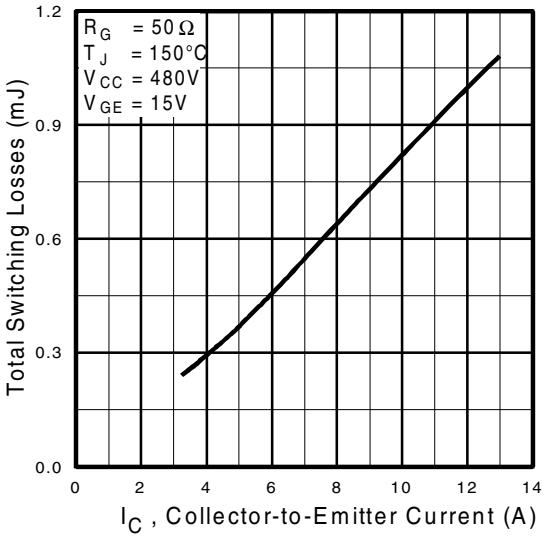


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

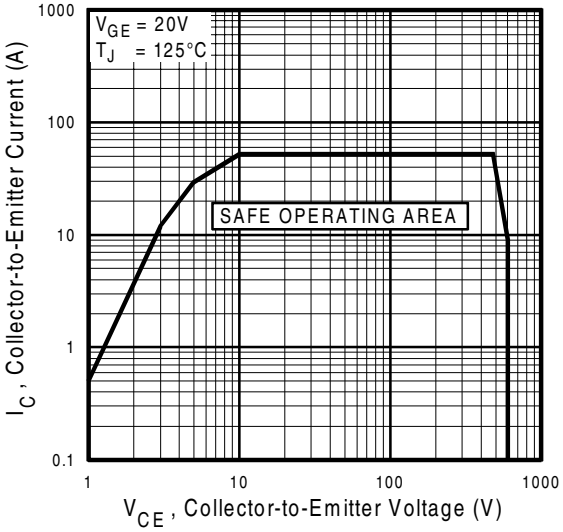


Fig. 12 - Turn-Off SOA

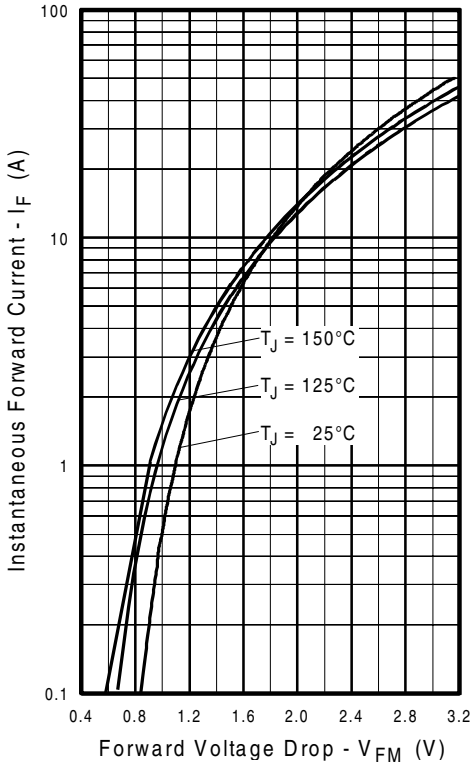


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

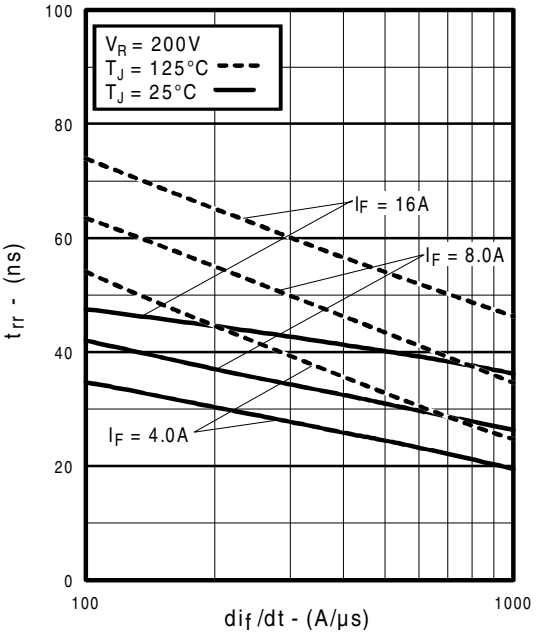


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

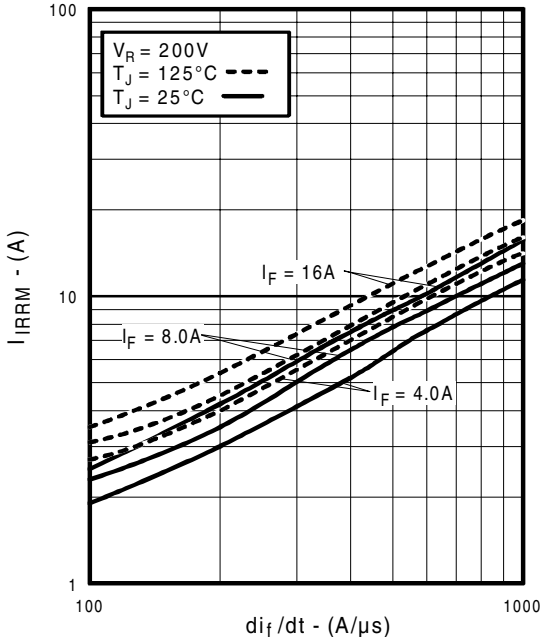


Fig. 15 - Typical Recovery Current vs. di_f/dt

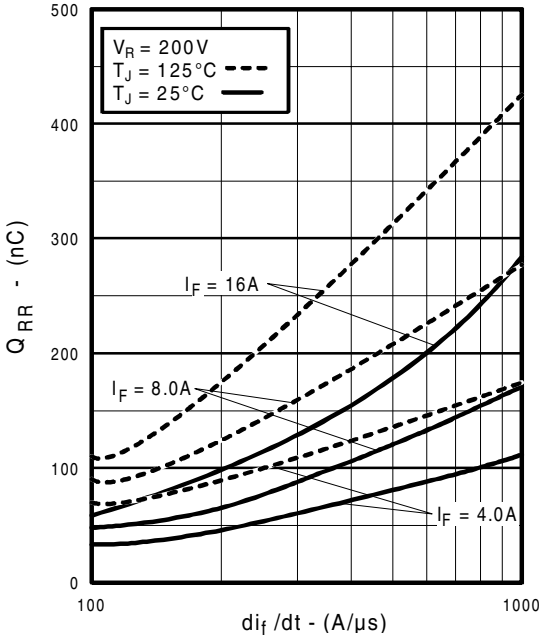


Fig. 16 - Typical Stored Charge vs. di_f/dt

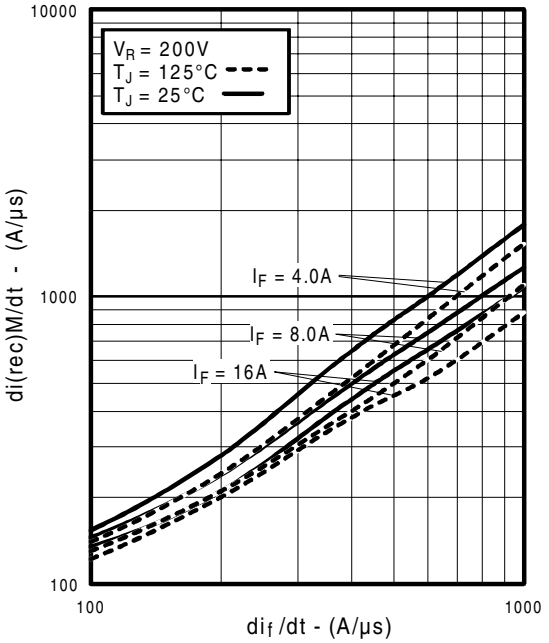


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

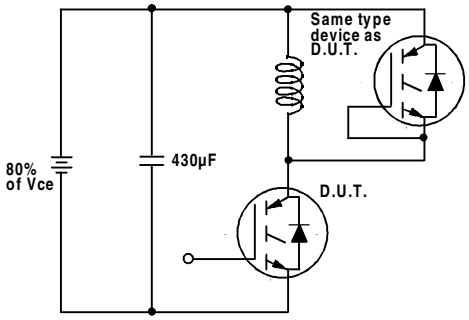


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

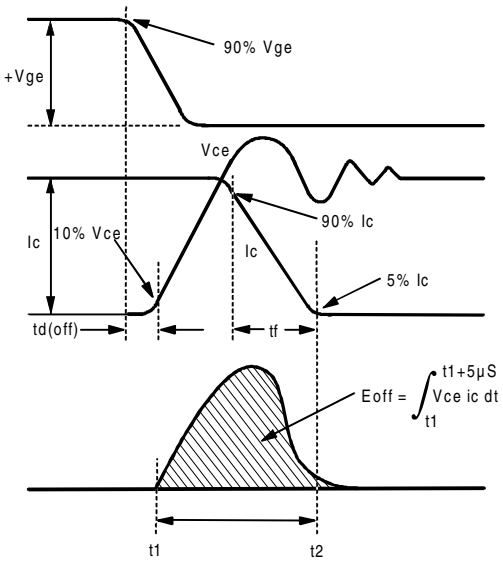


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

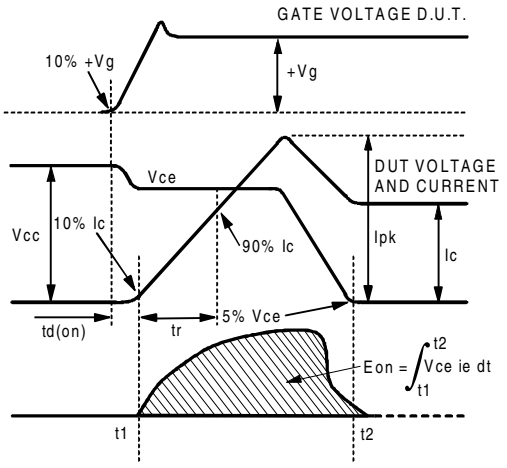


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

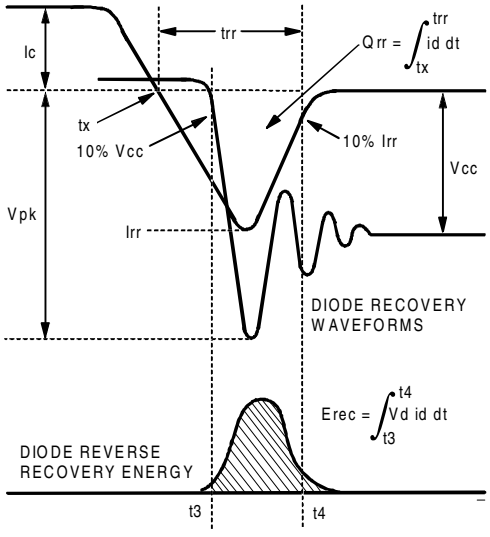


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

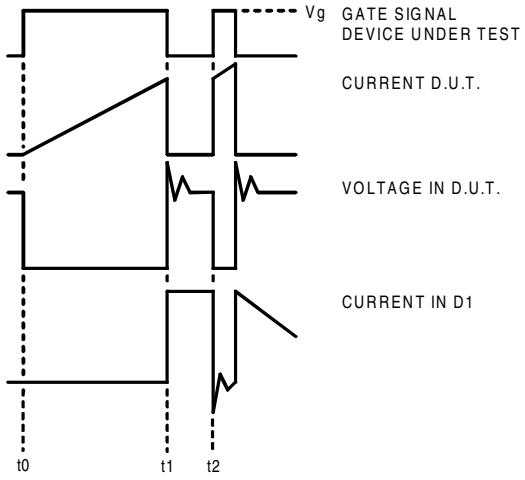


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

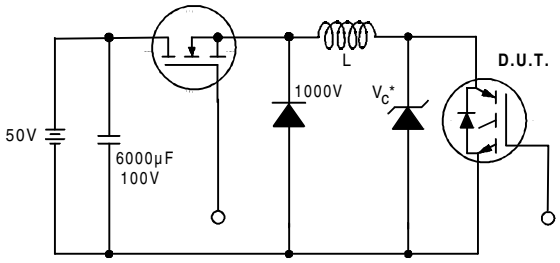


Figure 19. Clamped Inductive Load Test Circuit

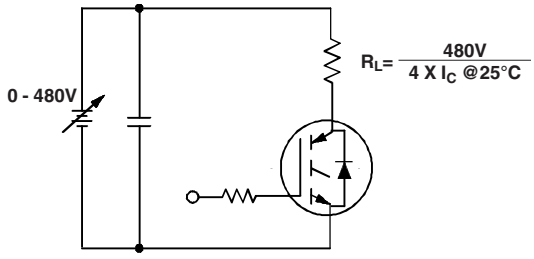


Figure 20. Pulsed Collector Current Test Circuit

Notes:

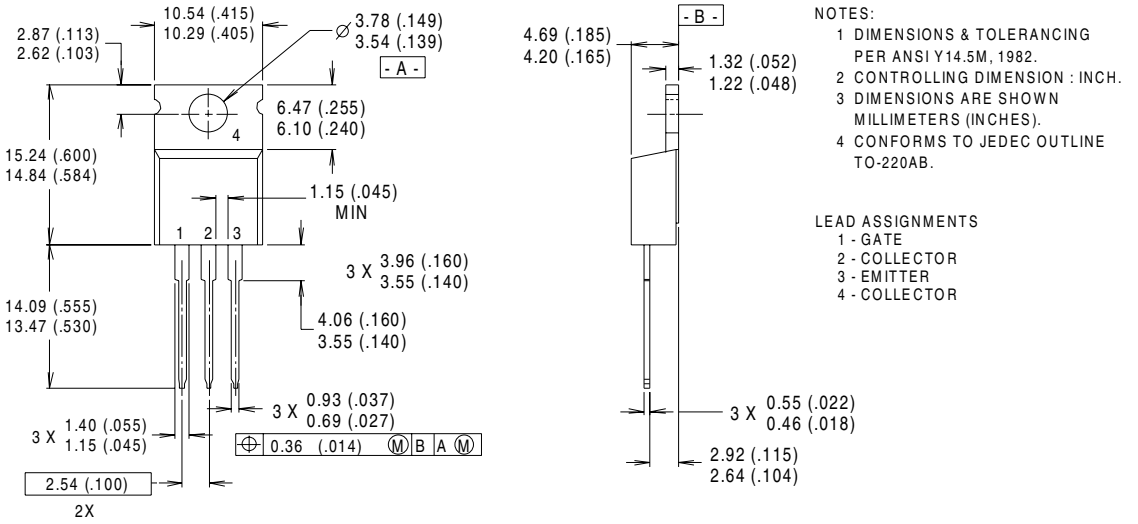
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 50Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD - 91732A

International
IOR Rectifier

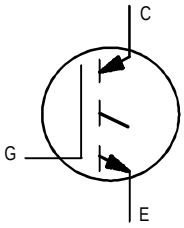
IRG4RC10S

INSULATED GATE BIPOLAR TRANSISTOR

Standard Speed IGBT

Features

- Extremely low voltage drop; 1.0V typical at 2A, 100°C
- Standard: Optimized for minimum saturation voltage and low operating frequencies (< 1kHz)
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than previous generation
- Industry standard TO-252AA package



n-channel

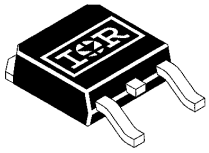
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.10V

@V_{GE} = 15V, I_C = 2.0A

Benefits

- Generation 4 IGBT's offer highest efficiency available
- IGBT's optimized for specified application conditions



D-PAK

TO-252AA

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	14	A
I_C @ T_C = 100°C	Continuous Collector Current	8.0	
I_{CM}	Pulsed Collector Current ①	18	
I_{LM}	Clamped Inductive Load Current ②	18	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	110	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	38	W
P_D @ T_C = 100°C	Maximum Power Dissipation	15	
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	3.3	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
Wt	Weight	0.3 (0.01)	—	g (oz)

* When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.64	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.58	1.7	V	I_C = 8.0A V_{GE} = 15V
		—	2.05	—		I_C = 14A See Fig.2, 5
		—	1.68	—		I_C = 8.0A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-9.5	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	3.7	5.5	—	S	V_{CE} = 100V, I_C = 8.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	15	22	nC	I_C = 8.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	2.4	3.6		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	6.5	9.8		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	
t_r	Rise Time	—	28	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	630	950		I_C = 8.0A, V_{CC} = 480V
t_f	Fall Time	—	710	1100		V_{GE} = 15V, R_G = 100Ω
E_{on}	Turn-On Switching Loss	—	0.14	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	2.58	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	2.72	4.3		
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	T_J = 150°C,
t_r	Rise Time	—	31	—		I_C = 8.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	810	—		V_{GE} = 15V, R_G = 100Ω
t_f	Fall Time	—	1300	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	3.94	—	mJ	See Fig. 11, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	280	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	30	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	4.0	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 100Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

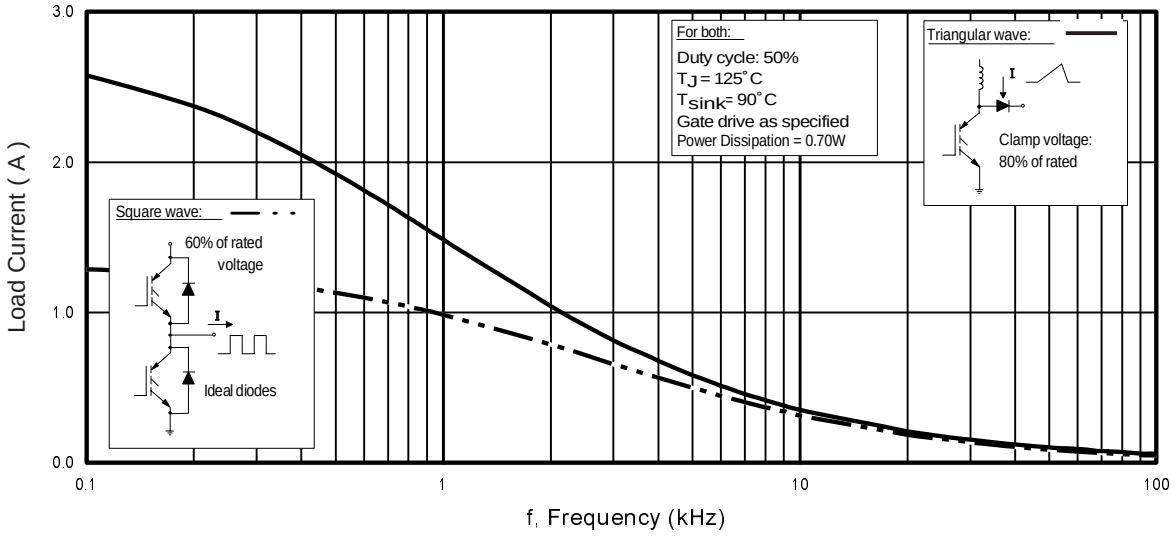


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

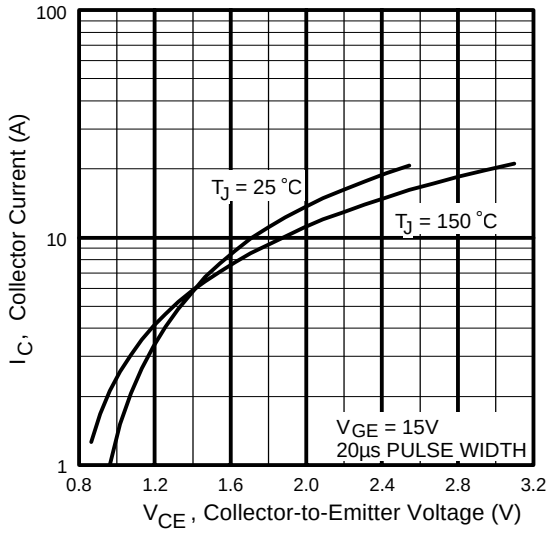


Fig. 2 - Typical Output Characteristics

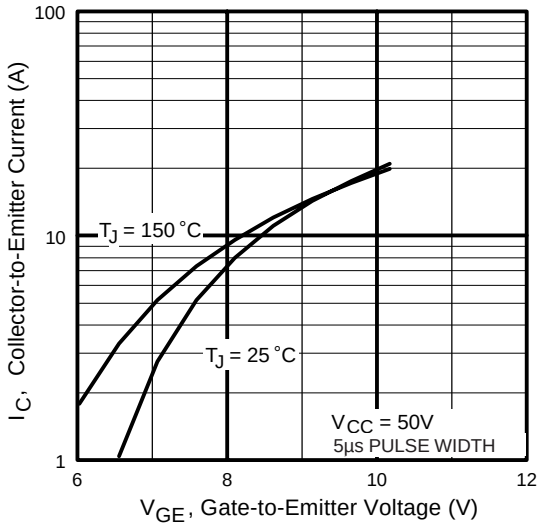


Fig. 3 - Typical Transfer Characteristics

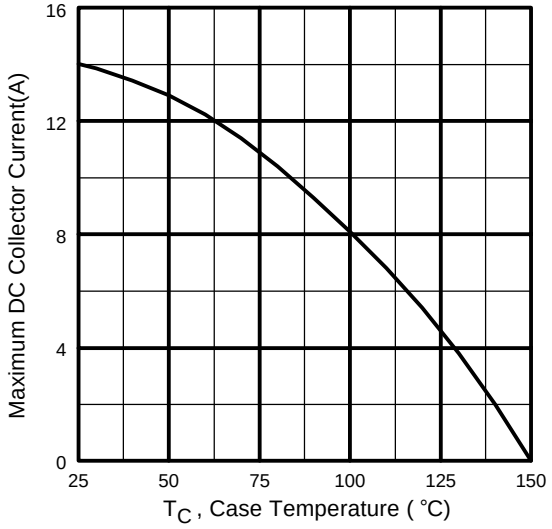


Fig. 4 - Maximum Collector Current vs. Case Temperature

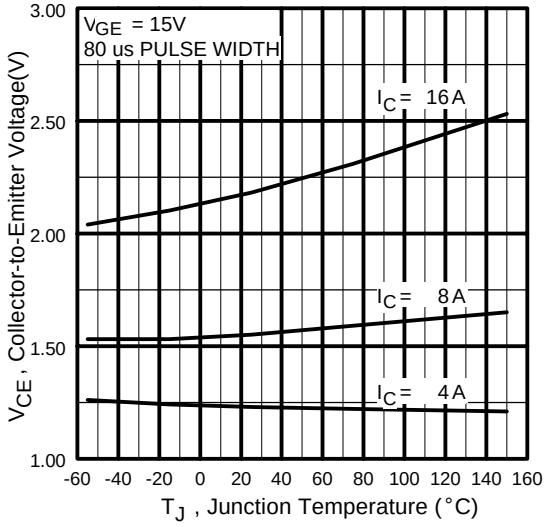


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

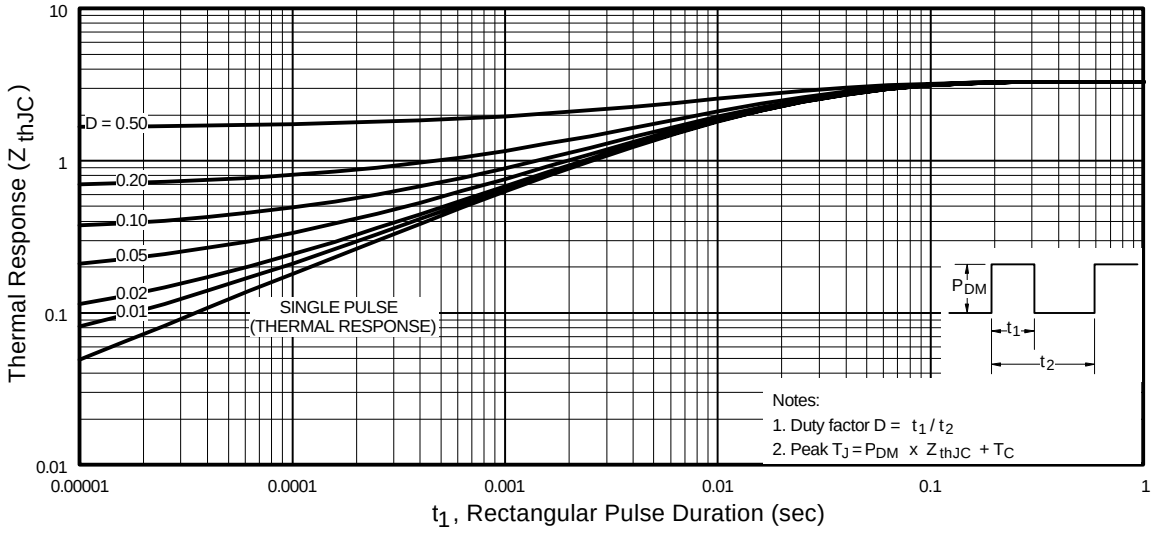


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

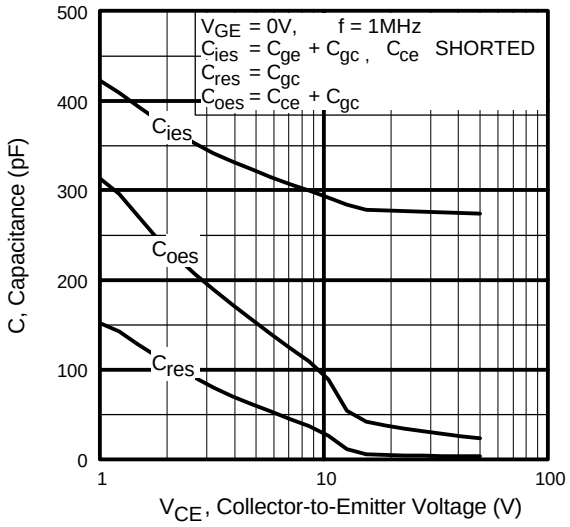


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

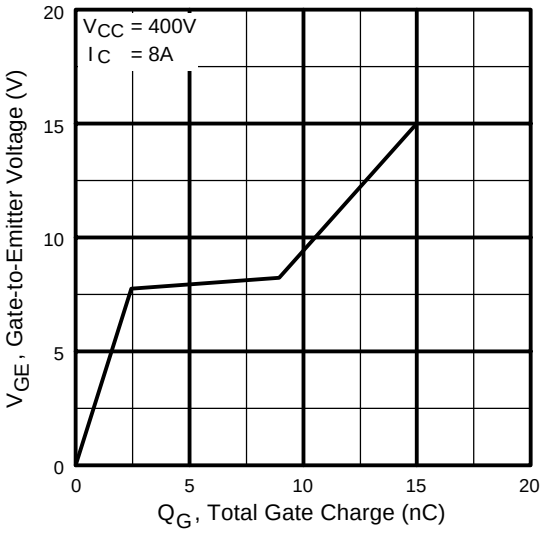


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

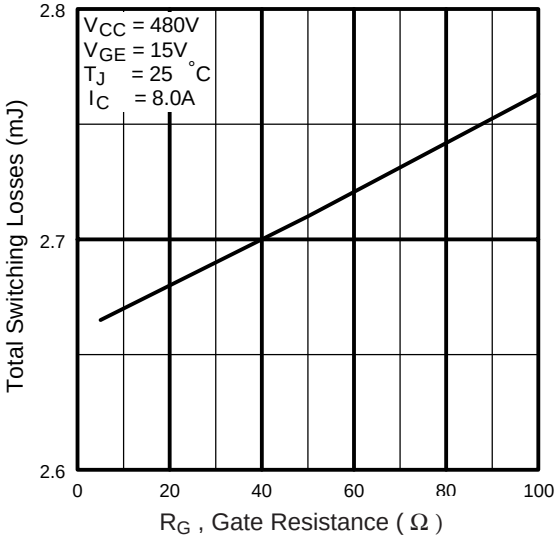


Fig. 9 - Typical Switching Losses vs. Gate Resistance

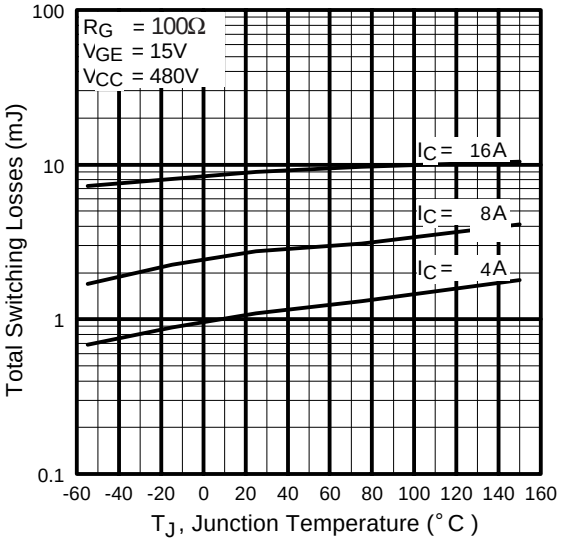


Fig. 10 - Typical Switching Losses vs. Junction Temperature

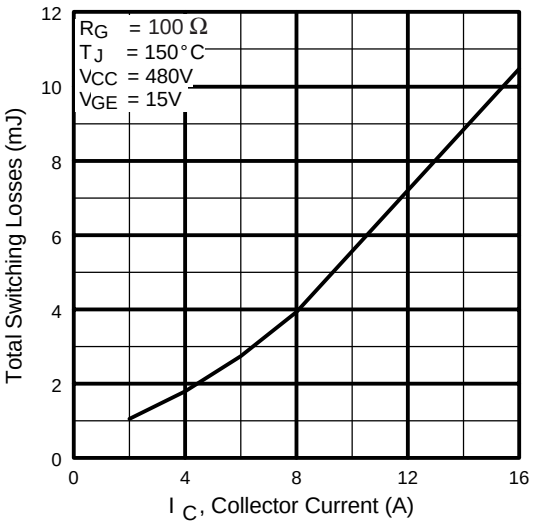


Fig. 11 - Typical Switching Losses vs. Collector Current

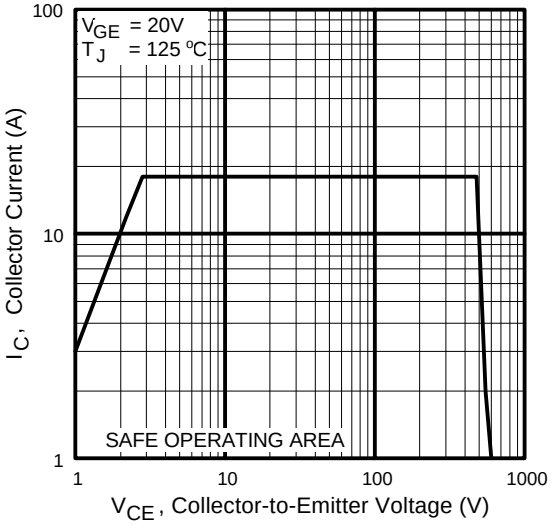


Fig. 12 - Turn-Off SOA

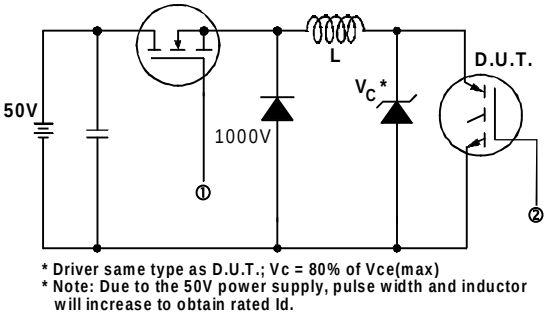


Fig. 13a - Clamped Inductive Load Test Circuit

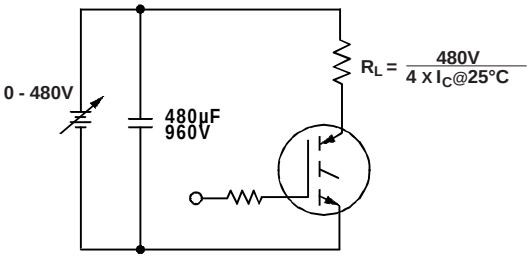


Fig. 13b - Pulsed Collector Current Test Circuit

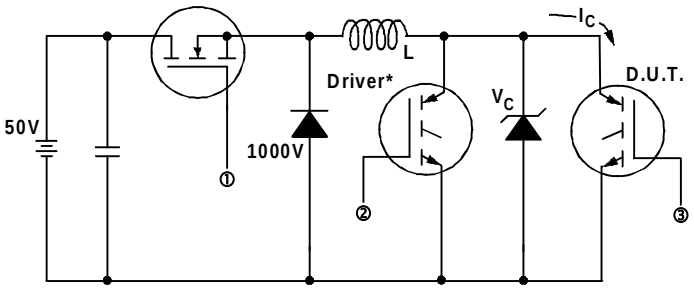


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

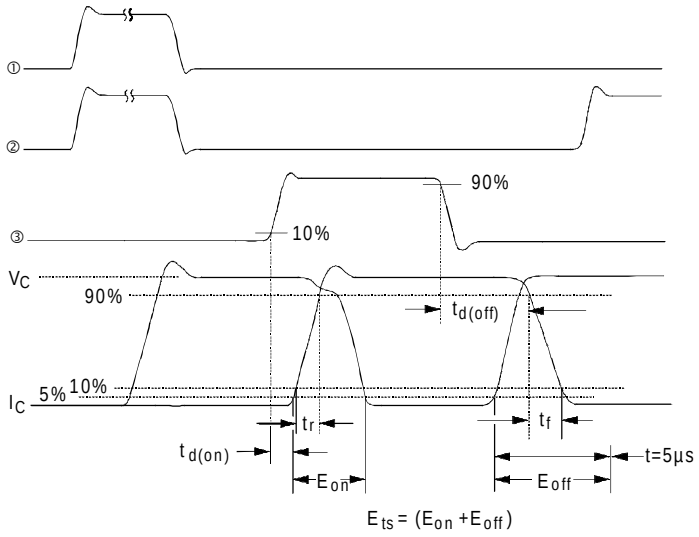
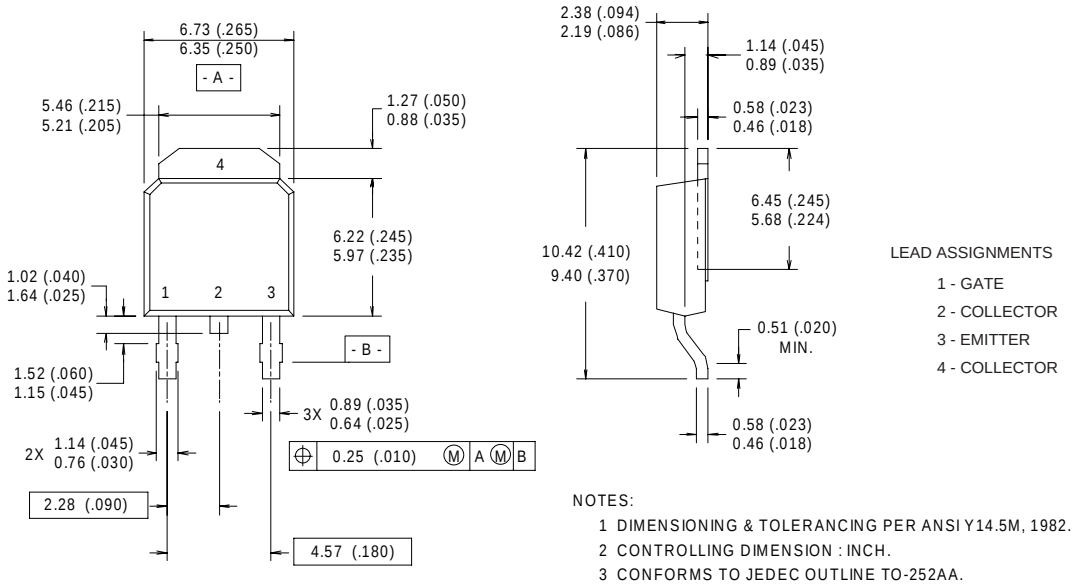


Fig. 14b - Switching Loss Waveforms

Package Outline

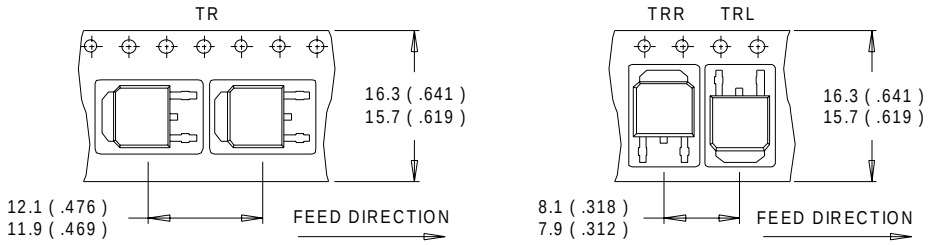
TO-252AA Outline
Dimensions are shown in millimeters (inches)



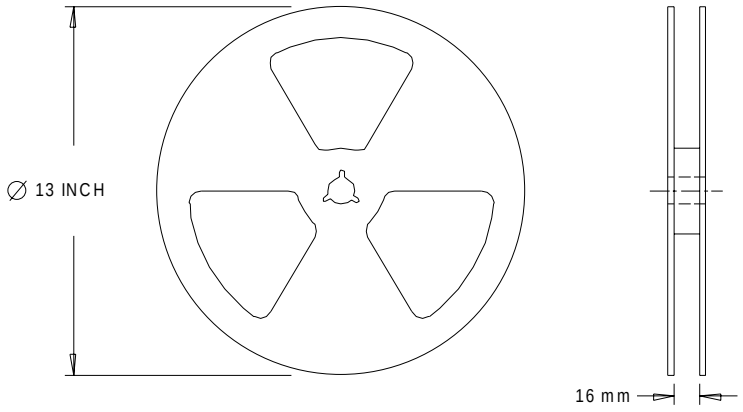
NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

Tape & Reel Information

TO-252AA



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936
http://www.irf.com/ Data and specifications subject to change without notice. 8/99

PD - 91786A

International
IOR Rectifier

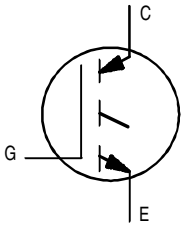
IRG4BC10S

INSULATED GATE BIPOLAR TRANSISTOR

Standard Speed IGBT

Features

- Extremely low voltage drop; 1.1V typical at 2A
- S-Speed: Minimizes power dissipation at up to 3 KHz PWM frequency in inverter drives, up to 4 KHz in brushless DC drives, up to 2KHz in Chopper Applications
- Very Tight Vce(on) distribution
- Industry standard TO-220AB package



n-channel

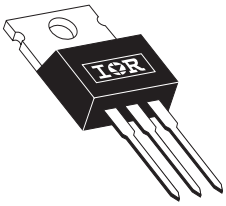
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.10V

@V_{GE} = 15V, I_C = 2.0A

Benefits

- Generation 4 IGBTs offer highest efficiency available
- IGBTs optimized for specified application conditions
- Lower conduction losses than many Power MOSFET''s



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	14	A
I_C @ T_C = 100°C	Continuous Collector Current	8.0	
I_{CM}	Pulsed Collector Current ①	18	
I_{LM}	Clamped Inductive Load Current ②	18	
V_{GE}	Gate-to-Emitter Voltage	± 20	
E_{ARV}	Reverse Voltage Avalanche Energy ③	110	mJ
P_DT_C = 25°C	Maximum Power Dissipation	38	W
P_D @ T_C = 100°C	Maximum Power Dissipation	15	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	3.3	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	50	
Wt	Weight	2.0(0.07)	—	g (oz)

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.64	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.58	1.7	V	I_C = 8.0A V_{GE} = 15V
		—	2.05	—		I_C = 14A See Fig.2, 5
		—	1.68	—		I_C = 8.0A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-9.5	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	3.7	5.5	—	S	V_{CE} = 100V, I_C = 8.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	15	22	nC	I_C = 8.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	2.4	3.6		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	6.5	9.8		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	
t_r	Rise Time	—	28	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	630	950		I_C = 8.0A, V_{CC} = 480V
t_f	Fall Time	—	710	1100		V_{GE} = 15V, R_G = 100Ω
E_{on}	Turn-On Switching Loss	—	0.14	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	2.58	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	2.72	4.3		
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	T_J = 150°C,
t_r	Rise Time	—	31	—		I_C = 8.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	810	—		V_{GE} = 15V, R_G = 100Ω
t_f	Fall Time	—	1300	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	3.94	—	mJ	See Fig. 11, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	280	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	30	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	4.0	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 100Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

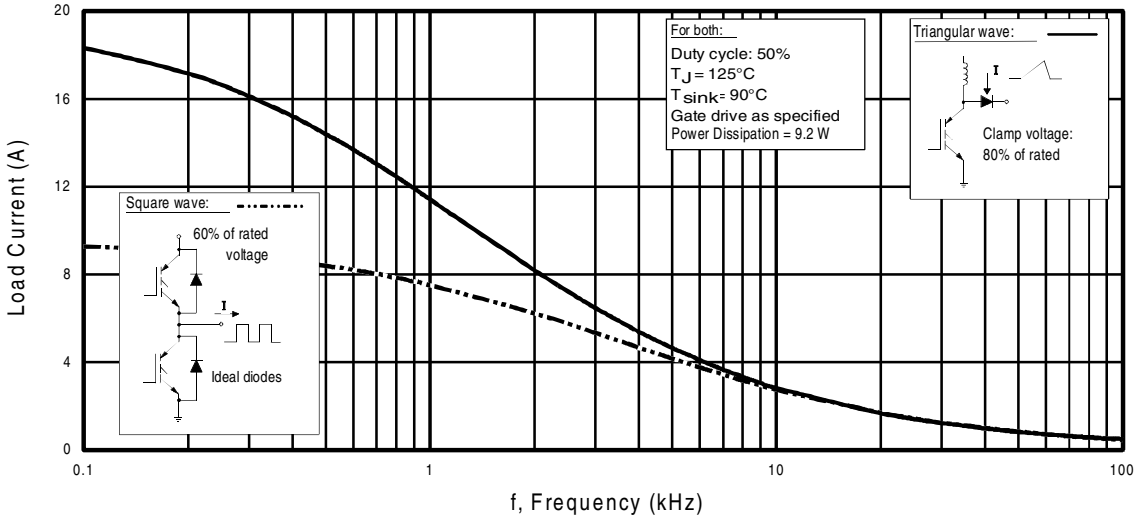


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

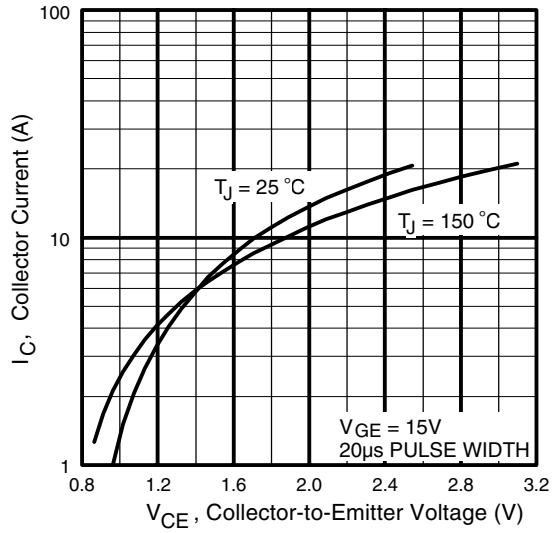


Fig. 2 - Typical Output Characteristics

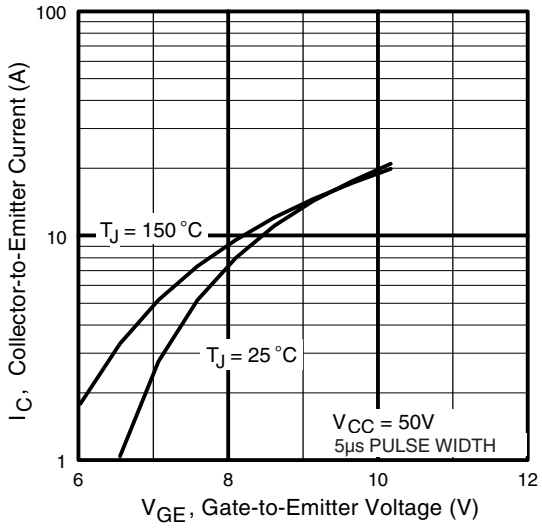


Fig. 3 - Typical Transfer Characteristics

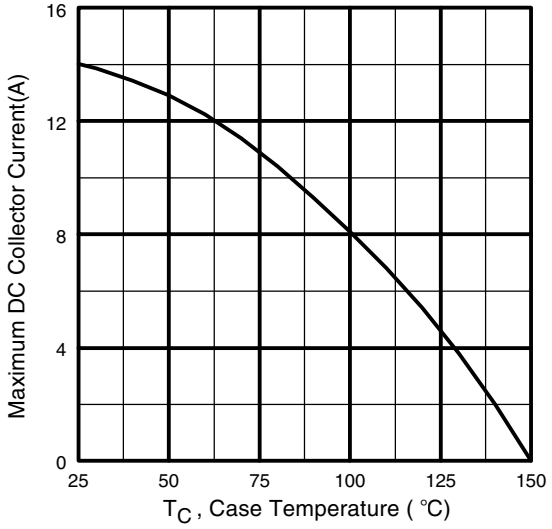


Fig. 4 - Maximum Collector Current vs. Case Temperature

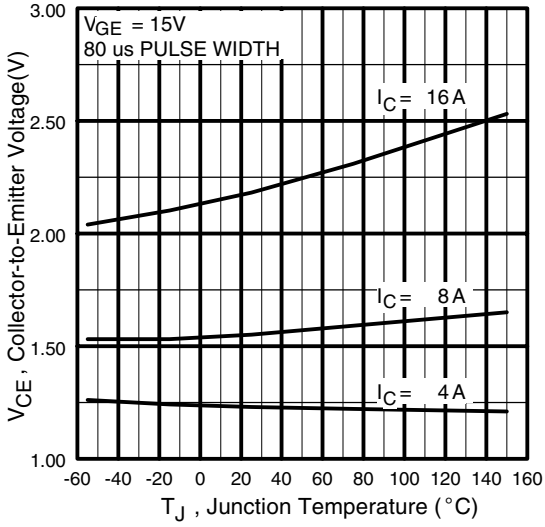


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

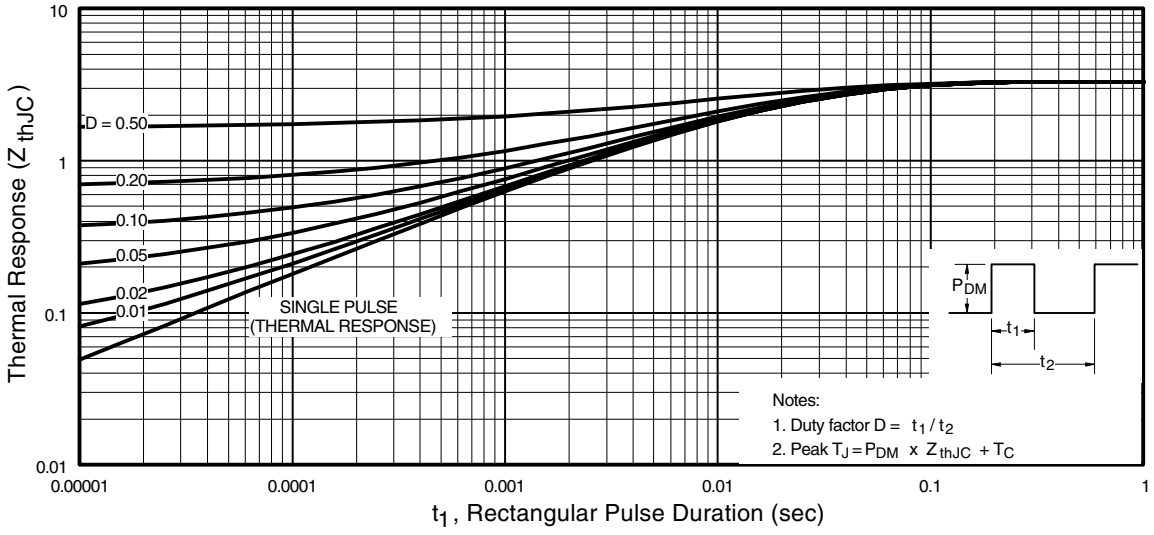


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

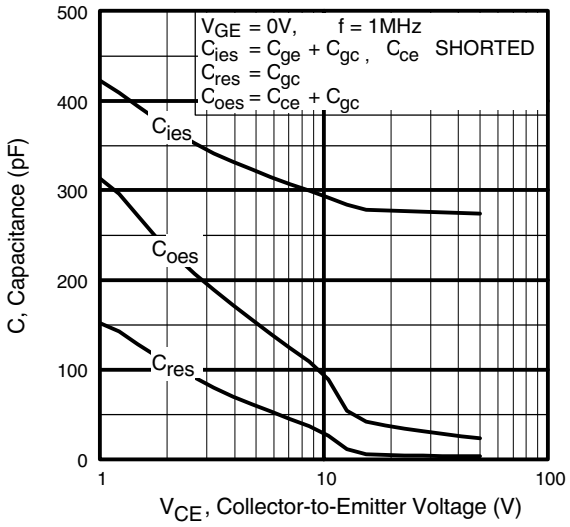


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

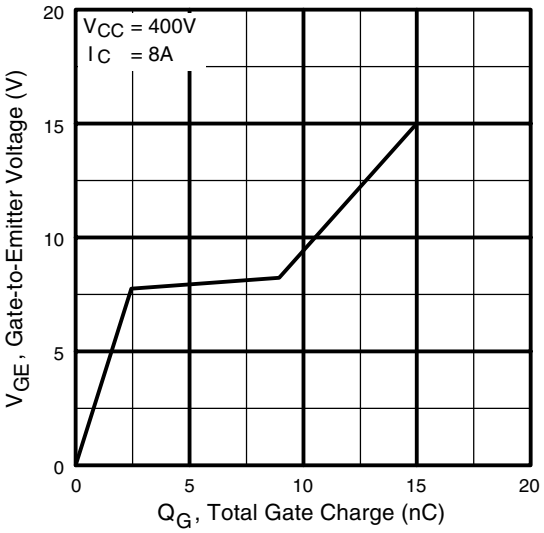


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

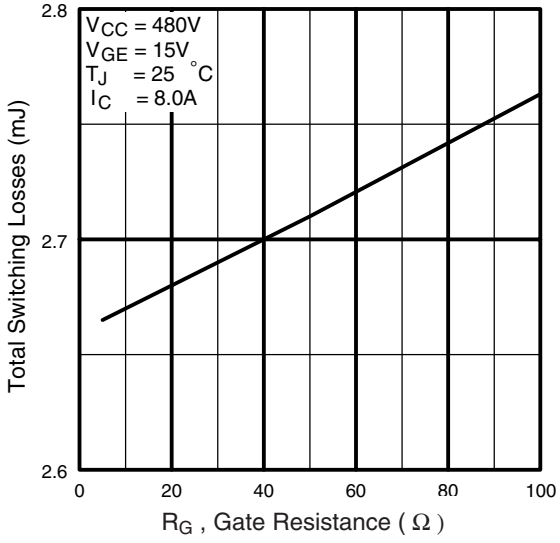


Fig. 9 - Typical Switching Losses vs. Gate Resistance

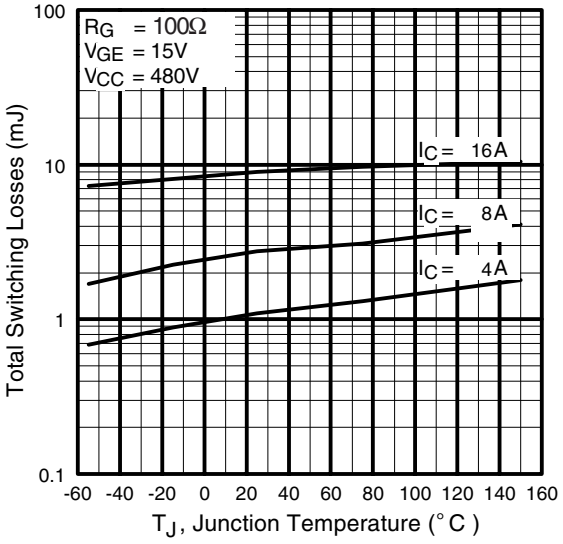


Fig. 10 - Typical Switching Losses vs. Junction Temperature

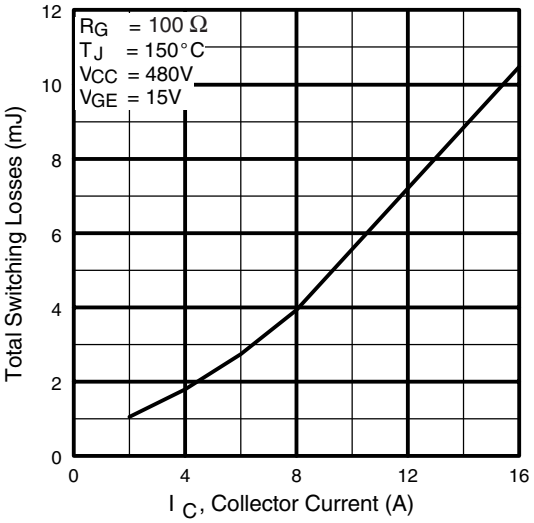


Fig. 11 - Typical Switching Losses vs. Collector Current

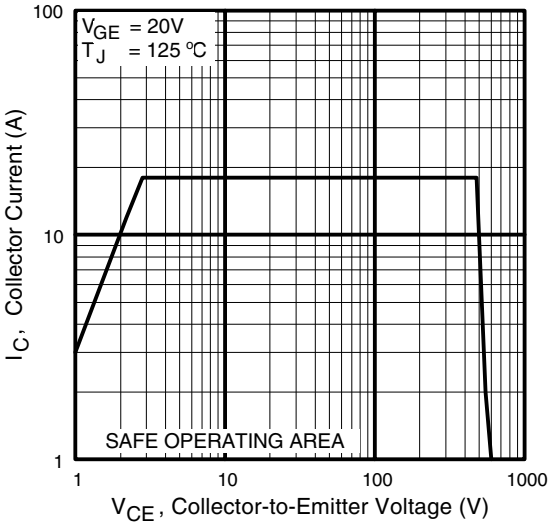


Fig. 12 - Turn-Off SOA

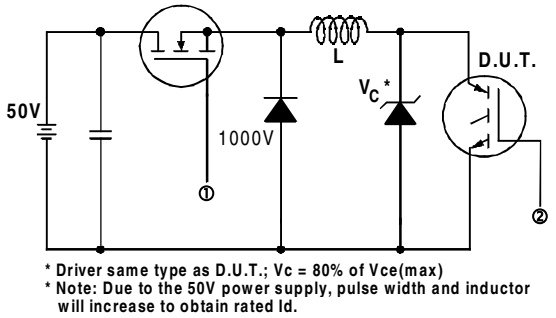


Fig. 13a - Clamped Inductive Load Test Circuit

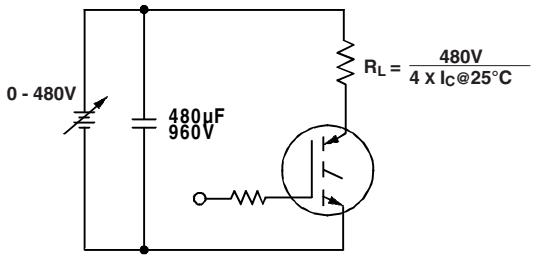


Fig. 13b - Pulsed Collector Current Test Circuit

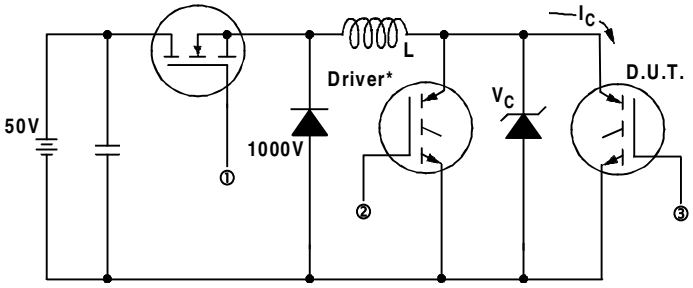


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

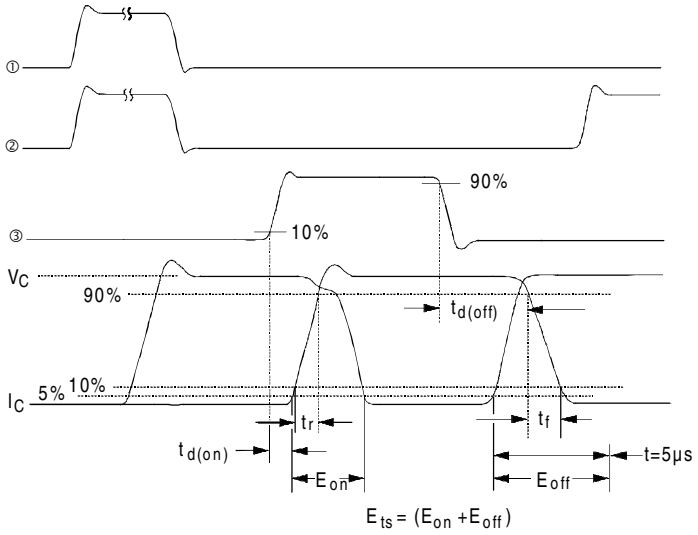
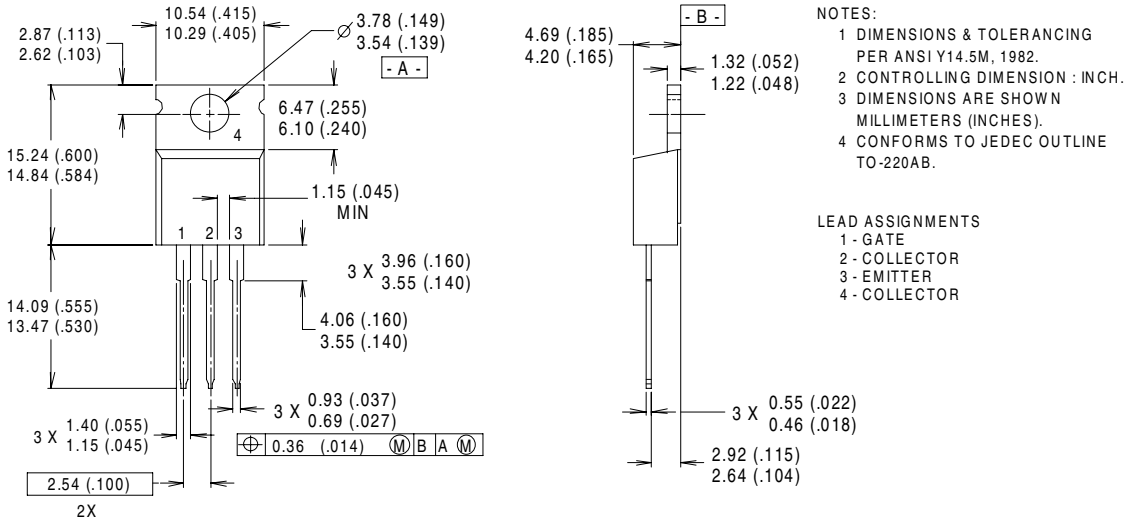


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-220AB



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-220AB.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

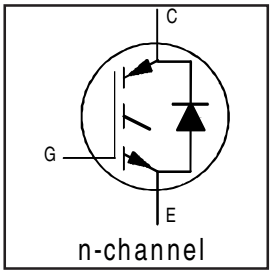
PD -91784A

International
IOR Rectifier

IRG4BC10SD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Standard Speed CoPack IGBT



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.10V

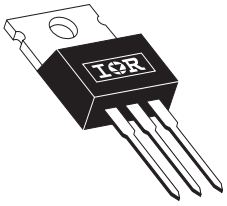
@V_{GE} = 15V, I_C = 2.0A

Features

- Extremely low voltage drop 1.1Vtyp. @ 2A
- S-Series: Minimizes power dissipation at up to 3 KHz PWM frequency in inverter drives, up to 4 KHz in brushless DC drives.
- Very Tight Vce(on) distribution
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-220AB package

Benefits

- Generation 4 IGBTs offer highest efficiencies available
- IGBTs optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBTs . Minimized recovery characteristics require less/no snubbing
- Lower losses than MOSFET's conduction and Diode losses



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	14	A
I_C @ T_C = 100°C	Continuous Collector Current	8.0	
I_{CM}	Pulsed Collector Current ①	18	
I_{LM}	Clamped Inductive Load Current ②	18	
I_F @ T_C = 100°C	Diode Continuous Forward Current	4.0	
I_{FM}	Diode Maximum Forward Current	18	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	38	W
P_D @ T_C = 100°C	Maximum Power Dissipation	15	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	——	——	3.3	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	——	——	7.0	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	——	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	——	80	
Wt	Weight	——	2.0(0.07)	——	g (oz)

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.64	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.58	1.7	V	I_C = 8.0A V_{GE} = 15V
		—	2.05	—		I_C = 14.0A See Fig. 2, 5
		—	1.68	—		I_C = 8.0A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-9.5	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance④	3.65	5.48	—	S	V_{CE} = 100V, I_C =8.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.5	1.8	V	I_C =4.0A See Fig. 13
		—	1.4	1.7		I_C =4.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	15	22	nC	I_C = 8.0A
Qge	Gate - Emitter Charge (turn-on)	—	2.42	3.6		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	6.53	9.8		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	76	—	ns	T_J = 25°C
t_r	Rise Time	—	32	—		I_C = 8.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	815	1200		V_{GE} = 15V, R_G = 100Ω
t_f	Fall Time	—	720	1080		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	0.31	—		diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	3.28	—	mJ	See Fig. 9, 10, 18
E_{ts}	Total Switching Loss	—	3.60	10.9		
E_{ts}	Total Switching Loss	—	1.46	2.6	mJ	I_C = 5.0A
$t_{d(on)}$	Turn-On Delay Time	—	70	—	ns	T_J = 150°C, See Fig. 10,11, 18
t_r	Rise Time	—	36	—		I_C = 8.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	890	—		V_{GE} = 15V, R_G = 100Ω
t_f	Fall Time	—	890	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	3.83	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	280	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	30	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	4.0	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	28	42	ns	T_J = 25°C See Fig.
		—	38	57		T_J = 125°C 14 I_F =4.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	2.9	5.2	A	T_J = 25°C See Fig.
		—	3.7	6.7		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	40	60	nC	T_J = 25°C See Fig.
		—	70	105		T_J = 125°C 16 di/dt = 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	280	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	235	—		T_J = 125°C 17

Details of note ① through ④ are on the last page

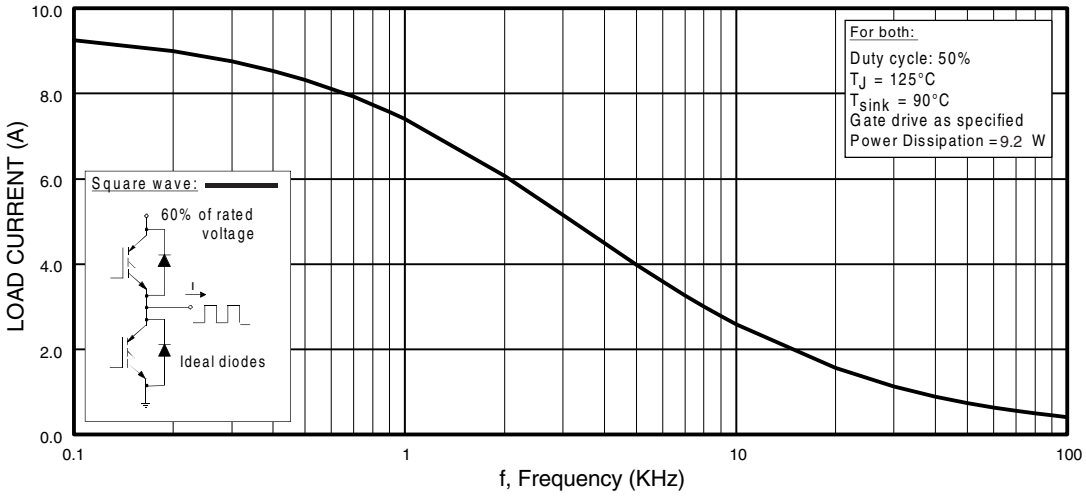


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

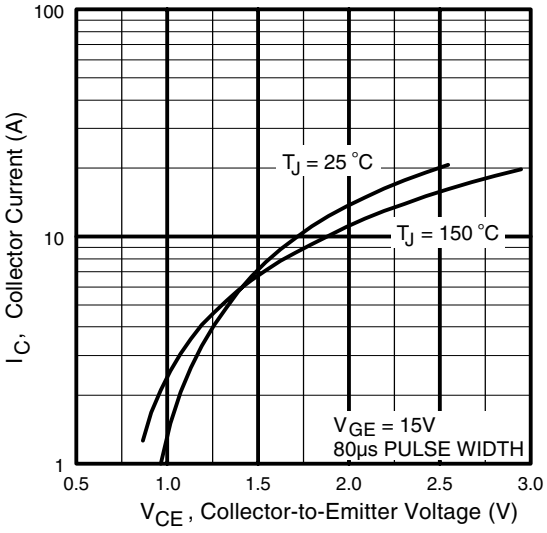


Fig. 2 - Typical Output Characteristics

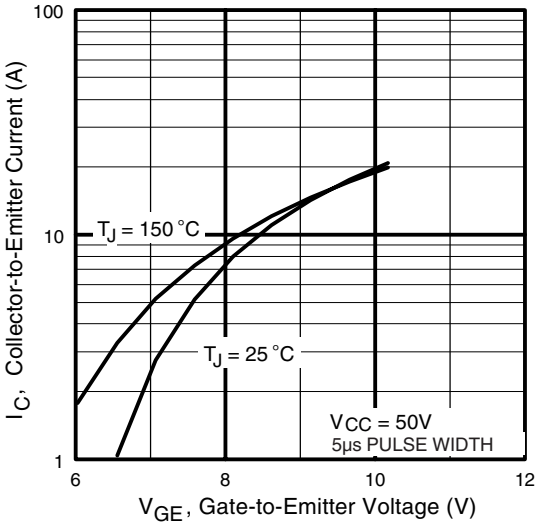


Fig. 3 - Typical Transfer Characteristics

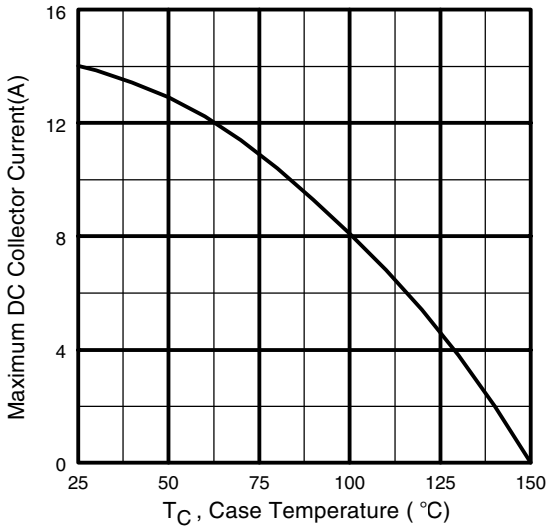


Fig. 4 - Maximum Collector Current vs. Case Temperature

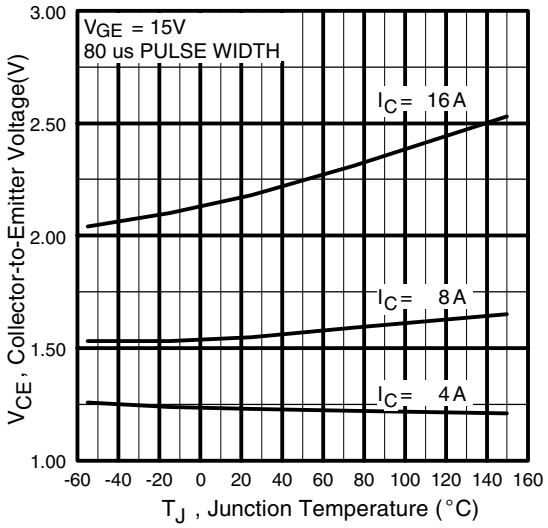


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

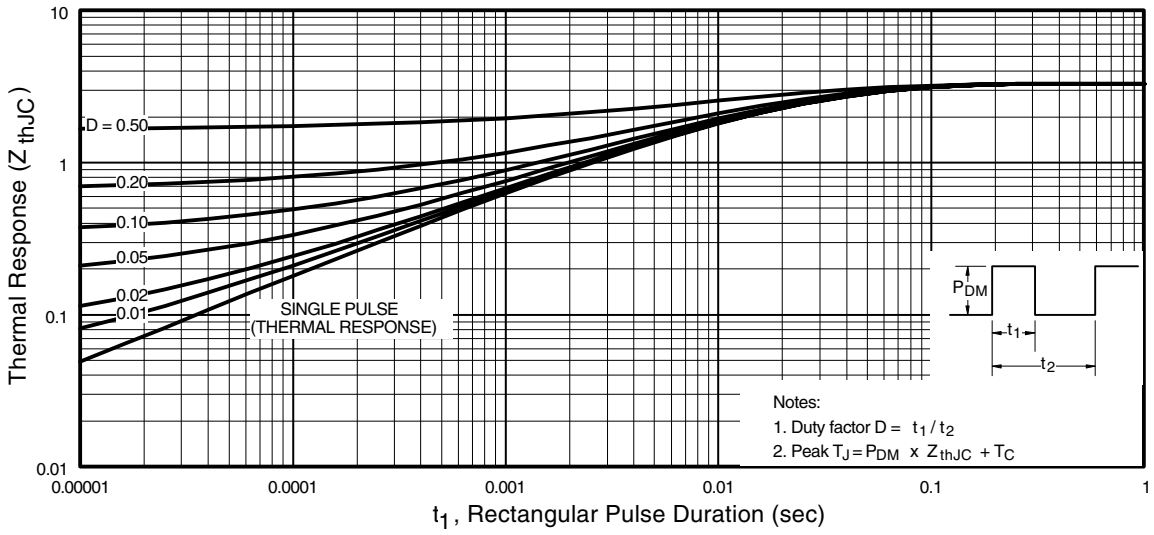


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

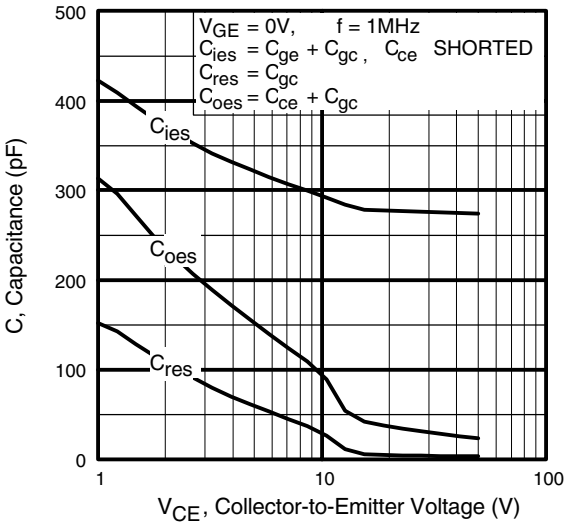


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

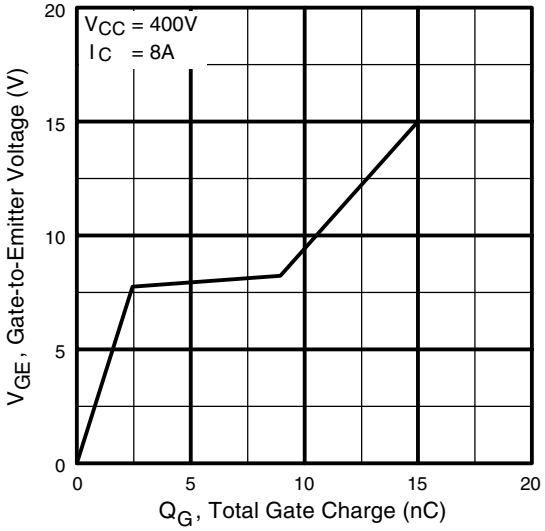


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

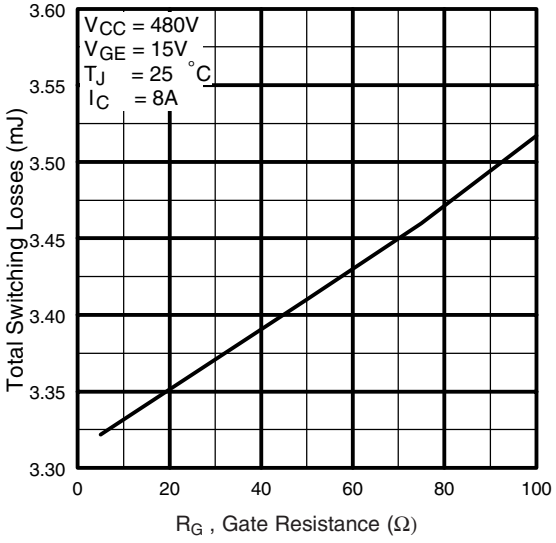


Fig. 9 - Typical Switching Losses vs. Gate Resistance

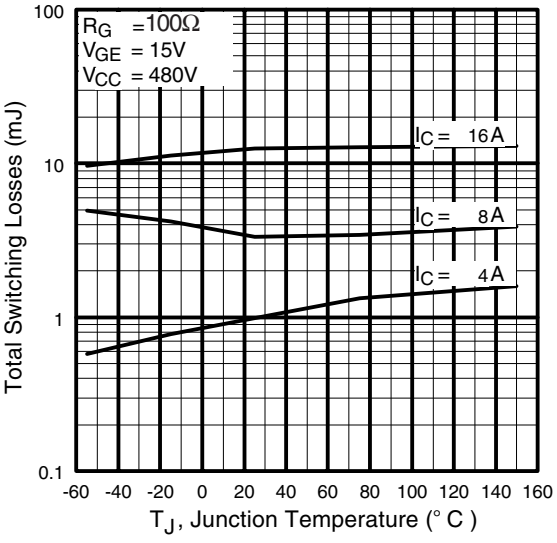


Fig. 10 - Typical Switching Losses vs. Junction Temperature

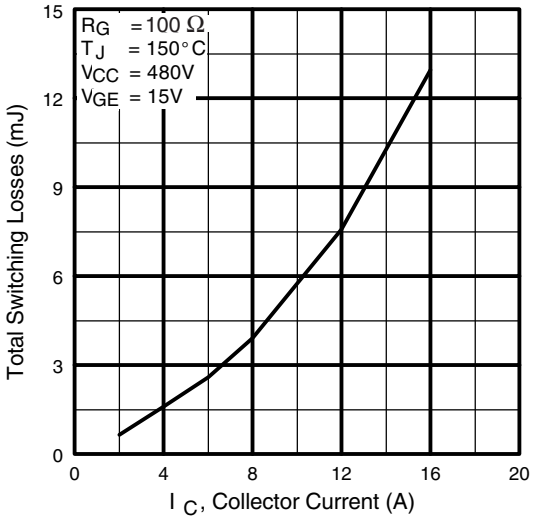


Fig. 11 - Typical Switching Losses vs. Collector Current

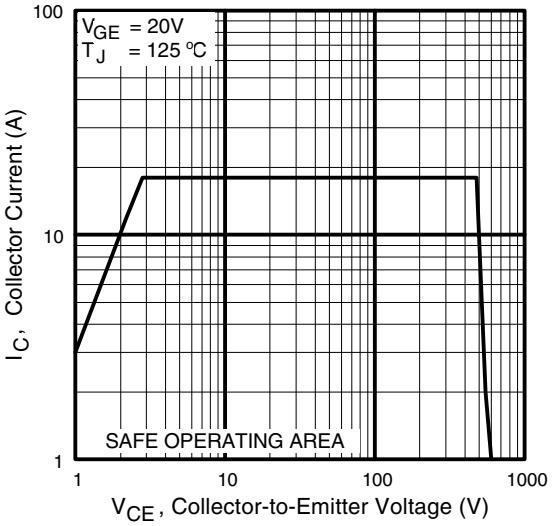


Fig. 12 - Turn-Off SOA

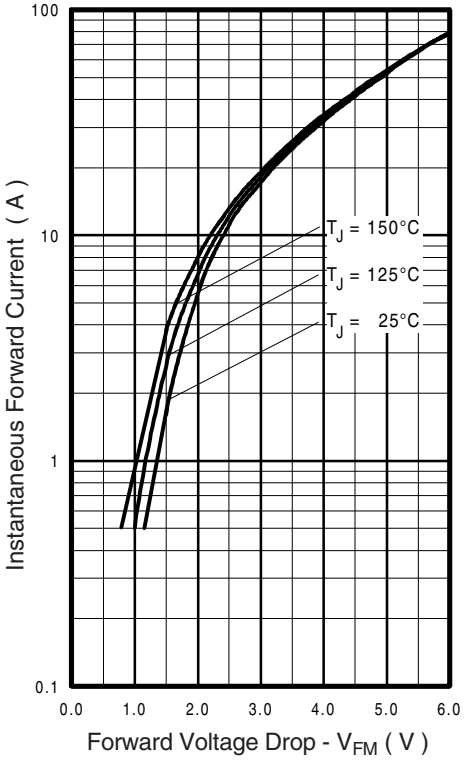


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

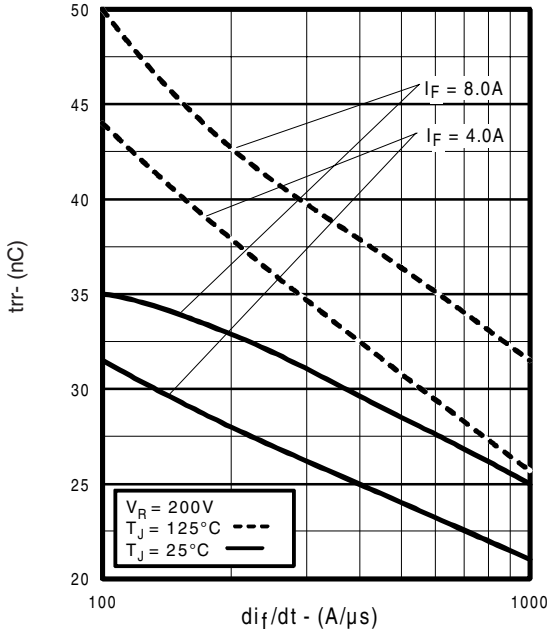


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

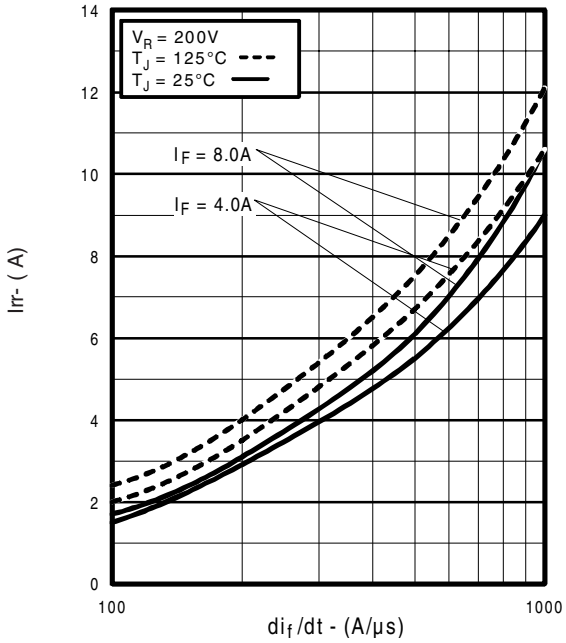


Fig. 15 - Typical Recovery Current vs. di_f/dt

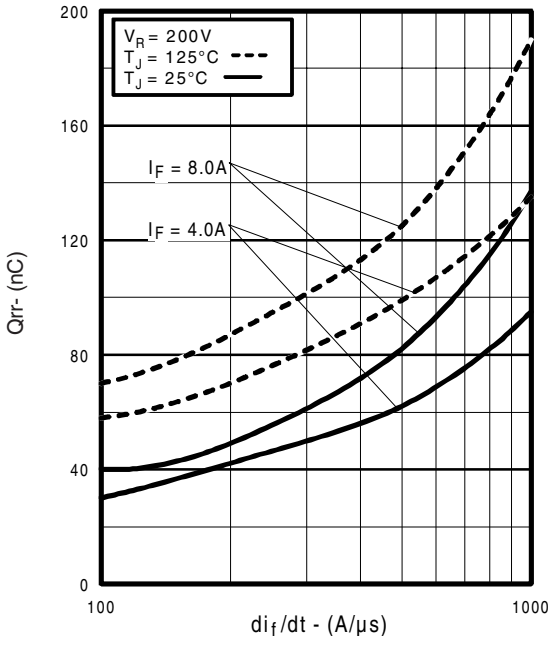


Fig. 16 - Typical Stored Charge vs. di_f/dt

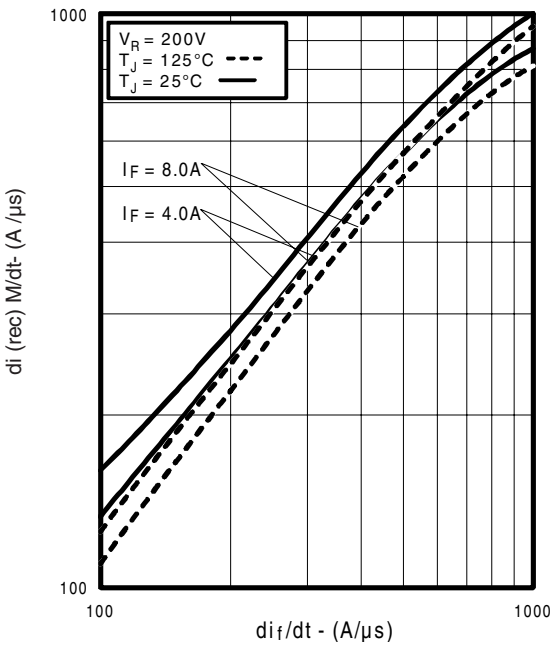


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt,

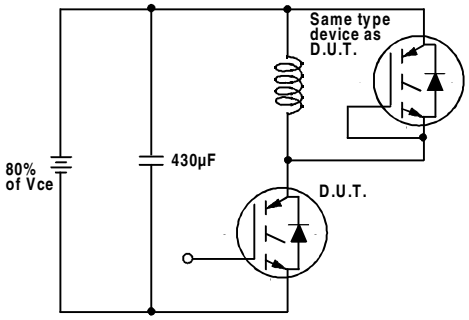


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

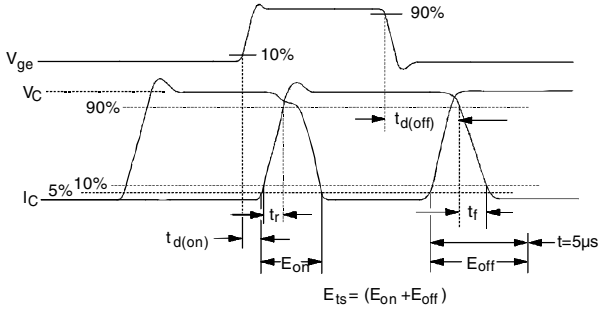


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

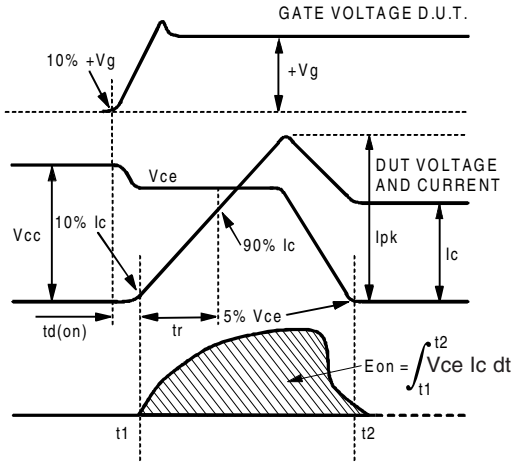


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

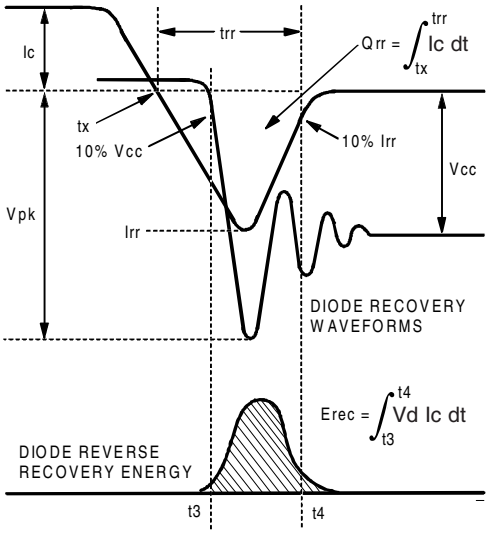


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

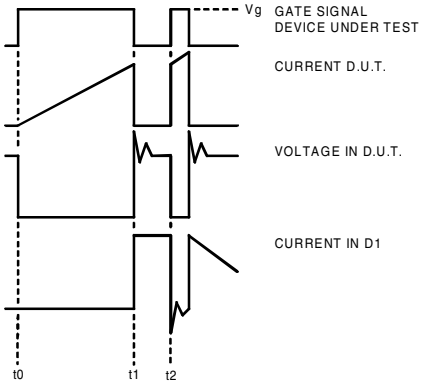


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

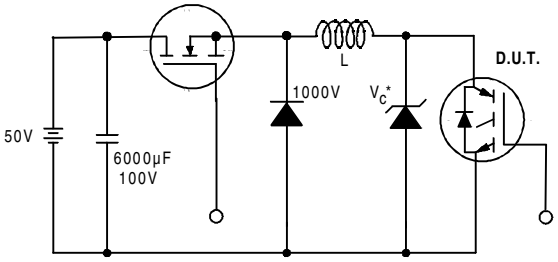


Figure 19. Clamped Inductive Load Test Circuit

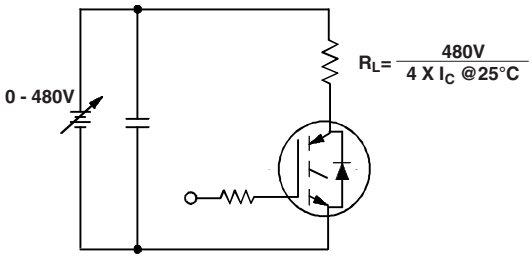


Figure 20. Pulsed Collector Current Test Circuit

Notes:

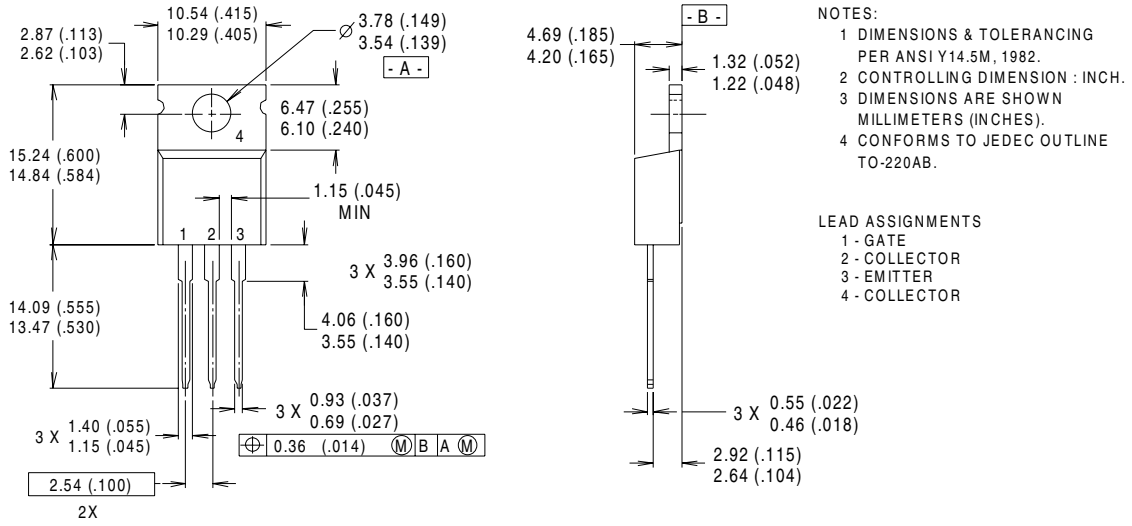
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

②V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 100W (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB

Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

Data and specifications subject to change without notice. 4/00

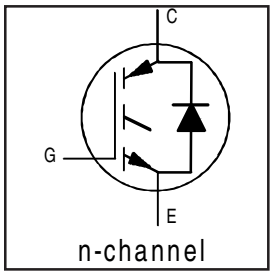
PD -91750A

International
IOR Rectifier

IRG4IBC20FD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Fast CoPack IGBT



n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.66V

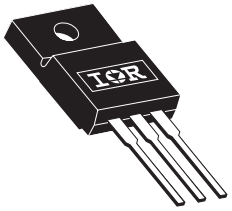
@V_{GE} = 15V, I_C = 9.0A

Features

- Very Low 1.66V votage drop
- 2.5kV, 60s insulation voltage ⑤
- 4.8 mm creapage distance to heatsink
- Fast: Optimized for medium operating frequencies (1-5 kHz in hard switching, >20 kHz in resonant mode).
- IGBT co-packaged with HEXFRED™ ultrafast, ultrasoft recovery antiparallel diodes
- Tighter parameter distribution
- Industry standard Isolated TO-220 Fullpak™ outline

Benefits

- Simplified assembly
- Highest efficiency and power density
- HEXFRED™ antiparallel Diode minimizes switching losses and EMI


TO-220 FULLPAK

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	14.3	A
I_C @ T_C = 100°C	Continuous Collector Current	7.7	
I_{CM}	Pulsed Collector Current ①	64	
I_{LM}	Clamped Inductive Load Current ②	64	
I_F @ T_C = 100°C	Diode Continuous Forward Current	6.5	
I_{FM}	Diode Maximum Forward Current	64	
Visol	RMS Isolation Voltage, Terminal to Case⑤	2500	V
V_{GE}	Gate-to-Emitter Voltage	± 20	
P_D @ T_C = 25°C	Maximum Power Dissipation	34	W
P_D @ T_C = 100°C	Maximum Power Dissipation	14	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	3.7	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	5.1	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	65	
Wt	Weight	2.0 (0.07)	—	g (oz)

4/24/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.72	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.66	2.0	V	I_C = 9.0A V_{GE} = 15V
		—	2.06	—		I_C = 16A See Fig. 2, 5
		—	1.76	—		I_C = 9.0A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	2.9	5.1	—	S	V_{CE} = 100V, I_C = 9.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1700		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 8.0A See Fig. 13
		—	1.3	1.6		I_C = 8.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	27	40	nC	I_C = 9.0A
Qge	Gate - Emitter Charge (turn-on)	—	4.2	6.2		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	9.9	15		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	43	—	ns	T_J = 25°C
t_r	Rise Time	—	20	—		I_C = 9.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	240	360		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	150	220		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	0.25	—	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	0.64	—		See Fig. 9, 10, 18
E_{ts}	Total Switching Loss	—	0.89	1.3		
$t_{d(on)}$	Turn-On Delay Time	—	41	—	ns	T_J = 150°C, See Fig. 11, 18
t_r	Rise Time	—	22	—		I_C = 9.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	320	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	290	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	1.35	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	540	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	37	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	7.0	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	37	55	ns	T_J = 25°C See Fig.
		—	55	90		T_J = 125°C 14 I_F = 8.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	5.0	A	T_J = 25°C See Fig.
		—	4.5	8.0		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	65	138	nC	T_J = 25°C See Fig.
		—	124	360		T_J = 125°C 16 di/dt = 200Aµs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	240	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	210	—		T_J = 125°C 17

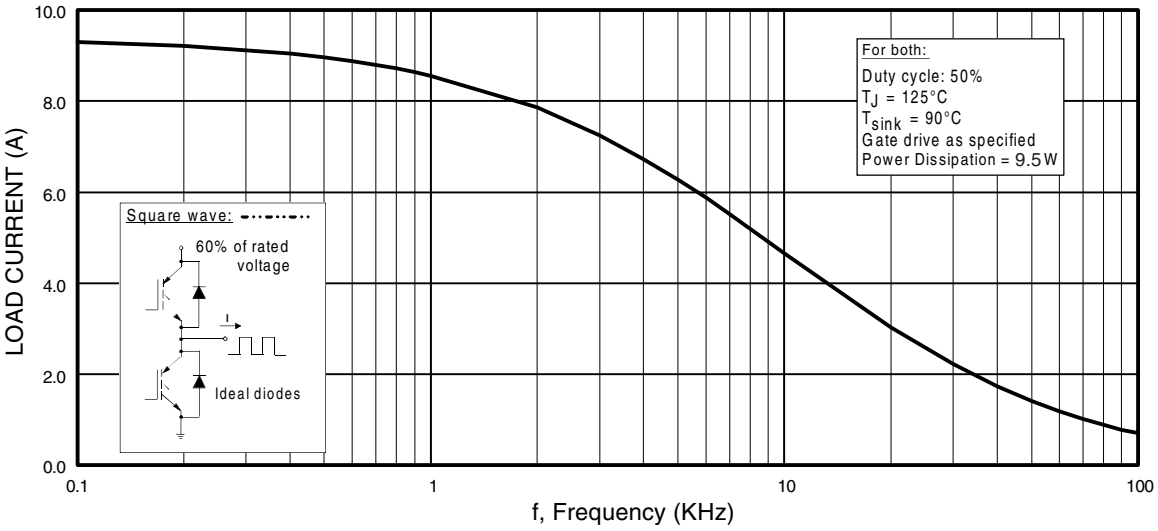


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

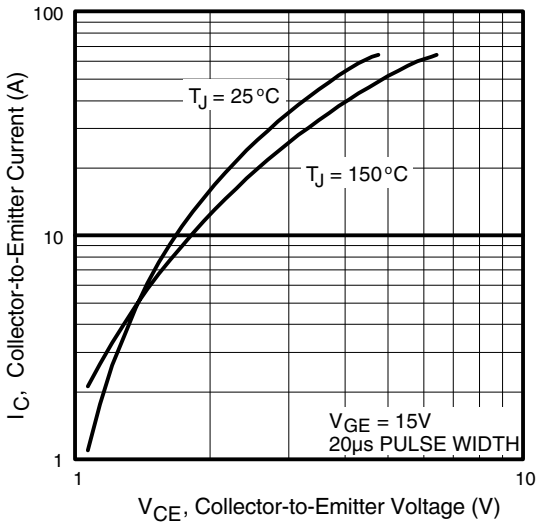


Fig. 2 - Typical Output Characteristics

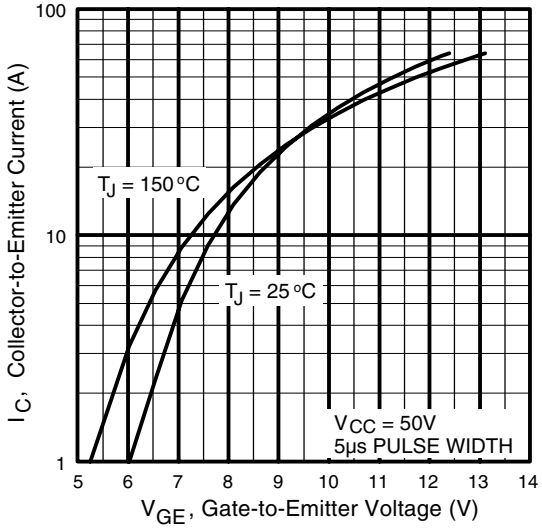


Fig. 3 - Typical Transfer Characteristics

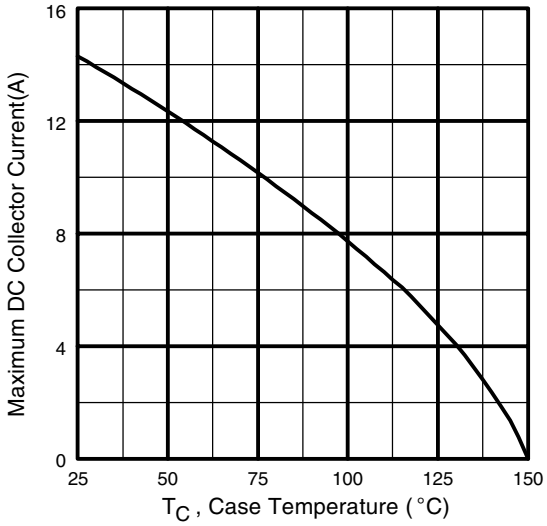


Fig. 4 - Maximum Collector Current vs. Case Temperature

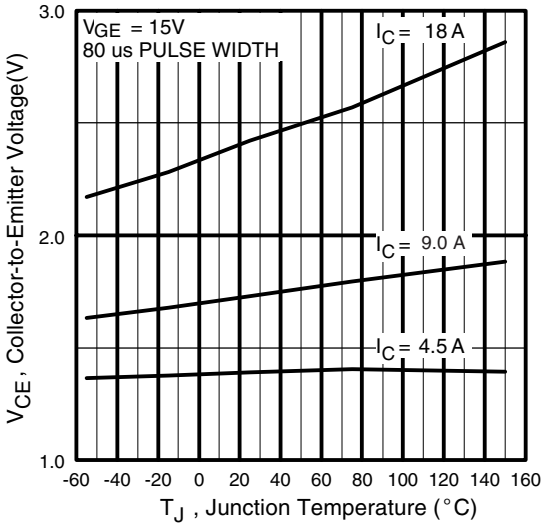


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

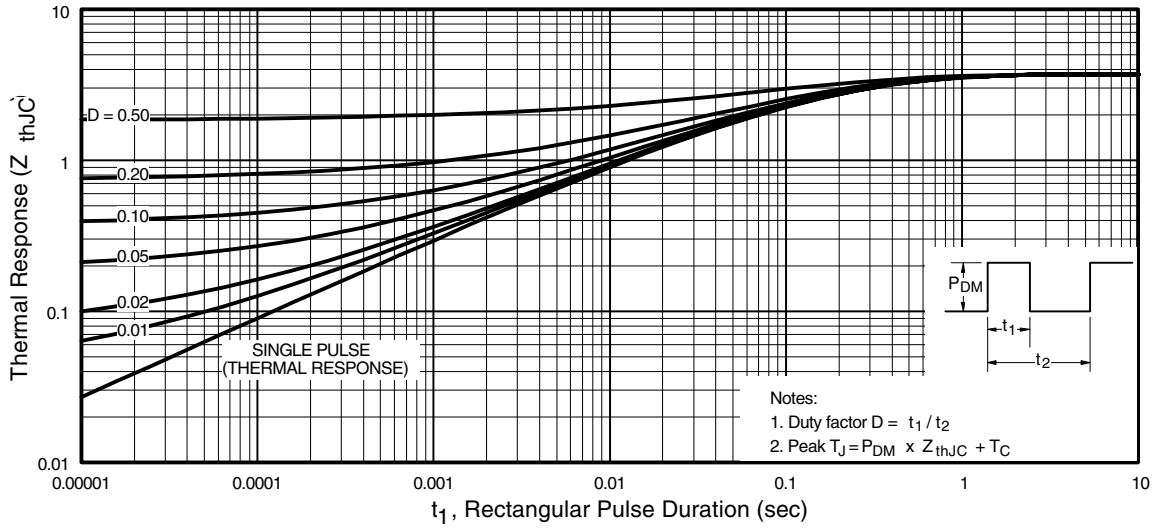


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

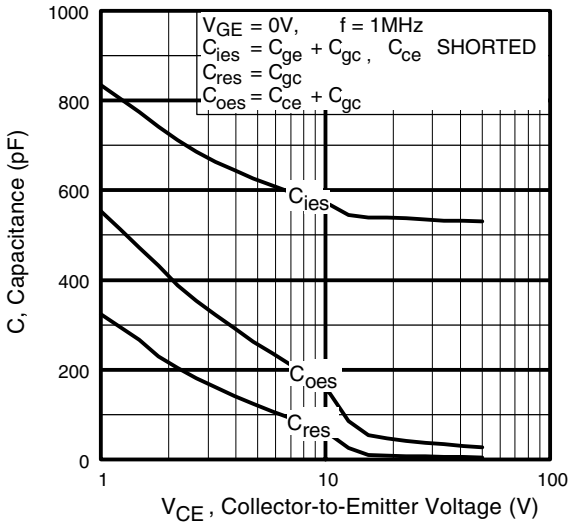


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

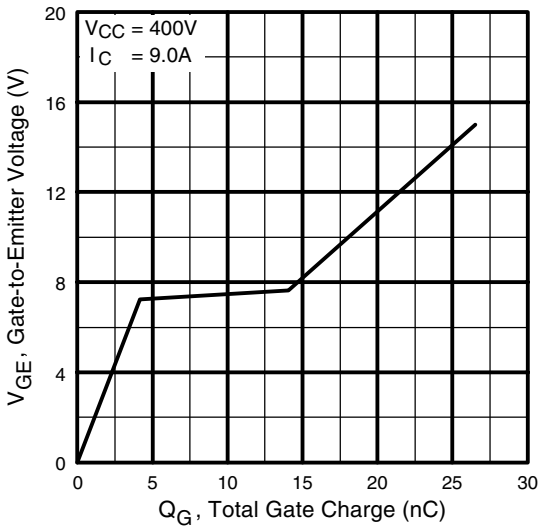


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

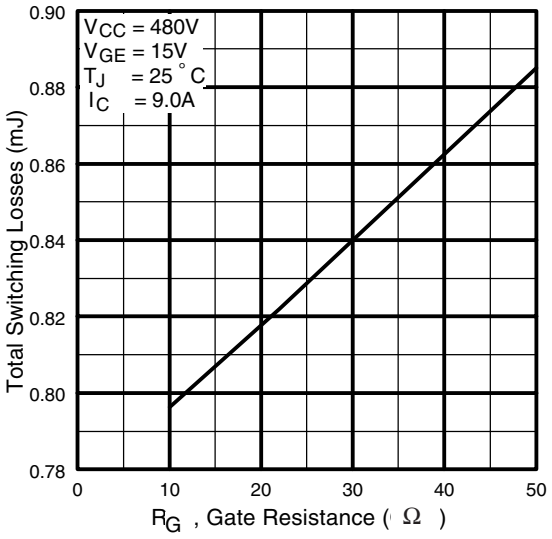


Fig. 9 - Typical Switching Losses vs. Gate Resistance

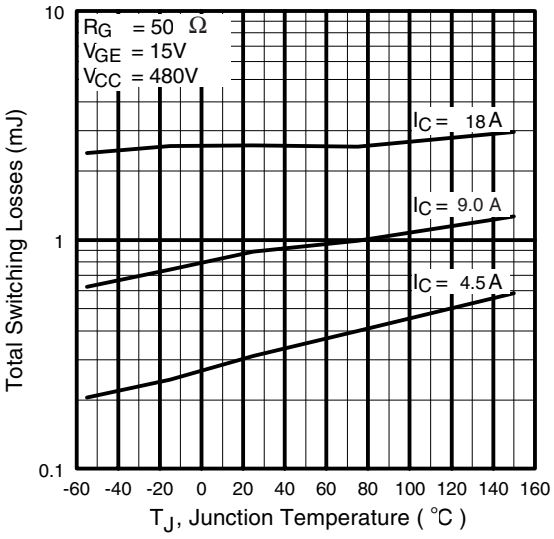


Fig. 10 - Typical Switching Losses vs. Junction Temperature

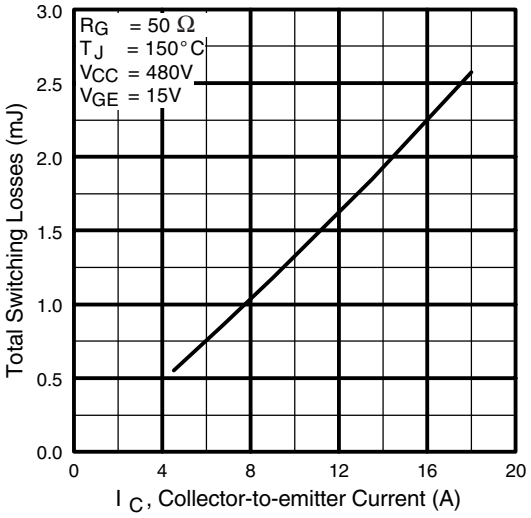


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

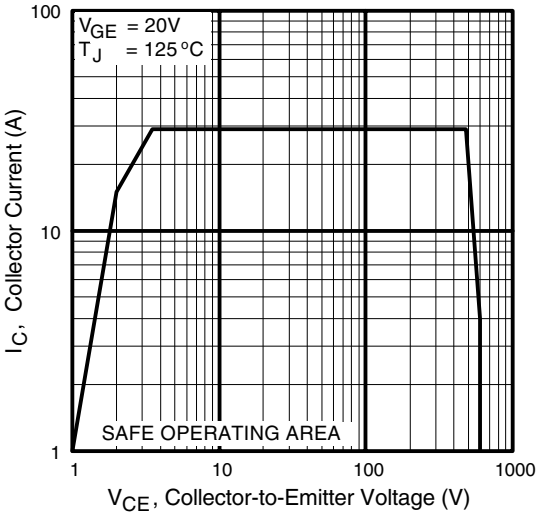


Fig. 12 - Turn-Off SOA

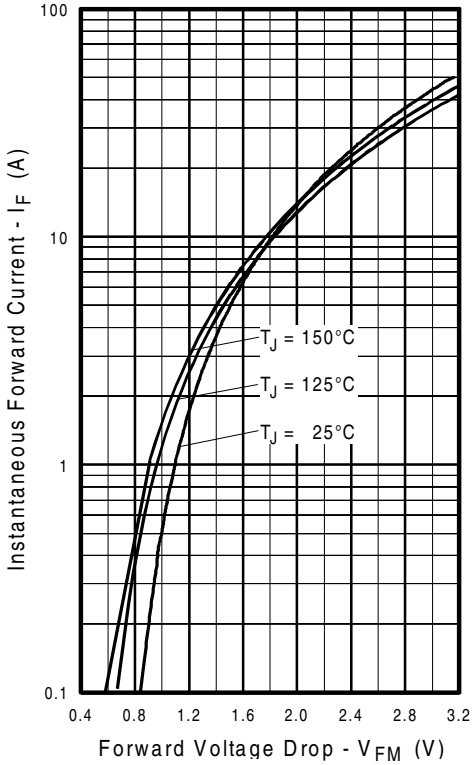


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

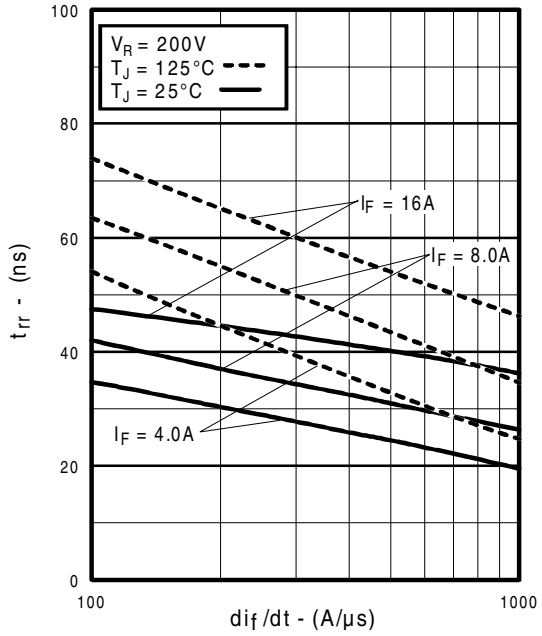


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

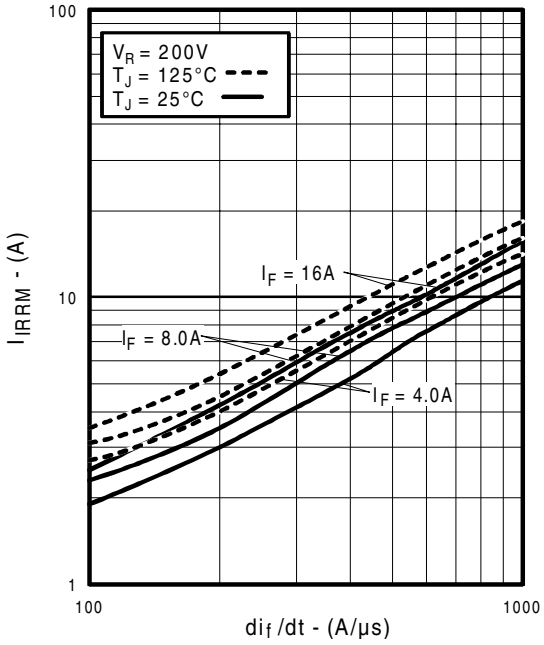


Fig. 15 - Typical Recovery Current vs. di_f/dt

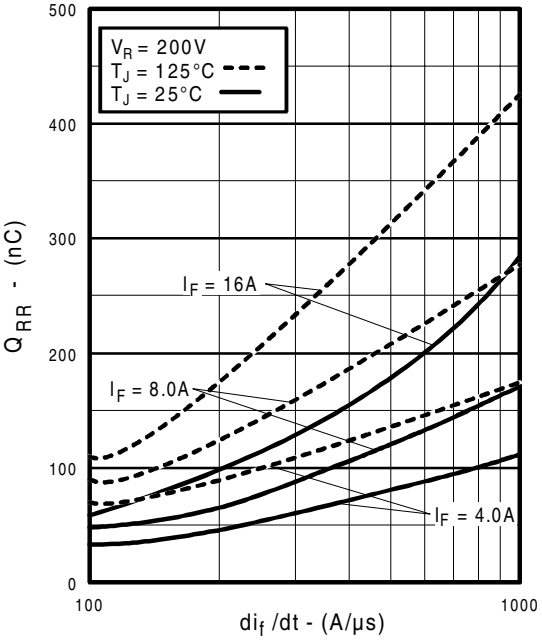


Fig. 16 - Typical Stored Charge vs. di_f/dt

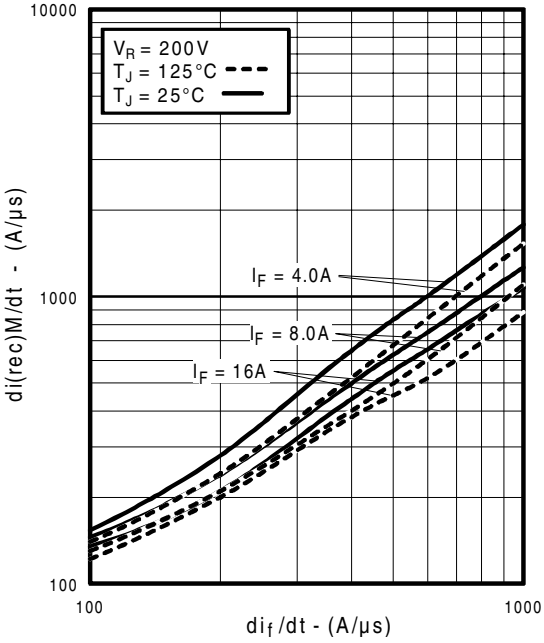


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

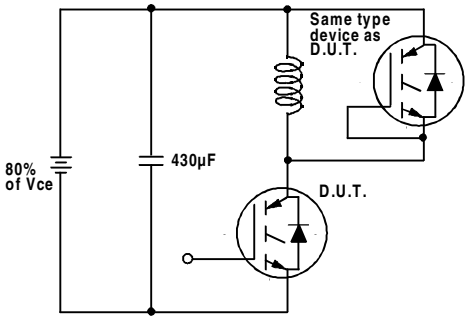


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

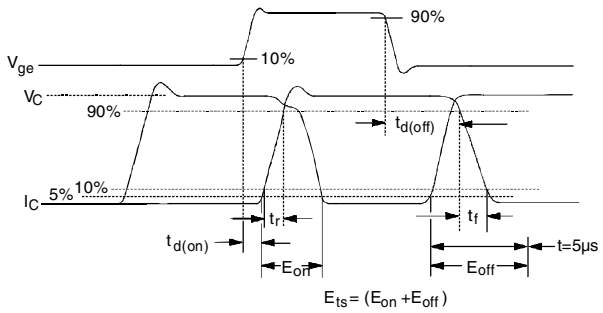


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

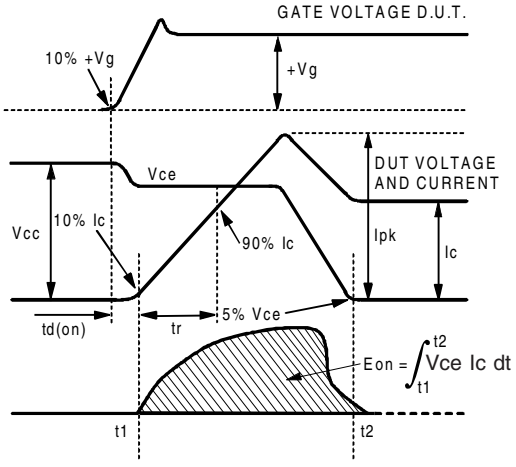


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

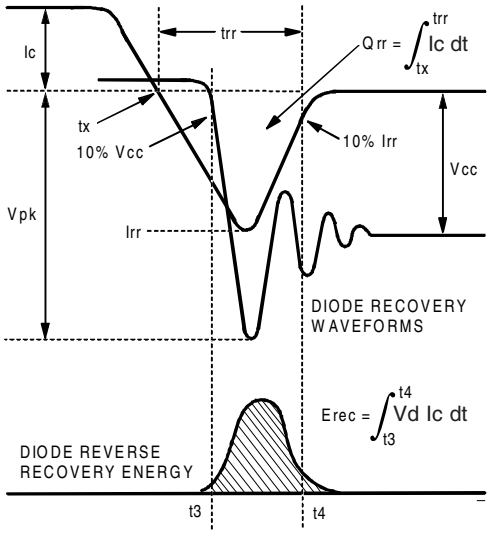


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

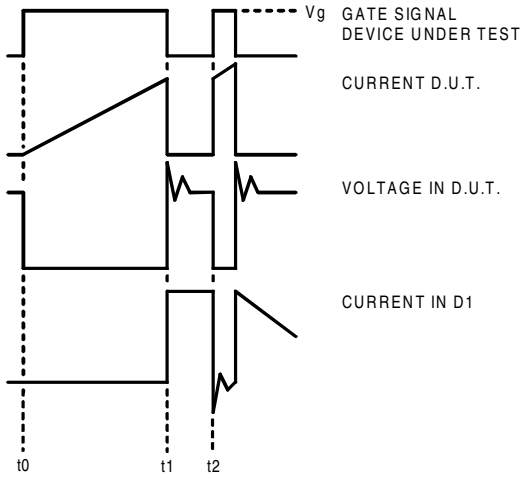


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

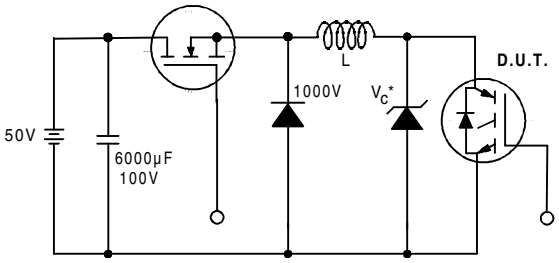


Figure 19. Clamped Inductive Load Test Circuit

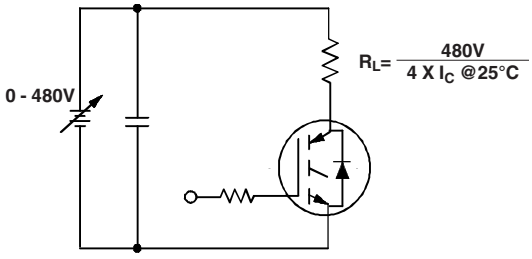


Figure 20. Pulsed Collector Current Test Circuit

Notes:

① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

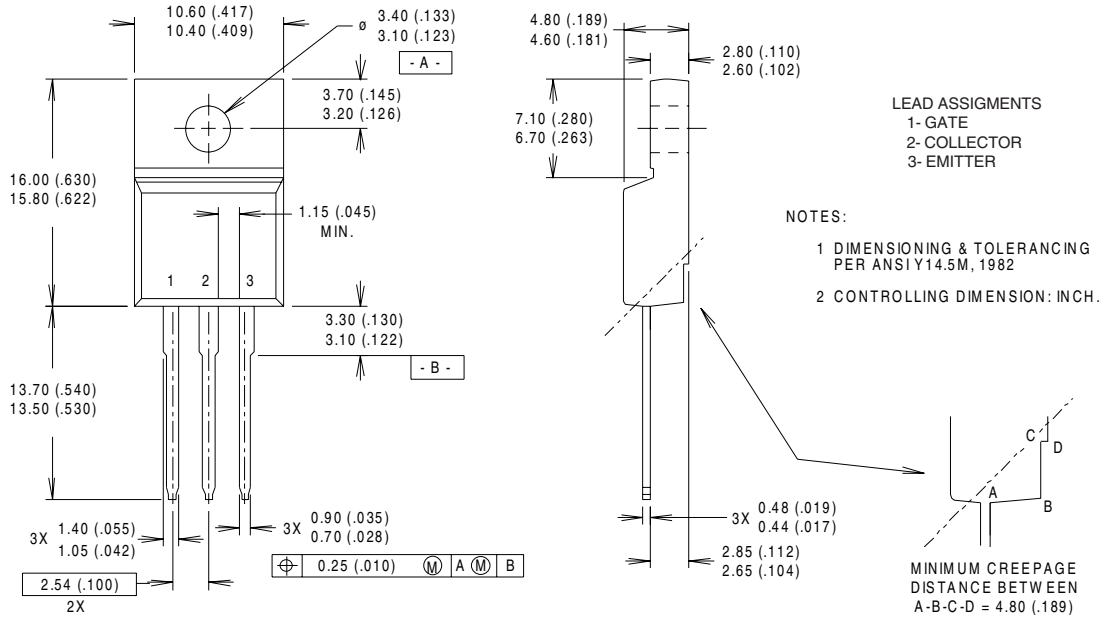
② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 50Ω (figure 19)

③ Pulse width £ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

⑤ t = 60s, f = 60Hz

Case Outline — TO-220 FULLPAK



International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

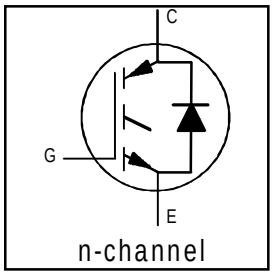
PD -91783A

International
IOR Rectifier

IRG4BC20FD-S

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Fast CoPack IGBT



n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.66V

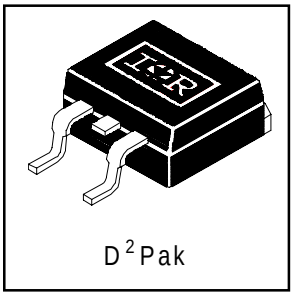
@V_{GE} = 15V, I_C = 9.0A

Features

- Fast: Optimized for medium operating frequencies (1-5 kHz in hard switching, >20 kHz in resonant mode).
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard D^2Pak package

Benefits

- Generation 4 IGBTs offer highest efficiencies available
- IGBTs optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBTs . Minimized recovery characteristics require less/no snubbing
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs


D^2Pak

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	16	A
I_C @ T_C = 100°C	Continuous Collector Current	9.0	
I_{CM}	Pulsed Collector Current ①	64	
I_{LM}	Clamped Inductive Load Current ②	64	
I_F @ T_C = 100°C	Diode Continuous Forward Current	8.0	
I_{FM}	Diode Maximum Forward Current	60	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	2.1	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	3.5	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted,steady-state)*	—	80	
Wt	Weight	1.44	—	g (oz)

* When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.72	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.66	2.0	V	I_C = 9.0A V_{GE} = 15V
		—	2.06	—		I_C = 16A See Fig. 2, 5
		—	1.76	—		I_C = 9.0A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	2.9	5.1	—	S	V_{CE} = 100V, I_C = 9.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1700		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 8.0A See Fig. 13
		—	1.3	1.6		I_C = 8.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	27	40	nC	I_C = 9.0A
Qge	Gate - Emitter Charge (turn-on)	—	4.2	6.2		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	9.9	15		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	43	—	ns	T_J = 25°C
t_r	Rise Time	—	20	—		I_C = 9.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	240	360		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	150	220		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	0.25	—	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	0.64	—		See Fig. 9, 10, 18
E_{ts}	Total Switching Loss	—	0.89	1.3		
$t_{d(on)}$	Turn-On Delay Time	—	41	—	ns	T_J = 150°C, See Fig. 10, 11, 18
t_r	Rise Time	—	22	—		I_C = 9.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	320	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	290	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	1.35	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	540	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	37	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	7.0	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	37	55	ns	T_J = 25°C See Fig.
		—	55	90		T_J = 125°C 14 I_F = 8.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	5.0	A	T_J = 25°C See Fig.
		—	4.5	8.0		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	65	138	nC	T_J = 25°C See Fig.
		—	124	360		T_J = 125°C 16 di/dt = 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	240	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	210	—		T_J = 125°C 17

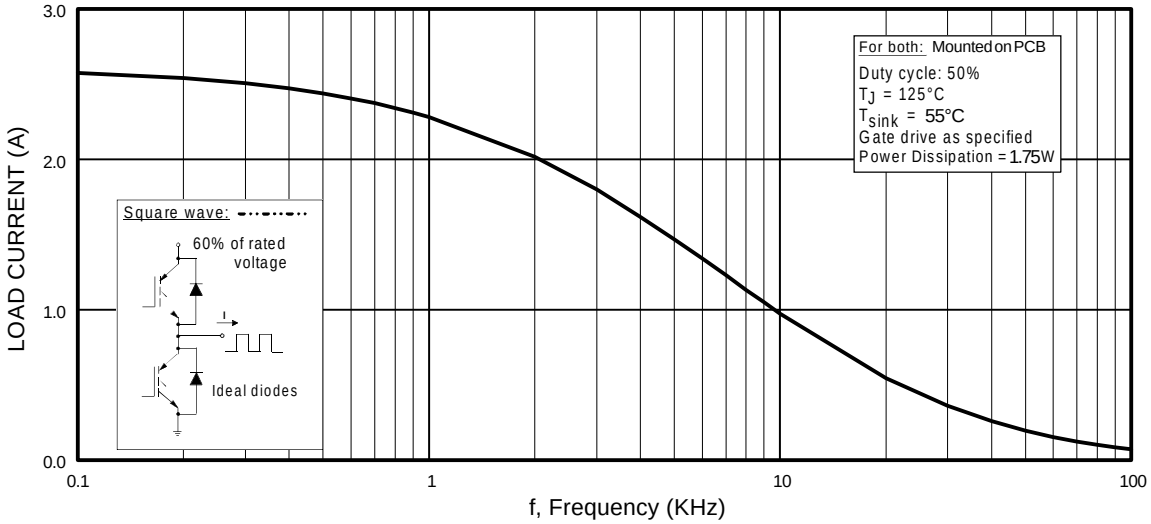


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

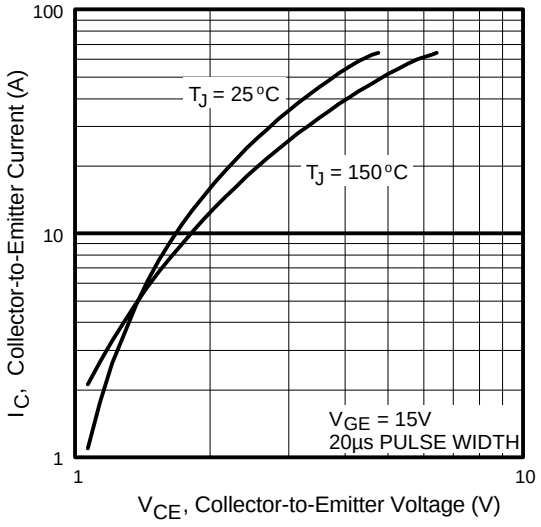


Fig. 2 - Typical Output Characteristics

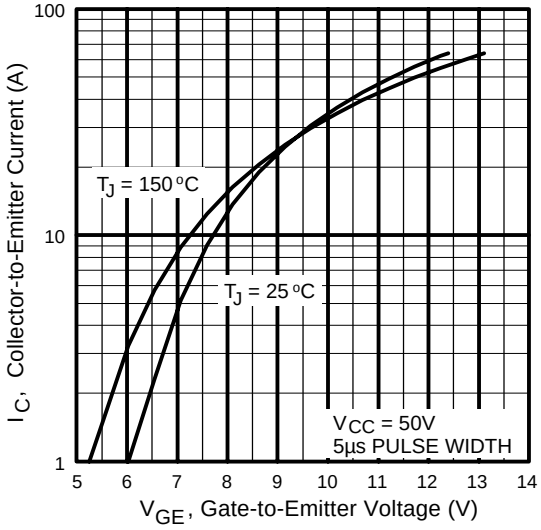


Fig. 3 - Typical Transfer Characteristics

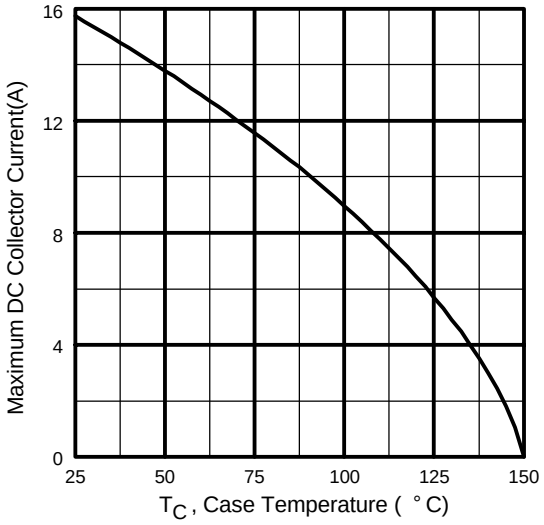


Fig. 4 - Maximum Collector Current vs. Case Temperature

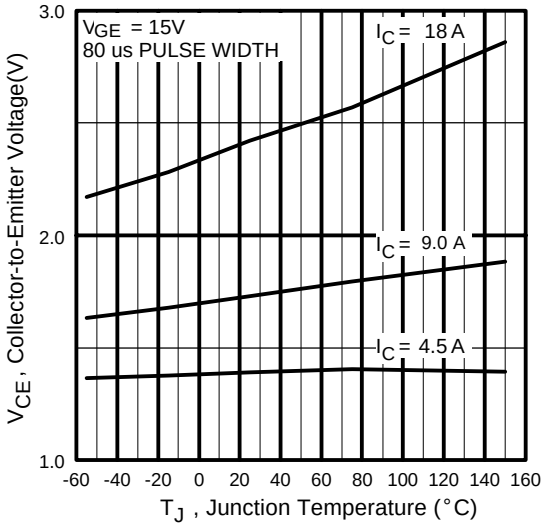


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

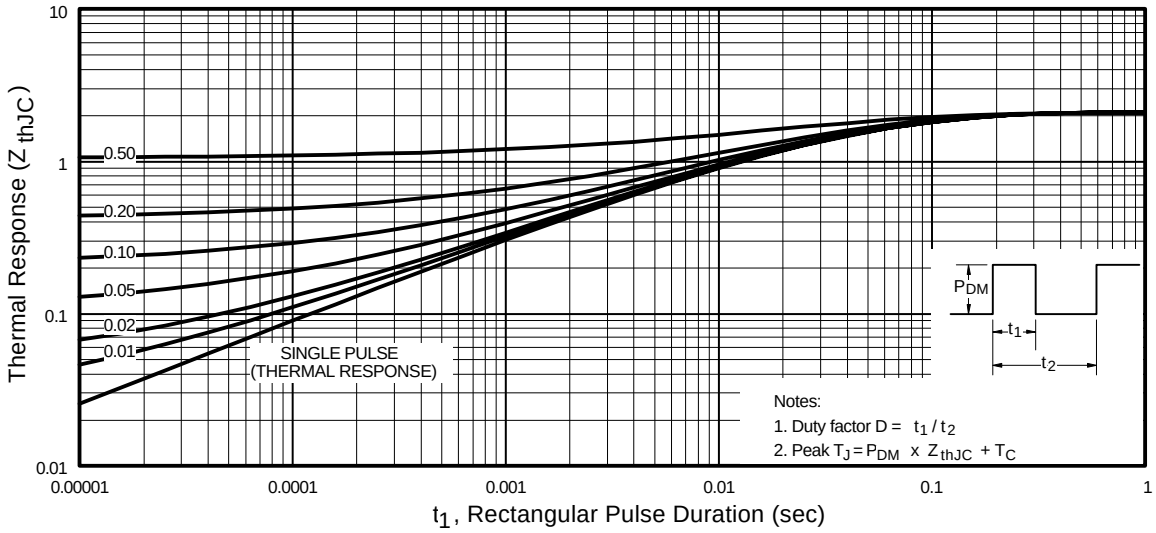


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

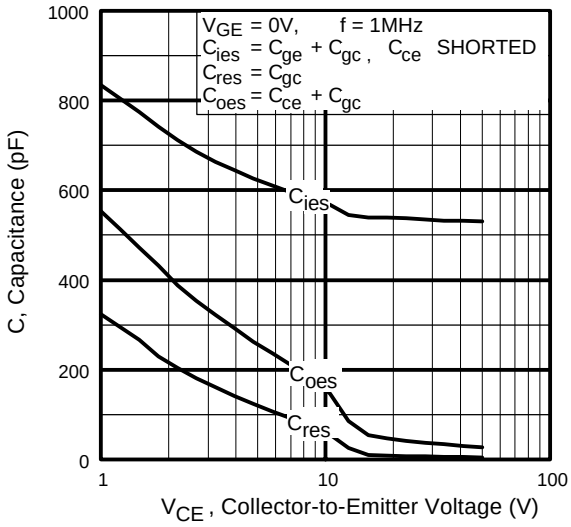


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

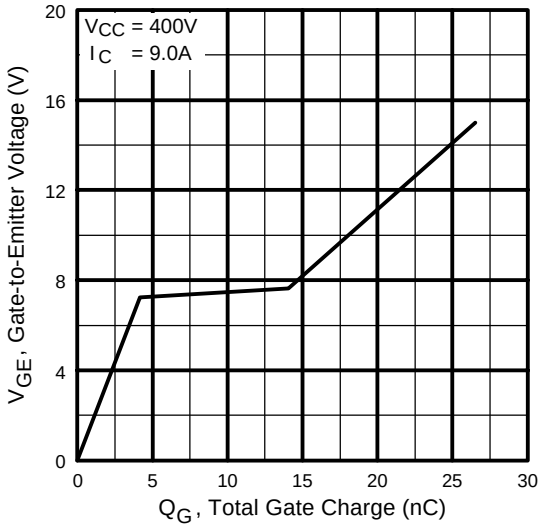


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

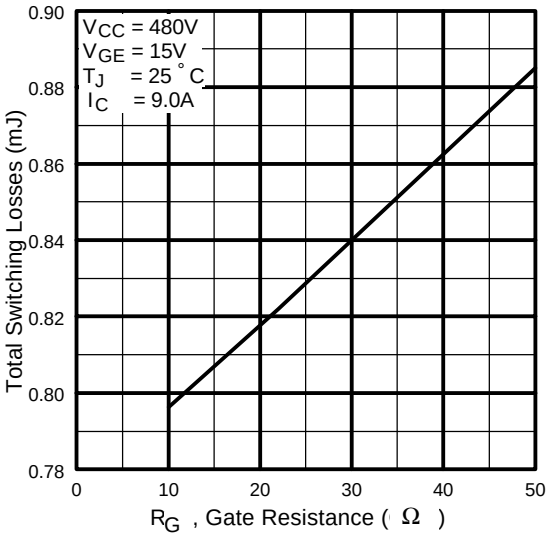


Fig. 9 - Typical Switching Losses vs. Gate Resistance

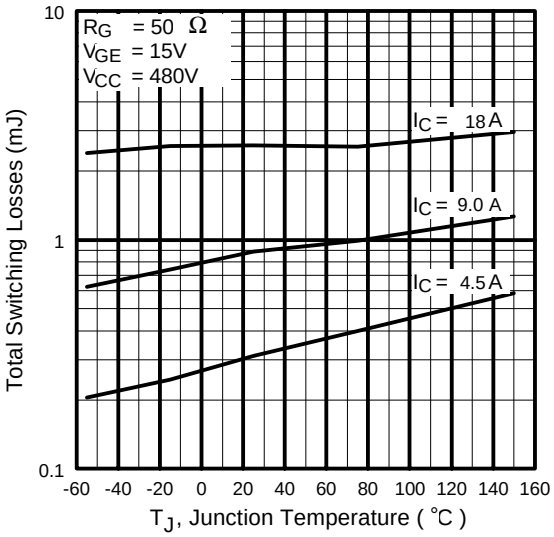


Fig. 10 - Typical Switching Losses vs. Junction Temperature

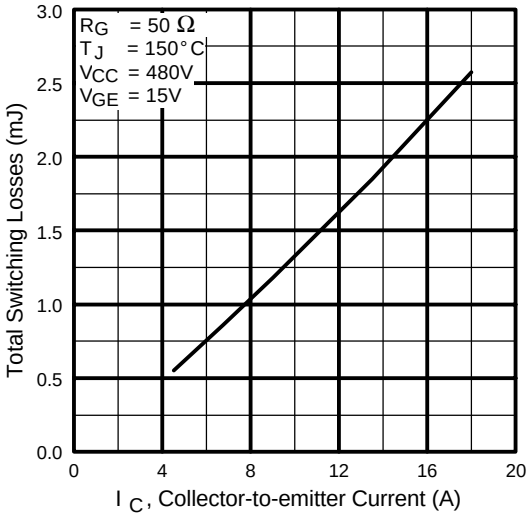


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

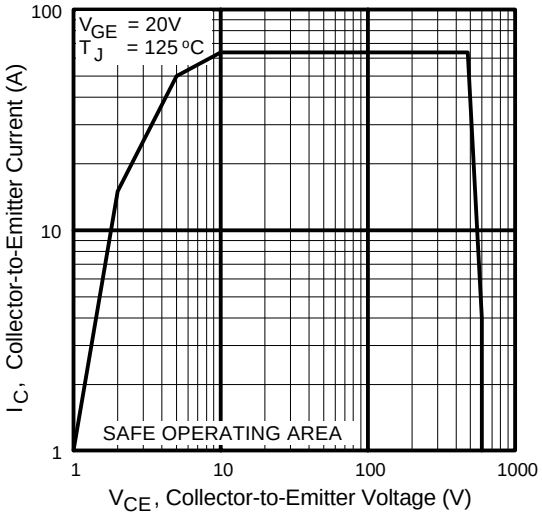


Fig. 12 - Turn-Off SOA

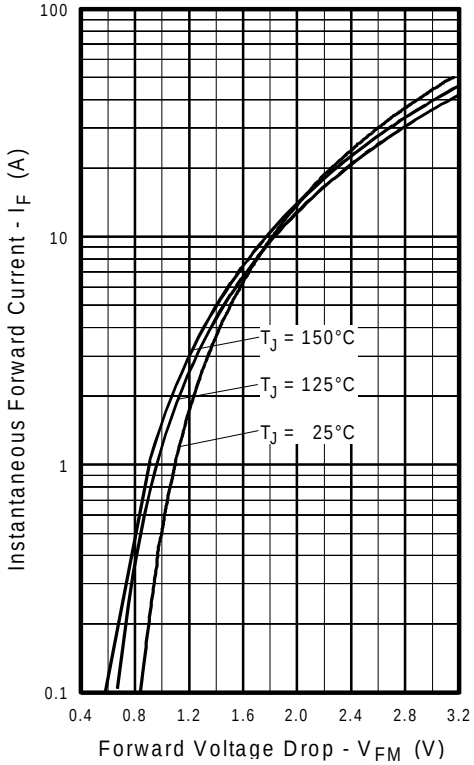


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

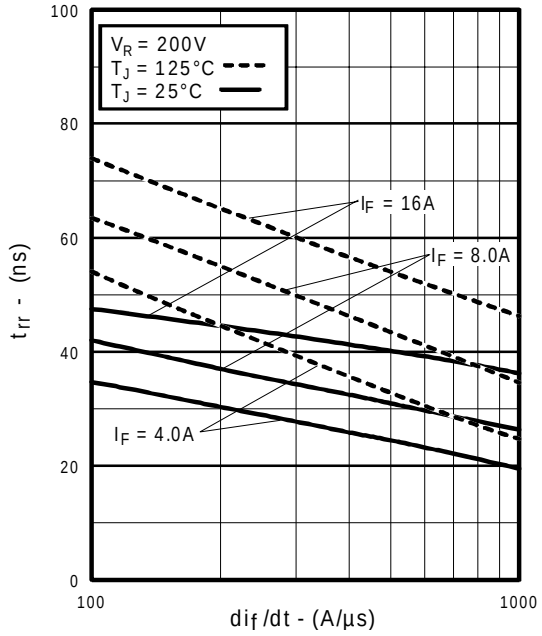


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

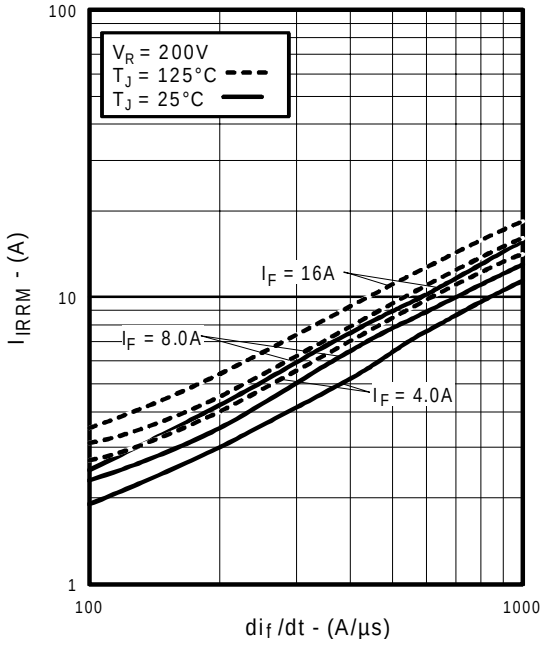


Fig. 15 - Typical Recovery Current vs. di_f/dt

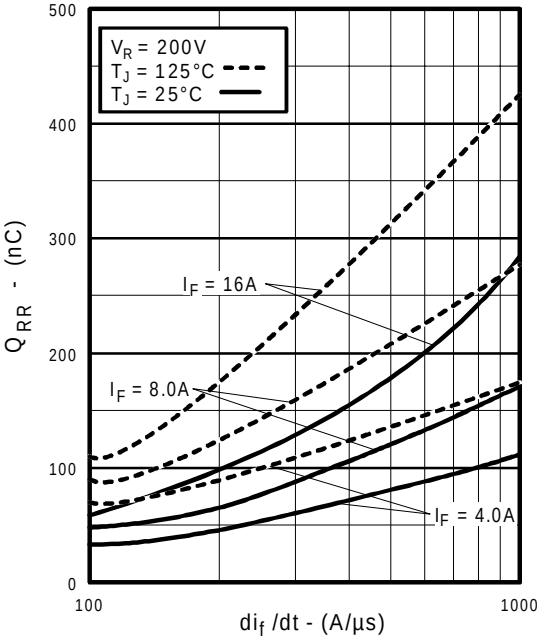


Fig. 16 - Typical Stored Charge vs. di_f/dt

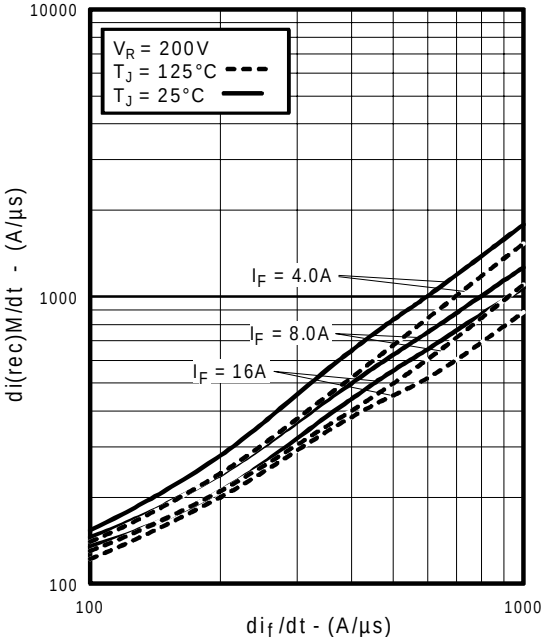


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

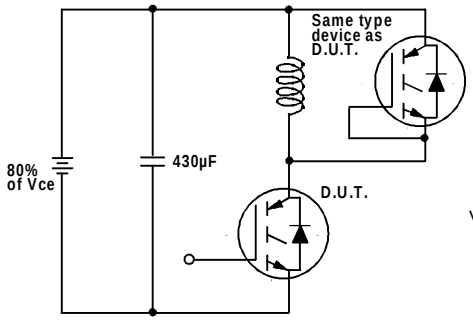


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

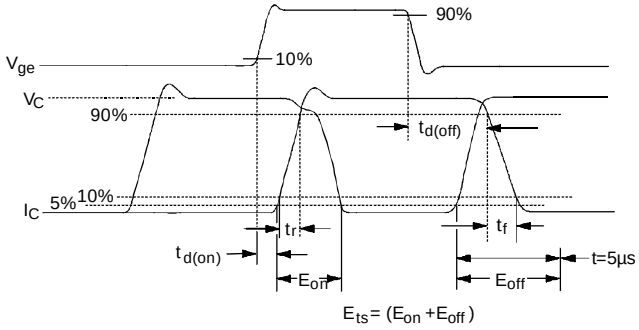


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

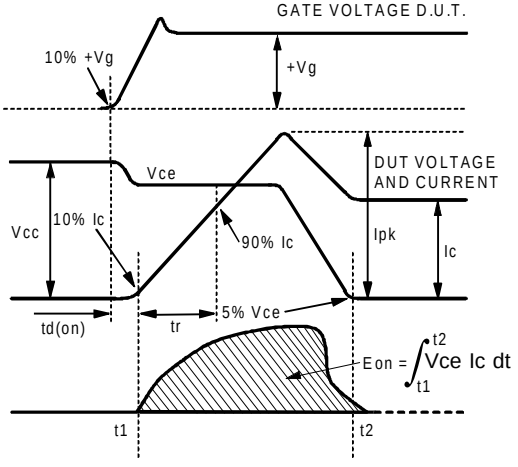


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

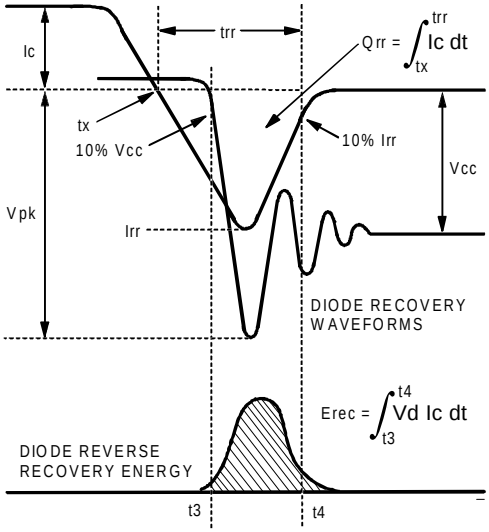


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

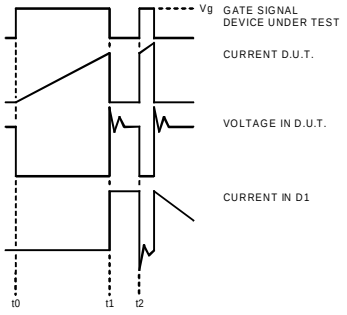


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

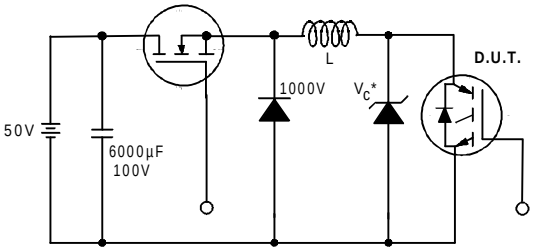


Figure 19. Clamped Inductive Load Test Circuit

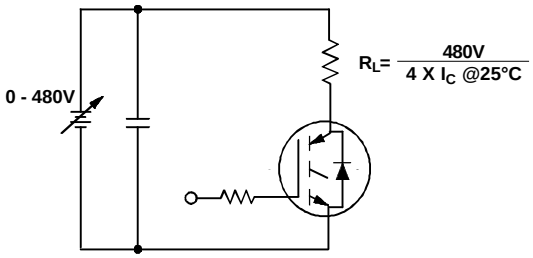
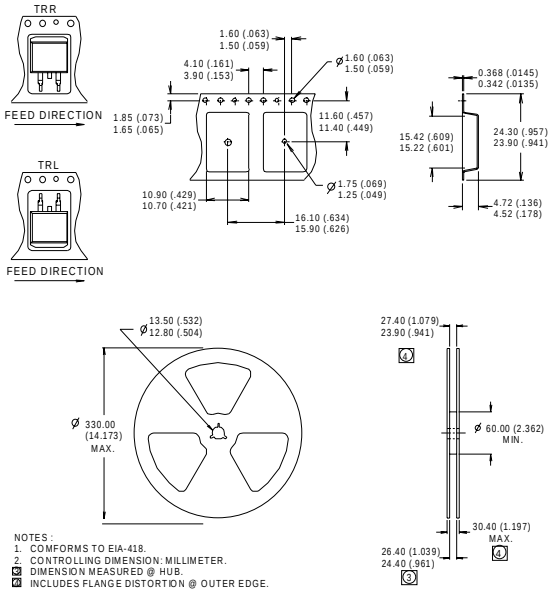


Figure 20. Pulsed Collector Current Test Circuit

Tape & Reel Information

D^2Pak



Notes:

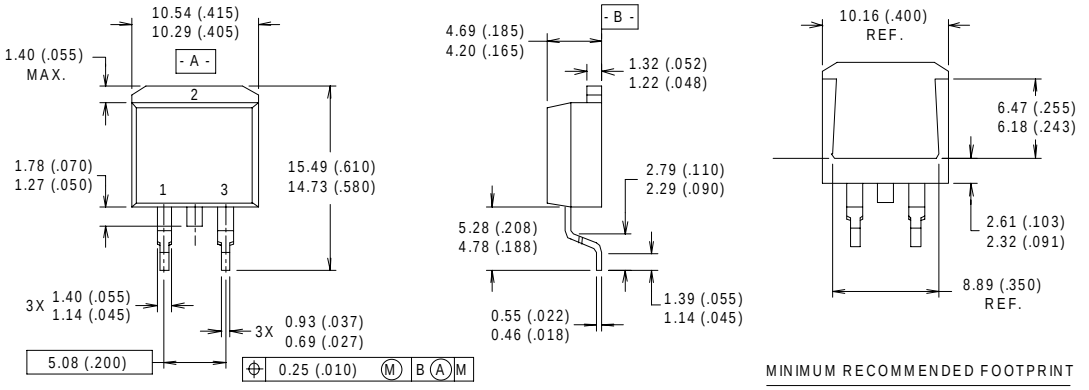
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 50Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

D²Pak Package Outline



NOTES:

1 DIMENSIONS AFTER SOLDER DIP.

2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.

3 CONTROLLING DIMENSION : INCH.

4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

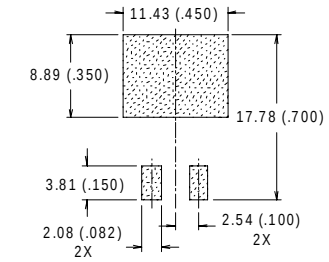
LEAD ASSIGNMENTS

1 - GATE

2 - DRAIN

3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT



International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

Data and specifications subject to change without notice. 4/00

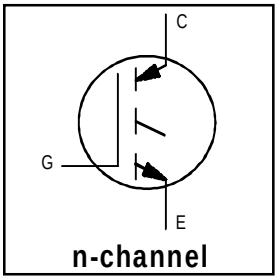
PD - 91620A

International
IOR Rectifier

IRG4BC20K-S

Short Circuit Rated
UltraFast IGBT

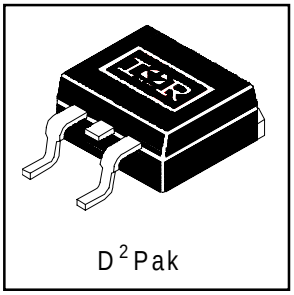
INSULATED GATE BIPOLAR TRANSISTOR



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.27V

@V_{GE} = 15V, I_C = 9.0A



D²Pak

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, @360V V_{CE} (start), T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Latest generation design provides tighter parameter distribution and higher efficiency than previous generations

Benefits

- As a Freewheeling Diode we recommend our HEXFRED™ ultrafast, ultrasoft recovery diodes for minimum EMI / Noise and switching losses in the Diode and IGBT
- Latest generation 4 IGBTs offer highest power density motor controls possible
- This part replaces the IRGBC20K-S and IRGBC20M-S devices

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	16	A
I_C @ T_C = 100°C	Continuous Collector Current	9.0	
I_{CM}	Pulsed Collector Current ①	32	
I_{LM}	Clamped Inductive Load Current ②	32	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	29	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted,steady-state)⑥	—	40	
Wt	Weight	1.44	—	g

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.49	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.00	—	V	I_C = 6.0A
		—	2.27	2.8		I_C = 9.0A V_{GE} = 15V
		—	3.01	—		I_C = 16A See Fig.2, 5
		—	2.43	—		I_C = 9.0A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	2.9	4.3	—	S	V_{CE} = 100 V, I_C = 9.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	34	51	nC	I_C = 9.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	4.9	7.4		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	14	21		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	28	—	ns	
t_r	Rise Time	—	27	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	150	220		I_C = 9.0A, V_{CC} = 480V
t_f	Fall Time	—	100	150		V_{GE} = 15V, R_G = 50Ω
E_{on}	Turn-On Switching Loss	—	0.15	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.25	—		See Fig. 9,10,14
E_{ts}	Total Switching Loss	—	0.40	0.6		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 400V, T_J = 125°C
						V_{GE} = 15V, R_G = 50Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	28	—	ns	T_J = 150°C,
t_r	Rise Time	—	29	—		I_C = 9.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	190	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	190	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.68	—	mJ	See Fig. 11,14
E_{on}	Turn-On Switching Loss	—	0.07	—	mJ	T_J = 25°C, V_{GE} = 15V, R_G = 50Ω
E_{off}	Turn-Off Switching Loss	—	0.13	—		I_C = 6.0A, V_{CC} = 480V
E_{ts}	Total Switching Loss	—	0.20	—		Energy losses include "tail"
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	450	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	61	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	14	—		f = 1.0MHz

Details of note ① through ⑥ are on the last page

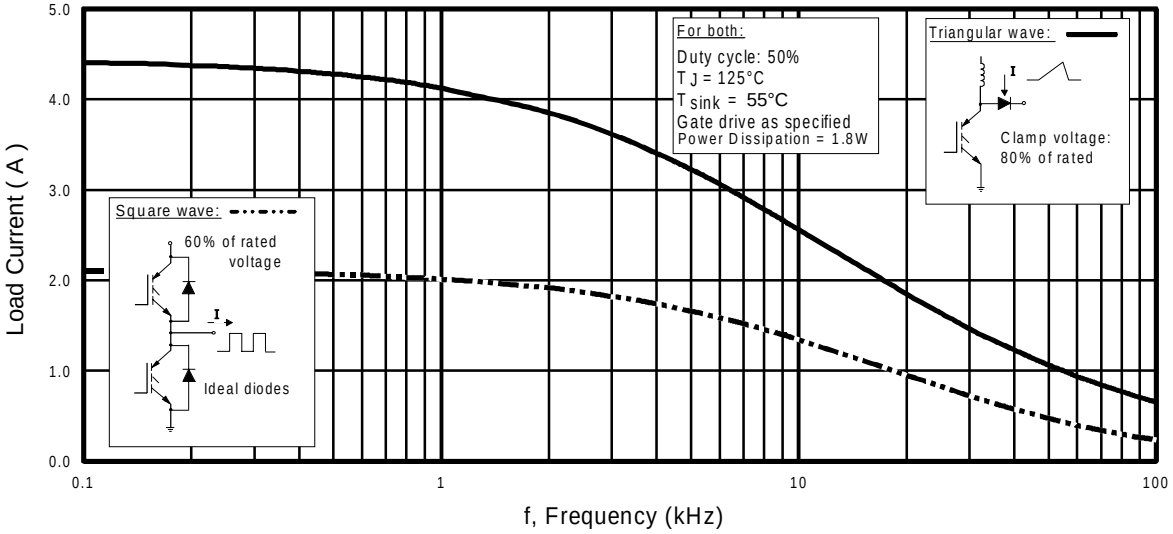


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

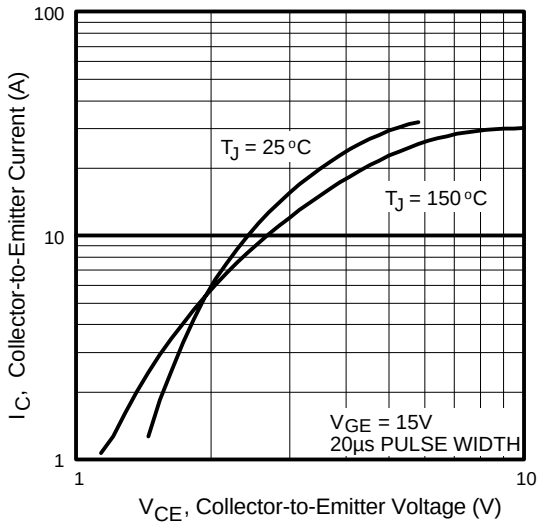


Fig. 2 - Typical Output Characteristics

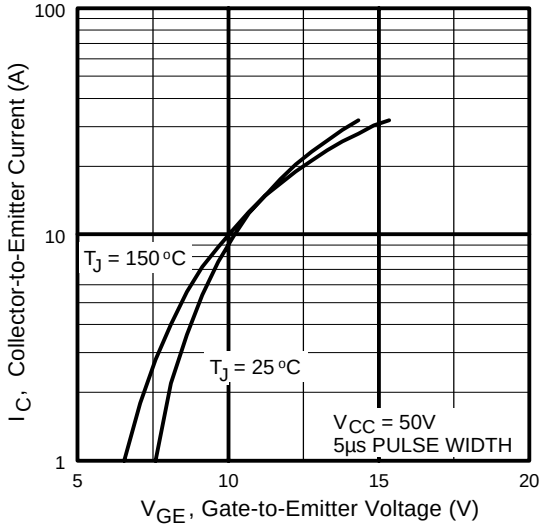


Fig. 3 - Typical Transfer Characteristics

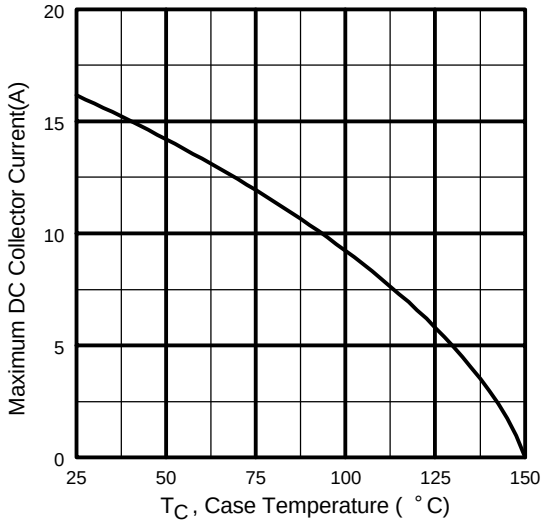


Fig. 4 - Maximum Collector Current vs. Case Temperature

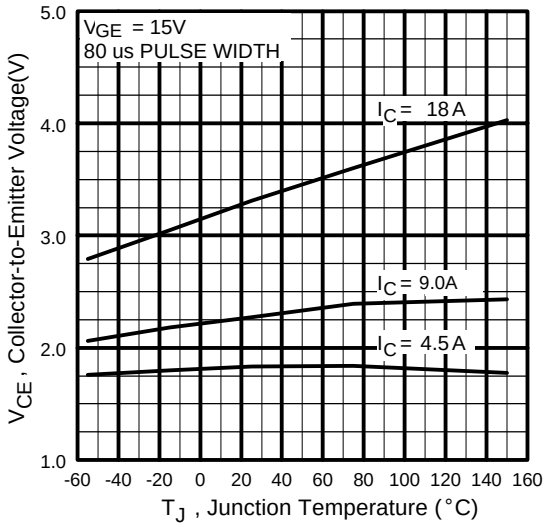


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

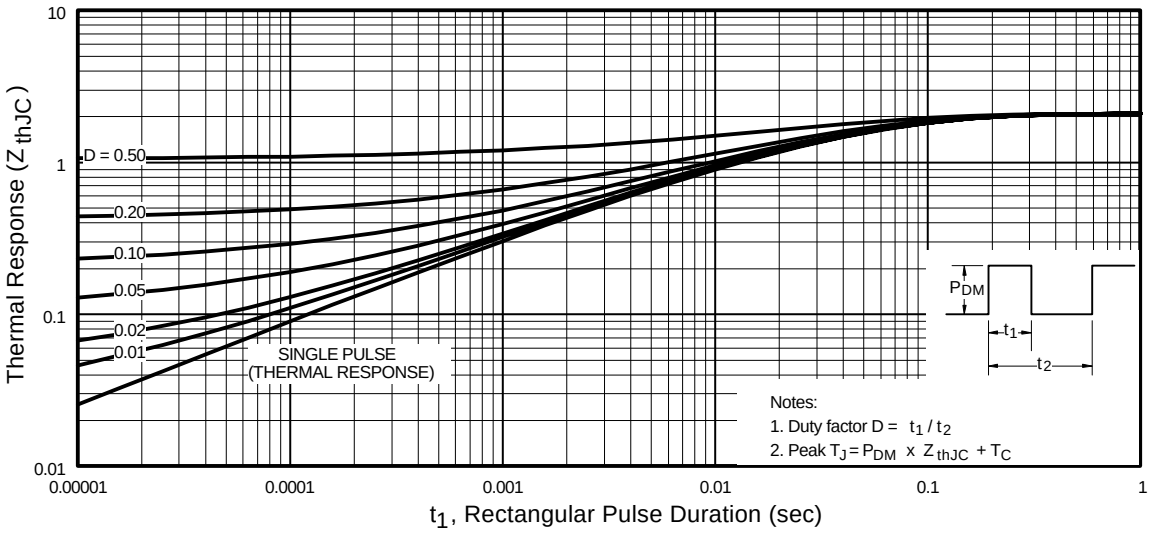


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

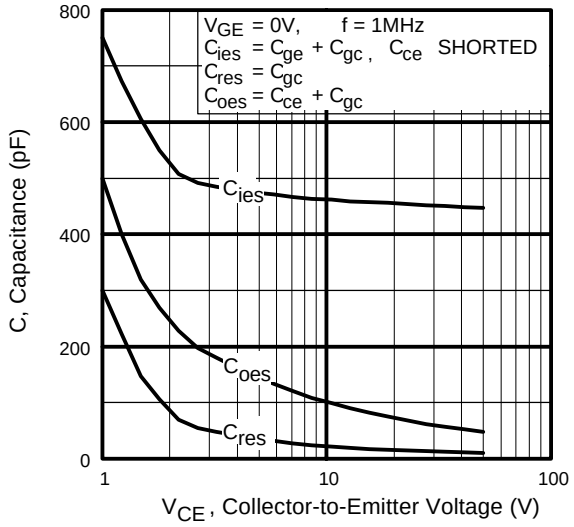


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

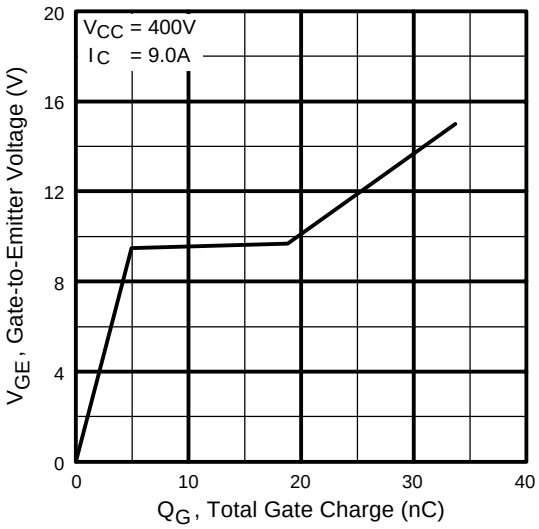


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

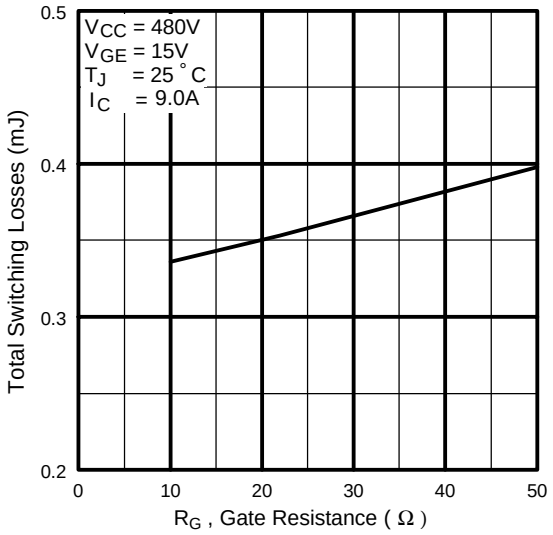


Fig. 9 - Typical Switching Losses vs. Gate Resistance

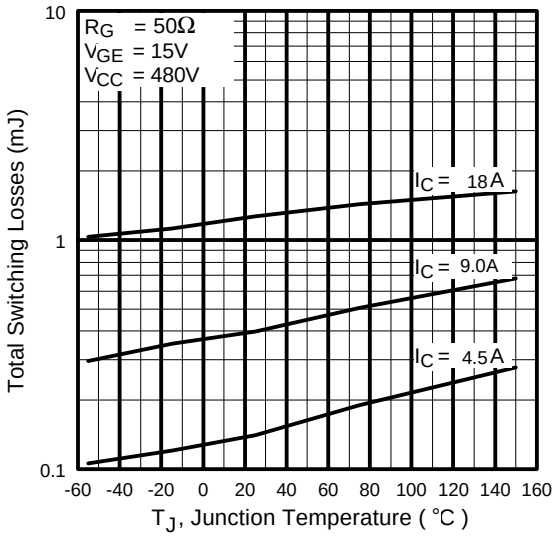


Fig. 10 - Typical Switching Losses vs. Junction Temperature

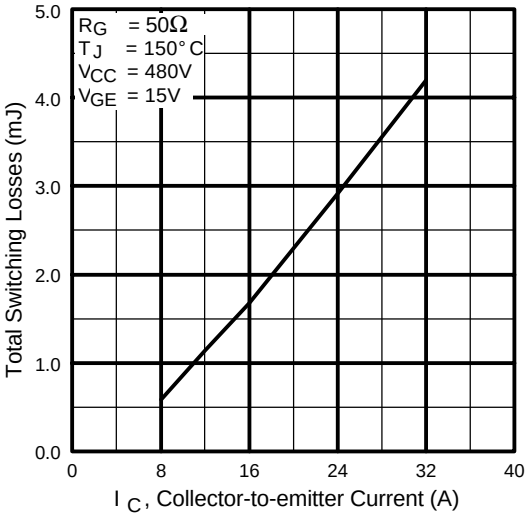


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

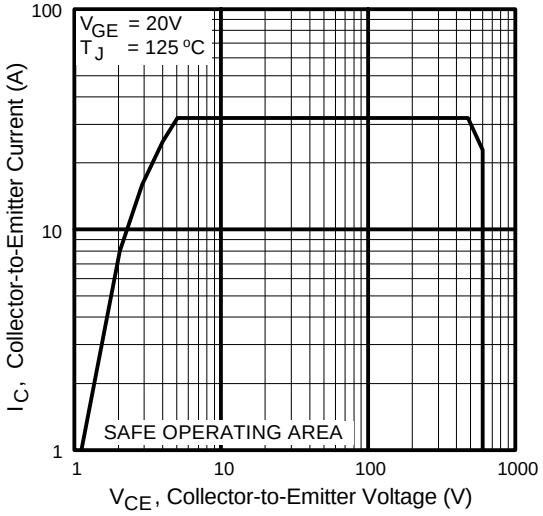
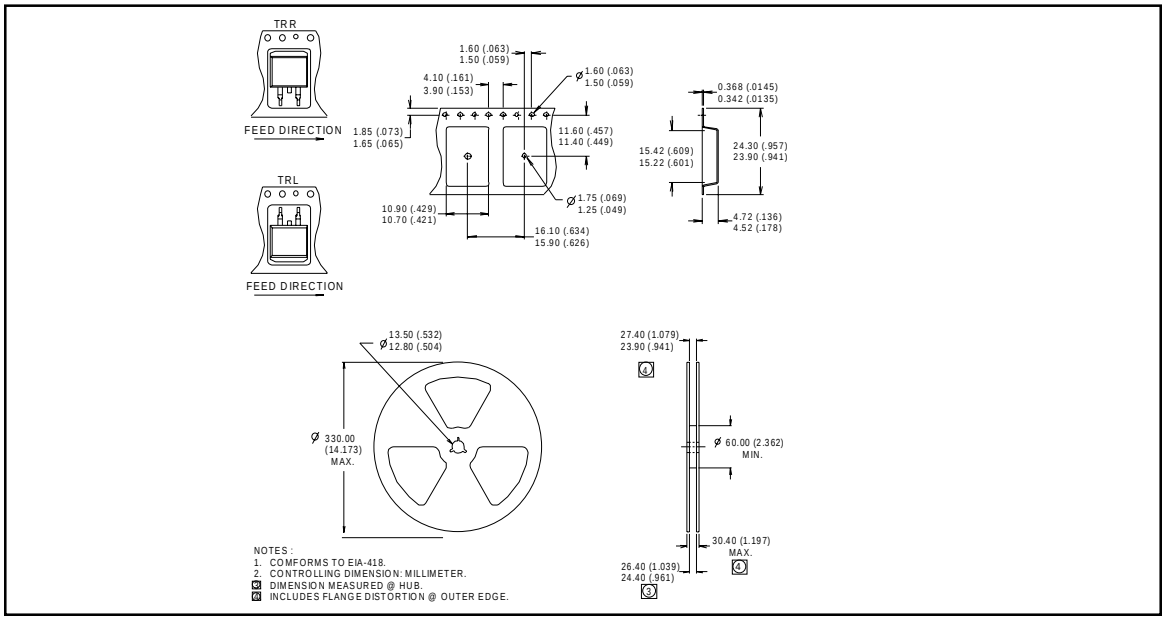


Fig. 12 - Turn-Off SOA

Tape & Reel Information

D²Pak



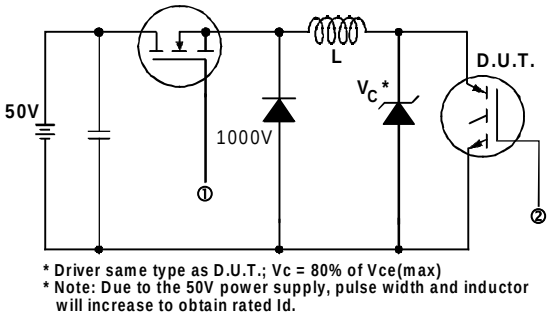


Fig. 13a - Clamped Inductive Load Test Circuit

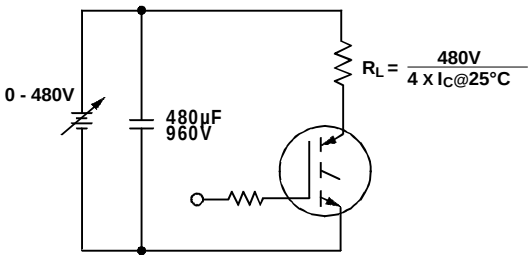


Fig. 13b - Pulsed Collector Current Test Circuit

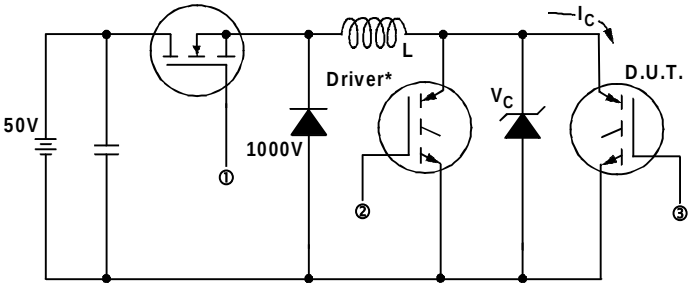


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

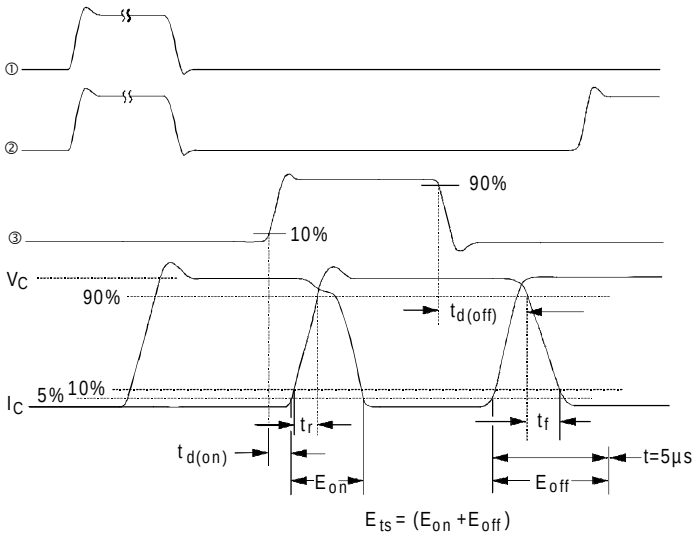


Fig. 14b - Switching Loss Waveforms

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 50Ω, (See fig. 13a)

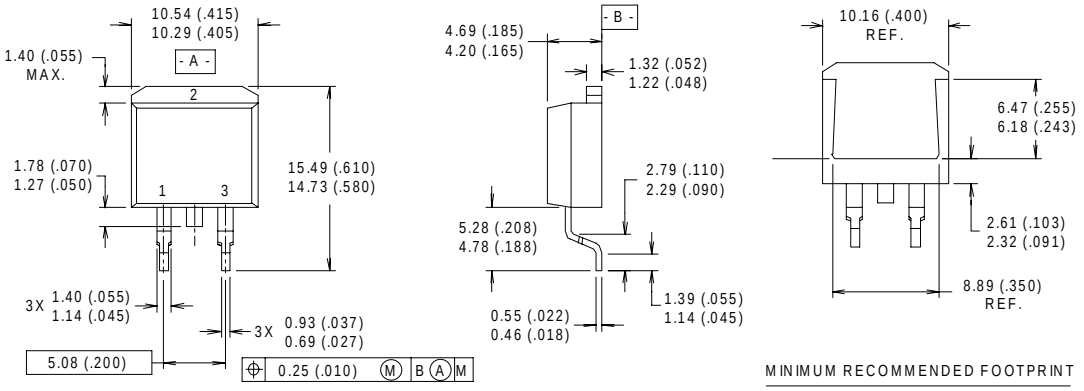
③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

⑥ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

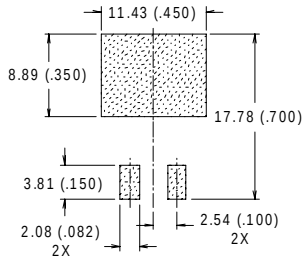
D²Pak Package Outline



NOTES:
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT



International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 10/00

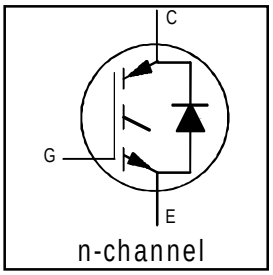
PD -91598A

International
IOR Rectifier

IRG4BC20KD-S

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

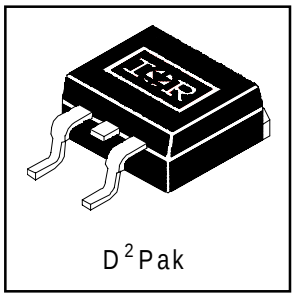
Short Circuit Rated UltraFast IGBT



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.27V

@V_{GE} = 15V, I_C = 9.0A



Features

- Short Circuit Rated UltraFast: Optimized for high operating frequencies >5.0 kHz , and Short Circuit Rated to 10µs @ 125°C, V_{GE} = 15V
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than previous generation
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard D²Pak package

Benefits

- Latest generation 4 IGBTs offer highest power density motor controls possible.
- HEXFRED™ diodes optimized for performance with IGBTs. Minimized recovery characteristics reduce noise, EMI and switching losses.
- This part replaces the IRGBC20KD2-S and IRGBC20MD2-S products.
- For hints see design tip 97003.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	16	A
I_C @ T_C = 100°C	Continuous Collector Current	9.0	
I_{CM}	Pulsed Collector Current ①	32	
I_{LM}	Clamped Inductive Load Current ②	32	
I_F @ T_C = 100°C	Diode Continuous Forward Current	7.0	
I_{FM}	Diode Maximum Forward Current	32	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	2.1	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode		2.5	
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted,steady-state)⑤	—	40	
Wt	Weight	1.44	—	g

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.49	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.27	2.8	V	I_C = 9.0A V_{GE} = 15V
		—	3.01	—		I_C = 16A See Fig. 2, 5
		—	2.43	—		I_C = 9.0A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	2.9	4.3	—	S	V_{CE} = 100V, I_C = 9.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 8.0A See Fig. 13
		—	1.3	1.6		I_C = 8.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	34	51	nC	I_C = 9.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	4.9	7.4		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	14	21		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	54	—	ns	
t_r	Rise Time	—	34	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	180	270		I_C = 9.0A, V_{CC} = 480V
t_f	Fall Time	—	72	110		V_{GE} = 15V, R_G = 50Ω
E_{on}	Turn-On Switching Loss	—	0.34	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.30	—		and diode reverse recovery
E_{ts}	Total Switching Loss	—	0.64	0.96		See Fig. 9,10,14
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 360V, T_J = 125°C
						V_{GE} = 15V, R_G = 50Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	51	—	ns	T_J = 150°C, See Fig. 11,14
t_r	Rise Time	—	37	—		I_C = 9.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	220	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	160	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.85	—	mJ	and diode reverse recovery
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	450	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	61	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	14	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	37	55	ns	T_J = 25°C See Fig.
		—	55	90		T_J = 125°C 14 I_F = 8.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	5.0	A	T_J = 25°C See Fig.
		—	4.5	8.0		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	65	138	nC	T_J = 25°C See Fig.
		—	124	360		T_J = 125°C 16 di/dt = 200Aµs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	240	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	210	—		T_J = 125°C 17

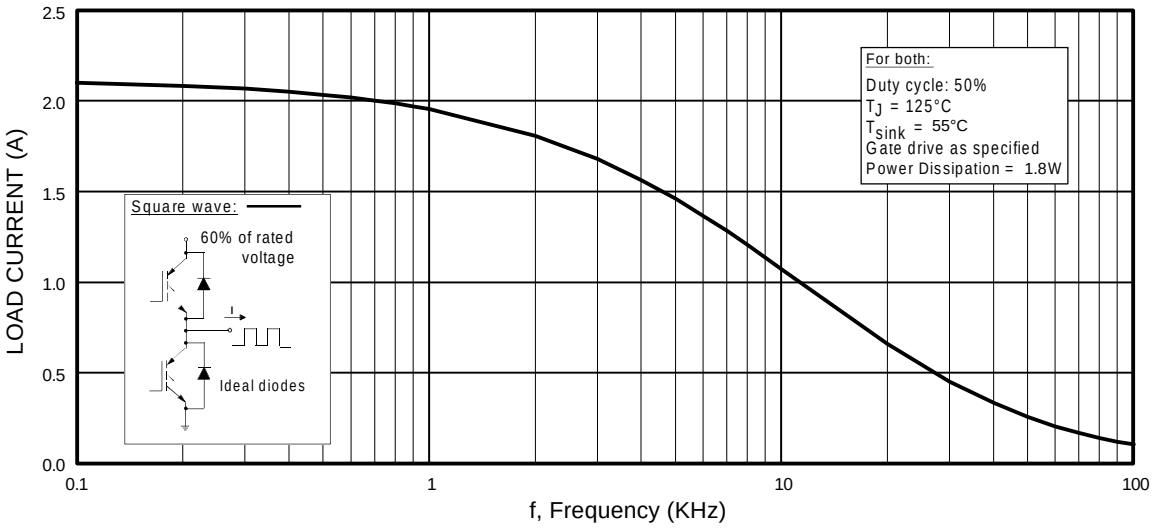


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

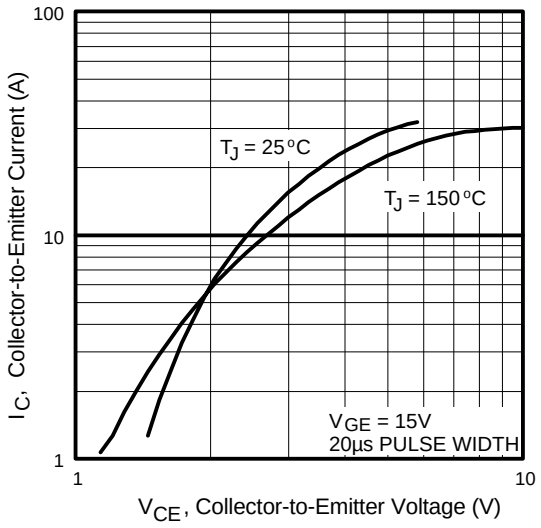


Fig. 2 - Typical Output Characteristics

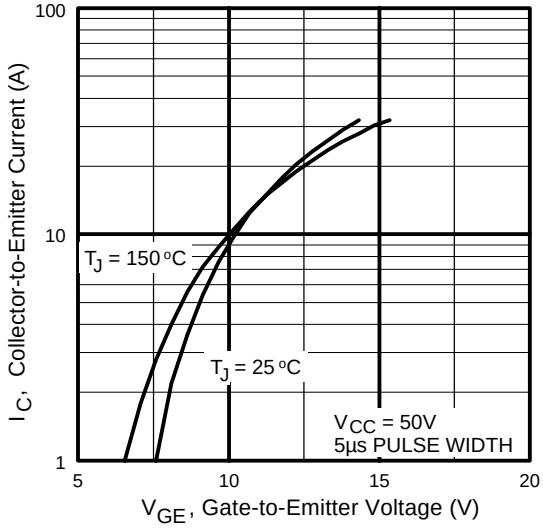


Fig. 3 - Typical Transfer Characteristics

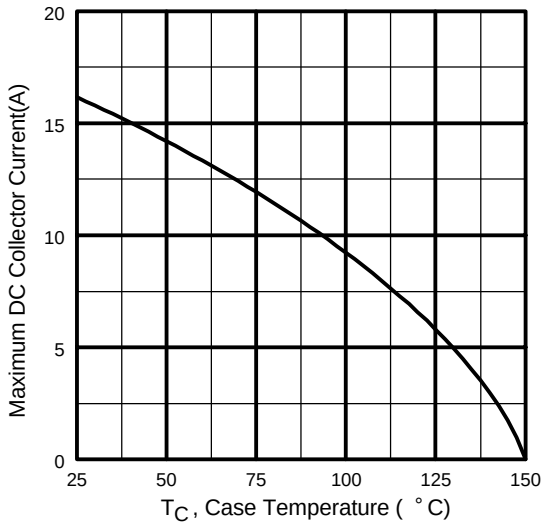


Fig. 4 - Maximum Collector Current vs. Case Temperature

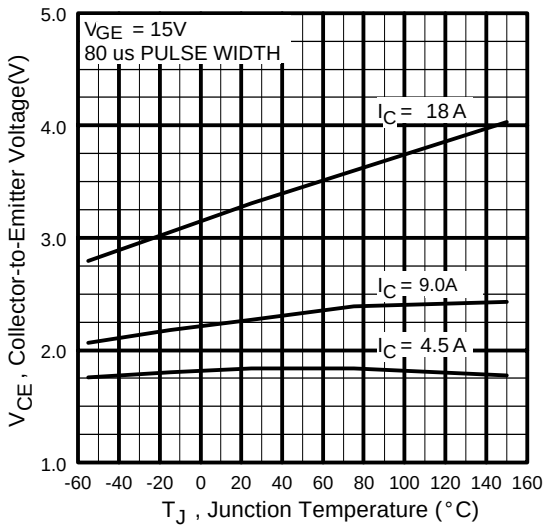


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

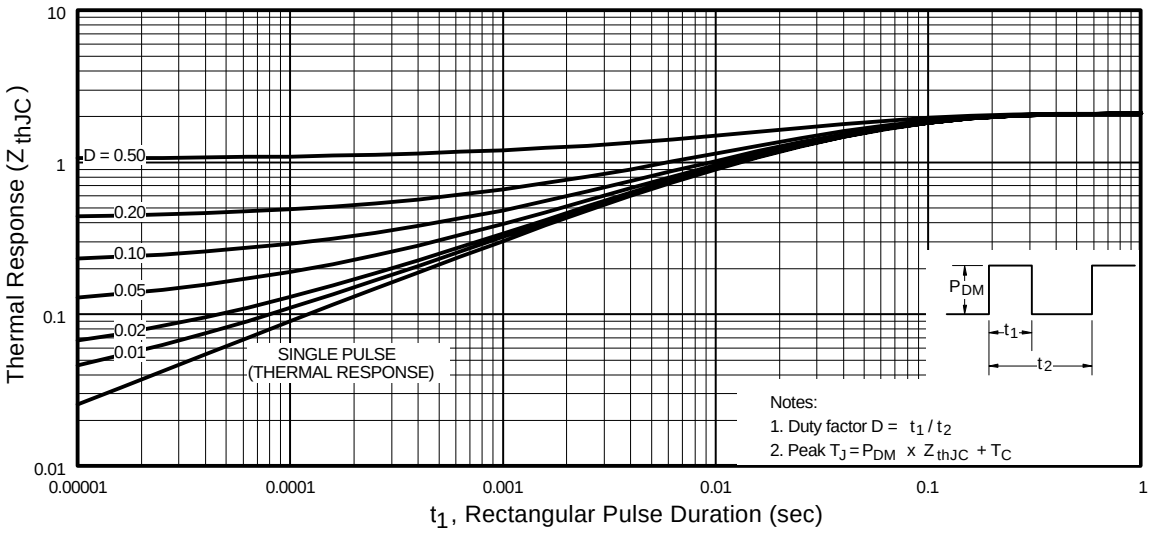


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

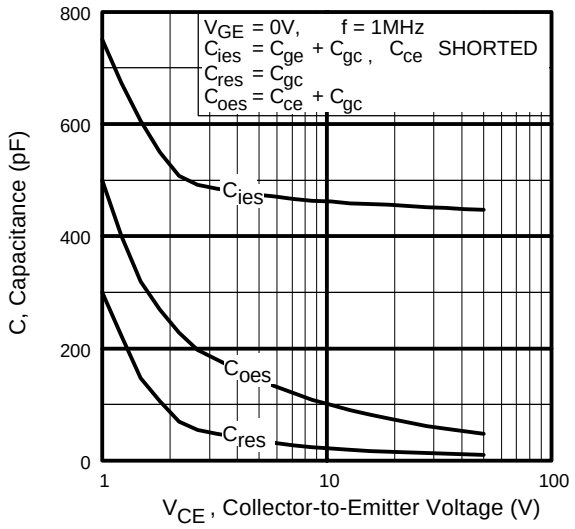


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

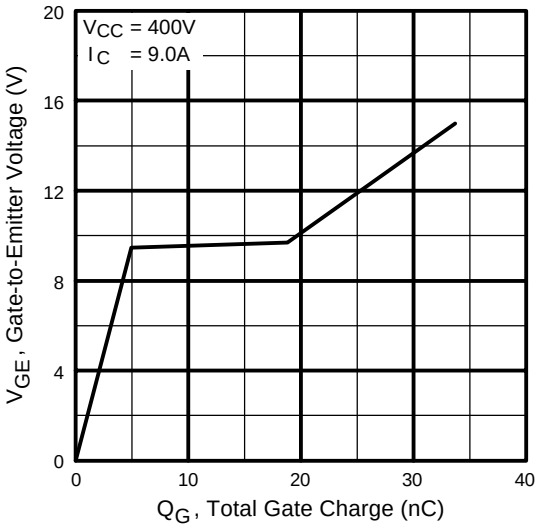


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

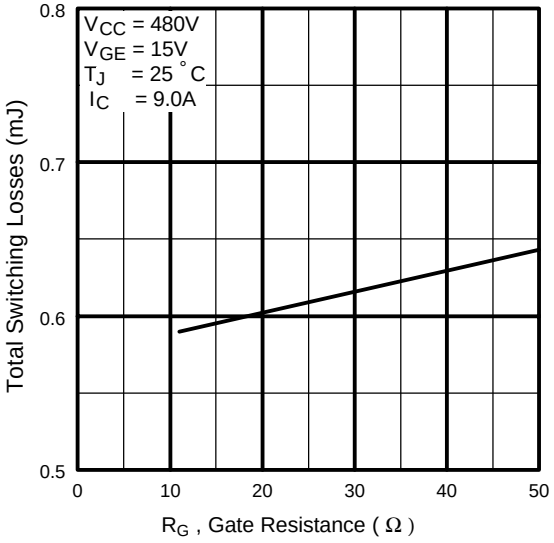


Fig. 9 - Typical Switching Losses vs. Gate Resistance

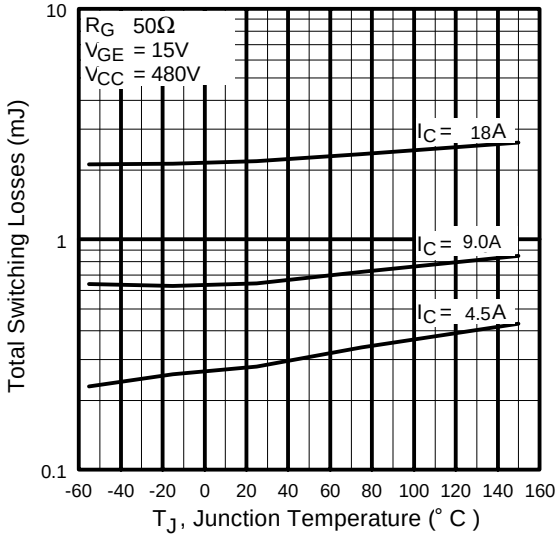


Fig. 10 - Typical Switching Losses vs. Junction Temperature

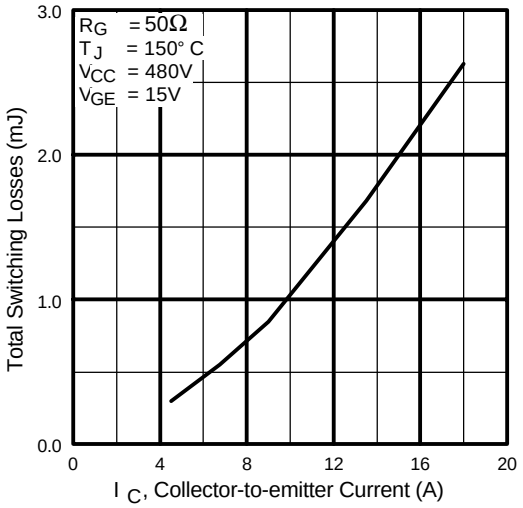


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

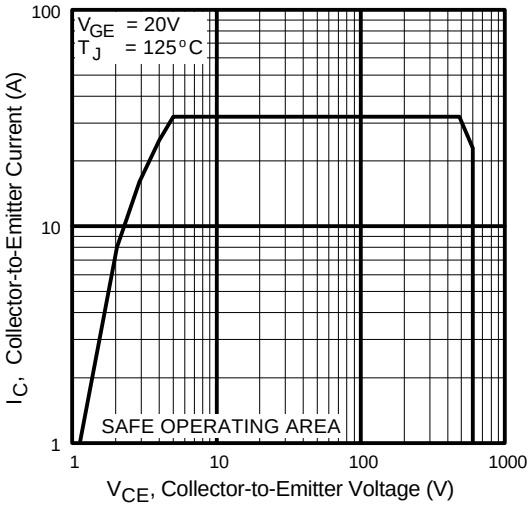


Fig. 12 - Turn-Off SOA

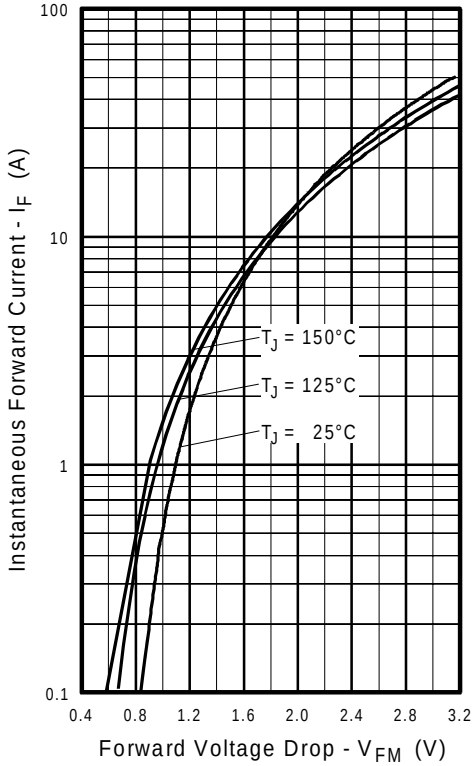


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

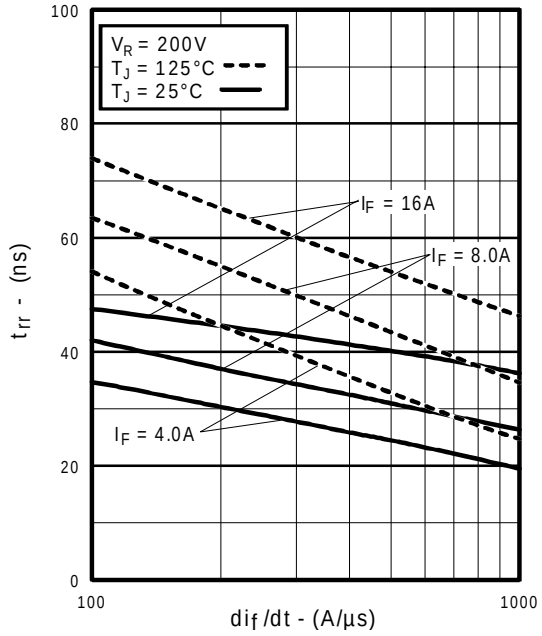


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

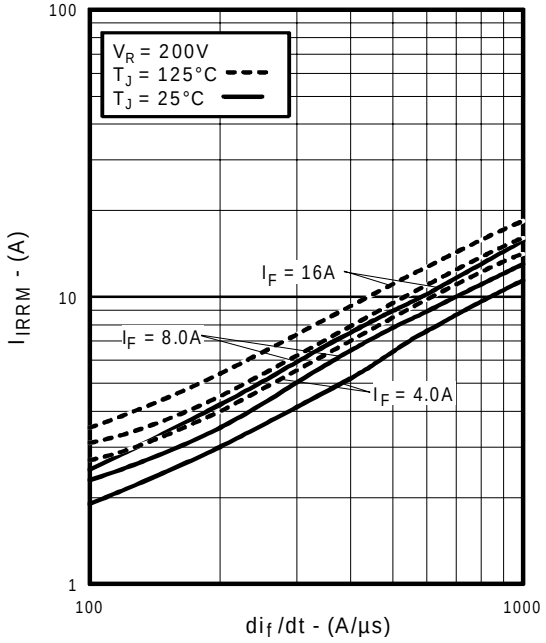


Fig. 15 - Typical Recovery Current vs. di_f/dt

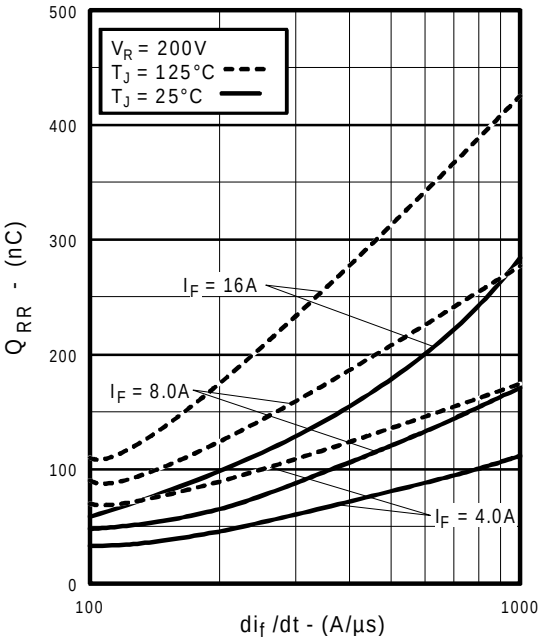


Fig. 16 - Typical Stored Charge vs. di_f/dt

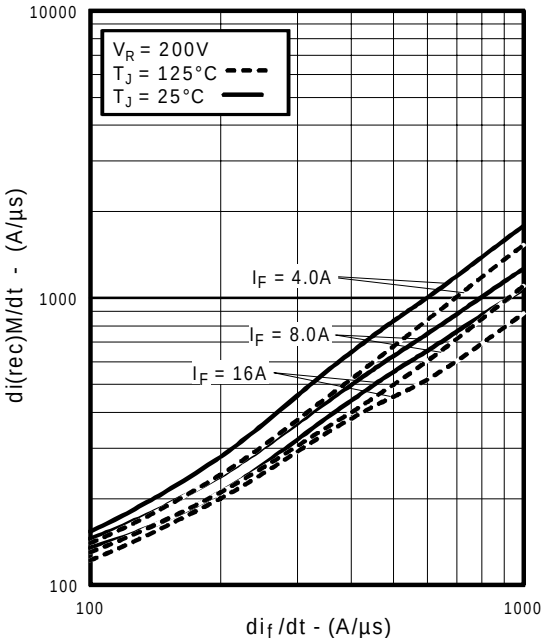


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

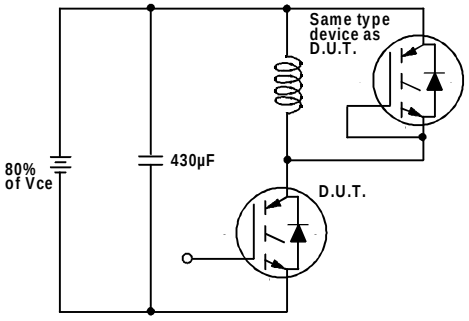


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

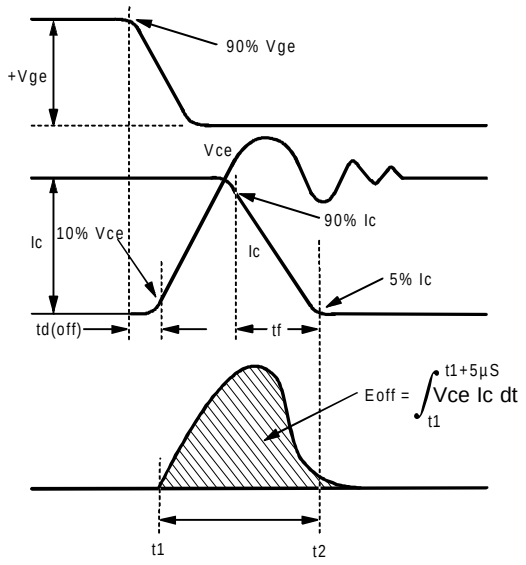


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

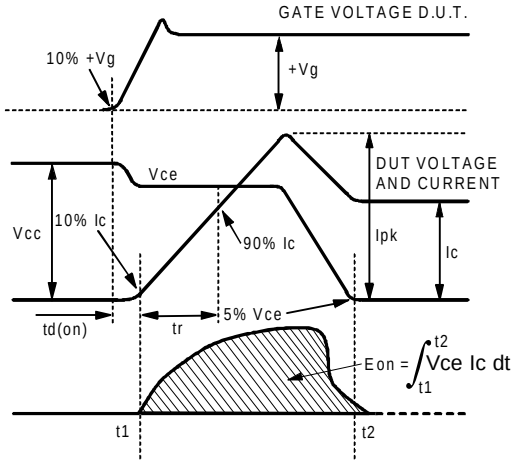


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

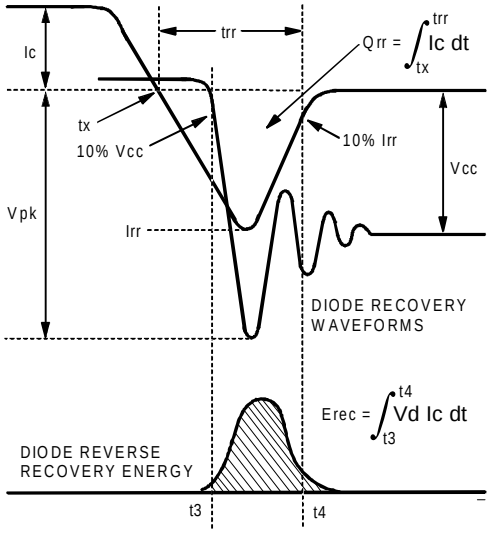


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

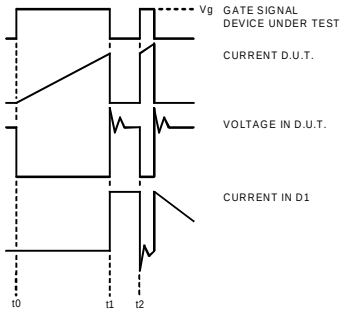


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

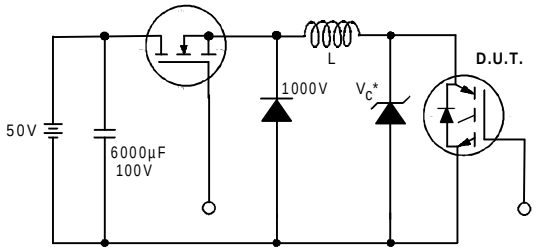


Figure 19. Clamped Inductive Load Test Circuit

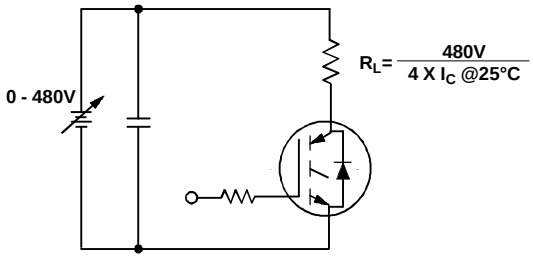
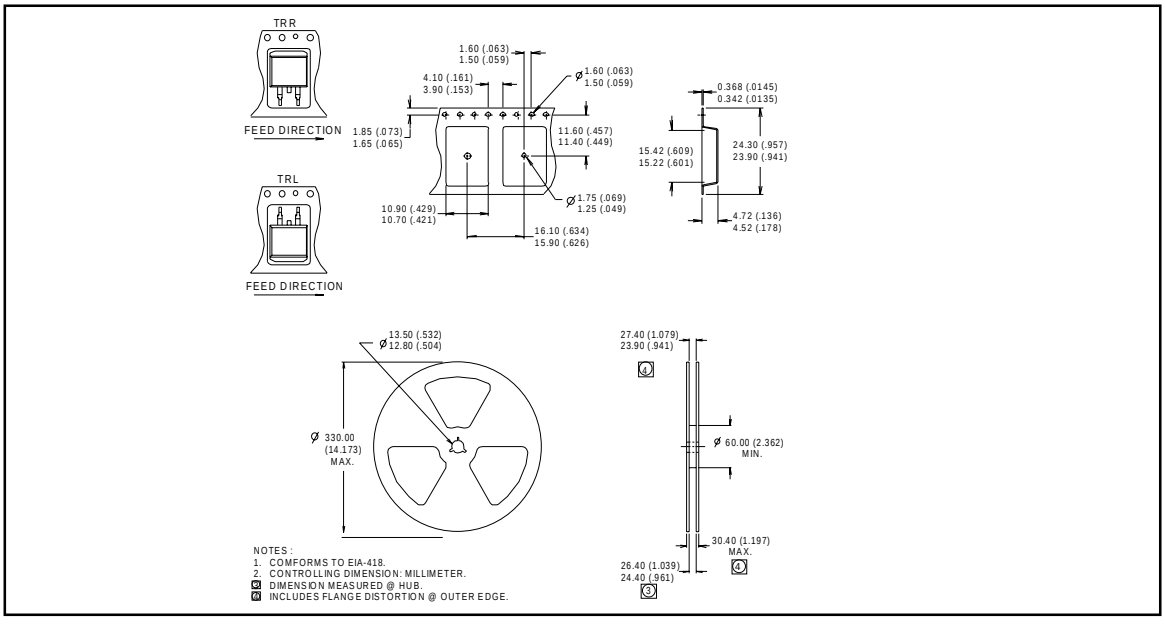


Figure 20. Pulsed Collector Current Test Circuit

Tape & Reel Information

D^2Pak



Notes:

① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

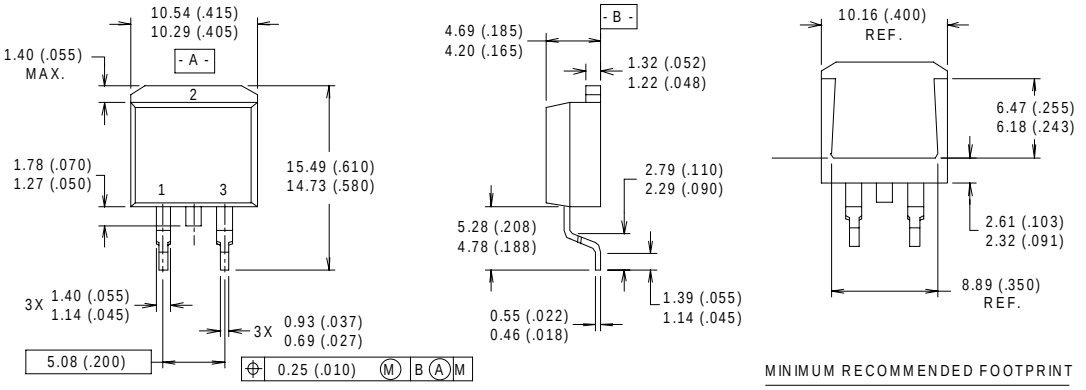
② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 50Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

⑤ When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

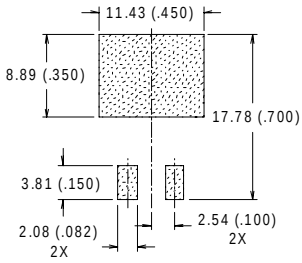
D²Pak Package Outline



NOTES:
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT



International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 10/00

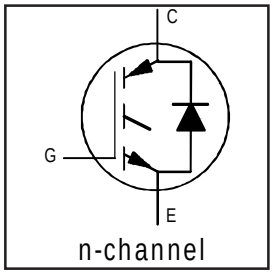
PD- 94151A

International
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IRG4BC15MD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
Fast IGBT

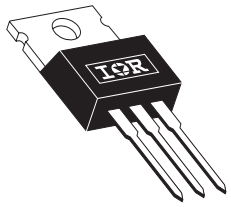


n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.88V

@V_{GE} = 15V, I_C = 8.6A



TO-220AB

Features

- Rugged: 10µsec short circuit capable at VGS = 15V
- Low VCE(on) for 4 to 10kHz applications
- IGBT co-packaged with ultra-soft-recovery anti-parallel diodes
- Industry standard TO-220AB package

Benefits

- Best Value for Appliance and Industrial applications
- Offers highest efficiency and short circuit capability for intermediate applications
- Provides best efficiency for the mid range frequency (4 to 10kHz)
- Optimized for Appliance and Industrial applications up to 1HP
- High noise immune "Positive Only" gate drive - Negative bias gate drive not necessary
- For Low EMI designs - requires little or no snubbing
- Single Package switch for bridge circuit applications
- Compatible with high voltage Gate Drive IC's
- Allows simpler gate drive

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	14	A
I_C @ T_C = 100°C	Continuous Collector Current	8.6	
I_{CM}	Pulsed Collector Current ①	28	
I_{LM}	Clamped Inductive Load Current ②	28	
I_F @ T_C = 100°C	Diode Continuous Forward Current	4.0	
t_{sc}	Short Circuit Withstand Time	12	µs
I_{FM}	Diode Maximum Forward Current	16	A
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	49	W
P_D @ T_C = 100°C	Maximum Power Dissipation	19	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	2.7	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	7.0	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	80	
Wt	Weight	—	2 (0.07)	—	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.65	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.88	2.3	V	I_C = 8.6A V_{GE} = 15V
		—	2.6	—		I_C = 14A
		—	2.1	—		I_C = 8.6A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	4.0	—	6.5		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	2.3	3.4	—	S	V_{CE} = 100V, I_C = 6.5A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1400		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.5	1.8	V	I_C = 4.0A
		—	1.4	1.7		I_C = 4.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	46	—	nC	I_C = 8.6A
Qge	Gate - Emitter Charge (turn-on)	—	4.2	—		V_{CC} = 400V
Q_{gc}	Gate - Collector Charge (turn-on)	—	15	—		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	T_J = 25°C
t_r	Rise Time	—	38	—		I_C = 8.6A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	540	810		V_{GE} = 15V, R_G = 75Ω
t_f	Fall Time	—	350	530		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	0.32	—	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	1.93	—		
E_{ts}	Total Switching Loss	—	2.25	3.6		
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	T_J = 150°C,
t_r	Rise Time	—	42	—		I_C = 8.6A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	650	—		V_{GE} = 15V, R_G = 75Ω
t_f	Fall Time	—	590	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	3.0	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	340	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	35	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	8.8	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	28	42	ns	T_J = 25°C
		—	38	57		T_J = 125°C I_F = 4.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	2.9	5.2	A	T_J = 25°C
		—	3.7	6.7		T_J = 125°C V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	40	60	nC	T_J = 25°C
		—	70	110		T_J = 125°C di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	280	—	A/µs	T_J = 25°C
	During t_b	—	240	—		T_J = 125°C

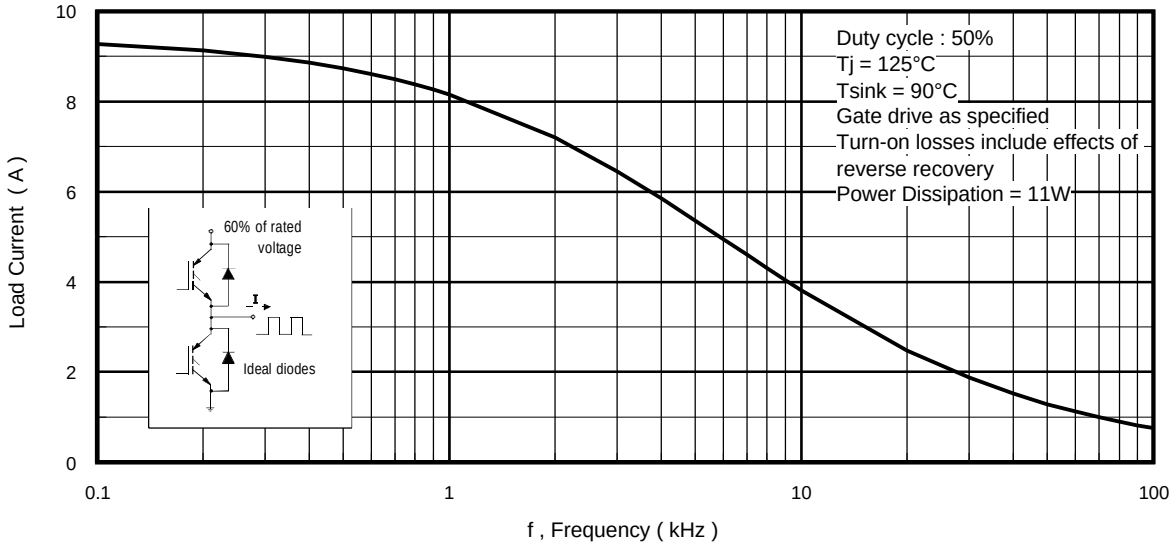


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

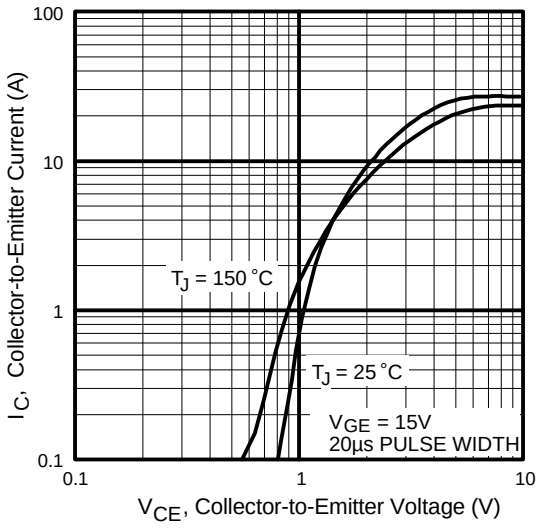


Fig. 2 - Typical Output Characteristics

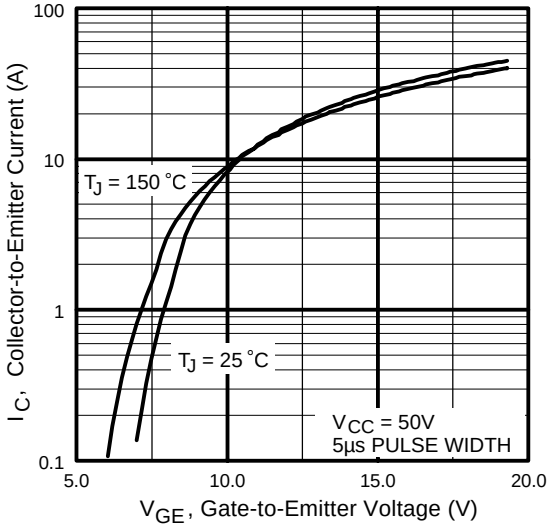


Fig. 3 - Typical Transfer Characteristics

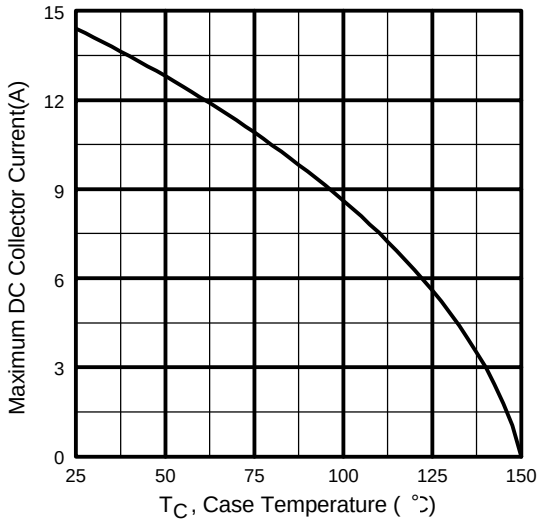


Fig. 4 - Maximum Collector Current vs. Case Temperature

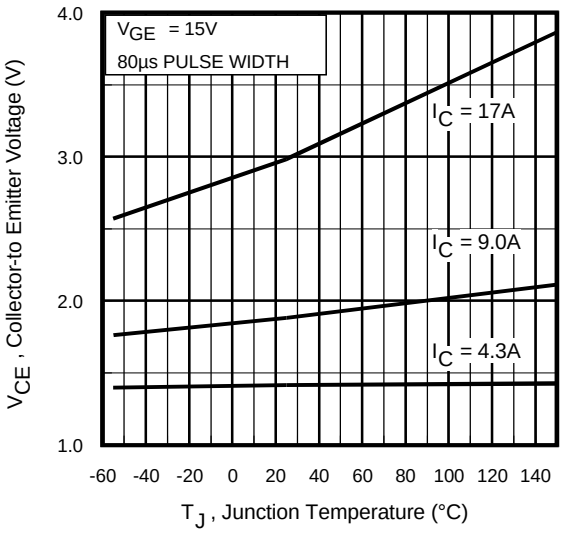


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

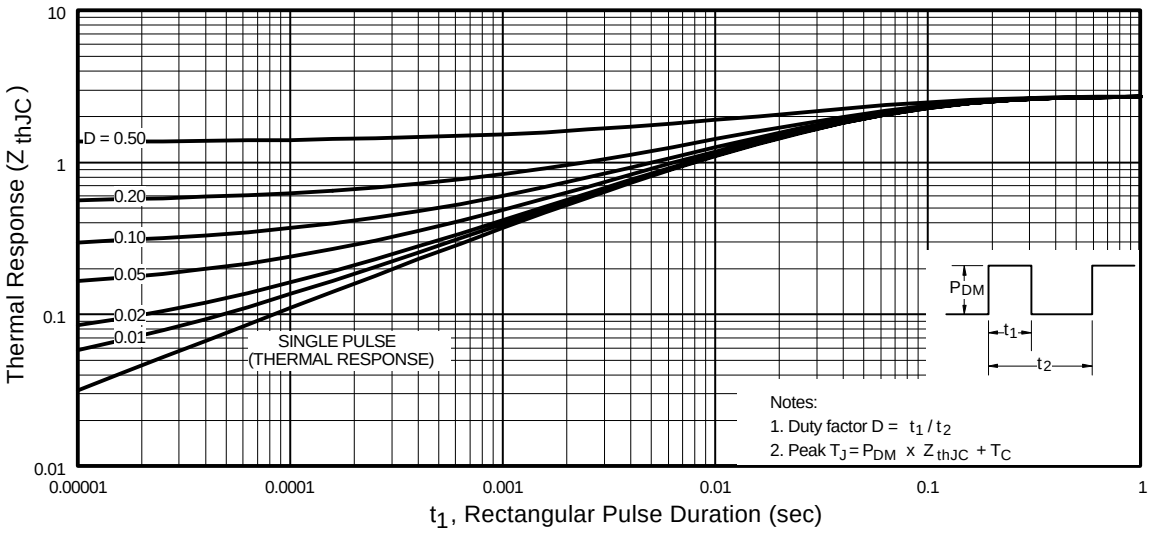


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

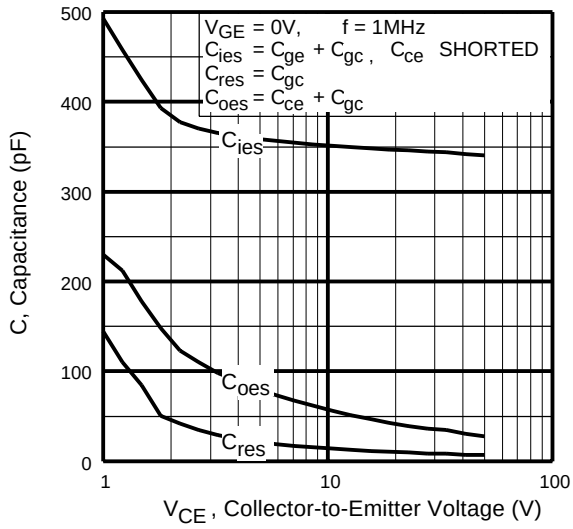


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

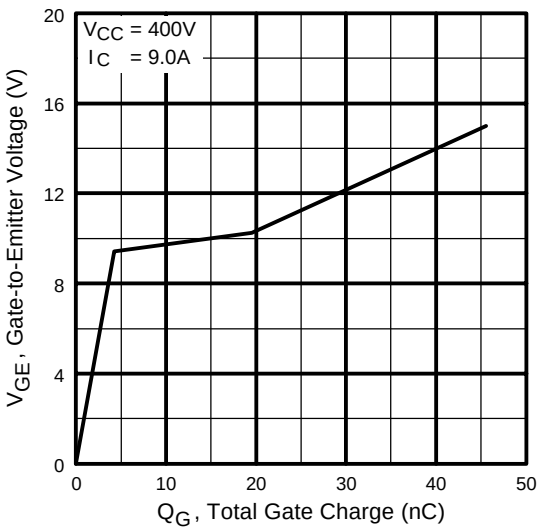


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

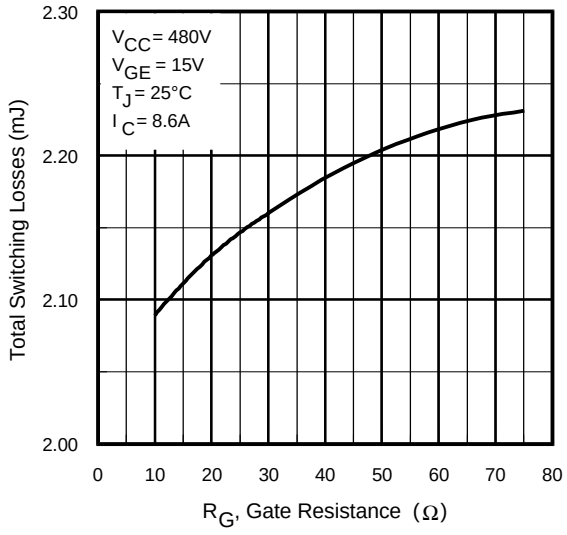


Fig. 9 - Typical Switching Losses vs. Gate Resistance

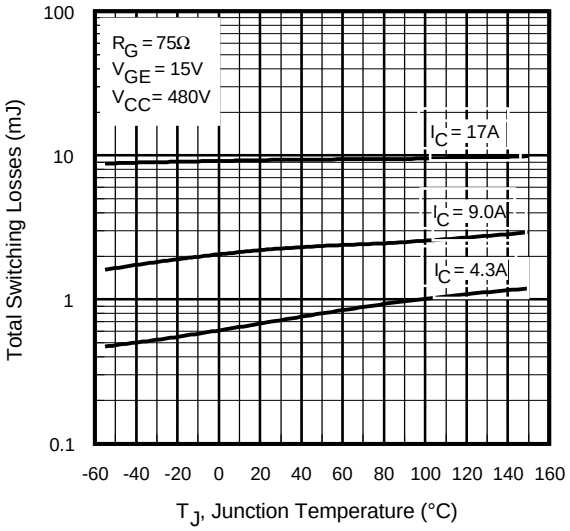


Fig. 10 - Typical Switching Losses vs. Junction Temperature

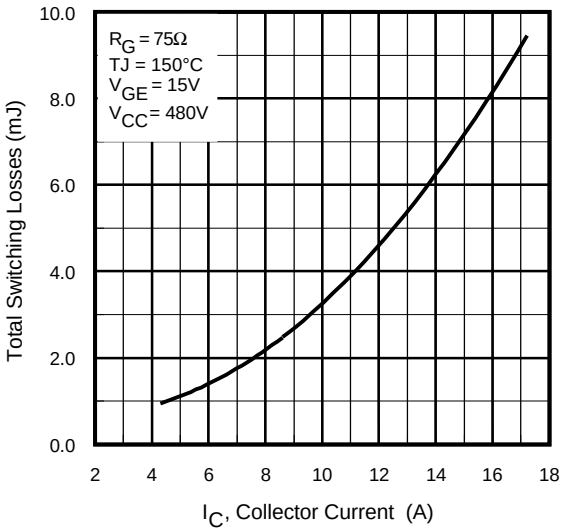


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

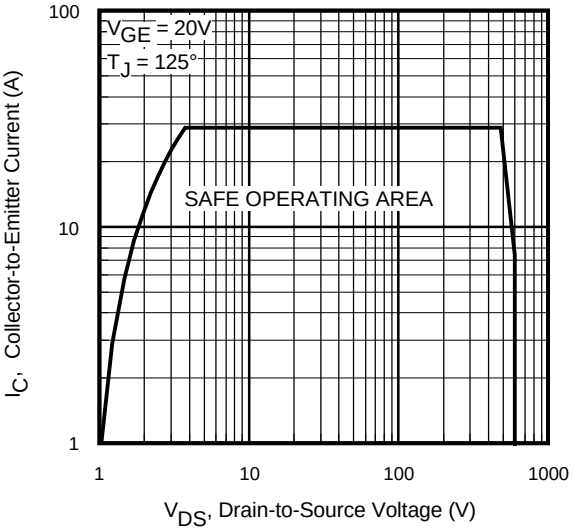
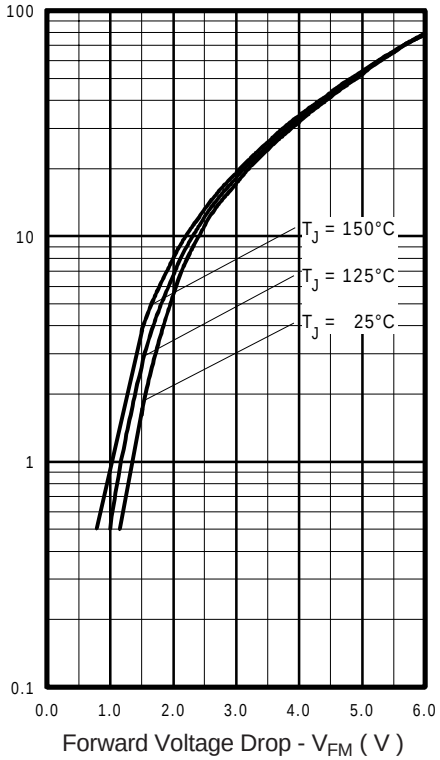


Fig. 12 - Turn-Off SOA



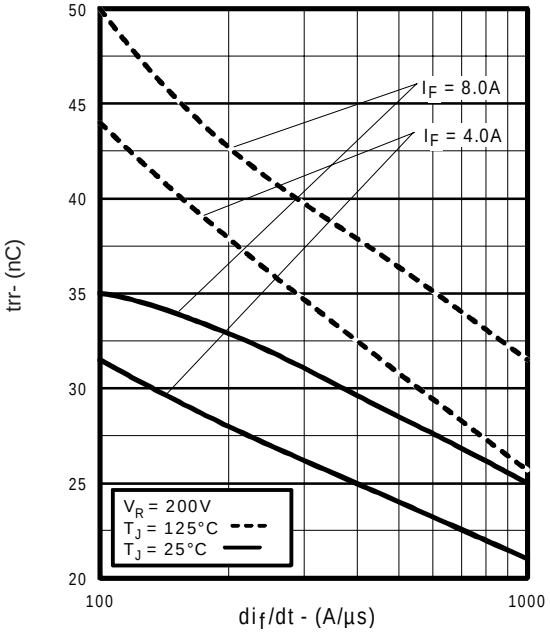


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

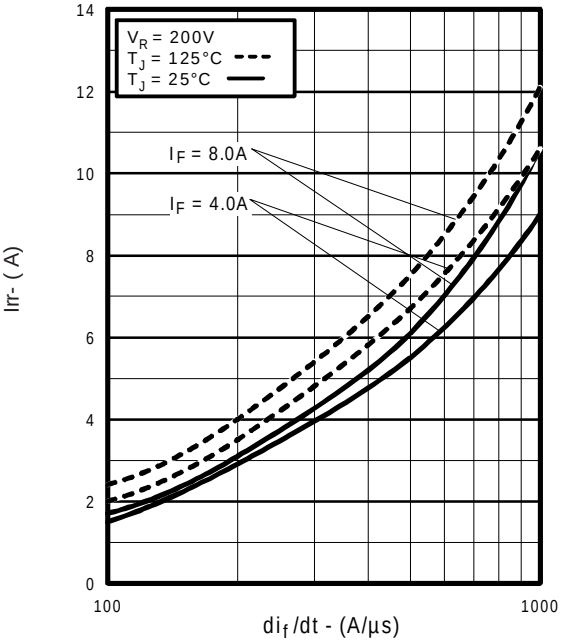


Fig. 15 - Typical Recovery Current vs. di_f/dt

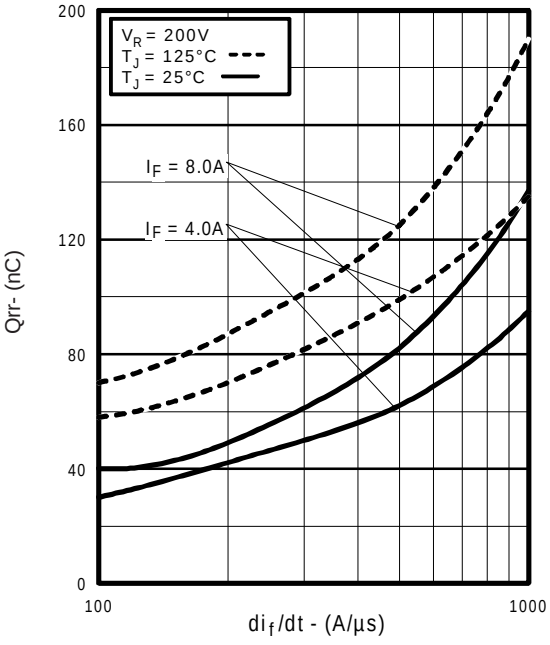


Fig. 16 - Typical Stored Charge vs. di_f/dt

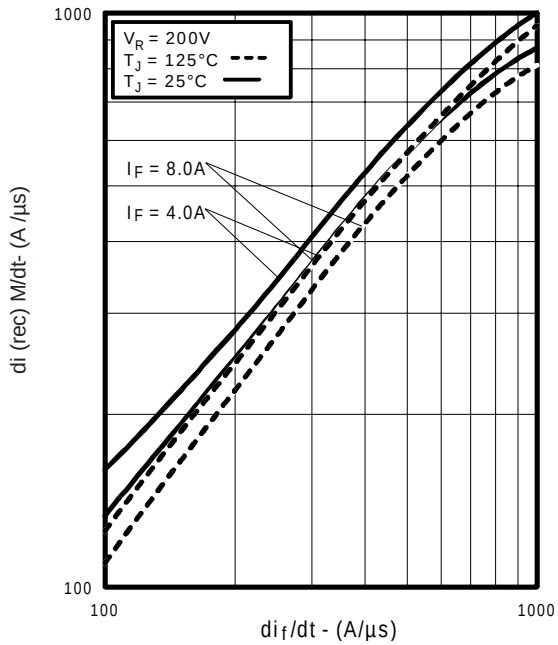


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt,

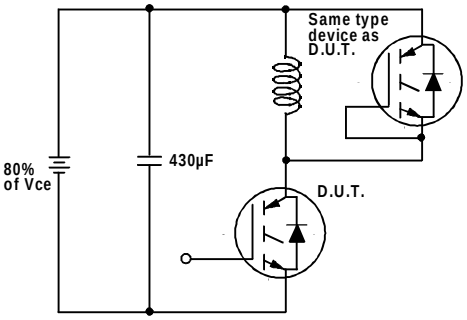


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

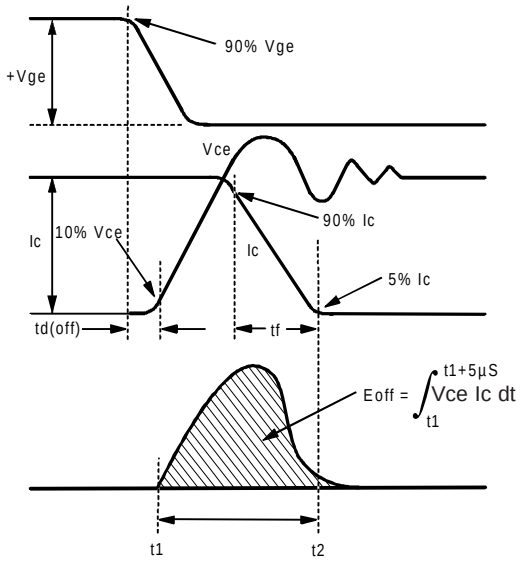


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

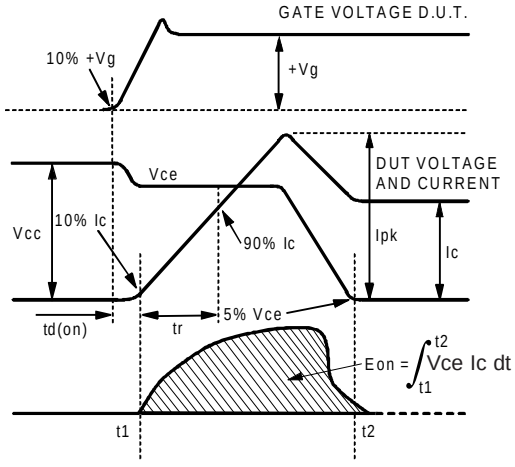


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

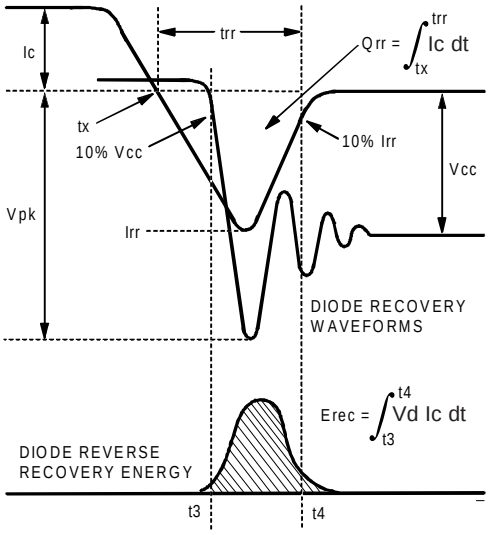


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

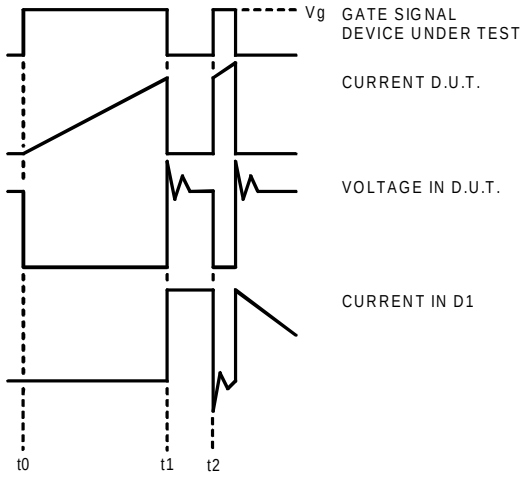


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

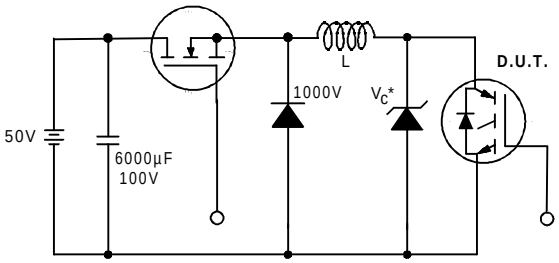


Figure 19. Clamped Inductive Load Test Circuit

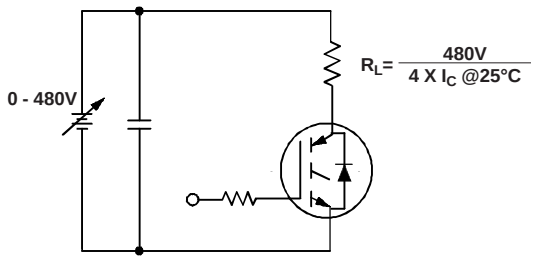


Figure 20. Pulsed Collector Current Test Circuit

Notes:

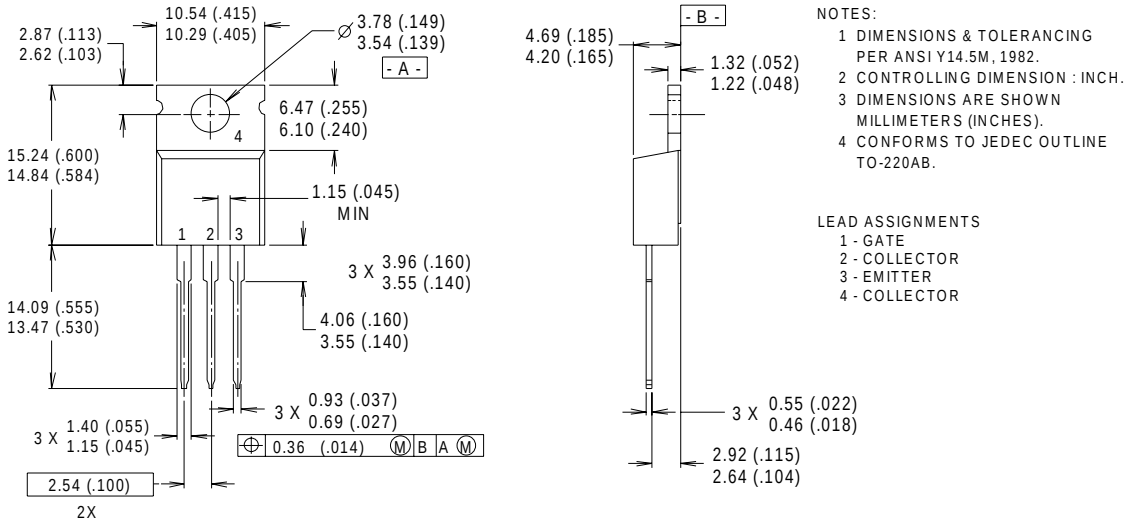
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 75Ω

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-220AB



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-220AB.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.05/01

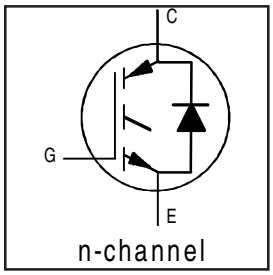
PD 91601A

International
IOR Rectifier

IRG4BC20FD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Fast CoPack IGBT



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.66V

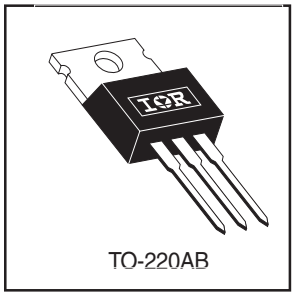
@V_{GE} = 15V, I_C = 9.0A

Features

- Fast: optimized for medium operating frequencies (1-5 kHz in hard switching, >20 kHz in resonant mode).
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-220AB package

Benefits

- Generation -4 IGBTs offer highest efficiencies available
- IGBTs optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBTs. Minimized recovery characteristics require less/no snubbing
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	16	A
I_C @ T_C = 100°C	Continuous Collector Current	9.0	
I_{CM}	Pulsed Collector Current ①	64	
I_{LM}	Clamped Inductive Load Current ②	64	
I_F @ T_C = 100°C	Diode Continuous Forward Current	7.0	
I_{FM}	Diode Maximum Forward Current	32	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	——	——	2.1	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	——	——	3.5	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	——	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	——	80	
Wt	Weight	——	2 (0.07)	——	g (oz)

7/11/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.72	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.66	2.0	V	I_C = 9.0A V_{GE} = 15V
		—	2.06	—		I_C = 16A See Fig. 2, 5
		—	1.76	—		I_C = 9.0A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	2.9	5.1	—	S	V_{CE} = 100V, I_C = 9.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1700		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 8.0A See Fig. 13
		—	1.3	1.6		I_C = 8.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	27	40	nC	I_C = 9.0A
Qge	Gate - Emitter Charge (turn-on)	—	4.2	6.2		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	9.9	15		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	43	—	ns	T_J = 25°C
t_r	Rise Time	—	20	—		I_C = 9.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	240	360		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	150	220		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	0.25	—	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	0.64	—		See Fig. 9, 10, 18
E_{ts}	Total Switching Loss	—	0.89	1.3		
$t_{d(on)}$	Turn-On Delay Time	—	41	—	ns	T_J = 150°C, See Fig. 11, 18
t_r	Rise Time	—	22	—		I_C = 9.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	320	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	290	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	1.35	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	540	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	37	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	7.0	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	37	55	ns	T_J = 25°C See Fig.
		—	55	90		T_J = 125°C 14 I_F = 8.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	5.0	A	T_J = 25°C See Fig.
		—	4.5	8.0		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	65	138	nC	T_J = 25°C See Fig.
		—	124	360		T_J = 125°C 16 di/dt = 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	240	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	210	—		T_J = 125°C 17

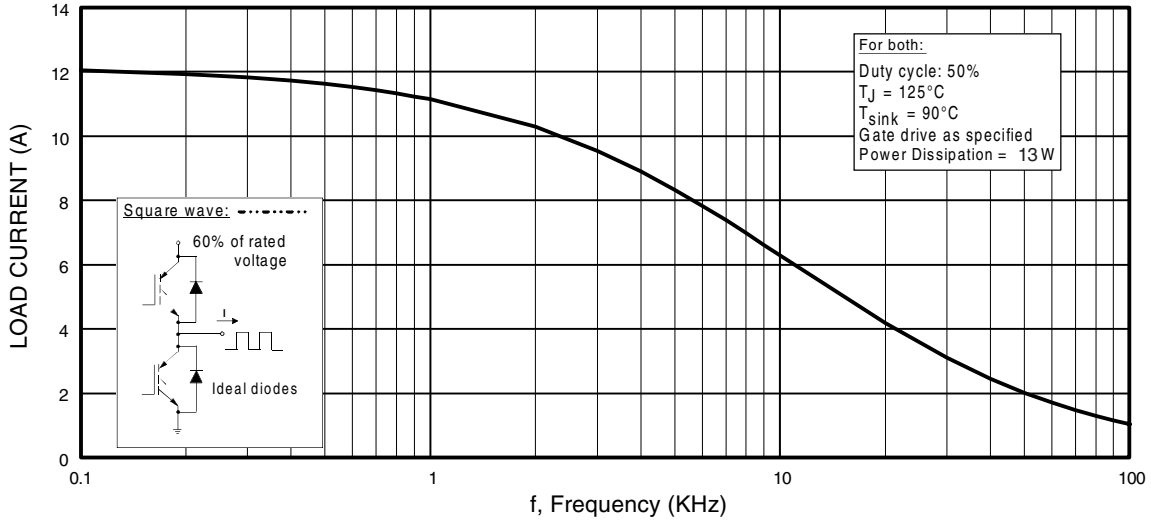


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

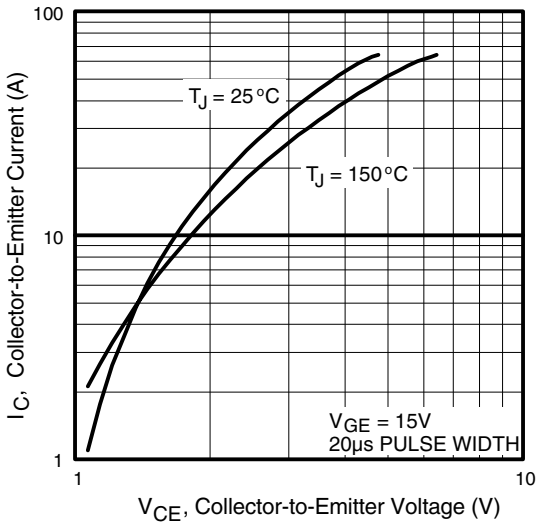


Fig. 2 - Typical Output Characteristics

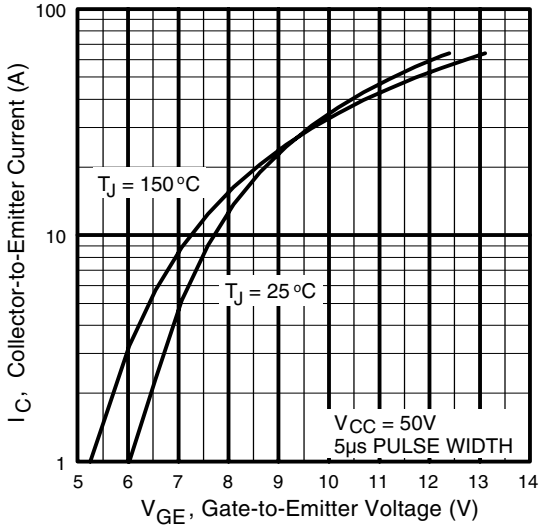


Fig. 3 - Typical Transfer Characteristics

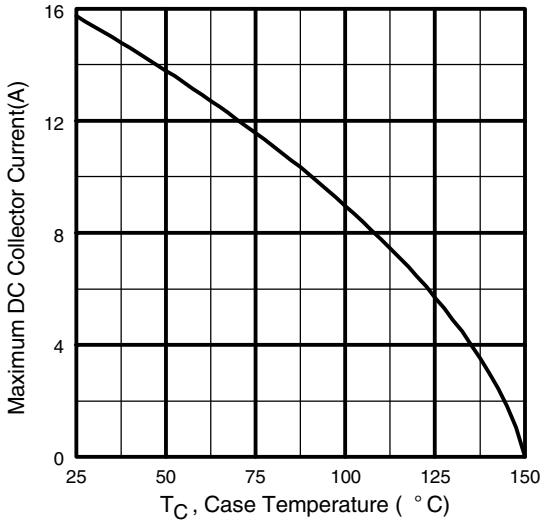


Fig. 4 - Maximum Collector Current vs. Case Temperature

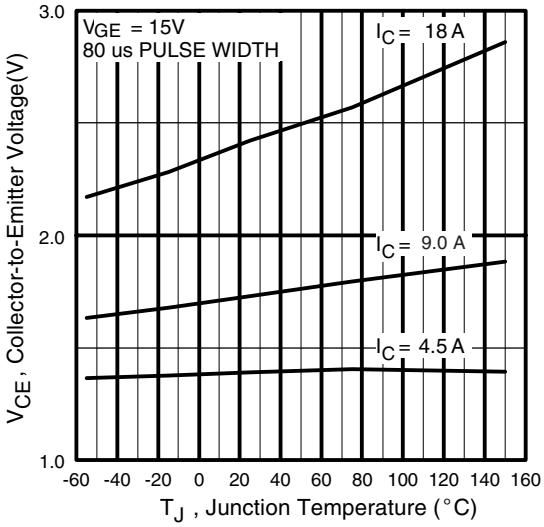


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

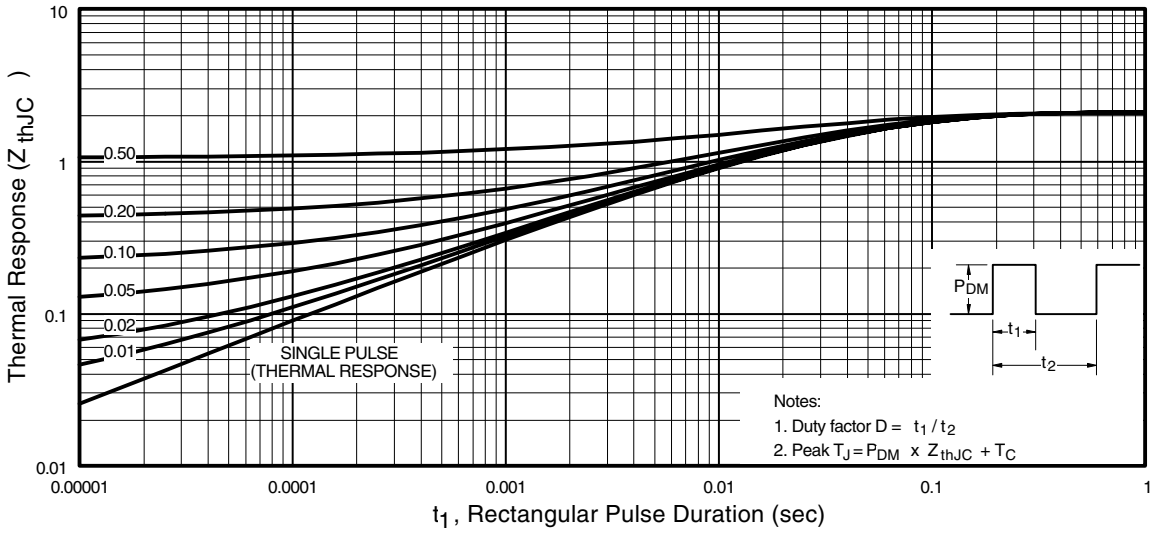


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

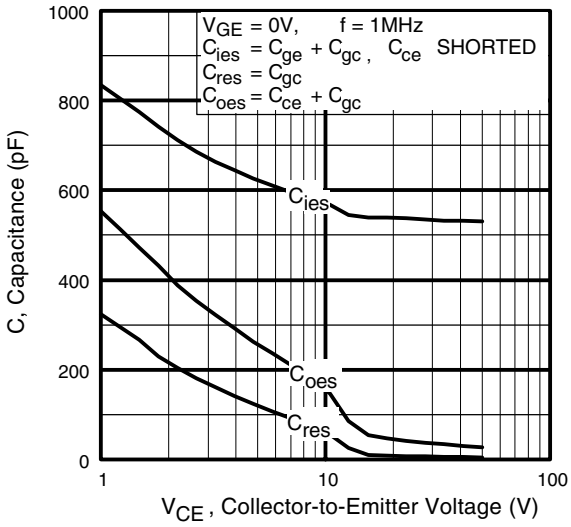


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

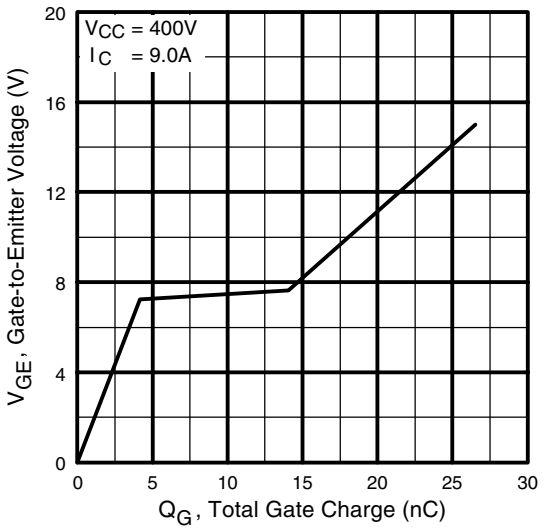


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

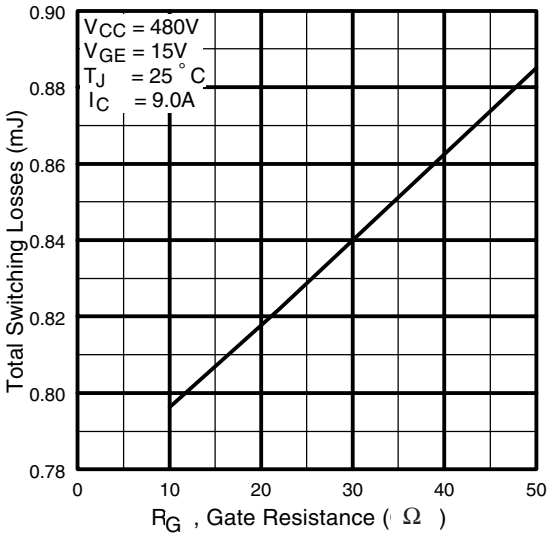


Fig. 9 - Typical Switching Losses vs. Gate Resistance

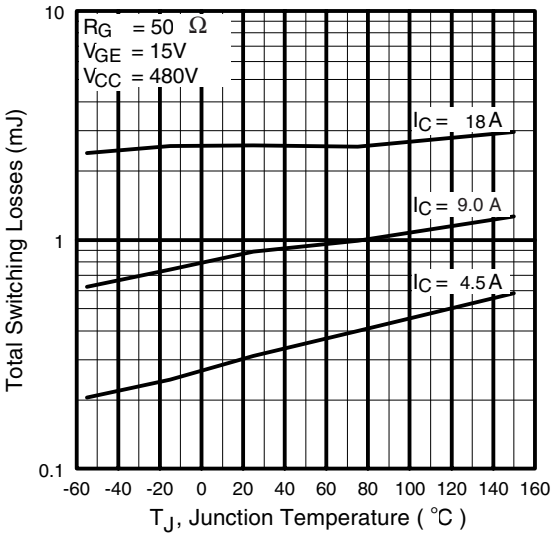


Fig. 10 - Typical Switching Losses vs. Junction Temperature

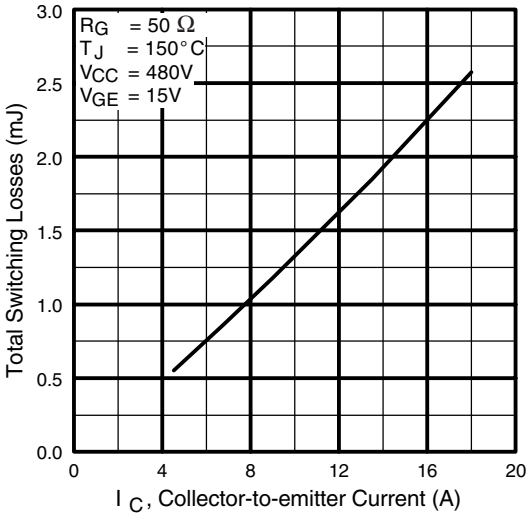


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

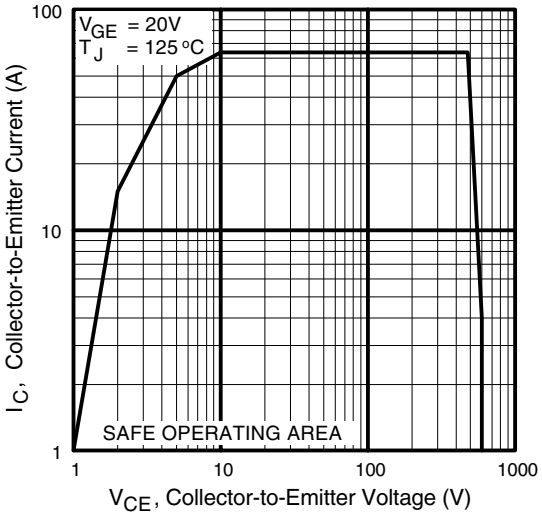


Fig. 12 - Turn-Off SOA

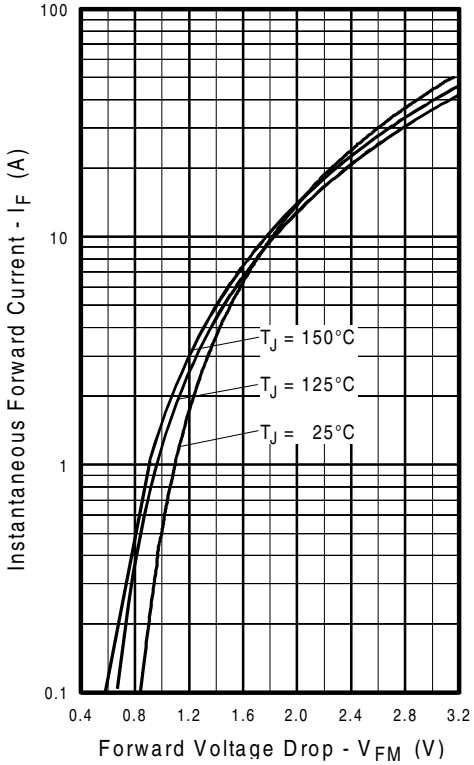


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

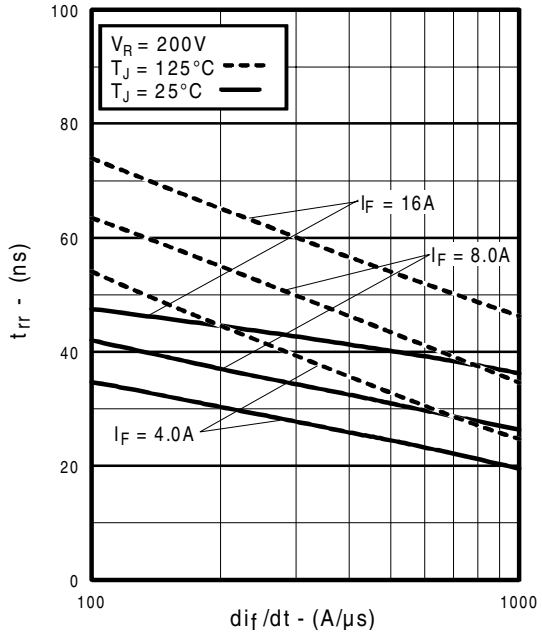


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

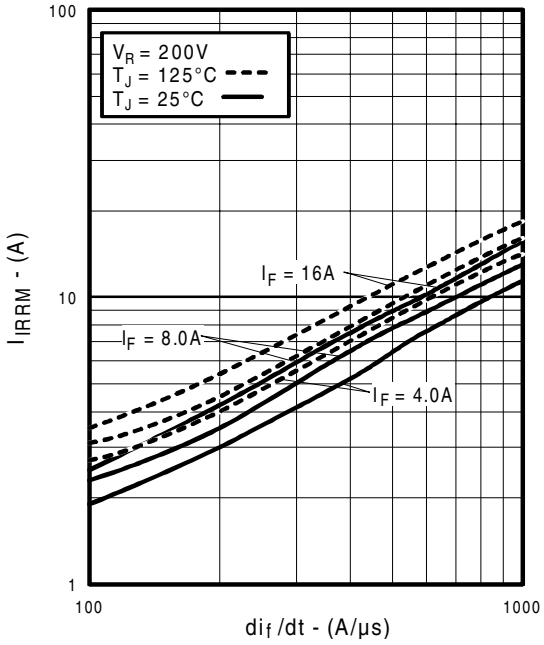


Fig. 15 - Typical Recovery Current vs. di_f/dt

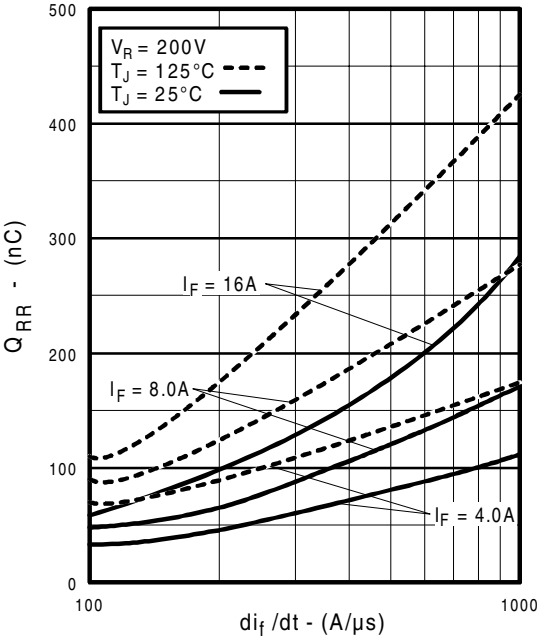


Fig. 16 - Typical Stored Charge vs. di_f/dt

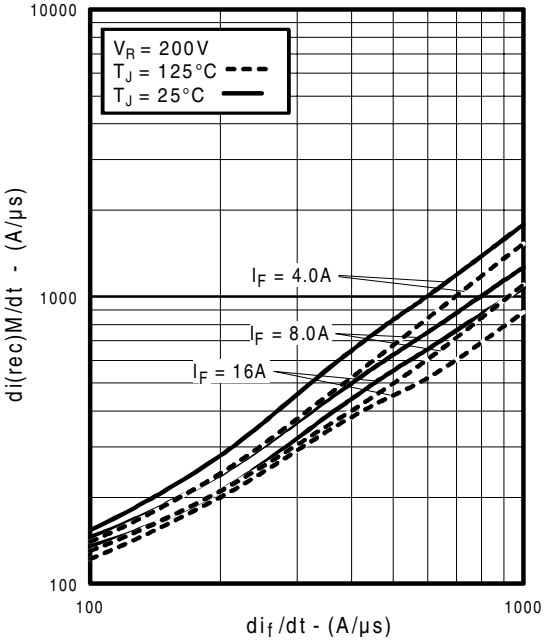


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

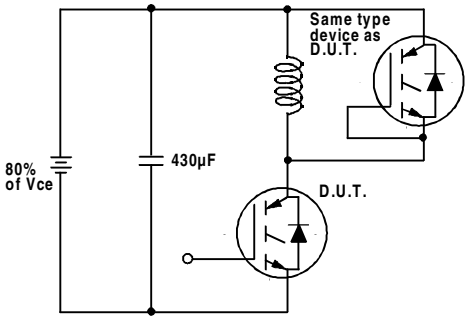


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

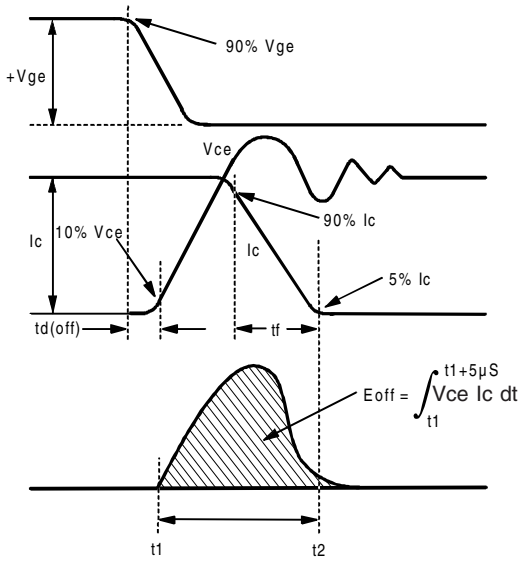


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

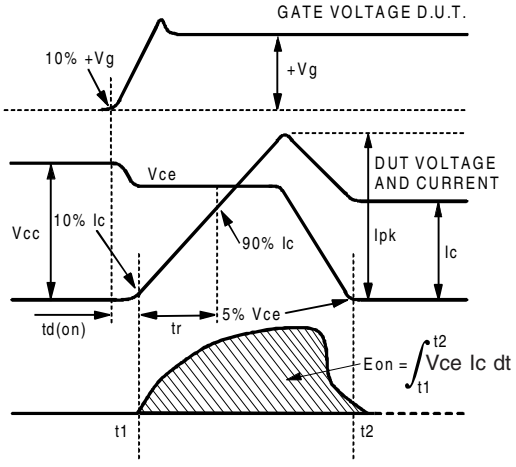


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

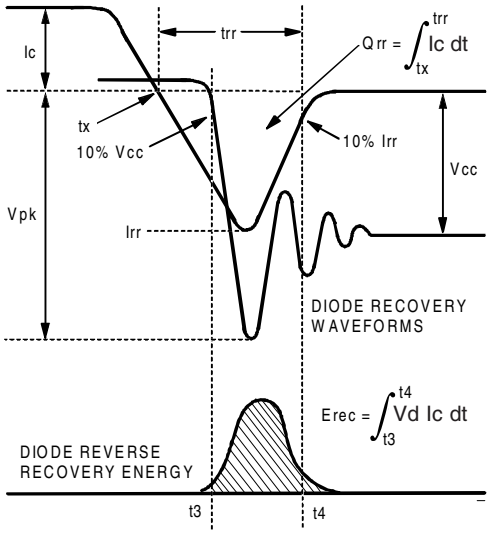


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

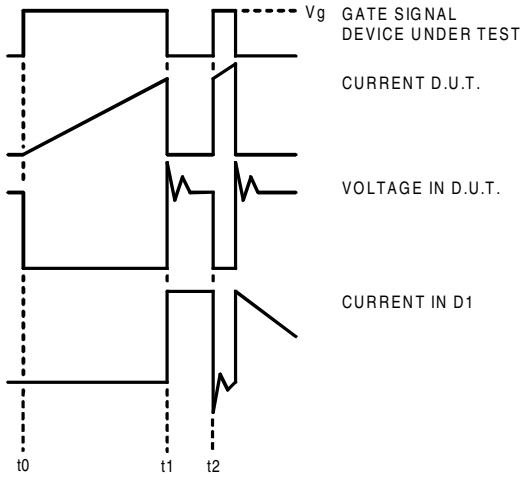


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

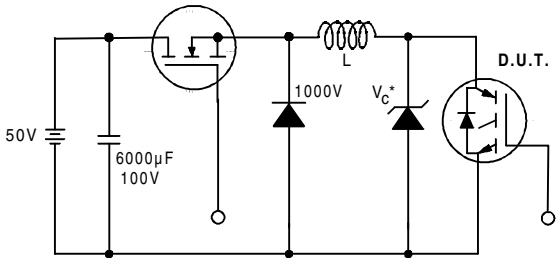


Figure 19. Clamped Inductive Load Test Circuit

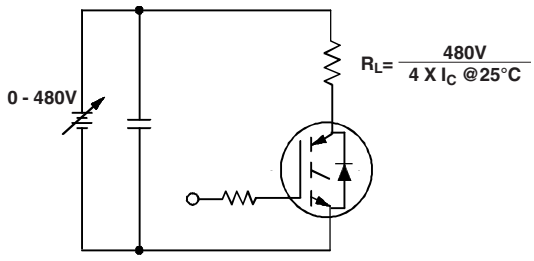


Figure 20. Pulsed Collector Current Test Circuit

Notes:

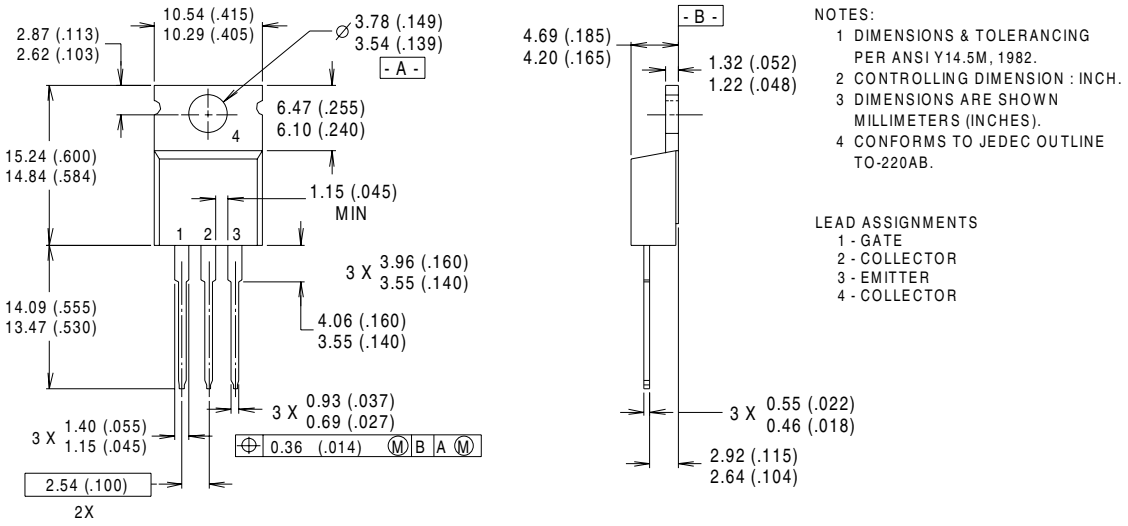
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 50Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB

Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

Data and specifications subject to change without notice. 7/00

International
IOR Rectifier

PD - 91602A

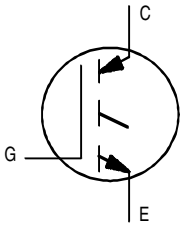
IRG4BC20F

INSULATED GATE BIPOLAR TRANSISTOR

Fast Speed IGBT

Features

- Fast: Optimized for medium operating frequencies (1-5 kHz in hard switching, >20 kHz in resonant mode).
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-220AB package



n-channel

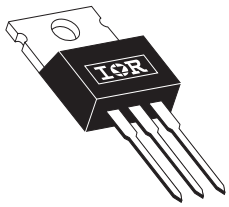
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.66V

@V_{GE} = 15V, I_C = 9.0A

Benefits

- Generation 4 IGBTs offer highest efficiency available
- IGBTs optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	16	A
I_C @ T_C = 100°C	Continuous Collector Current	9.0	
I_{CM}	Pulsed Collector Current ①	64	
I_{LM}	Clamped Inductive Load Current ②	64	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	5.0	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	80	
Wt	Weight	2.0 (0.07)	—	g (oz)

4/17/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.72	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.66	2.0	V	I_C = 9.0A V_{GE} = 15V
		—	2.06	—		I_C = 16A See Fig.2, 5
		—	1.76	—		I_C = 9.0A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	2.9	5.1	—	S	V_{CE} = 100V, I_C = 9.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	27	40	nC	I_C = 9.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	4.2	6.2		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	9.9	15		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	
t_r	Rise Time	—	17	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	190	280		I_C = 9.0A, V_{CC} = 480V
t_f	Fall Time	—	210	320		V_{GE} = 15V, R_G = 50Ω
E_{on}	Turn-On Switching Loss	—	0.07	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.60	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	0.67	1.1		
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	T_J = 150°C,
t_r	Rise Time	—	17	—		I_C = 9.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	300	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	340	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.30	—	mJ	See Fig. 11, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	540	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	37	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	7.0	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 50Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

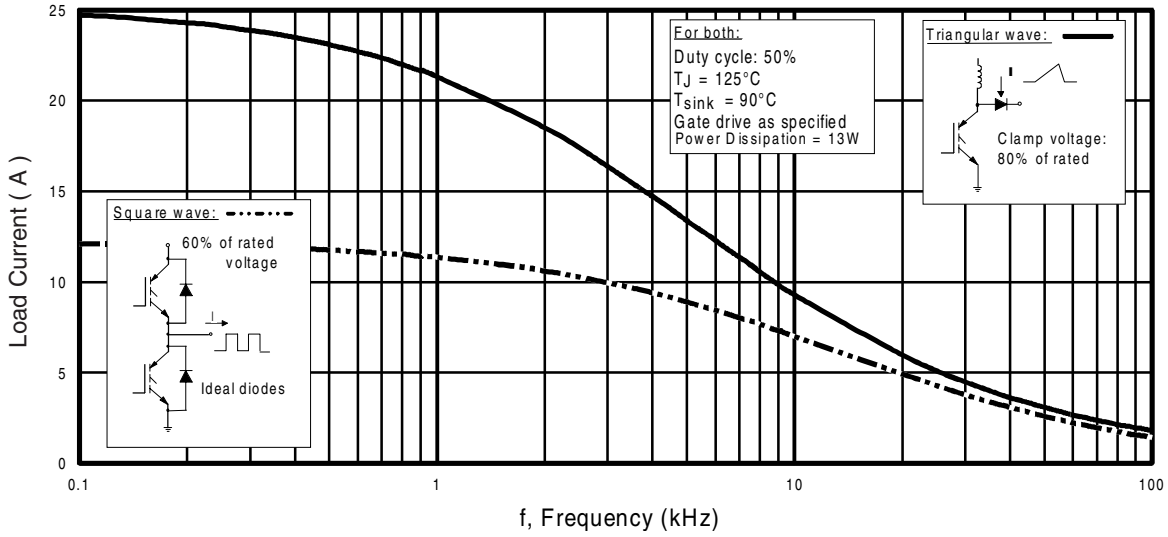


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

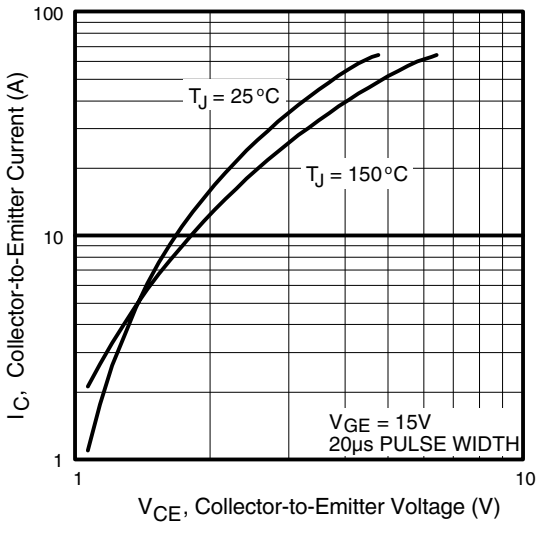


Fig. 2 - Typical Output Characteristics

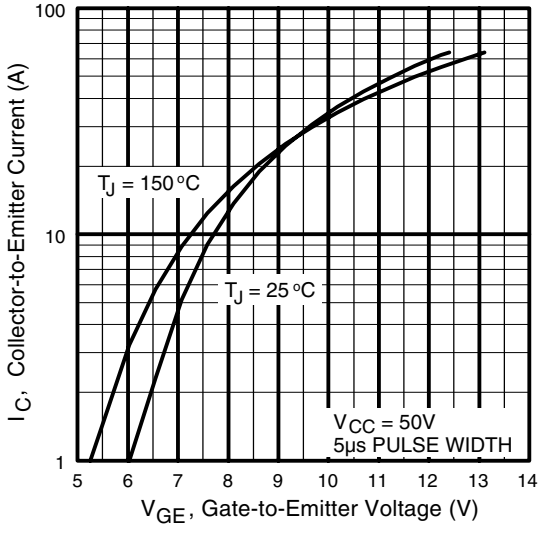


Fig. 3 - Typical Transfer Characteristics

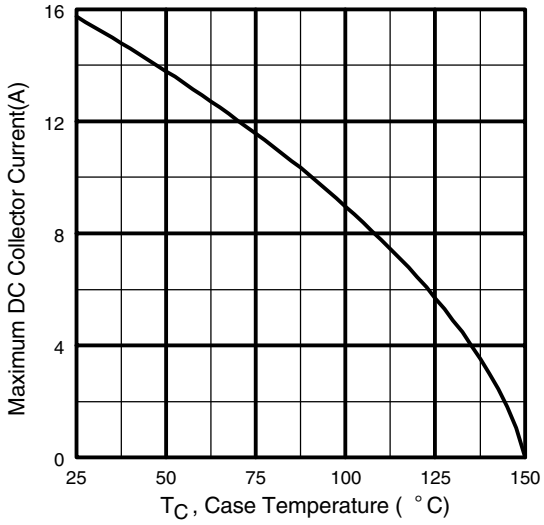


Fig. 4 - Maximum Collector Current vs. Case Temperature

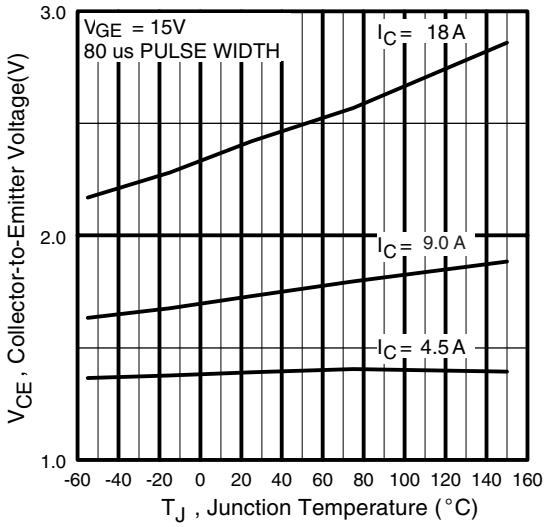


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

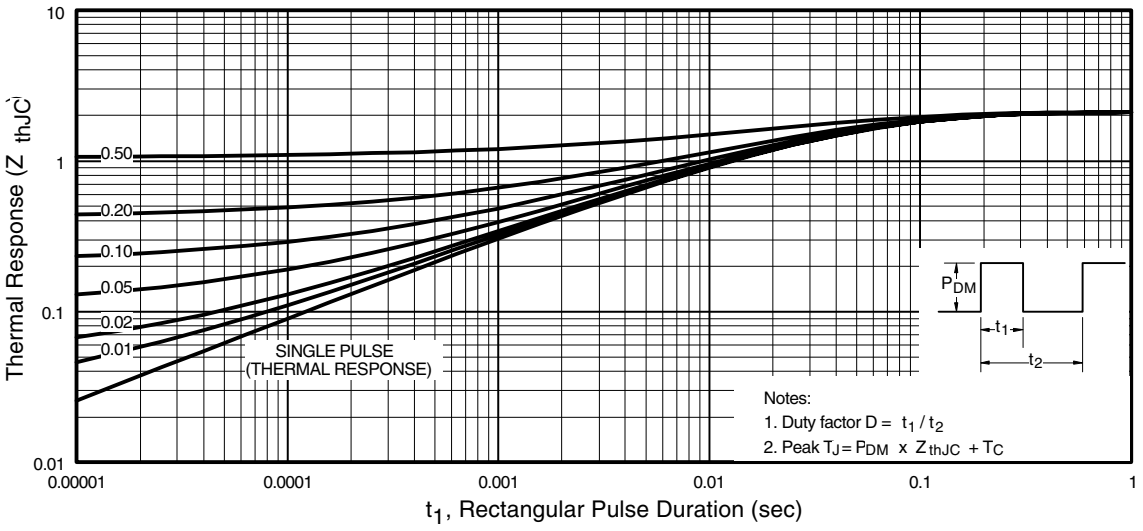


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

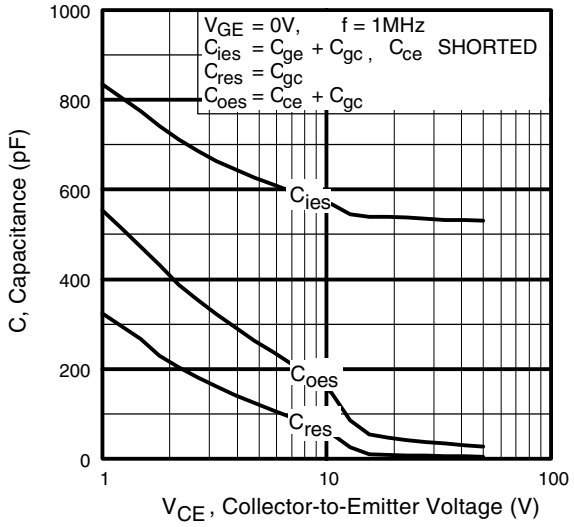


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

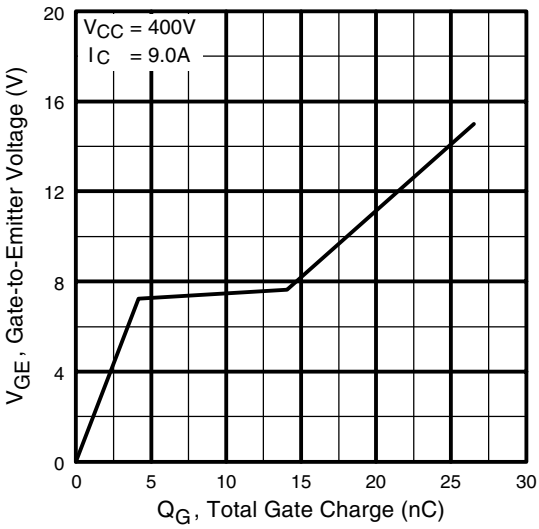


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

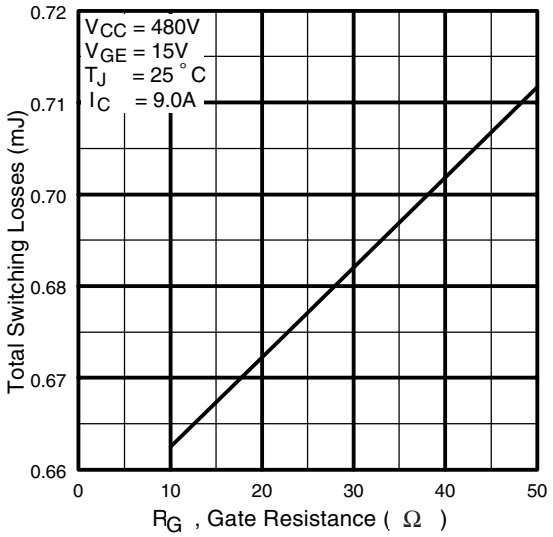


Fig. 9 - Typical Switching Losses vs. Gate Resistance

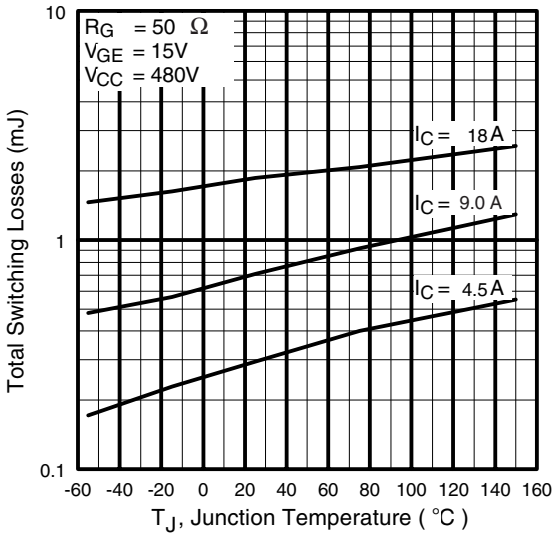


Fig. 10 - Typical Switching Losses vs. Junction Temperature

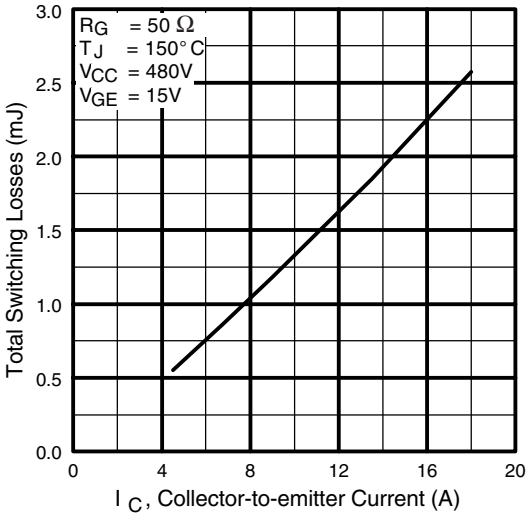


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

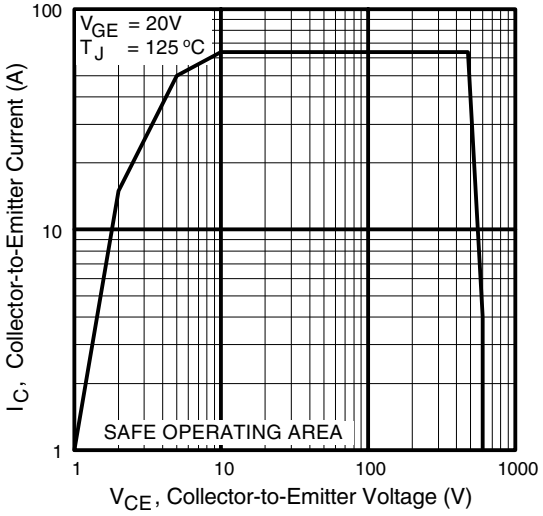


Fig. 12 - Turn-Off SOA

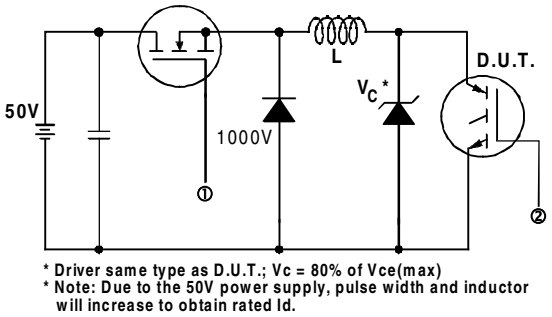


Fig. 13a - Clamped Inductive Load Test Circuit

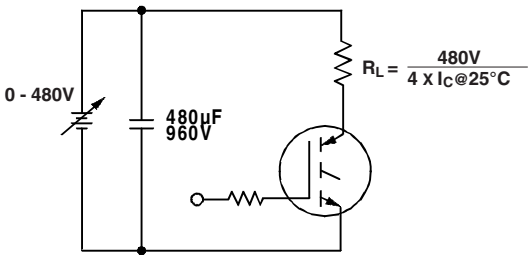


Fig. 13b - Pulsed Collector Current Test Circuit

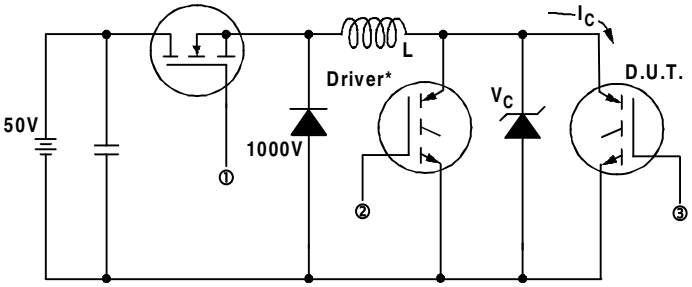


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

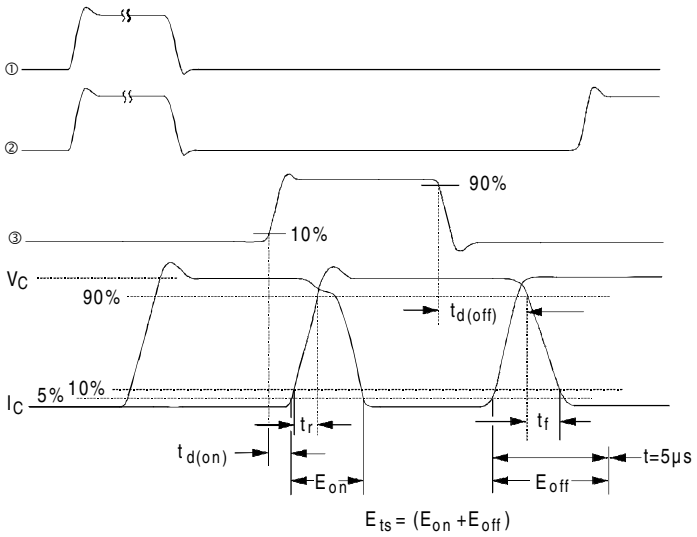
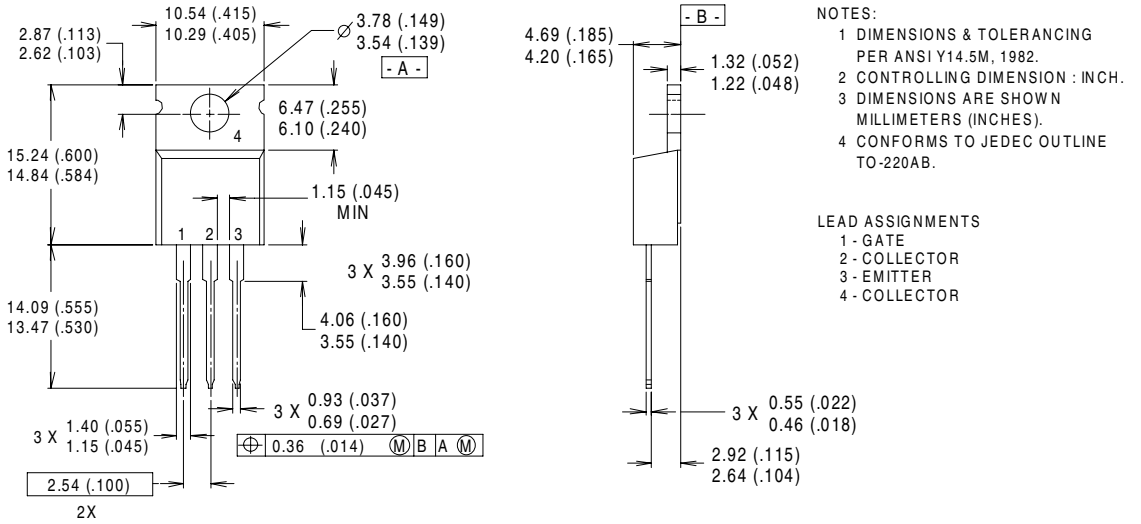


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

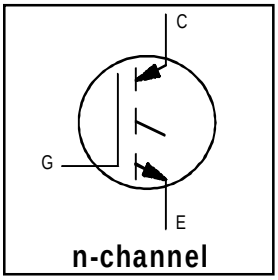
International
IOR Rectifier

PD - 91600A

IRG4BC20K

Short Circuit Rated
UltraFast IGBT

INSULATED GATE BIPOLAR TRANSISTOR



n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.27V

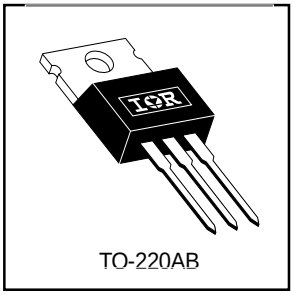
@V_{GE} = 15V, I_C = 9.0A

Features

- High short circuit rating optimized for motor control, t_{sc} =10µs, @360V V_{CE} (start), T_J = 125°C, V_{GE} = 15V
- Combines low conduction losses with high switching speed
- Latest generation design provides tighter parameter distribution and higher efficiency than previous generations

Benefits

- As a Freewheeling Diode we recommend our HEXFRED™ ultrafast, ultrasoft recovery diodes for minimum EMI / Noise and switching losses in the Diode and IGBT
- Latest generation 4 IGBTs offer highest power density motor controls possible
- This part replaces the IRGBC20K and IRGBC20M devices


TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	16	A
I_C @ T_C = 100°C	Continuous Collector Current	9.0	
I_{CM}	Pulsed Collector Current ①	32	
I_{LM}	Clamped Inductive Load Current ②	32	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	±20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	29	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	80	
Wt	Weight	2.0 (0.07)	—	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.49	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.00	—	V	I_C = 6.0A
		—	2.27	2.8		I_C = 9.0A, V_{GE} = 15V
		—	3.01	—		I_C = 16A, See Fig.2, 5
		—	2.43	—		I_C = 9.0A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	2.9	4.3	—	S	V_{CE} = 100 V, I_C = 9.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	34	51	nC	I_C = 9.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	4.9	7.4		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	14	21		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	28	—	ns	T_J = 25°C
t_r	Rise Time	—	27	—		I_C = 9.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	150	220		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	100	150		Energy losses include "tail"
E_{on}	Turn-On Switching Loss	—	0.15	—	mJ	See Fig. 9,10,14
E_{off}	Turn-Off Switching Loss	—	0.25	—		
E_{ts}	Total Switching Loss	—	0.40	0.6		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 400V, T_J = 125°C
						V_{GE} = 15V, R_G = 50Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	28	—	ns	T_J = 150°C,
t_r	Rise Time	—	29	—		I_C = 9.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	190	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	190	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.68	—	mJ	See Fig. 11,14
E_{on}	Turn-On Switching Loss	—	0.07	—	mJ	T_J = 25°C, V_{GE} = 15V, R_G = 50Ω
E_{off}	Turn-Off Switching Loss	—	0.13	—		I_C = 6.0A, V_{CC} = 480V
E_{ts}	Total Switching Loss	—	0.20	—		Energy losses include "tail"
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	450	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	61	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	14	—		f = 1.0MHz

Details of note ① through ⑤ are on the last page

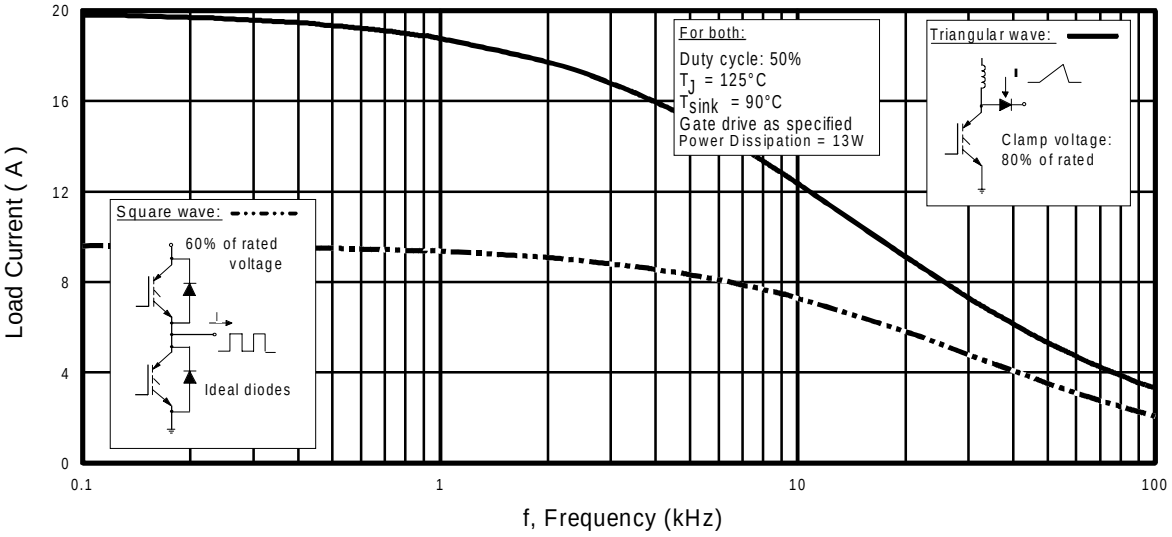


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

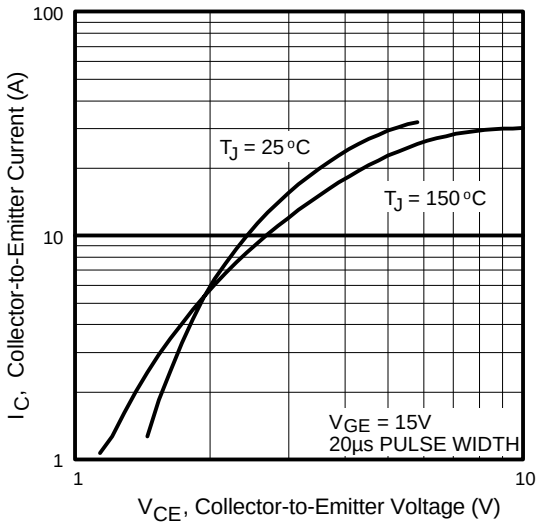


Fig. 2 - Typical Output Characteristics

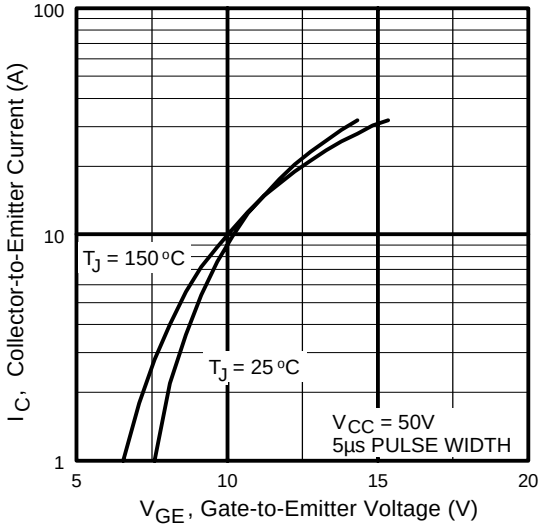


Fig. 3 - Typical Transfer Characteristics

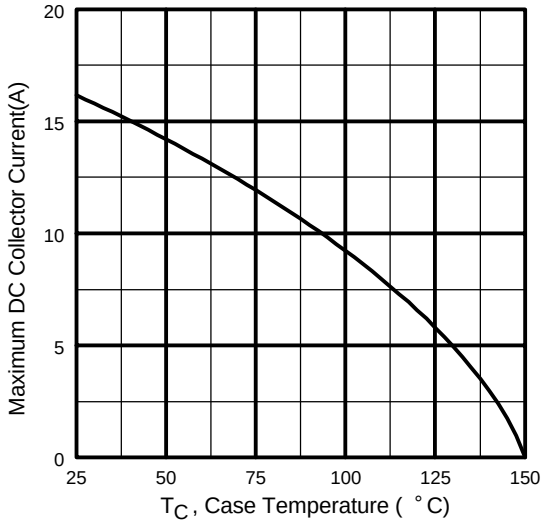


Fig. 4 - Maximum Collector Current vs. Case Temperature

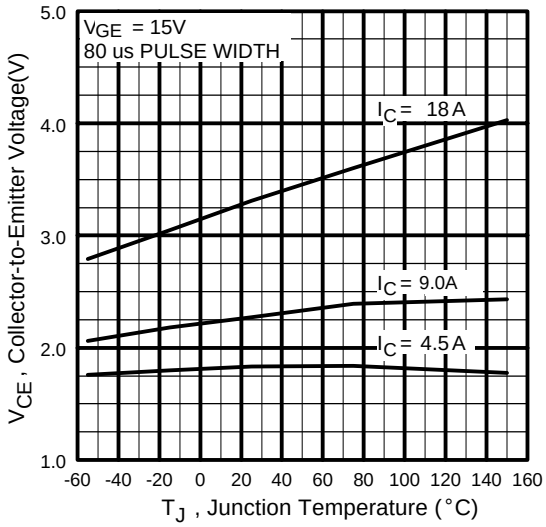


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

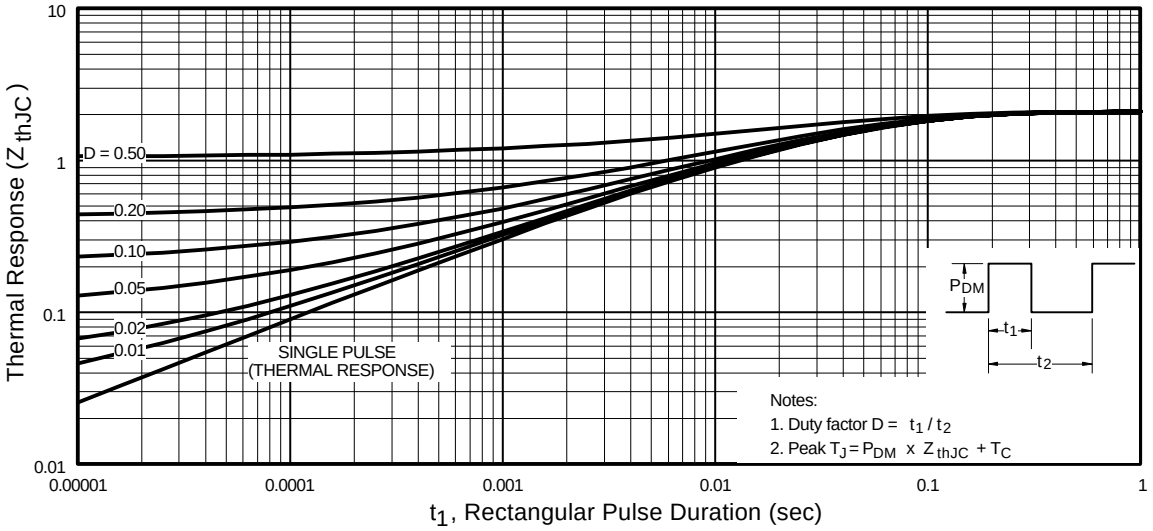


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

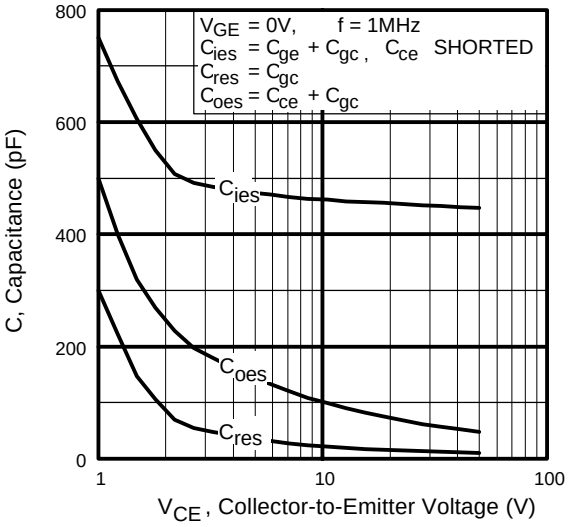


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

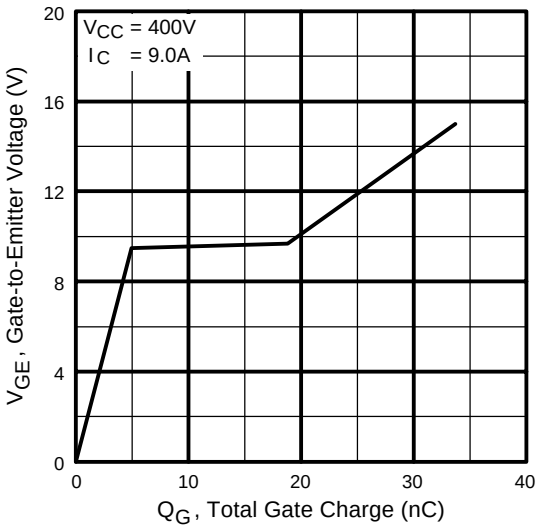


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

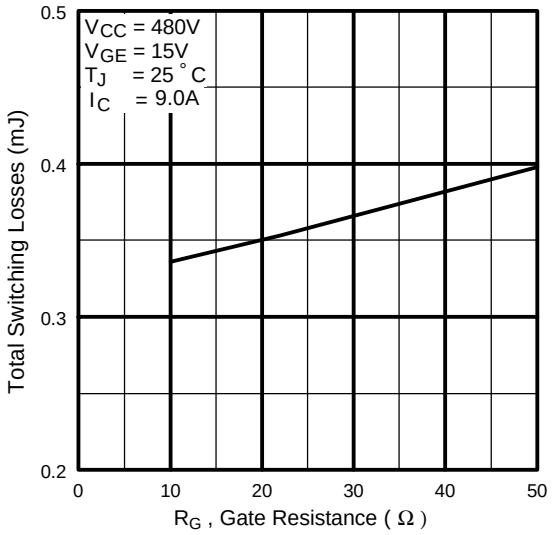


Fig. 9 - Typical Switching Losses vs. Gate Resistance

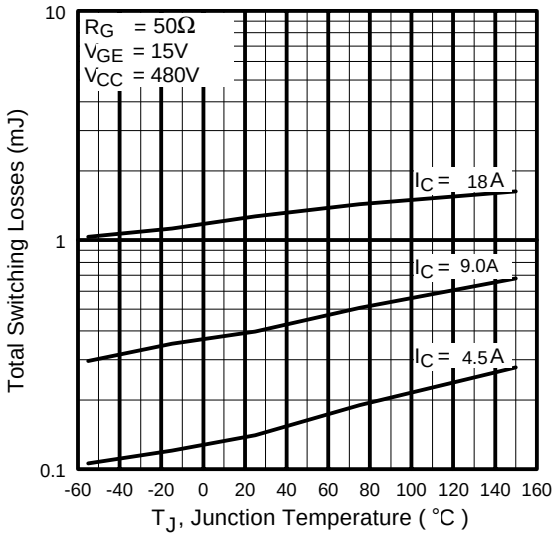


Fig. 10 - Typical Switching Losses vs. Junction Temperature

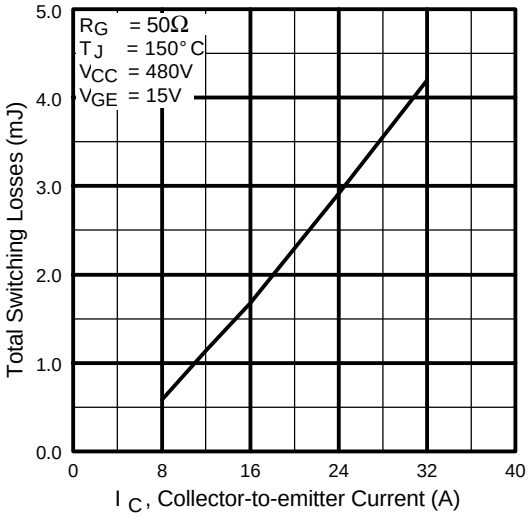


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

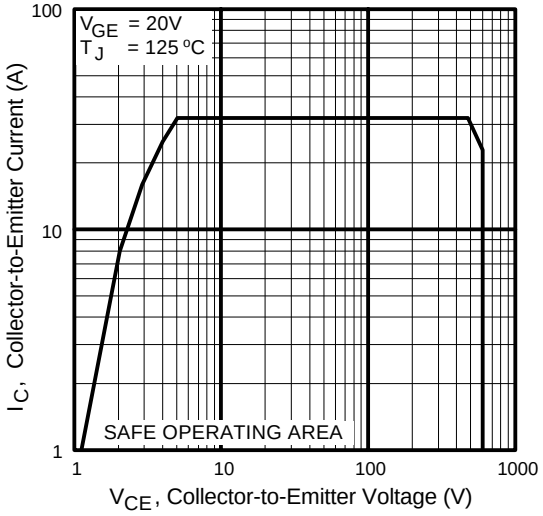


Fig. 12 - Turn-Off SOA

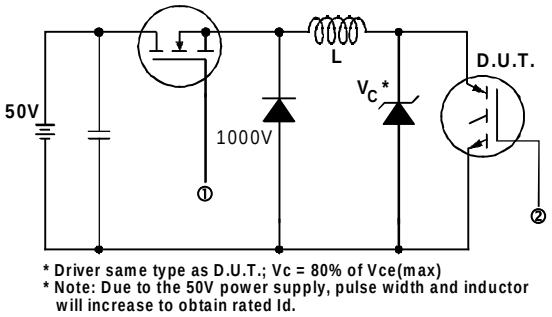


Fig. 13a - Clamped Inductive Load Test Circuit

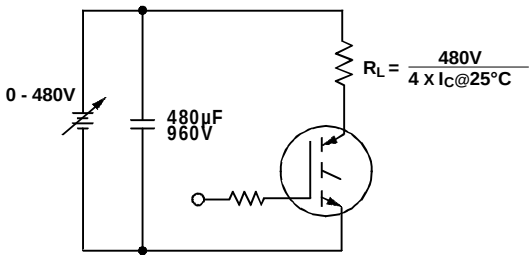


Fig. 13b - Pulsed Collector Current Test Circuit

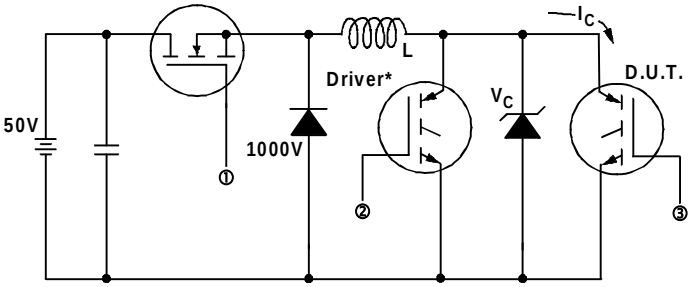


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

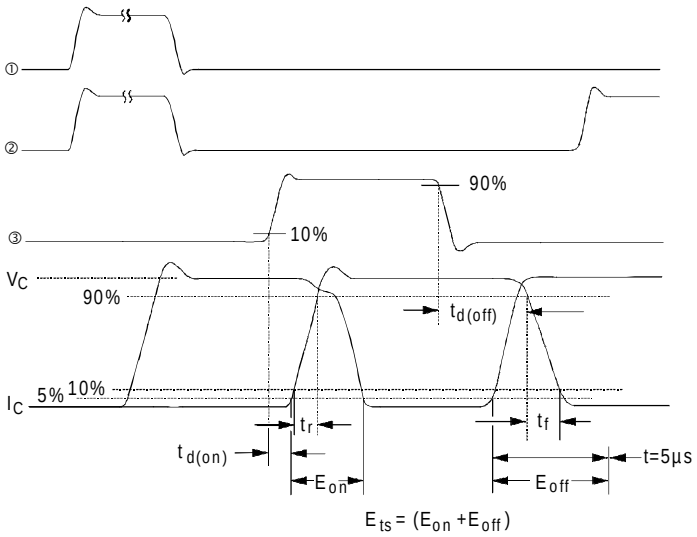


Fig. 14b - Switching Loss Waveforms

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

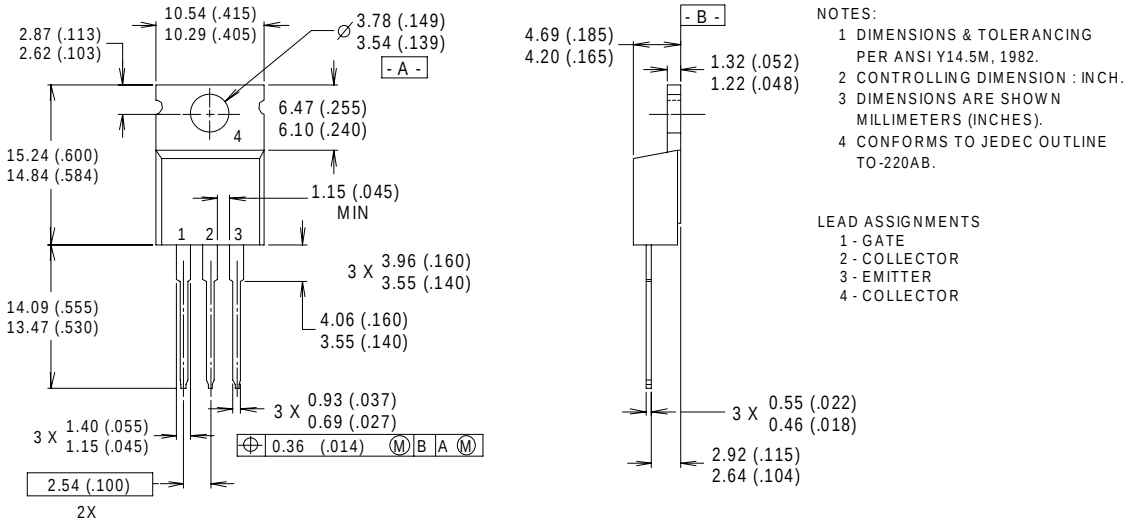
② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 50Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

Case Outline and Dimensions — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 10/00

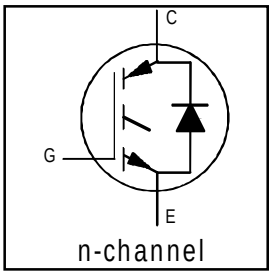
PD -91599A

International
IOR Rectifier

IRG4BC20KD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated UltraFast IGBT



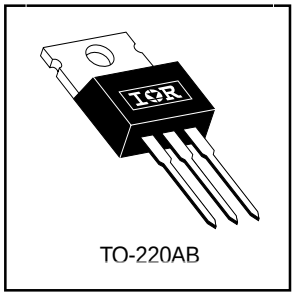
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.27V

@V_{GE} = 15V, I_C = 9.0A

Features

- Short Circuit Rated UltraFast: Optimized for high operating frequencies >5.0 kHz , and Short Circuit Rated to 10µs @ 125°C, V_{GE} = 15V
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than previous generation
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-220AB package



TO-220AB

Benefits

- Latest generation 4 IGBTs offer highest power density motor controls possible
- HEXFRED™ diodes optimized for performance with IGBTs. Minimized recovery characteristics reduce noise, EMI and switching losses
- This part replaces the IRGBC20KD2 and IRGBC20MD2 products
- For hints see design tip 97003

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	16	A
I_C @ T_C = 100°C	Continuous Collector Current	9.0	
I_{CM}	Pulsed Collector Current ①	32	
I_{LM}	Clamped Inductive Load Current ②	32	
I_F @ T_C = 100°C	Diode Continuous Forward Current	7.0	
I_{FM}	Diode Maximum Forward Current	32	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	——	——	2.1	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	——	——	3.5	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	——	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	——	80	
Wt	Weight	——	2 (0.07)	——	g (oz)

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.49	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.27	2.8	V	I_C = 9.0A V_{GE} = 15V
		—	3.01	—		I_C = 16A See Fig. 2, 5
		—	2.43	—		I_C = 9.0A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	2.9	4.3	—	S	V_{CE} = 100V, I_C = 9.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 8.0A See Fig. 13
		—	1.3	1.6		I_C = 8.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	34	51	nC	I_C = 9.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	4.9	7.4		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	14	21		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	54	—	ns	
t_r	Rise Time	—	34	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	180	270		I_C = 9.0A, V_{CC} = 480V
t_f	Fall Time	—	72	110		V_{GE} = 15V, R_G = 50Ω
E_{on}	Turn-On Switching Loss	—	0.34	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.30	—		and diode reverse recovery
E_{ts}	Total Switching Loss	—	0.64	0.96		See Fig. 9,10,14
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 360V, T_J = 125°C
						V_{GE} = 15V, R_G = 50Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	51	—	ns	T_J = 150°C, See Fig. 11,14
t_r	Rise Time	—	37	—		I_C = 9.0A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	220	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	160	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.85	—	mJ	and diode reverse recovery
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	450	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	61	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	14	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	37	55	ns	T_J = 25°C See Fig.
		—	55	90		T_J = 125°C 14 I_F = 8.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	5.0	A	T_J = 25°C See Fig.
		—	4.5	8.0		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	65	138	nC	T_J = 25°C See Fig.
		—	124	360		T_J = 125°C 16 di/dt = 200Aµs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	240	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	210	—		T_J = 125°C 17

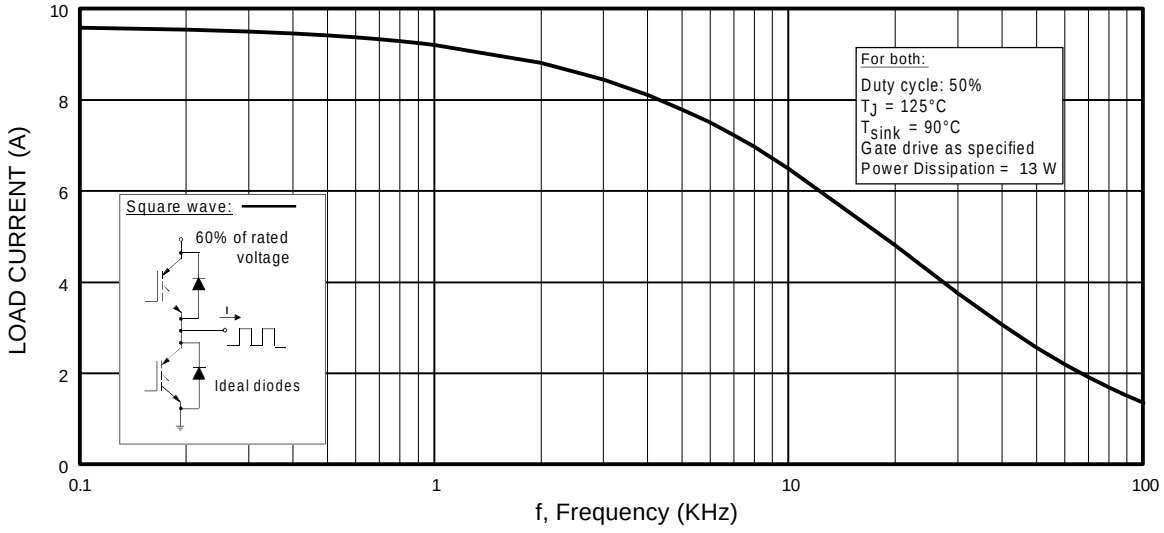


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

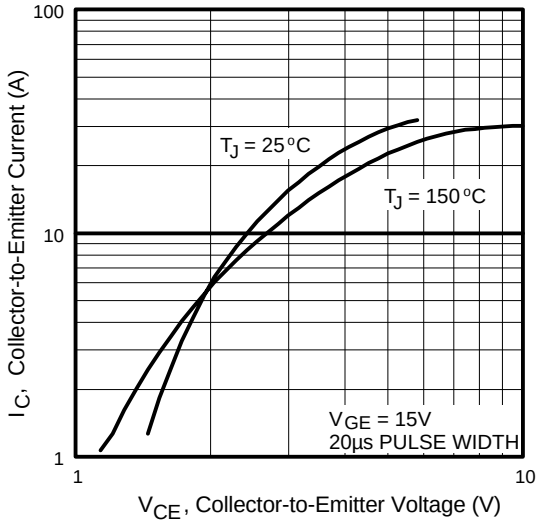


Fig. 2 - Typical Output Characteristics

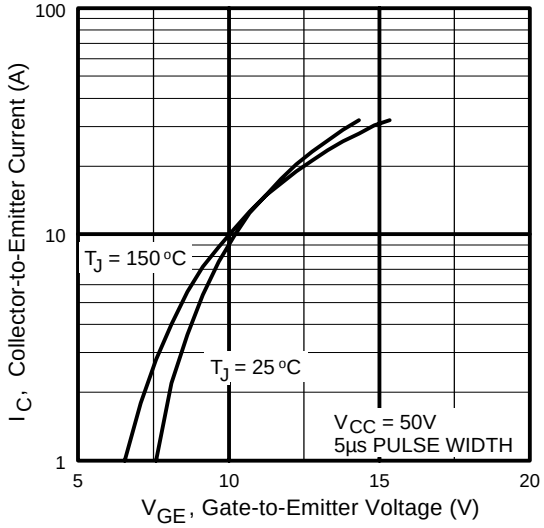


Fig. 3 - Typical Transfer Characteristics

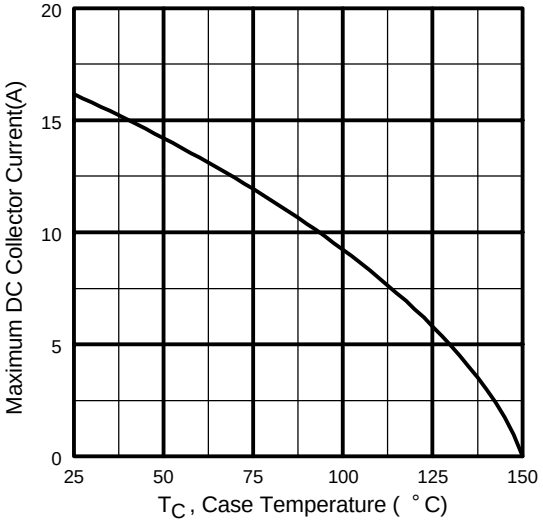


Fig. 4 - Maximum Collector Current vs. Case Temperature

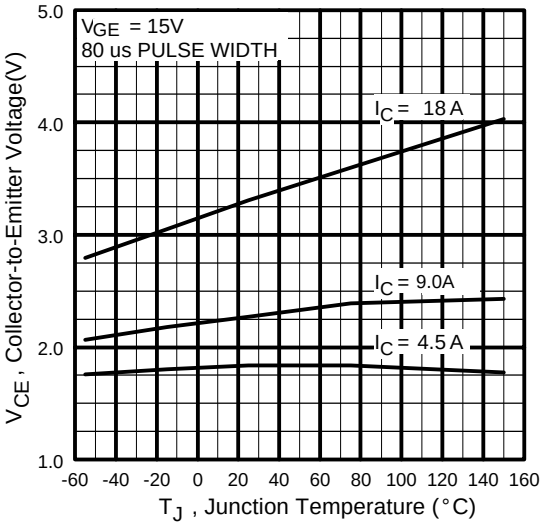


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

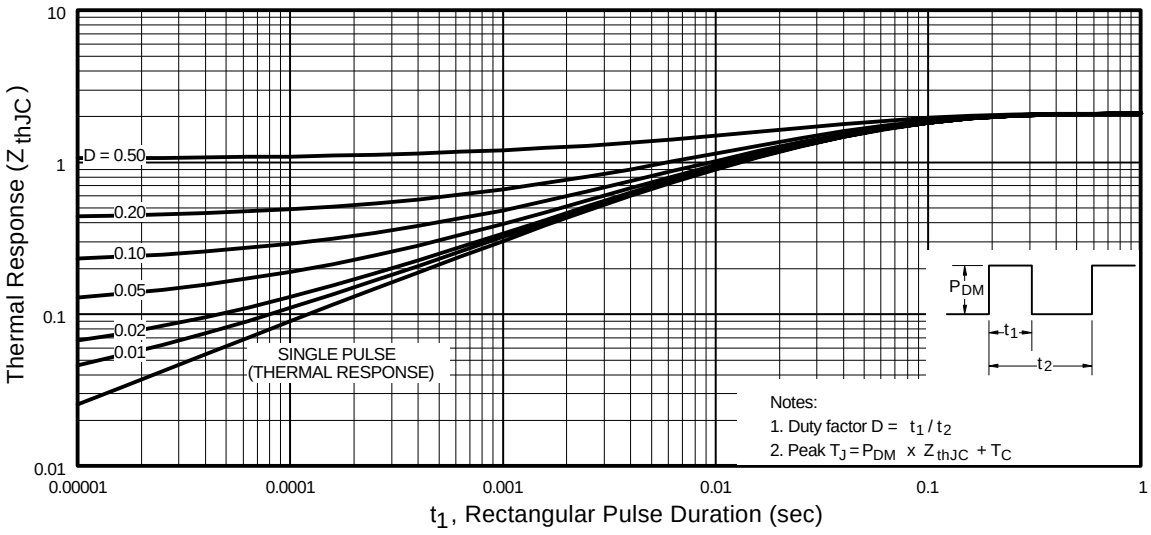


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

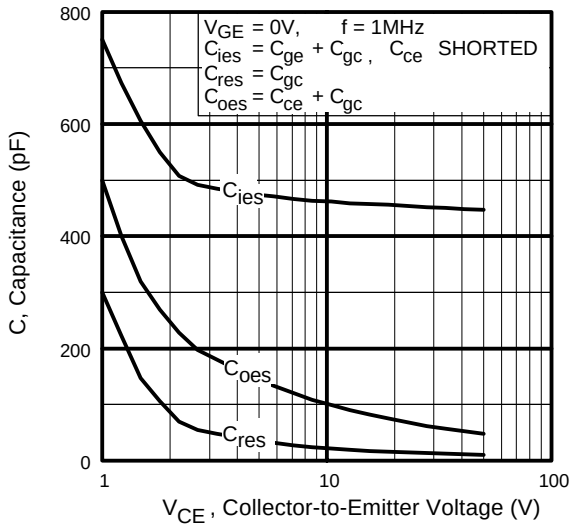


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

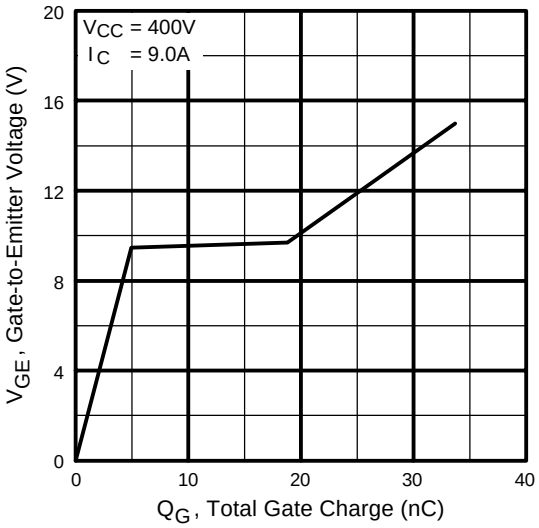


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

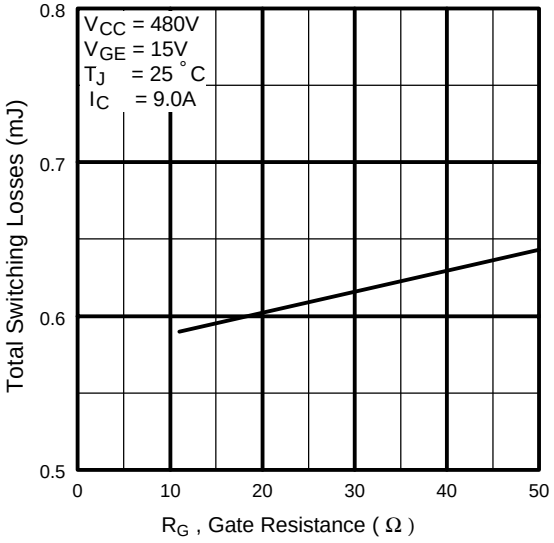


Fig. 9 - Typical Switching Losses vs. Gate Resistance

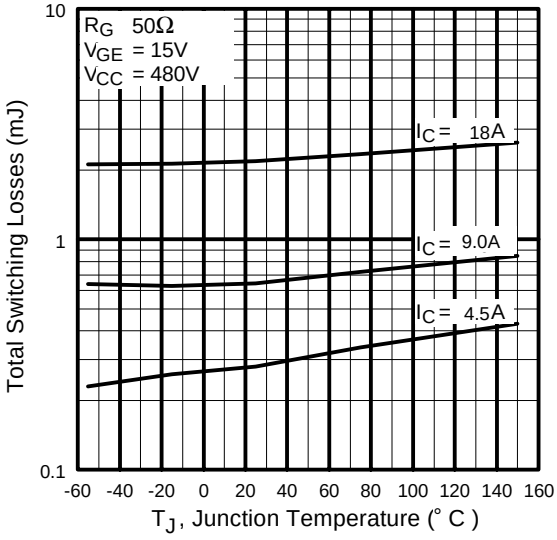


Fig. 10 - Typical Switching Losses vs. Junction Temperature

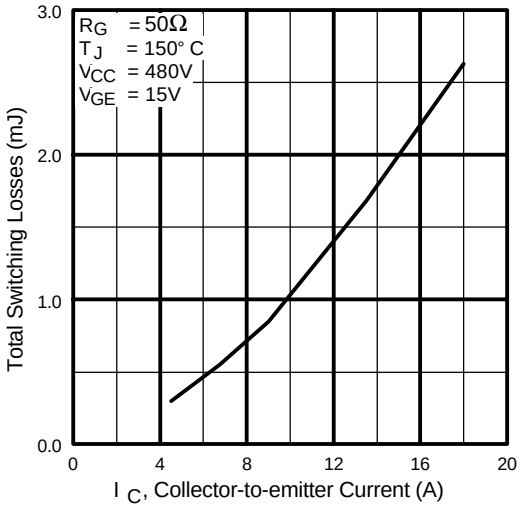


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

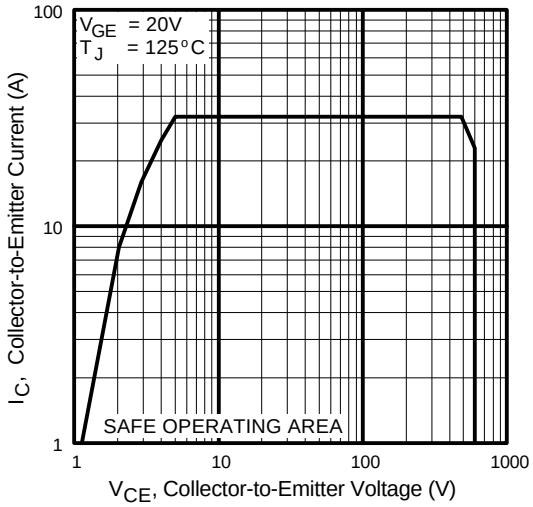


Fig. 12 - Turn-Off SOA

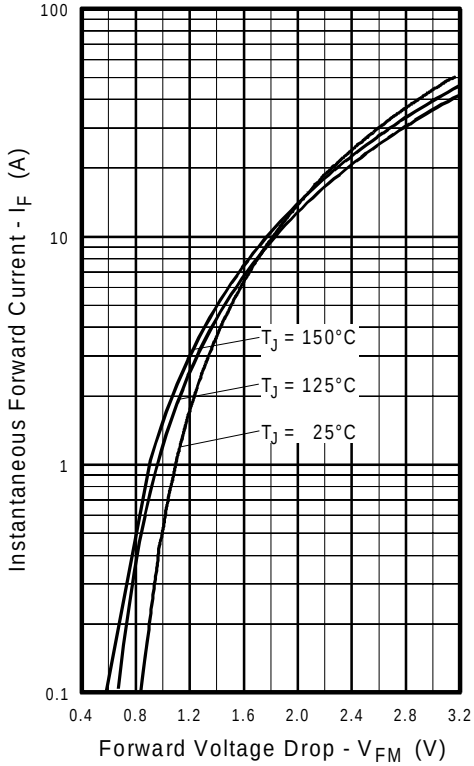


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

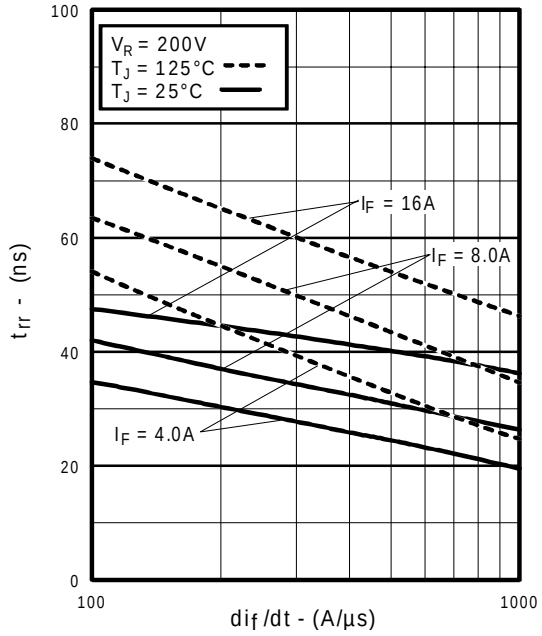


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

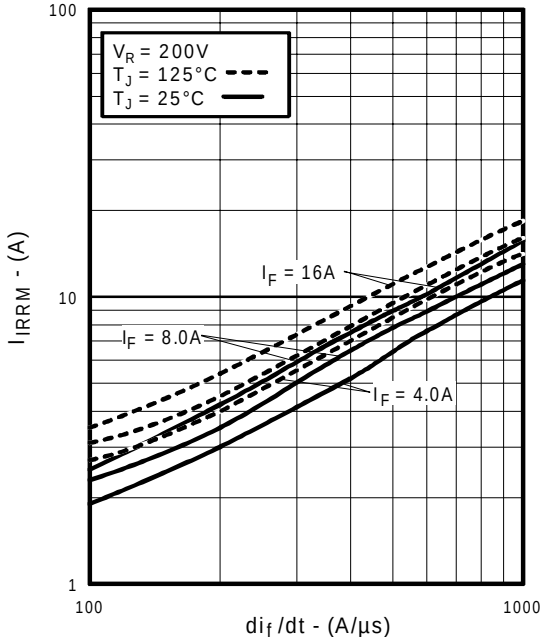


Fig. 15 - Typical Recovery Current vs. di_f/dt

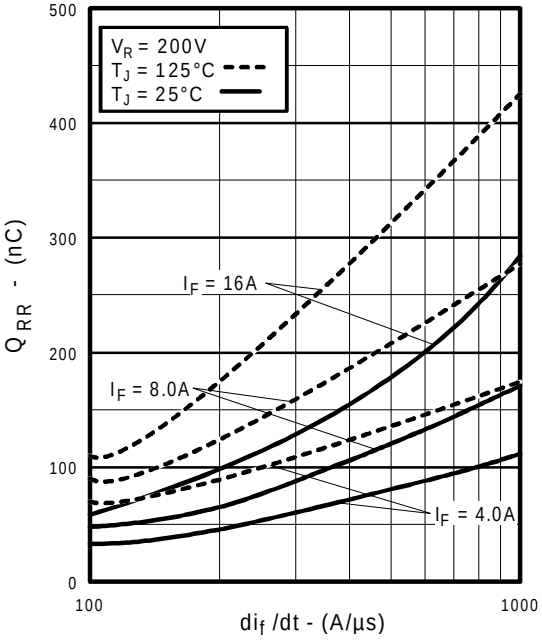


Fig. 16 - Typical Stored Charge vs. di_f/dt

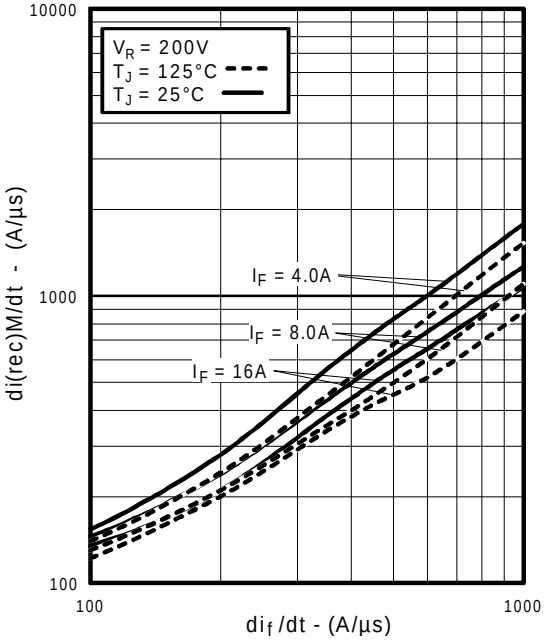


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

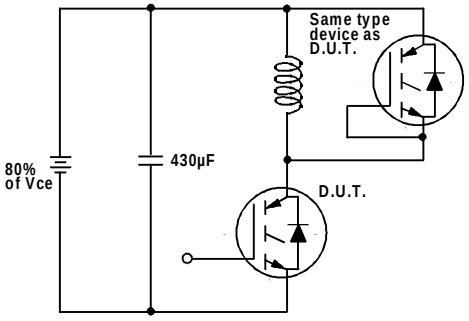


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

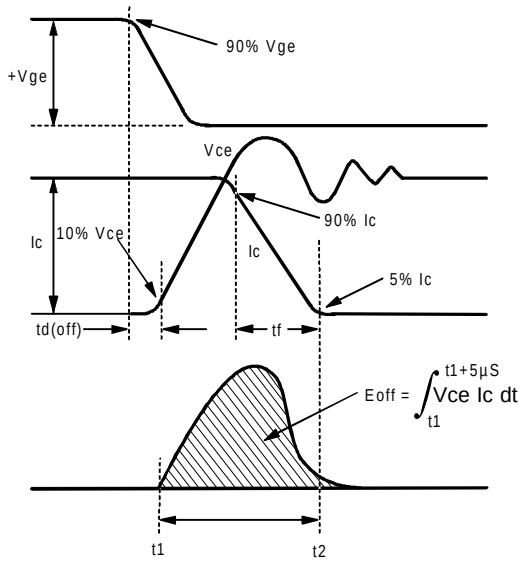


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

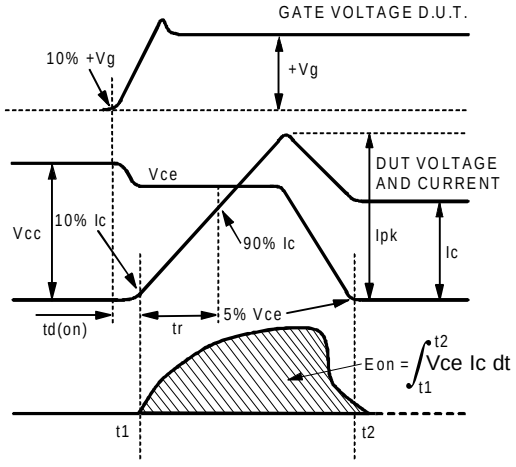


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

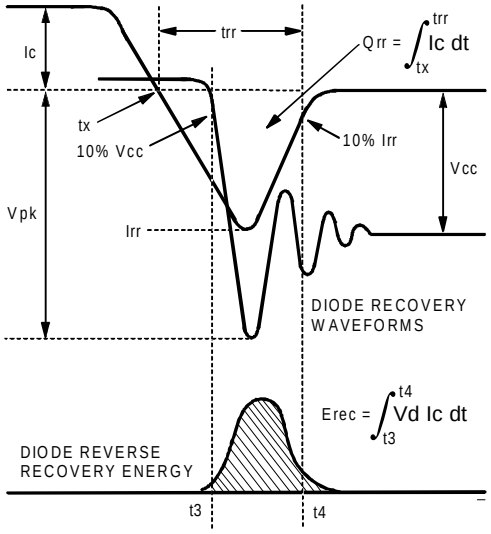


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

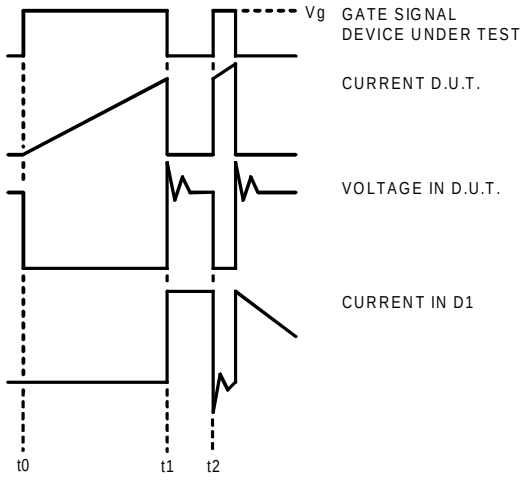


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

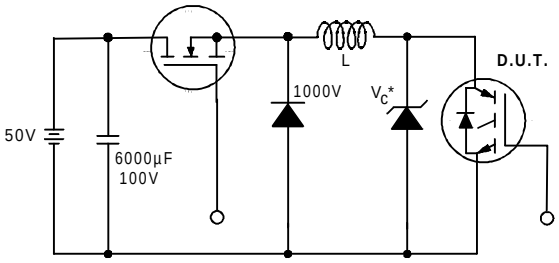


Figure 19. Clamped Inductive Load Test Circuit

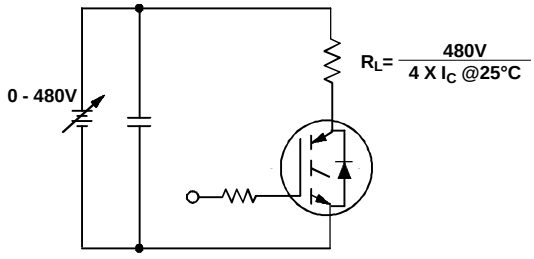


Figure 20. Pulsed Collector Current Test Circuit

Notes:

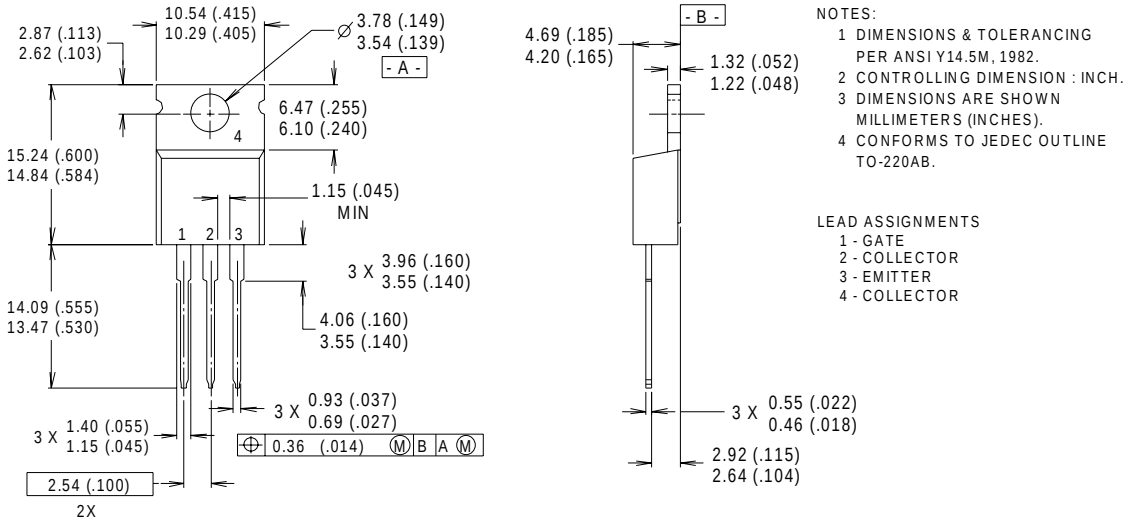
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 50Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB

Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

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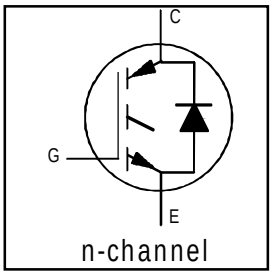
PD -91690A

International
IOR Rectifier

IRG4IBC30KD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
UltraFast IGBT



V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.21V

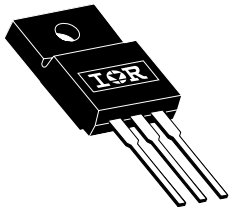
@V_{GE} = 15V, I_C = 9.2A

Features

- High switching speed optimized for up to 25kHz with low $V_{CE(on)}$
- Short Circuit Rating 10µs @ 125°C, V_{GE} = 15V
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than previous generation
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-220 FULLPAK

Benefits

- Generation 4 IGBTs offer highest efficiencies available maximizing the power density of the system
- IGBT's optimized for specific application conditions
- HEXFRED™ diodes optimized for performance with IGBTs. Minimized recovery characteristics reduce noise EMI
- Designed to exceed the power handling capability of equivalent industry-standard IGBT



TO-220 FULLPAK

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	17	A
I_C @ T_C = 100°C	Continuous Collector Current	9.2	
I_{CM}	Pulsed Collector Current ①⑤	34	
I_{LM}	Clamped Inductive Load Current ②⑤	34	
I_F @ T_C = 100°C	Diode Continuous Forward Current	9.2	
I_{FM}	Diode Maximum Forward Current	34	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{ISOL}	RMS Isolation Voltage, Terminal to Case, t = 1 min	2500	V
V_{GE}	Gate-to-Emitter Voltage	± 20	
P_D @ T_C = 25°C	Maximum Power Dissipation	45	W
P_D @ T_C = 100°C	Maximum Power Dissipation	18	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	2.8	°C/W
$R_{\theta CS}$	Junction-to-Case - Diode	—	3.7	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	65	
Wt	Weight	2.0 (0.07)	—	g (oz)

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.54	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.21	2.7	V	I_C = 16A V_{GE} = 15V
		—	2.88	—		I_C = 28A See Fig. 2, 5
		—	2.36	—		I_C = 16A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-12	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	5.4	8.1	—	S	V_{CE} = 100V, I_C = 16A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 12A See Fig. 13
		—	1.3	1.6		I_C = 12A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	67	100	nC	I_C = 16A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	11	16		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	25	37		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	60	—	ns	
t_r	Rise Time	—	42	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	160	250		I_C = 16A, V_{CC} = 480V
t_f	Fall Time	—	80	120		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.60	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.58	—		and diode reverse recovery
E_{ts}	Total Switching Loss	—	1.18	1.6		See Fig. 9,10,14
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 360V, T_J = 125°C
						V_{GE} = 15V, R_G = 10Ω , V_{CPK} < 500V
$t_{d(on)}$	Turn-On Delay Time	—	58	—	ns	T_J = 150°C, See Fig. 10,11,18
t_r	Rise Time	—	42	—		I_C = 16A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	210	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	160	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.69	—	mJ	and diode reverse recovery
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	920	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	110	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	27	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	42	60	ns	T_J = 25°C See Fig. 14 I_F = 12A
		—	80	120		T_J = 125°C
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	6.0	A	T_J = 25°C See Fig. 15 V_R = 200V
		—	5.6	10		T_J = 125°C
Q_{rr}	Diode Reverse Recovery Charge	—	80	180	nC	T_J = 25°C See Fig. 16 di/dt = 200Aµs
		—	220	600		T_J = 125°C
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	180	—	A/µs	T_J = 25°C See Fig. 17
	During t_b	—	160	—		T_J = 125°C

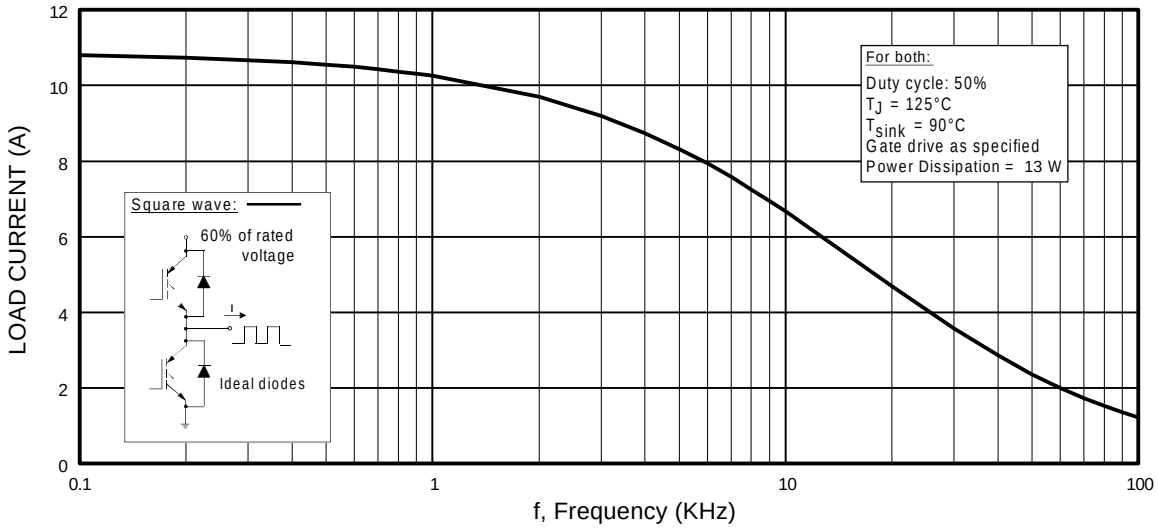


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

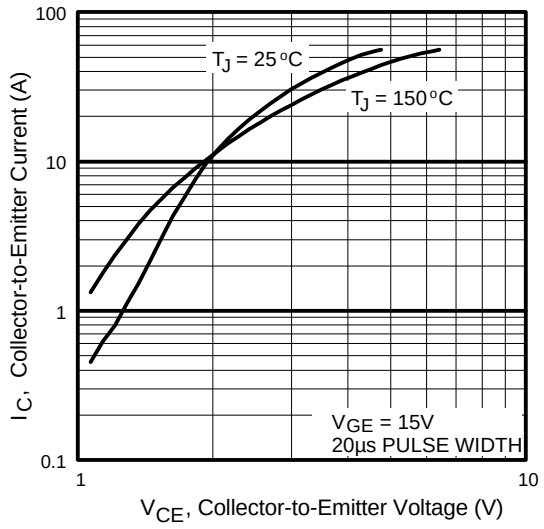


Fig. 2 - Typical Output Characteristics

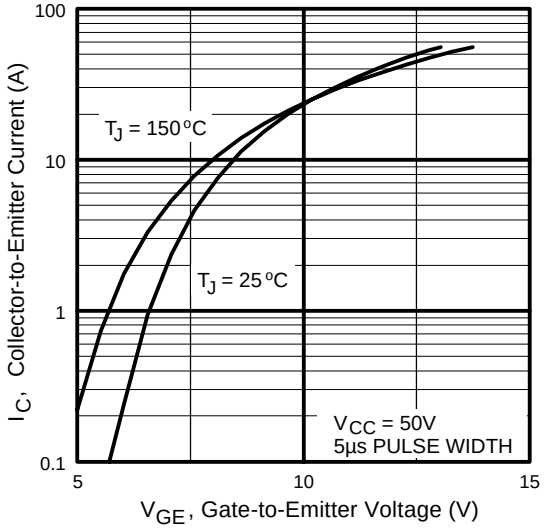


Fig. 3 - Typical Transfer Characteristics

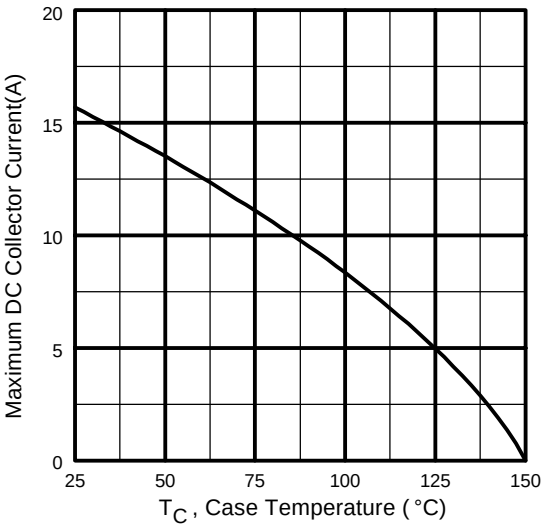


Fig. 4 - Maximum Collector Current vs. Case Temperature

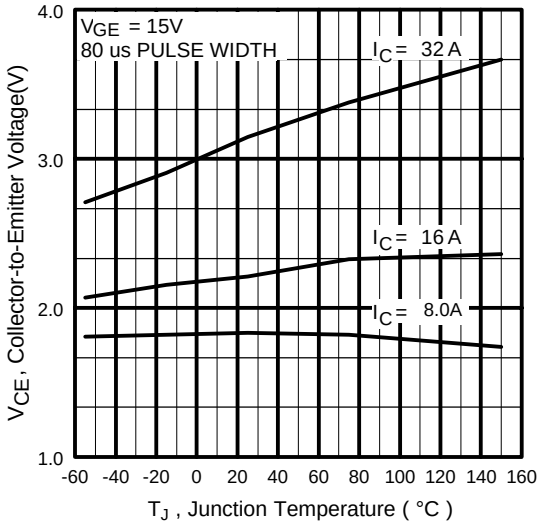


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

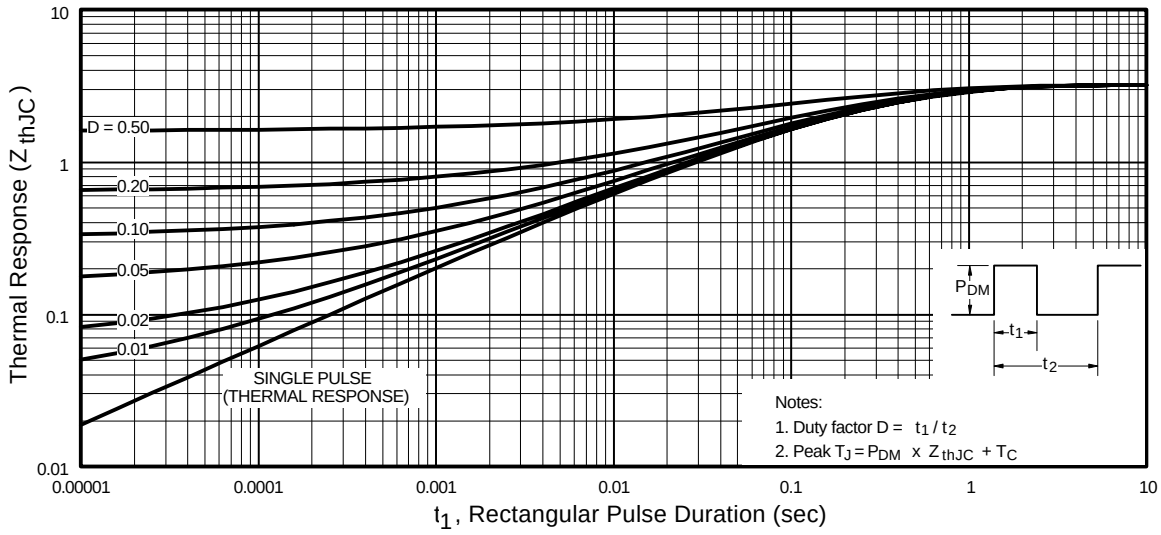


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

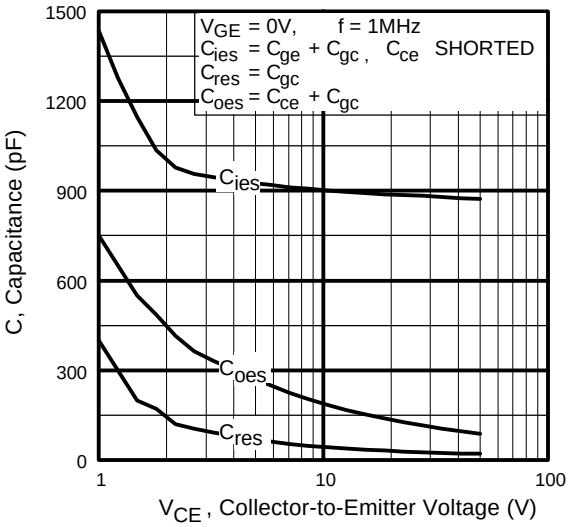


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

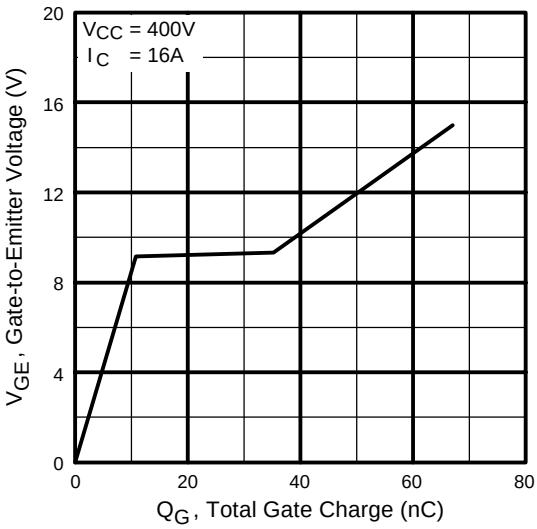


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

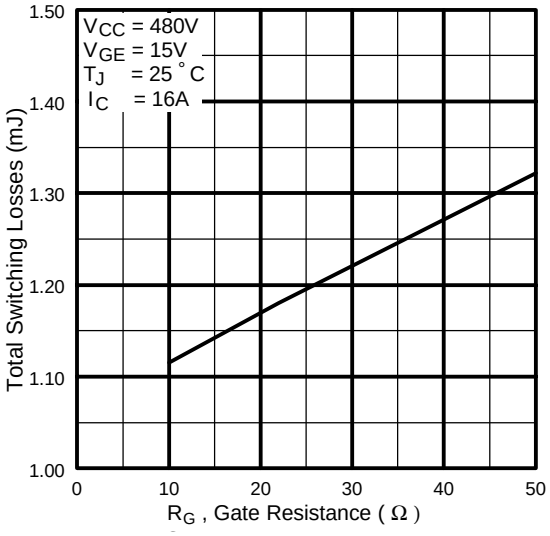


Fig. 9 - Typical Switching Losses vs. Gate Resistance

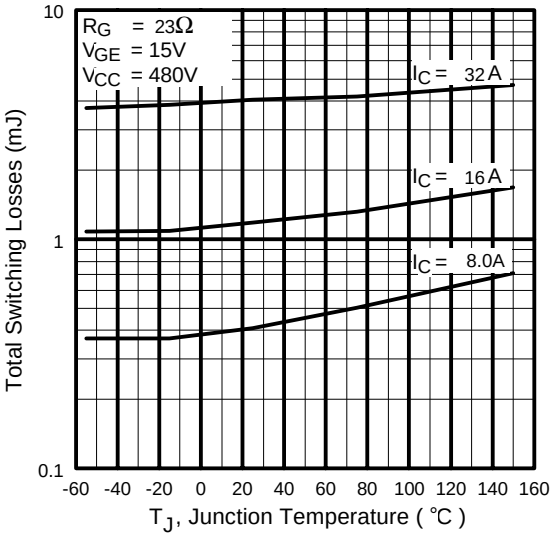


Fig. 10 - Typical Switching Losses vs. Junction Temperature

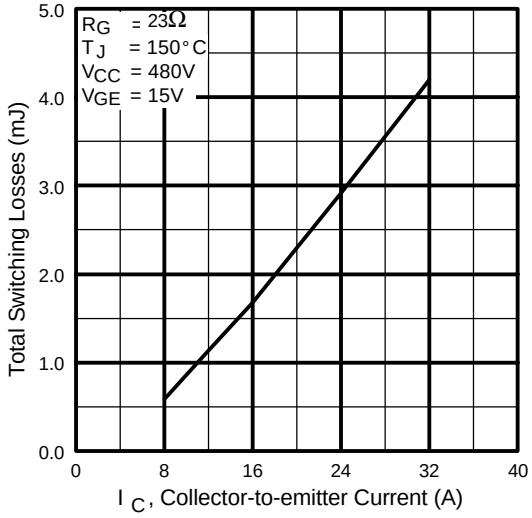


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

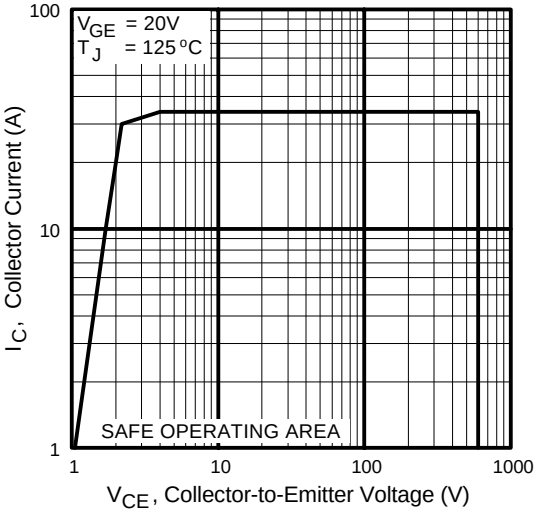


Fig. 12 - Turn-Off SOA

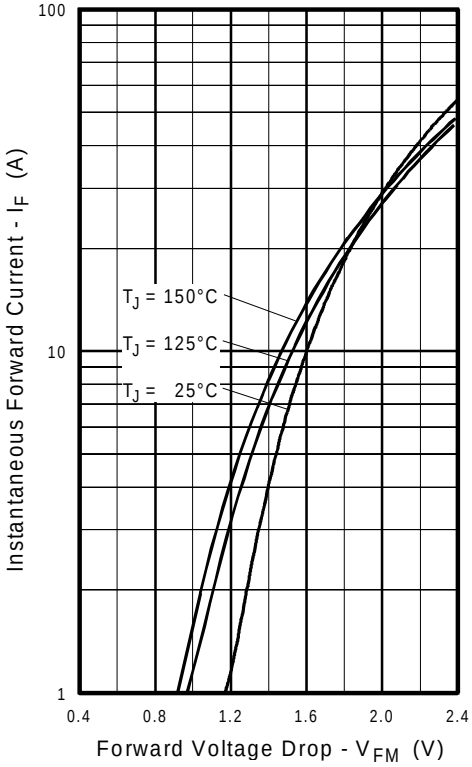


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

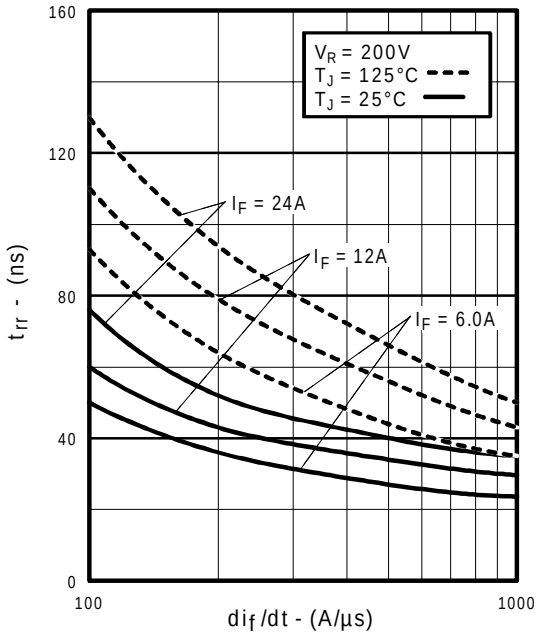


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

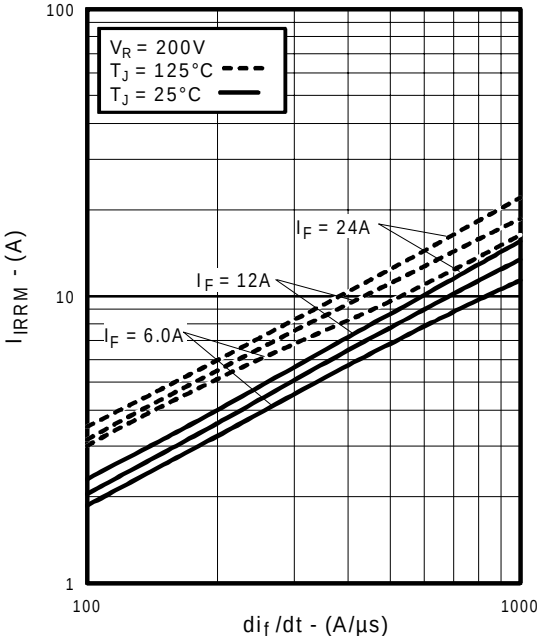


Fig. 15 - Typical Recovery Current vs. di_f/dt

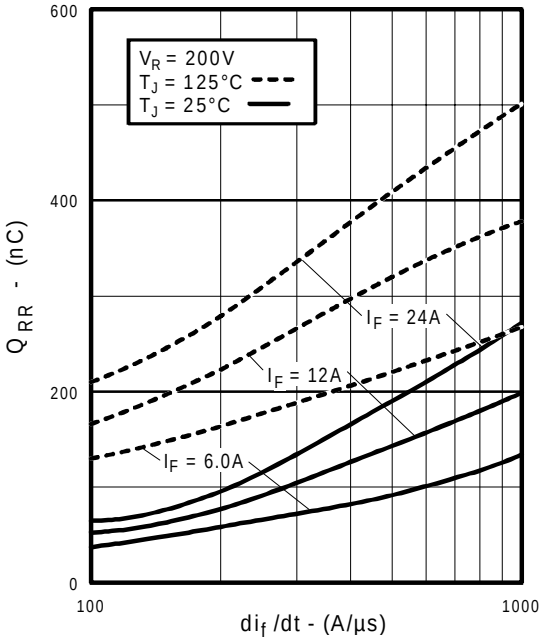


Fig. 16 - Typical Stored Charge vs. di_f/dt

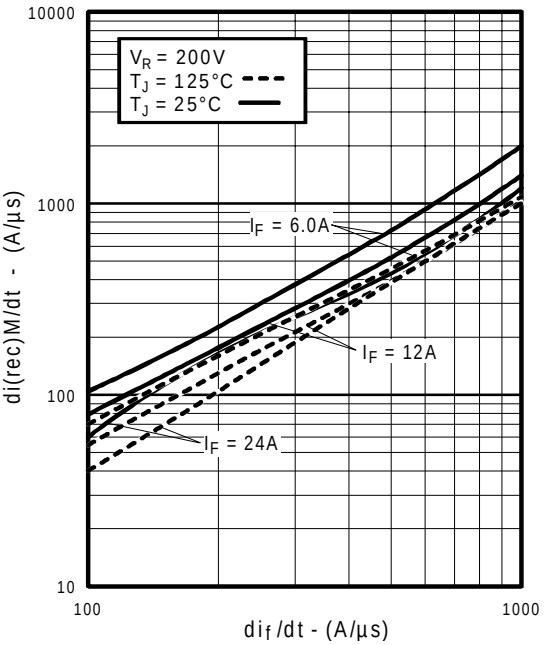


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

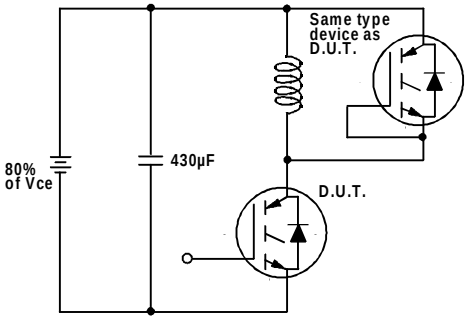


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

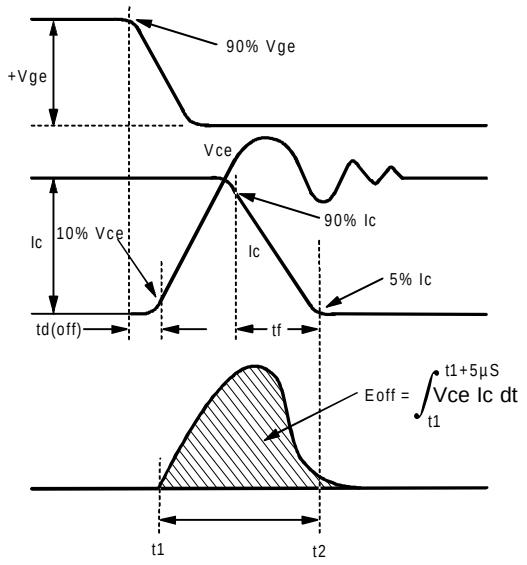


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

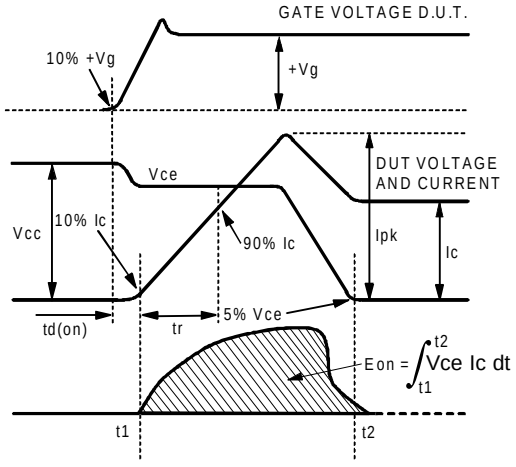


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

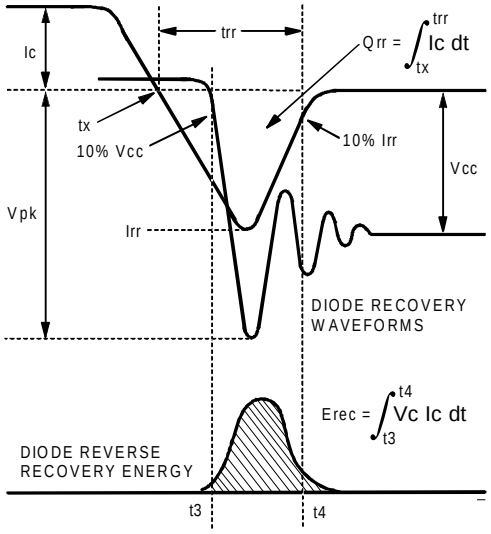


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

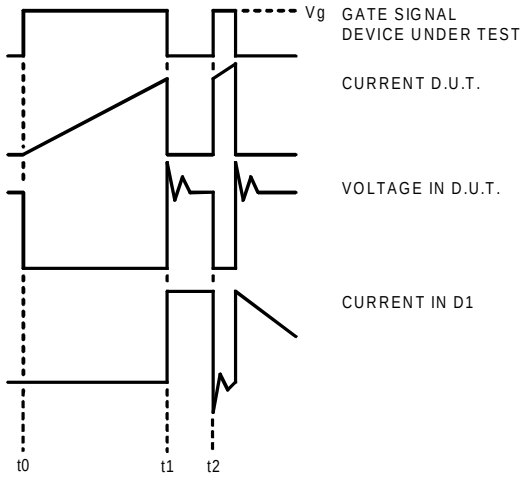


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

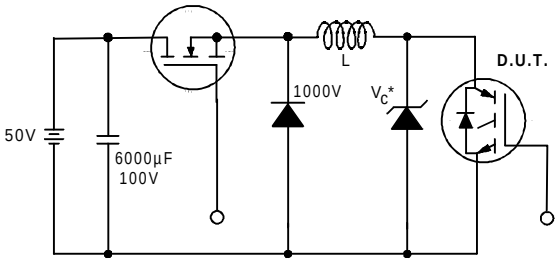


Figure 19. Clamped Inductive Load Test Circuit

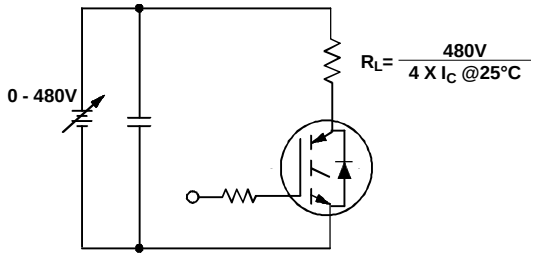


Figure 20. Pulsed Collector Current Test Circuit

Notes:

① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

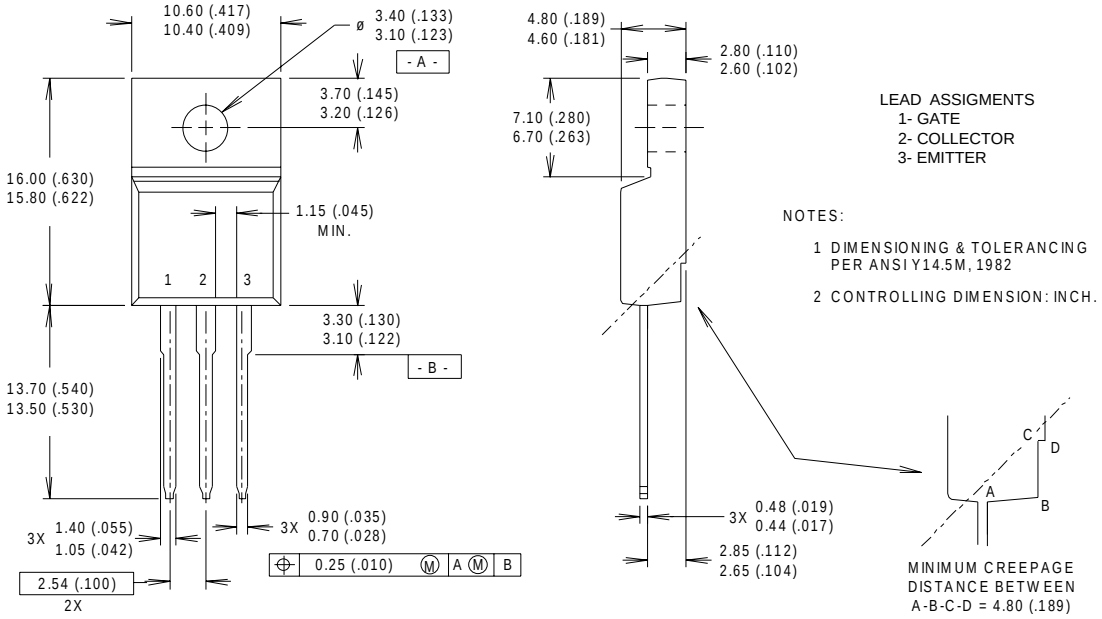
② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 23Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

⑤ Uses IRG4BC30KD data and test conditions

Case Outline — TO-220 FULLPAK



International
IOR Rectifier

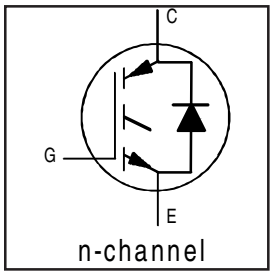
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IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
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IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 10/00

International
IOR Rectifier

IRG4IBC30UD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

UltraFast CoPack IGBT



n-channel

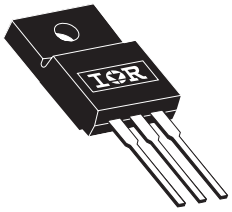
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.95V

@V_{GE} = 15V, I_C = 12A

Features

- 2.5kV, 60s insulation voltage ⑤
- 4.8 mm creapage distance to heatsink
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- IGBT co-packaged with HEXFRED™ ultrafast, ultrasoft recovery antiparallel diodes
- Tighter parameter distribution
- Industry standard Isolated TO-220 Fullpak™ outline


TO-220 FULLPAK

Benefits

- Simplified assembly
- Highest efficiency and power density
- HEXFRED™ antiparallel Diode minimizes switching losses and EMI

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	17	A
I_C @ T_C = 100°C	Continuous Collector Current	8.9	
I_{CM}	Pulsed Collector Current ①	92	
I_{LM}	Clamped Inductive Load Current ②	92	
I_F @ T_C = 100°C	Diode Continuous Forward Current	8.5	
I_{FM}	Diode Maximum Forward Current	92	
Visol	RMS Isolation Voltage, Terminal to Case⑤	2500	V
V_{GE}	Gate-to-Emitter Voltage	± 20	
P_D @ T_C = 25°C	Maximum Power Dissipation	45	W
P_D @ T_C = 100°C	Maximum Power Dissipation	18	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	2.8	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	4.1	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	65	
Wt	Weight	2.0 (0.07)	—	g (oz)

7/17/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage ƒ	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.63	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.95	2.1	V	I_C = 12A V_{GE} = 15V
		—	2.52	—		I_C = 23A See Fig. 2, 5
		—	2.09	—		I_C = 12A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	3.1	8.6	—	S	V_{CE} = 100V, I_C = 12A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 12A See Fig. 13
		—	1.3	1.6		I_C = 12A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	50	75		I_C = 12A
Qge	Gate - Emitter Charge (turn-on)	—	8.1	12	nC	V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	18	27		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	40	—		T_J = 25°C
t_r	Rise Time	—	21	—	ns	I_C = 12A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	91	140		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	80	130		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	0.38	—		diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	0.16	—	mJ	See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	—	0.54	0.9		
$t_{d(on)}$	Turn-On Delay Time	—	40	—		T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	—	22	—	ns	I_C = 12A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	120	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	180	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	0.89	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1100	—		V_{GE} = 0V
C_{oes}	Output Capacitance	—	73	—	pF	V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	14	—		ƒ = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	42	60	ns	T_J = 25°C See Fig.
		—	80	120		T_J = 125°C 14 I_F = 12A
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	6.0	A	T_J = 25°C See Fig.
		—	5.6	10		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	80	180	nC	T_J = 25°C See Fig.
		—	220	600		T_J = 125°C 16 di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	180	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	120	—		T_J = 125°C 17

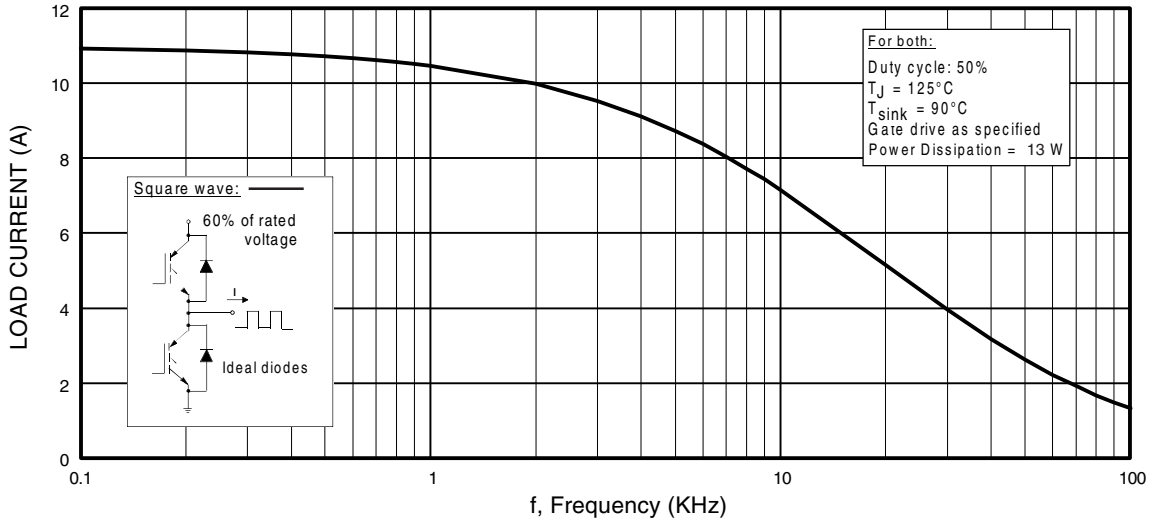


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

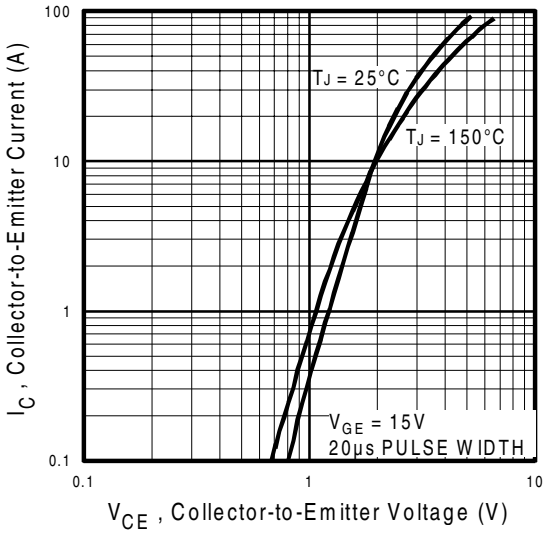


Fig. 2 - Typical Output Characteristics

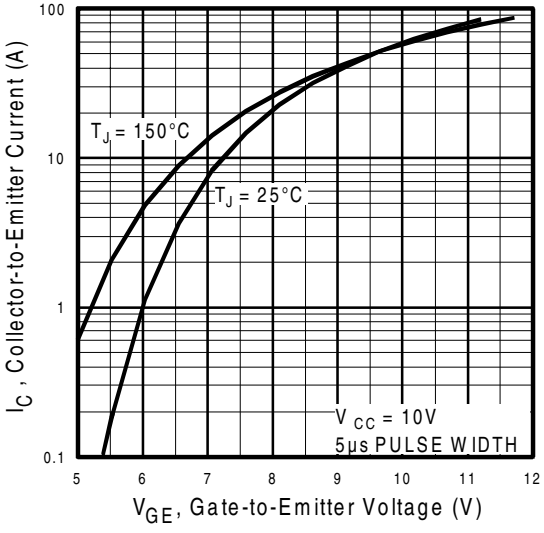


Fig. 3 - Typical Transfer Characteristics

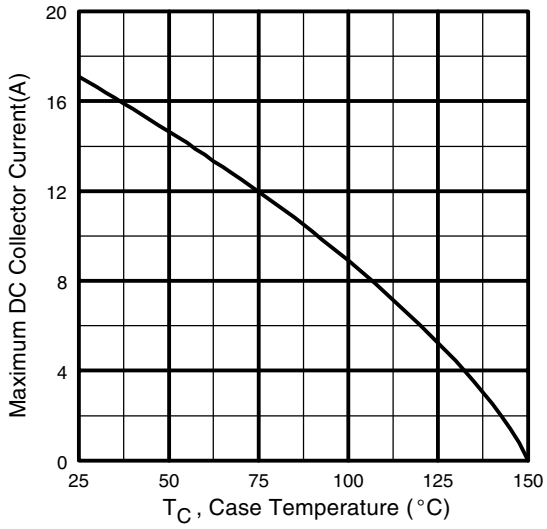


Fig. 4 - Maximum Collector Current vs. Case Temperature

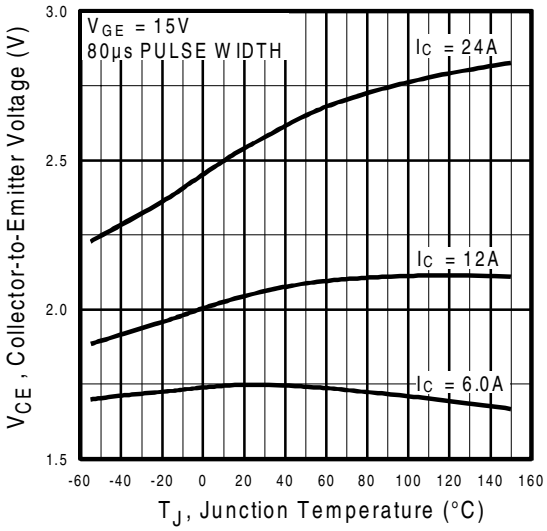


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

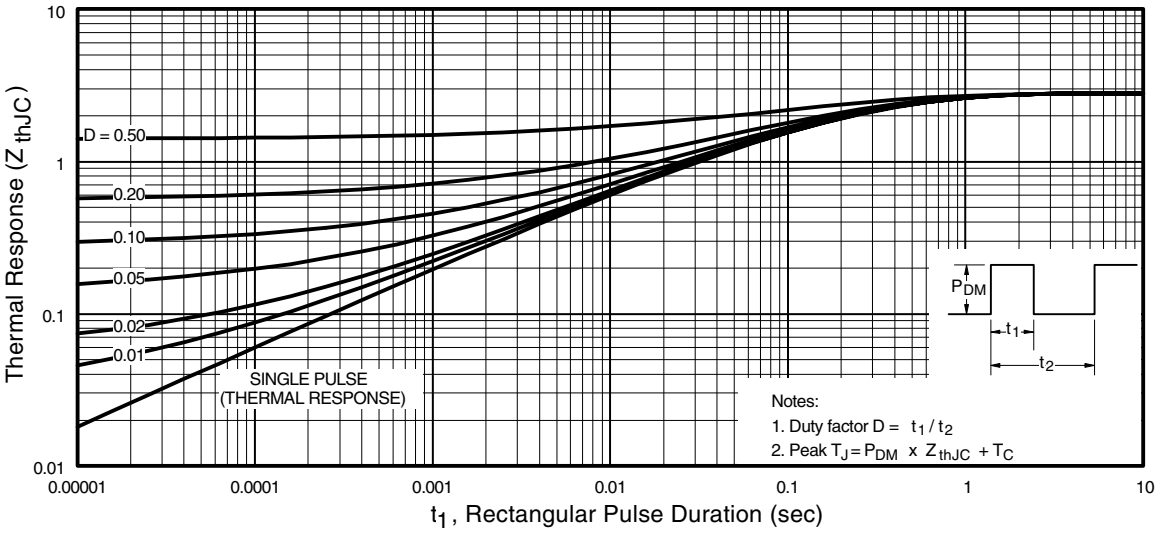


Fig. 6 - Maximum IGBT Effective Transient Thermal Impedance, Junction-to-Case

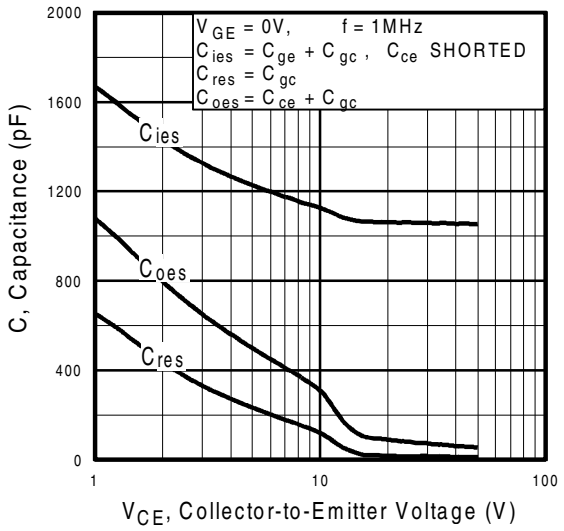


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

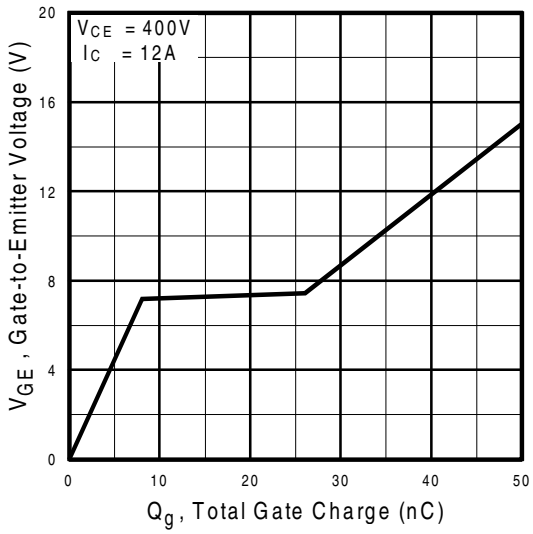


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

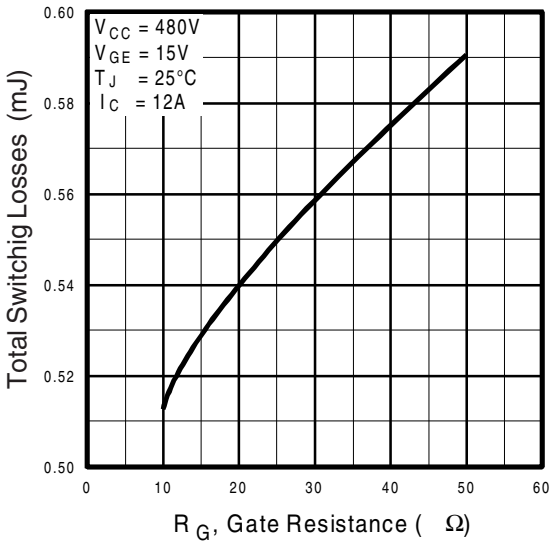


Fig. 9 - Typical Switching Losses vs. Gate Resistance

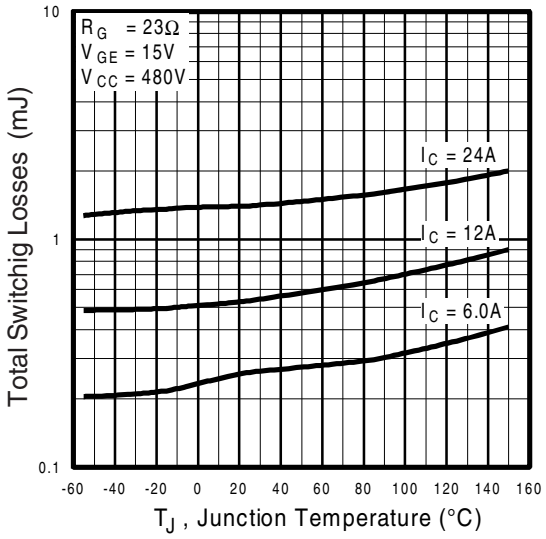


Fig. 10 - Typical Switching Losses vs. Junction Temperature

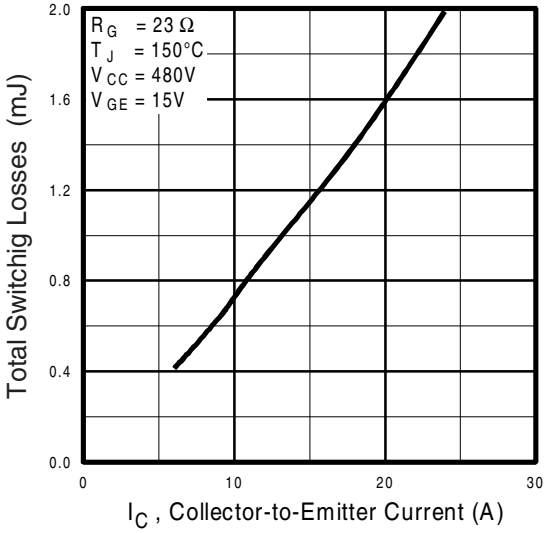


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

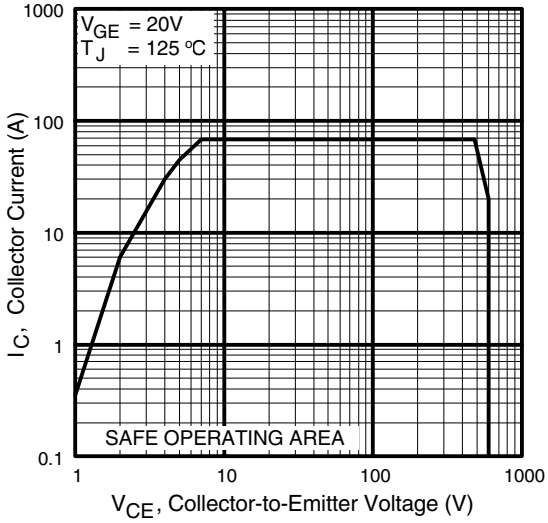


Fig. 12 - Turn-Off SOA

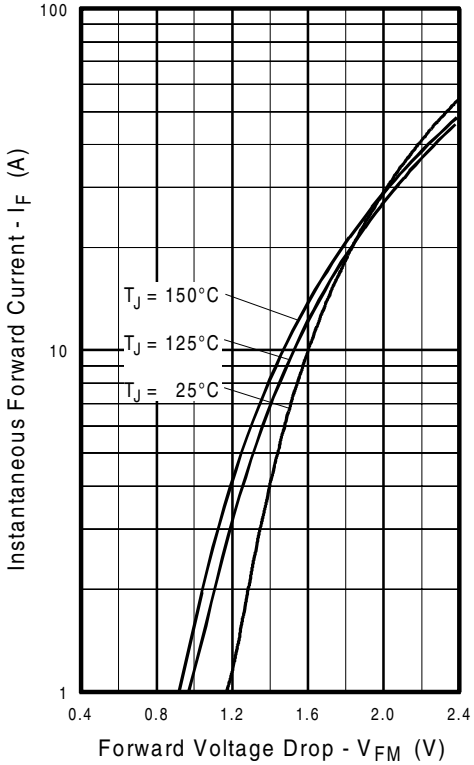


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

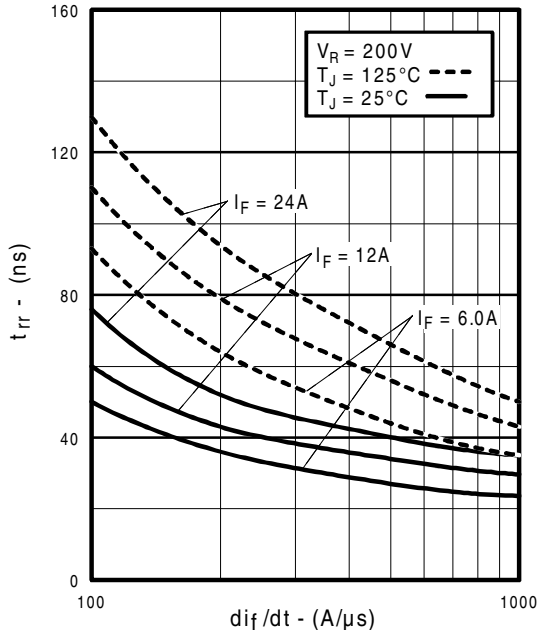


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

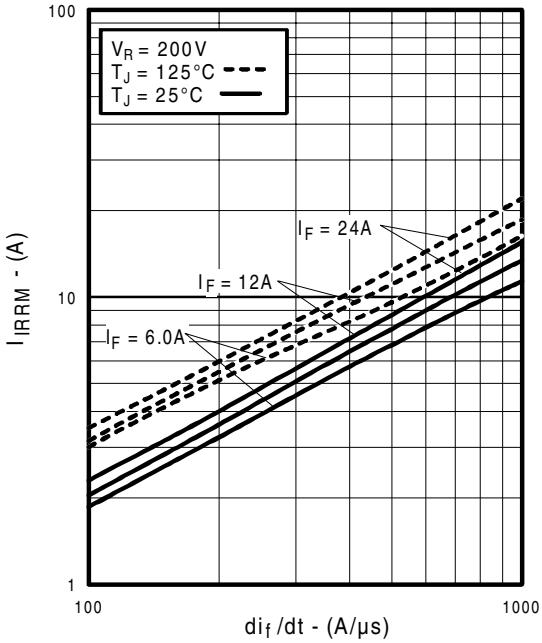


Fig. 15 - Typical Recovery Current vs. di_f/dt

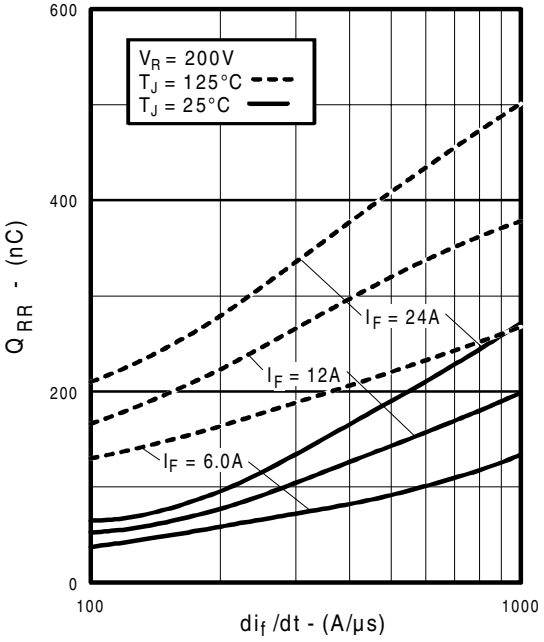


Fig. 16 - Typical Stored Charge vs. di_f/dt

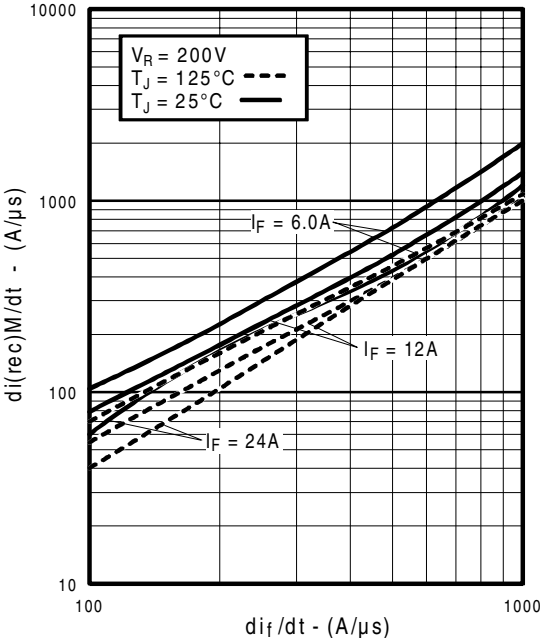


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

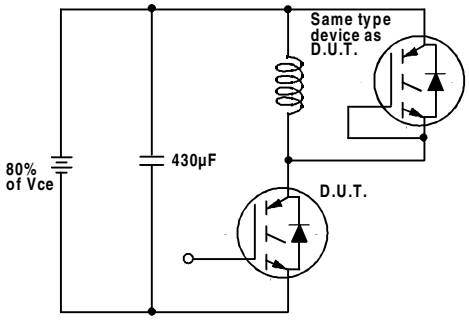


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

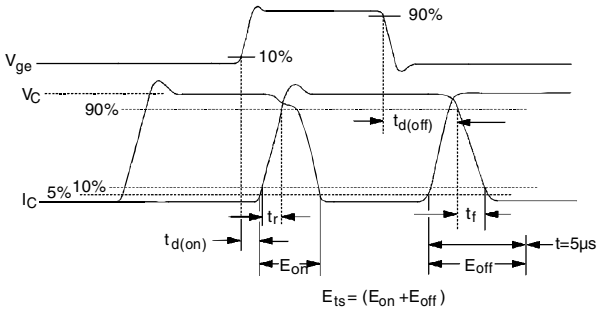


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

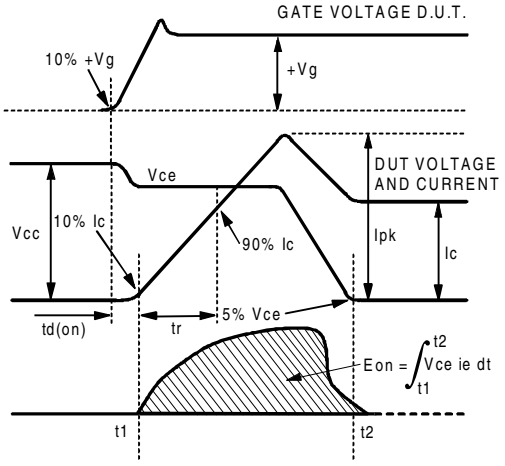


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

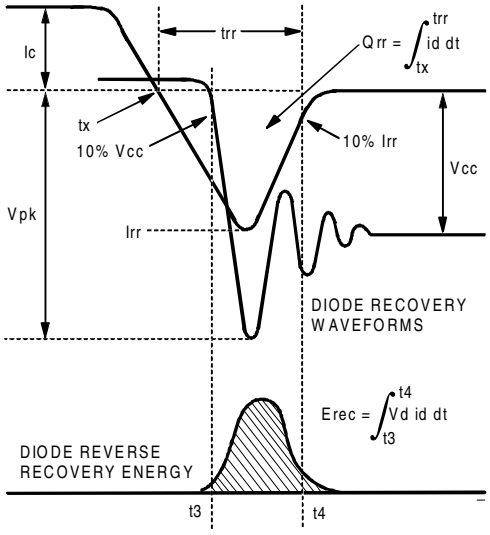


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

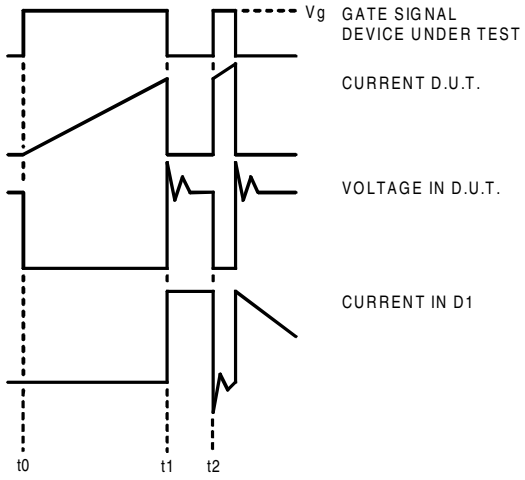


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

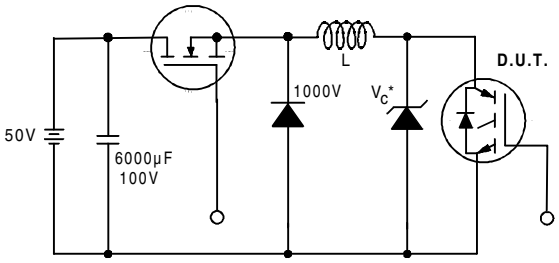


Figure 19. Clamped Inductive Load Test Circuit

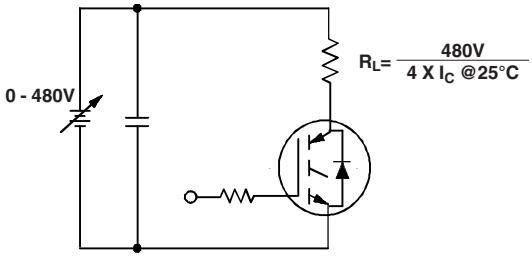


Figure 20. Pulsed Collector Current Test Circuit

Notes:

① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

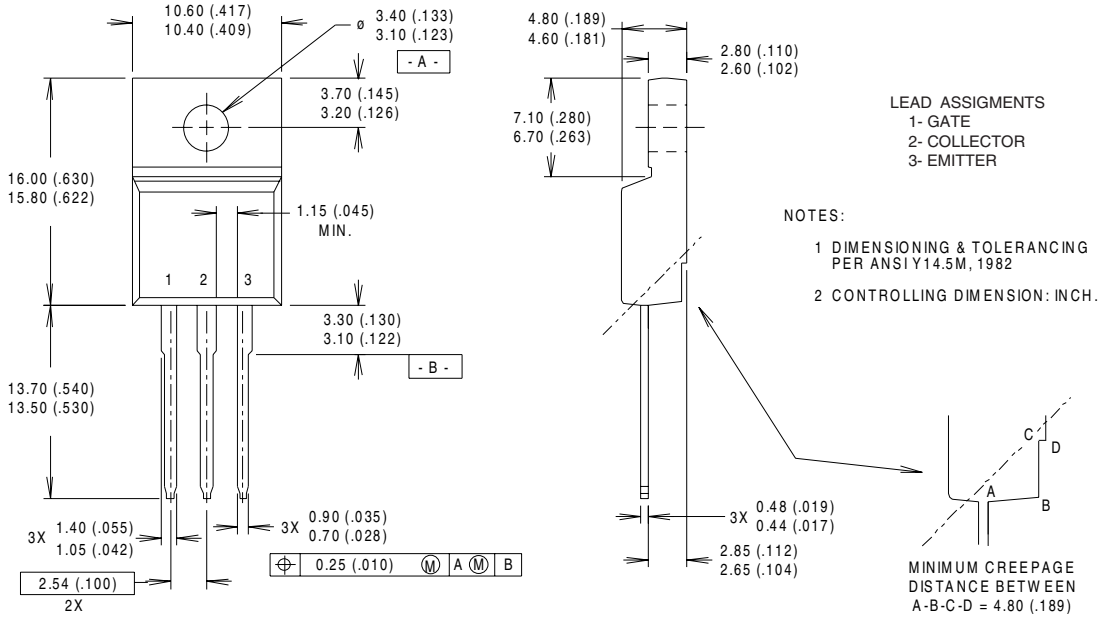
② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 23Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

⑤ t = 60s, f = 60Hz

Case Outline — TO-220 FULLPAK



International
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IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

Data and specifications subject to change without notice. 7/00

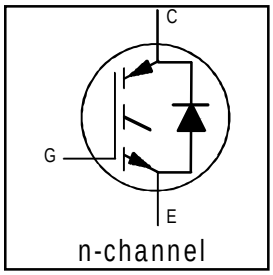
PD -94116

International
IOR Rectifier

IRG4BC20MD-S

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
Fast IGBT



n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.85V

@V_{GE} = 15V, I_C = 11A



D^{2}Pak

Features

- Rugged: 10µsec short circuit capable at V_{GS}=15V
- Low $V_{CE(on)}$ for 4 to 10kHz applications
- IGBT Co-packaged with ultra-soft-recovery antiparallel diode
- Industry standard D^{2}Pak package

Benefits

- Offers highest efficiency and short circuit capability for intermediate applications
- Provides best efficiency for the mid range frequency (4 to 10kHz)
- Optimized for Appliance Motor Drives, Industrial (Short Circuit Proof) Drives and Intermediate Frequency Range Drives
- High noise immune "Positive Only" gate drive- Negative bias gate drive not necessary
- For Low EMI designs- requires little or no snubbing
- Single Package switch for bridge circuit applications
- Compatible with high voltage Gate Driver IC's
- Allows simpler gate drive

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	18	A
I_C @ T_C = 100°C	Continuous Collector Current	11	
I_{CM}	Pulsed Collector Current ①	36	
I_{LM}	Clamped Inductive Load Current ②	36	
I_F @ T_C = 100°C	Diode Continuous Forward Current	7.0	
t_{sc}	Short Circuit Withstand Time	10	µs
I_{FM}	Diode Maximum Forward Current	36	A
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	------	------	2.1	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	------	------	2.5	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	------	0.50	------	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	-----	-----	80	
Wt	Weight	------	2 (0.07)	------	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	----	----	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	----	0.67	----	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	----	1.85	2.1	V	I_C = 11A V_{GE} = 15V
		----	2.46	----		I_C = 18A See Fig. 2, 5
		----	2.07	----		I_C = 11A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	4.0	----	6.5		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	----	-11	----	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	3.0	3.6	----	S	V_{CE} = 100V, I_C = 11A
I_{CES}	Zero Gate Voltage Collector Current	----	----	250	µA	V_{GE} = 0V, V_{CE} = 600V
		----	----	2500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	----	1.4	1.7	V	I_C = 8.0A See Fig. 13
		----	1.3	1.6		I_C = 8.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	----	----	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	----	39	59	nC	I_C = 11A
Qge	Gate - Emitter Charge (turn-on)	----	5.3	8.0		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	----	20	30		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	----	21	----	ns	T_J = 25°C
t_r	Rise Time	----	37	----		I_C = 11A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	463	690		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	----	340	510		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	----	0.41	----	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	----	2.03	----		See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	----	2.44	3.7		
$t_{d(on)}$	Turn-On Delay Time	----	19	----	ns	T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	----	41	----		I_C = 6.5A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	590	----		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	----	600	----		Energy losses include "tail" and
E_{ts}	Total Switching Loss	----	3.49	----	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	----	7.5	----	nH	Measured 5mm from package
C_{ies}	Input Capacitance	----	460	----	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	----	54	----		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	----	14	----		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	----	37	55	ns	T_J = 25°C See Fig.
		----	55	90		T_J = 125°C 14 I_F = 8.0A
I_{rr}	Diode Peak Reverse Recovery Current	----	3.5	5.0	A	T_J = 25°C See Fig.
		----	4.5	8.0		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	----	65	138	nC	T_J = 25°C See Fig.
		----	124	360		T_J = 125°C 16 di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	----	240	----	A/µs	T_J = 25°C See Fig.
	During t_b	----	210	----		T_J = 125°C 17

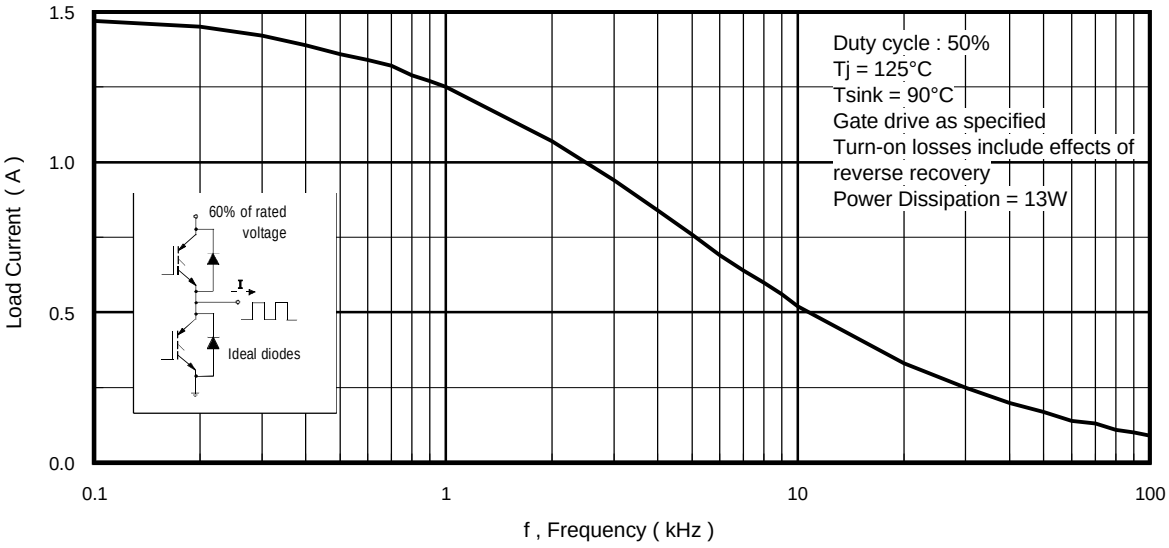


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

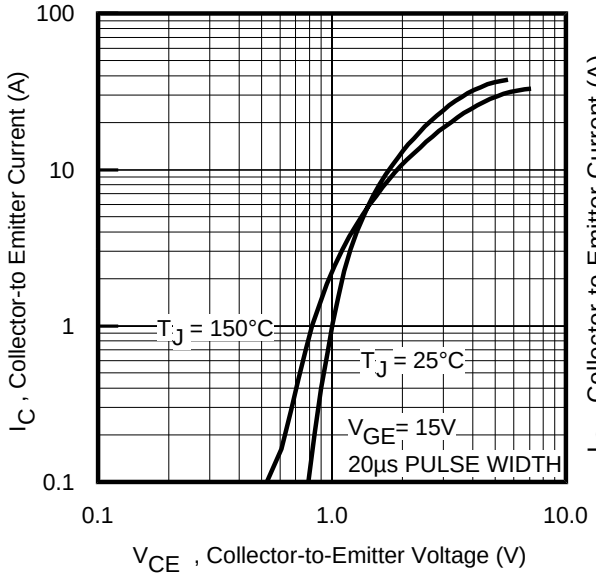


Fig. 2 - Typical Output Characteristics

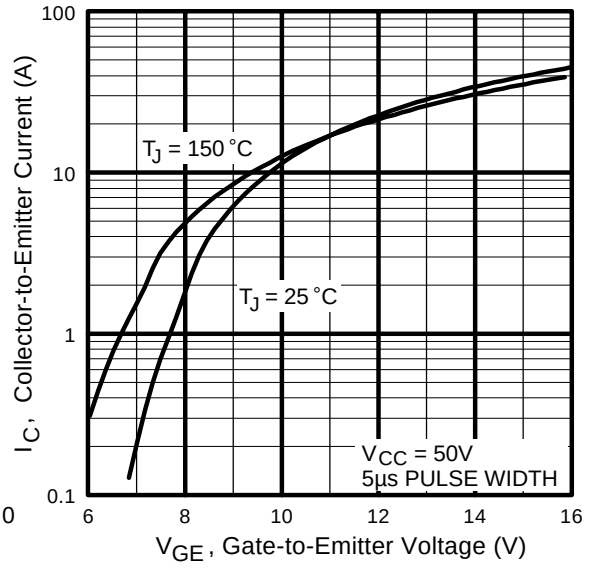


Fig. 3 - Typical Transfer Characteristics

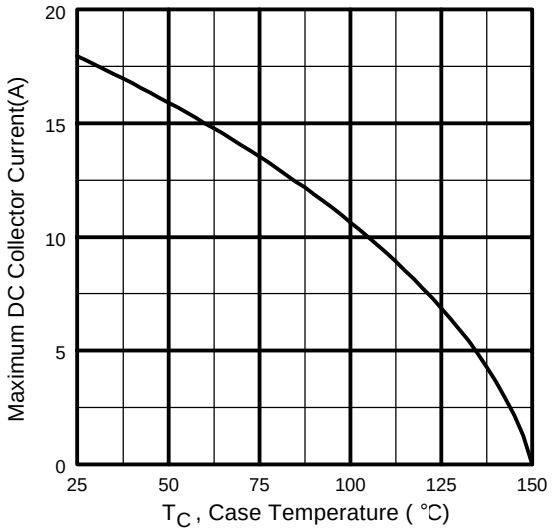


Fig. 4 - Maximum Collector Current vs. Case Temperature

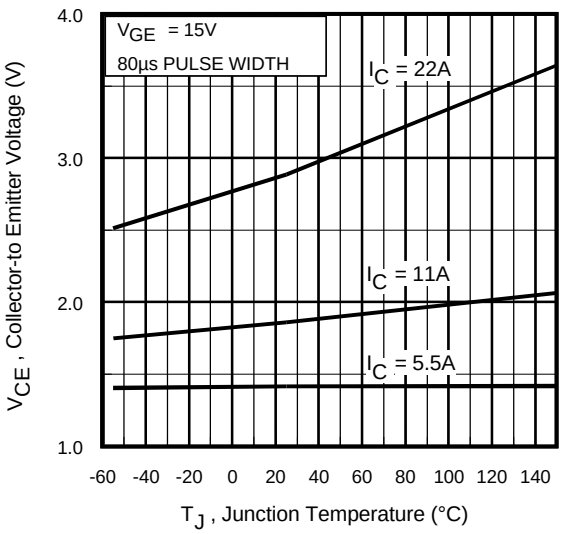


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

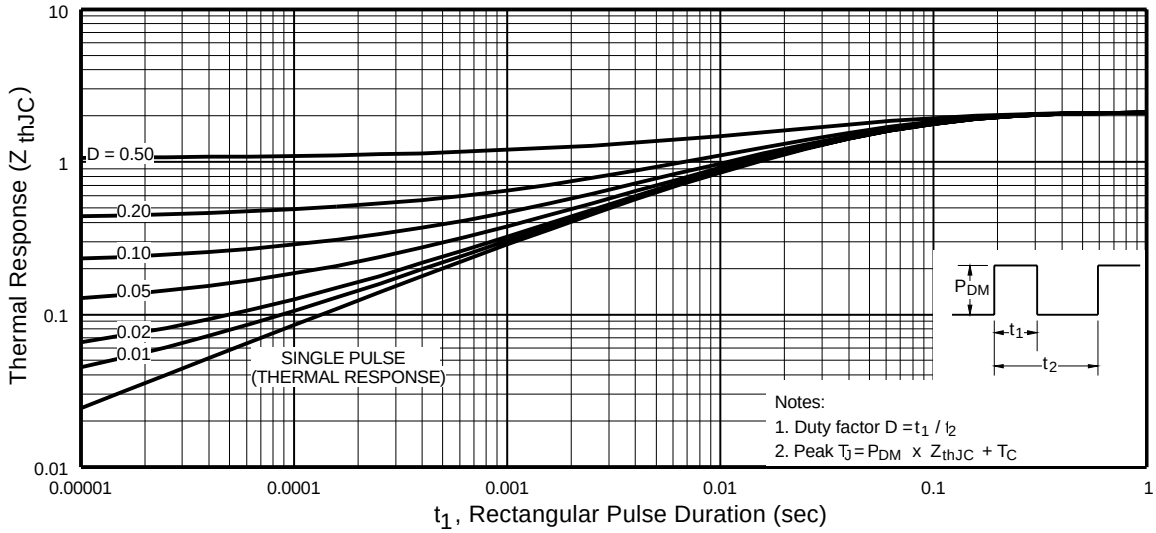


Fig. 6 - Maximum IGBT Effective Transient Thermal Impedance, Junction-to-Case

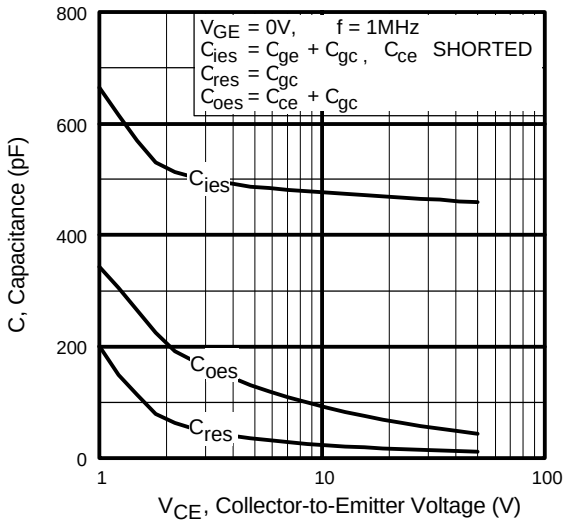


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

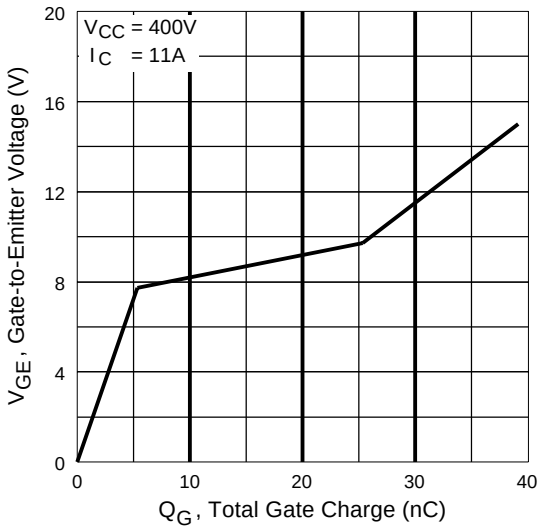


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

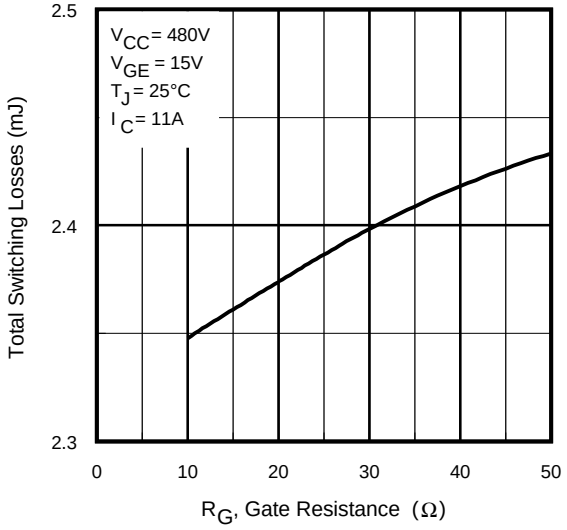


Fig. 9 - Typical Switching Losses vs. Gate Resistance

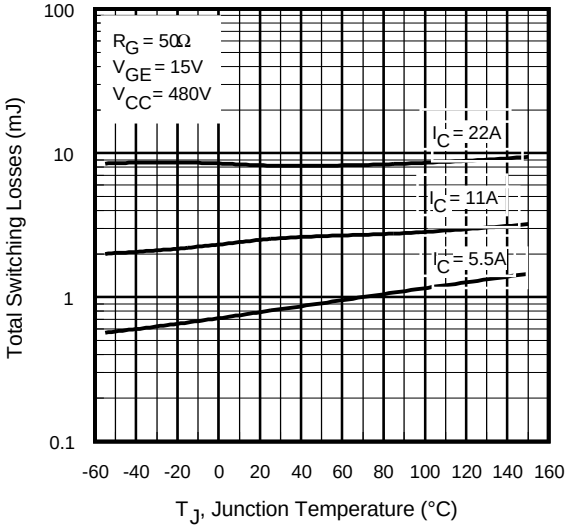


Fig. 10 - Typical Switching Losses vs. Junction Temperature

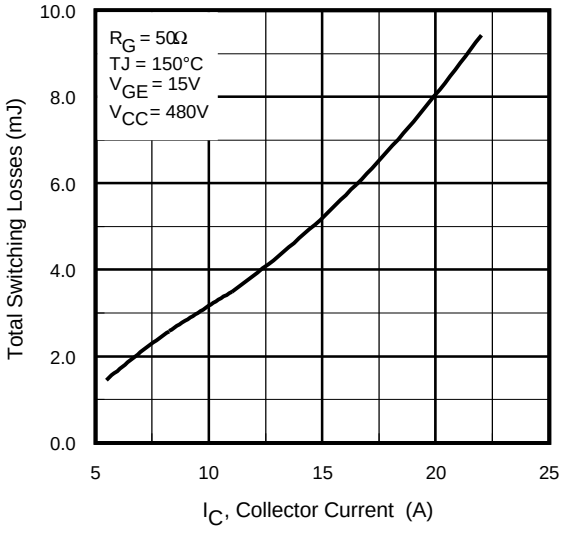


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

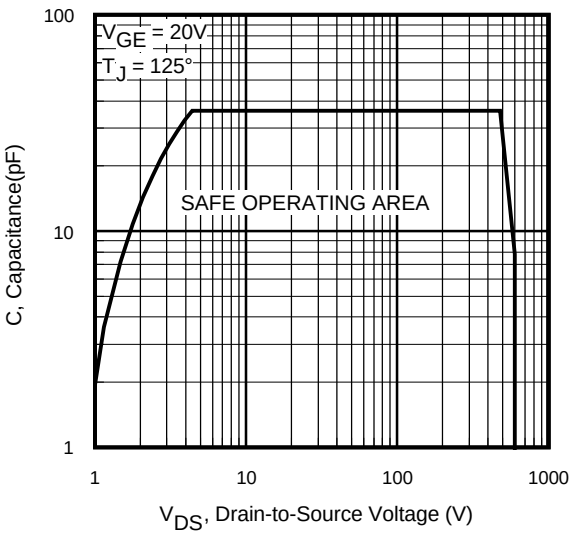


Fig. 12 - Turn-Off SOA

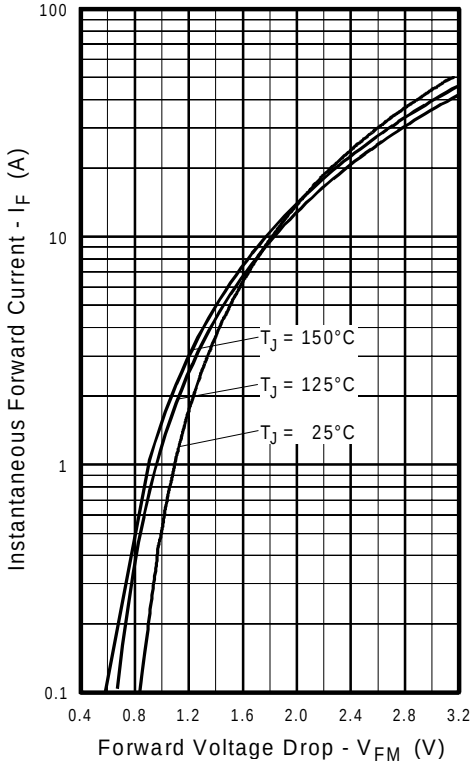


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

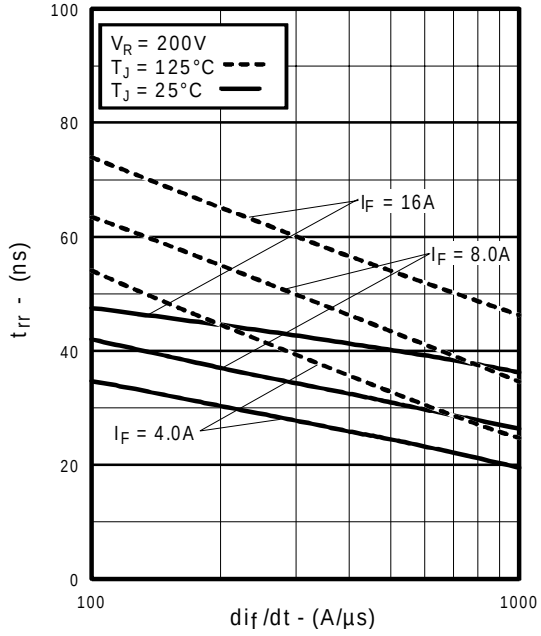


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

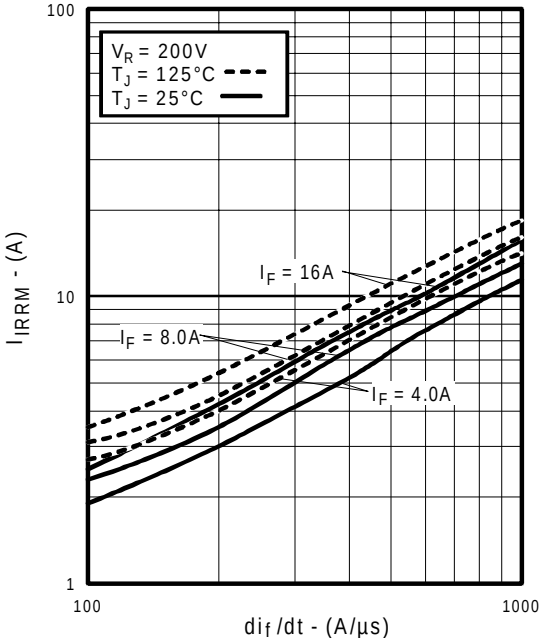


Fig. 15 - Typical Recovery Current vs. di_f/dt

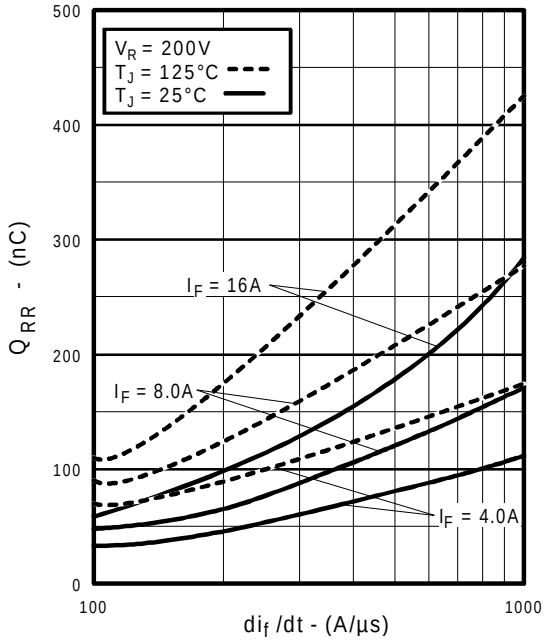


Fig. 16 - Typical Stored Charge vs. di_f/dt

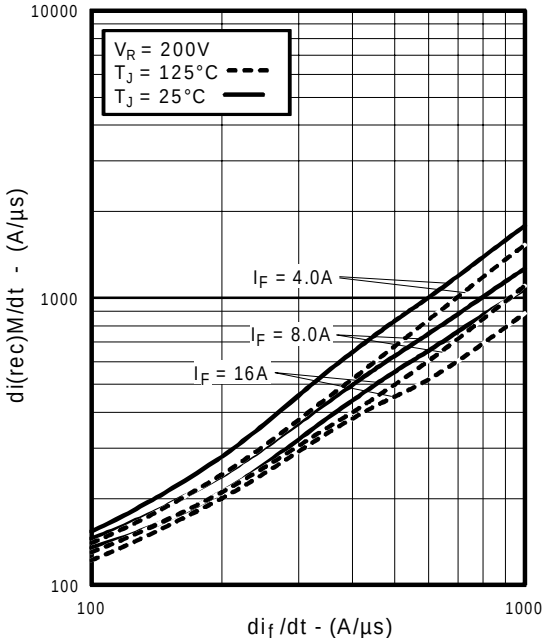


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

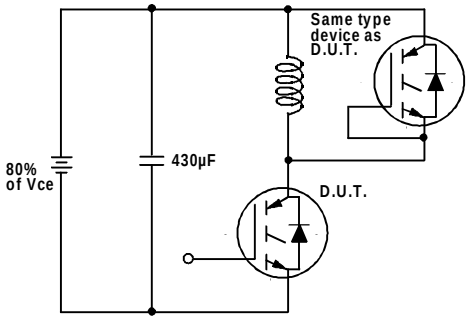


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

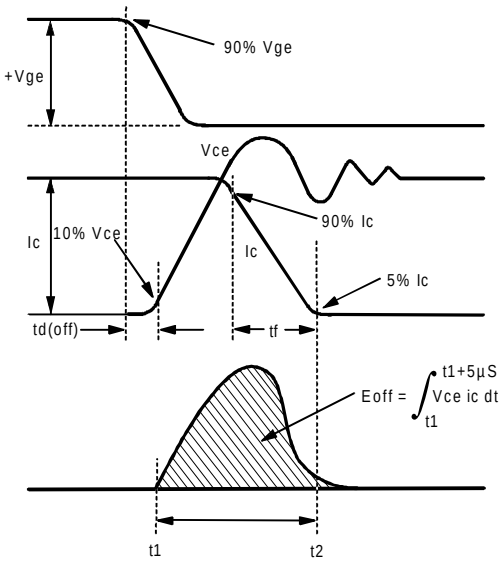


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

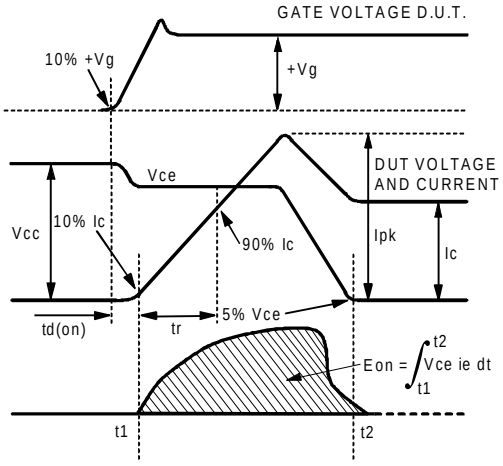


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

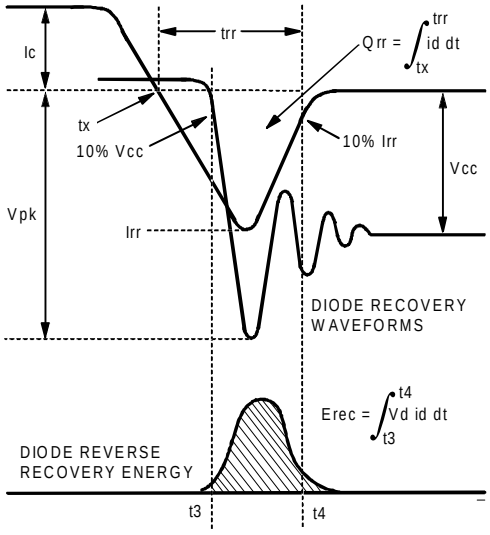


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

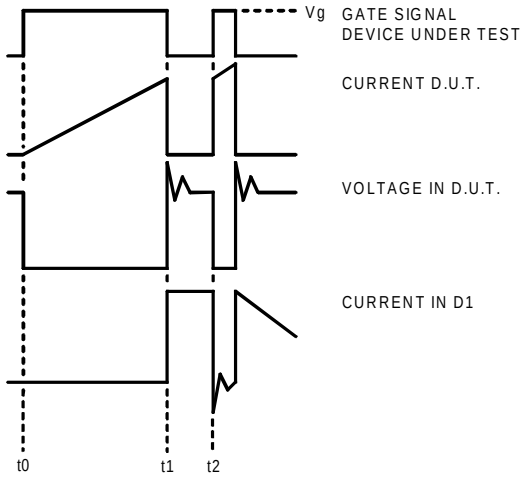


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

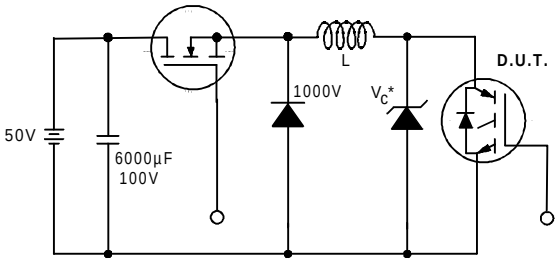


Figure 19. Clamped Inductive Load Test Circuit

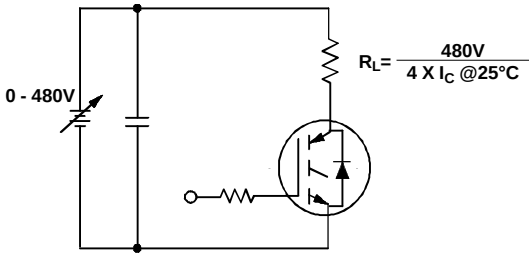
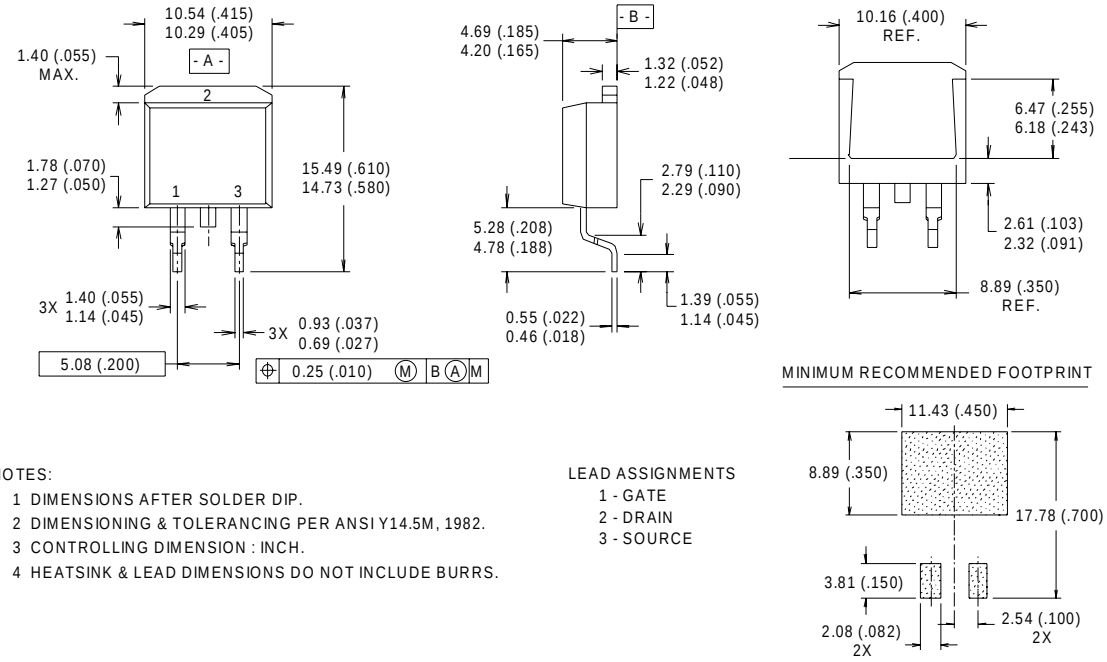


Figure 20. Pulsed Collector Current Test Circuit

D²Pak Package Outline



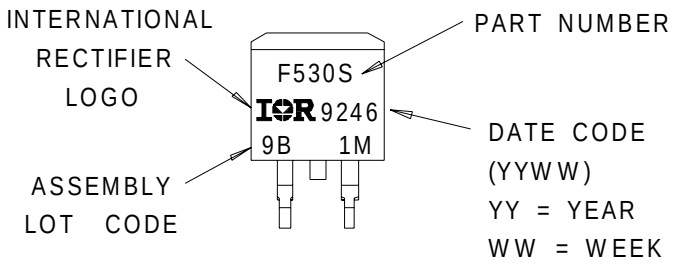
NOTES:

1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

1 - GATE
2 - DRAIN
3 - SOURCE

D²Pak Part Marking Information



Notes:

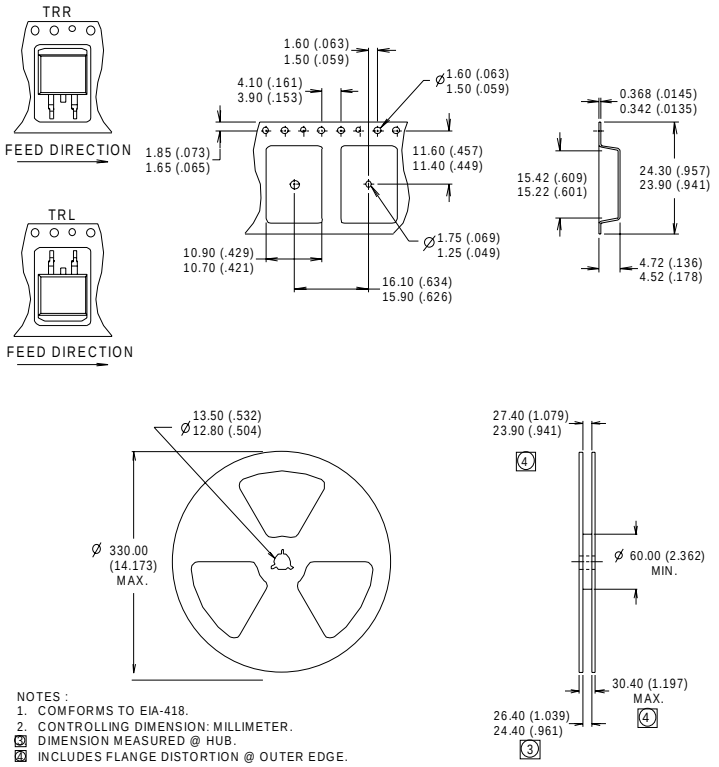
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 50Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

D²Pak Tape & Reel Information



Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information. 3/01

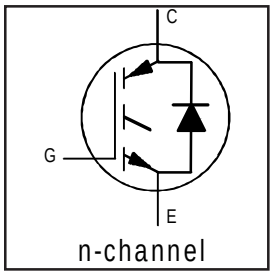
PD -94115

International
IOR Rectifier

IRG4BC20MD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
Fast IGBT

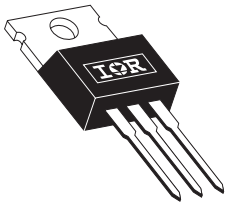


n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.85V

@V_{GE} = 15V, I_C = 11A



TO-220AB

Features

- Rugged: 10µsec short circuit capable at V_{GS}=15V
- Low $V_{CE(on)}$ for 4 to 10kHz applications
- IGBT Co-packaged with ultra-soft-recovery antiparallel diode
- Industry standard TO-220AB package

Benefits

- Offers highest efficiency and short circuit capability for intermediate applications
- Provides best efficiency for the mid range frequency (4 to 10kHz)
- Optimized for Appliance Motor Drives, Industrial (Short Circuit Proof) Drives and Intermediate Frequency Range Drives
- High noise immune "Positive Only" gate drive- Negative bias gate drive not necessary
- For Low EMI designs- requires little or no snubbing
- Single Package switch for bridge circuit applications
- Compatible with high voltage Gate Driver IC's
- Allows simpler gate drive

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	18	A
I_C @ T_C = 100°C	Continuous Collector Current	11	
I_{CM}	Pulsed Collector Current ①	36	
I_{LM}	Clamped Inductive Load Current ②	36	
I_F @ T_C = 100°C	Diode Continuous Forward Current	7.0	
t_{sc}	Short Circuit Withstand Time	10	µs
I_{FM}	Diode Maximum Forward Current	36	A
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	------	------	2.1	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	------	------	2.5	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	------	0.50	------	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	-----	-----	80	
Wt	Weight	------	2 (0.07)	------	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	600	----	----	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	----	0.67	----	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	----	1.85	2.1	V	I_C = 11A V_{GE} = 15V
		----	2.46	----		I_C = 18A See Fig. 2, 5
		----	2.07	----		I_C = 11A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	4.0	----	6.5		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	----	-11	----	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	3.0	3.6	----	S	V_{CE} = 100V, I_C = 11A
I_{CES}	Zero Gate Voltage Collector Current	----	----	250	µA	V_{GE} = 0V, V_{CE} = 600V
		----	----	2500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	----	1.4	1.7	V	I_C = 8.0A See Fig. 13
		----	1.3	1.6		I_C = 8.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	----	----	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	----	39	59	nC	I_C = 11A
Qge	Gate - Emitter Charge (turn-on)	----	5.3	8.0		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	----	20	30		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	----	21	----	ns	T_J = 25°C
t_r	Rise Time	----	37	----		I_C = 11A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	463	690		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	----	340	510		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	----	0.41	----	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	----	2.03	----		See Fig. 9, 10, 11, 18
E_{ts}	Total Switching Loss	----	2.44	3.7		
$t_{d(on)}$	Turn-On Delay Time	----	19	----	ns	T_J = 150°C, See Fig. 9, 10, 11, 18
t_r	Rise Time	----	41	----		I_C = 6.5A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	----	590	----		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	----	600	----		Energy losses include "tail" and
E_{ts}	Total Switching Loss	----	3.49	----	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	----	7.5	----	nH	Measured 5mm from package
C_{ies}	Input Capacitance	----	460	----	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	----	54	----		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	----	14	----		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	----	37	55	ns	T_J = 25°C See Fig.
		----	55	90		T_J = 125°C 14 I_F = 8.0A
I_{rr}	Diode Peak Reverse Recovery Current	----	3.5	5.0	A	T_J = 25°C See Fig.
		----	4.5	8.0		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	----	65	138	nC	T_J = 25°C See Fig.
		----	124	360		T_J = 125°C 16 di/dt 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	----	240	----	A/µs	T_J = 25°C See Fig.
	During t_b	----	210	----		T_J = 125°C 17

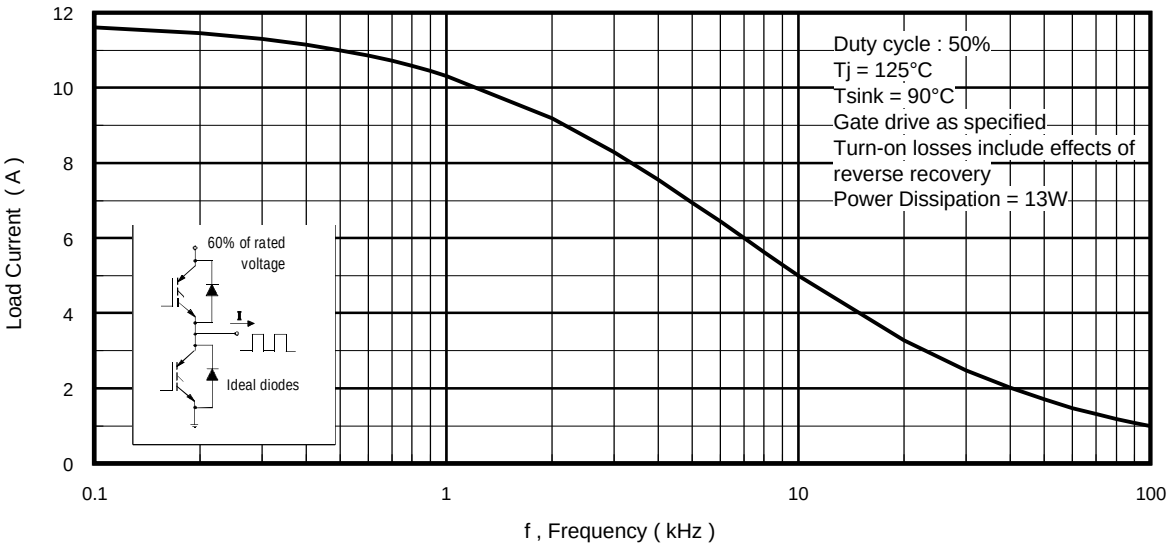


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

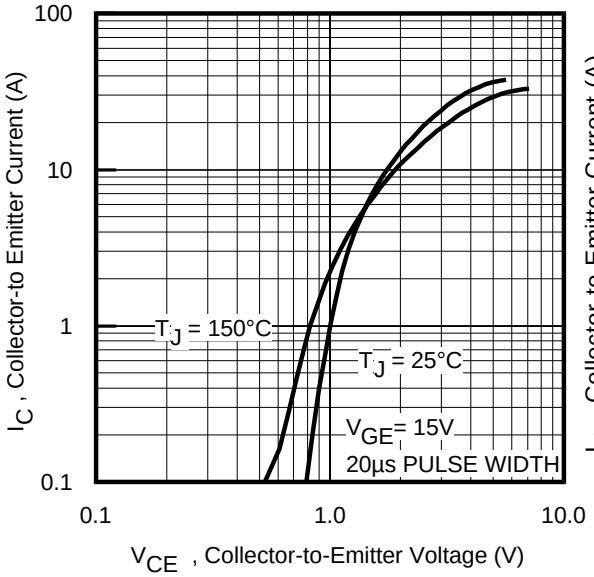


Fig. 2 - Typical Output Characteristics

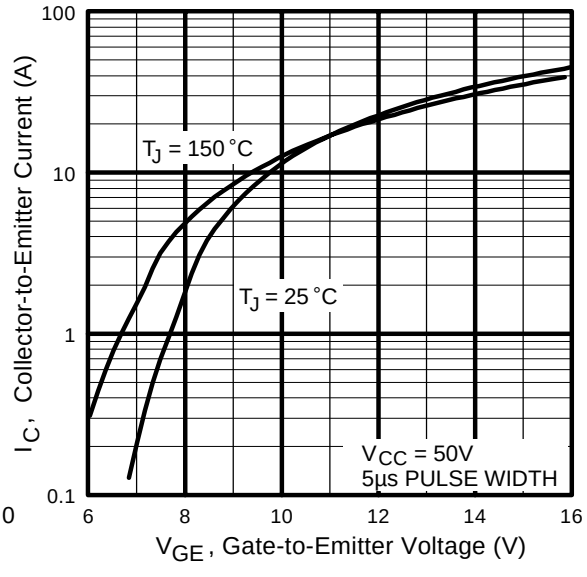


Fig. 3 - Typical Transfer Characteristics

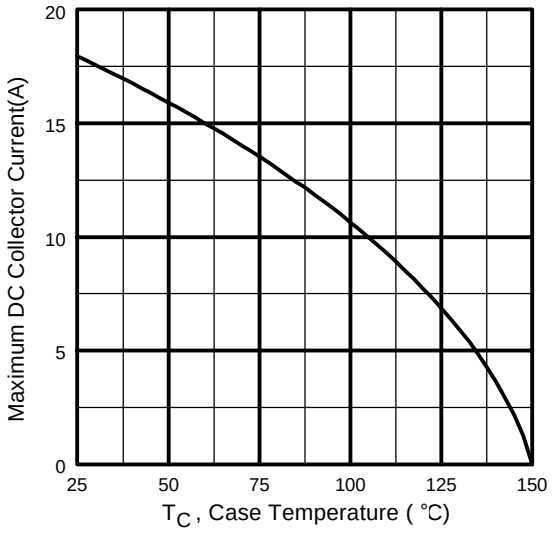


Fig. 4 - Maximum Collector Current vs. Case Temperature

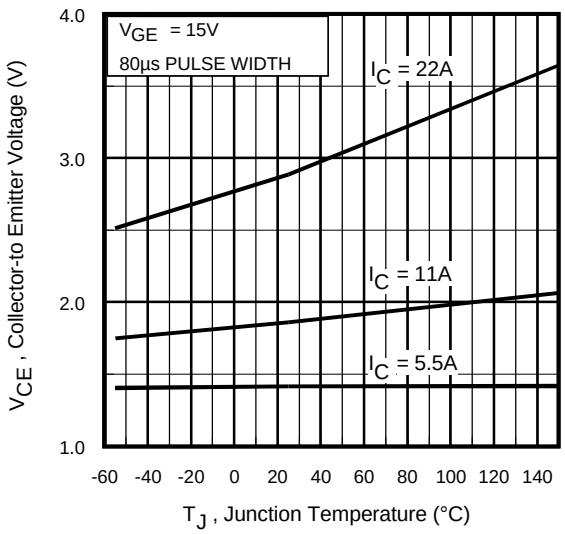


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

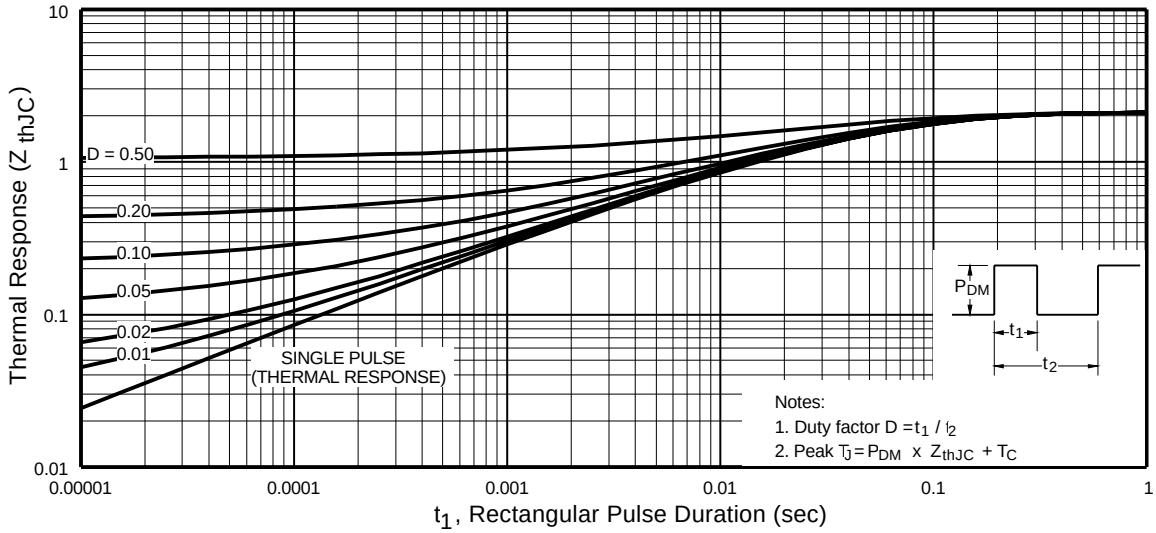


Fig. 6 - Maximum IGBT Effective Transient Thermal Impedance, Junction-to-Case

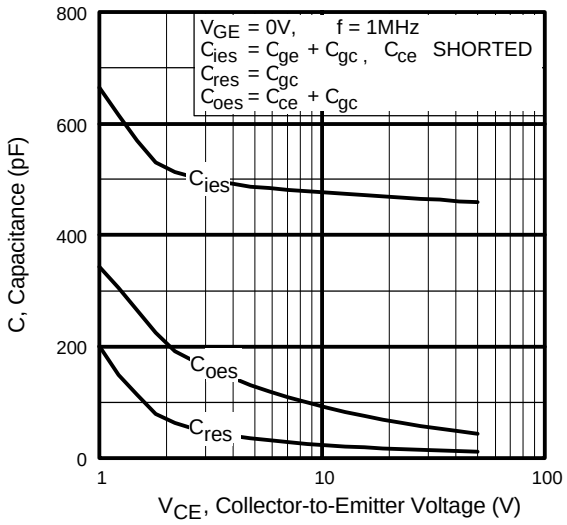


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

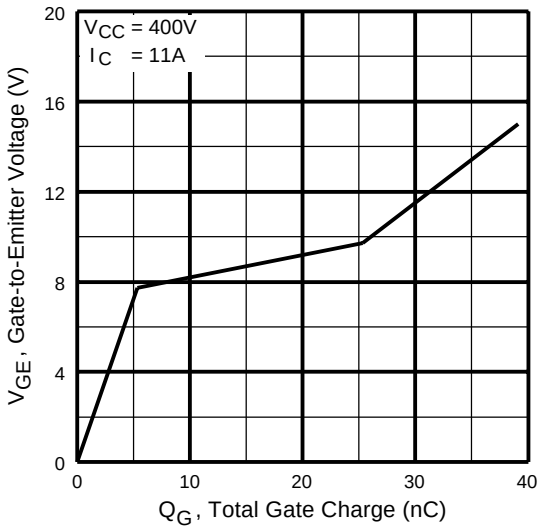


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

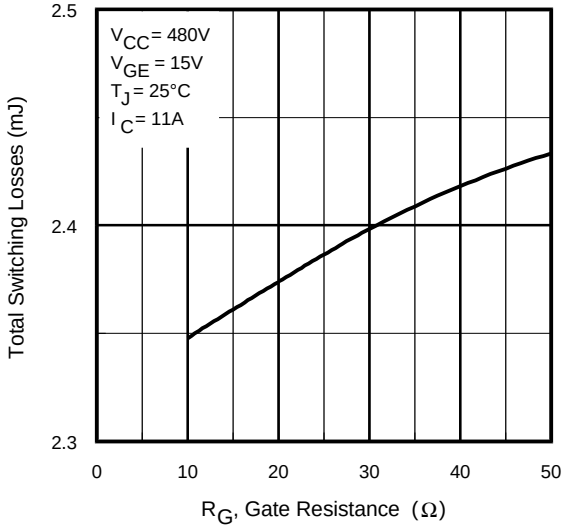


Fig. 9 - Typical Switching Losses vs. Gate Resistance

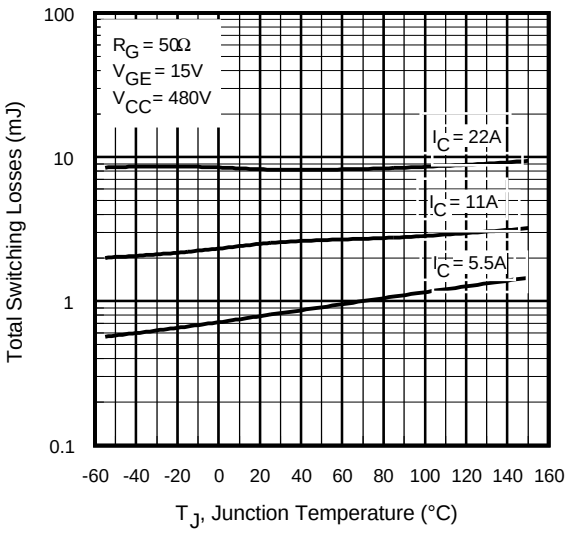


Fig. 10 - Typical Switching Losses vs. Junction Temperature

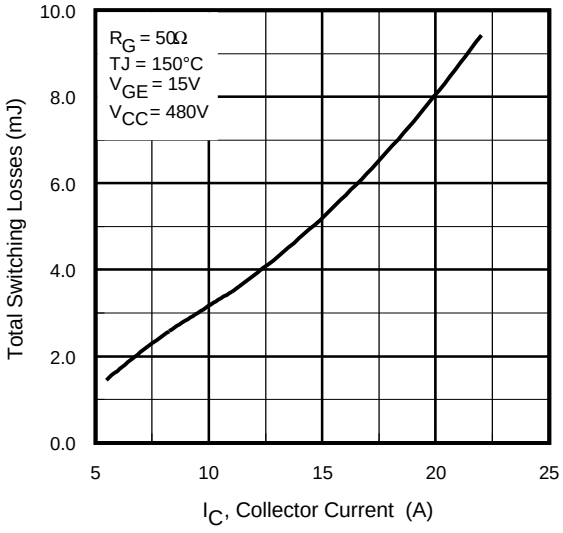


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

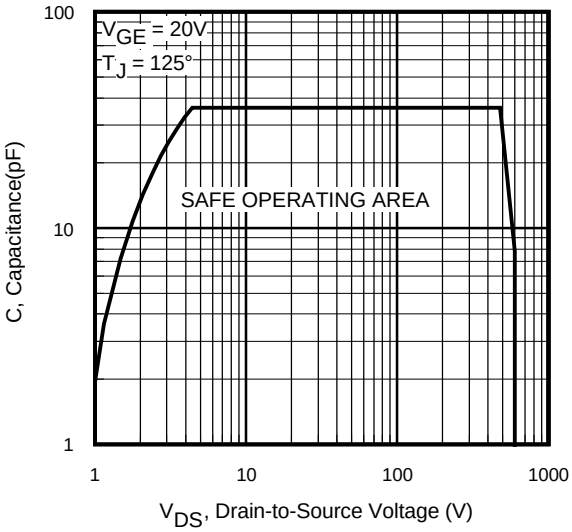


Fig. 12 - Turn-Off SOA

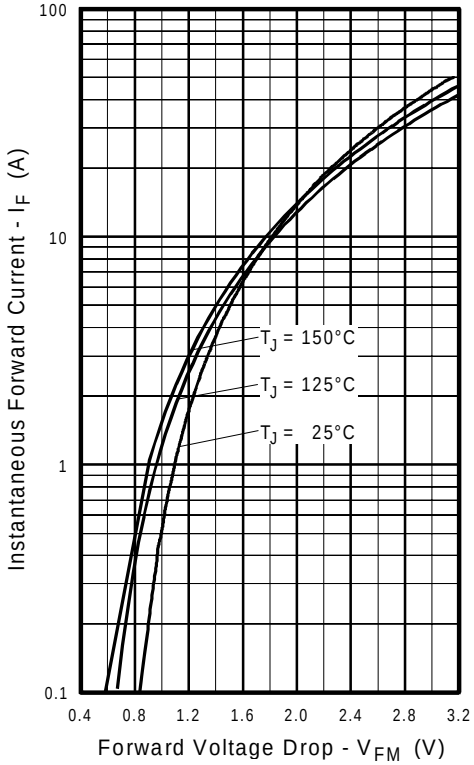


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

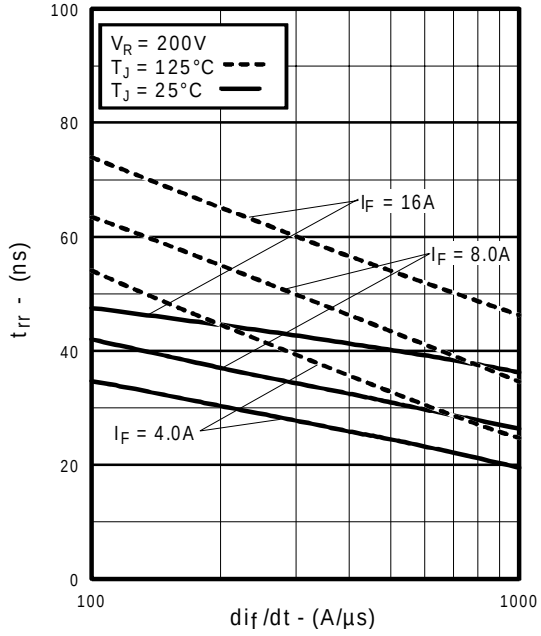


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

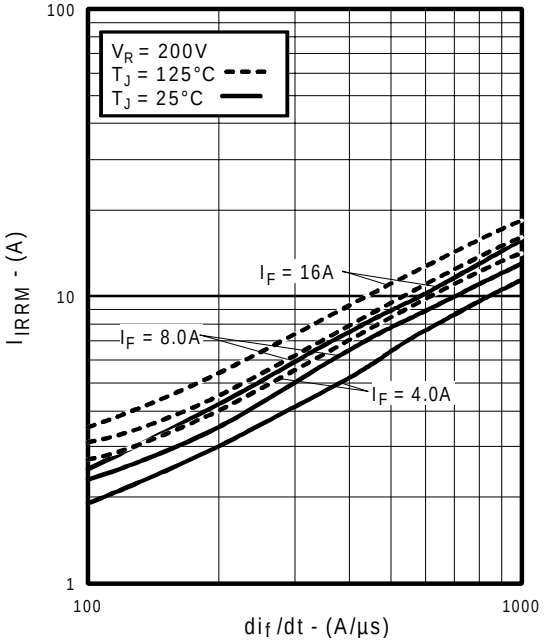


Fig. 15 - Typical Recovery Current vs. di_f/dt

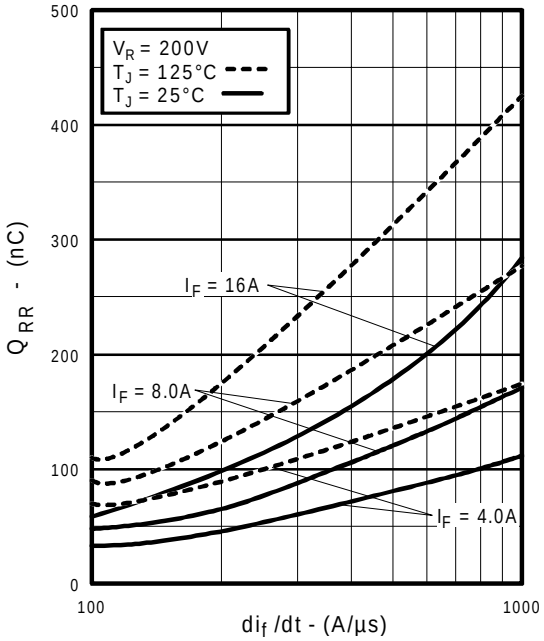


Fig. 16 - Typical Stored Charge vs. di_f/dt

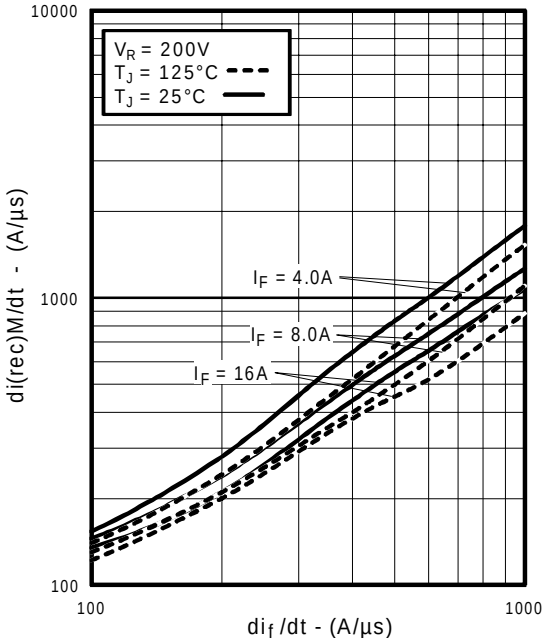


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

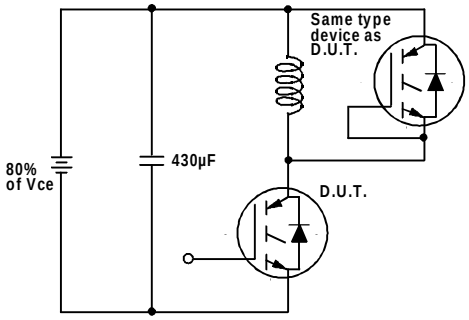


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

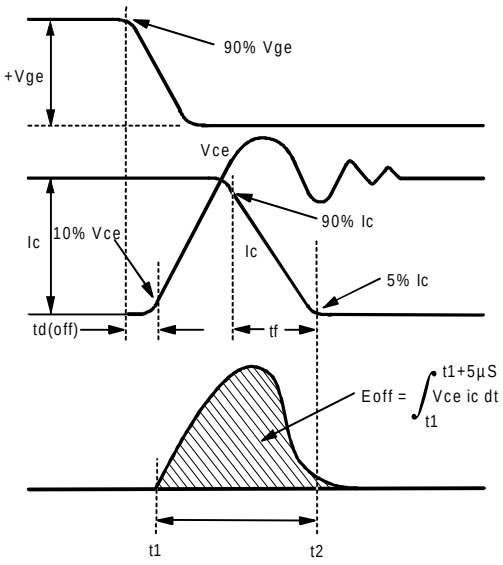


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

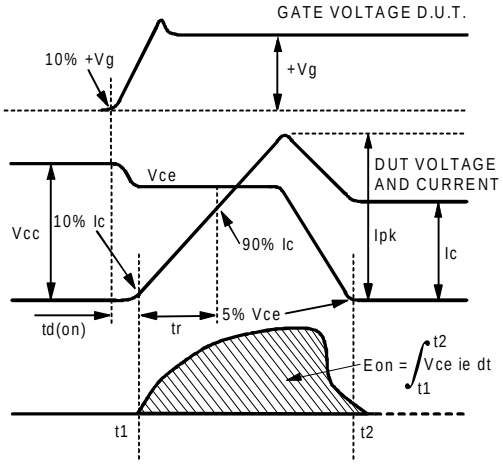


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

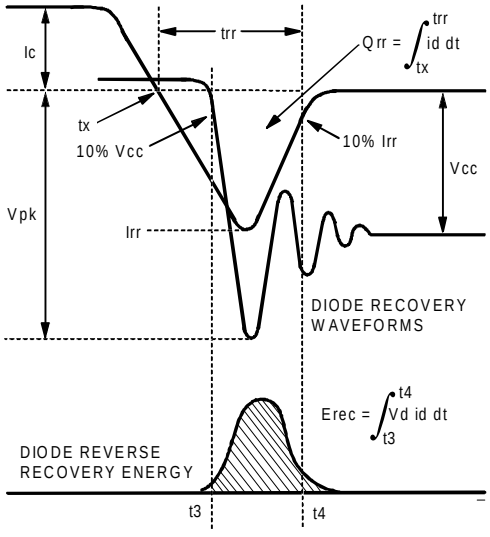


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

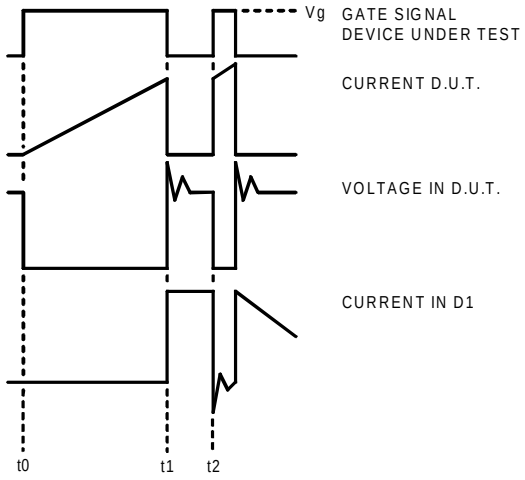


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

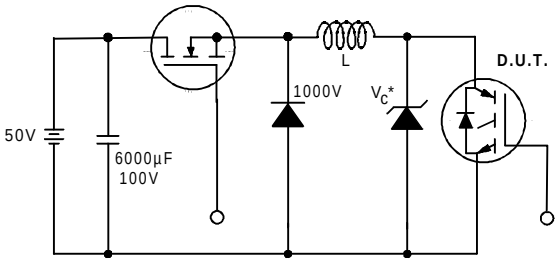


Figure 19. Clamped Inductive Load Test Circuit

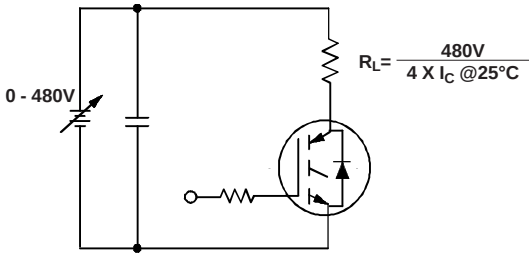


Figure 20. Pulsed Collector Current Test Circuit

Notes:

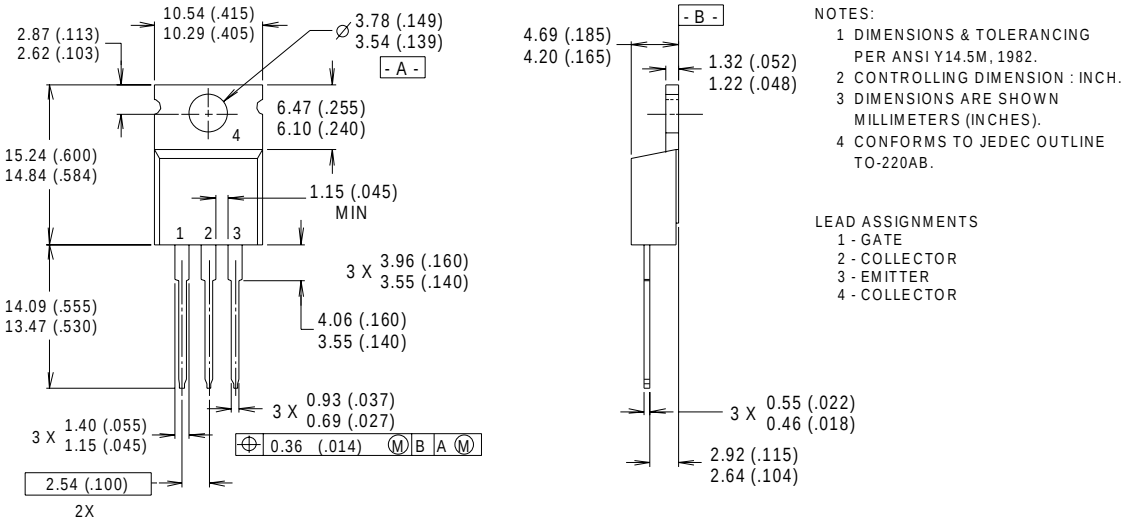
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 50Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information. 3/01

PD -91794

International
IOR Rectifier

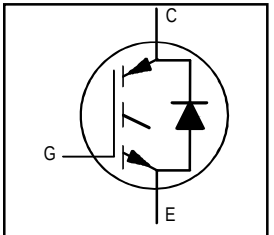
IRG4BC20SD-S

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Standard Speed IGBT

Features

- Extremely low voltage drop 1.4Vtyp. @ 10A
- S-Series: Minimizes power dissipation at up to 3 KHz PWM frequency in inverter drives, up to 4 KHz in brushless DC drives.
- Very Tight Vce(on) distribution
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard D²Pak package



n-channel

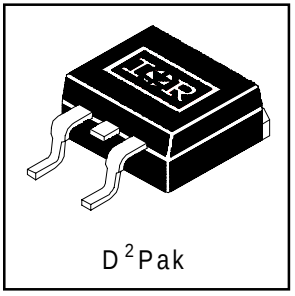
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.4V

@V_{GE} = 15V, I_C = 10A

Benefits

- Generation 4 IGBT's offer highest efficiencies available
- IGBT's optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBT's . Minimized recovery characteristics require less/no snubbing
- Lower losses than MOSFET's conduction and Diode losses


D²Pak

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	19	A
I_C @ T_C = 100°C	Continuous Collector Current	10	
I_{CM}	Pulsed Collector Current ①	38	
I_{LM}	Clamped Inductive Load Current ②	38	
I_F @ T_C = 100°C	Diode Continuous Forward Current	7.0	
I_{FM}	Diode Maximum Forward Current	38	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
R_{qJC}	Junction-to-Case - IGBT	——	2.1	°C/W
R_{qJC}	Junction-to-Case - Diode	——	3.5	
R_{qJA}	Junction-to-Ambient (PCB Mounted,steady-state)*	——	80	
Wt	Weight	1.44	——	g (oz)

* When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage*f*	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.75	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.40	1.6	V	I_C = 10A V_{GE} = 15V
		—	1.85	—		I_C = 19A See Fig. 2, 5
		—	1.44	—		I_C = 10A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	2.0	5.8	—	S	V_{CE} = 100V, I_C = 10A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1700		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 8.0A See Fig. 13
		—	1.3	1.6		I_C = 8.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	27	40	nC	I_C = 10A
Qge	Gate - Emitter Charge (turn-on)	—	4.3	6.5		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	10	15		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	62	—	ns	T_J = 25°C
t_r	Rise Time	—	32	—		I_C = 10A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	690	1040		V_{GE} = 15V, R_G = 50W
t_f	Fall Time	—	480	730		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	0.32	—	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	2.58	—		See Fig. 9, 10, 11,18
E_{ts}	Total Switching Loss	—	2.90	4.5		
$t_{d(on)}$	Turn-On Delay Time	—	64	—	ns	T_J = 150°C, See Fig. 10,11, 18
t_r	Rise Time	—	35	—		I_C = 10A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	980	—		V_{GE} = 15V, R_G = 50W
t_f	Fall Time	—	800	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	4.33	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	550	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	39	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	7.1	—		*f* = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	37	55	ns	T_J = 25°C See Fig.
		—	55	90		T_J = 125°C 14 I_F = 8.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	5.0	A	T_J = 25°C See Fig.
		—	4.5	8.0		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	65	138	nC	T_J = 25°C See Fig.
		—	124	360		T_J = 125°C 16 di/dt = 200Aµs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	240	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	210	—		T_J = 125°C 17

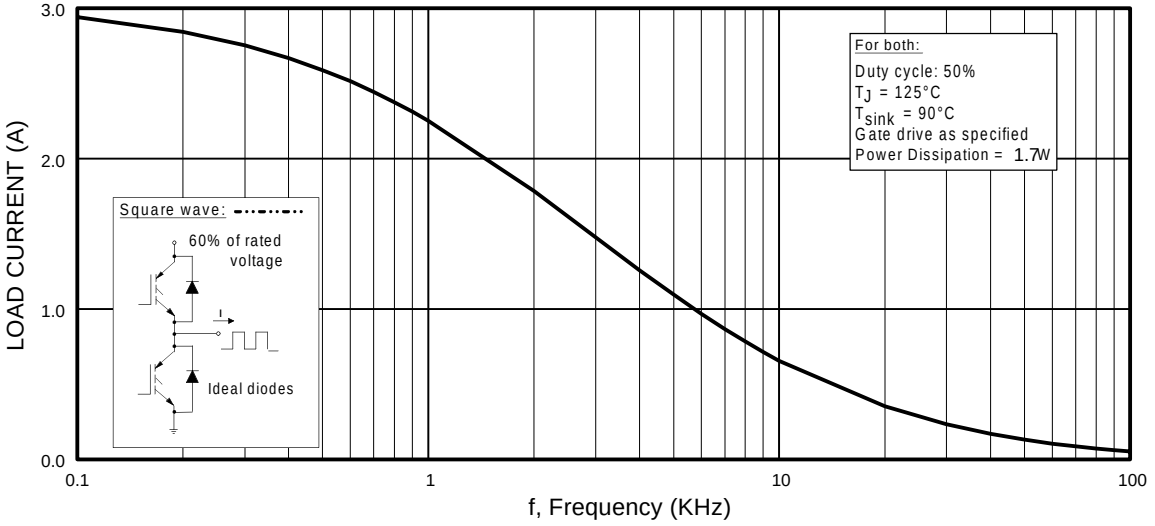


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

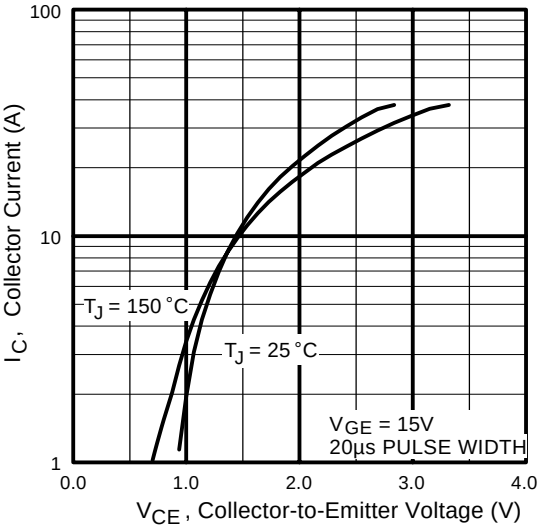


Fig. 2 - Typical Output Characteristics

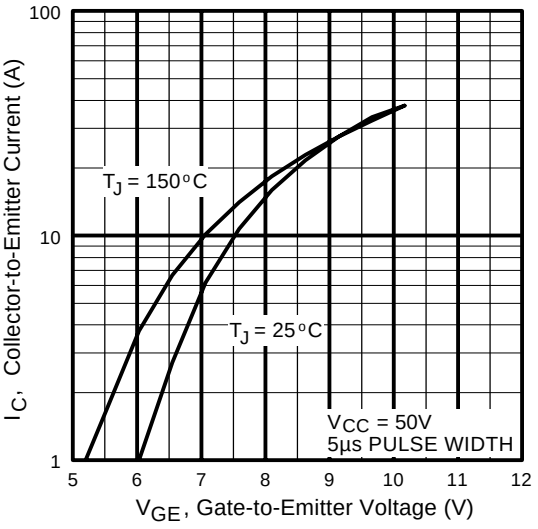


Fig. 3 - Typical Transfer Characteristics

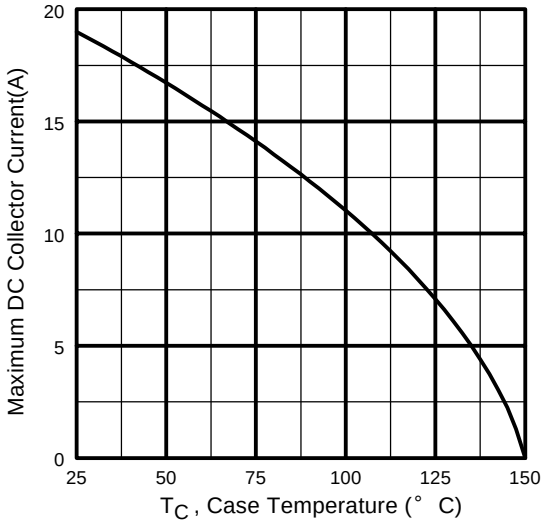


Fig. 4 - Maximum Collector Current vs. Case Temperature

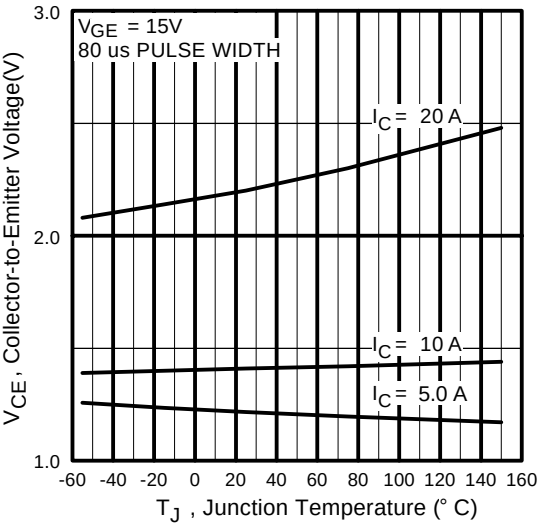


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

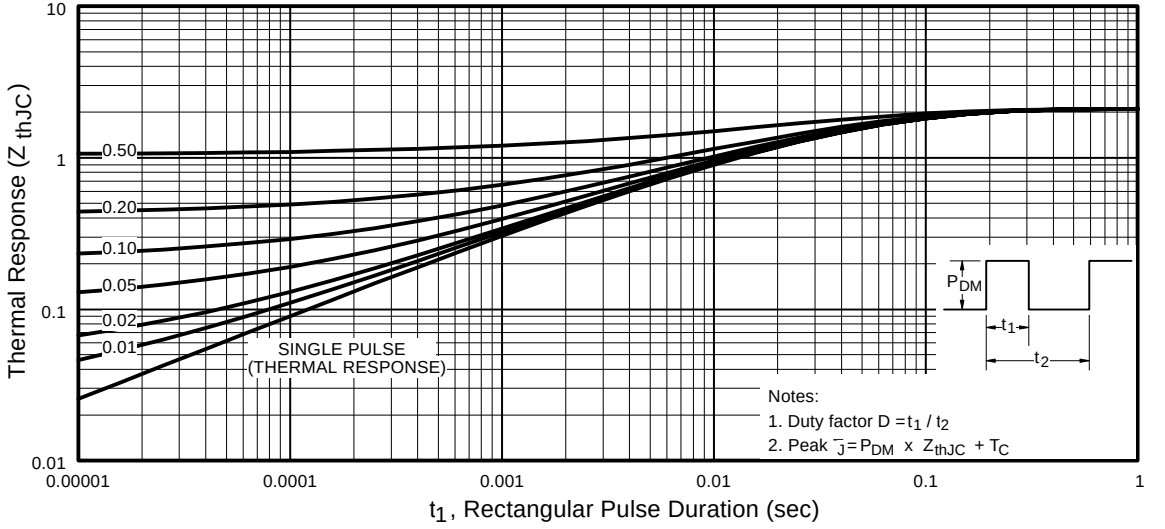


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

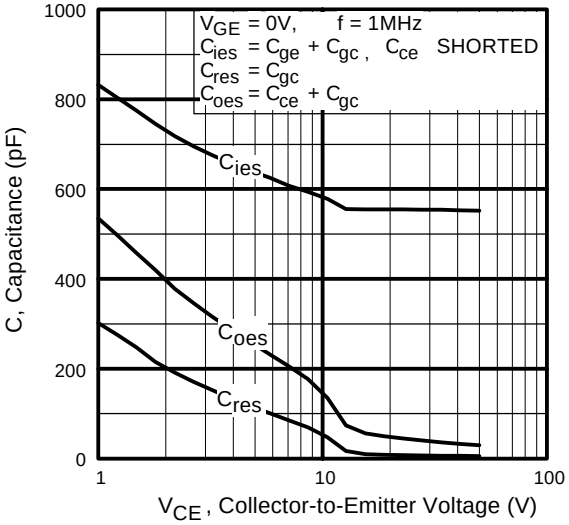


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

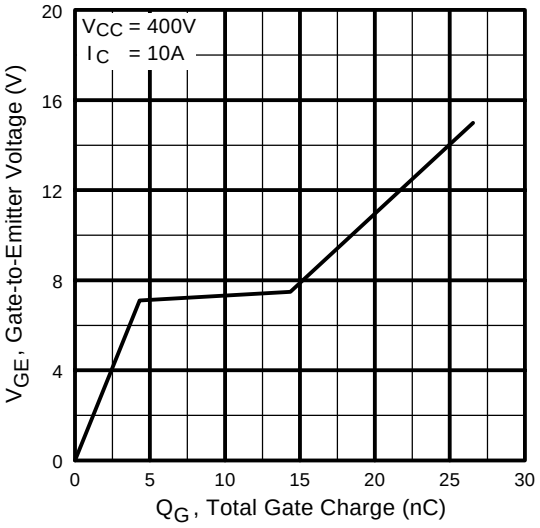


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

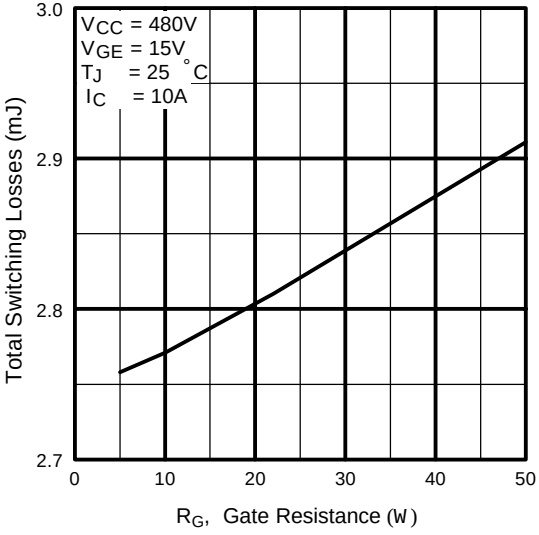


Fig. 9 - Typical Switching Losses vs. Gate Resistance

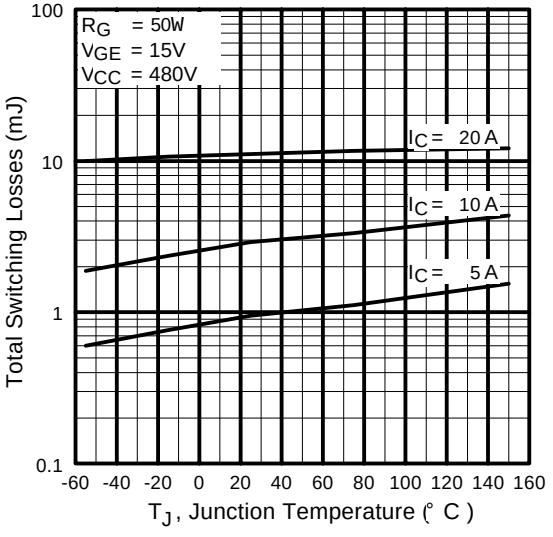


Fig. 10 - Typical Switching Losses vs. Junction Temperature

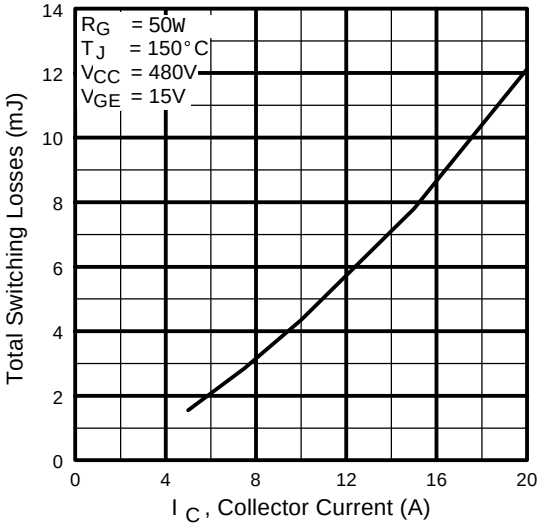


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

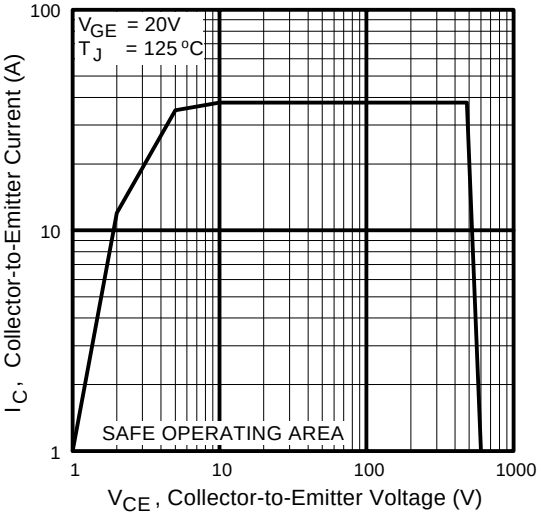


Fig. 12 - Turn-Off SOA

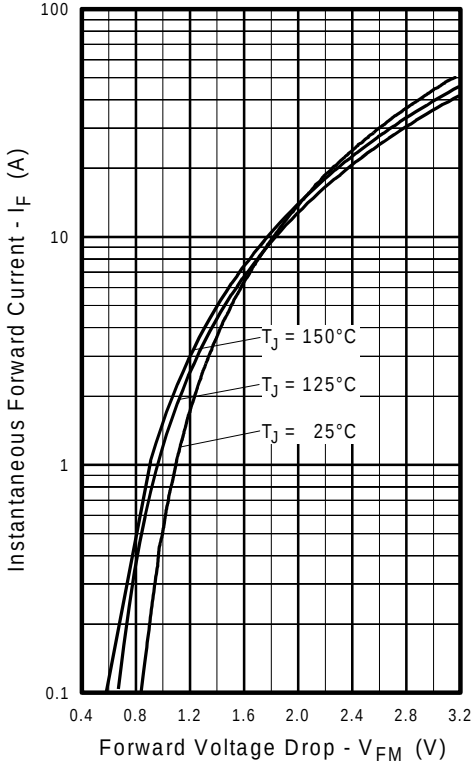


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

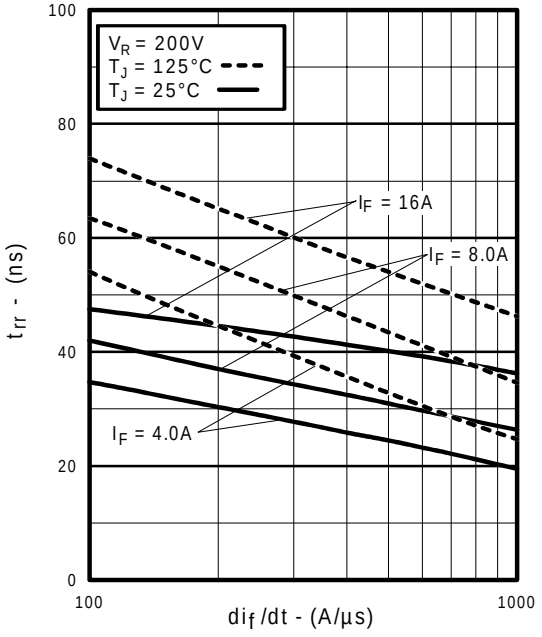


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

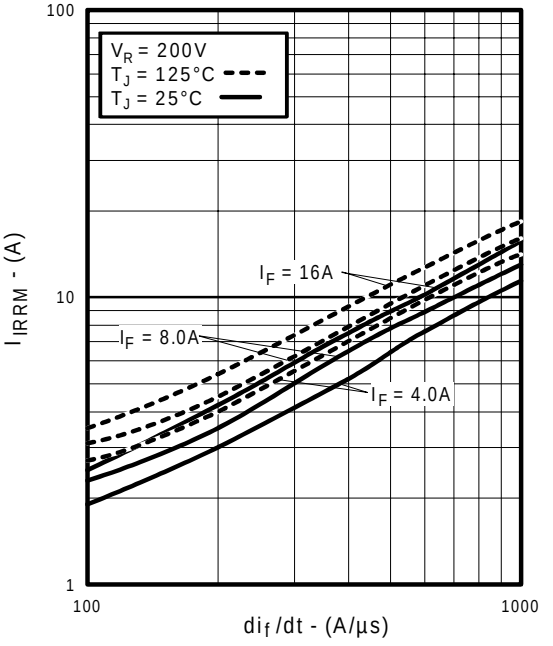


Fig. 15 - Typical Recovery Current vs. di_f/dt

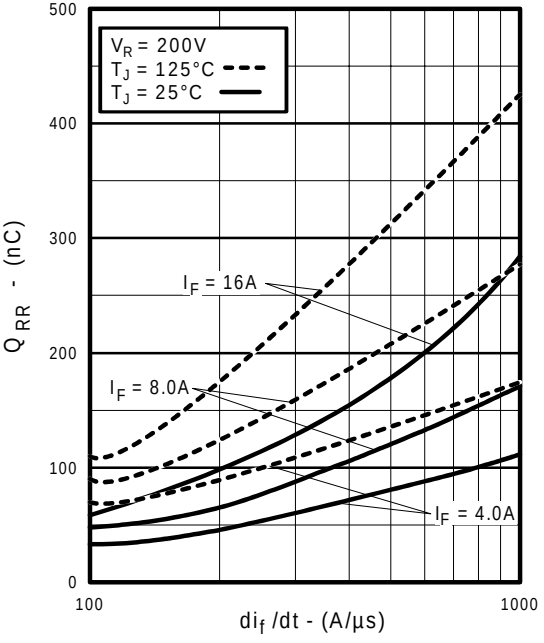


Fig. 16 - Typical Stored Charge vs. di_f/dt

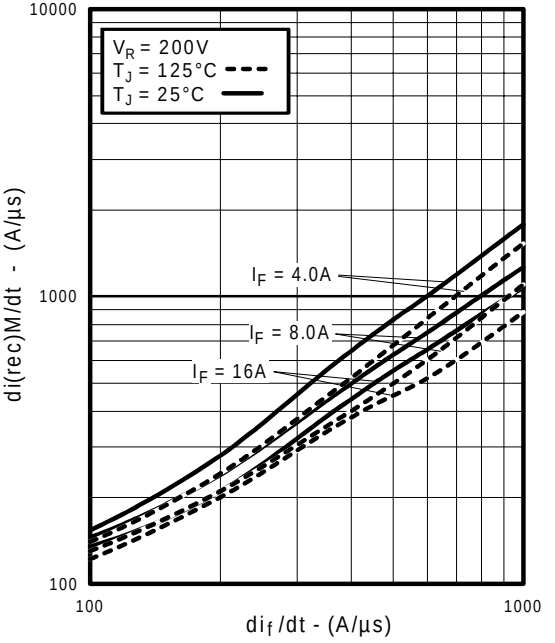


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

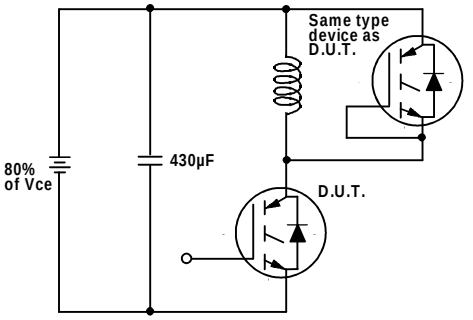


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

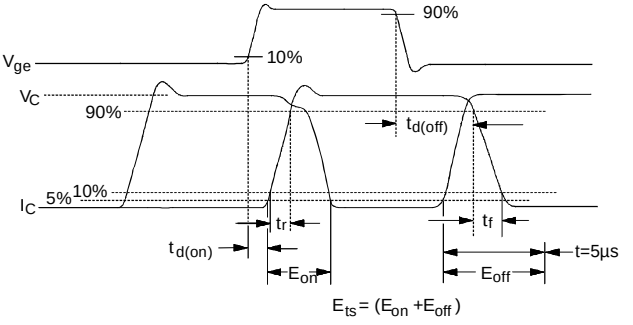


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

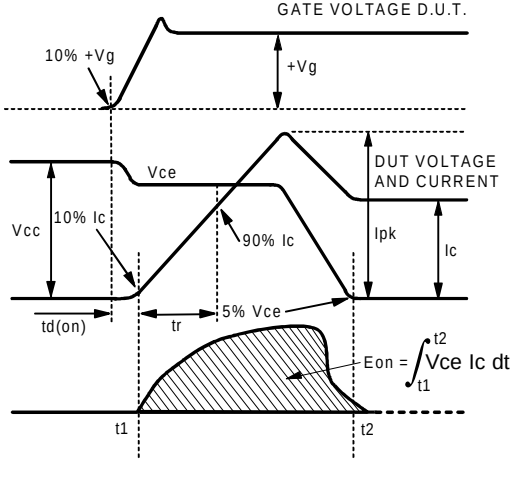


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

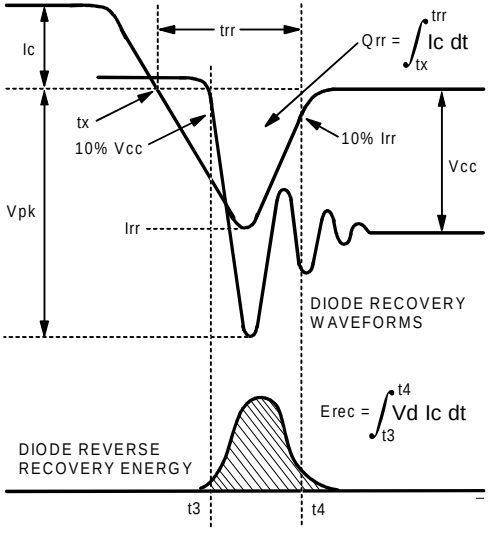


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

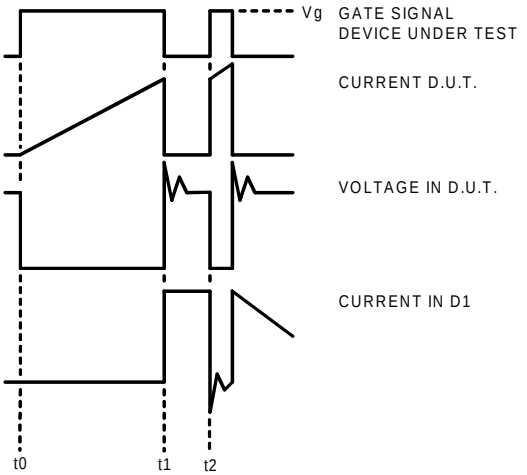


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

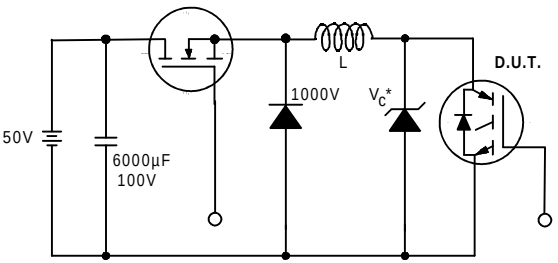


Figure 19. Clamped Inductive Load Test Circuit

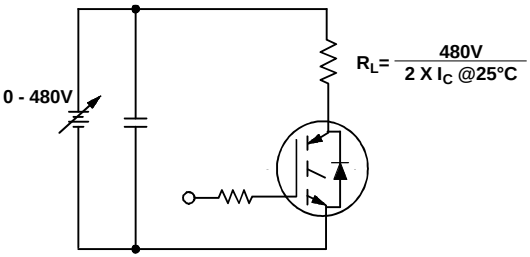


Figure 20. Pulsed Collector Current Test Circuit

Notes:

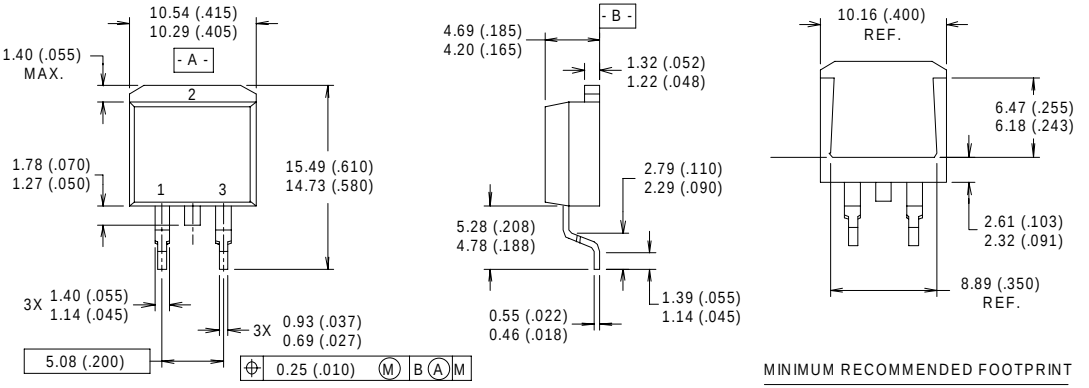
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 50W (figure 19)

③ Pulse width £ 80µs; duty factor £ 0.1%.

④ Pulse width 5.0µs, single shot.

D²Pak Package Outline



NOTES:

1 DIMENSIONS AFTER SOLDER DIP.

2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.

3 CONTROLLING DIMENSION : INCH.

4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

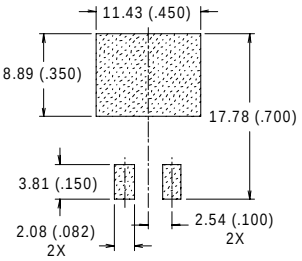
LEAD ASSIGNMENTS

1 - GATE

2 - DRAIN

3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT



International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936
http://www.irf.com/ Data and specifications subject to change without notice. 9/98

PD - 91597A

International
IOR Rectifier

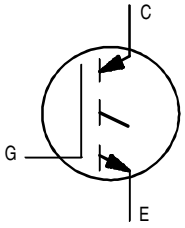
IRG4BC20S

INSULATED GATE BIPOLAR TRANSISTOR

Standard Speed IGBT

Features

- Standard: optimized for minimum saturation voltage and low operating frequencies (< 1kHz)
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-220AB package



n-channel

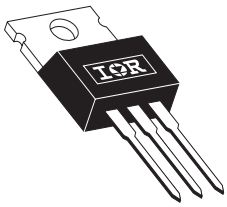
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.4V

@V_{GE} = 15V, I_C = 10A

Benefits

- Generation 4 IGBTs offer highest efficiency available
- IGBTs optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	19	A
I_C @ T_C = 100°C	Continuous Collector Current	10	
I_{CM}	Pulsed Collector Current ①	38	
I_{LM}	Clamped Inductive Load Current ②	38	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	5.0	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	80	
Wt	Weight	2.0 (0.07)	—	g (oz)

4/17/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.75	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.40	1.6	V	I_C = 10A V_{GE} = 15V
		—	1.85	—		I_C = 19A See Fig.2, 5
		—	1.44	—		I_C = 10A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	2.0	5.8	—	S	V_{CE} = 100V, I_C = 10A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	27	40	nC	I_C = 10A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	4.3	6.5		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	10	15		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	27	—	ns	
t_r	Rise Time	—	9.7	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	540	810		I_C = 10A, V_{CC} = 480V
t_f	Fall Time	—	430	640		V_{GE} = 15V, R_G = 50Ω
E_{on}	Turn-On Switching Loss	—	0.12	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	2.05	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	2.17	3.2		
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	T_J = 150°C,
t_r	Rise Time	—	13	—		I_C = 10A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	760	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	780	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	3.46	—	mJ	See Fig. 11, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	550	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	39	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	7.1	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 50Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

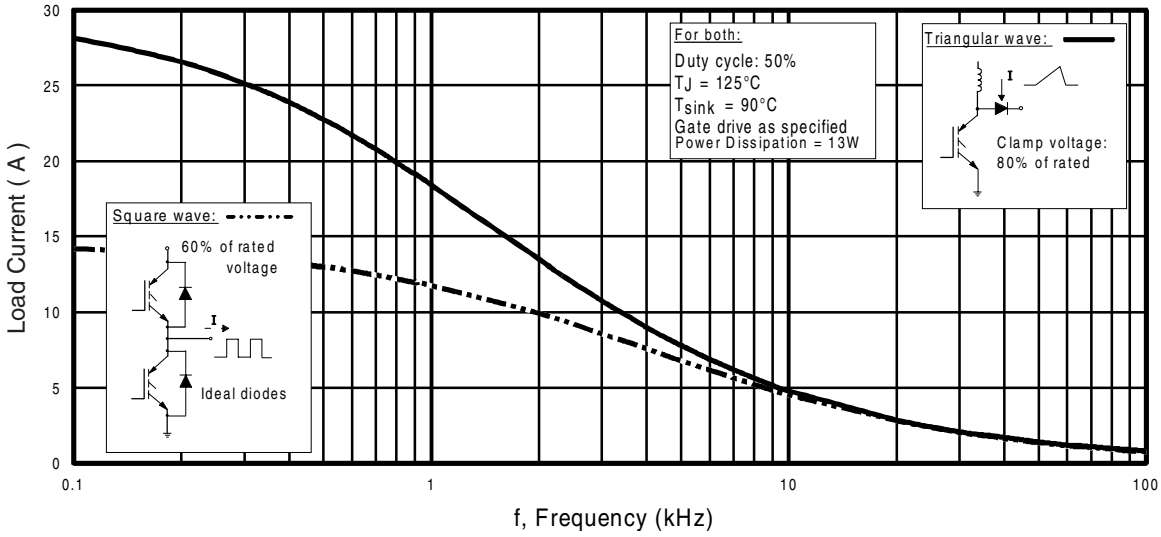


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

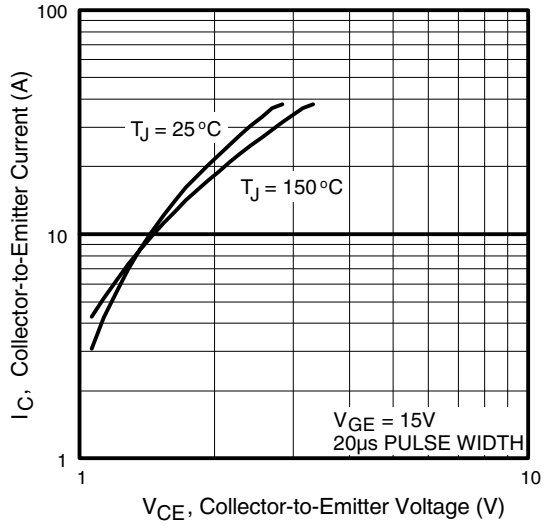


Fig. 2 - Typical Output Characteristics

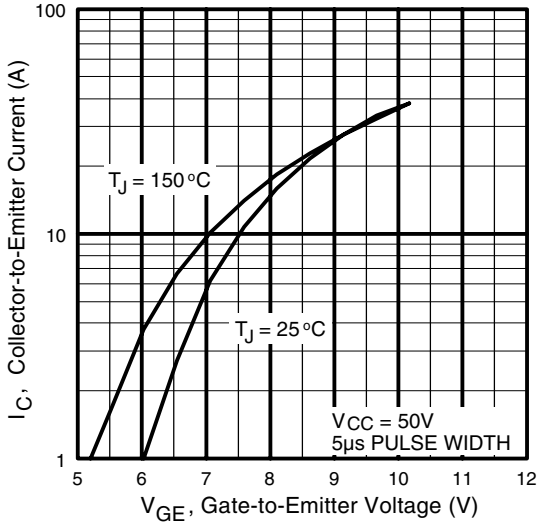


Fig. 3 - Typical Transfer Characteristics

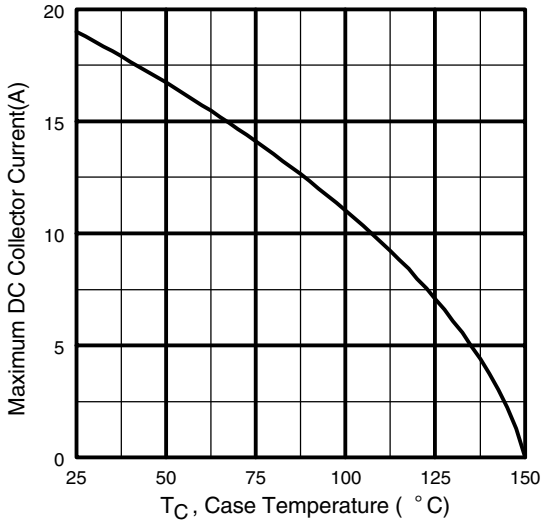


Fig. 4 - Maximum Collector Current vs. Case Temperature

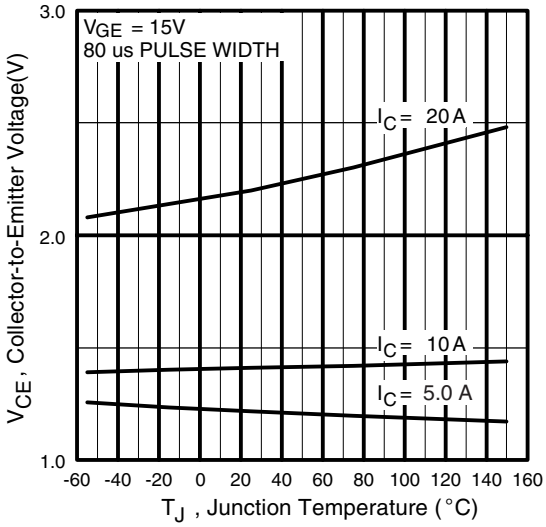


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

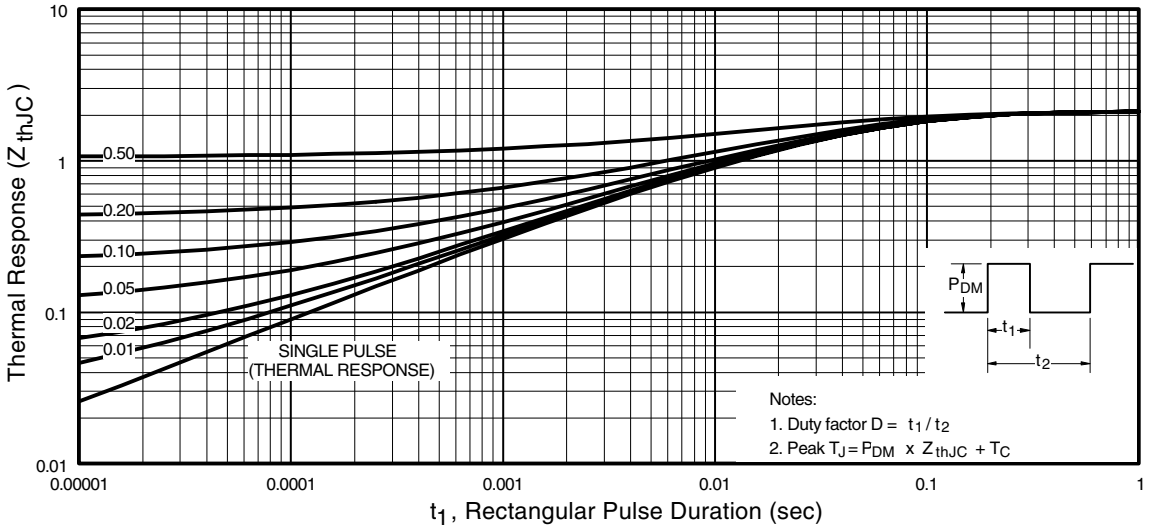


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

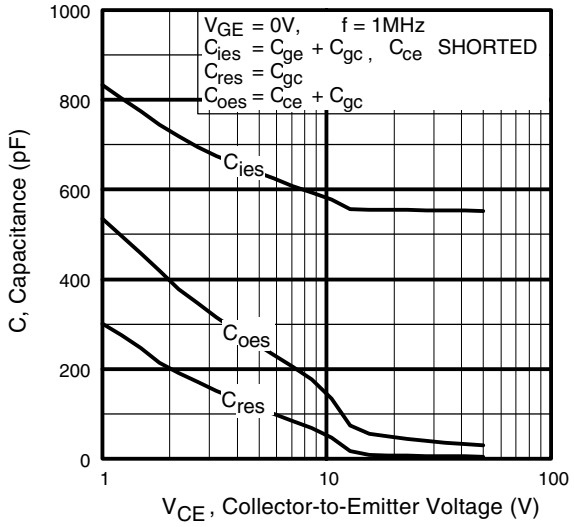


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

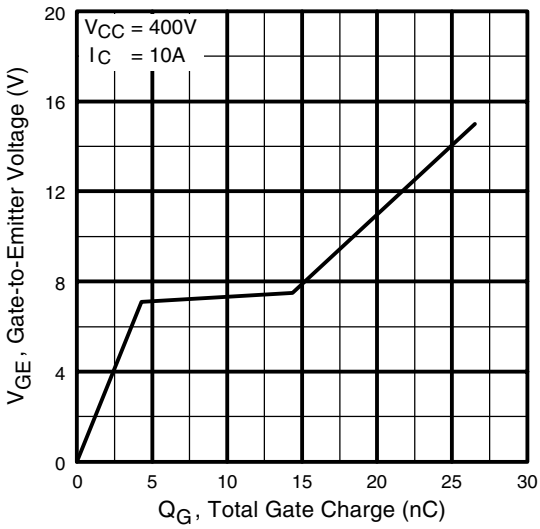


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

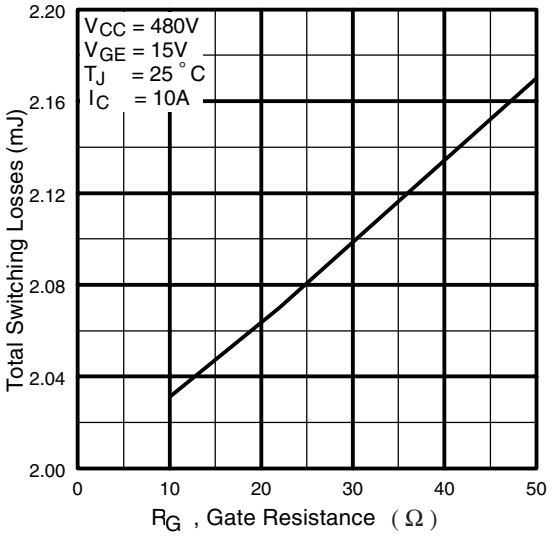


Fig. 9 - Typical Switching Losses vs. Gate Resistance

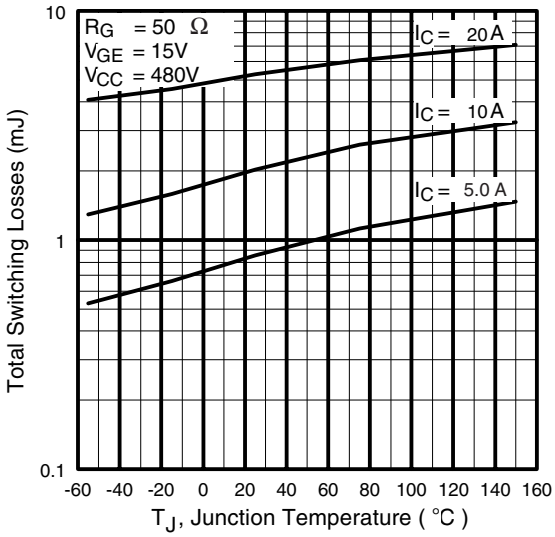


Fig. 10 - Typical Switching Losses vs. Junction Temperature

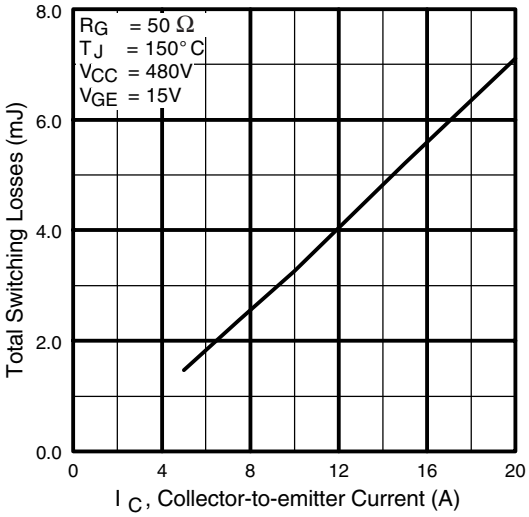


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

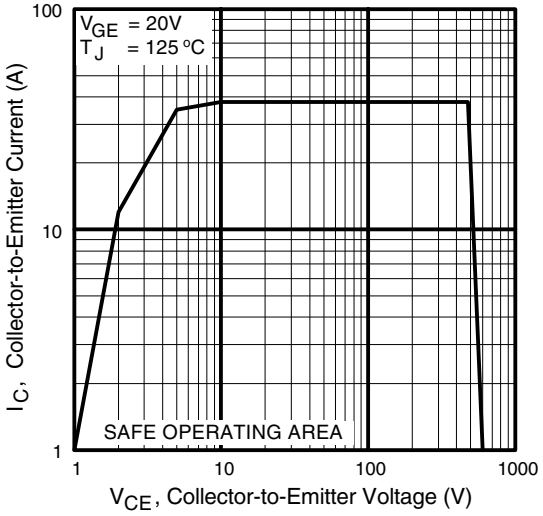


Fig. 12 - Turn-Off SOA

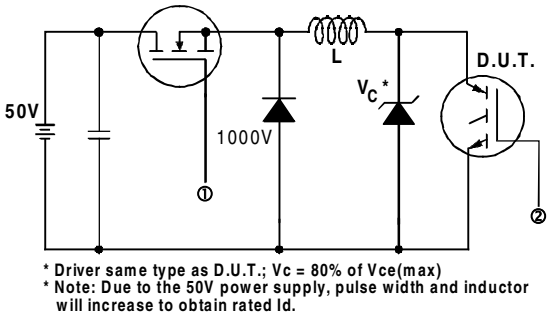


Fig. 13a - Clamped Inductive Load Test Circuit

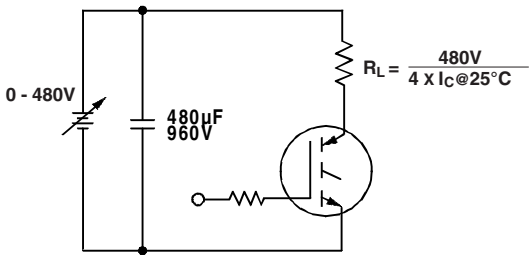


Fig. 13b - Pulsed Collector Current Test Circuit

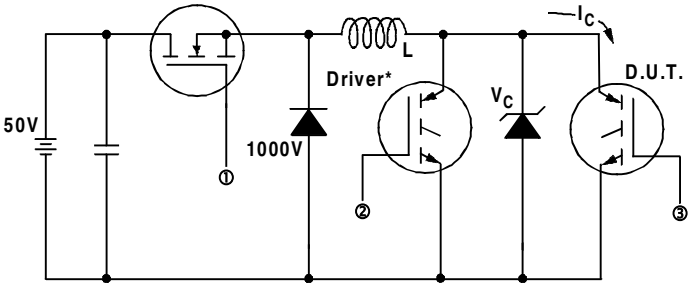


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

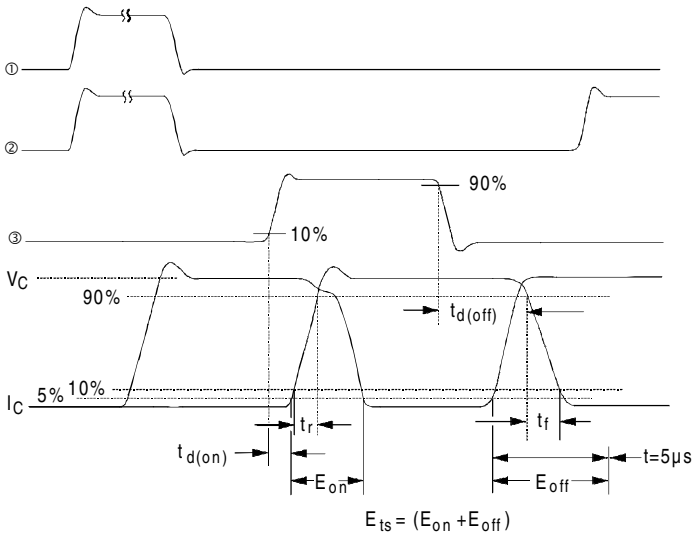
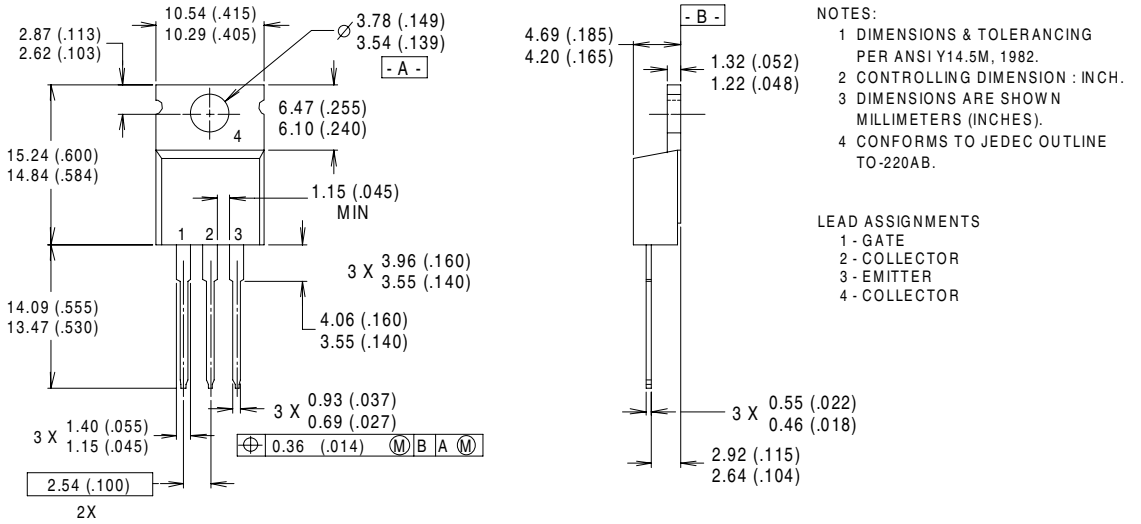


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD- 91793

International
IOR Rectifier

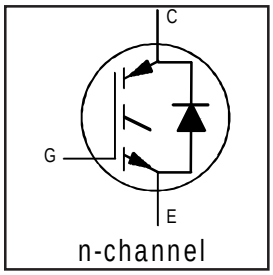
IRG4BC20SD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Standard Speed IGBT

Features

- Extremely low voltage drop 1.4Vtyp. @ 10A
- S-Series: Minimizes power dissipation at up to 3 KHz PWM frequency in inverter drives, up to 4 KHz in brushless DC drives.
- Very Tight Vce(on) distribution
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-220AB package



n-channel

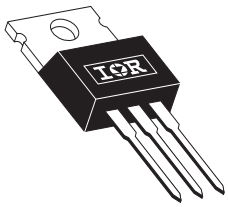
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 1.4V

@V_{GE} = 15V, I_C = 10A

Benefits

- Generation 4 IGBT's offer highest efficiencies available
- IGBT's optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBT's . Minimized recovery characteristics require less/no snubbing
- Lower losses than MOSFET's conduction and Diode losses



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	19	A
I_C @ T_C = 100°C	Continuous Collector Current	10	
I_{CM}	Pulsed Collector Current ①	38	
I_{LM}	Clamped Inductive Load Current ②	38	
I_F @ T_C = 100°C	Diode Continuous Forward Current	7.0	
I_{FM}	Diode Maximum Forward Current	38	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	2.1	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	3.5	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	80	
Wt	Weight	—	2 (0.07)	—	g (oz)

9/23/98

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage*f*	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.75	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.40	1.6	V	I_C = 10A V_{GE} = 15V
		—	1.85	—		I_C = 19A See Fig. 2, 5
		—	1.44	—		I_C = 10A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	2.0	5.8	—	S	V_{CE} = 100V, I_C = 10A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	1700		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	I_C = 8.0A See Fig. 13
		—	1.3	1.6		I_C = 8.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	27	40	nC	I_C = 10A
Qge	Gate - Emitter Charge (turn-on)	—	4.3	6.5		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	10	15		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	62	—	ns	T_J = 25°C
t_r	Rise Time	—	32	—		I_C = 10A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	690	1040		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	480	730		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	0.32	—	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	2.58	—		See Fig. 9, 10, 11,18
E_{ts}	Total Switching Loss	—	2.90	4.5		
$t_{d(on)}$	Turn-On Delay Time	—	64	—	ns	T_J = 150°C, See Fig. 10,11, 18
t_r	Rise Time	—	35	—		I_C = 10A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	980	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	800	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	4.33	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	550	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	39	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	7.1	—		*f* = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	37	55	ns	T_J = 25°C See Fig.
		—	55	90		T_J = 125°C 14 I_F = 8.0A
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	5.0	A	T_J = 25°C See Fig.
		—	4.5	8.0		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	65	138	nC	T_J = 25°C See Fig.
		—	124	360		T_J = 125°C 16 di/dt = 200Aµs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	240	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	210	—		T_J = 125°C 17

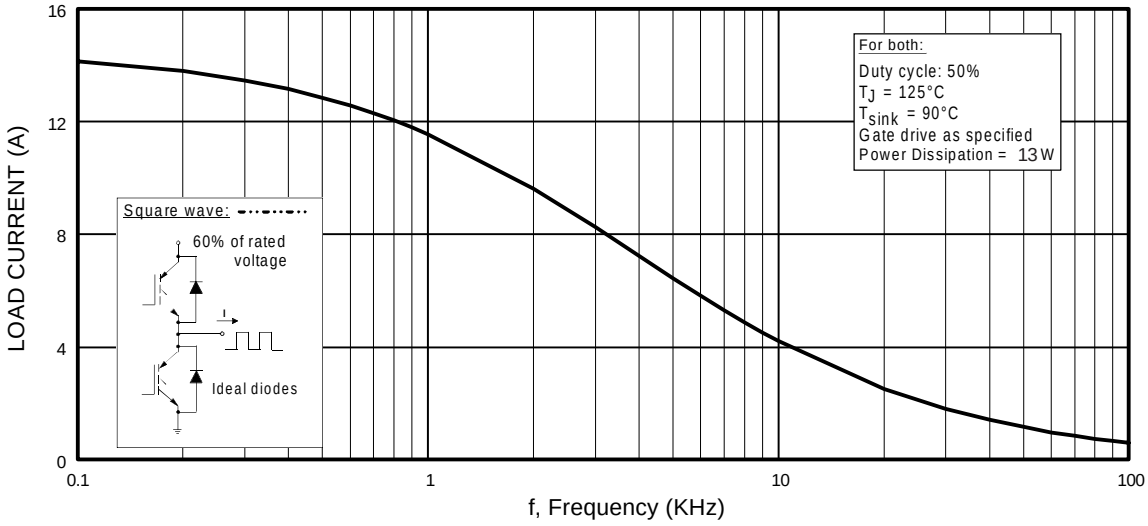


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

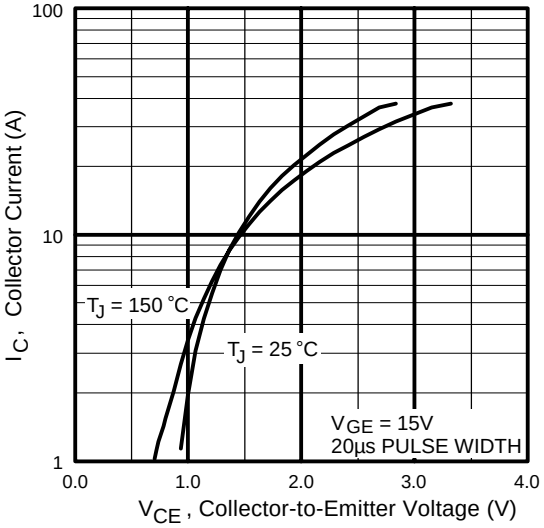


Fig. 2 - Typical Output Characteristics

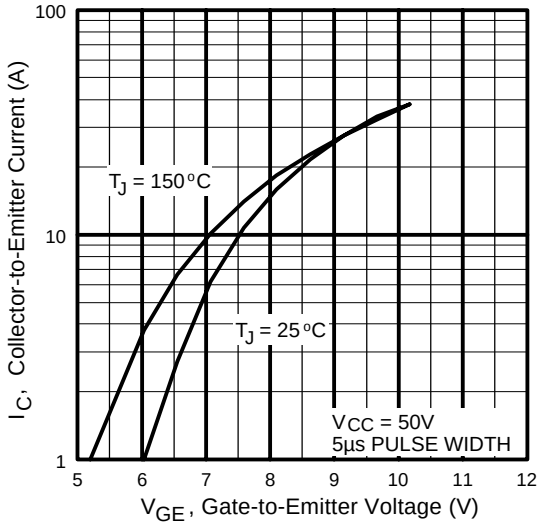


Fig. 3 - Typical Transfer Characteristics

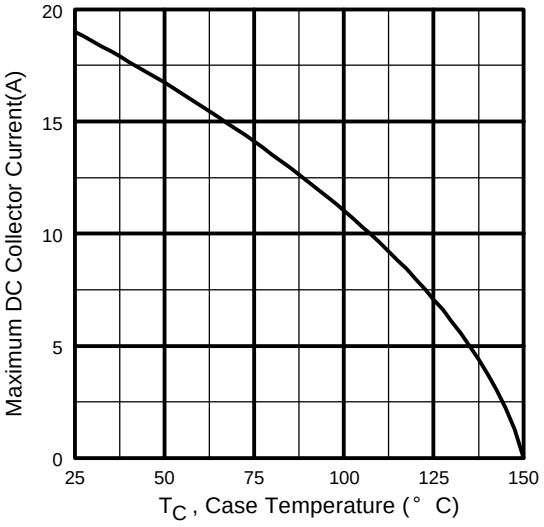


Fig. 4 - Maximum Collector Current vs. Case Temperature

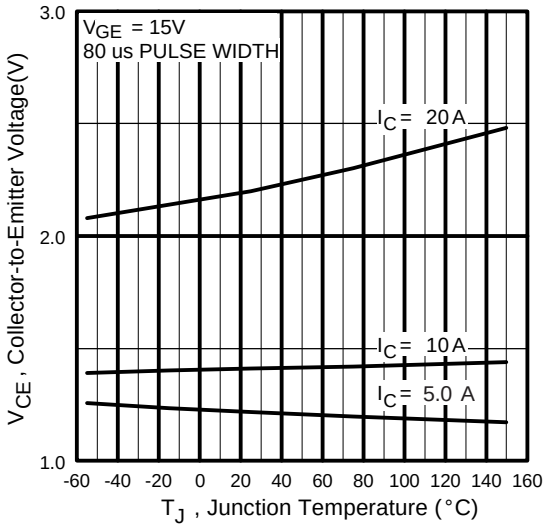


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

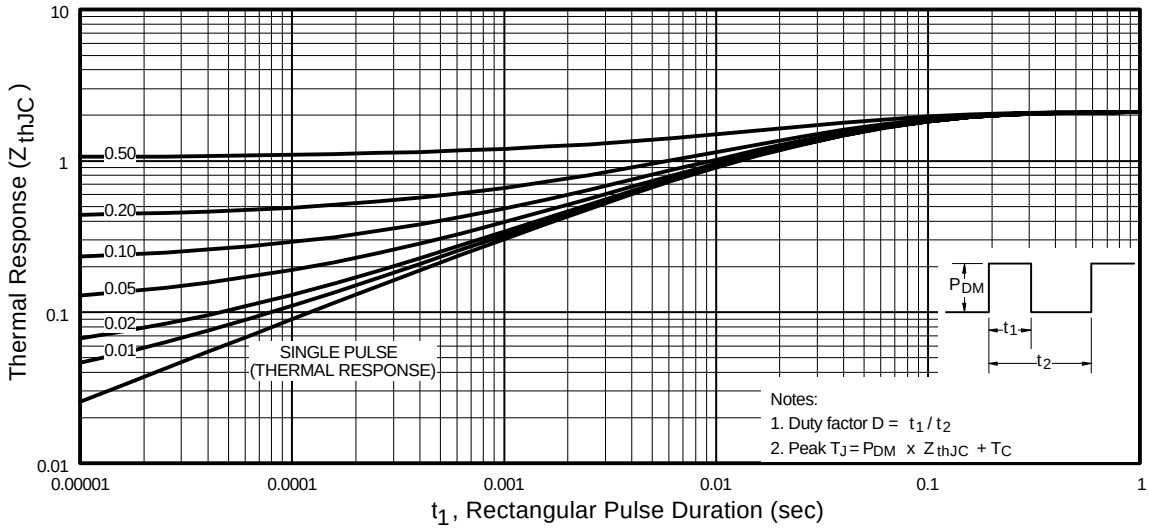


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

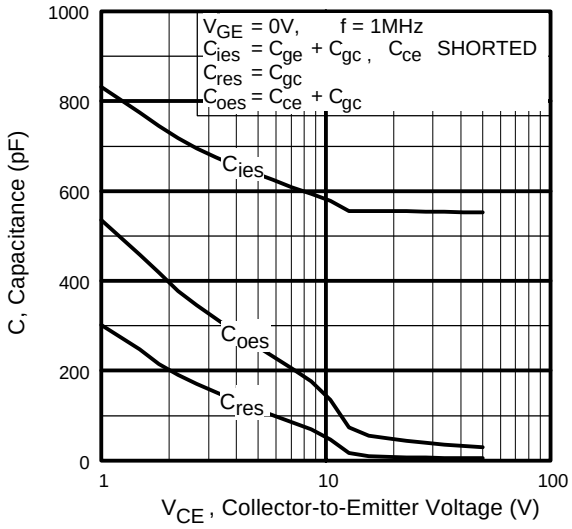


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

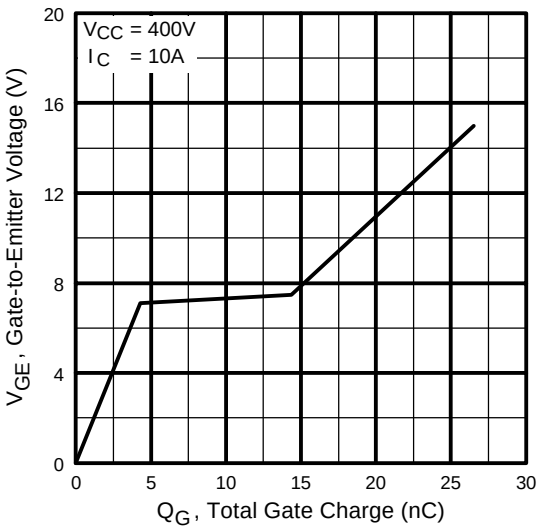


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

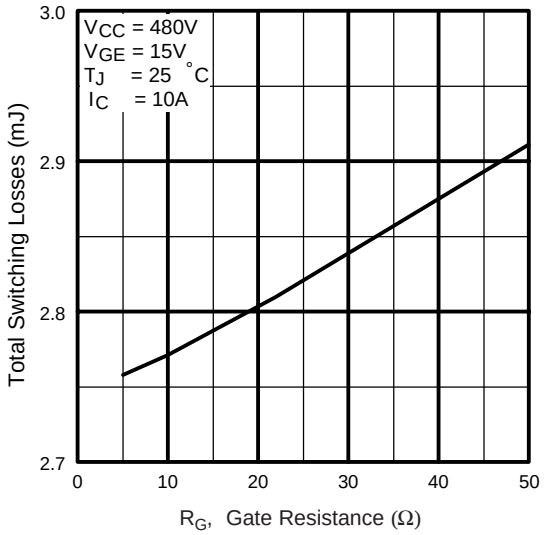


Fig. 9 - Typical Switching Losses vs. Gate Resistance

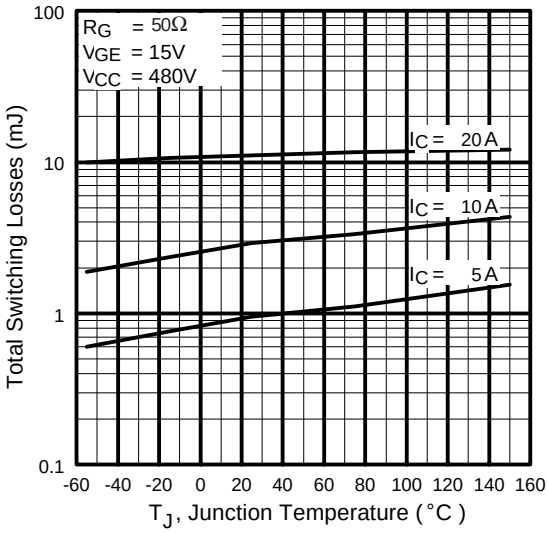


Fig. 10 - Typical Switching Losses vs. Junction Temperature

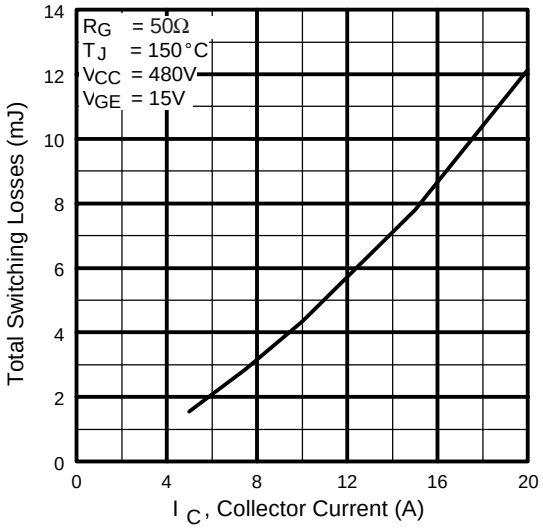


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

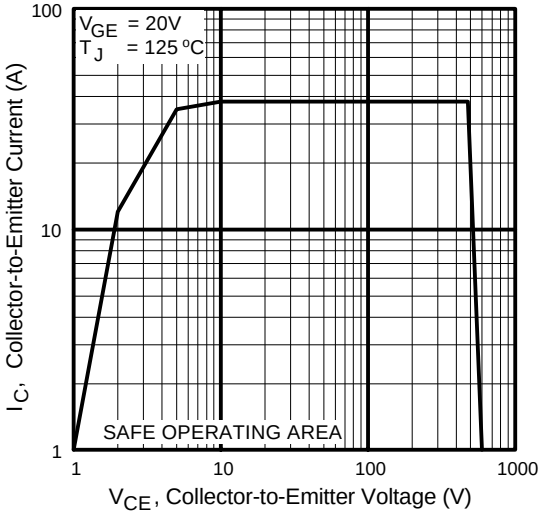


Fig. 12 - Turn-Off SOA

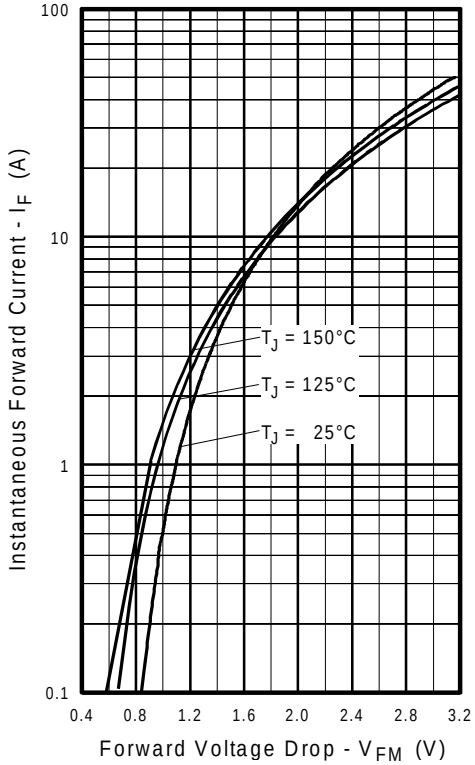


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

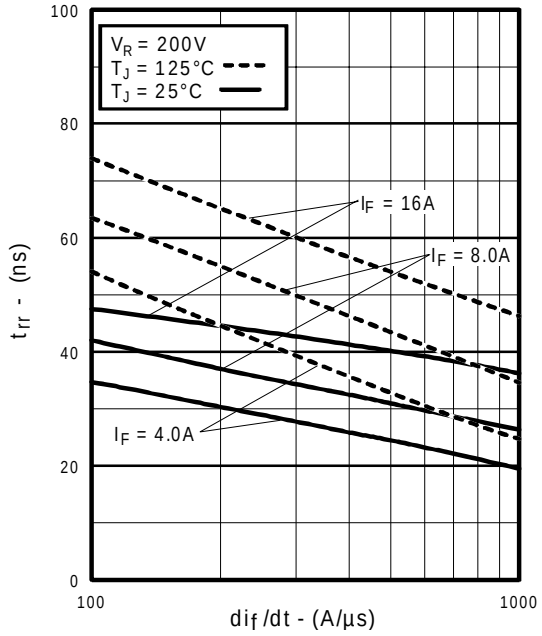


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

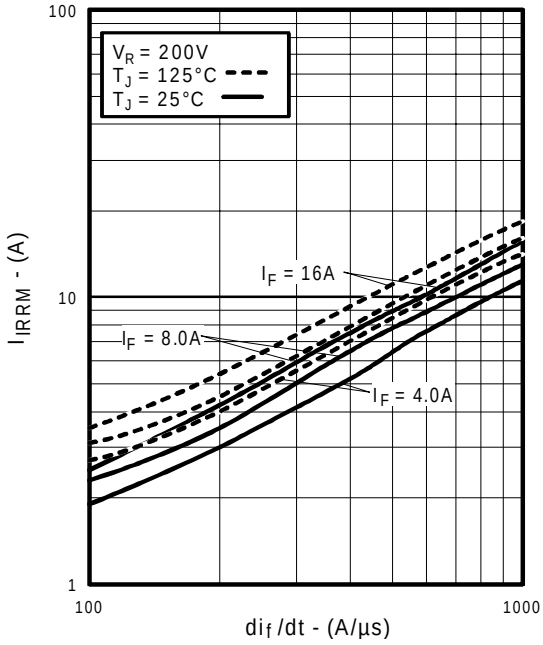


Fig. 15 - Typical Recovery Current vs. di_f/dt

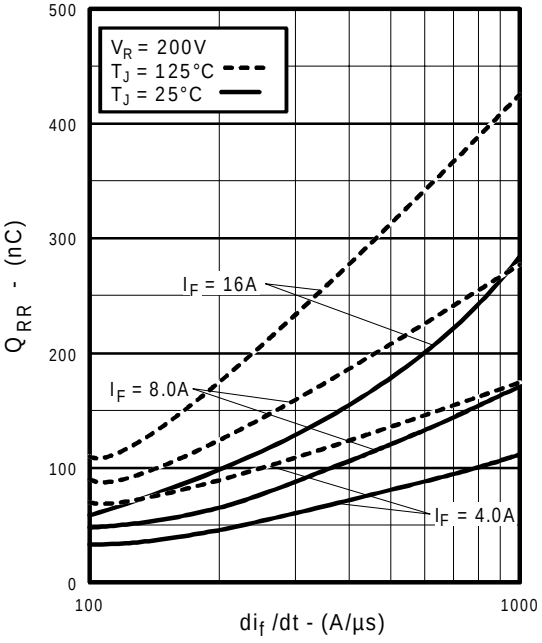


Fig. 16 - Typical Stored Charge vs. di_f/dt

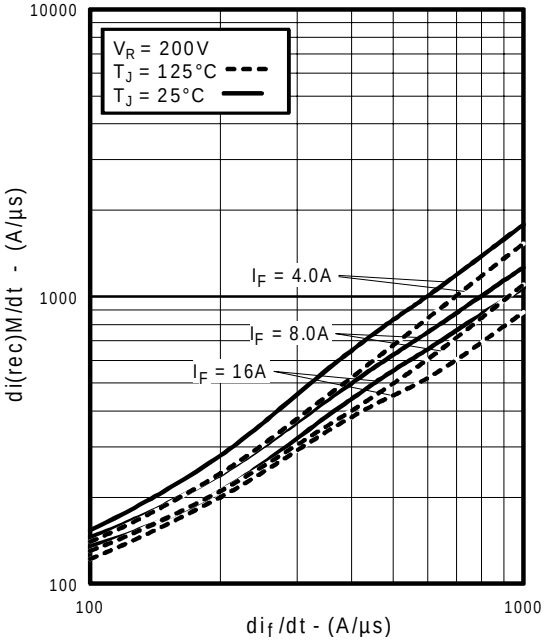


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

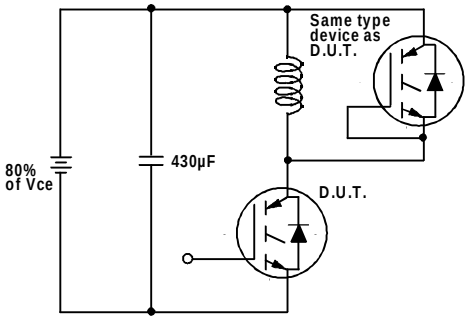


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

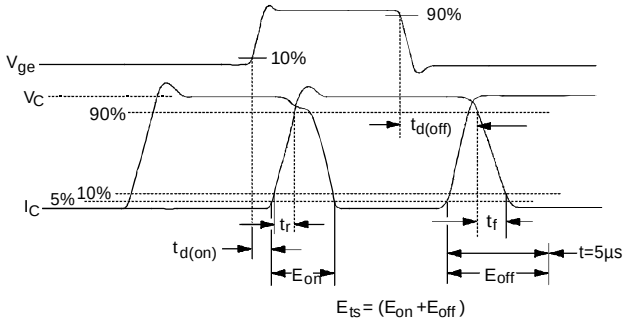


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

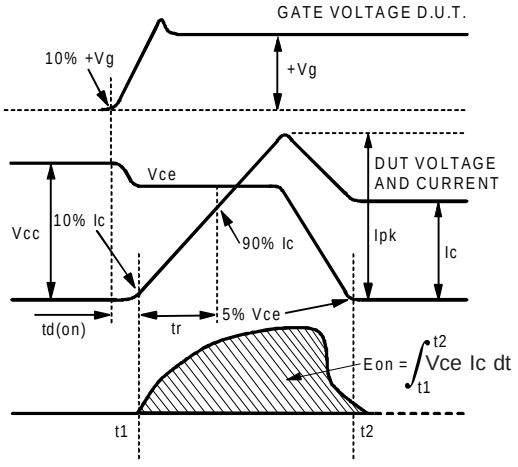


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

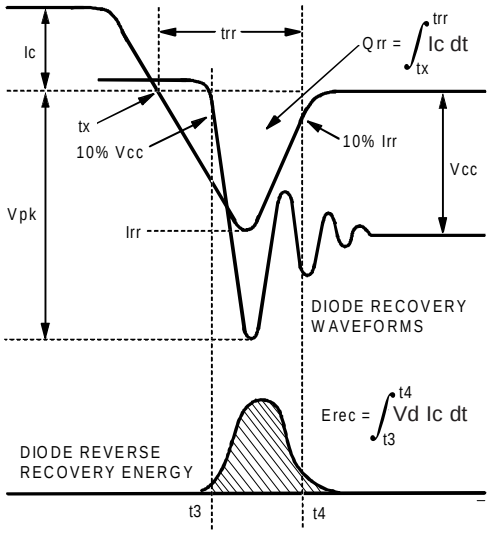


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

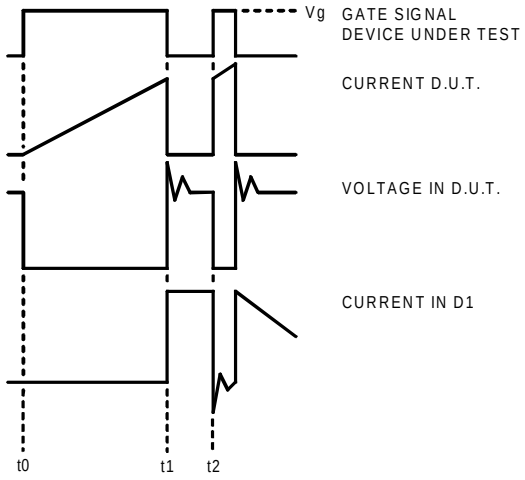


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

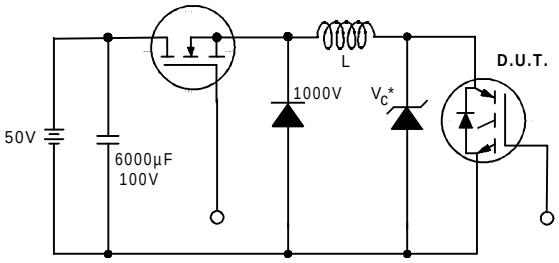


Figure 19. Clamped Inductive Load Test Circuit

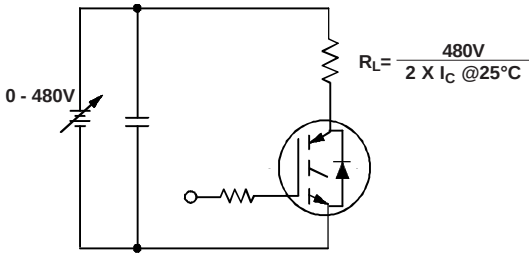


Figure 20. Pulsed Collector Current Test Circuit

Notes:

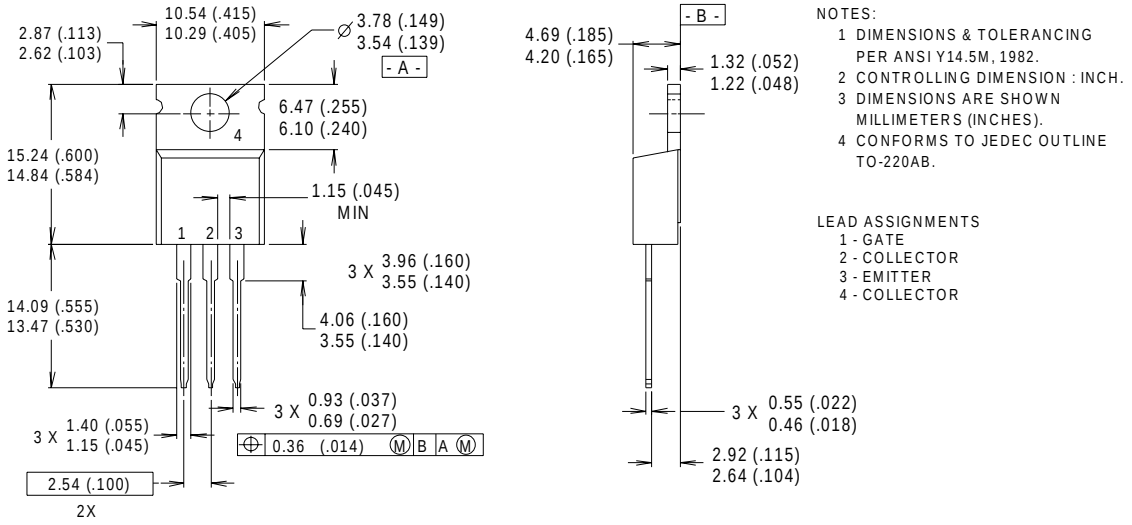
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G = 50Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936
http://www.irf.com/ Data and specifications subject to change without notice. 9/98

Fig.1 - Typical Diode Recovery
V_{CC}=600V; Rg=5Ω; T_J=125°C;
L=200µH; Driver=IRGC100B120KB

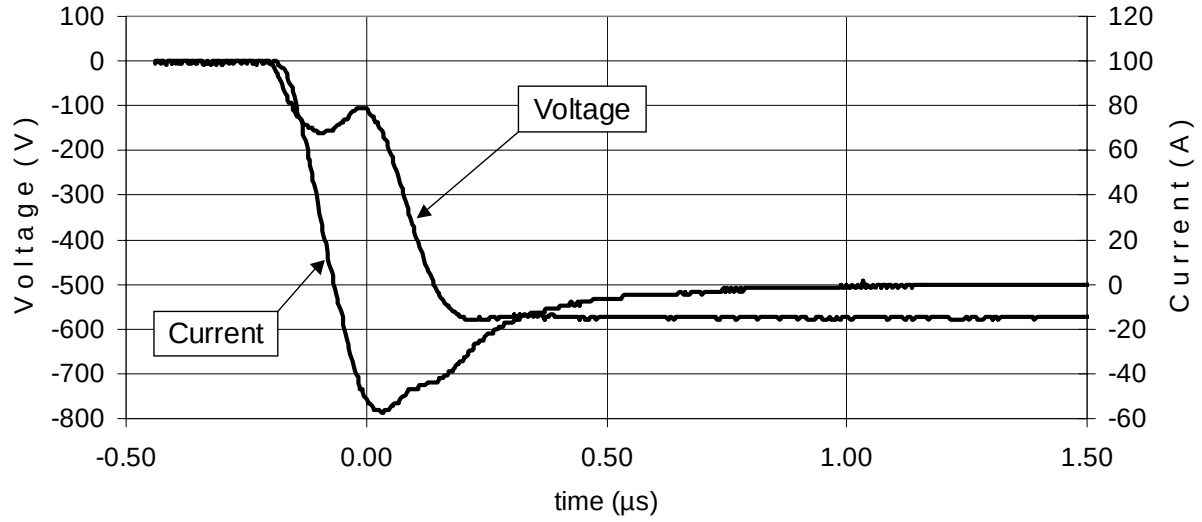


Fig.2 - Typical Diode Forward Characteristic
tp=300µs

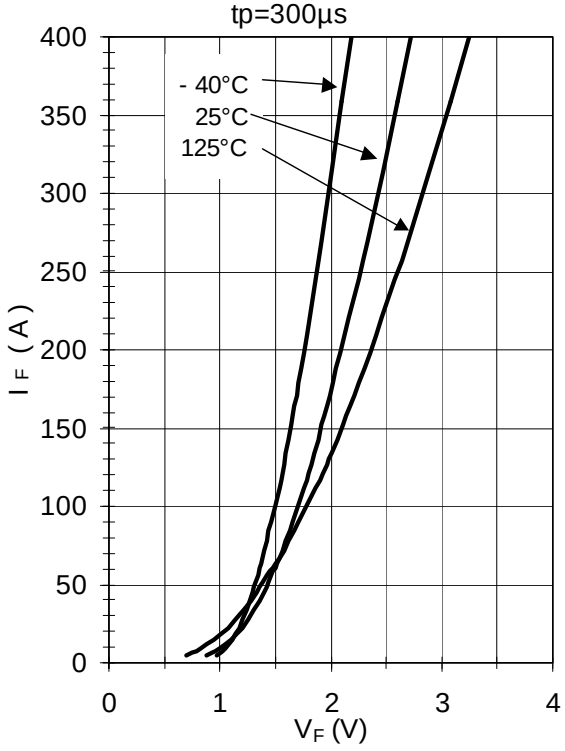
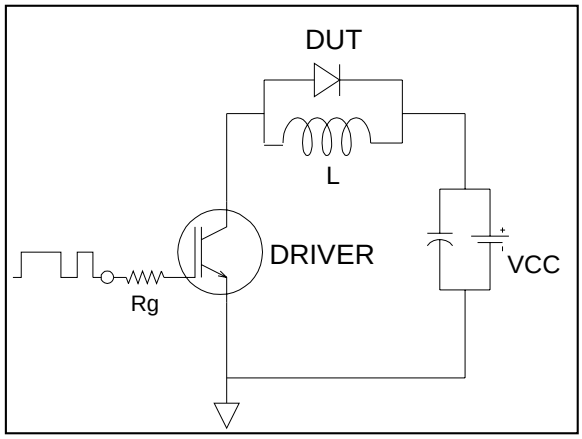


Fig. 3 - Diode Recovery Circuit



Bulletin I0115J 09/00

International
IOR Rectifier

IR135DM16CCB

STANDARD RECOVERY DIODES

- **Junction Size:** **Rectangular 135 x 100 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **1600 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:** **8EWS..S Series**

Major Ratings and Characteristics

Parameters		Units	Test Conditions	
V_{FM}	Maximum Forward Voltage	1.15V	T_J = 25°C, I_F = 8 A	
V_{RRM}	Reverse Breakdown Voltage	1600 V **(**)**	T_J = 25°C, I_{RRM} = 100 µA	**(*)**

(*) Nitrogen flow on die edge.

(**) Wafer and die Probe test clamped at 1200V to limit arcing. **1600V BV testable only in encapsulated packages**

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (5 µm)
Chip Dimensions	135 x 100 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	330 µm, ± 10 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

International
IOR Rectifier

Ordering Information Table

Device Code

IR	135	D	M	16	C	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: D = Wire Bondable Standard Recovery Diode

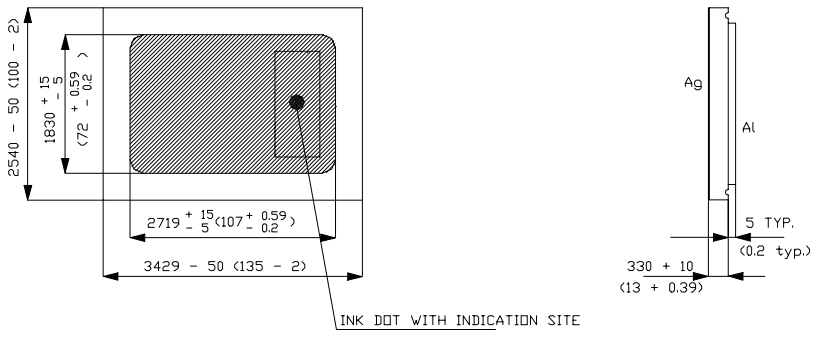
4 - Passivation Process: M = Glassivated MOAT

5 - Voltage code: Code x 100 = V_{RRM}

6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

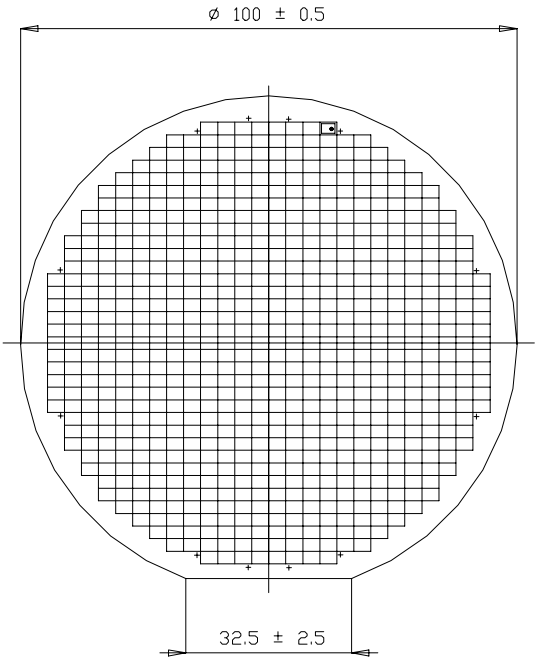


All dimensions are in microns (mils)

Wafer Layout

TOP VIEW

N° 734 Basic Cells



All dimensions are in millimeters

Bulletin I0122J rev. A 02/97

International
IOR Rectifier

IR135DM12CCB

STANDARD RECOVERY DIODES

- **Junction Size:** **Rectangular 135 x 100 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **1200 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:** **8EWS..S Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	1.1 V	T_J = 25°C, I_F = 8 A
V_{RRM} Reverse Breakdown Voltage	1200 V	T_J = 25°C, I_{RRM} = 100 µA **(1)**

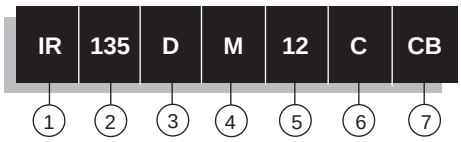
(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20 µm)
Chip Dimensions	135 x 100 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	300 µm, ± 10 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code



1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: D = Wire Bondable Standard Recovery Diode

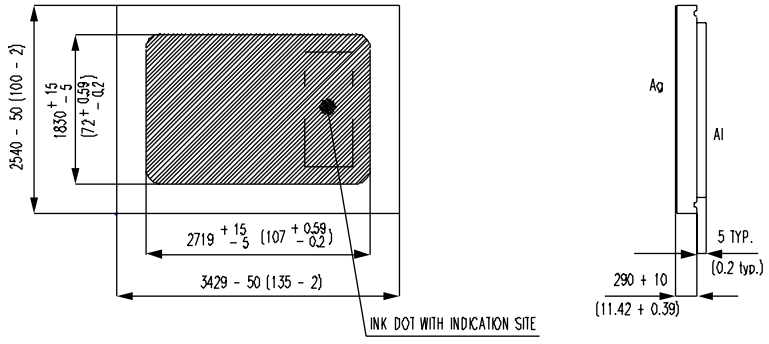
4 - Passivation Process: M = Glassivated MOAT

5 - Voltage code: Code x 100 = V_{RRM}

6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

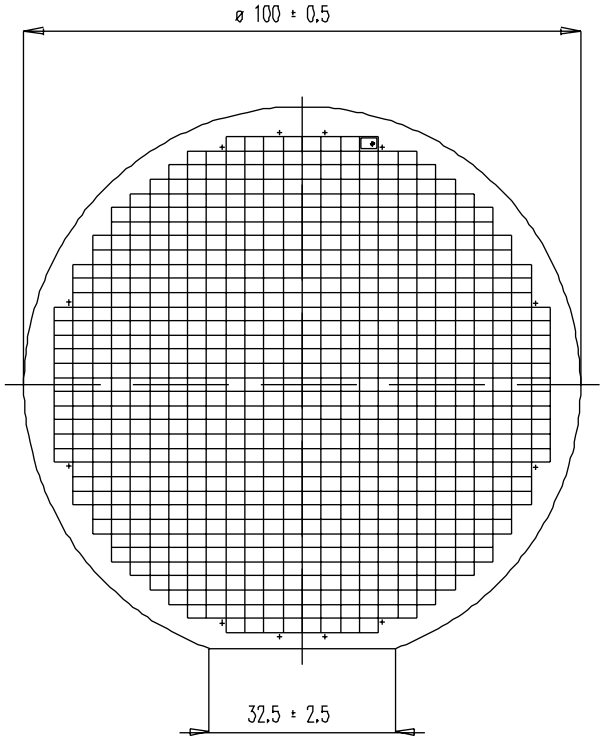


All dimensions are in microns (mils)

Wafer Layout

TOP VIEW

N° 735 Basic Cells



All dimensions are in millimeters

International
IOR Rectifier

IR150DG..HCB SERIES

HIGH POWER RECTIFIER DIODES

- **Junction Size:** **Square 150 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **600 and 1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **12F Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	1100 mV	T_J = 25°C I_F = 25A
V_{RRM} Reverse Breakdown Voltage Range	600 and 1200 V	T_J = 25°C I_R = 100µA **(1)**

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	150 x 150 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	300 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	150	D	G	12	H	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: D = Standard Recovery Diode

4 - Passivation Process: G = Glassivated MESA

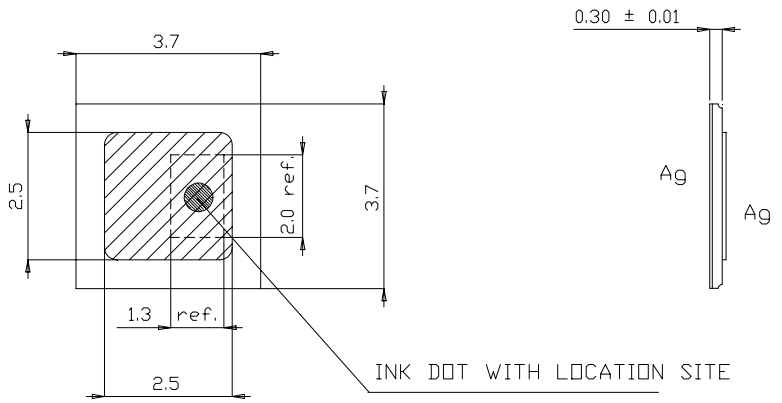
5 - Voltage code: Code x 100 = V_{RRM}

Available Class	
06 =	600V
12 =	1200V

6 - Metallization: H = Silver (Anode) - Silver (Cathode)

7 - Probed Uncut Die

Outline Table



All dimensions are in millimeters

Bulletin I0132J 05/99

International
IOR Rectifier

IR180DG..HCB SERIES

HIGH POWER RECTIFIER DIODES

- **Junction Size:** **Square 180 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **600 and 1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **26MB Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	1030 mV	T_J = 25°C I_F = 25A
V_{RRM} Reverse Breakdown Voltage Range	600 and 1200 V	T_J = 25°C I_R = 100µA **(1)**

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	180 x 180 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	300 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	180	D	G	12	H	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: D = Standard Recovery Diode

4 - Passivation Process: G = Glassivated MESA

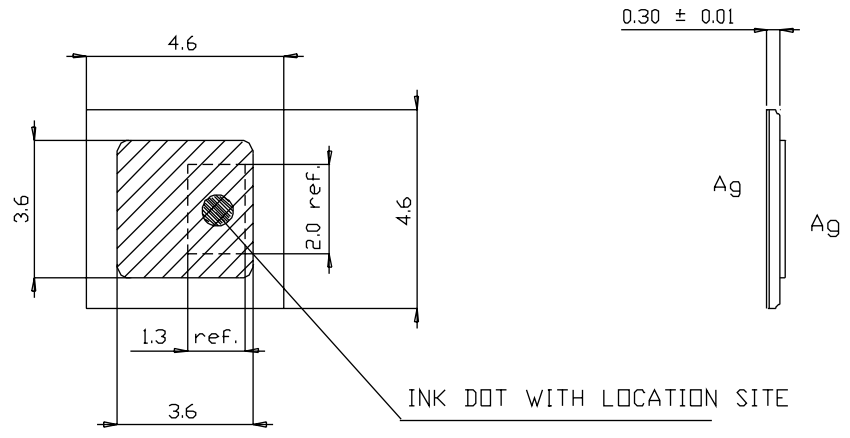
5 - Voltage code: Code x 100 = V_{RRM}

Available Class
06 = 600V
12 = 1200V

6 - Metallization: H = Silver (Anode) - Silver (Cathode)

7 - Probed Uncut Die

Outline Table

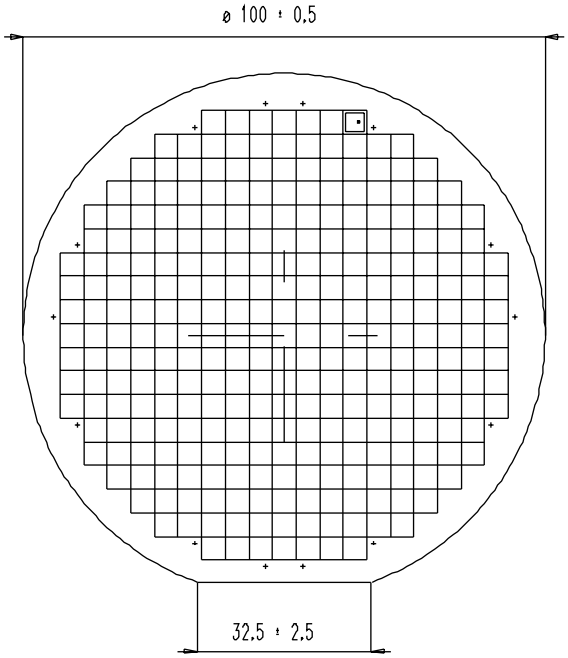


All dimensions are in millimeters

Wafer Layout

TOP VIEW

N° 293 Basic Cells



All dimensions are in millimeters

Bulletin I0116J 09/00

International
IOR Rectifier

IR180DM16CCB SERIES

STANDARD RECOVERY DIODES

- **Junction Size:** **Square 180 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **1600 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:** **20ETS Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	1100 mV	T_J = Amb., I_F = 20 A
V_{RRM} Reverse Breakdown Voltage Range	1600 V **(**)**	T_J = Amb., I_{RRM} = 100 µA **(*)**

(*) Nitrogen flow on die edge.

(**) Wafer and die Probe test clamped at 1200V to limit arcing. **1600V BV testable only in encapsulated packages**

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20 µm)
Chip Dimensions	180 x 180 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	330 µm, ± 10 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	180	D	M	16	C	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: D = Wire Bondable Standard Recovery Diode

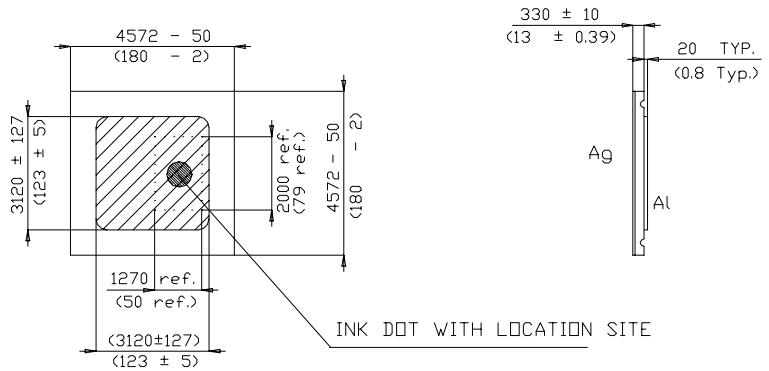
4 - Passivation Process: M = Glassivated MOAT

5 - Voltage code: Code x 100 = V_{RRM}

6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

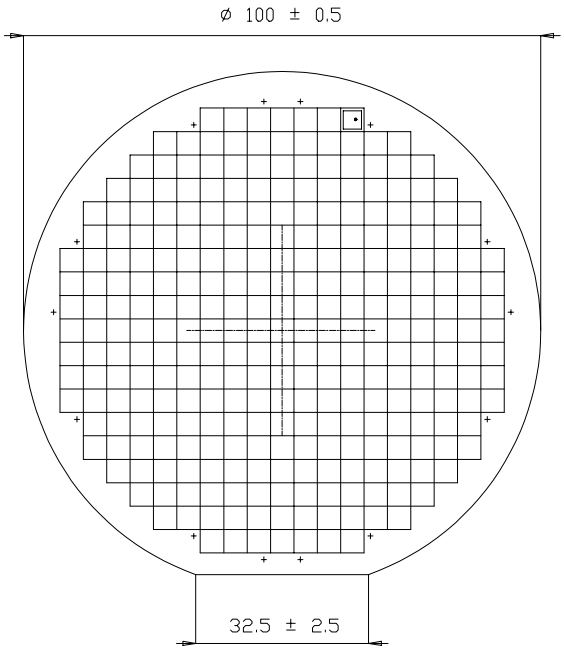


All dimensions are in microns (mils)

Wafer Layout

TOP VIEW

N° 293 Basic Cells



All dimensions are in millimeters

International
IOR Rectifier

IR180DM..CCB SERIES

STANDARD RECOVERY DIODES

- **Junction Size:** **Square 180 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **800 and 1200 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:** **20ETS Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	1050 mV	T_J = Amb., I_F = 20 A
V_{RRM} Reverse Breakdown Voltage Range	800 and 1200 V	T_J = Amb., I_{RRM} = 100 µA **(1)**

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20 µm)
Chip Dimensions	180 x 180 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	300 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	180	D	M	12	C	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: D = Wire Bondable Standard Recovery Diode

4 - Passivation Process: M = Glassivated MOAT

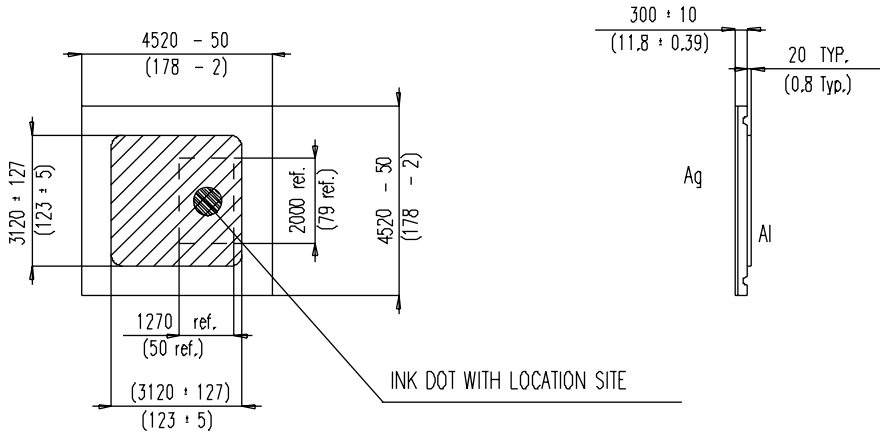
5 - Voltage code: Code x 100 = V_{RRM}

Available Class
08 = 800 V
12 = 1200 V

6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

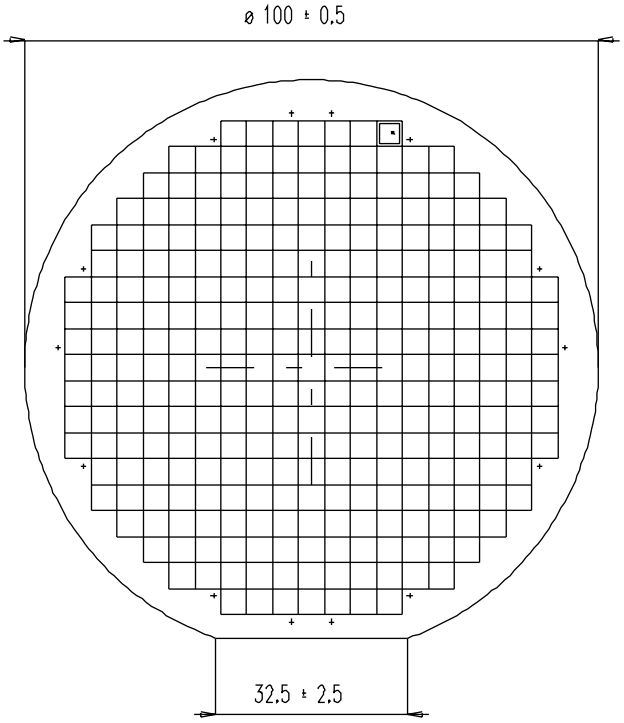


All dimensions are in microns (mils)

Wafer Layout

TOP VIEW

N° 293 Basic Cells



All dimensions are in millimeters

Bulletin I0140J 09/00

International
IOR Rectifier

IR207DM16CCB

STANDARD RECOVERY DIODES

- **Junction Size:** **Rectangular 207 x 157 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **1600 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:** **20ETS Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	1.15 V	T_J = 25°C, I_F = 20 A
V_{RRM} Reverse Breakdown Voltage	1600 V **(**)**	T_J = 25°C, I_{RRM} = 100 µA **(*)**

(*) Nitrogen flow on die edge.

(**) Wafer and die Probe test clamped at 1200V to limit arcing. **1600V BV testable only in encapsulated packages**

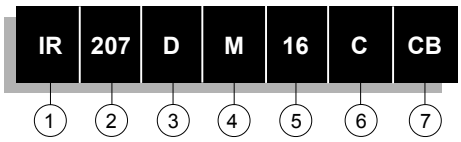
Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20 µm)
Chip Dimensions	207 x 157 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	330 µm, ± 10 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

International
IOR Rectifier

Ordering Information Table

Device Code



1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: D = Wire Bondable Standard Recovery Diode

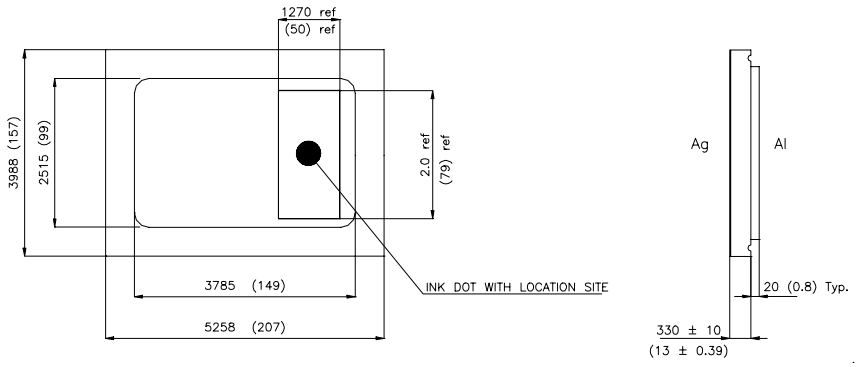
4 - Passivation Process: M = Glassivated MOAT

5 - Voltage code: Code x 100 = V_{RRM}

6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

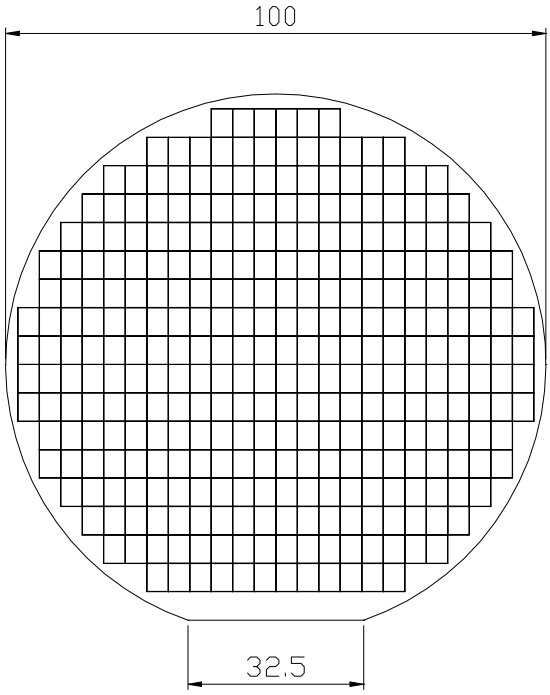


All dimensions are in microns (mils)

Wafer Layout

TOP VIEW

N° 304 Basic Cells



All dimensions are in millimeters

Bulletin I0133J 05/99

International
IOR Rectifier

IR210DG..HCB SERIES

HIGH POWER RECTIFIER DIODES

- **Junction Size:** **Square 210 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **600 and 1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **40HF Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	1000 mV	T_J = 25°C I_F = 25A
V_{RRM} Reverse Breakdown Voltage Range	600 and 1200 V	T_J = 25°C I_R = 100µA **(1)**

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	210 x 210 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	300 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	210	D	G	12	H	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: D = Standard Recovery Diode

4 - Passivation Process: G = Glassivated MESA

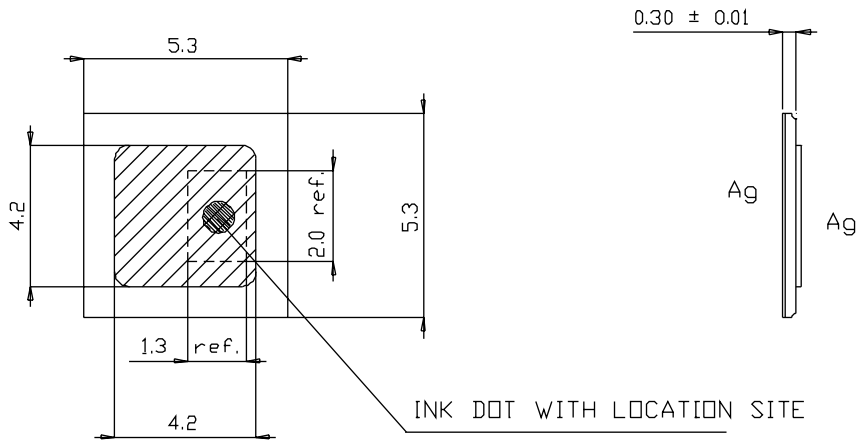
5 - Voltage code: Code x 100 = V_{RRM}

Available Class
06 = 600V
12 = 1200V

6 - Metallization: H = Silver (Anode) - Silver (Cathode)

7 - Probed Uncut Die

Outline Table

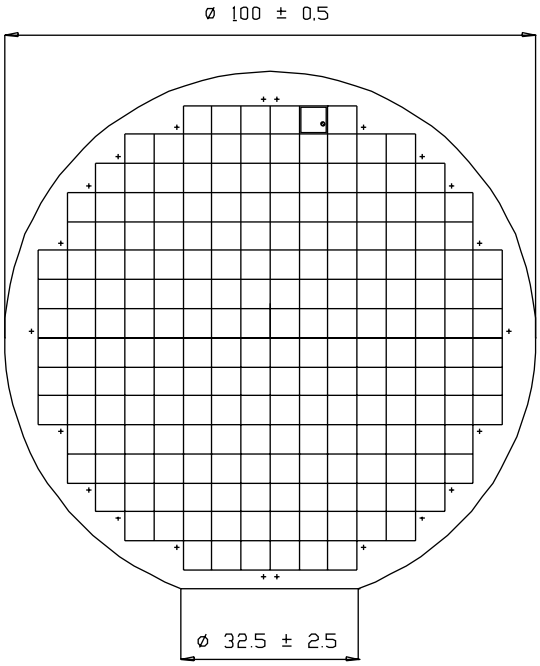


All dimensions are in millimeters

Wafer Layout

TOP VIEW

N° 208 Basic Cells



All dimensions are in millimeters

Bulletin I0134J 05/99

International
IOR Rectifier

IR230DG..HCB SERIES

HIGH POWER RECTIFIER DIODES

- **Junction Size:** **Square 230 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **600 and 1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **9AF Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	1000 mV	T_J = 25°C I_F = 25A
V_{RRM} Reverse Breakdown Voltage Range	600 and 1200 V	T_J = 25°C I_R = 100µA **(1)**

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	230 x 230 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	300 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	230	D	G	12	H	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: D = Standard Recovery Diode

4 - Passivation Process: G = Glassivated MESA

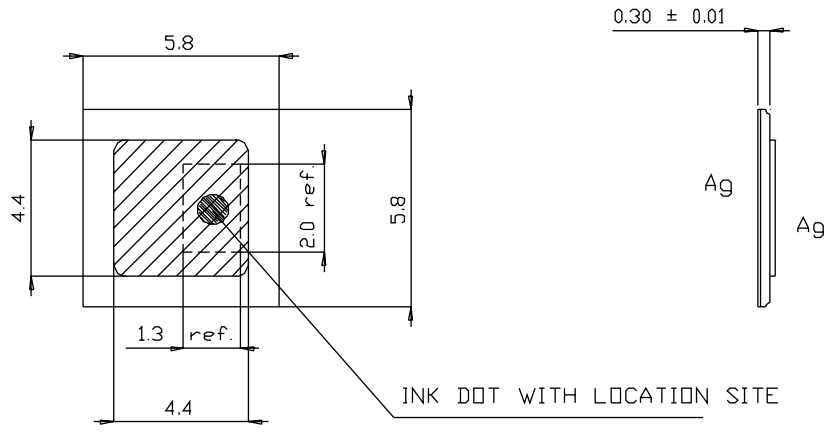
5 - Voltage code: Code x 100 = V_{RRM}

Available Class
06 = 600V
12 = 1200V

6 - Metallization: H = Silver (Anode) - Silver (Cathode)

7 - Probed Uncut Die

Outline Table

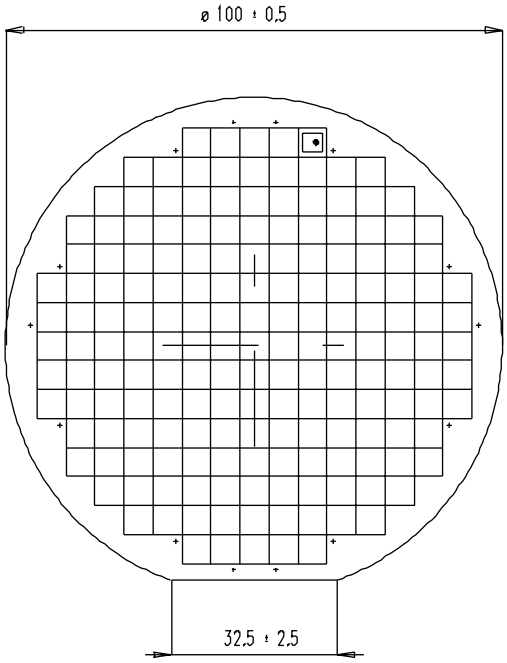


All dimensions are in millimeters

Wafer Layout

TOP VIEW

N° 177 Basic Cells



All dimensions are in millimeters

Bulletin I0121J rev. A 02/97

International
IOR Rectifier

IR230DM12CCB

STANDARD RECOVERY DIODES

- **Junction Size:** **Square 230 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **1200 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:** **40EPS Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	1050 mV	T_J = 25°C, I_F = 20 A
V_{RRM} Reverse Breakdown Voltage	1200 V	T_J = 25°C, I_{RRM} = 100 µA **(1)**

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20 µm)
Chip Dimensions	230 x 230 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	300 µm, ± 10 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	230	D	M	12	C	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: D = Wire Bondable Standard Recovery Diode

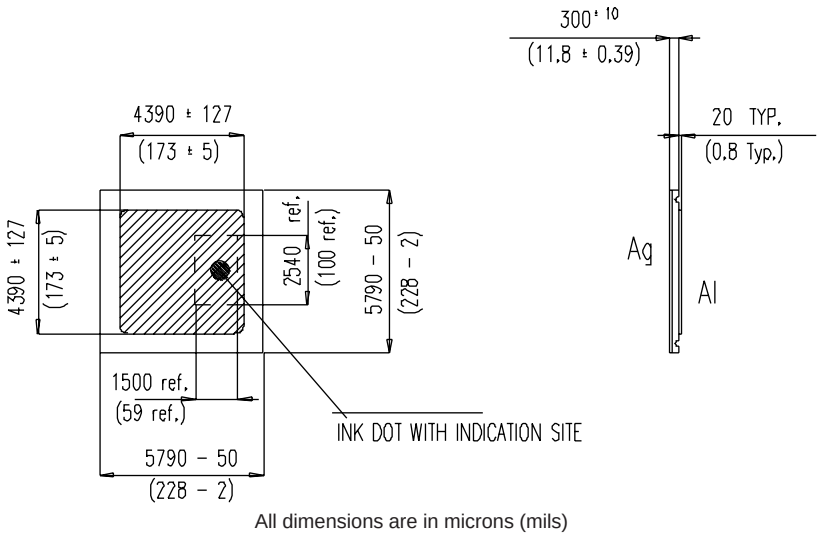
4 - Passivation Process: M = Glassivated MOAT

5 - Voltage code: Code x 100 = V_{RRM}

6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

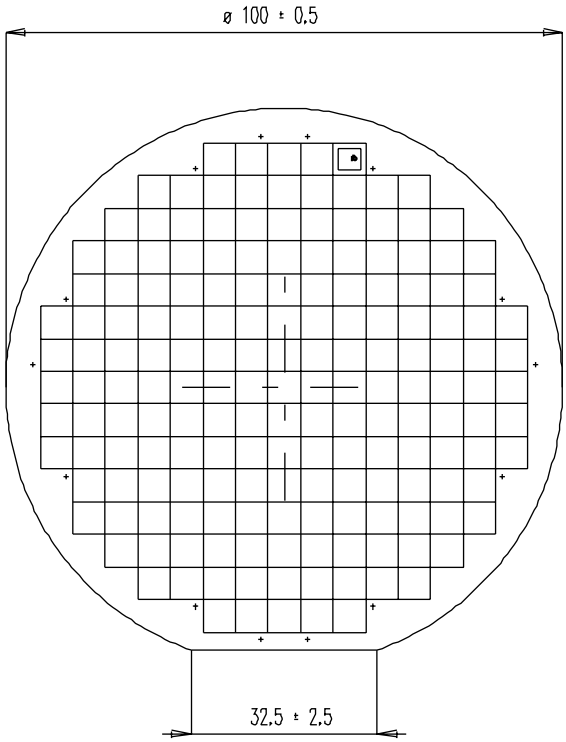


All dimensions are in microns (mils)

Wafer Layout

TOP VIEW

N° 177 Basic Cells



All dimensions are in millimeters

Bulletin I0117J 09/00

International
IOR Rectifier

IR230DM16CCB

STANDARD RECOVERY DIODES

- **Junction Size:** **Square 230 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **1600 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:** **40EPS Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	1050 mV	T_J = 25°C, I_F = 20 A
V_{RRM} Reverse Breakdown Voltage	1600 V **(**)**	T_J = 25°C, I_{RRM} = 100 µA **(*)**

(*) Nitrogen flow on die edge.

(**) Wafer and die Probe test clamped at 1200V to limit arcing. **1600V BV testable only in encapsulated packages**

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20 µm)
Chip Dimensions	230 x 230 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	330 µm, ± 10 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	230	D	M	16	C	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: D = Wire Bondable Standard Recovery Diode

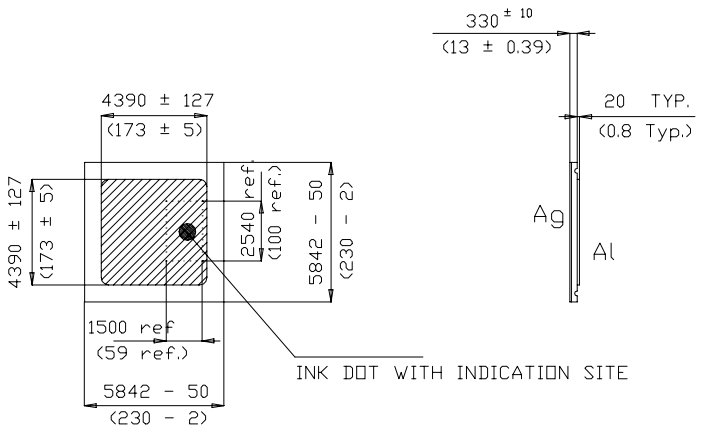
4 - Passivation Process: M = Glassivated MOAT

5 - Voltage code: Code x 100 = V_{RRM}

6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

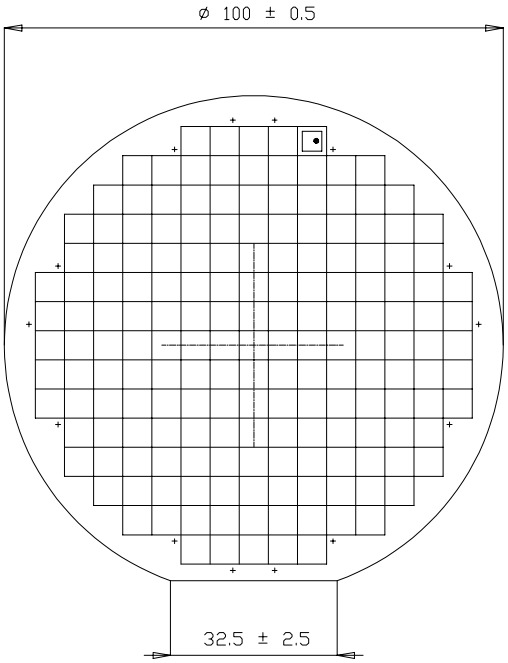


All dimensions are in microns (mils)

Wafer Layout

TOP VIEW

N° 177 Basic Cells



All dimensions are in millimeters

Bulletin I0121J rev. A 02/97

International
IOR Rectifier

IR230DM12CCB

STANDARD RECOVERY DIODES

- **Junction Size:** **Square 230 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **1200 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:** **40EPS Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	1050 mV	T_J = 25°C, I_F = 20 A
V_{RRM} Reverse Breakdown Voltage	1200 V	T_J = 25°C, I_{RRM} = 100 µA **(1)**

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20 µm)
Chip Dimensions	230 x 230 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	300 µm, ± 10 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	230	D	M	12	C	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: D = Wire Bondable Standard Recovery Diode

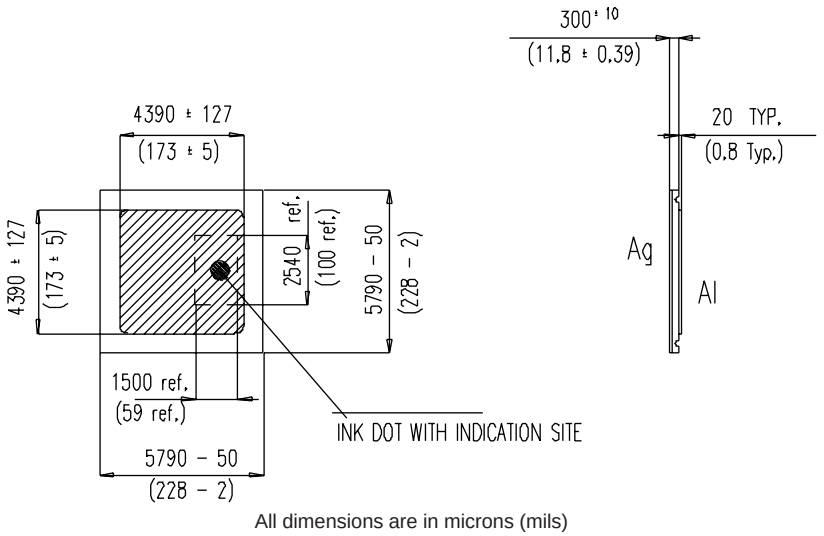
4 - Passivation Process: M = Glassivated MOAT

5 - Voltage code: Code x 100 = V_{RRM}

6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

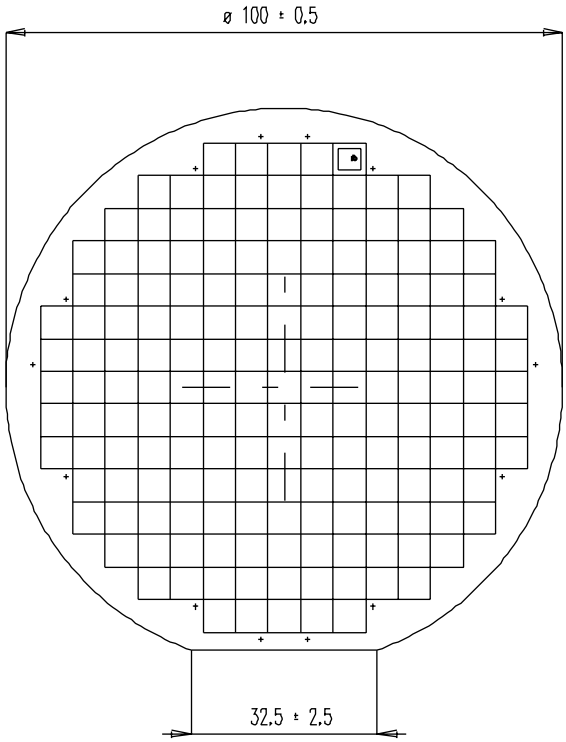


All dimensions are in microns (mils)

Wafer Layout

TOP VIEW

N° 177 Basic Cells



All dimensions are in millimeters

Bulletin I0135J 05/99

International
IOR Rectifier

IR280DG..HCB SERIES

HIGH POWER RECTIFIER DIODES

- **Junction Size:** **Square 280 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **600 and 1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **70HF Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	990 mV	T_J = 25°C I_F = 25A
V_{RRM} Reverse Breakdown Voltage Range	600 and 1200 V	T_J = 25°C I_R = 100µA **(1)**

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	280 x 280 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	300 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	280	D	G	12	H	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: D = Standard Recovery Diode

4 - Passivation Process: G = Glassivated MESA

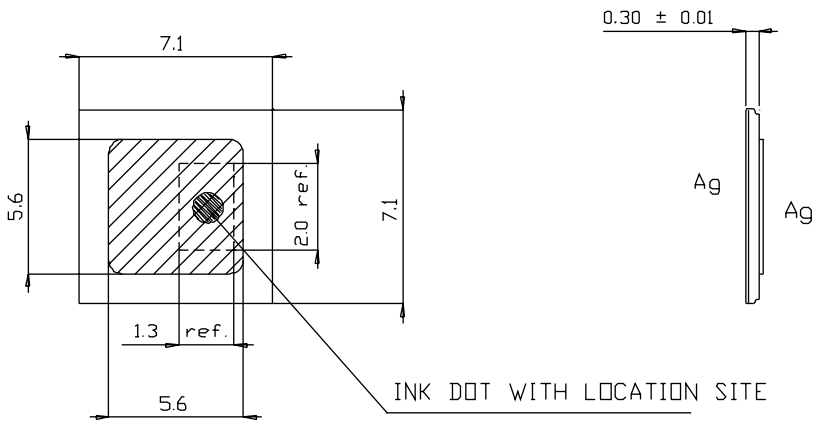
5 - Voltage code: Code x 100 = V_{RRM}

Available Class
06 = 600V
12 = 1200V

6 - Metallization: H = Silver (Anode) - Silver (Cathode)

7 - Probed Uncut Die

Outline Table

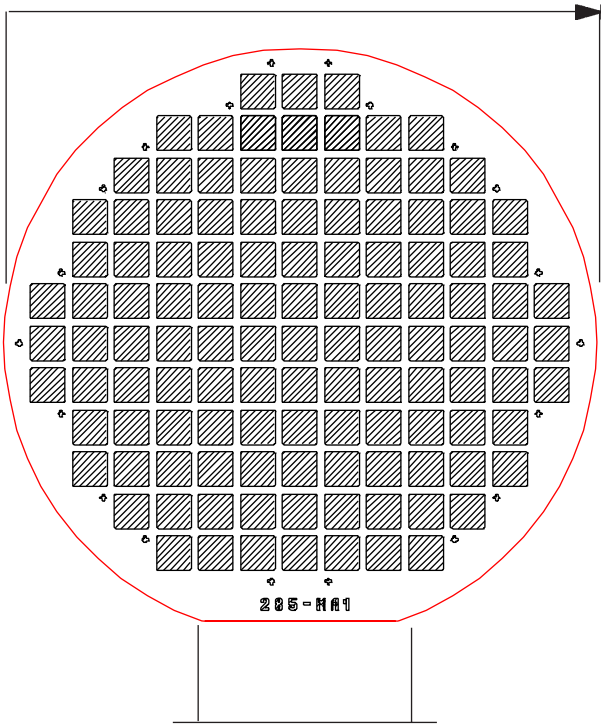


All dimensions are in millimeters

Wafer Layout

TOP VIEW

N° 118 Basic Cells



All dimensions are in millimeters

Bulletin I0136J 05/99

International
IOR Rectifier

IR350DG..HCB SERIES

HIGH POWER RECTIFIER DIODES

- **Junction Size:** **Square 350 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **600 and 1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **T70HF Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	960 mV	T_J = 25°C I_F = 25A
V_{RRM} Reverse Breakdown Voltage Range	600 and 1200 V	T_J = 25°C I_R = 100µA **(1)**

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	350 x 350 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	300 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	350	D	G	12	H	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: D = Standard Recovery Diode

4 - Passivation Process: G = Glassivated MESA

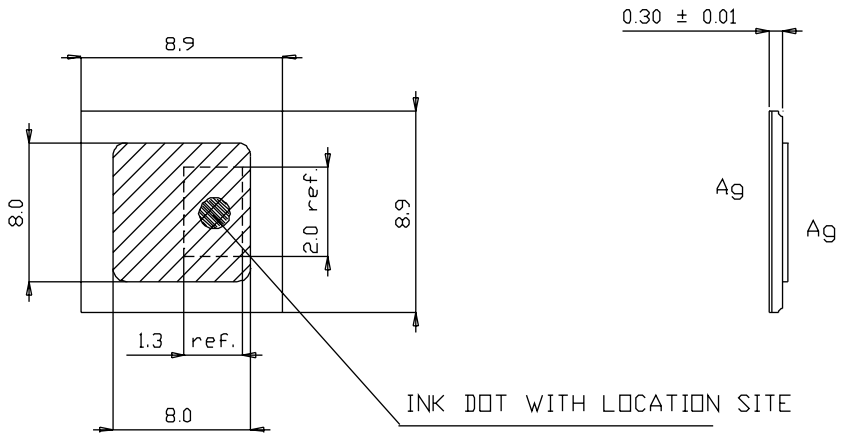
5 - Voltage code: Code x 100 = V_{RRM}

Available Class
06 = 600V
12 = 1200V

6 - Metallization: H = Silver (Anode) - Silver (Cathode)

7 - Probed Uncut Die

Outline Table

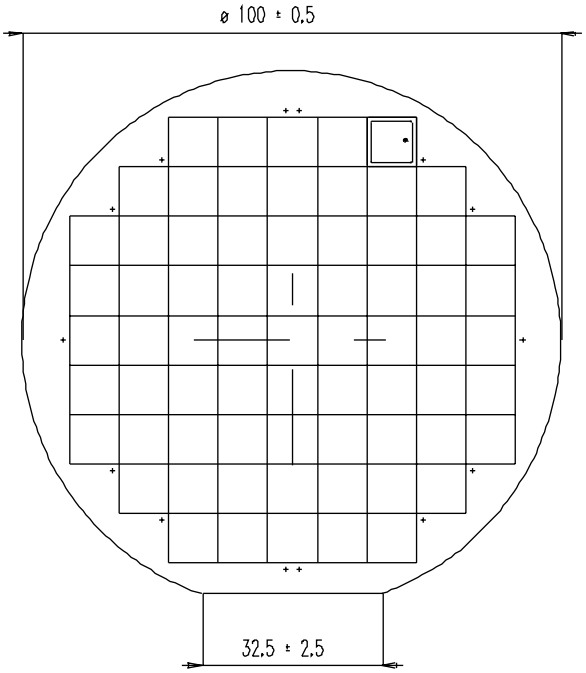


All dimensions are in millimeters

Wafer Layout

TOP VIEW

N° 69 Basic Cells



All dimensions are in millimeters

Bulletin I0123J rev. A 02/97

International
IOR Rectifier

IR350DM..CCB SERIES

STANDARD RECOVERY DIODES

- **Junction Size:** **Square 350 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **800 and 1200 V**
- **Passivation Process:** **Glassivated MOAT**
- **Reference IR Packaged Part:** **IRKD71 Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	960 mV	T_J = 25°C, I_F = 25 A
V_{RRM} Reverse Breakdown Voltage Range	800 and 1200 V	T_J = 25°C, I_{RRM} = 100 µA **(1)**

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20 µm)
Chip Dimensions	350 x 350 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	300 µm, ± 10 µm
Maximum Width of Sawing Line	45 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

IR350DM..CCB Series

Bulletin I0123J rev. A 02/97

Ordering Information Table

Device Code

IR	350	D	M	12	C	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: D = Wire Bondable Standard Recovery Diode

4 - Passivation Process: M = Glassivated MOAT

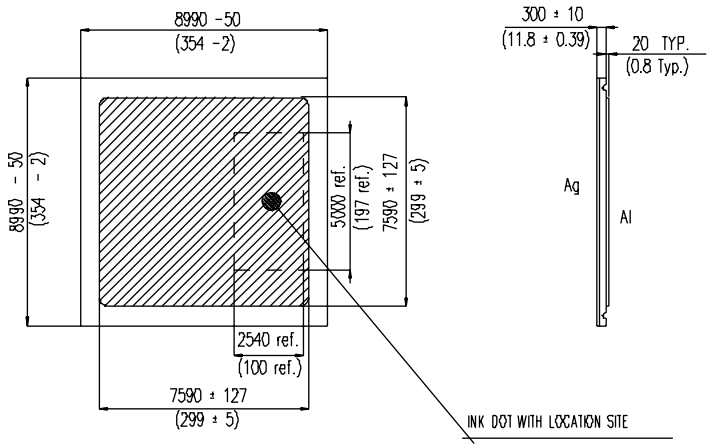
5 - Voltage code: Code x 100 = V_{RRM}

Available Class
08 = 800 V
12 = 1200 V

6 - Metallization: C = Aluminium (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

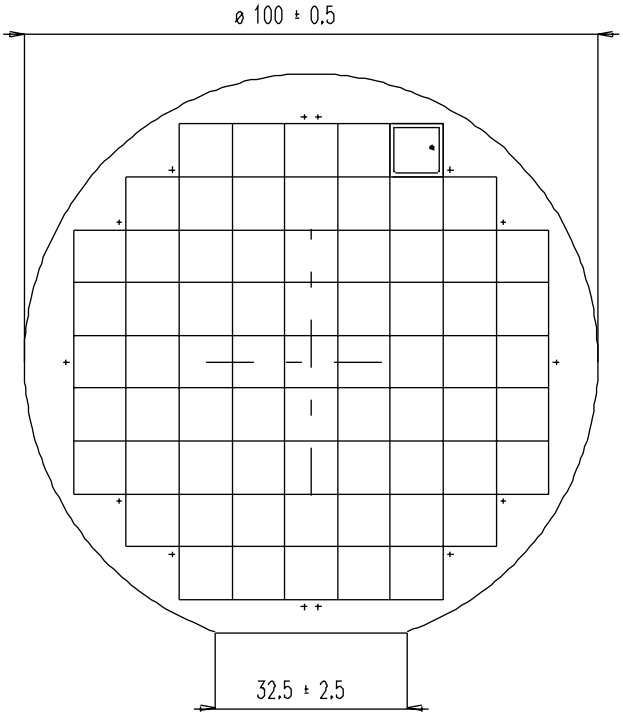


All dimensions are in microns (mils)

Wafer Layout

TOP VIEW

N° 69 Basic Cells



All dimensions are in millimeters

Bulletin I0137J 05/99

International
IOR Rectifier

IR480DG..HCB SERIES

HIGH POWER RECTIFIER DIODES

- **Junction Size:** **Square 480 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **600 and 1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **T110HF Series**

Major Ratings and Characteristics

Parameters	Units	Test Conditions
V_{FM} Maximum Forward Voltage	940 mV	T_J = 25°C I_F = 25A
V_{RRM} Reverse Breakdown Voltage Range	600 and 1200 V	T_J = 25°C I_R = 100µA **(1)**

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	480 x 480 mils (see drawing)
Wafer Diameter	100 mm, with std. < 110 > flat
Wafer Thickness	300 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	480	D	G	12	H	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: D = Standard Recovery Diode

4 - Passivation Process: G = Glassivated MESA

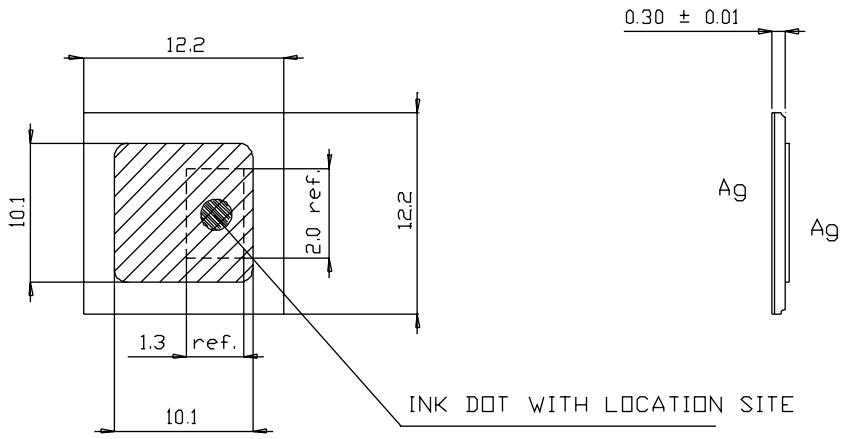
5 - Voltage code: Code x 100 = V_{RRM}

6 - Metallization: H = Silver (Anode) - Silver (Cathode)

7 - Probed Uncut Die

Available Class
06 = 600V
12 = 1200V

Outline Table

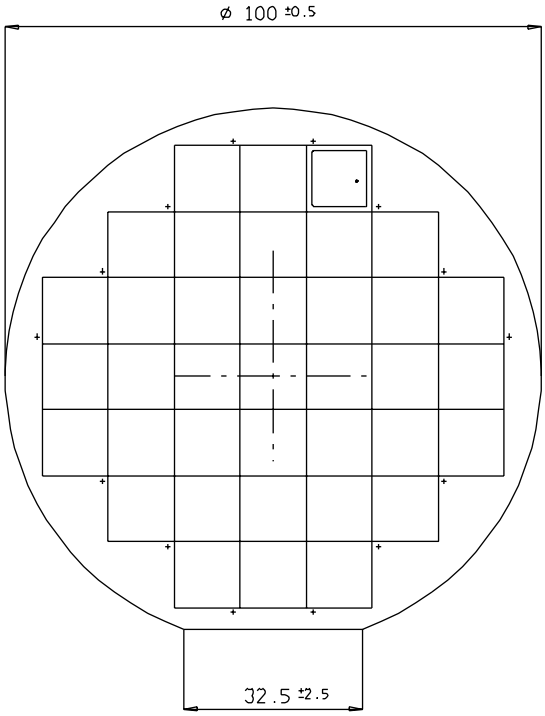


All dimensions are in millimeters

Wafer Layout

TOP VIEW

N° 37 Basic Cells



All dimensions are in millimeters

PD - 93806

International
IOR Rectifier

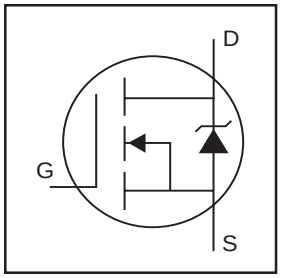
AUTOMOTIVE MOSFET

IRFBA1404P

HEXFET® Power MOSFET

Typical Applications

- Anti-lock Braking Systems (ABS)
- Electric Power Steering (EPS)
- Electric Braking
- Radiator Fan Control



V_{DSS} = 40V

$R_{DS(on)}$ = 3.7mΩ

I_D = 206A⑥

Benefits

- Advanced Process Technology
- Ultra Low On-Resistance
- Increase Current Handling Capability
- 175°C Operating Temperature
- Fast Switching
- Dynamic dv/dt Rating
- Repetitive Avalanche Allowed up to Tjmax

Description

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this MOSFET are a 175ºC junction operating temperature, fast switching speed and improved ruggedness in single and repetitive avalanche. The Super-220 ™ is a package that has been designed to have the same mechanical outline and pinout as the industry standard TO-220 but can house a considerably larger silicon die. The result is significantly increased current handling capability over both the TO-220 and the much larger TO-247 package. The combination of extremely low on-resistance silicon and the Super-220 ™ package makes it ideal to reduce the component count in multiparalled TO-220 applications, reduce system power dissipation, upgrade existing designs or have TO-247 performance in a TO-220 outline. This package has been designed to meet automotive, Q101, qualification standard.

These benefits make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



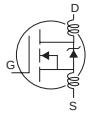
Super-220™

Absolute Maximum Ratings

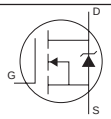
	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	206⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	145⑥	
I_{DM}	Pulsed Drain Current ①	650	
P_D @T_C = 25°C	Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	See Fig.12a, 12b, 15, 16	mJ
I_{AR}	Avalanche Current①		A
E_{AR}	Repetitive Avalanche Energy①	30	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-40 to + 175	°C
T_{STG}	Storage Temperature Range	-55 to + 175	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Recommended clip force	20	N

10/24/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.036	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	3.7	mΩ	V_{GS} = 10V, I_D = 95A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = 10V, I_D = 250µA
g_{fs}	Forward Transconductance	106	—	—	S	V_{DS} = 25V, I_D = 60A
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 40V, V_{GS} = 0V
		—	—	250		V_{DS} = 32V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V
Q_g	Total Gate Charge	—	160	200	nC	I_D = 95A
Q_{gs}	Gate-to-Source Charge	—	35	—		V_{DS} = 32V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	42	60		V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	V_{DD} = 20V
t_r	Rise Time	—	140	—		I_D = 95A
$t_{d(off)}$	Turn-Off Delay Time	—	72	—		R_G = 2.5Ω
t_f	Fall Time	—	26	—		R_D = 0.21Ω ④
L_D	Internal Drain Inductance	—	2.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	5.0	—		
C_{iss}	Input Capacitance	—	7360	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1680	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	240	—		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	6630	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	1490	—		V_{GS} = 0V, V_{DS} = 32V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	—	1540	—		V_{GS} = 0V, V_{DS} = 0V to 32V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	206⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	650		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 95A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	71	110	ns	T_J = 25°C, I_F = 95A
Q_{rr}	Reverse Recovery Charge	—	180	270	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.50	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient	—	58	

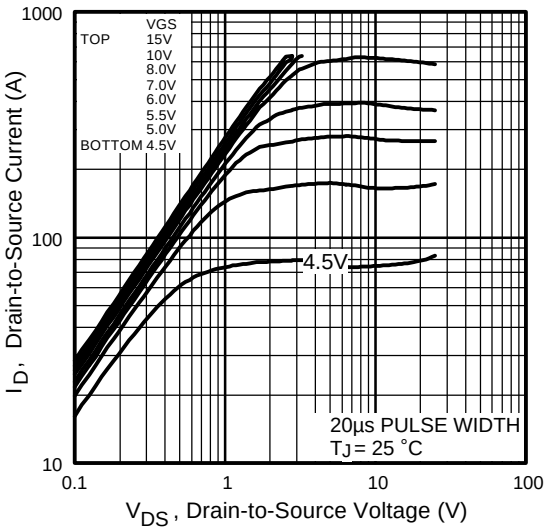


Fig 1. Typical Output Characteristics

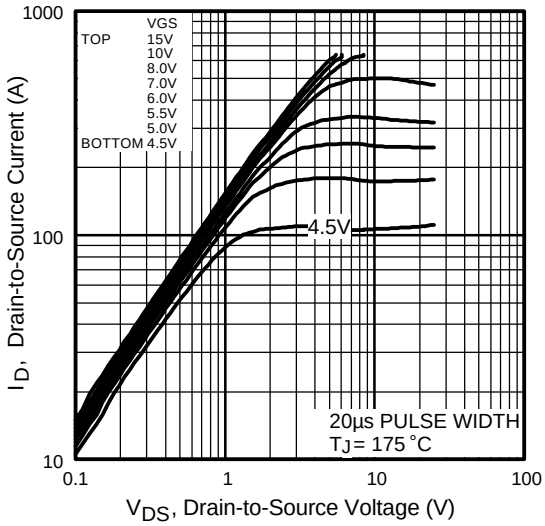


Fig 2. Typical Output Characteristics

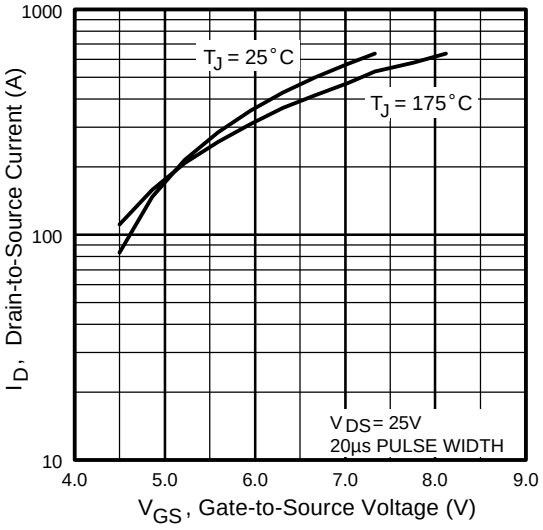


Fig 3. Typical Transfer Characteristics

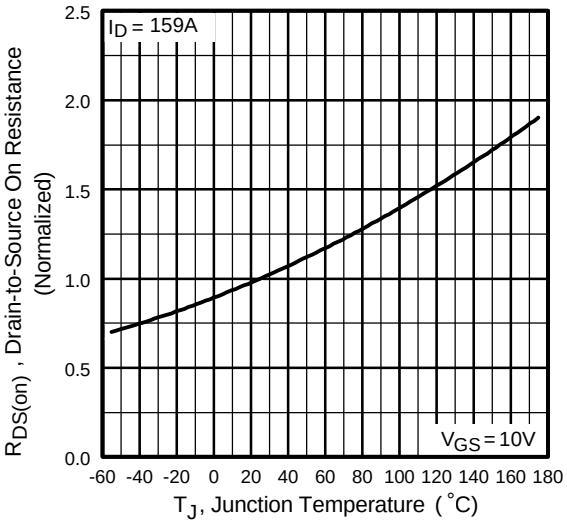


Fig 4. Normalized On-Resistance Vs. Temperature

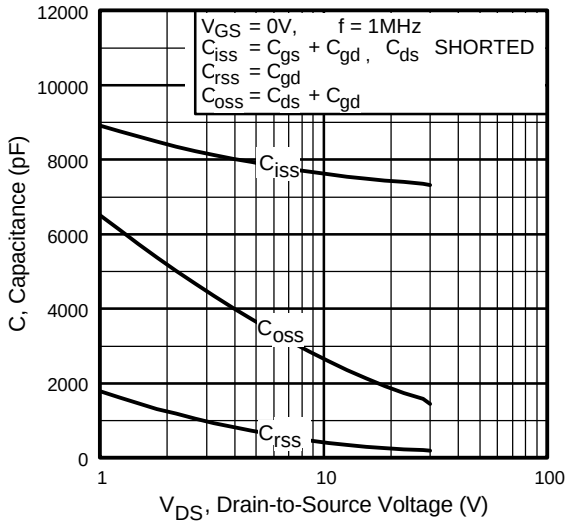


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

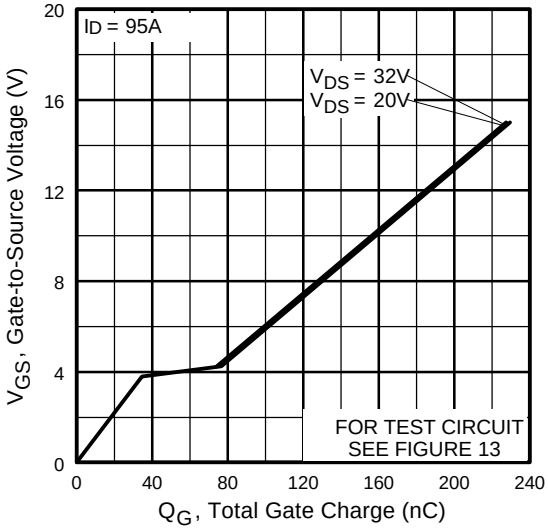


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

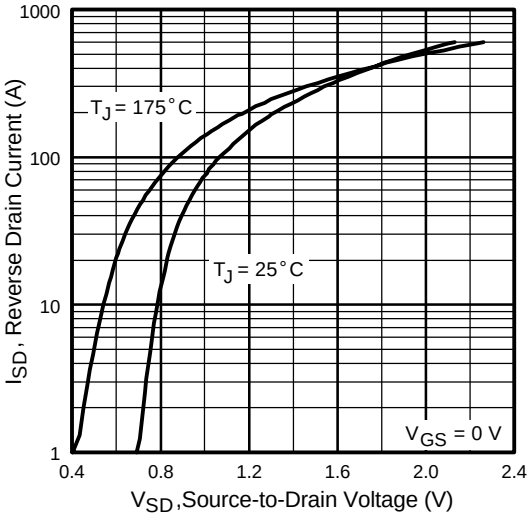


Fig 7. Typical Source-Drain Diode Forward Voltage

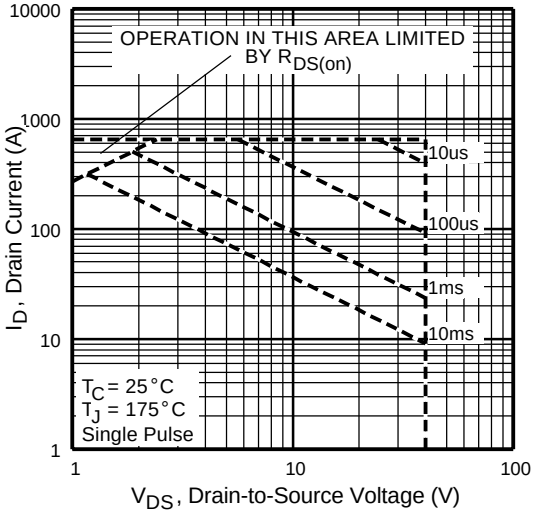


Fig 8. Maximum Safe Operating Area

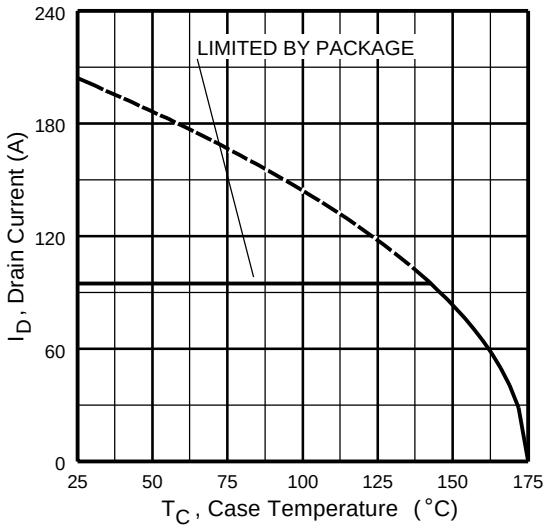


Fig 9. Maximum Drain Current Vs. Case Temperature

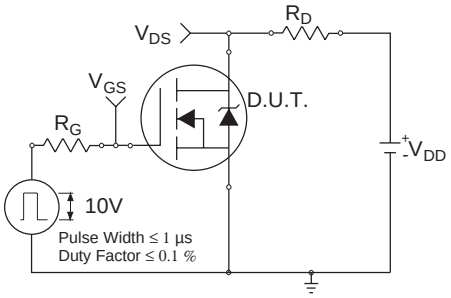


Fig 10a. Switching Time Test Circuit

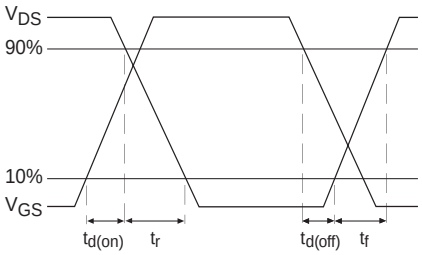


Fig 10b. Switching Time Waveforms

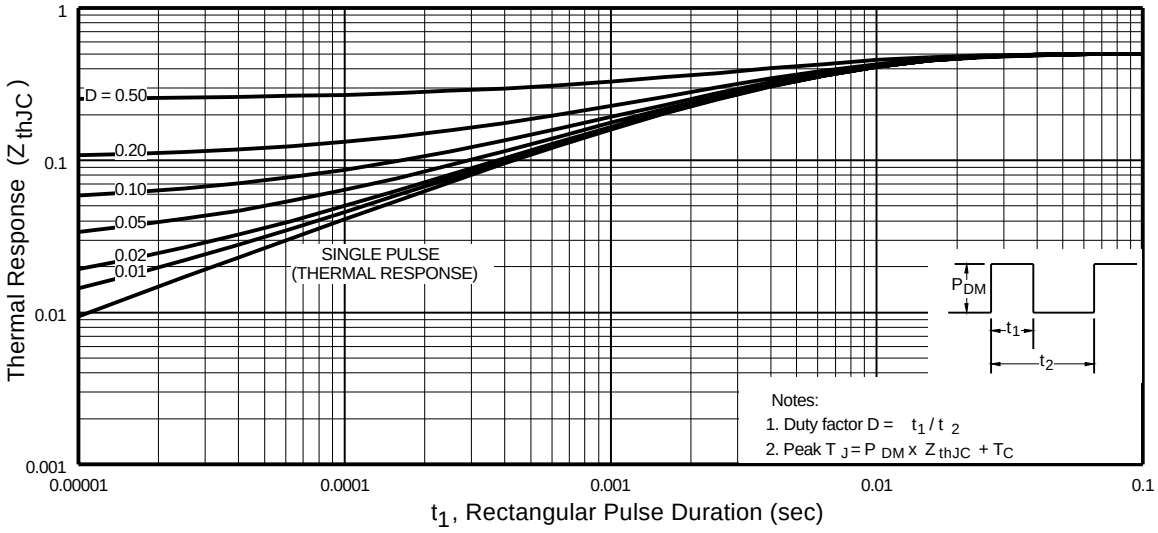


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

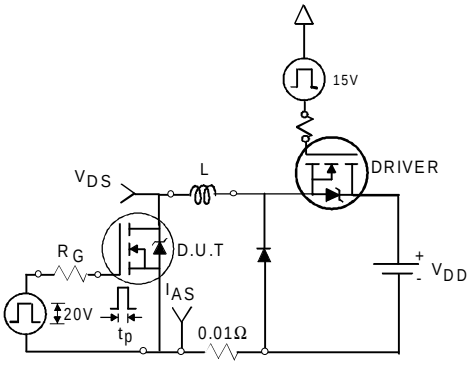


Fig 12a. Unclamped Inductive Test Circuit

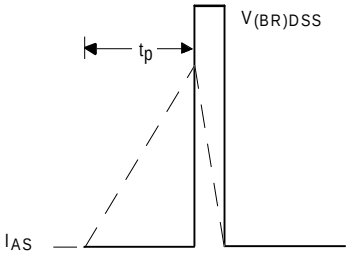


Fig 12b. Unclamped Inductive Waveforms

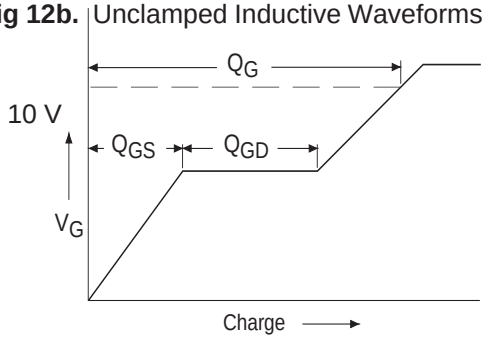


Fig 13a. Basic Gate Charge Waveform

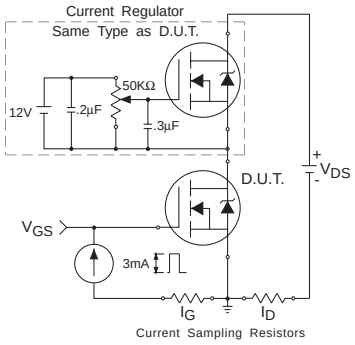


Fig 13b. Gate Charge Test Circuit

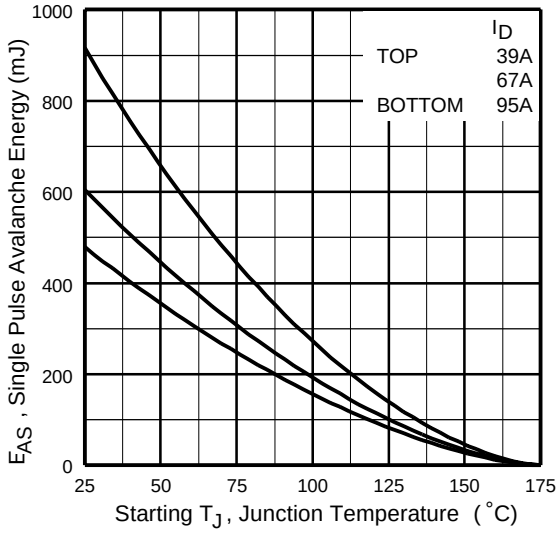


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

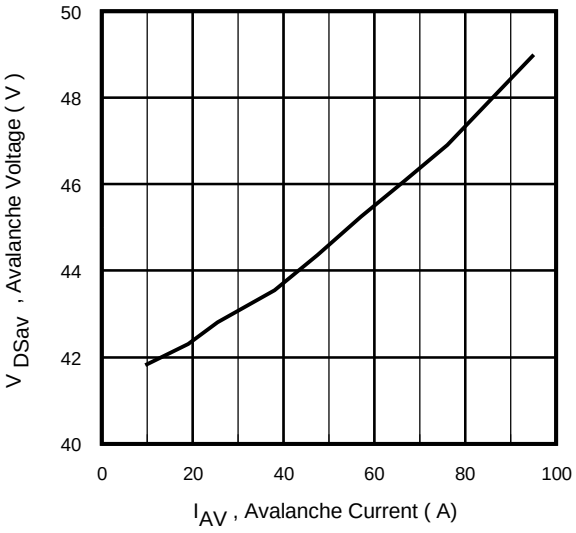


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

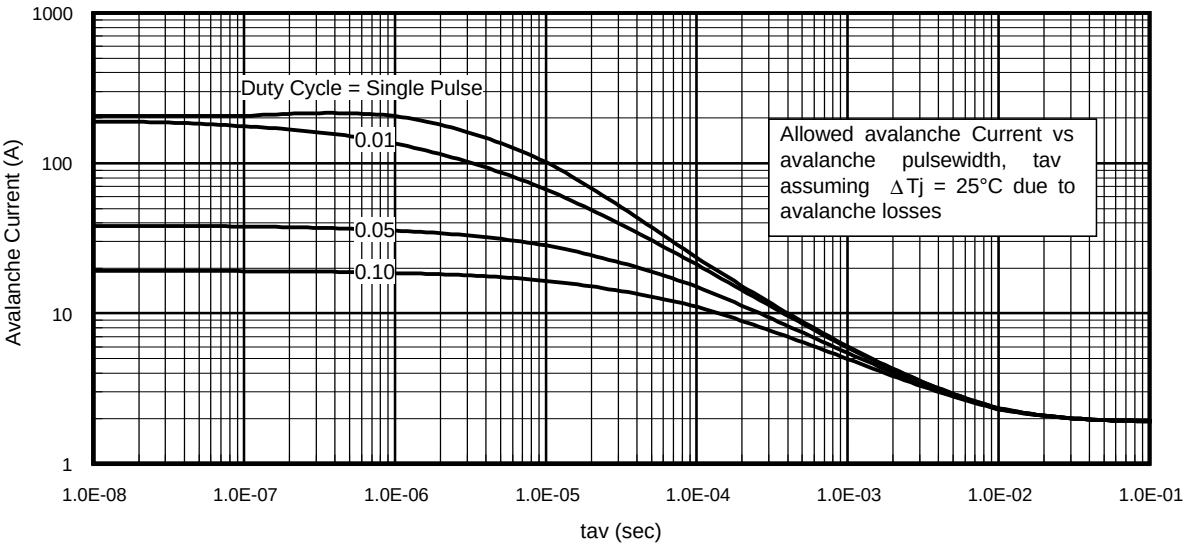


Fig 15. Typical Avalanche Current Vs.Pulsewidth

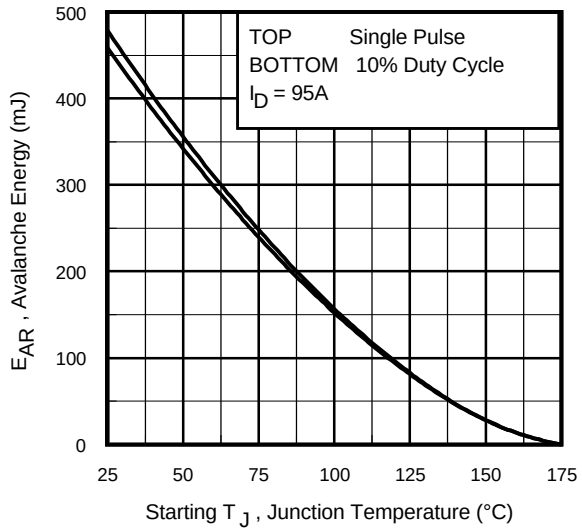


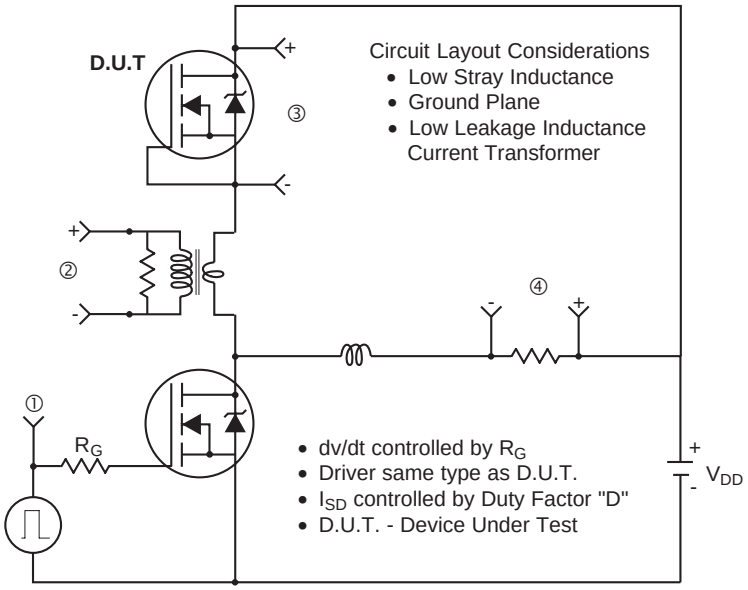
Fig 16. Maximum Avalanche Energy Vs. Temperature

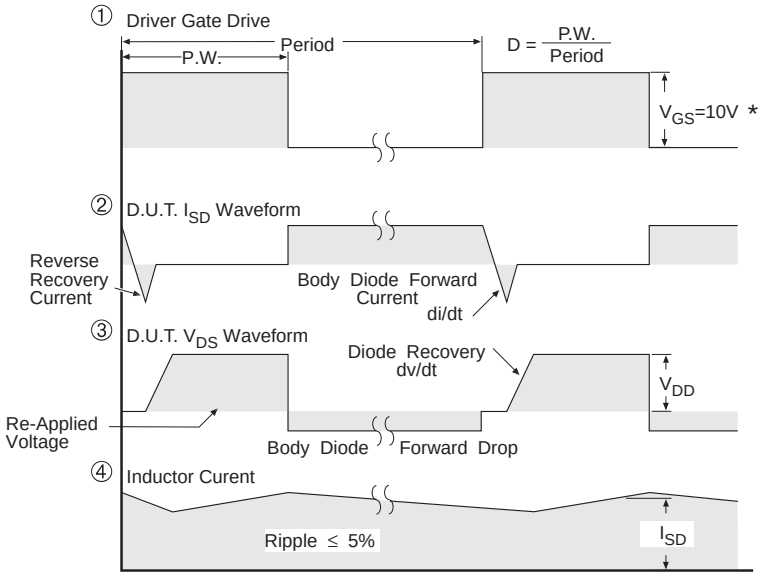
Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

Peak Diode Recovery dv/dt Test Circuit

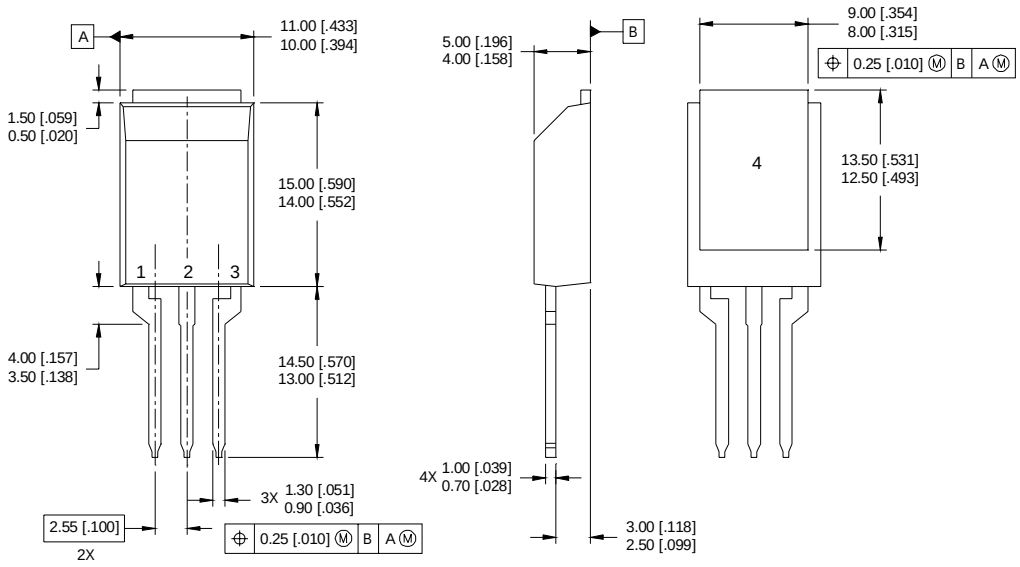




* V_{GS} = 5V for Logic Level Devices

Fig 17. For N-Channel HEXFET® Power MOSFETs

Super-220™ Package Outline



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-273AA.

LEAD ASSIGNMENTS

MOSFET	IGBT
1 - GATE	1 - GATE
2 - DRAIN	2 - COLLECTOR
3 - SOURCE	3 - EMITTER
4 - DRAIN	4 - COLLECTOR

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 0.12mH R_G = 25Ω, I_{AS} = 95A.

③ $I_{SD} \leq$ 95A, di/dt ≤ 150A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} . Refer to AN-1001

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 95A.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 10/00

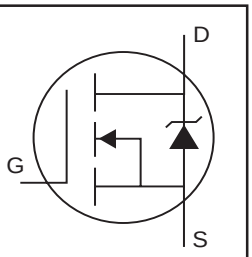
International
IOR Rectifier

PD -91896E

IRF1404

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 40V

$R_{DS(on)}$ = 0.004Ω

I_D = 162A⑥



TO-220AB

Description

Seventh Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	162⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	115⑥	
I_{DM}	Pulsed Drain Current ①	650	
P_D @T_C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	519	mJ
I_{AR}	Avalanche Current①	95	A
E_{AR}	Repetitive Avalanche Energy①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range	-55 to + 175	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

10/20/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.036	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.0035	0.004	Ω	V_{GS} = 10V, I_D = 95A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = 10V, I_D = 250µA
g_{fs}	Forward Transconductance	106	—	—	S	V_{DS} = 25V, I_D = 60A
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 40V, V_{GS} = 0V
		—	—	250		V_{DS} = 32V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V
Q_g	Total Gate Charge	—	160	200	nC	I_D = 95A
Q_{gs}	Gate-to-Source Charge	—	35	—		V_{DS} = 32V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	42	60		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	V_{DD} = 20V
t_r	Rise Time	—	140	—		I_D = 95A
$t_{d(off)}$	Turn-Off Delay Time	—	72	—		R_G = 2.5Ω
t_f	Fall Time	—	26	—		R_D = 0.21Ω ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	7360	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1680	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	240	—		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	6630	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	1490	—		V_{GS} = 0V, V_{DS} = 32V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	—	1540	—		V_{GS} = 0V, V_{DS} = 0V to 32V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	162⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	650		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 95A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	71	110	ns	T_J = 25°C, I_F = 95A
Q_{rr}	Reverse RecoveryCharge	—	180	270	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 0.12mH R_G = 25Ω, I_{AS} = 95A. (See Figure 12)

③ I_{SD} ≤ 95A, di/dt ≤ 150A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A

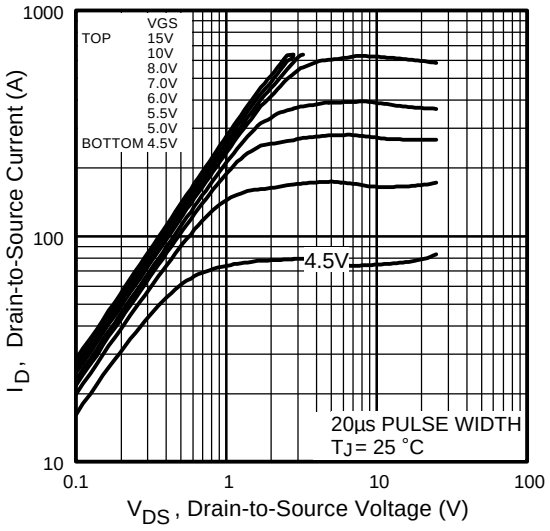


Fig 1. Typical Output Characteristics

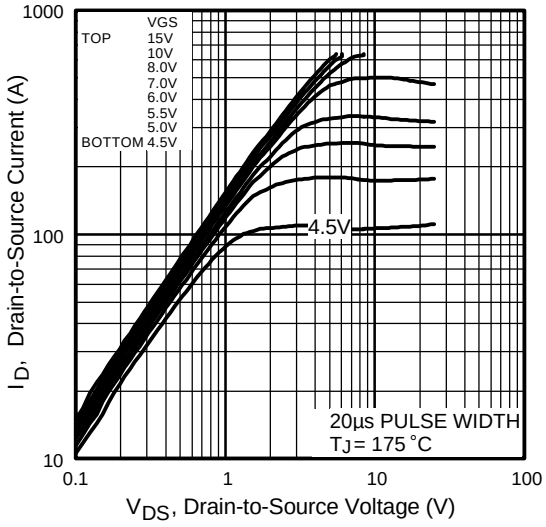


Fig 2. Typical Output Characteristics

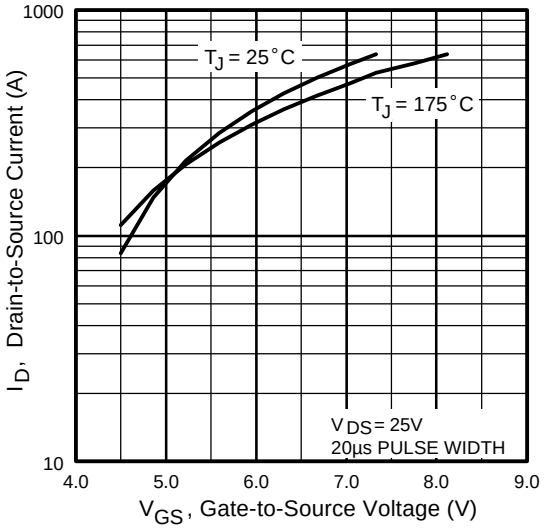


Fig 3. Typical Transfer Characteristics

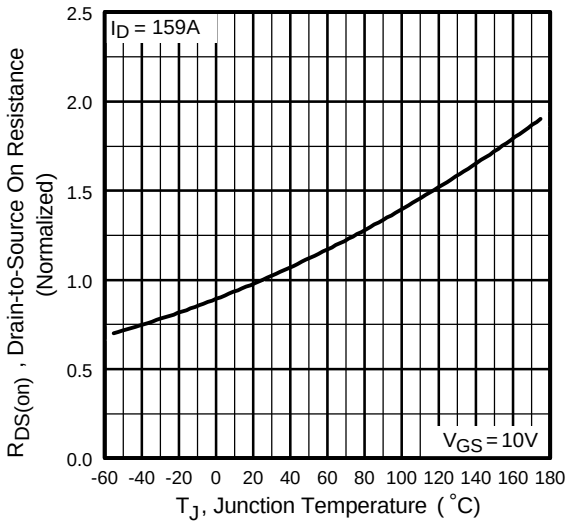


Fig 4. Normalized On-Resistance Vs. Temperature

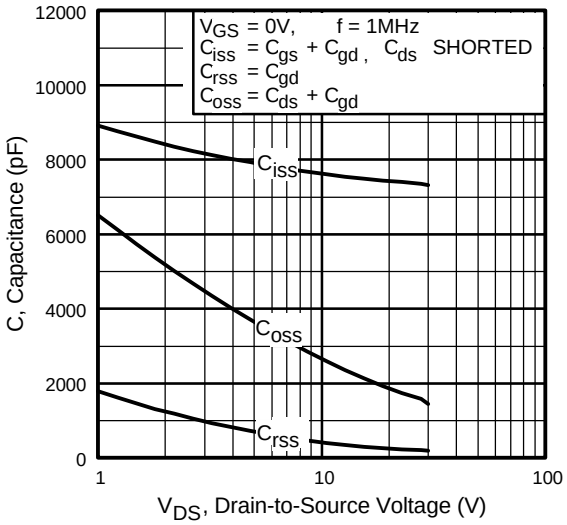


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

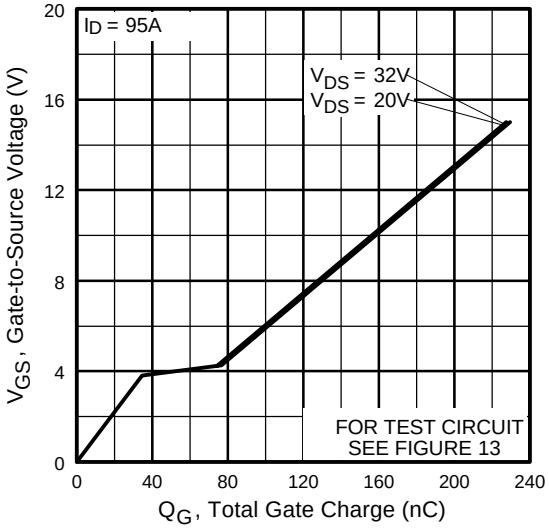


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

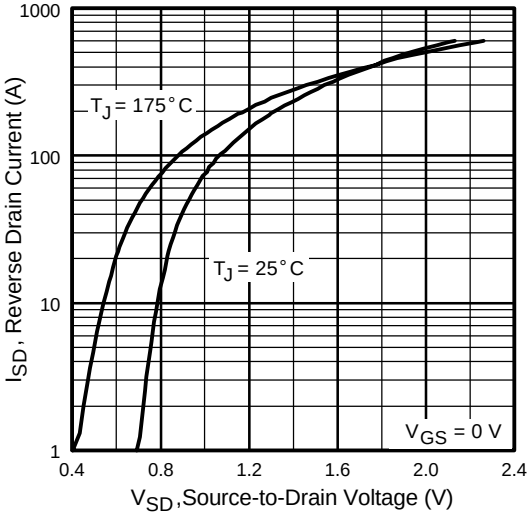


Fig 7. Typical Source-Drain Diode Forward Voltage

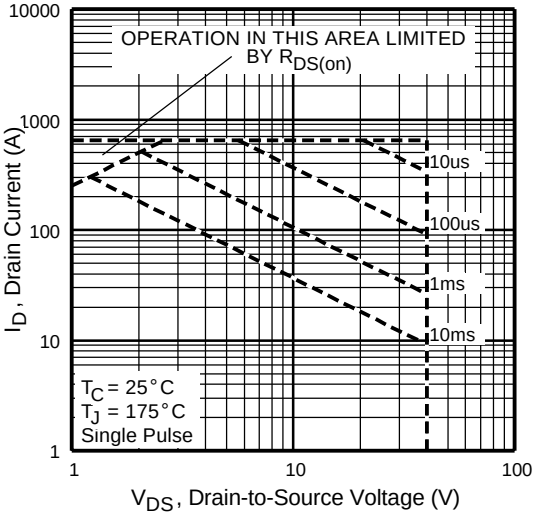


Fig 8. Maximum Safe Operating Area

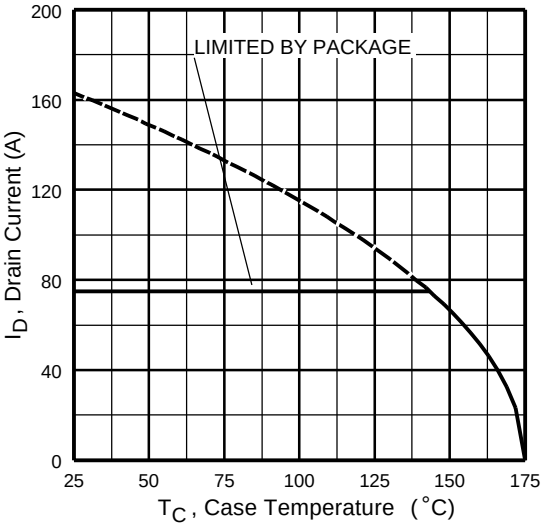


Fig 9. Maximum Drain Current Vs. Case Temperature

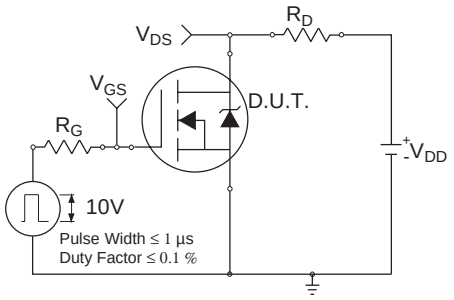


Fig 10a. Switching Time Test Circuit

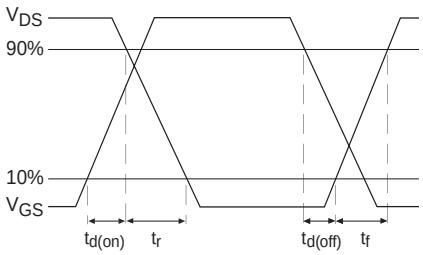


Fig 10b. Switching Time Waveforms

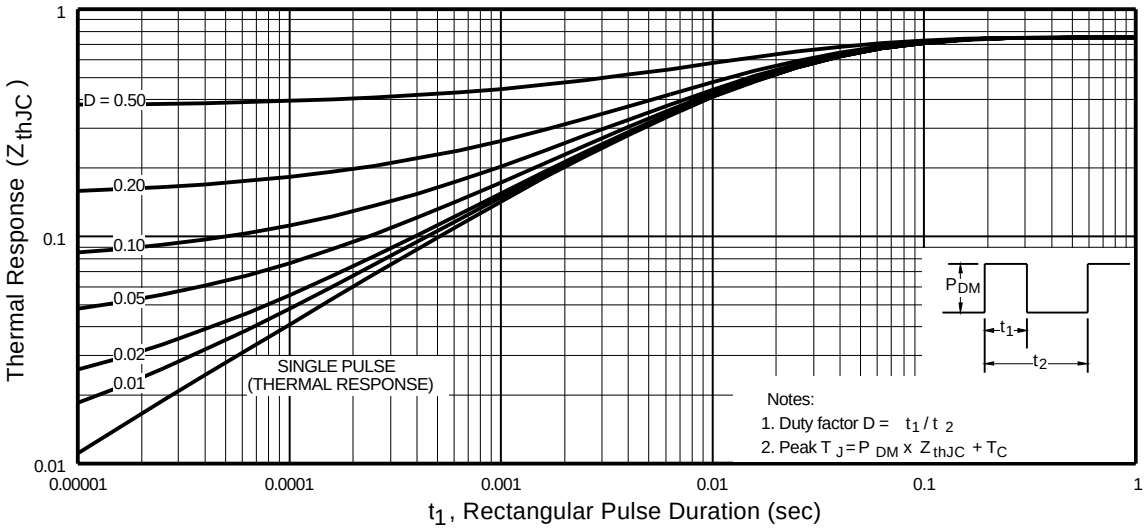


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

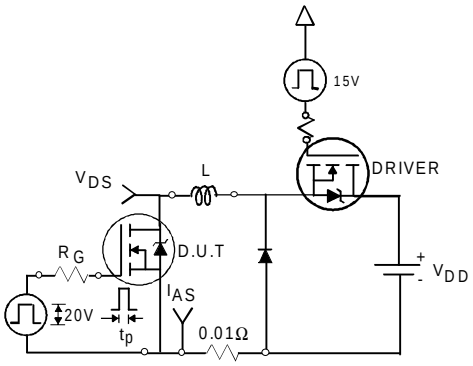


Fig 12a. Unclamped Inductive Test Circuit

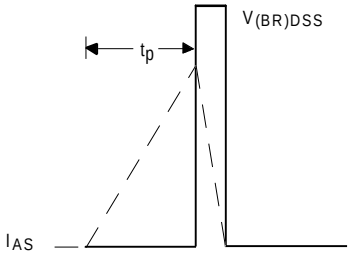


Fig 12b. Unclamped Inductive Waveforms

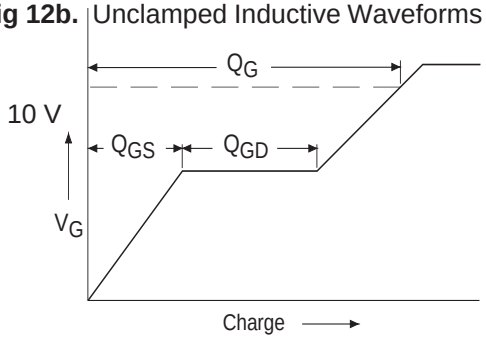


Fig 13a. Basic Gate Charge Waveform

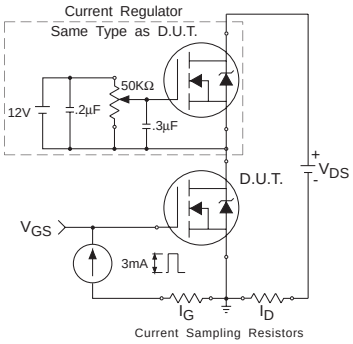


Fig 13b. Gate Charge Test Circuit

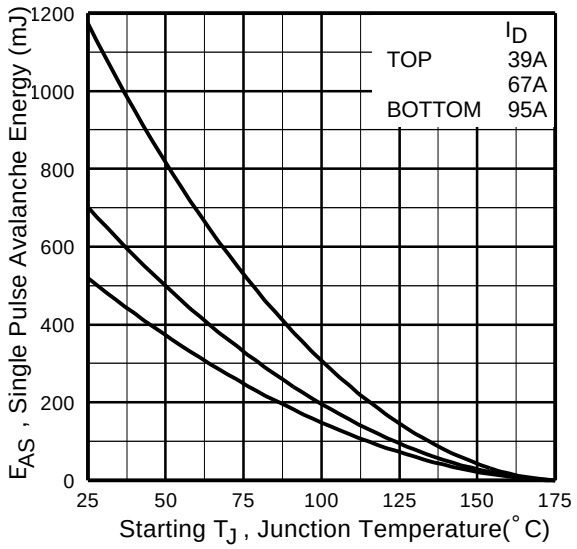


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

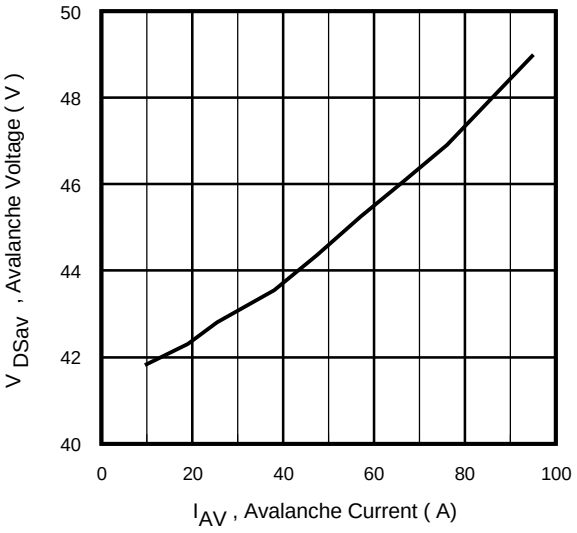
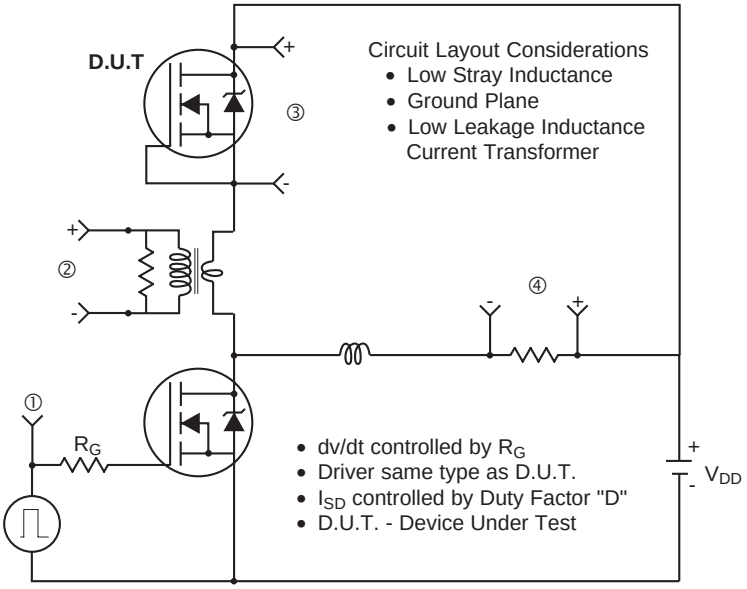
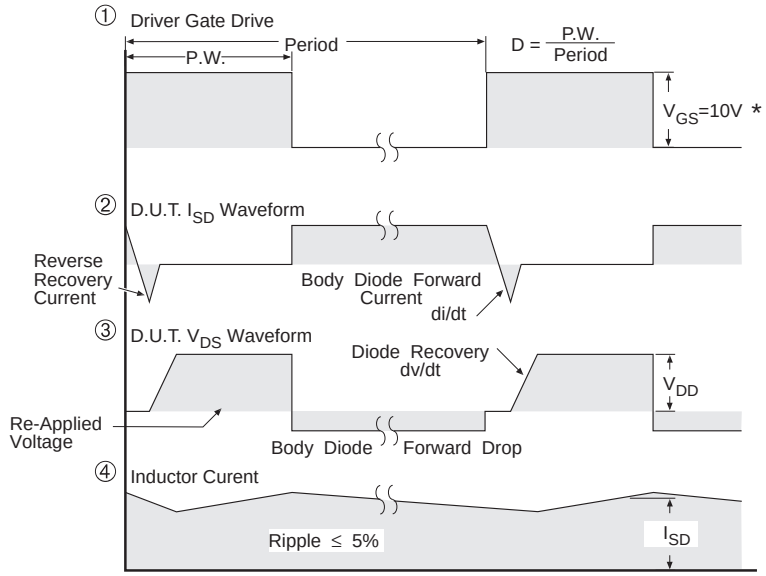


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

Peak Diode Recovery dv/dt Test Circuit



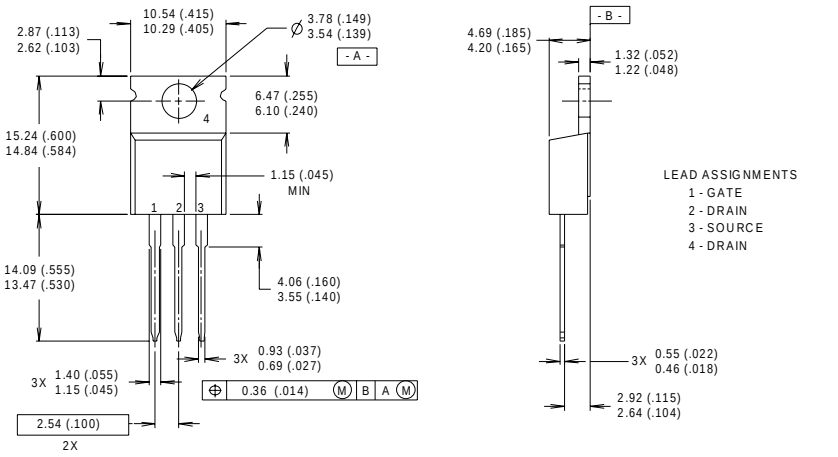


* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-channel HEXFET® Power MOSFETs

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

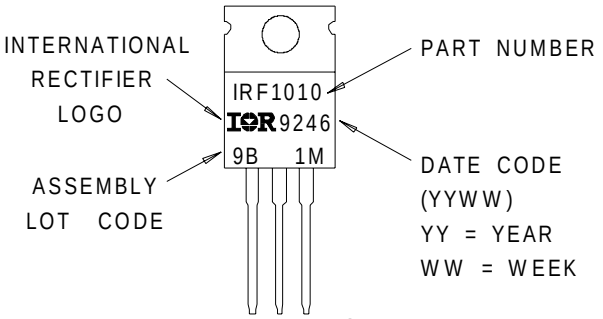


NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

Data and specifications subject to change without notice. 10/00

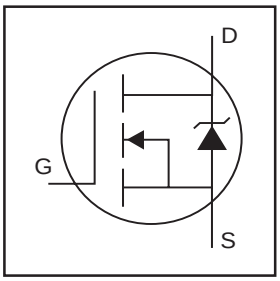
International
IOR Rectifier

PD-93853C

IRF1404S
IRF1404L

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 40V

$R_{DS(on)}$ = 0.004Ω

I_D = 162A⑥



D^2Pak
IRF1404S

TO-262
IRF1404L

Description

Seventh Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D^2Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D^2Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.
The through-hole version (IRF1404L) is available for low-profile applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V⑦	162⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V⑦	115⑥	
I_{DM}	Pulsed Drain Current ①⑦	650	
P_D @T_A = 25°C	Power Dissipation	3.8	W
P_D @T_C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy⑦	519	mJ
I_{AR}	Avalanche Current①	95	A
E_{AR}	Repetitive Avalanche Energy①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑦	5.0	V/ns
T_J	Operating Junction and	-55 to +175	°C
T_{STG}	Storage Temperature Range	-55 to +175	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

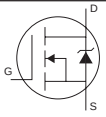
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mounted, steady-state)*	——	40	

5/18/01

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.036	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	0.0035	0.004	Ω	V_{GS} = 10V, I_D = 95A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = 10V, I_D = 250µA
g_{fs}	Forward Transconductance	106	——	——	S	V_{DS} = 25V, I_D = 60A⑦
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	µA	V_{DS} = 40V, V_{GS} = 0V
		——	——	250		V_{DS} = 32V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V
Q_g	Total Gate Charge	——	160	200	nC	I_D = 95A
Q_{gs}	Gate-to-Source Charge	——	35	——		V_{DS} = 32V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	42	60		V_{GS} = 10V ④⑦
$t_{d(on)}$	Turn-On Delay Time	——	17	——	ns	V_{DD} = 20V
t_r	Rise Time	——	140	——		I_D = 95A
$t_{d(off)}$	Turn-Off Delay Time	——	72	——		R_G = 2.5Ω
t_f	Fall Time	——	26	——		R_D = 0.21Ω ④⑦
L_S	Internal Source Inductance	——	7.5	——	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	——	7360	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	1680	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	240	——		f = 1.0MHz, See Fig. 5 ⑦
C_{oss}	Output Capacitance	——	6630	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	——	1490	——		V_{GS} = 0V, V_{DS} = 32V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤⑦	——	1540	——		V_{GS} = 0V, V_{DS} = 0V to 32V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	162⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	650		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 95A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	71	110	ns	T_J = 25°C, I_F = 95A
Q_{rr}	Reverse RecoveryCharge	——	180	270	nC	di/dt = 100A/µs ④⑦
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 0.12mH R_G = 25Ω, I_{AS} = 95A. (See Figure 12)

③ I_{SD} ≤ 95A, di/dt ≤ 150A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A

⑦ Use IRF1404 data and test conditions.

* When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

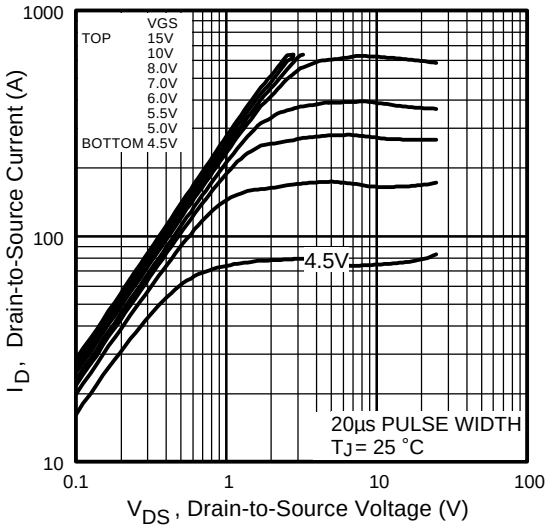


Fig 1. Typical Output Characteristics

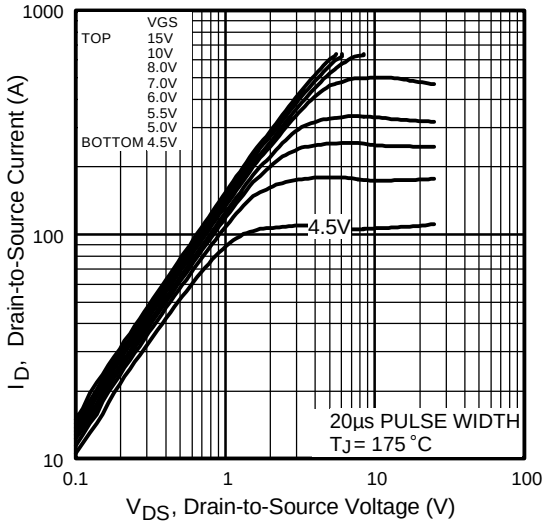


Fig 2. Typical Output Characteristics

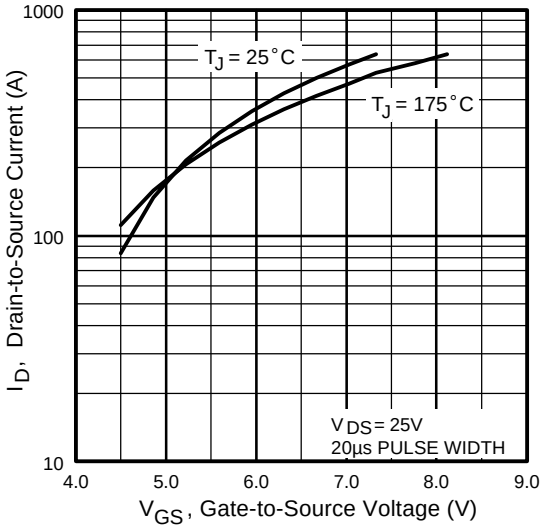


Fig 3. Typical Transfer Characteristics

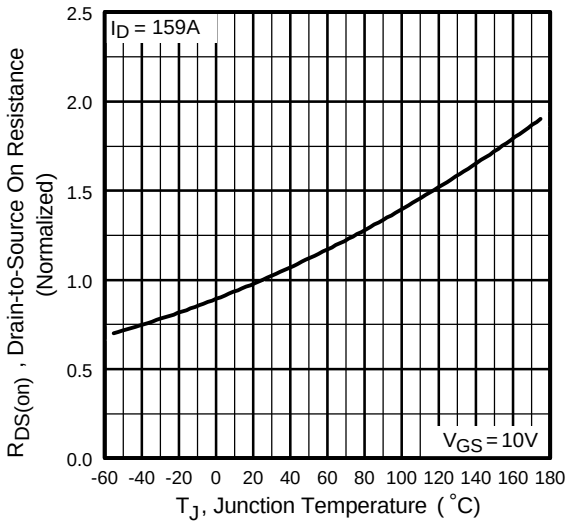


Fig 4. Normalized On-Resistance Vs. Temperature

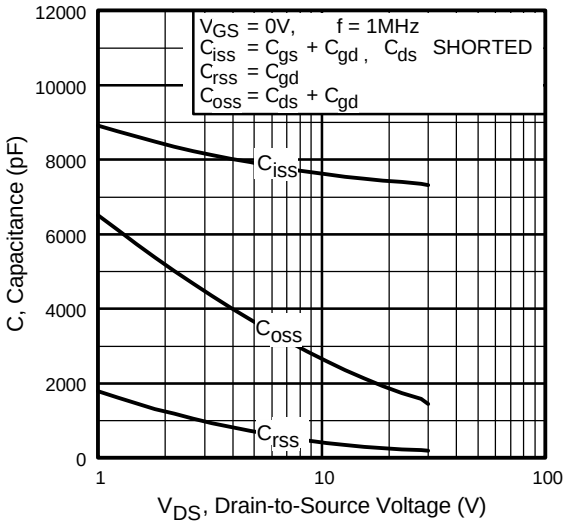


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

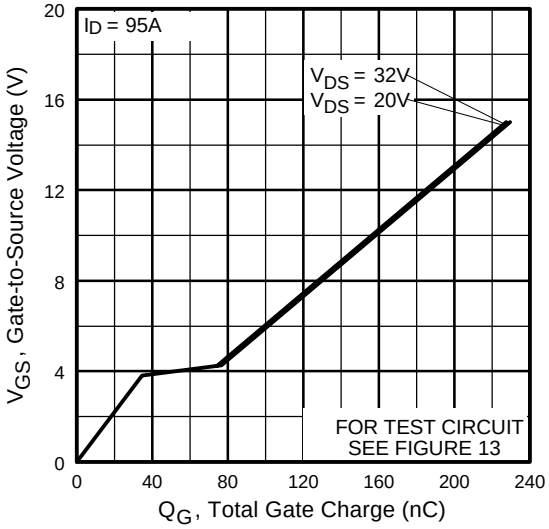


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

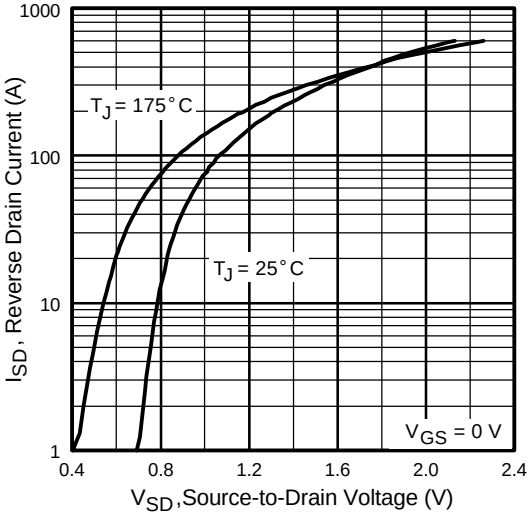


Fig 7. Typical Source-Drain Diode Forward Voltage

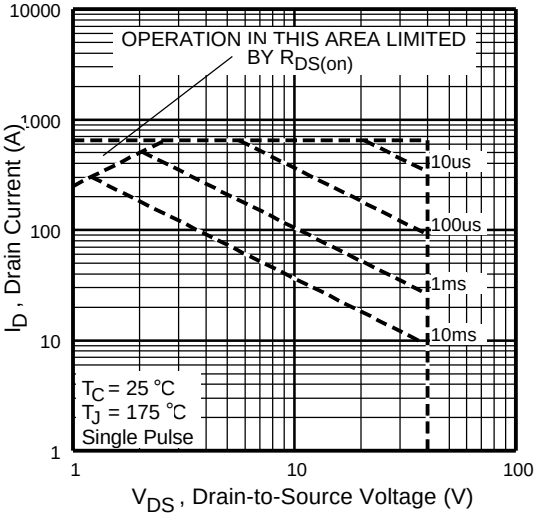


Fig 8. Maximum Safe Operating Area

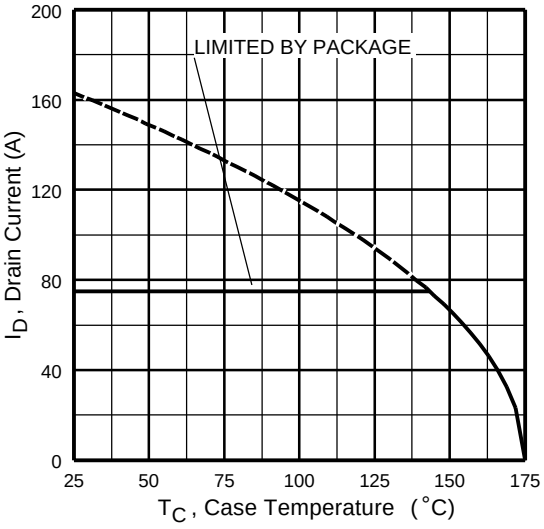


Fig 9. Maximum Drain Current Vs. Case Temperature

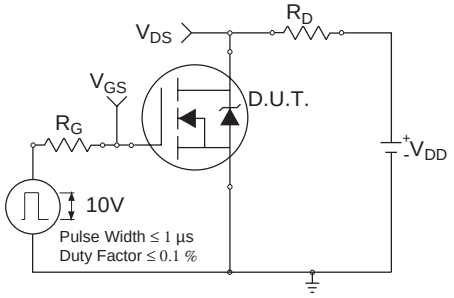


Fig 10a. Switching Time Test Circuit

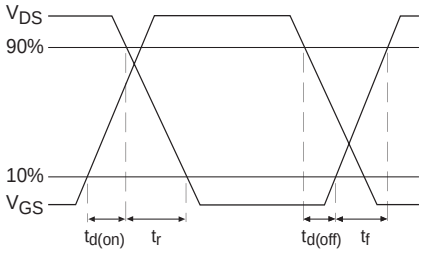


Fig 10b. Switching Time Waveforms

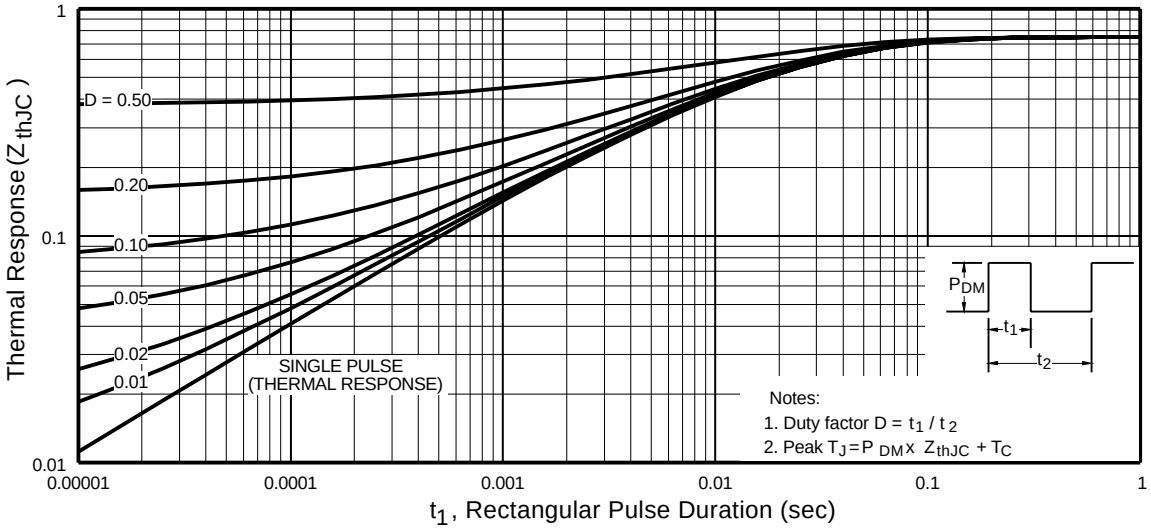


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

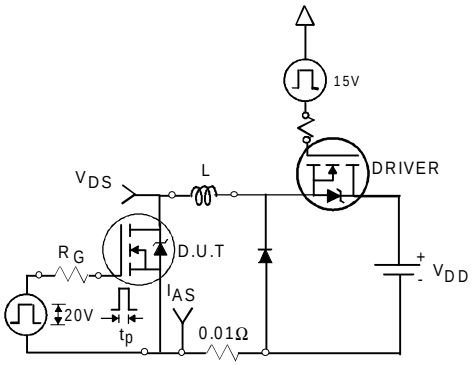


Fig 12a. Unclamped Inductive Test Circuit

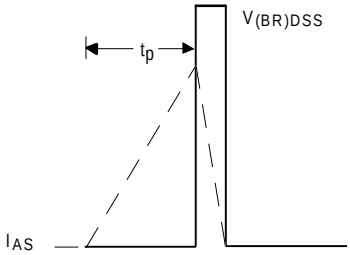


Fig 12b. Unclamped Inductive Waveforms

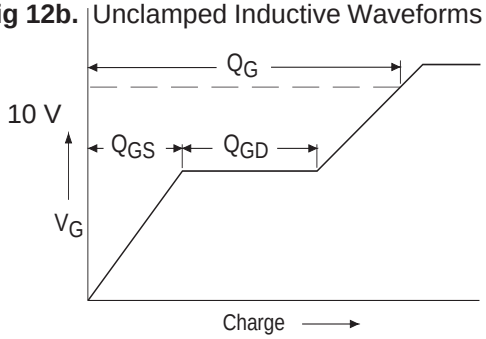


Fig 13a. Basic Gate Charge Waveform

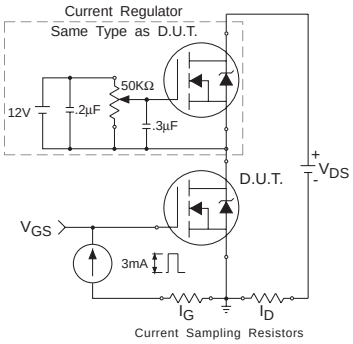


Fig 13b. Gate Charge Test Circuit

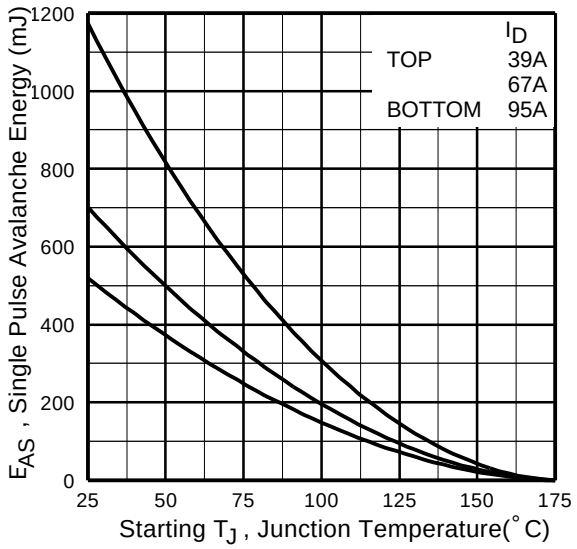


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

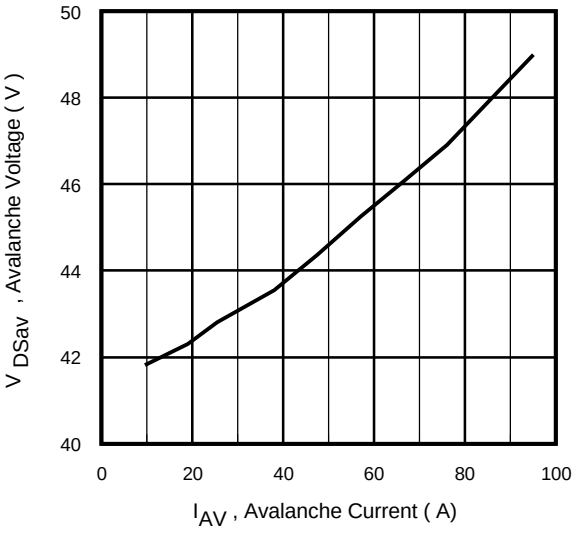
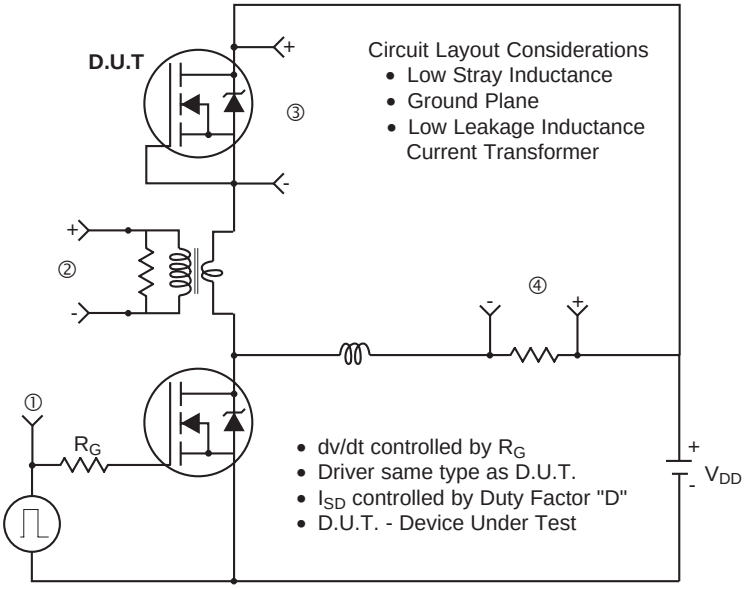
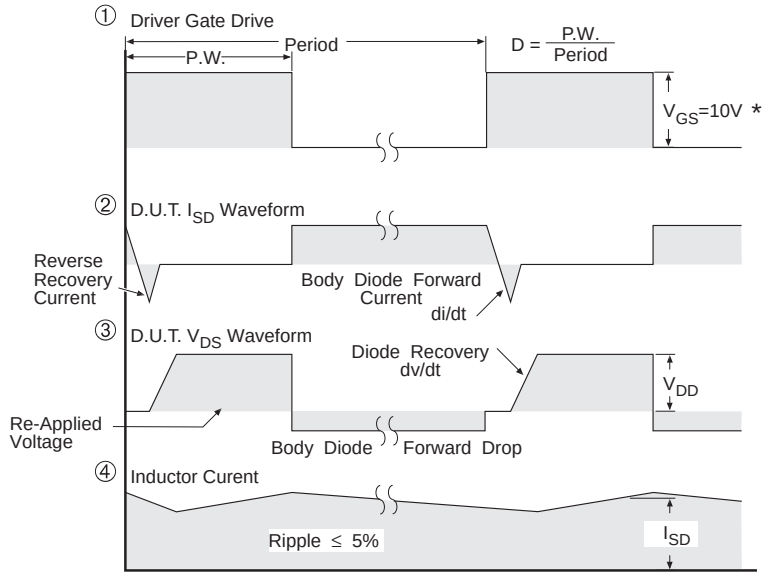


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

Peak Diode Recovery dv/dt Test Circuit

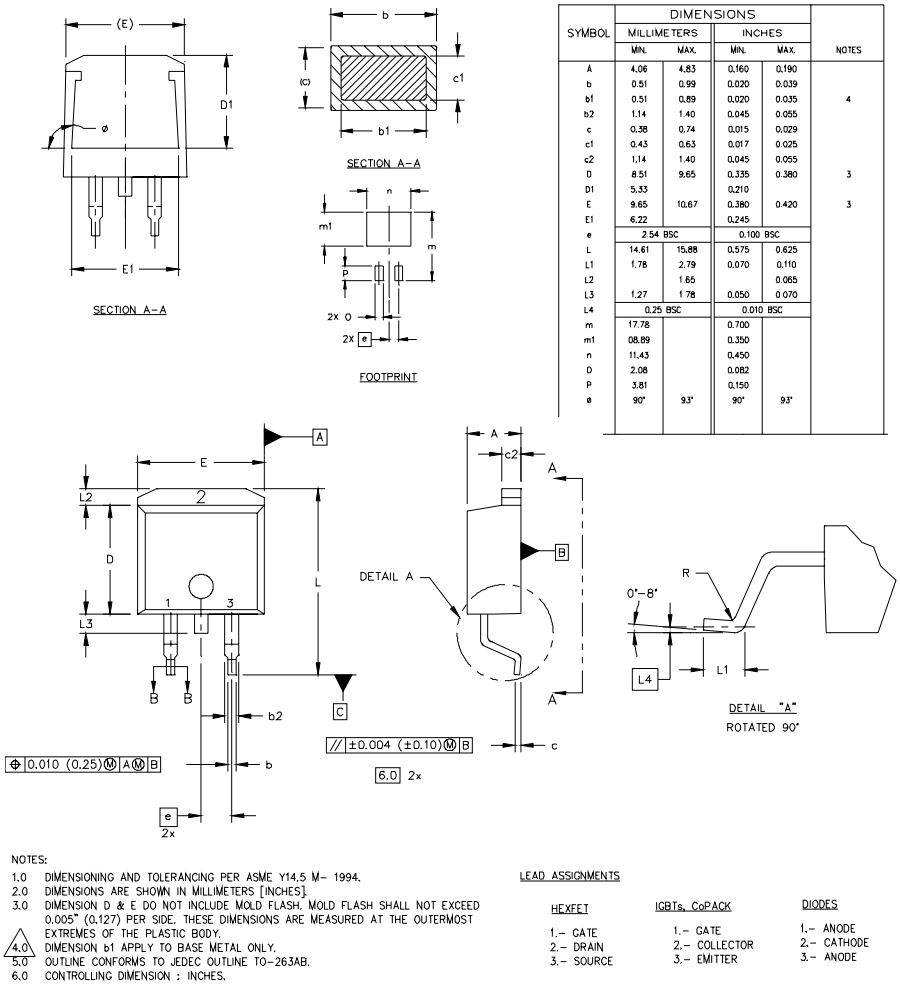




* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-channel HEXFET® Power MOSFETs

D²Pak Package Outline



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	0.160	0.190	
b	0.51	0.99	0.020	0.039	
b1	0.51	0.89	0.020	0.035	4
b2	1.14	1.40	0.045	0.055	
c	0.38	0.74	0.015	0.029	
c1	0.43	0.63	0.017	0.025	
c2	1.14	1.40	0.045	0.055	
D	8.51	9.65	0.335	0.380	3
D1	5.33		0.210		
E	9.65	10.67	0.380	0.420	3
E1	6.22		0.245		
e	2.54 BSC		0.100 BSC		
L	14.61	15.88	0.575	0.625	
L1	1.78	2.79	0.070	0.110	
L2		1.65		0.065	
L3	1.27	1.78	0.050	0.070	
L4	0.25 BSC		0.010 BSC		
m	17.78		0.700		
m1	08.89		0.350		
n	11.43		0.450		
Q	2.08		0.082		
P	3.81		0.150		
ø	90°	93°	90°	93°	

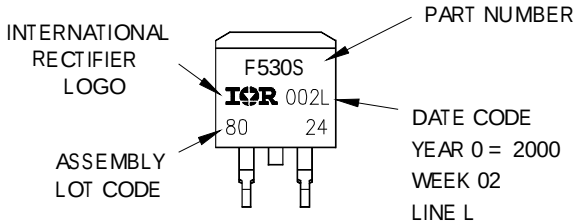
NOTES:
1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M– 1994.
2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
4.0 DIMENSION b1 APPLY TO BASE METAL ONLY.
5.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO–263AB.
6.0 CONTROLLING DIMENSION : INCHES.

LEAD ASSIGNMENTS

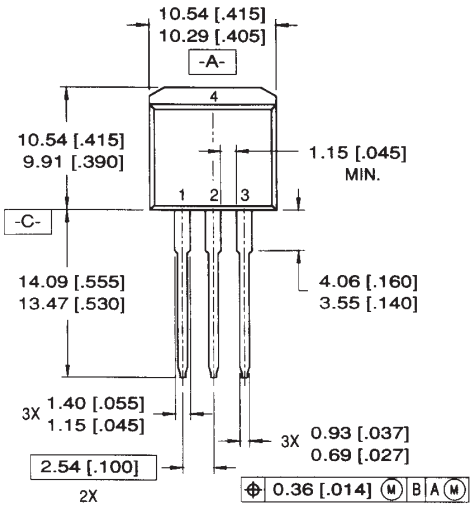
HEXFET	IGBTs, CoPACK	DIODES
1.– GATE	1.– GATE	1.– ANODE
2.– DRAIN	2.– COLLECTOR	2.– CATHODE
3.– SOURCE	3.– EMITTER	3.– ANODE

D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

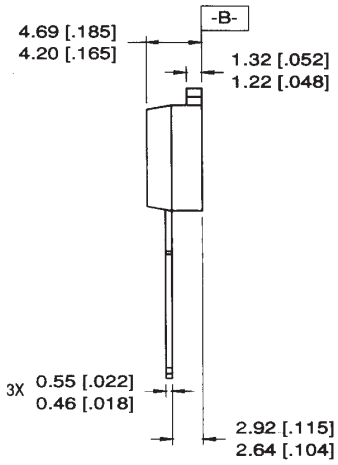


TO-262 Package Outline



LEAD ASSIGNMENTS

1 = GATE 3 = SOURCE
2 = DRAIN 4 = DRAIN

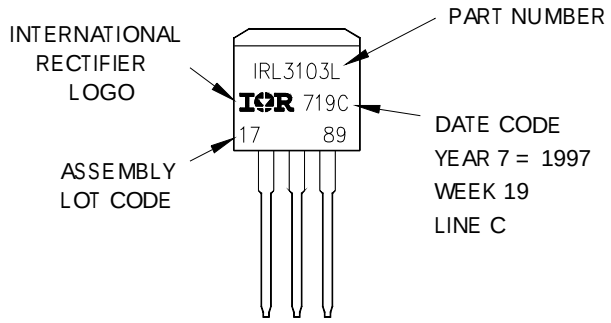


NOTES:

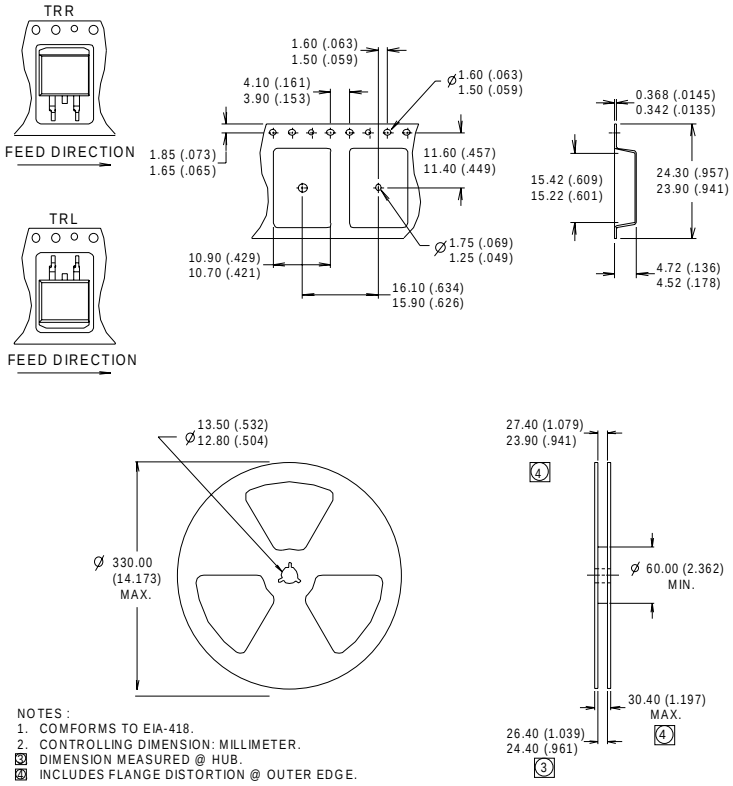
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



D²Pak Tape & Reel Information



NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3 DIMENSION MEASURED @ HUB.
4 INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.5/01

PD -93992

International
IOR Rectifier

AUTOMOTIVE MOSFET

IRF1405S
IRF1405L

Typical Applications

- Electric Power Steering (EPS)
- Anti-lock Braking System (ABS)
- Wiper Control
- Climate Control
- Power Door

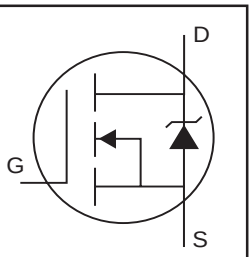
Benefits

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

Description

Stripe Planar design of HEXFET® Power MOSFETs utilizes the lastest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

HEXFET® Power MOSFET



V_{DSS} = 55V

$R_{DS(on)}$ = 5.3mΩ

I_D = 131A⑥





D^2Pak
IRF1405S

TO-262
IRF1405L

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	131⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	93⑥	
I_{DM}	Pulsed Drain Current ①	680	
P_D @T_C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	590	mJ
I_{AR}	Avalanche Current	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy⑦		mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)⑧	—	40	

1/11/01

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.057	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	4.6	5.3	mΩ	V_{GS} = 10V, I_D = 101A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = 10V, I_D = 250µA
g_{fs}	Forward Transconductance	69	—	—	S	V_{DS} = 25V, I_D = 110A
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 55V, V_{GS} = 0V
		—	—	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V
Q_g	Total Gate Charge	—	170	260	nC	I_D = 101A
Q_{gs}	Gate-to-Source Charge	—	44	66		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	62	93		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	V_{DD} = 38V
t_r	Rise Time	—	190	—		I_D = 110A
$t_{d(off)}$	Turn-Off Delay Time	—	130	—		R_G = 1.1Ω
t_f	Fall Time	—	110	—		V_{GS} = 10V ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	5480	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1210	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	280	—		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	5210	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	900	—		V_{GS} = 0V, V_{DS} = 44V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	—	1500	—		V_{GS} = 0V, V_{DS} = 0V to 44V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	131⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	680		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 101A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	88	130	ns	T_J = 25°C, I_F = 101A
Q_{rr}	Reverse RecoveryCharge	—	250	380	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

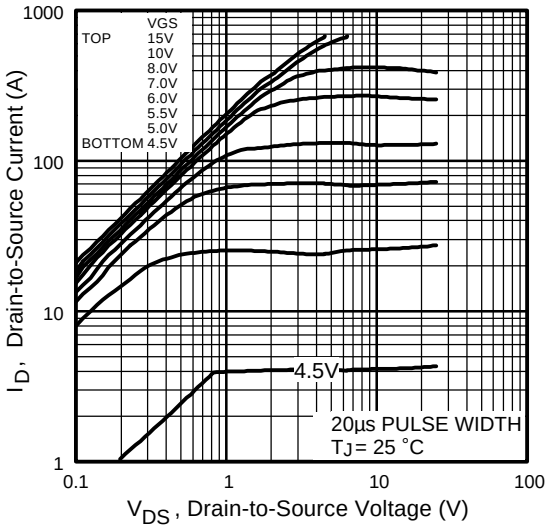


Fig 1. Typical Output Characteristics

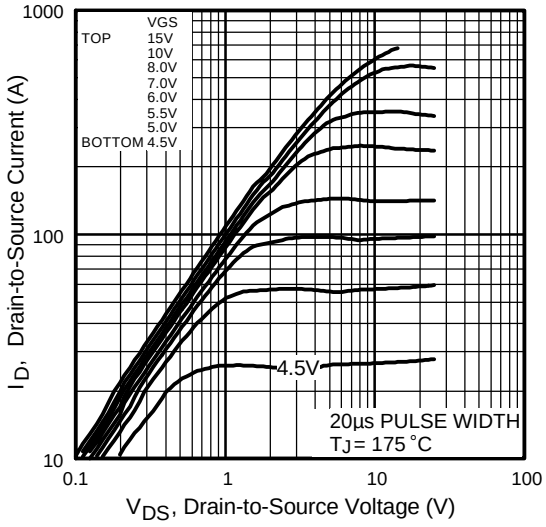


Fig 2. Typical Output Characteristics

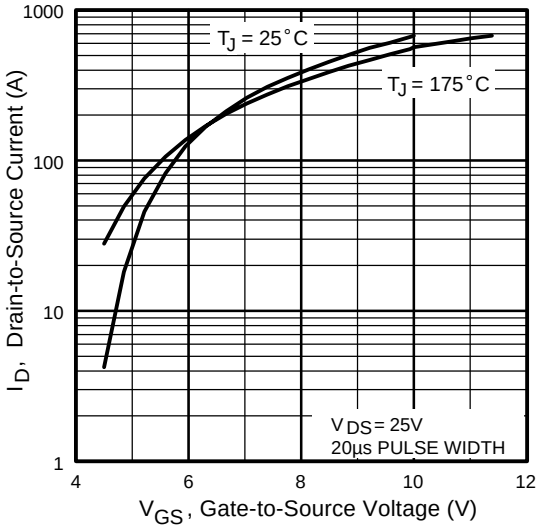


Fig 3. Typical Transfer Characteristics

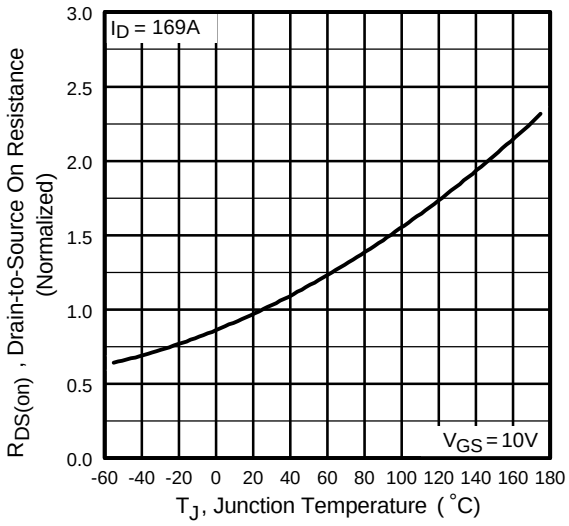


Fig 4. Normalized On-Resistance Vs. Temperature

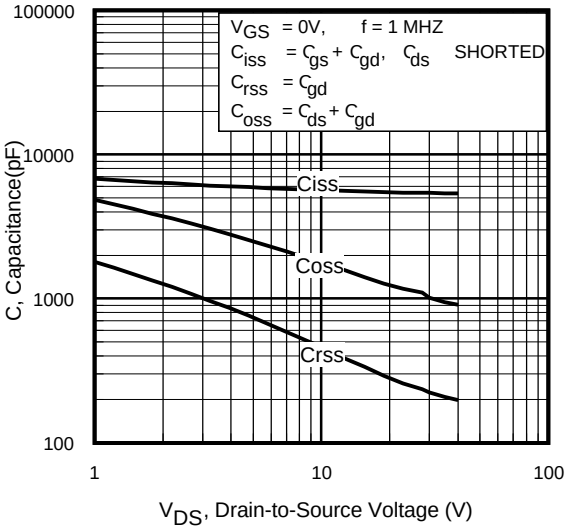


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

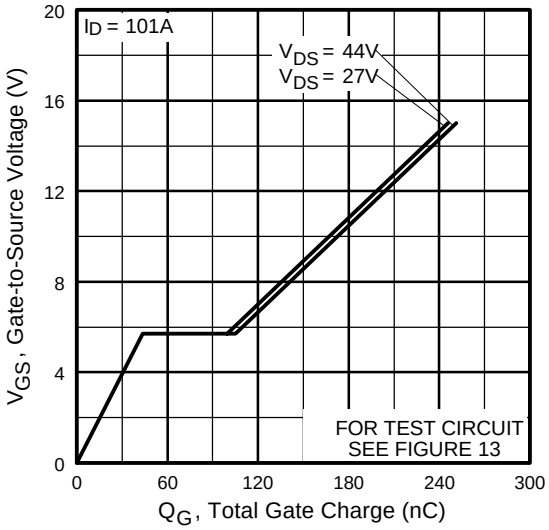


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

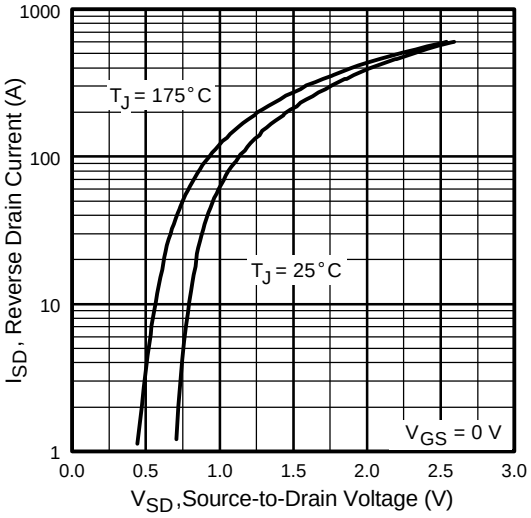


Fig 7. Typical Source-Drain Diode Forward Voltage

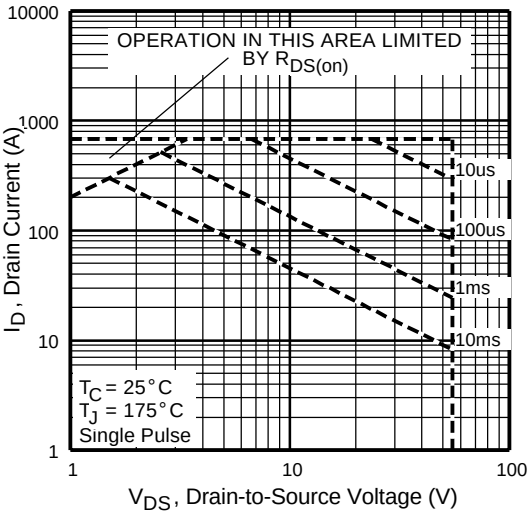


Fig 8. Maximum Safe Operating Area

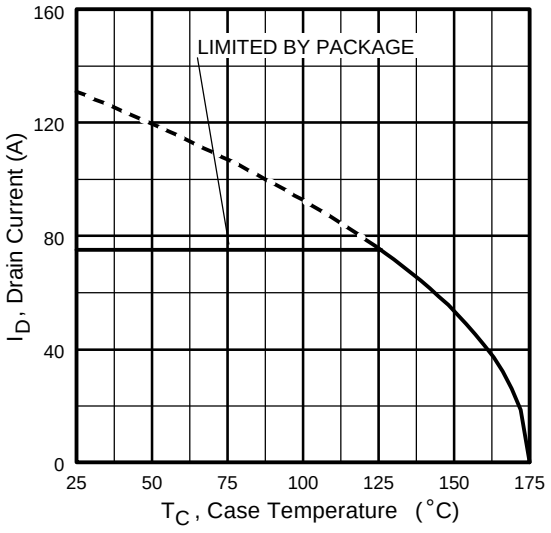


Fig 9. Maximum Drain Current Vs. Case Temperature

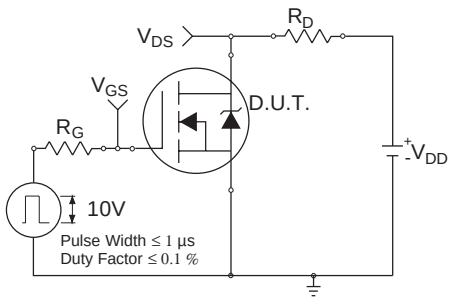


Fig 10a. Switching Time Test Circuit

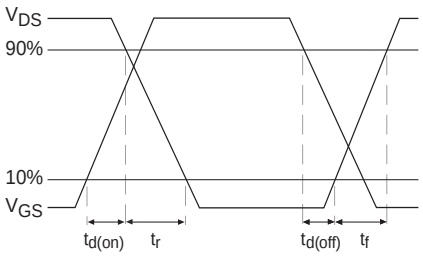


Fig 10b. Switching Time Waveforms

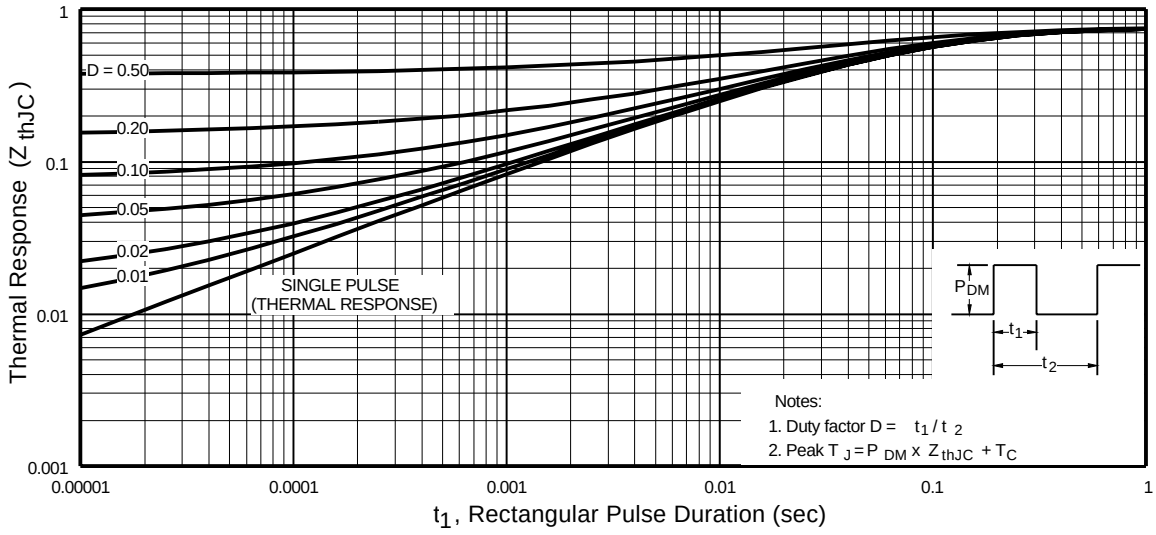


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

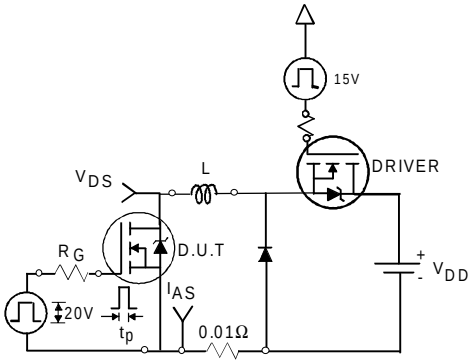


Fig 12a. Unclamped Inductive Test Circuit

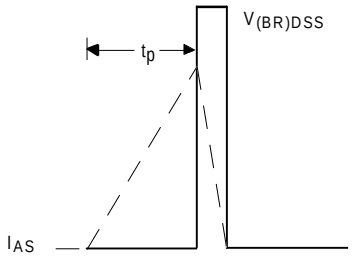


Fig 12b. Unclamped Inductive Waveforms

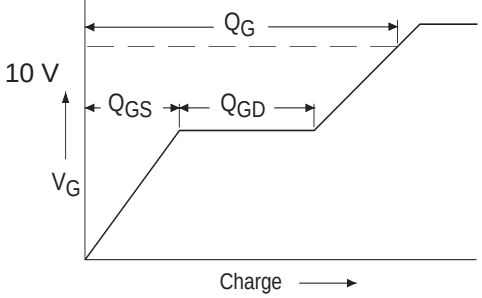


Fig 13a. Basic Gate Charge Waveform

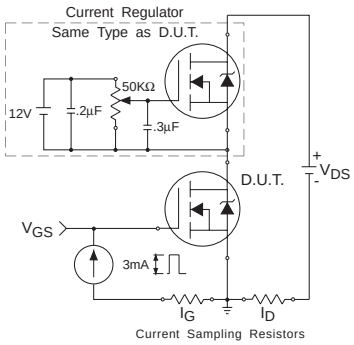


Fig 13b. Gate Charge Test Circuit

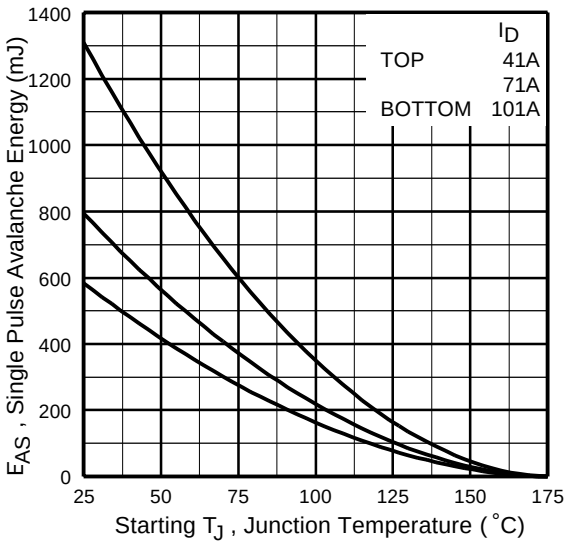


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

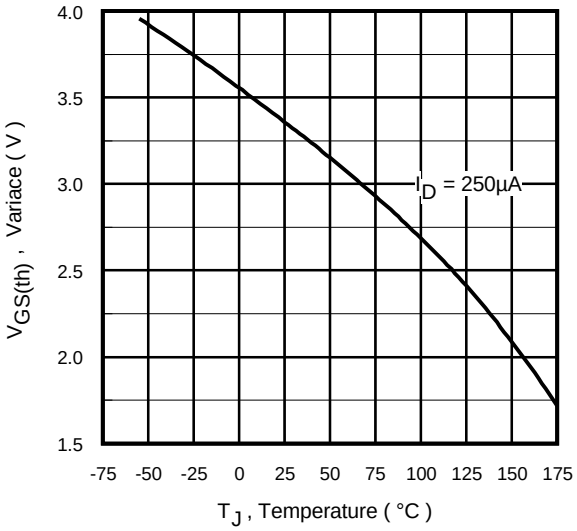


Fig 14. Threshold Voltage Vs. Temperature

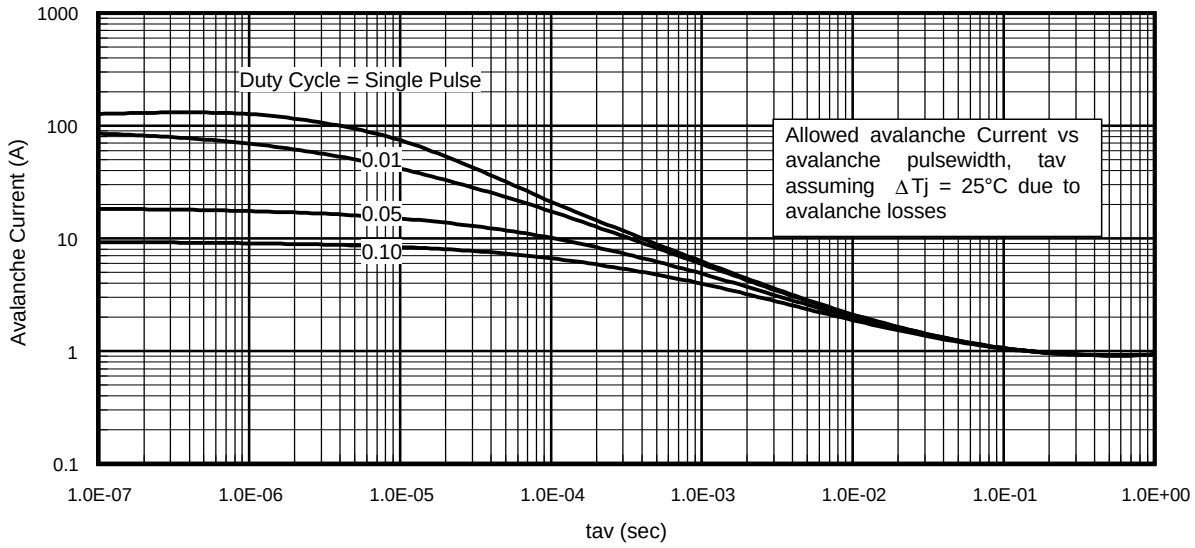


Fig 15. Typical Avalanche Current Vs.Pulsewidth

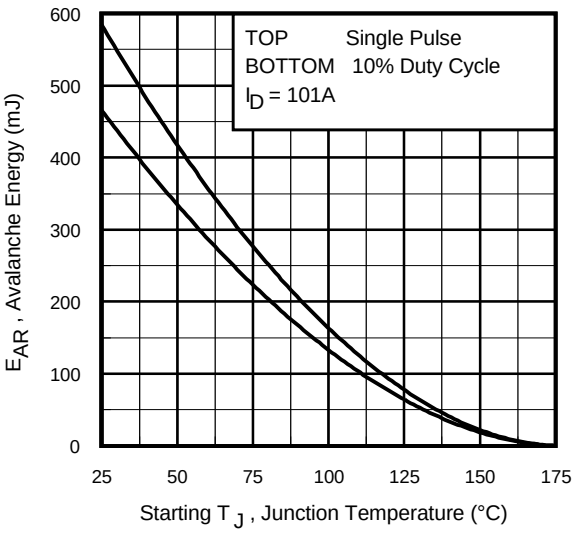


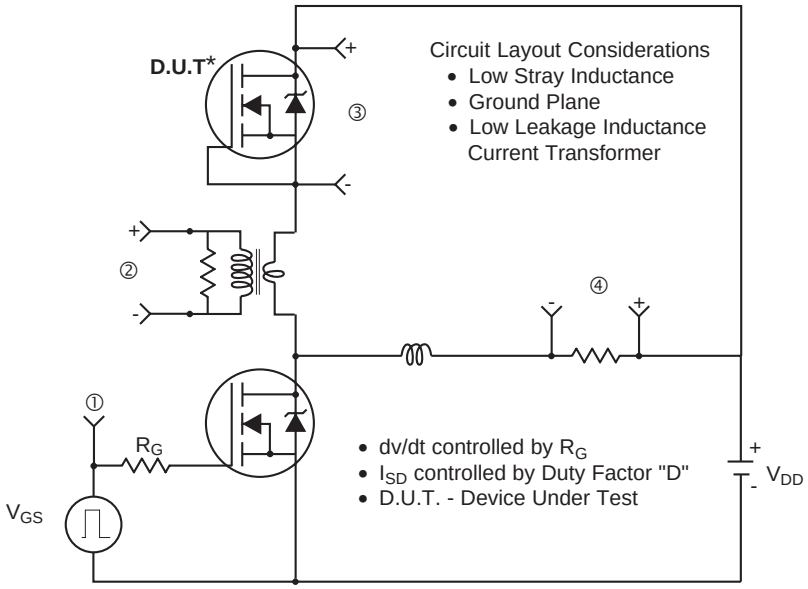
Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at www.irf.com)

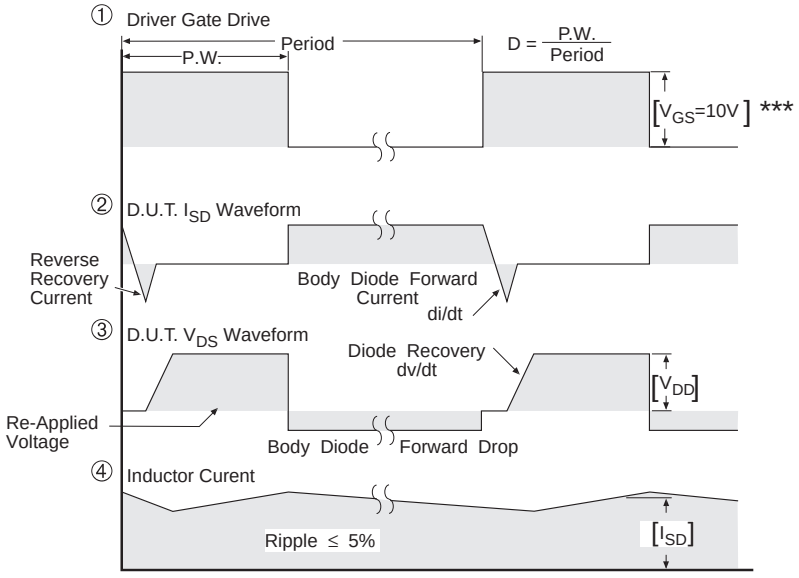
1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

Peak Diode Recovery dv/dt Test Circuit



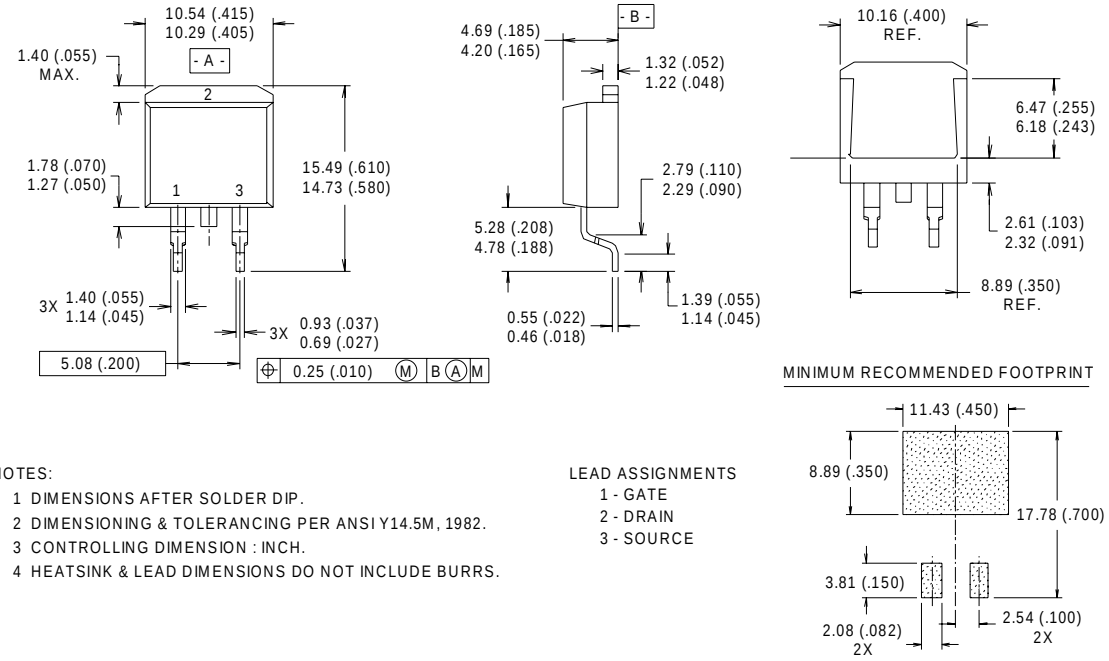
* Reverse Polarity of D.U.T for P-Channel



*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 17. For N-channel HEXFET® power MOSFETs

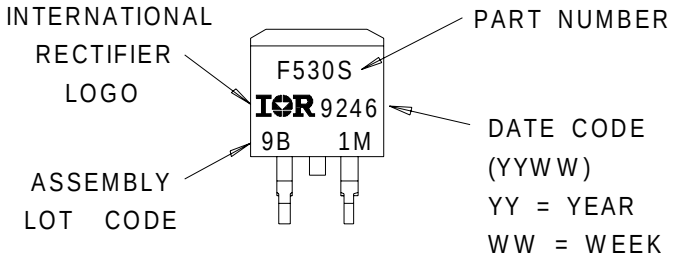
D²Pak Package Outline



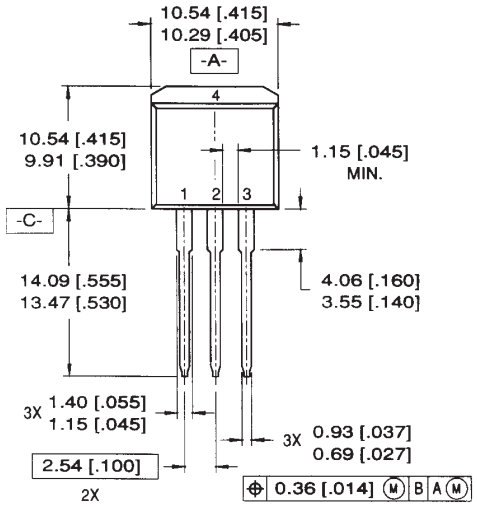
NOTES:
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

D²Pak Part Marking Information

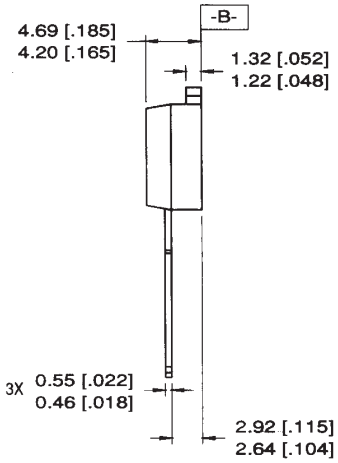


TO-262 Package Outline



LEAD ASSIGNMENTS

1 = GATE 3 = SOURCE
2 = DRAIN 4 = DRAIN

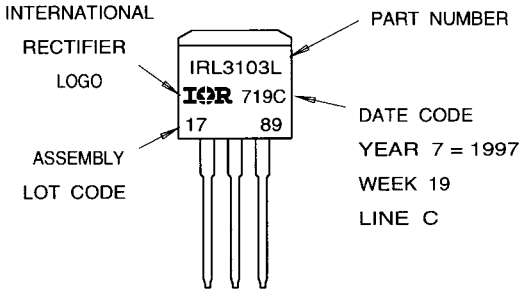


NOTES:

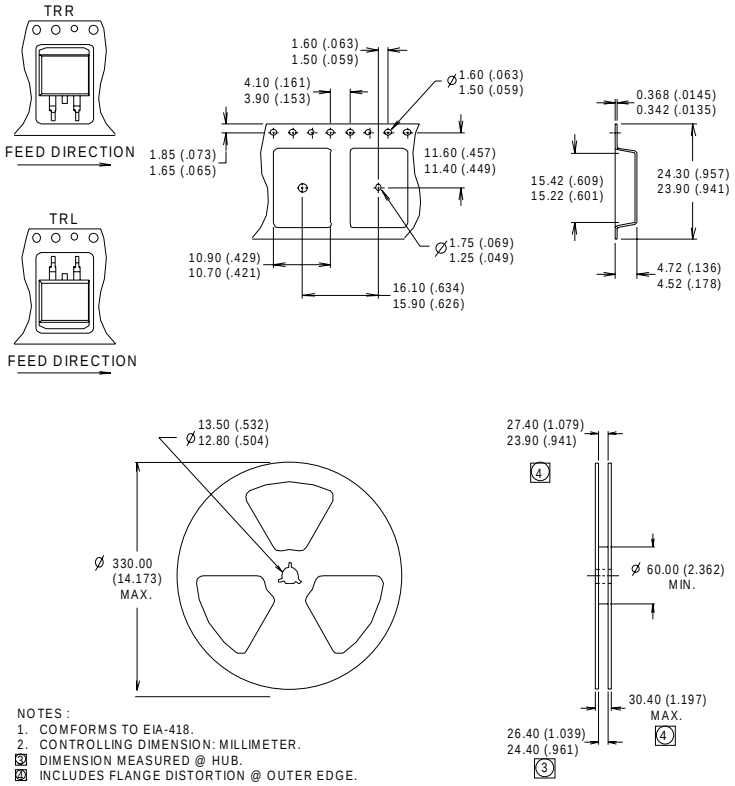
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



D²Pak Tape & Reel Information



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Starting T_J = 25°C, L = 0.11mH R_G = 25Ω, I_{AS} = 101A. (See Figure 12).

③ $I_{SD} \leq$ 101A, di/dt ≤ 210A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

⑦ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑧ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.1/01

International
IOR Rectifier

PD -93906A

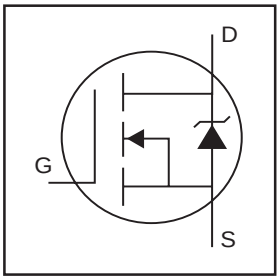
IRFP2907

AUTOMOTIVE MOSFET

HEXFET® Power MOSFET

Typical Applications

- Integrated Starter Alternator
- 42 Volts Automotive Electrical Systems



V_{DSS} = 75V

$R_{DS(on)}$ = 4.5mΩ

I_D = 209A⑥

Benefits

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

Description

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the lastest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	209⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	148⑥	
I_{DM}	Pulsed Drain Current ①	840	
P_D @T_C = 25°C	Power Dissipation	470	W
	Linear Derating Factor	3.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	1970	mJ
I_{AR}	Avalanche Current	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy⑦		mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.32	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient	——	40	

9/7/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.085	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.6	4.5	mΩ	V_{GS} = 10V, I_D = 125A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = 10V, I_D = 250µA
g_{fs}	Forward Transconductance	130	—	—	S	V_{DS} = 25V, I_D = 125A
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 75V, V_{GS} = 0V
		—	—	250		V_{DS} = 60V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V
Q_g	Total Gate Charge	—	410	620	nC	I_D = 125A
Q_{gs}	Gate-to-Source Charge	—	92	140		V_{DS} = 60V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	140	210		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	V_{DD} = 38V
t_r	Rise Time	—	190	—		I_D = 125A
$t_{d(off)}$	Turn-Off Delay Time	—	130	—		R_G = 1.2Ω
t_f	Fall Time	—	130	—		V_{GS} = 10V ④
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	13	—		
C_{iss}	Input Capacitance	—	13000	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	2100	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	500	—		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	9780	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	1360	—		V_{GS} = 0V, V_{DS} = 60V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	—	2320	—		V_{GS} = 0V, V_{DS} = 0V to 60V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	209⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	840		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 125A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	140	210	ns	T_J = 25°C, I_F = 125A
Q_{rr}	Reverse RecoveryCharge	—	880	1320	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Starting T_J = 25°C, L = 0.25mH R_G = 25Ω, I_{AS} = 125A. (See Figure 12).

③ I_{SD} ≤ 125A, di/dt ≤ 260A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 90A.

⑦ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

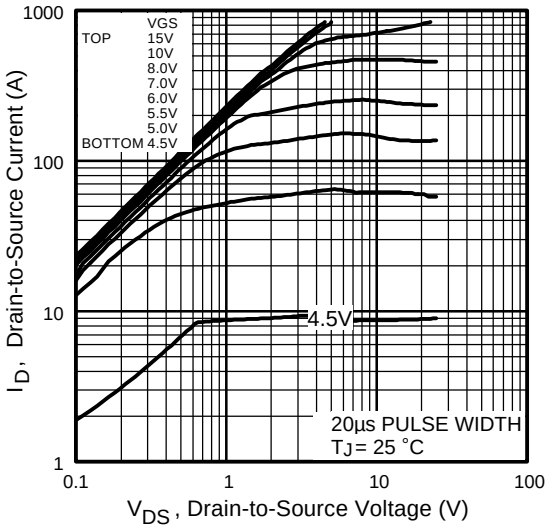


Fig 1. Typical Output Characteristics

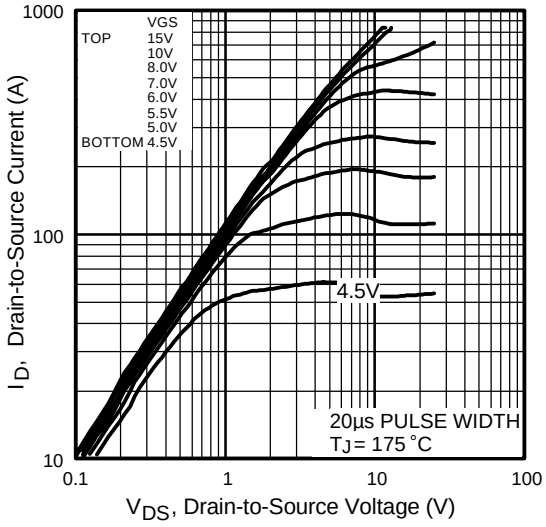


Fig 2. Typical Output Characteristics

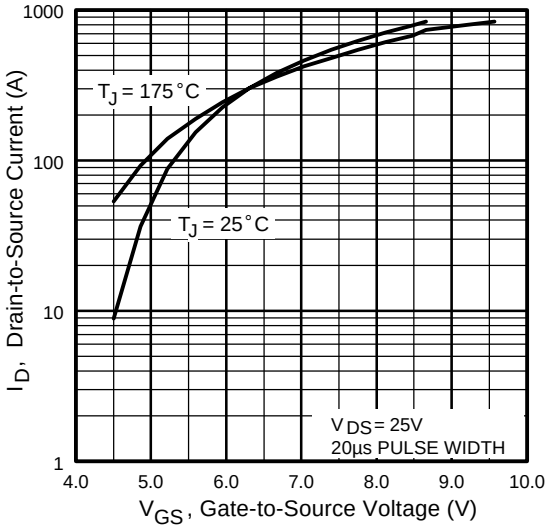


Fig 3. Typical Transfer Characteristics

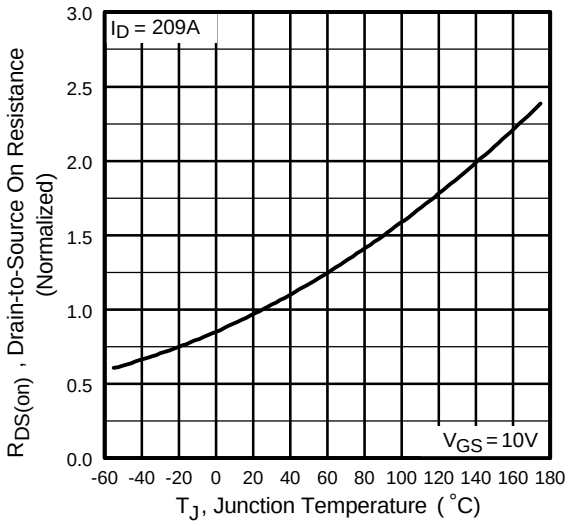


Fig 4. Normalized On-Resistance Vs. Temperature

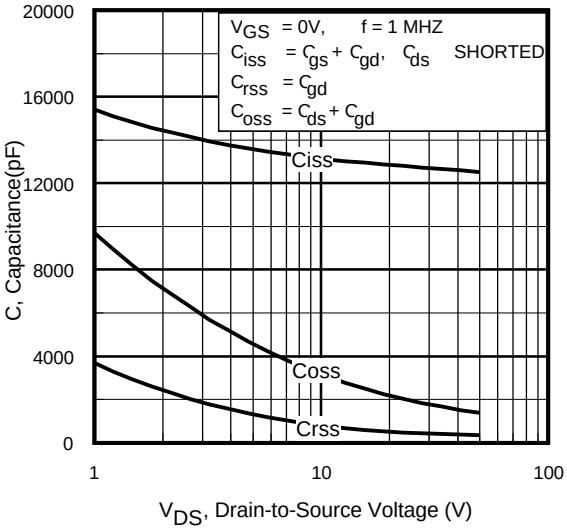


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

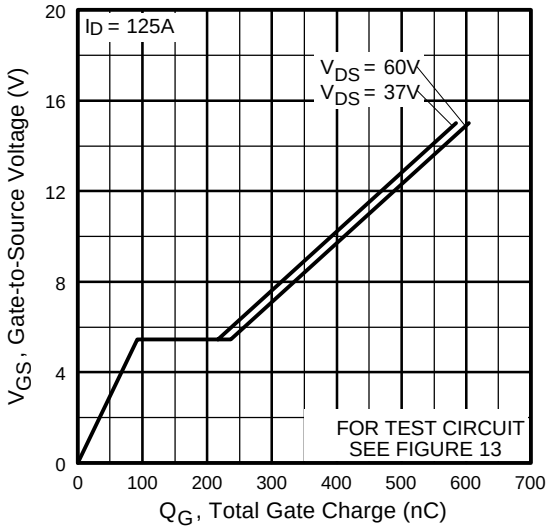


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

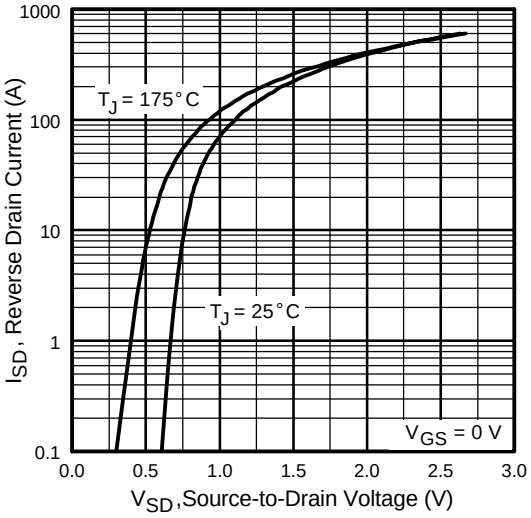


Fig 7. Typical Source-Drain Diode Forward Voltage

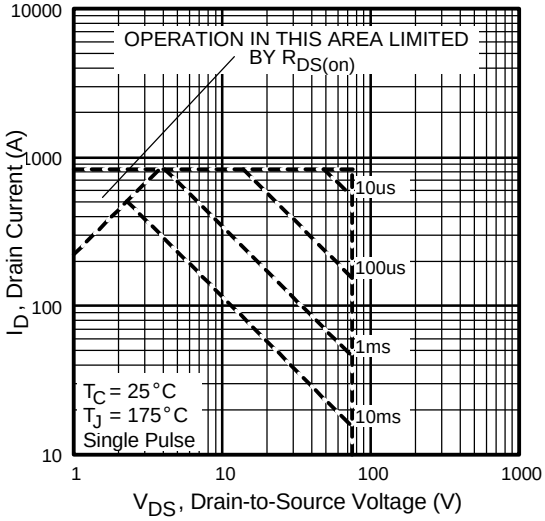


Fig 8. Maximum Safe Operating Area

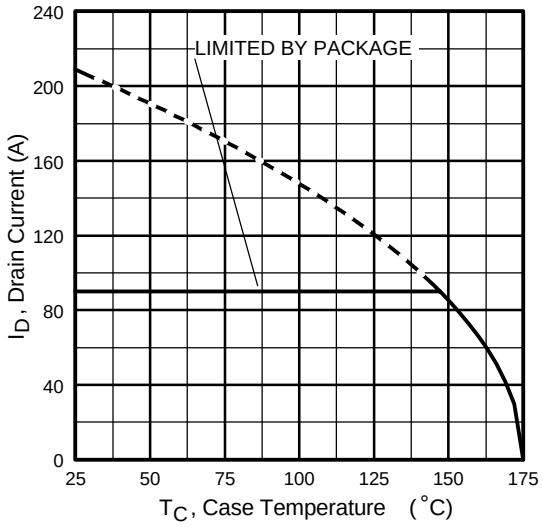


Fig 9. Maximum Drain Current Vs. Case Temperature

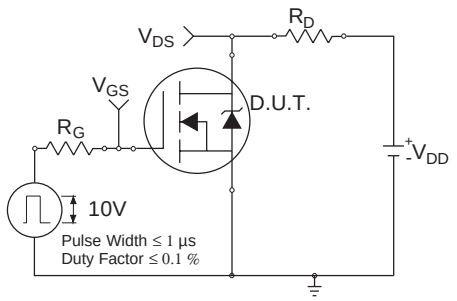


Fig 10a. Switching Time Test Circuit

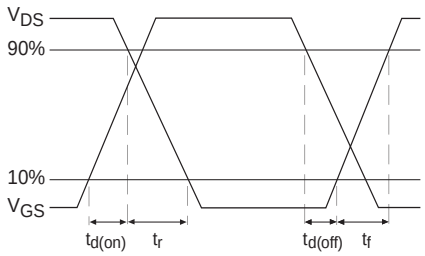


Fig 10b. Switching Time Waveforms

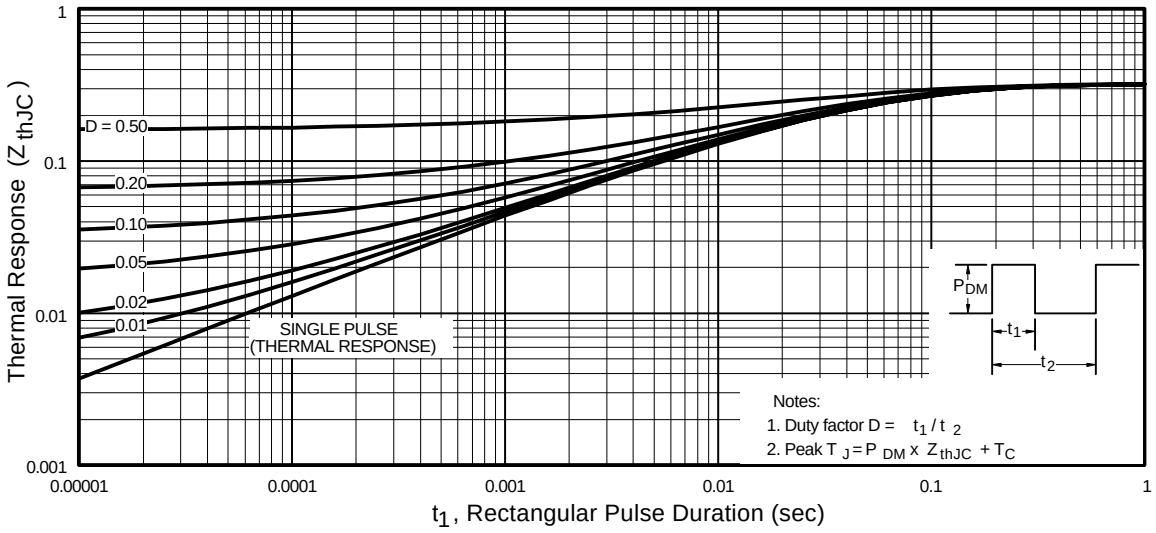


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

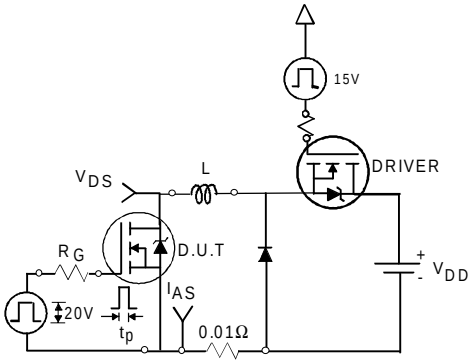


Fig 12a. Unclamped Inductive Test Circuit

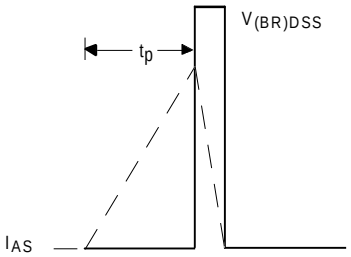


Fig 12b. Unclamped Inductive Waveforms

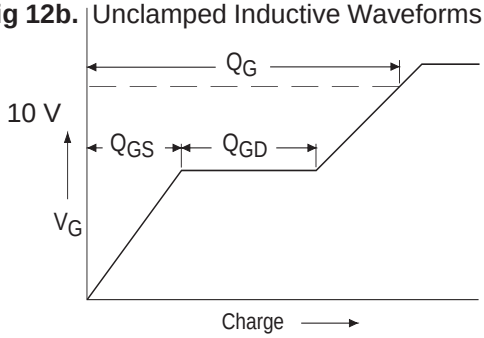


Fig 13a. Basic Gate Charge Waveform

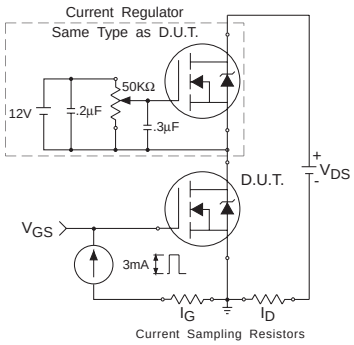


Fig 13b. Gate Charge Test Circuit

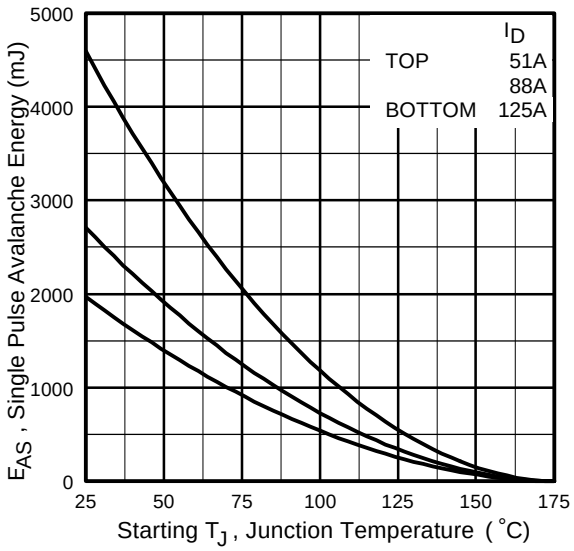


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

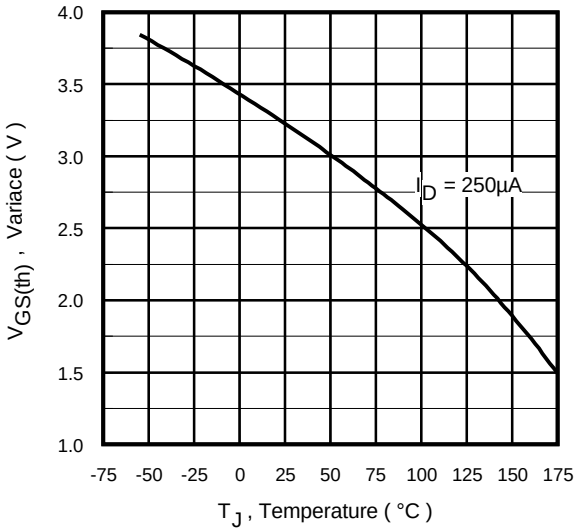


Fig 14. Threshold Voltage Vs. Temperature

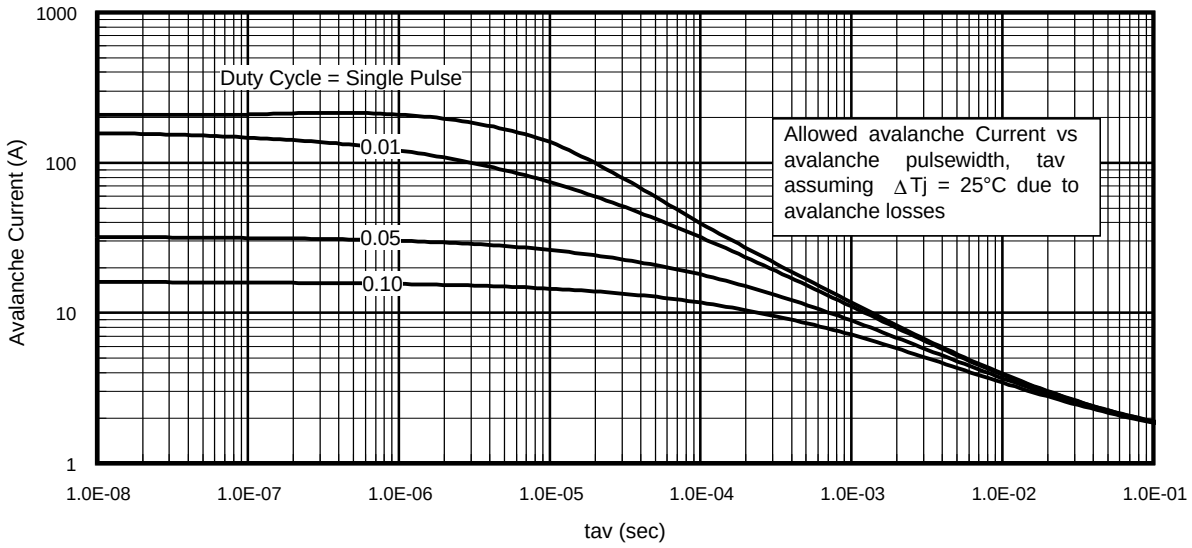


Fig 15. Typical Avalanche Current Vs.Pulsewidth

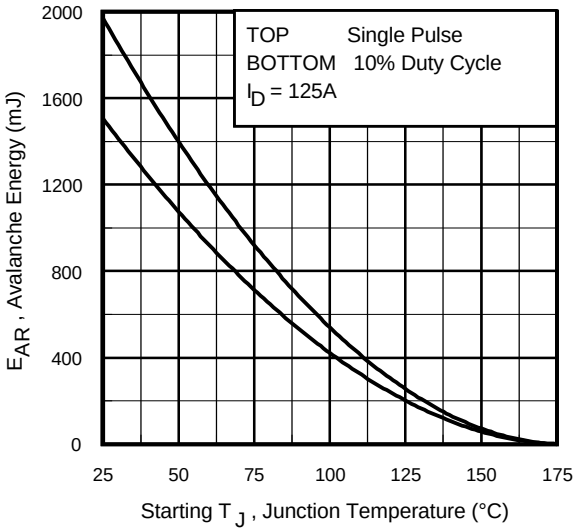


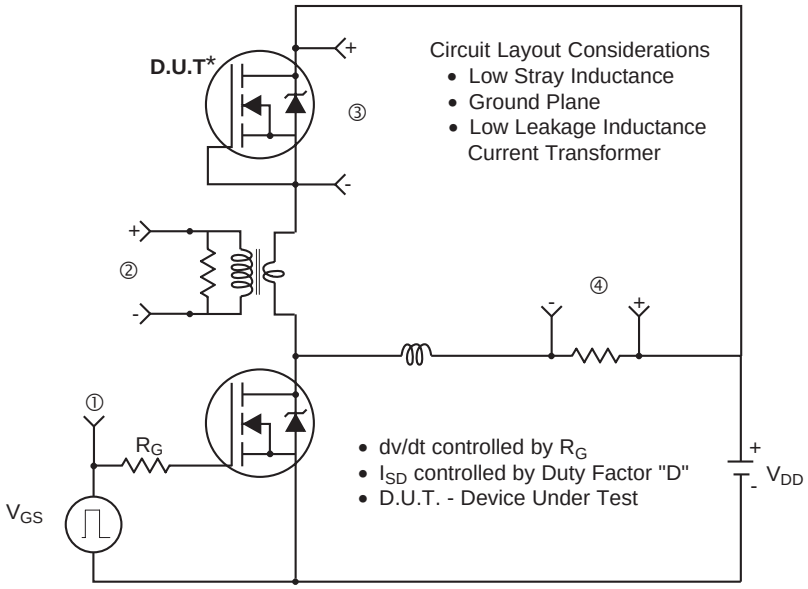
Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at www.irf.com)

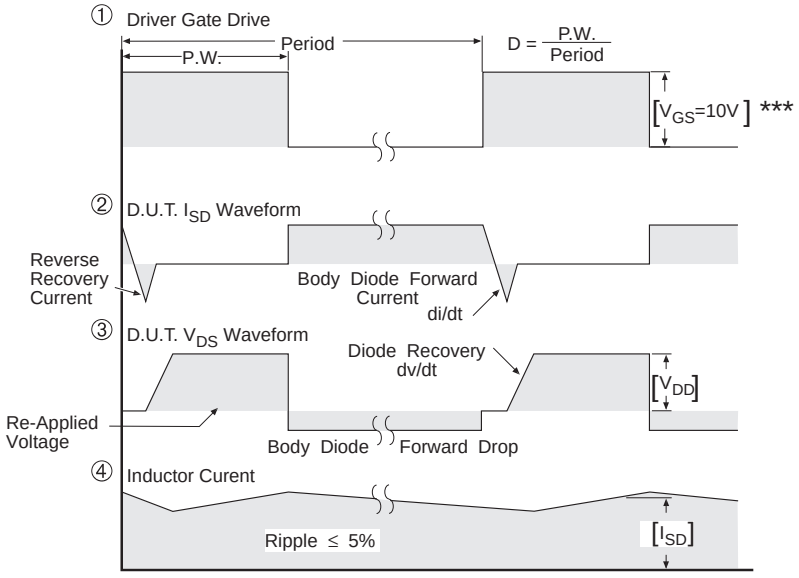
1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

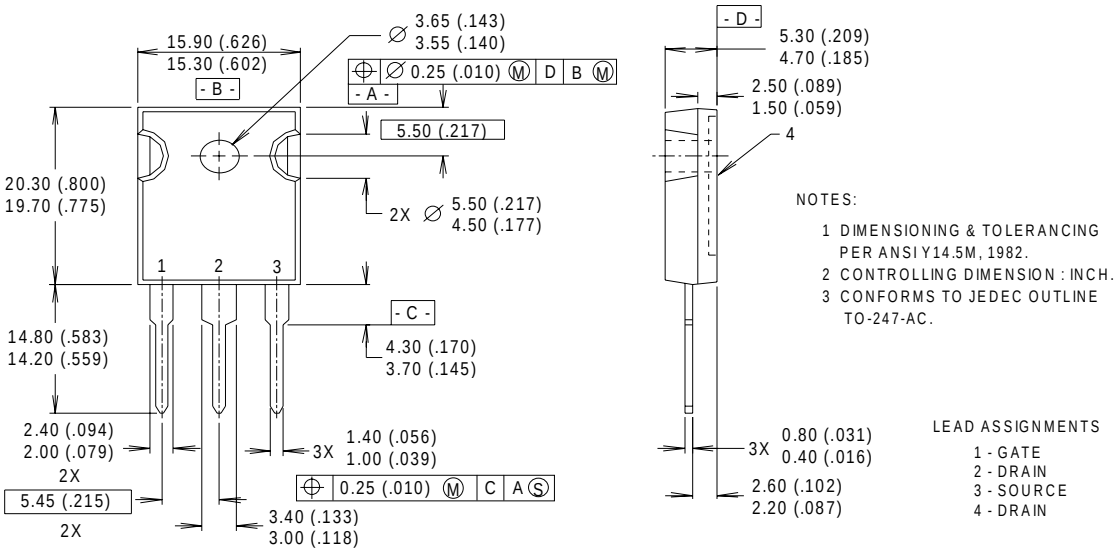


*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 17. For N-channel HEXFET® power MOSFETs

TO - 247 Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-247-AC.

LEAD ASSIGNMENTS

1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

Data and specifications subject to change without notice9/00

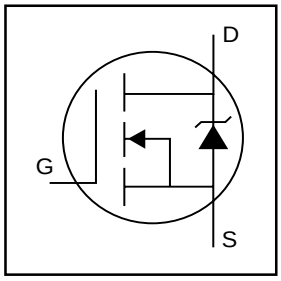
International
IOR Rectifier

PD - 91477D

IRF3415

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 150V

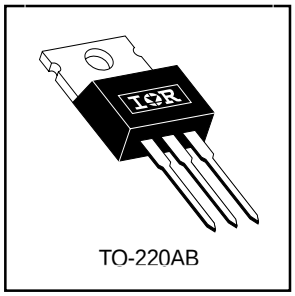
$R_{DS(on)}$ = 0.042Ω

I_D = 43A

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

Absolute Maximum Ratings

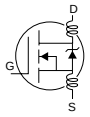
	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	43	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	30	
I_{DM}	Pulsed Drain Current ①	150	
P_D @T_C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	590	mJ
I_{AR}	Avalanche Current①	22	A
E_{AR}	Repetitive Avalanche Energy①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

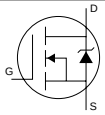
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.17	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.042	Ω	V_{GS} = 10V, I_D = 22A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	19	—	—	S	V_{DS} = 50V, I_D = 22A
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 150V, V_{GS} = 0V
		—	—	250		V_{DS} = 120V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	200	nC	I_D = 22A
Q_{gs}	Gate-to-Source Charge	—	—	17		V_{DS} = 120V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	98		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	V_{DD} = 75V
t_r	Rise Time	—	55	—		I_D = 22A
$t_{d(off)}$	Turn-Off Delay Time	—	71	—		R_G = 2.5Ω
t_f	Fall Time	—	69	—		R_D = 3.3Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	2400	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	640	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	340	—		f = 1.0MHz, See Fig. 5



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	43	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	150		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 22A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	260	390	ns	T_J = 25°C, I_F = 22A
Q_{rr}	Reverse RecoveryCharge	—	2.2	3.3	µC	di/dt = 100A/µs ④



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = 25V, starting T_J = 25°C, L = 2.4mH R_G = 25Ω, I_{AS} = 22A. (See Figure 12)

③ I_{SD} ≤ 22A, di/dt ≤ 820A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

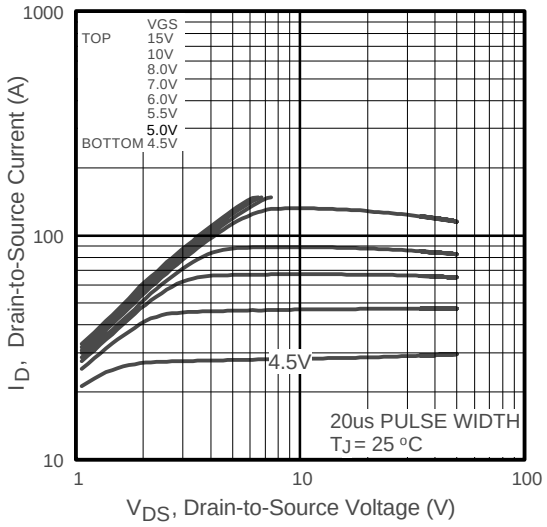


Fig 1. Typical Output Characteristics

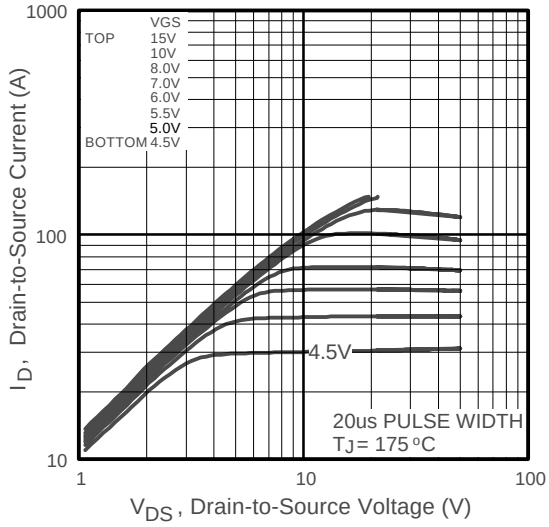


Fig 2. Typical Output Characteristics

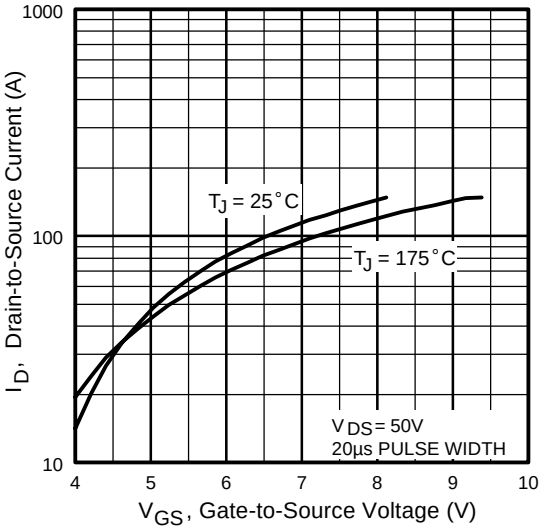


Fig 3. Typical Transfer Characteristics

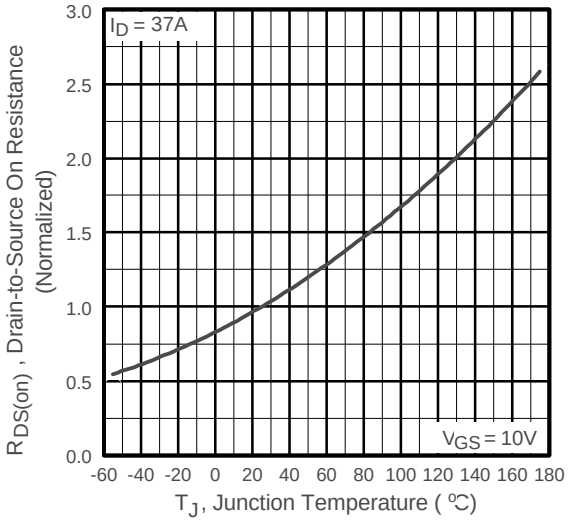


Fig 4. Normalized On-Resistance Vs. Temperature

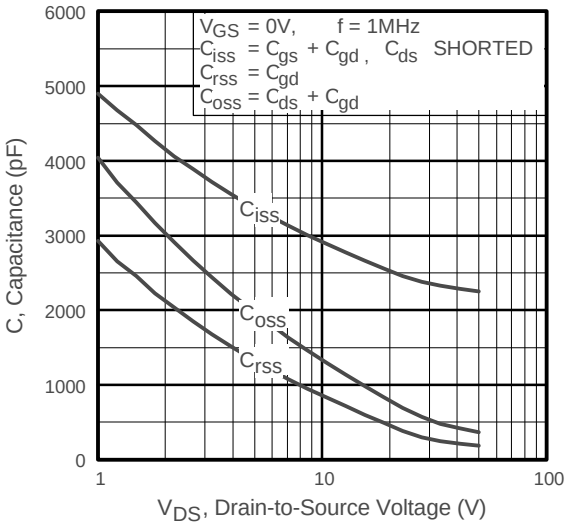


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

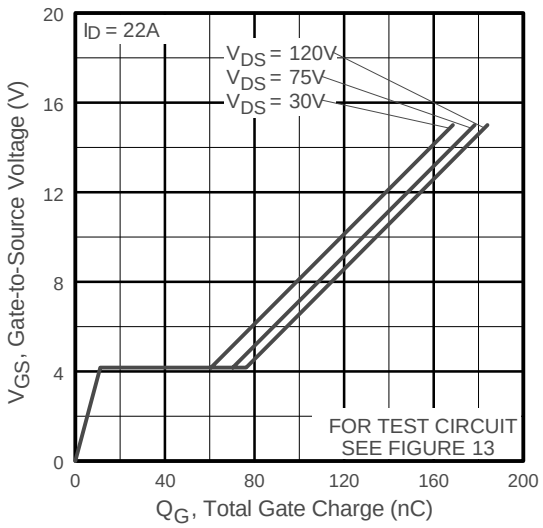


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

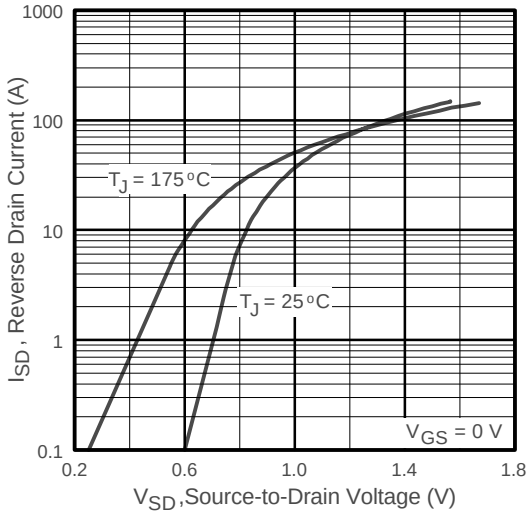


Fig 7. Typical Source-Drain Diode Forward Voltage

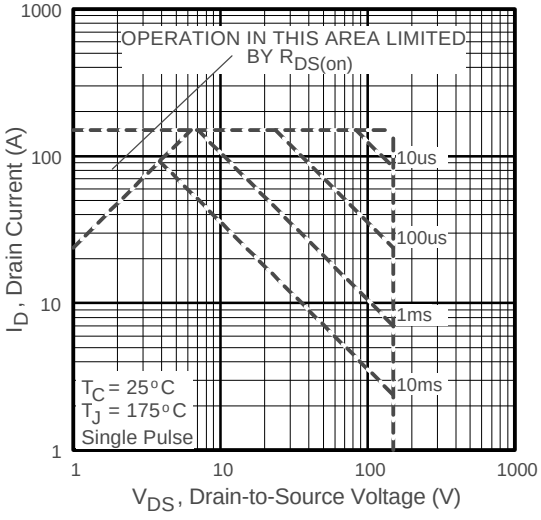


Fig 8. Maximum Safe Operating Area

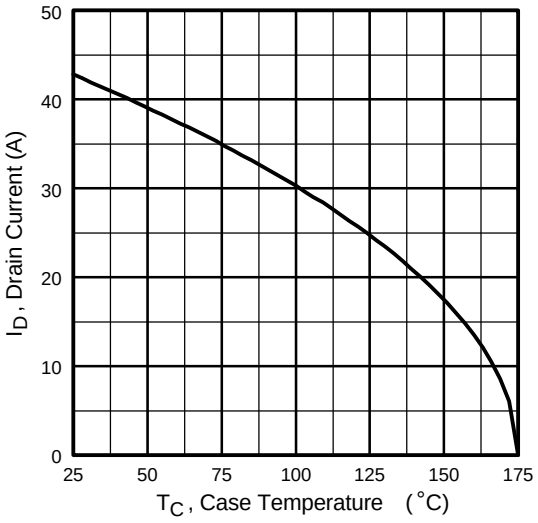


Fig 9. Maximum Drain Current Vs. Case Temperature

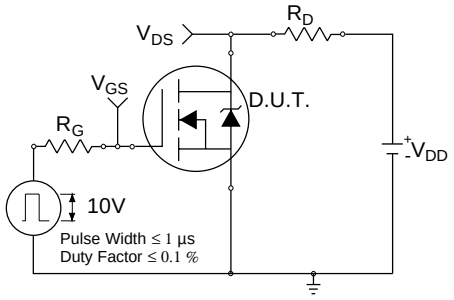


Fig 10a. Switching Time Test Circuit

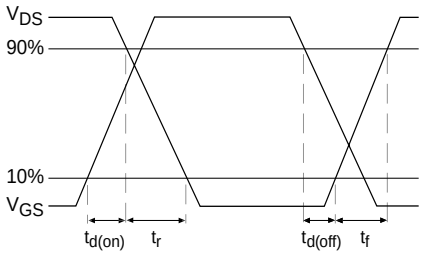


Fig 10b. Switching Time Waveforms

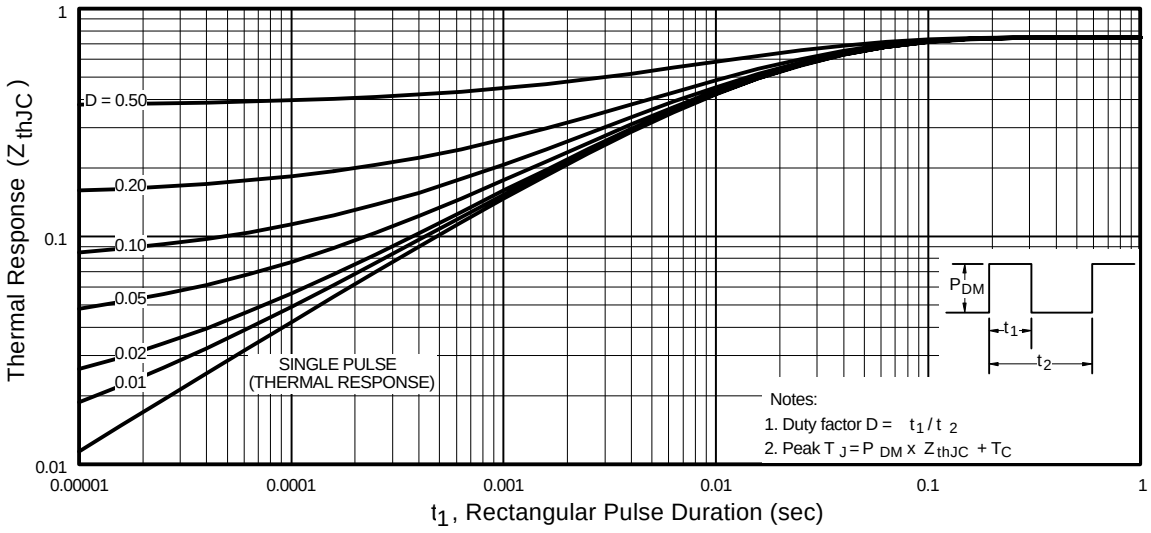


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

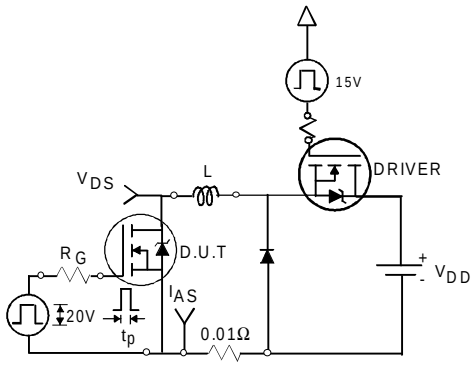


Fig 12a. Unclamped Inductive Test Circuit

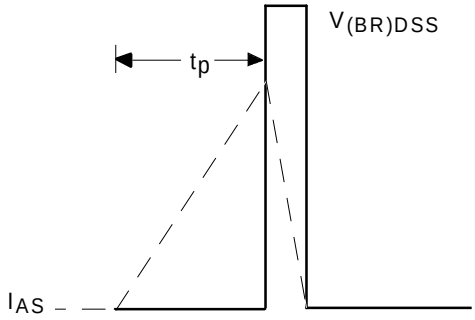


Fig 12b. Unclamped Inductive Waveforms

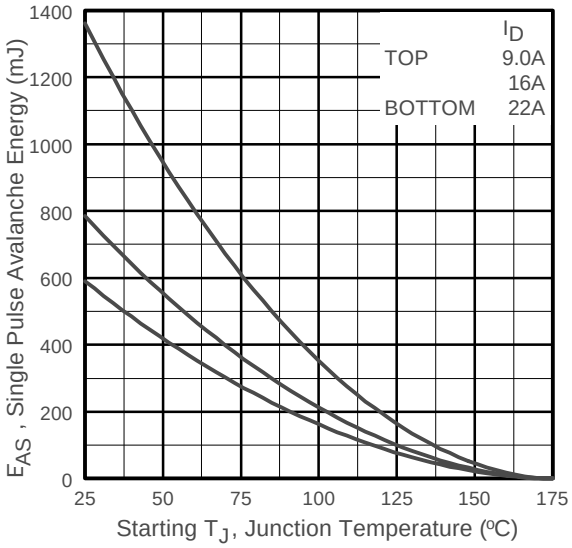


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

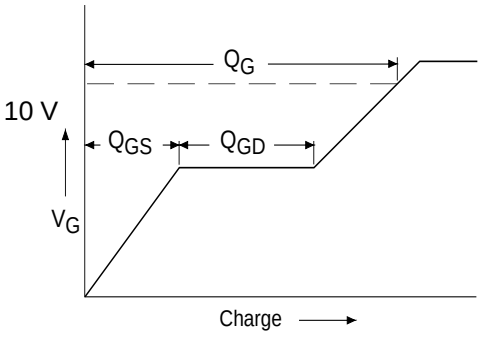


Fig 13a. Basic Gate Charge Waveform

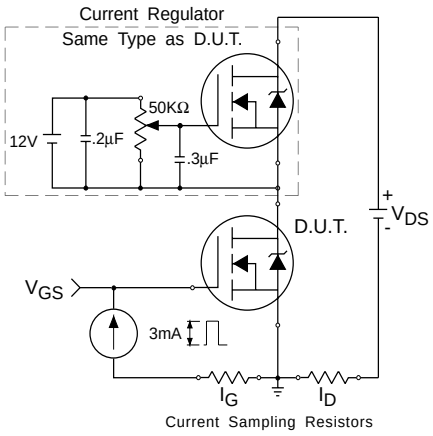
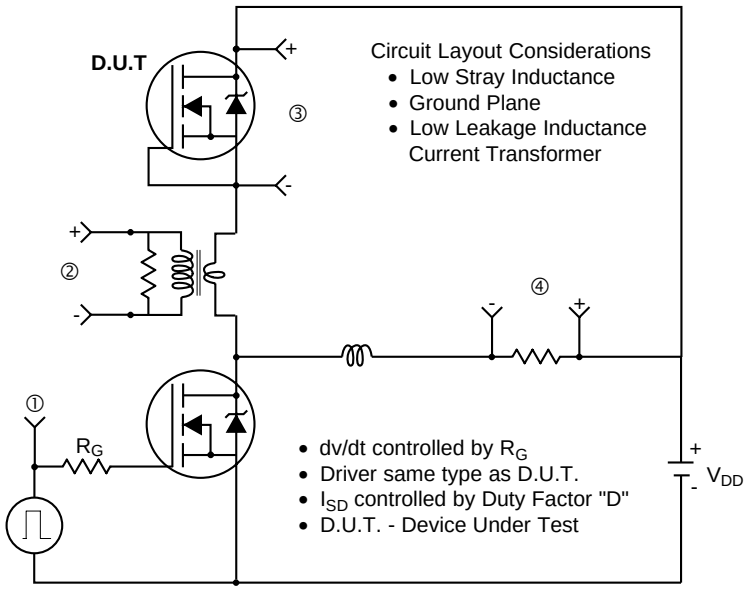
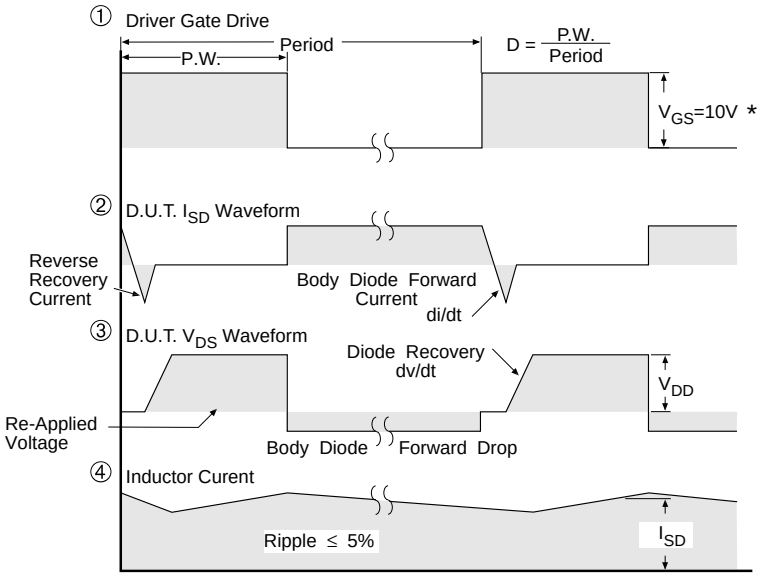


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit





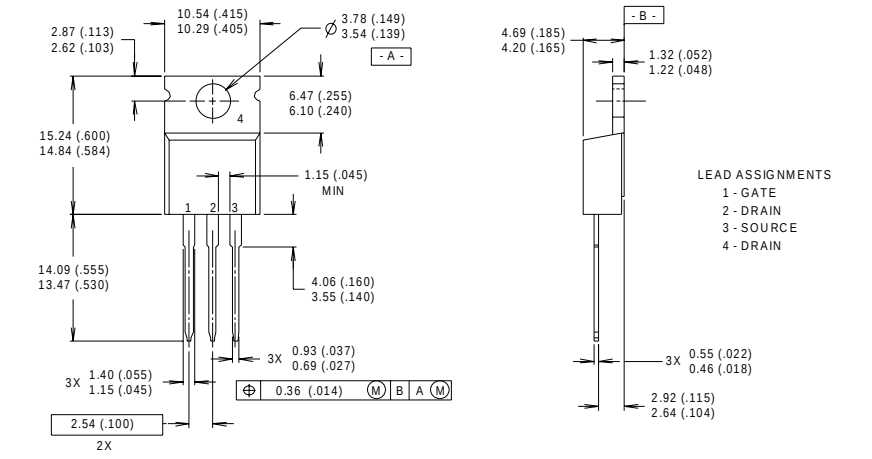
* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

TO-220AB Outline

Dimensions are shown in millimeters (inches)



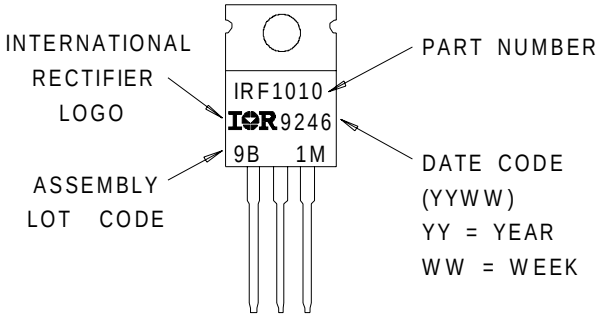
NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371

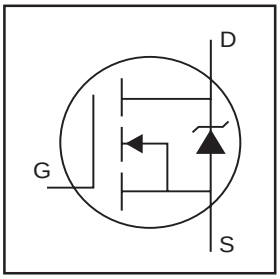
International
IOR Rectifier

PD - 91509C

IRF3415S/L

HEXFET® Power MOSFET

- Advanced Process Technology
- Surface Mount (IRF3415S)
- Low-profile through-hole (IRF3415L)
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 150V

$R_{DS(on)}$ = 0.042Ω

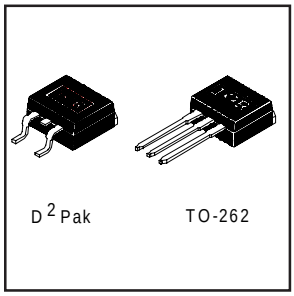
I_D = 43A

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D^2Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D^2Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRF3415L) is available for low-profile applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V⑤	43	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V⑤	30	
I_{DM}	Pulsed Drain Current ①⑤	150	
P_D @T_A = 25°C	Power Dissipation	3.8	W
P_D @T_C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑤	590	mJ
I_{AR}	Avalanche Current①	22	A
E_{AR}	Repetitive Avalanche Energy①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	℃
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

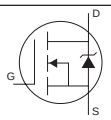
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted,steady-state)**	——	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.17	—	V/°C	Reference to 25°C, I_D = 1mA⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.042	Ω	V_{GS} = 10V, I_D = 22A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	19	—	—	S	V_{DS} = 50V, I_D = 22A⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 150V, V_{GS} = 0V
		—	—	250		V_{DS} = 120V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	200	nC	I_D = 22A
Q_{gs}	Gate-to-Source Charge	—	—	17		V_{DS} = 120V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	98		V_{GS} = 10V, See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	V_{DD} = 75V
t_r	Rise Time	—	55	—		I_D = 22A
$t_{d(off)}$	Turn-Off Delay Time	—	71	—		R_G = 2.5Ω
t_f	Fall Time	—	69	—		R_D = 3.3Ω, See Fig. 10 ④⑤
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	2400	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	640	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	340	—		f = 1.0MHz, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	43	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑤	—	—	150		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 22A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	260	390	ns	T_J = 25°C, I_F = 22A
Q_{rr}	Reverse Recovery Charge	—	2.2	3.3	µC	di/dt = 100A/µs ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 2.4mH R_G = 25Ω, I_{AS} = 22A. (See Figure 12)

③ I_{SD} ≤ 22A, di/dt ≤ 820A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ Uses IRF3415 data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended soldering techniques refer to application note #AN-994.

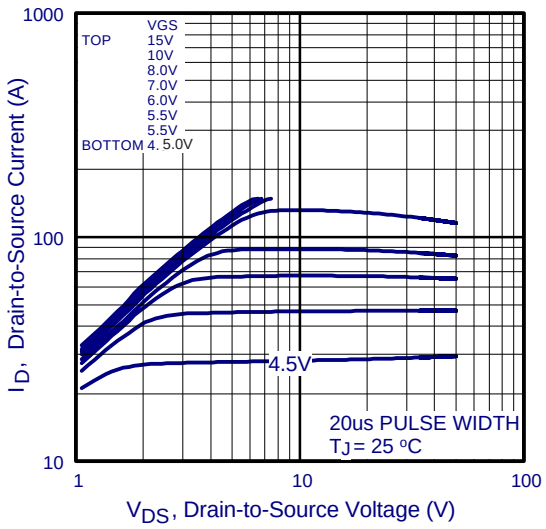


Fig 1. Typical Output Characteristics

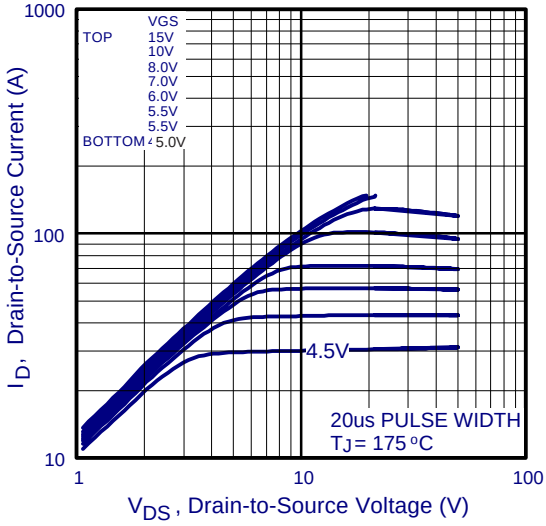


Fig 2. Typical Output Characteristics

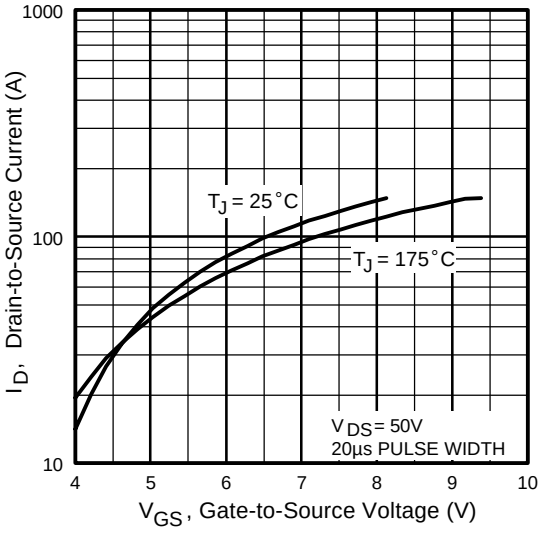


Fig 3. Typical Transfer Characteristics

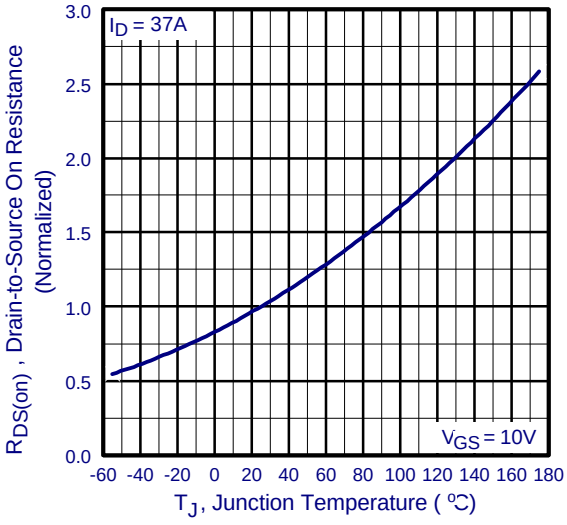


Fig 4. Normalized On-Resistance Vs. Temperature

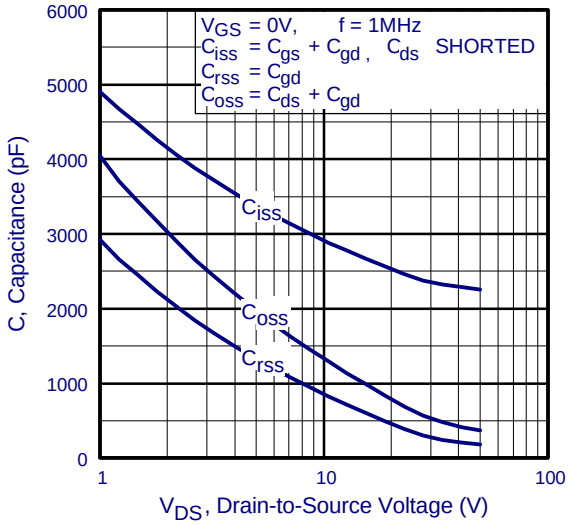


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

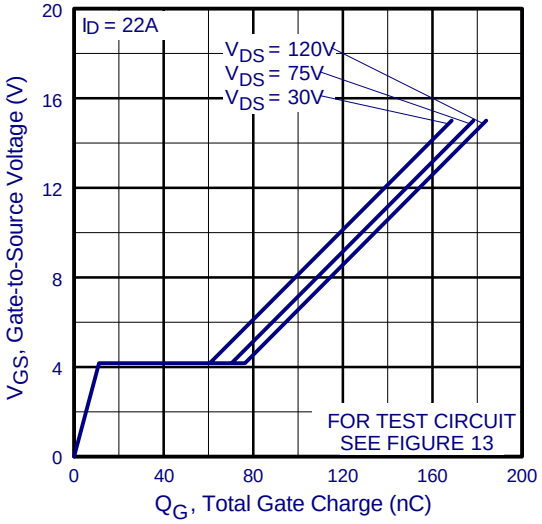


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

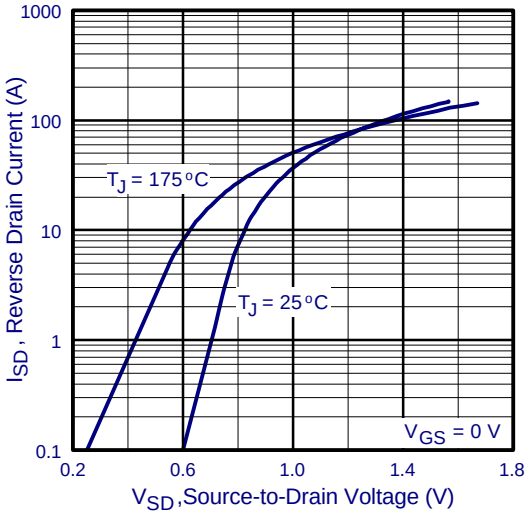


Fig 7. Typical Source-Drain Diode Forward Voltage

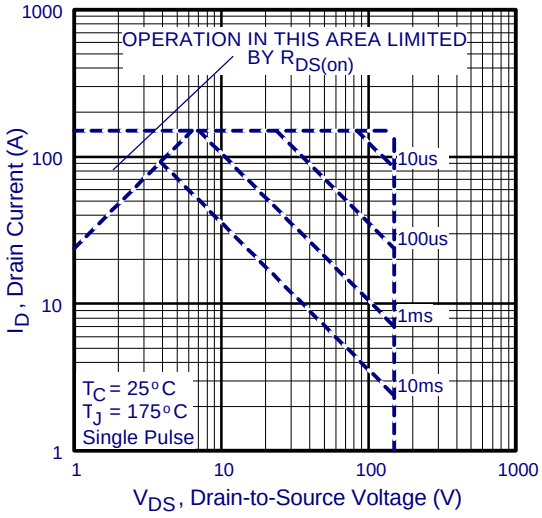


Fig 8. Maximum Safe Operating Area

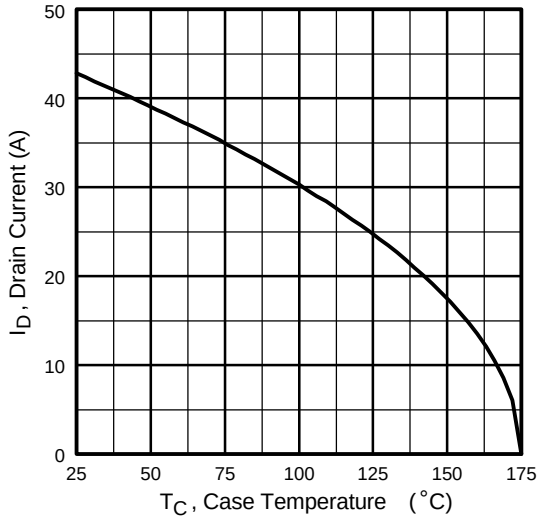


Fig 9. Maximum Drain Current Vs. Case Temperature

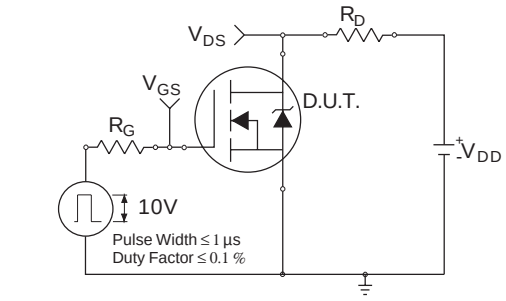


Fig 10a. Switching Time Test Circuit

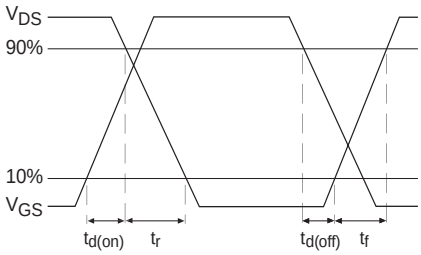


Fig 10b. Switching Time Waveforms

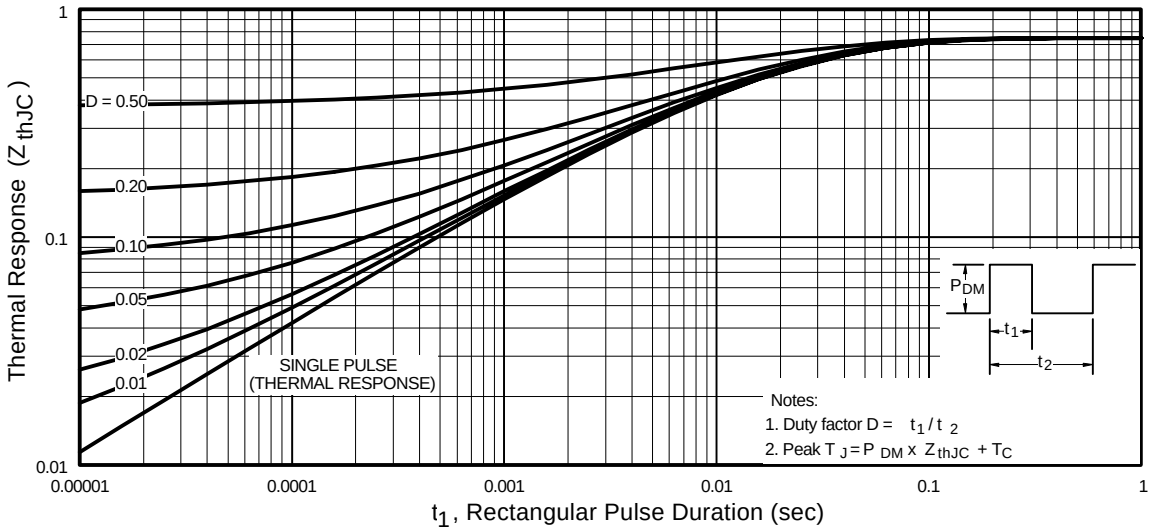


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

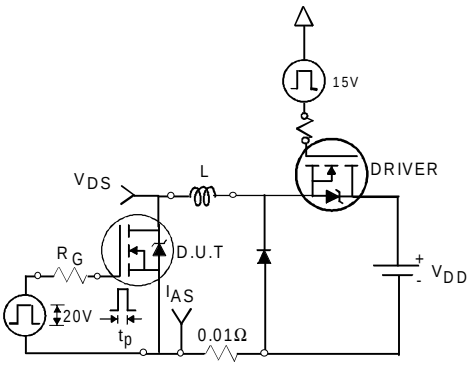


Fig 12a. Unclamped Inductive Test Circuit

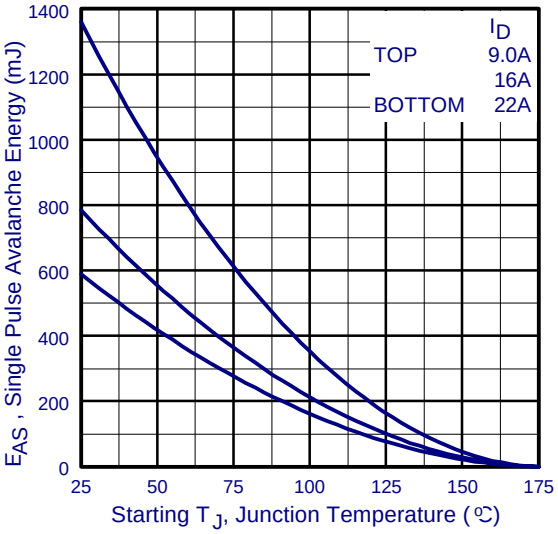


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

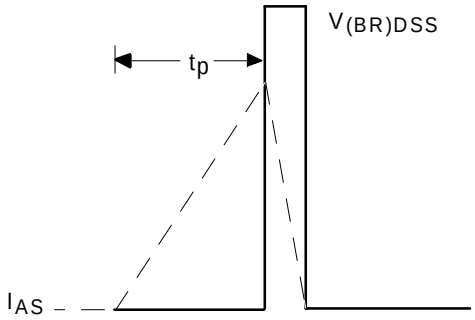


Fig 12b. Unclamped Inductive Waveforms

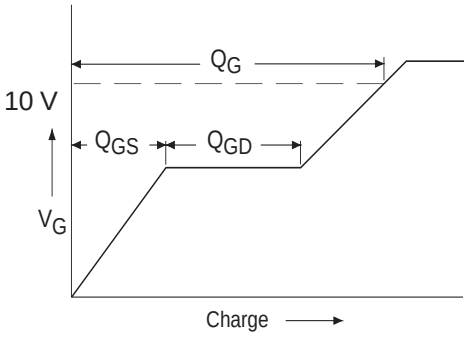


Fig 13a. Basic Gate Charge Waveform

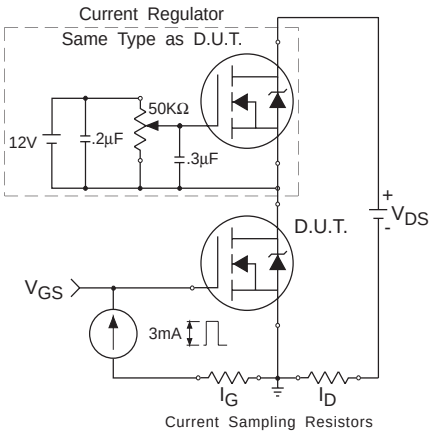
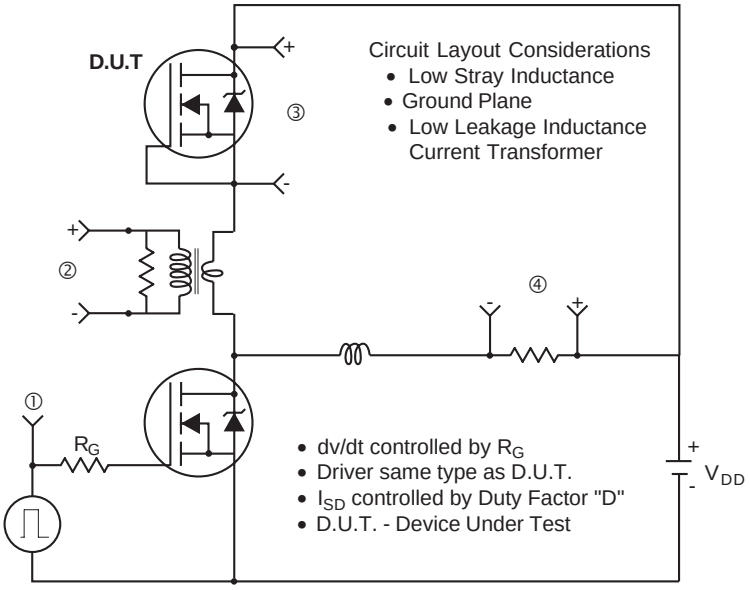
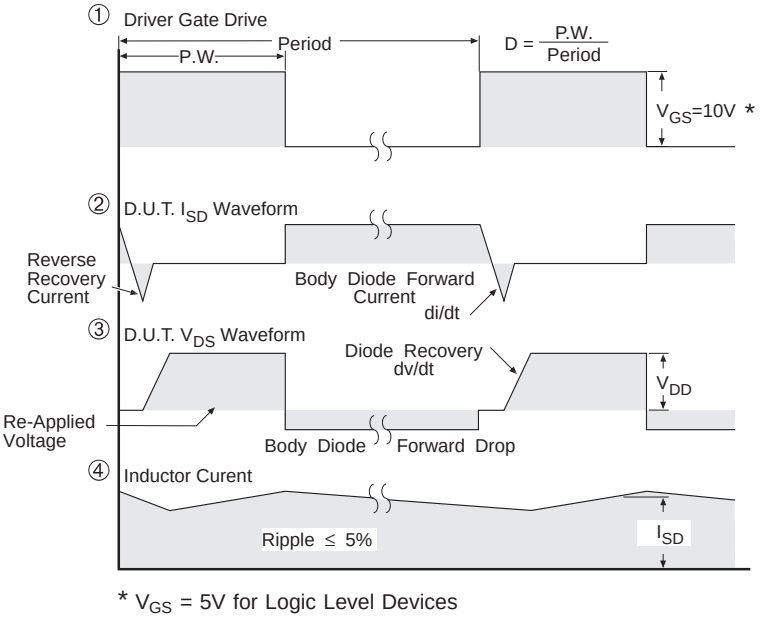


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

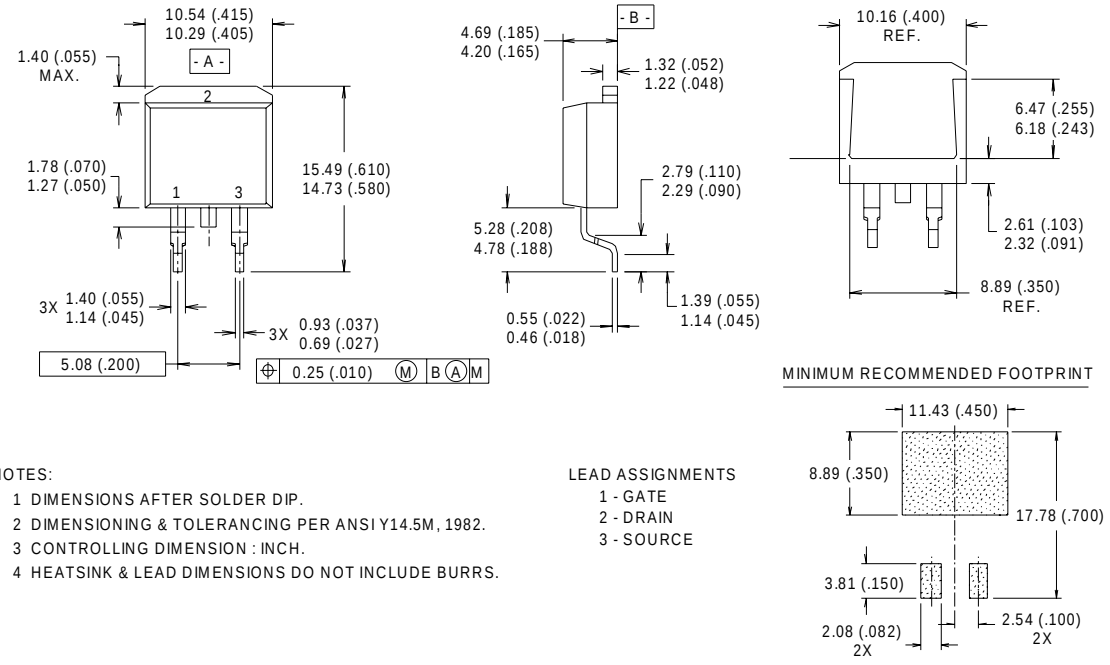




* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

D²Pak Package Outline



NOTES:

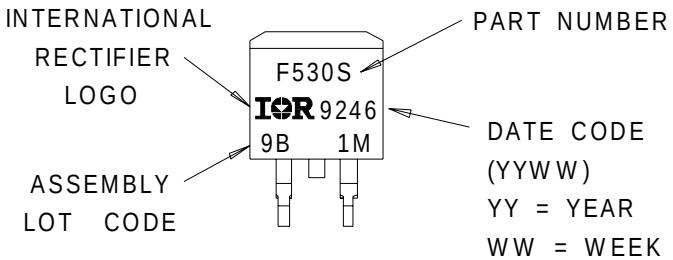
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

1 - GATE
2 - DRAIN
3 - SOURCE

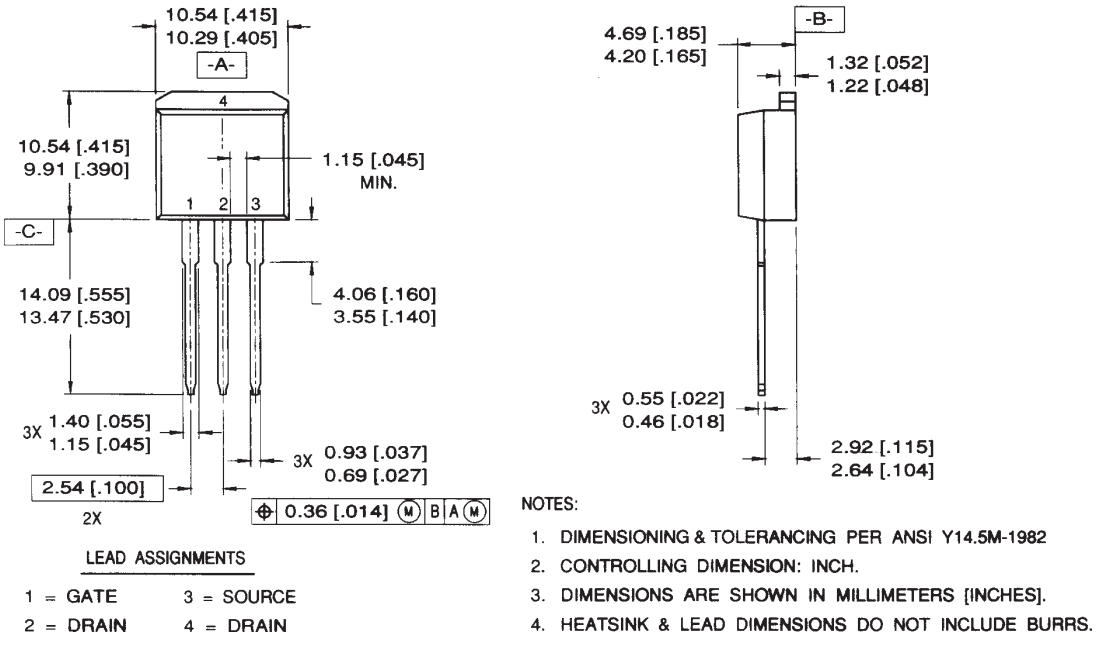
Part Marking Information

D²Pak



Package Outline

TO-262 Outline



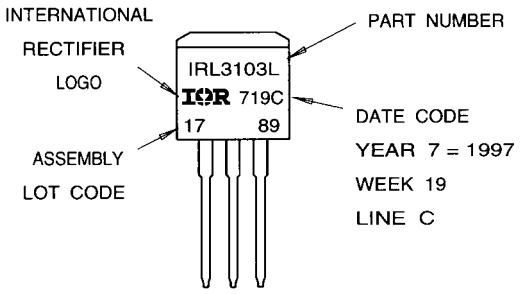
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

Part Marking Information

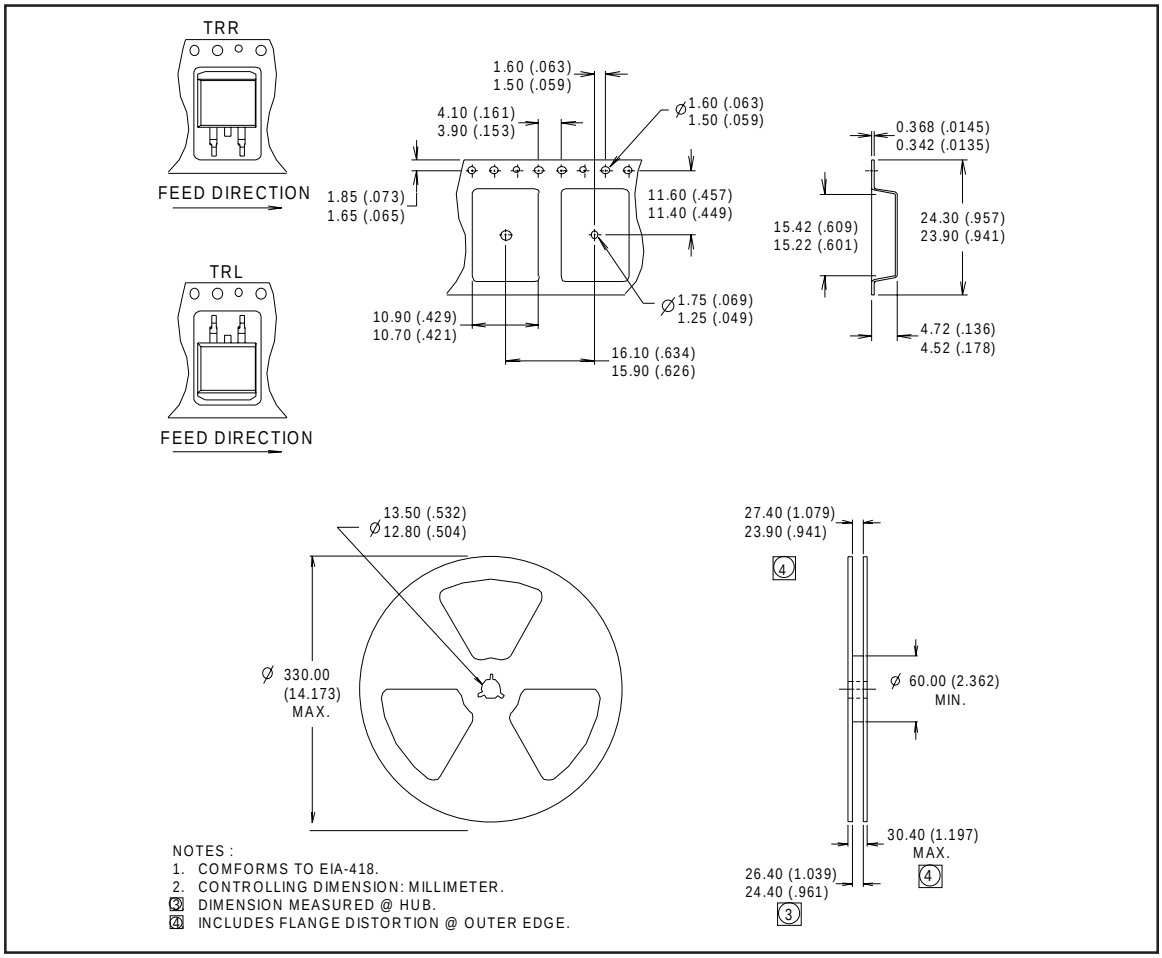
TO-262

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



Tape & Reel Information

D^2Pak



NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371

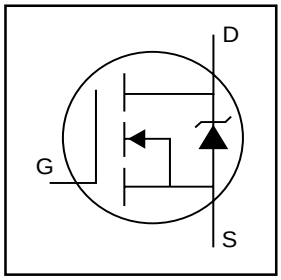
International
IOR Rectifier

PD - 93962

IRFP3415

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 150V

$R_{DS(on)}$ = 0.042Ω

I_D = 43A

Description

Fifth Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	43	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	30	
I_{DM}	Pulsed Drain Current ①	150	
P_D @T_C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	590	mJ
I_{AR}	Avalanche Current①	22	A
E_{AR}	Repetitive Avalanche Energy①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

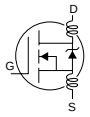
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

8/16/00

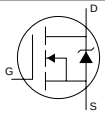
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.17	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.042	Ω	V_{GS} = 10V, I_D = 22A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	19	—	—	S	V_{DS} = 50V, I_D = 22A
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 150V, V_{GS} = 0V
		—	—	250		V_{DS} = 120V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	200	nC	I_D = 22A
Q_{gs}	Gate-to-Source Charge	—	—	17		V_{DS} = 120V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	98		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	V_{DD} = 75V
t_r	Rise Time	—	55	—		I_D = 22A
$t_{d(off)}$	Turn-Off Delay Time	—	71	—		R_G = 2.5Ω
t_f	Fall Time	—	69	—		R_D = 3.3Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	2400	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	640	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	340	—		f = 1.0MHz, See Fig. 5



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	43	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	150		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 22A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	260	390	ns	T_J = 25°C, I_F = 22A
Q_{rr}	Reverse RecoveryCharge	—	2.2	3.3	µC	di/dt = 100A/µs ④



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = 25V, starting T_J = 25°C, L = 2.4mH R_G = 25Ω, I_{AS} = 22A. (See Figure 12)

③ I_{SD} ≤ 22A, di/dt ≤ 820A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

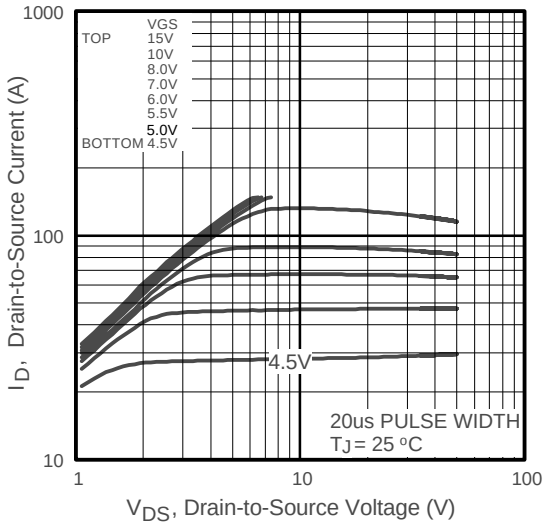


Fig 1. Typical Output Characteristics

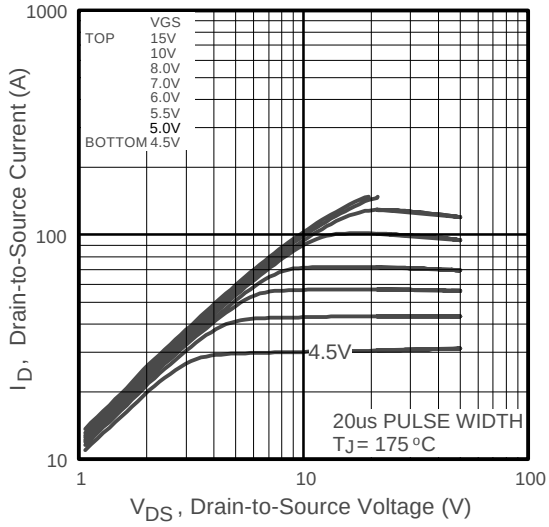


Fig 2. Typical Output Characteristics

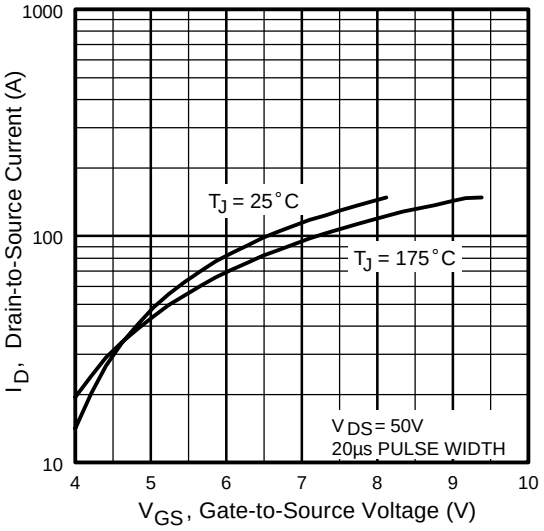


Fig 3. Typical Transfer Characteristics

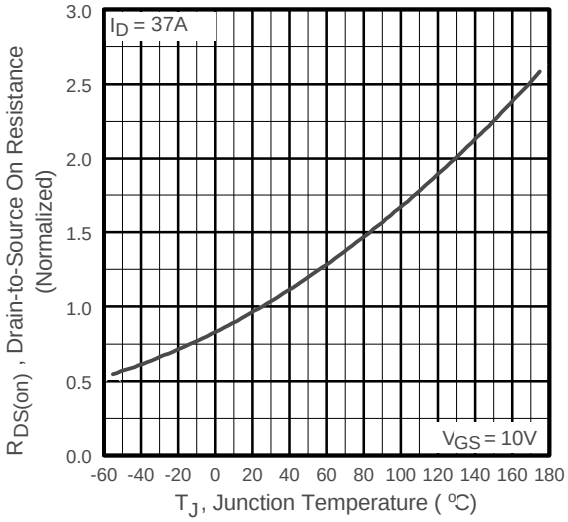


Fig 4. Normalized On-Resistance Vs. Temperature

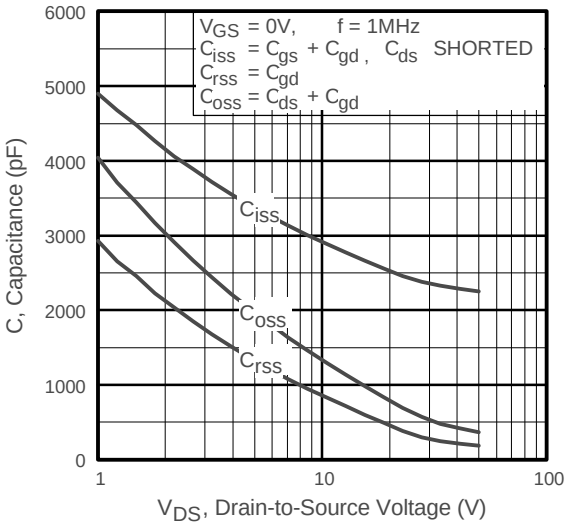


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

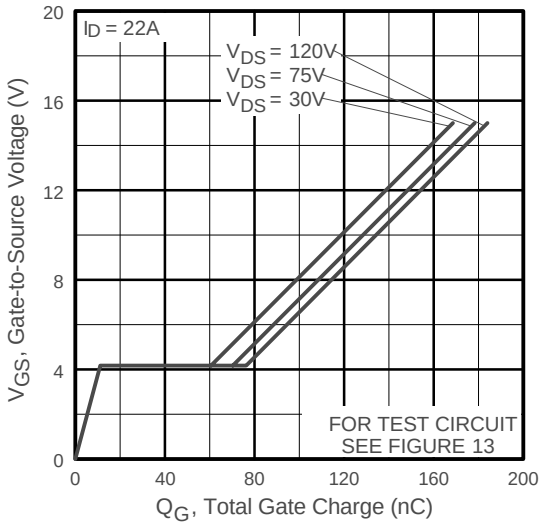


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

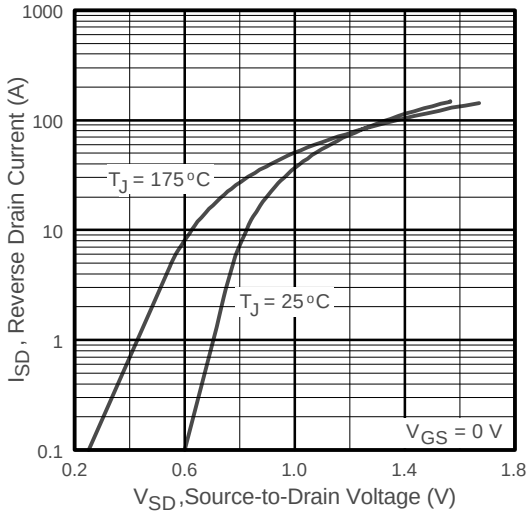


Fig 7. Typical Source-Drain Diode Forward Voltage

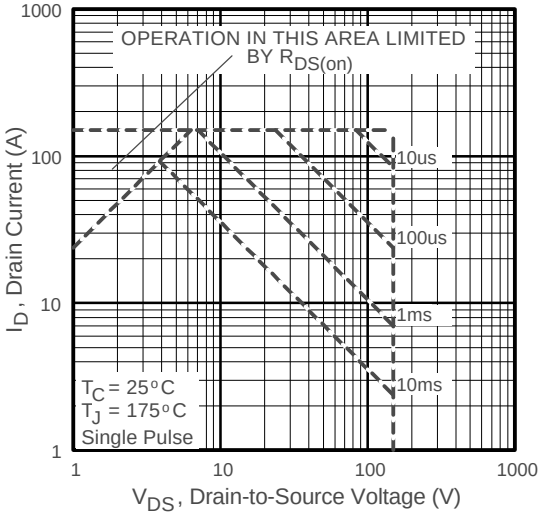


Fig 8. Maximum Safe Operating Area

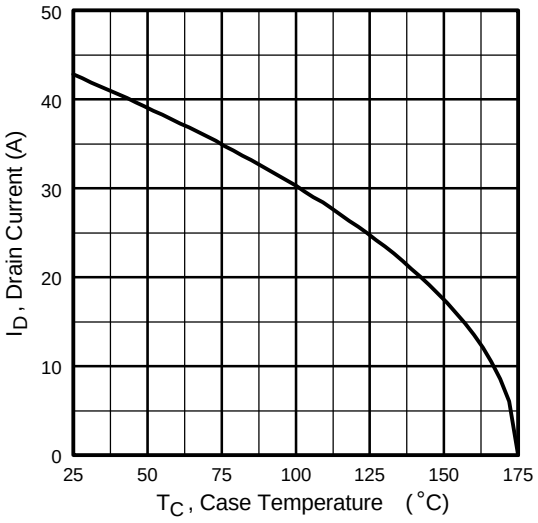


Fig 9. Maximum Drain Current Vs. Case Temperature

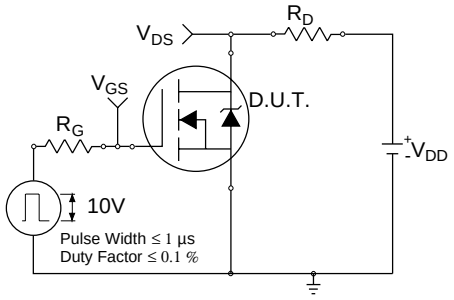


Fig 10a. Switching Time Test Circuit

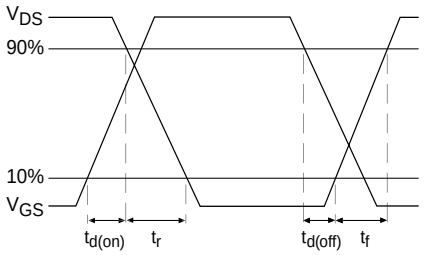


Fig 10b. Switching Time Waveforms

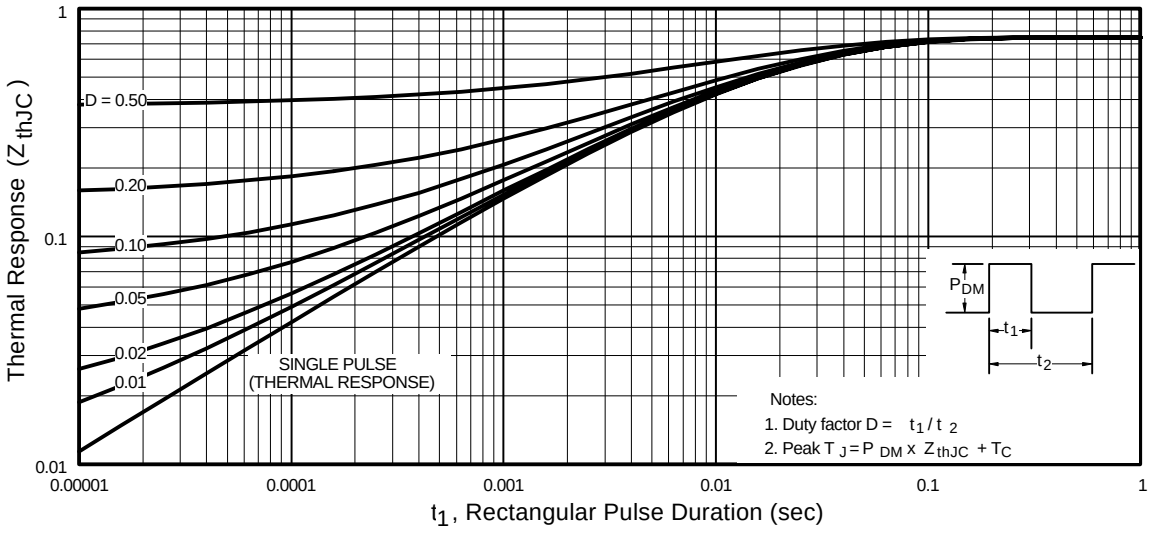


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

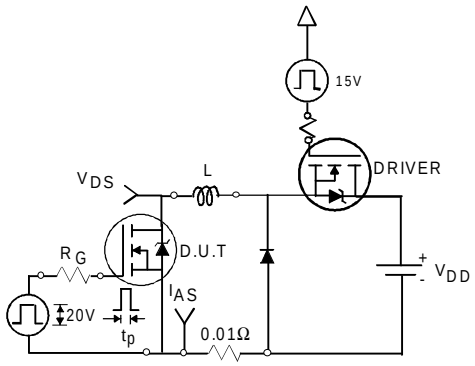


Fig 12a. Unclamped Inductive Test Circuit

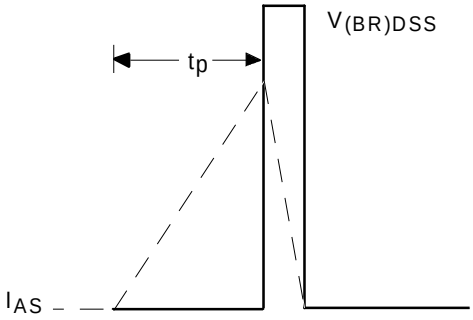


Fig 12b. Unclamped Inductive Waveforms

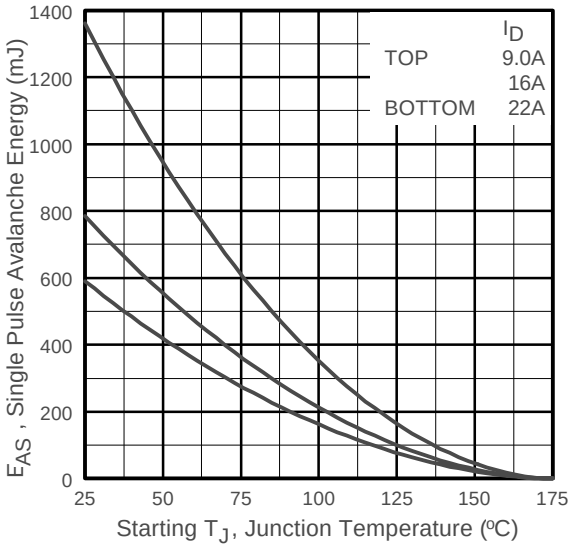


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

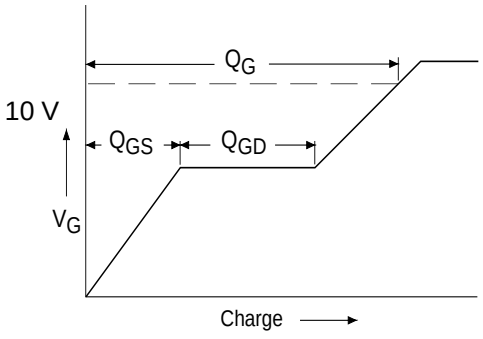


Fig 13a. Basic Gate Charge Waveform

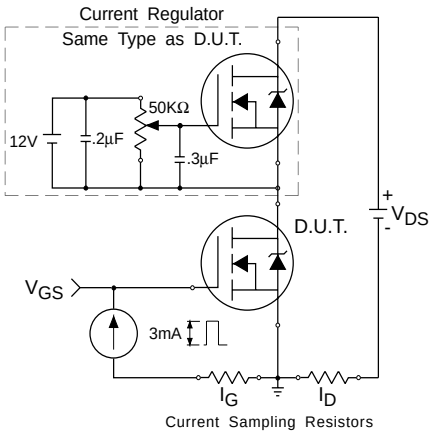
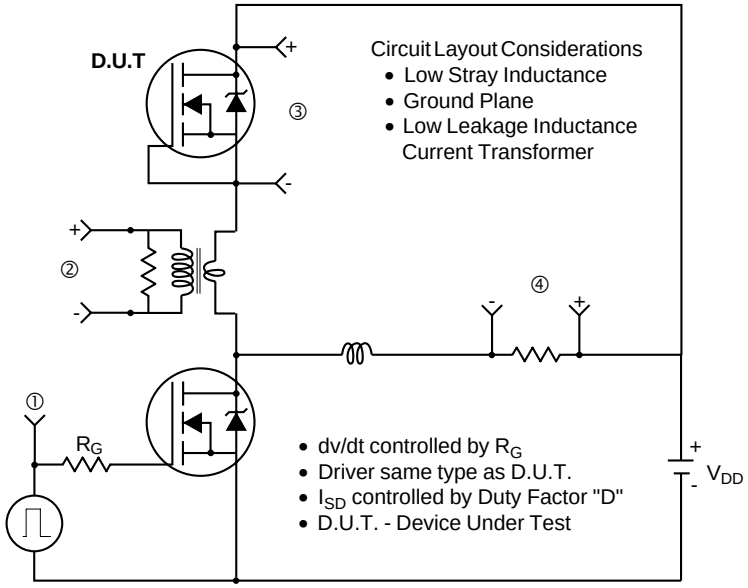
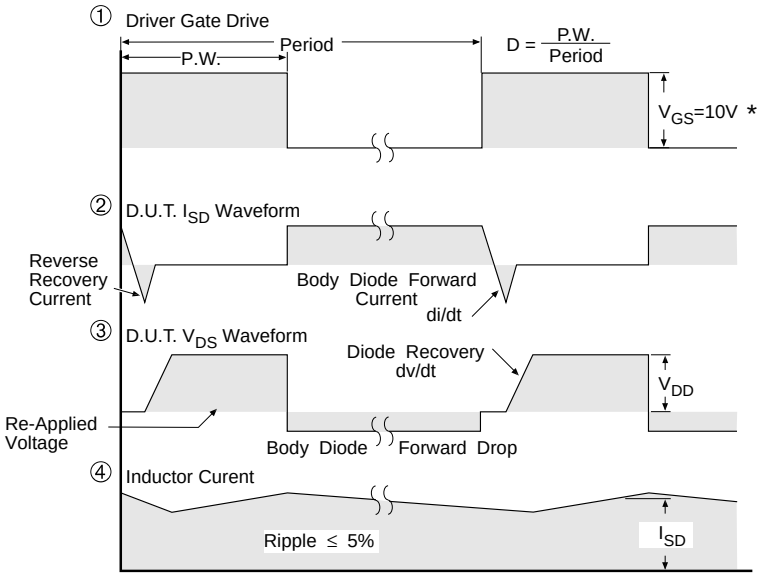


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



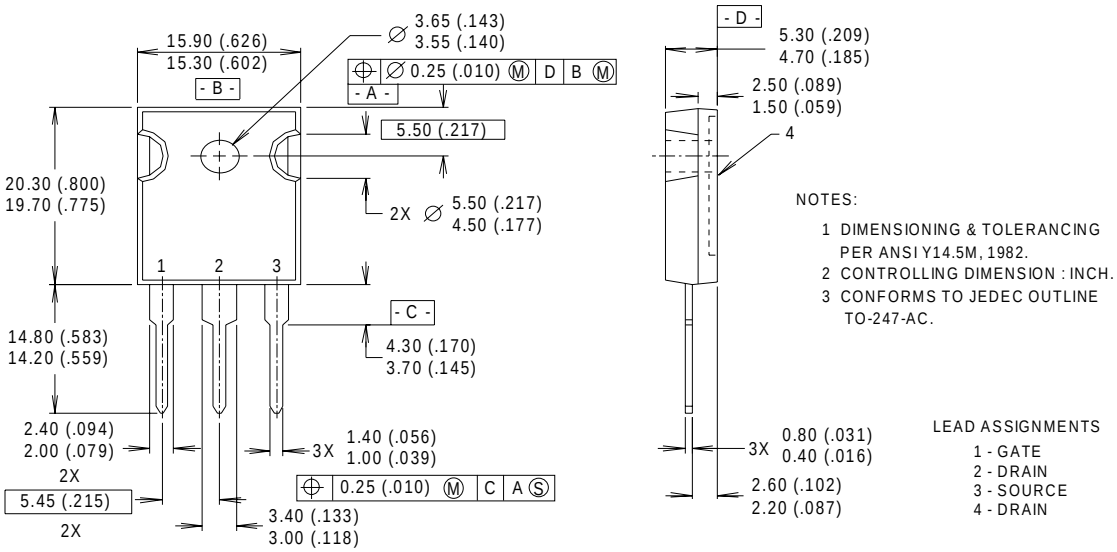


* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

TO - 247 Package Outline

Dimensions are shown in millimeters (inches)



International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN: 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 8/00

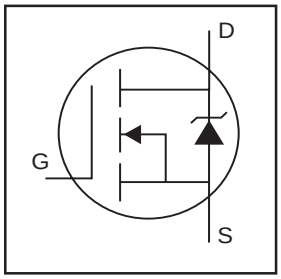
PD - 91309

International
IOR Rectifier

IRF3710

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 100V

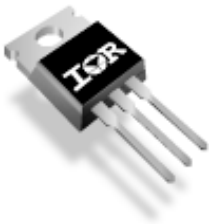
$R_{DS(on)}$ = 23mΩ

I_D = 57A

Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	57	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	40	
I_{DM}	Pulsed Drain Current ①	180	
P_D @T_C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.4	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current①	28	A
E_{AR}	Repetitive Avalanche Energy①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.74	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	23	mΩ	V_{GS} = 10V, I_D =28A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	35	—	—	S	V_{DS} = 25V, I_D = 28A④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 100V, V_{GS} = 0V
		—	—	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	140	nC	I_D = 28A
Q_{gs}	Gate-to-Source Charge	—	—	24		V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	44		V_{GS} = 10V, See Fig. 6 and 13
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	V_{DD} = 50V
t_r	Rise Time	—	43	—		I_D = 28A
$t_{d(off)}$	Turn-Off Delay Time	—	49	—		R_G = 2.5Ω
t_f	Fall Time	—	40	—		V_{GS} = 10V, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	3230	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	420	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	81	—		f = 1.0MHz, See Fig. 5
E_{AS}	Single Pulse Avalanche Energy②	—	1160⑤	340⑥	mJ	I_{AS} = 28A, L = 0.86mH

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	57	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)①	—	—	180		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C, I_S = 28A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	130	200	ns	T_J = 25°C, I_F = 28A
Q_{rr}	Reverse Recovery Charge	—	740	1100	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 0.86mH R_G = 25Ω, I_{AS} = 28A, V_{GS}=10V (See Figure 12)

③ I_{SD} ≤ 28A, di/dt ≤ 370A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ This is a typical value at device destruction and represents operation outside rated limits.

⑥ This is a calculated value limited to T_J = 175°C .

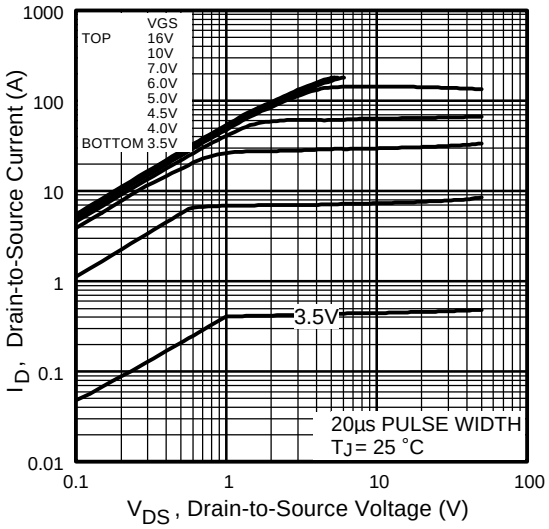


Fig 1. Typical Output Characteristics

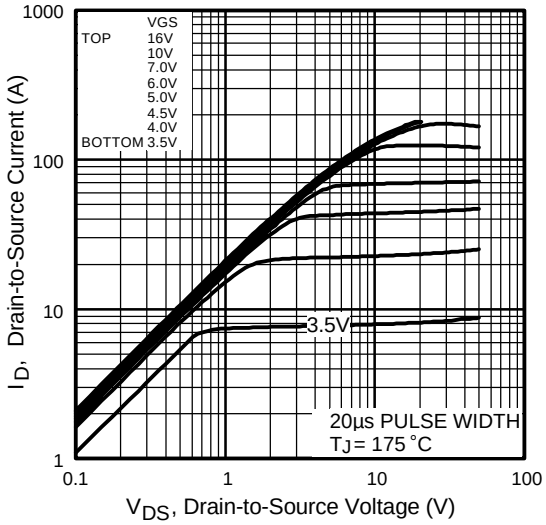


Fig 2. Typical Output Characteristics

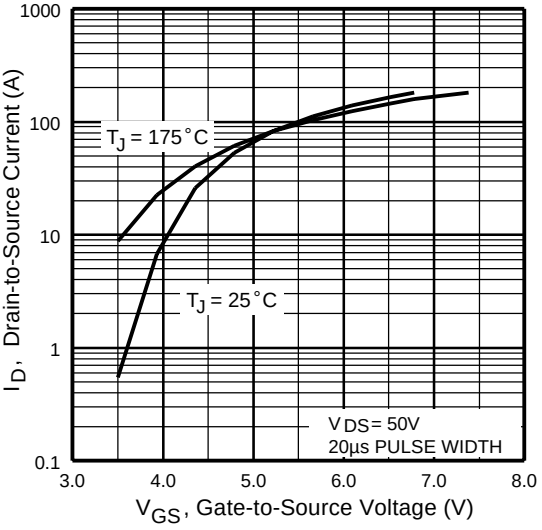


Fig 3. Typical Transfer Characteristics

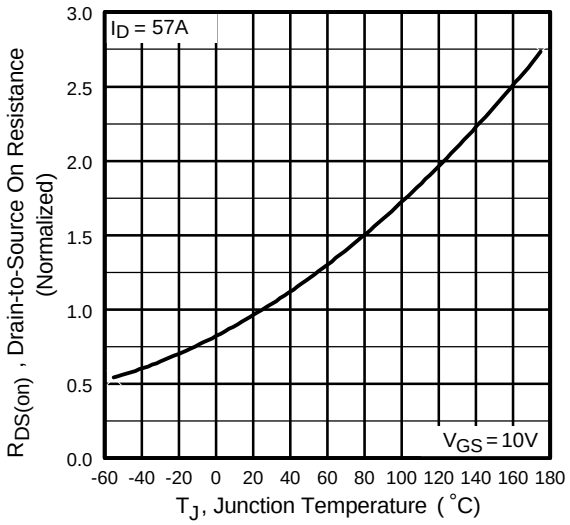


Fig 4. Normalized On-Resistance Vs. Temperature

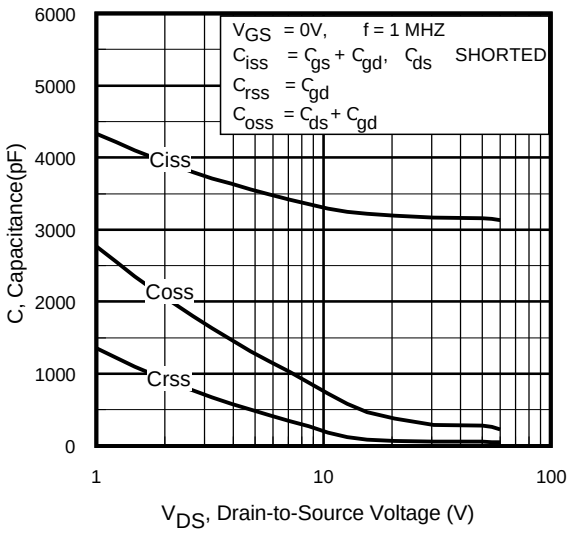


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

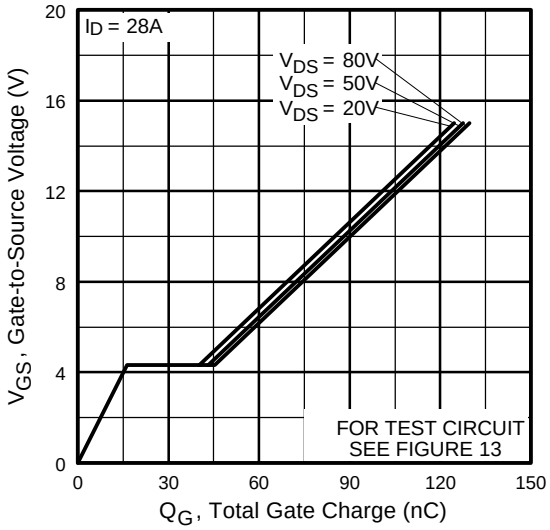


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

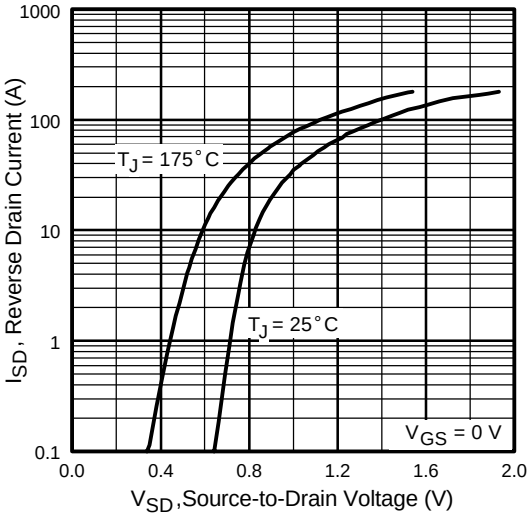


Fig 7. Typical Source-Drain Diode Forward Voltage

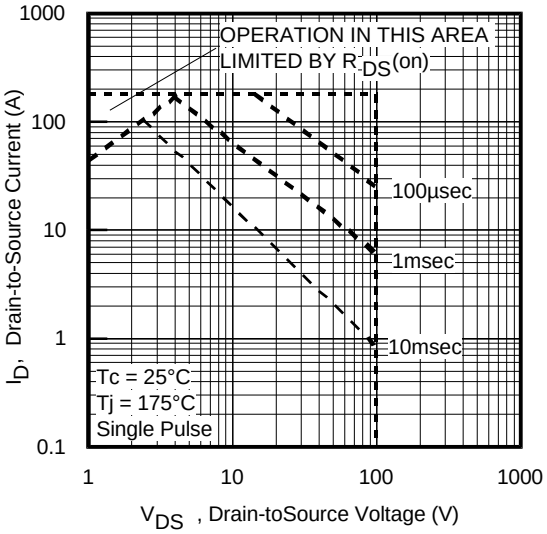


Fig 8. Maximum Safe Operating Area

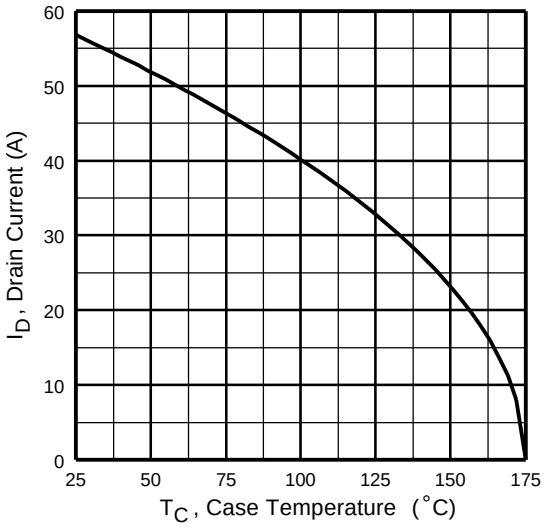


Fig 9. Maximum Drain Current Vs. Case Temperature

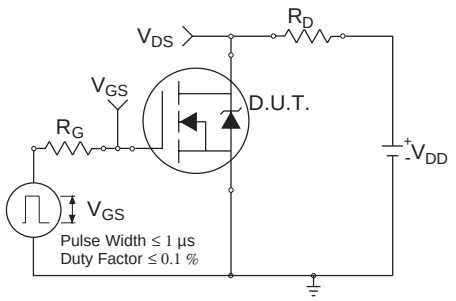


Fig 10a. Switching Time Test Circuit

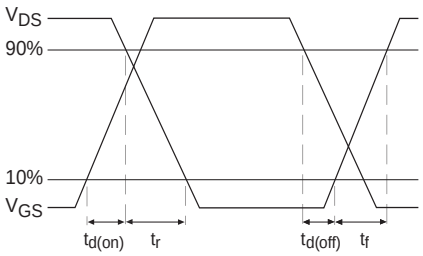


Fig 10b. Switching Time Waveforms

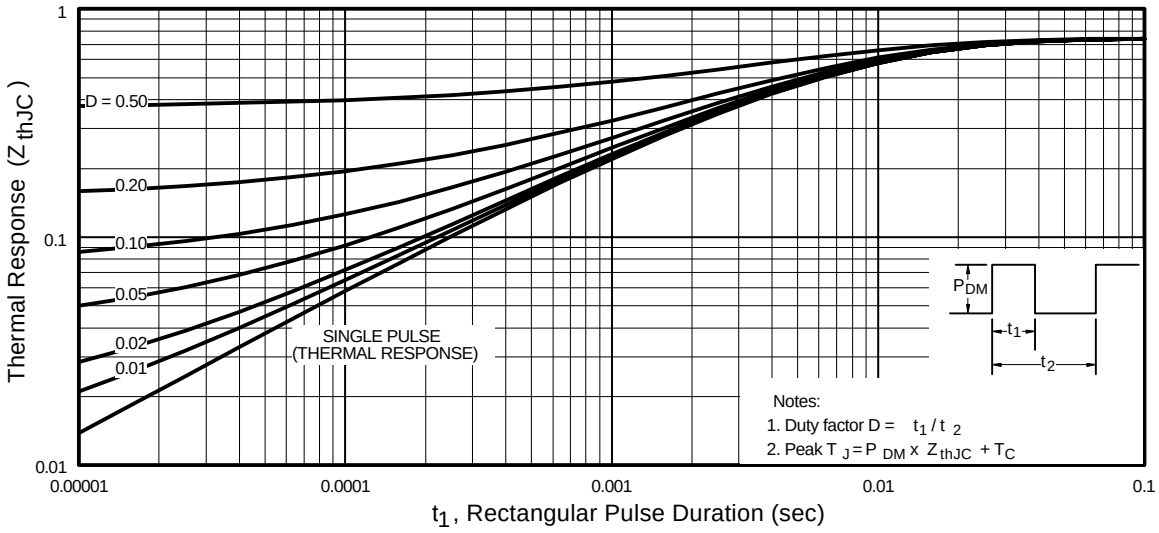


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

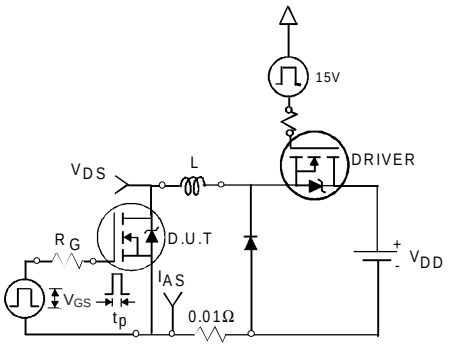


Fig 12a. Unclamped Inductive Test Circuit

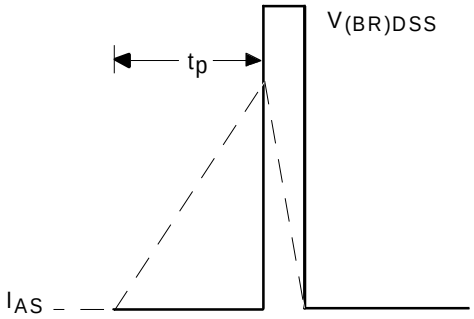


Fig 12b. Unclamped Inductive Waveforms

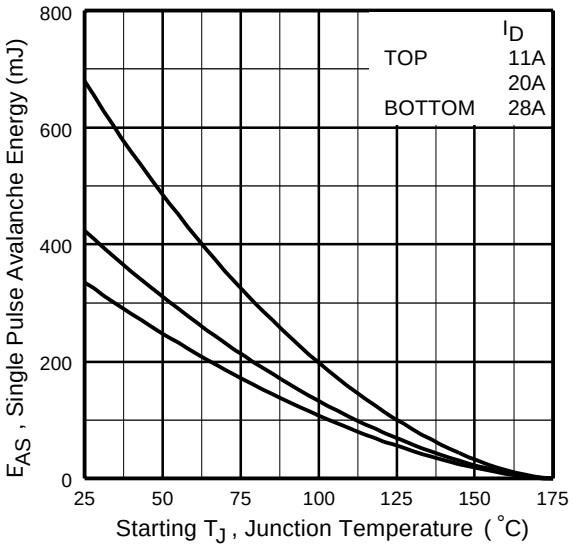


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

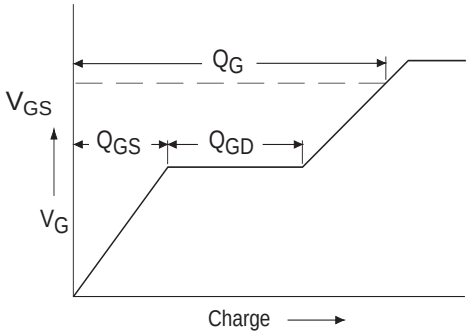


Fig 13a. Basic Gate Charge Waveform

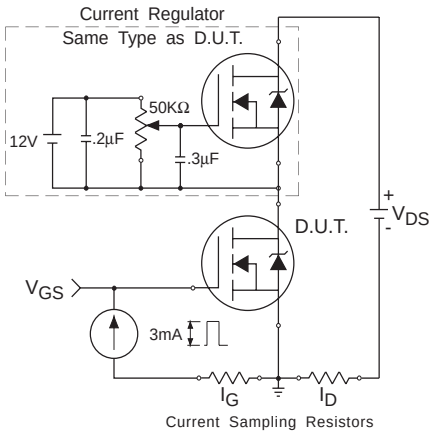
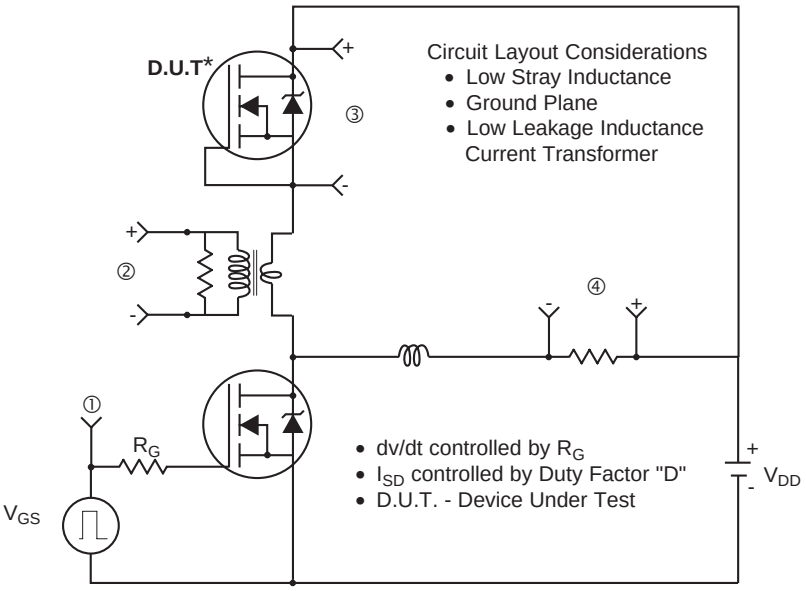
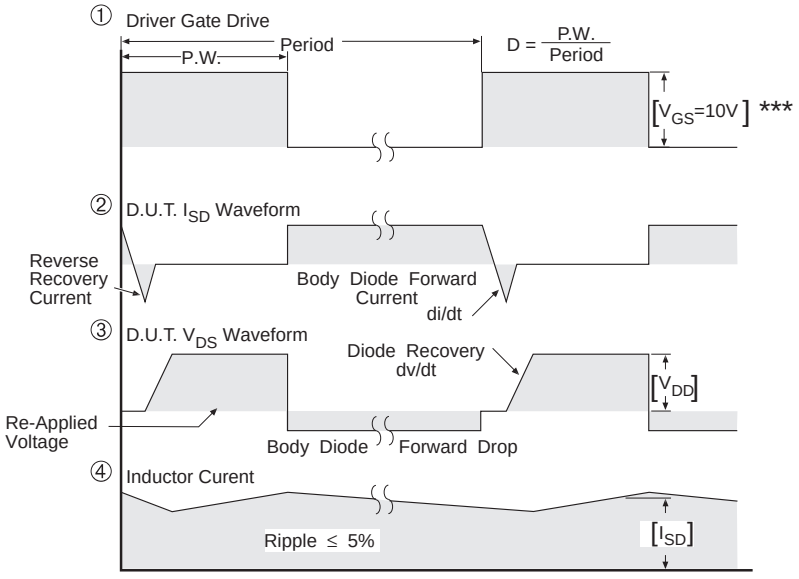


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



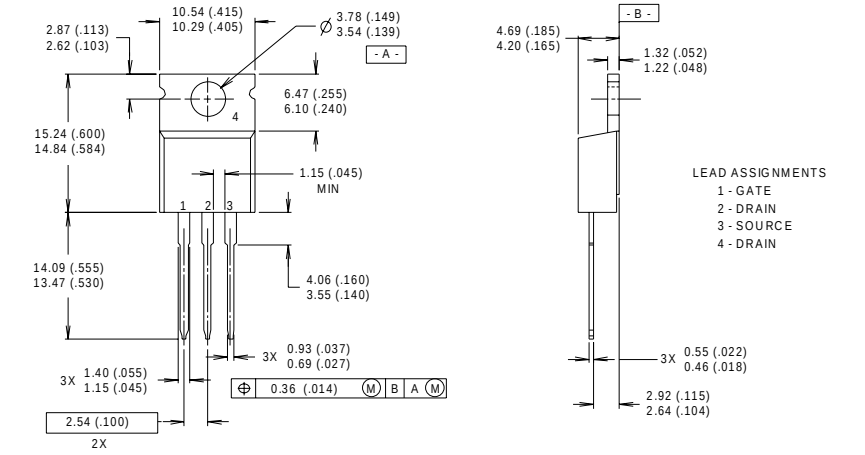
*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

Package Outline

TO-220AB

Dimensions are shown in millimeters (inches)



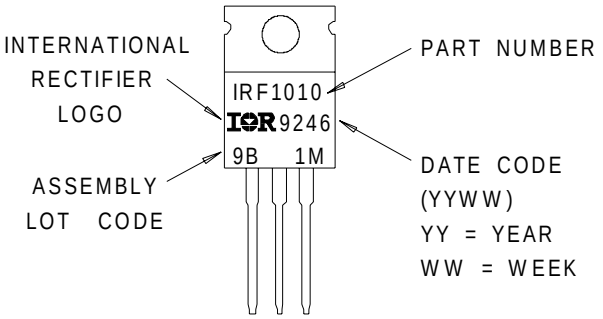
NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

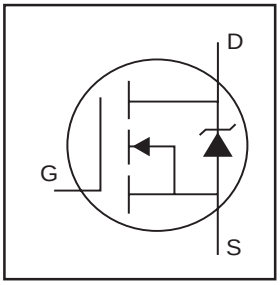
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.3/01

International
IOR Rectifier

IRF3710S/L

HEXFET® Power MOSFET

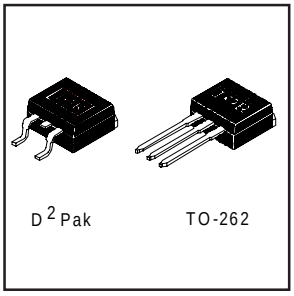
- Advanced Process Technology
- Surface Mount (IRF3710S)
- Low-profile through-hole (IRF3710L)
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 100V

$R_{DS(on)}$ = 0.025Ω

I_D = 57A



Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D^2Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D^2Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRF3710L) is available for low-profile applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V⑤	57	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V⑤	40	
I_{DM}	Pulsed Drain Current ①⑤	180	
P_D @T_A = 25°C	Power Dissipation	3.8	W
P_D @T_C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑤	530	mJ
I_{AR}	Avalanche Current①	28	A
E_{AR}	Repetitive Avalanche Energy①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

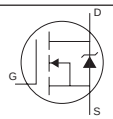
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted,steady-state)**	——	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C, I_D = 1mA⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.025	Ω	V_{GS} = 10V, I_D = 28A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	20	—	—	S	V_{DS} = 25V, I_D = 28A⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 100V, V_{GS} = 0V
		—	—	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	190	nC	I_D = 28A
Q_{gs}	Gate-to-Source Charge	—	—	26		V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	82		V_{GS} = 10V, See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	V_{DD} = 50V
t_r	Rise Time	—	59	—		I_D = 28A
$t_{d(off)}$	Turn-Off Delay Time	—	58	—		R_G = 2.5Ω
t_f	Fall Time	—	48	—		R_D = 1.7Ω, See Fig. 10 ④⑤
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	3000	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	640	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	330	—		f = 1.0MHz, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	57	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑤	—	—	180		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 28A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	210	320	ns	T_J = 25°C, I_F = 28A
Q_{rr}	Reverse RecoveryCharge	—	1.7	2.6	µC	di/dt = 100A/µs ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = 25V, starting T_J = 25°C, L = 1.4mH R_G = 25Ω, I_{AS} = 28A. (See Figure 12)

③ I_{SD} ≤ 28A, di/dt ≤ 460A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ Uses IRF3710 data and test conditions

** When mounted on FR-4 board using minimum recommended footprint.
For recommended footprint and soldering techniques refer to application note #AN-994.

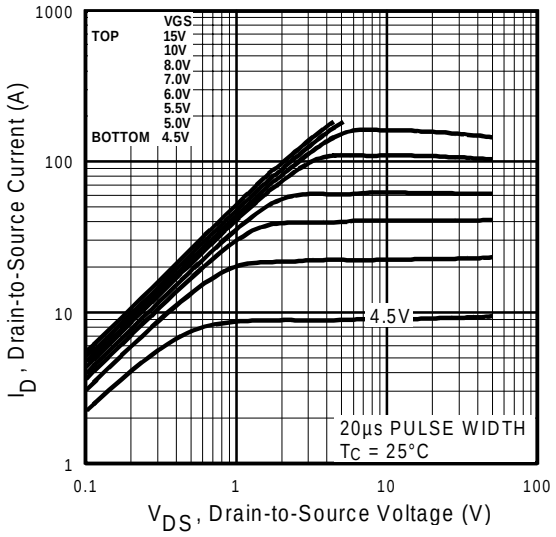


Fig 1. Typical Output Characteristics

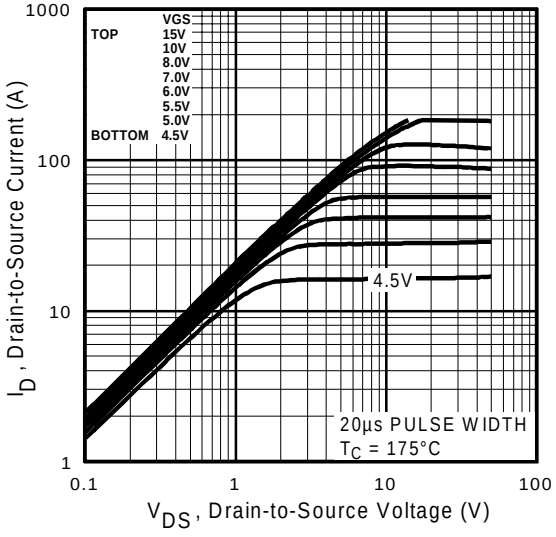


Fig 2. Typical Output Characteristics

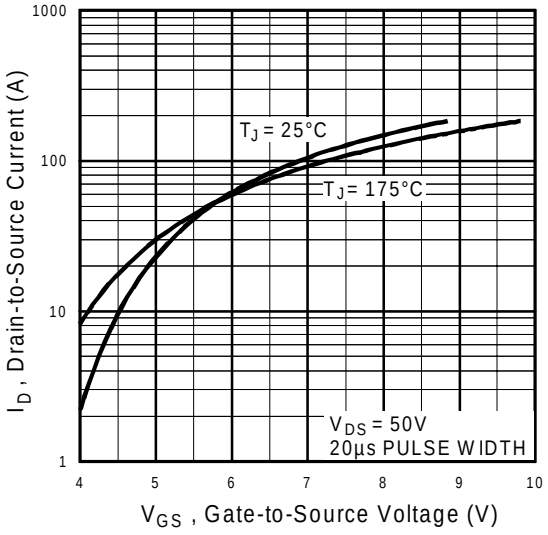


Fig 3. Typical Transfer Characteristics

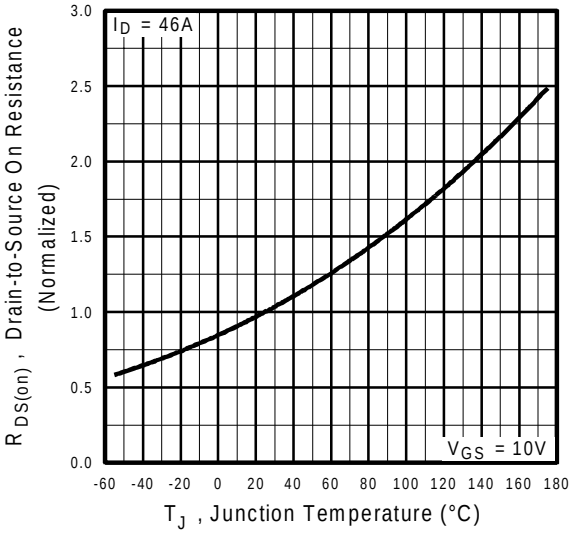


Fig 4. Normalized On-Resistance Vs. Temperature

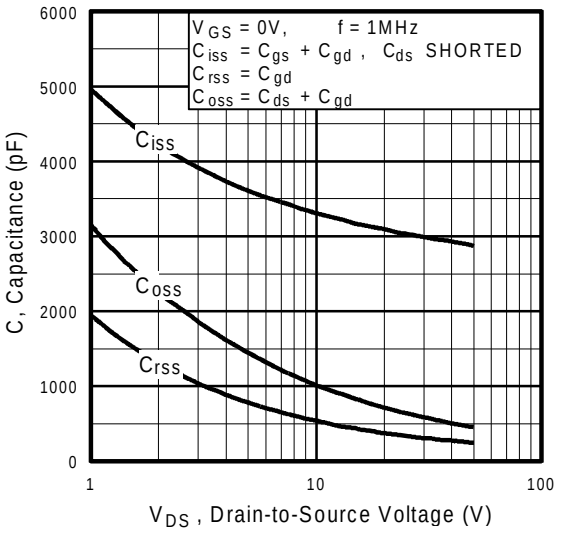


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

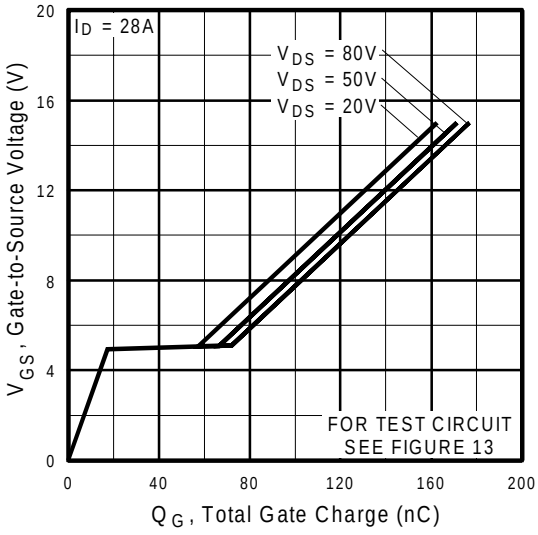


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

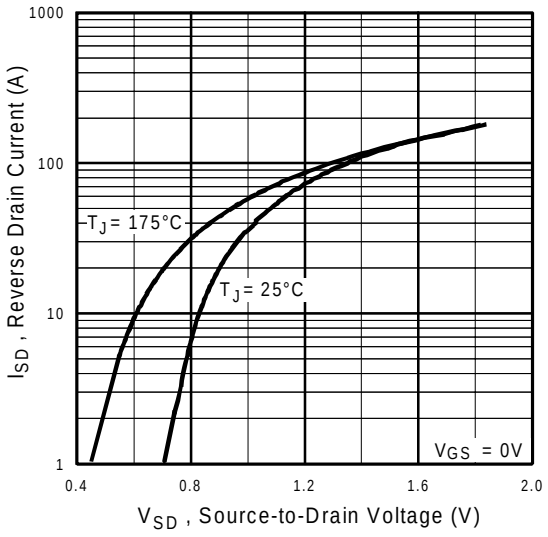


Fig 7. Typical Source-Drain Diode Forward Voltage

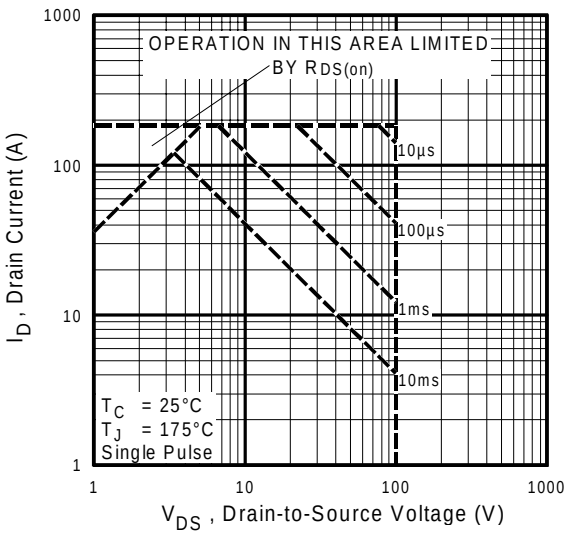


Fig 8. Maximum Safe Operating Area

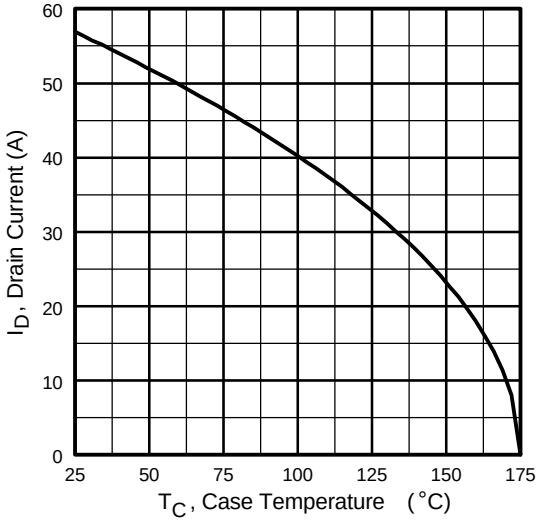


Fig 9. Maximum Drain Current Vs. Case Temperature

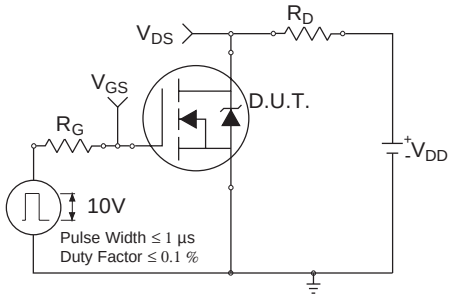


Fig 10a. Switching Time Test Circuit

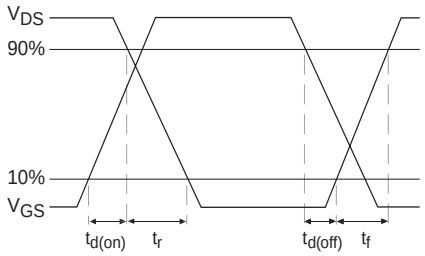


Fig 10b. Switching Time Waveforms

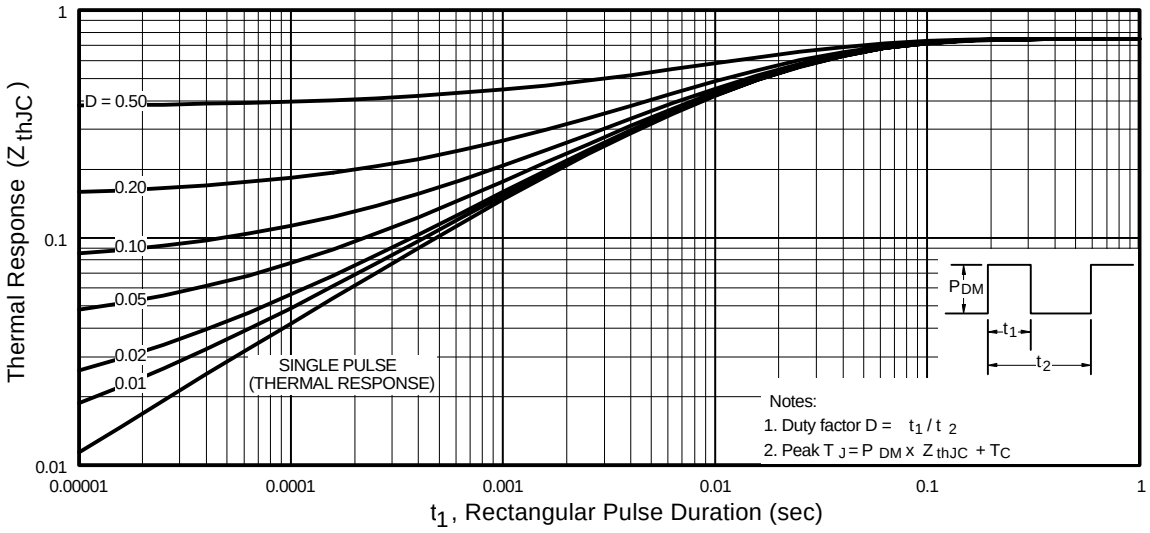


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

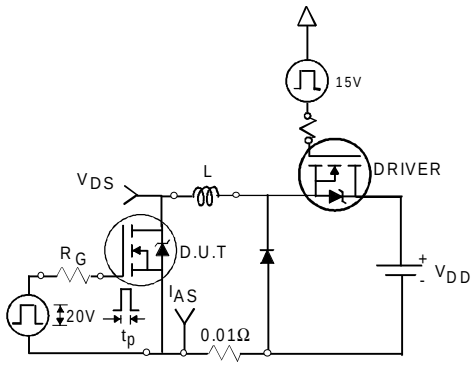


Fig 12a. Unclamped Inductive Test Circuit

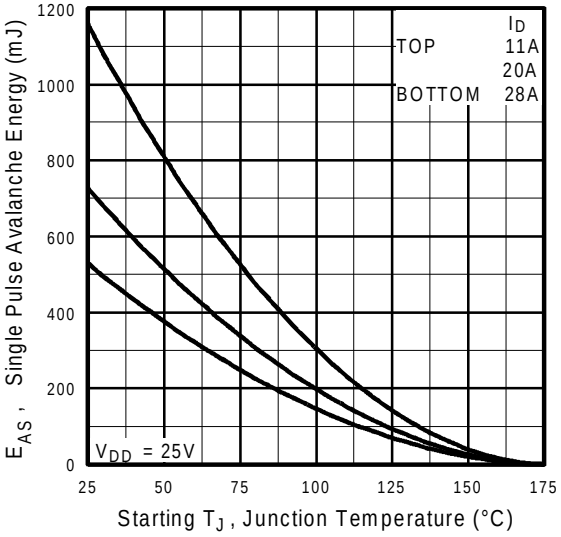


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

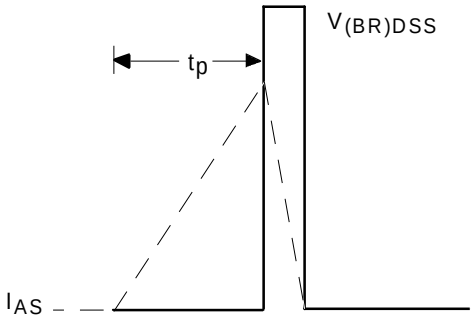


Fig 12b. Unclamped Inductive Waveforms

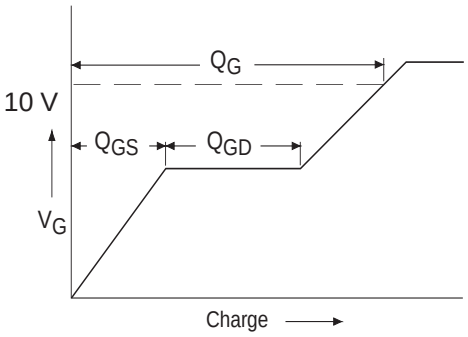


Fig 13a. Basic Gate Charge Waveform

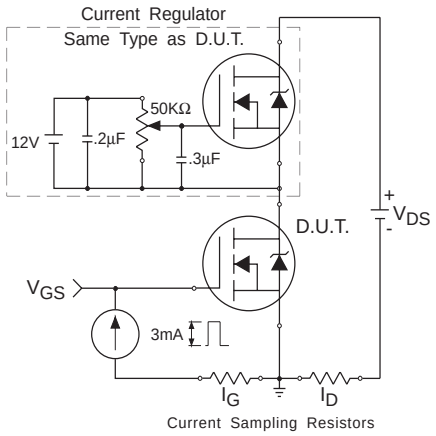
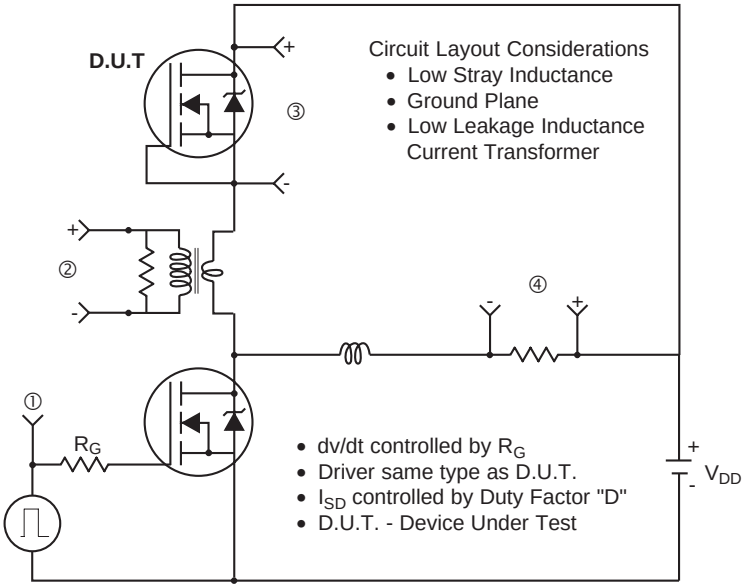
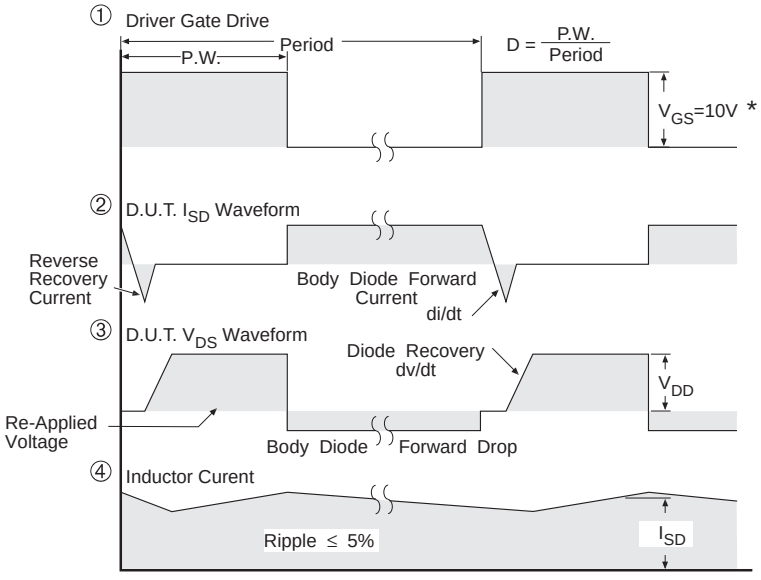


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

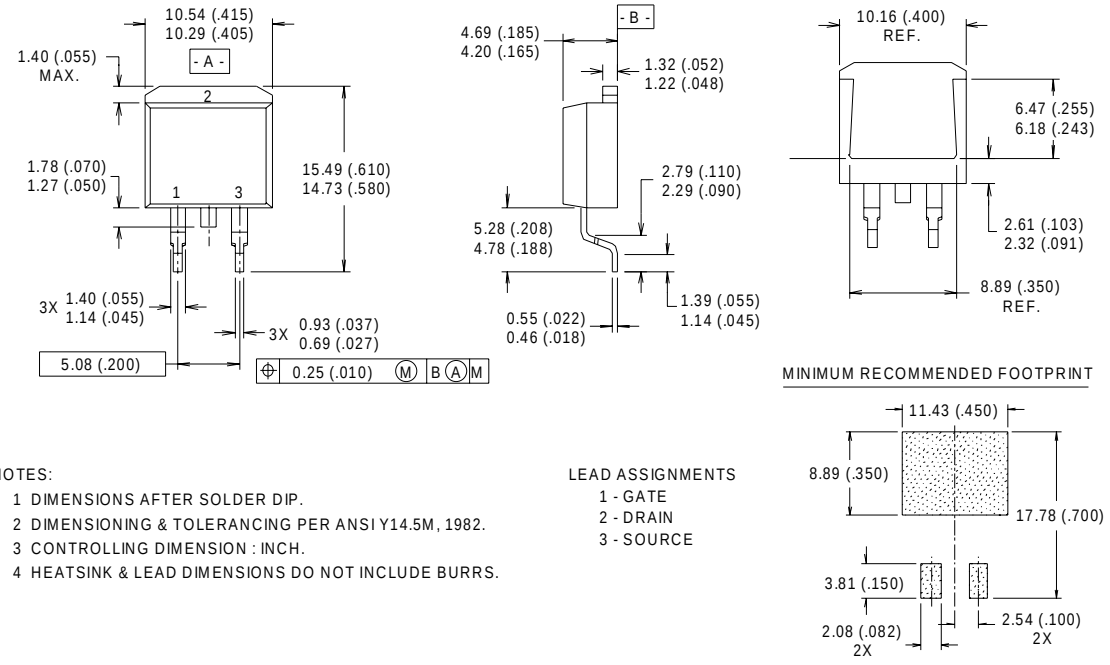




* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

D²Pak Package Outline



NOTES:

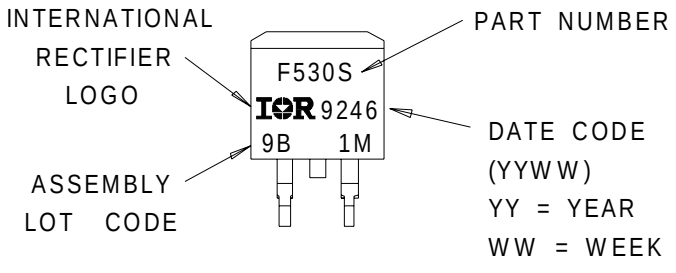
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

1 - GATE
2 - DRAIN
3 - SOURCE

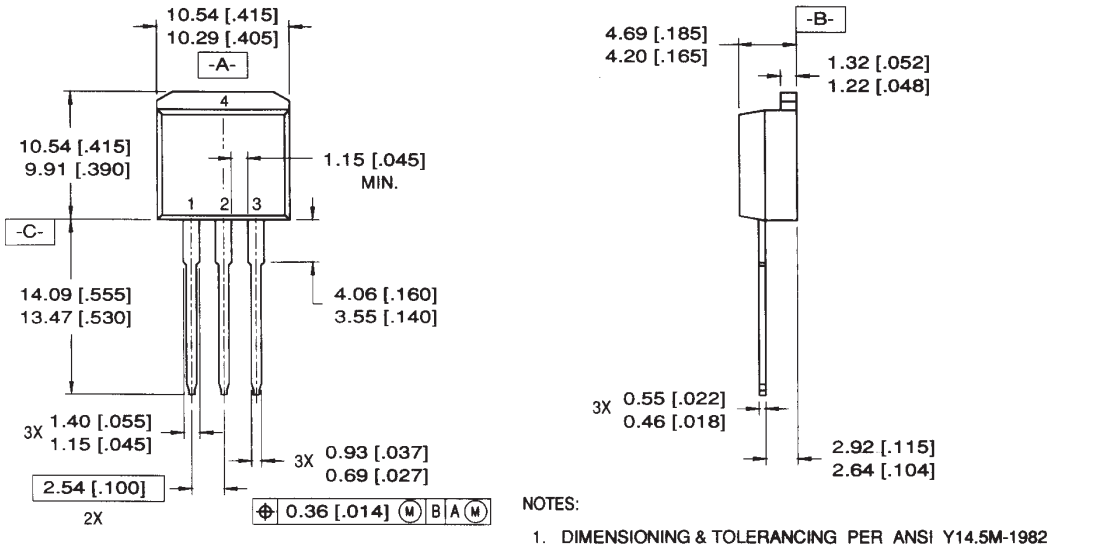
Part Marking Information

D²Pak



Package Outline

TO-262 Outline



LEAD ASSIGNMENTS

1 = GATE 3 = SOURCE
2 = DRAIN 4 = DRAIN

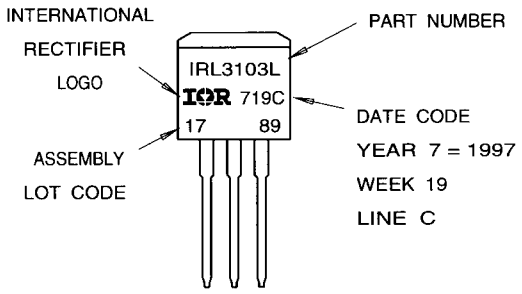
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

Part Marking Information

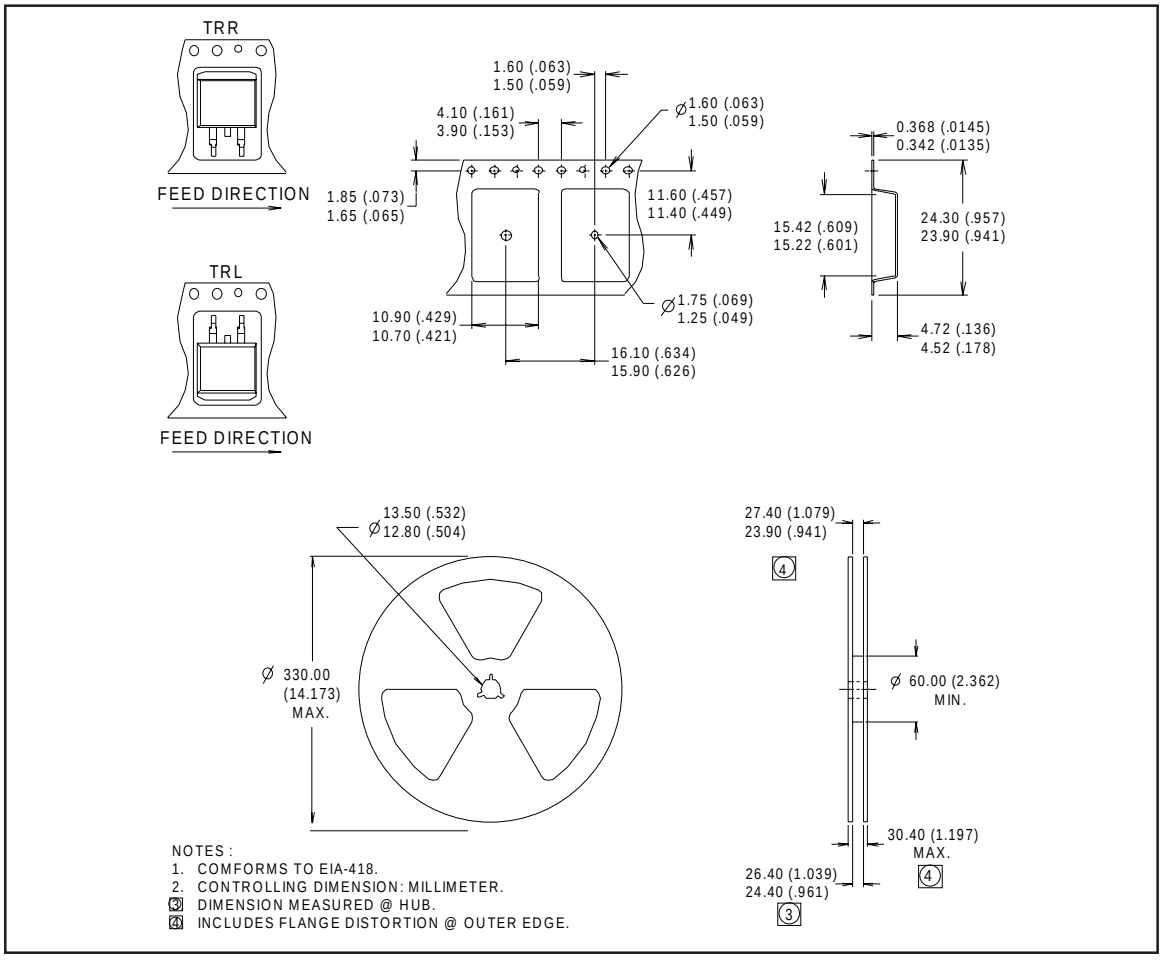
TO-262

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



Tape & Reel Information

D^2Pak



NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371

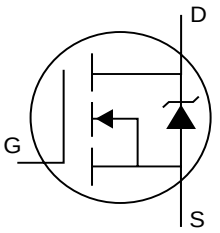
International
IOR Rectifier

PD - 93912

IRFPS3810

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 100V

$R_{DS(on)}$ = 0.010Ω

I_D = 141A⑥

Description

The HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.



Super-247™

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	141⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	99⑥	
I_{DM}	Pulsed Drain Current ①	520	
P_D @T_C = 25°C	Power Dissipation	441	W
	Linear Derating Factor	2.9	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy②	1970	mJ
I_{AR}	Avalanche Current①	78	A
E_{AR}	Repetitive Avalanche Energy①	38	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.1	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.34	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

02/26/01

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.010	Ω	V_{GS} = 10V, I_D = 85A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	V_{DS} = 10V, I_D = 250µA
g_{fs}	Forward Transconductance	50	—	—	S	V_{DS} = 50V, I_D = 78A
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 100V, V_{GS} = 0V
		—	—	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -30V
Q_g	Total Gate Charge	—	270	410	nC	I_D = 78A
Q_{gs}	Gate-to-Source Charge	—	58	87		V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	150	230		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	—	22	—	ns	V_{DD} = 50V
t_r	Rise Time	—	170	—		I_D = 78A
$t_{d(off)}$	Turn-Off Delay Time	—	44	—		R_G = 1.03Ω
t_f	Fall Time	—	68	—		V_{GS} = 10V ④
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	13	—		
C_{iss}	Input Capacitance	—	6880	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	2420	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	900	—		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	10610	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	1170	—		V_{GS} = 0V, V_{DS} = 80V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	—	2130	—		V_{GS} = 0V, V_{DS} = 0V to 80V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	141⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	520		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 78A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	210	320	ns	T_J = 25°C, I_F = 78A
Q_{rr}	Reverse RecoveryCharge	—	1920	2880	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 0.65mH R_G = 25Ω, I_{AS} = 78A. (See Figure 12)

③ I_{SD} ≤ 78A, di/dt ≤ 380A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 105A.

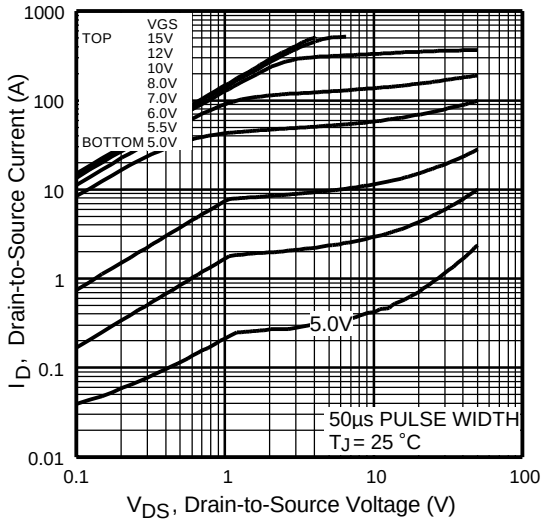


Fig 1. Typical Output Characteristics

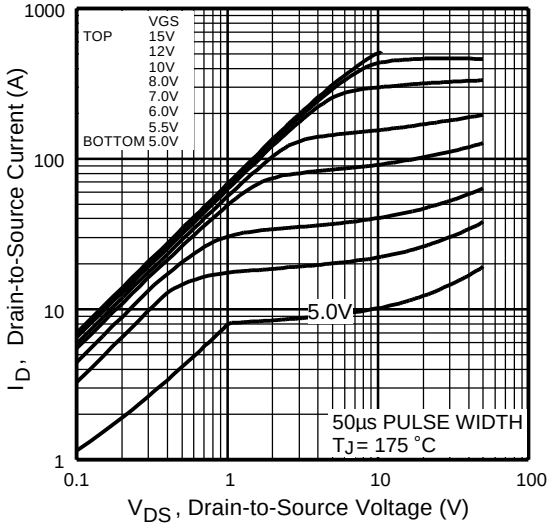


Fig 2. Typical Output Characteristics

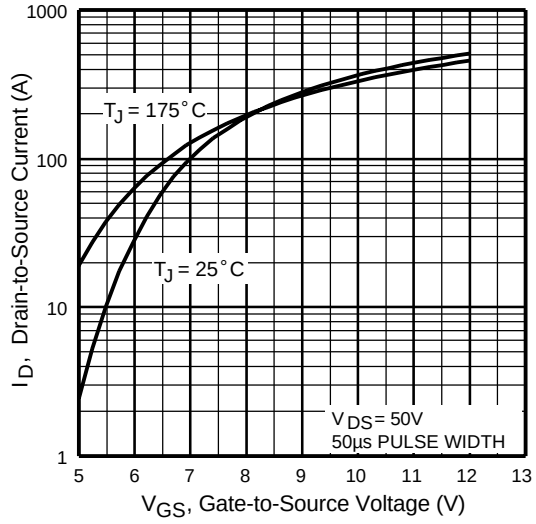


Fig 3. Typical Transfer Characteristics

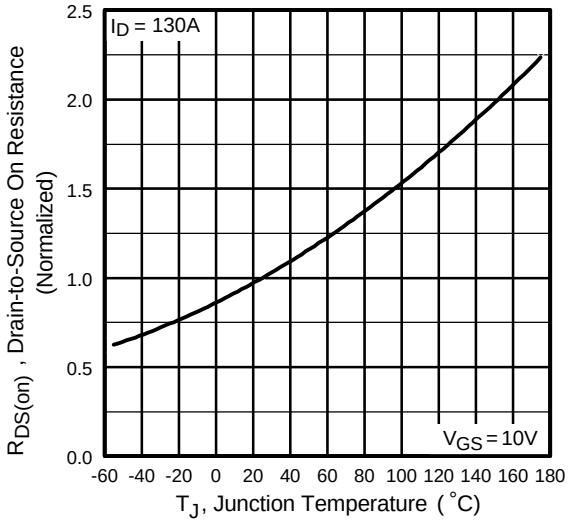


Fig 4. Normalized On-Resistance Vs. Temperature

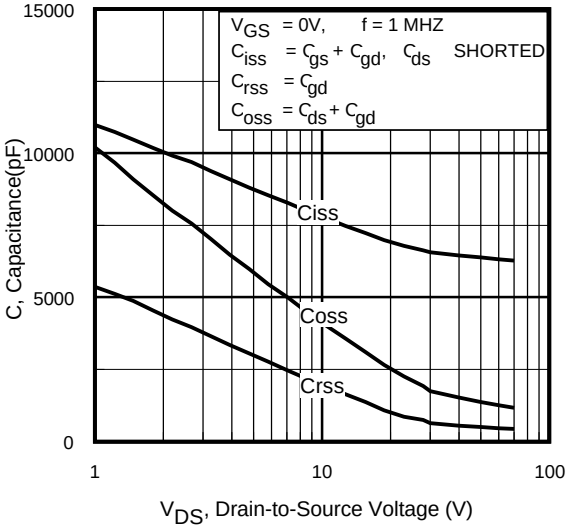


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

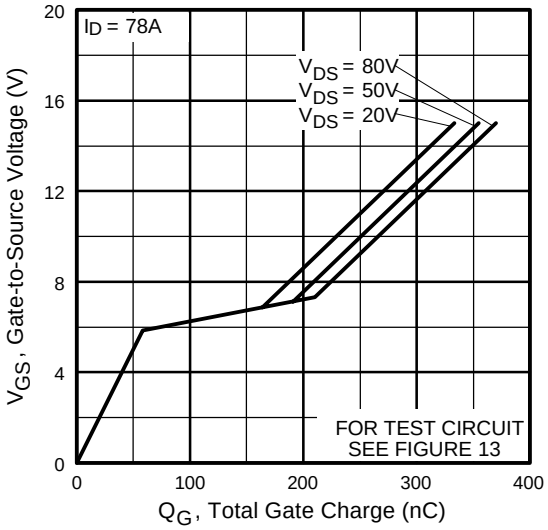


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

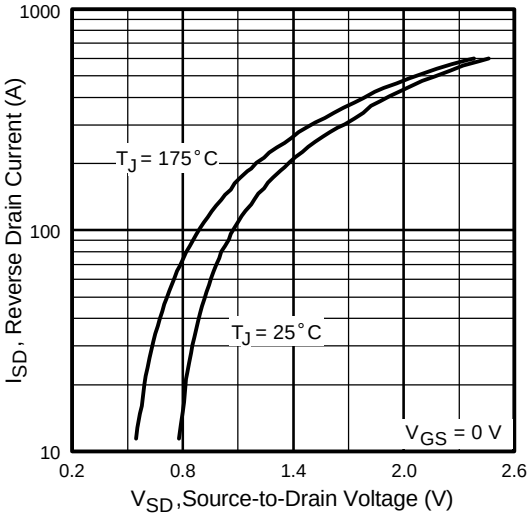


Fig 7. Typical Source-Drain Diode Forward Voltage

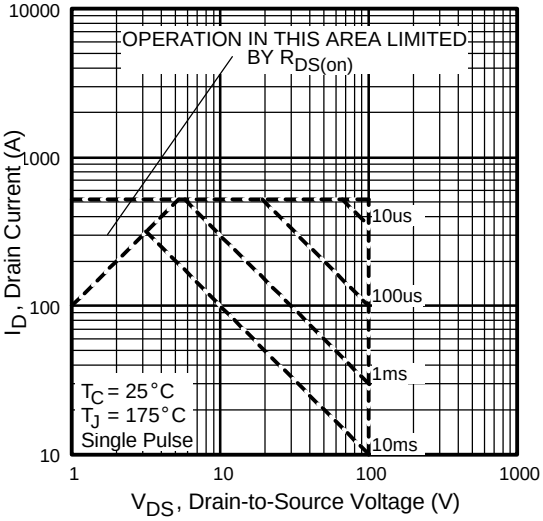


Fig 8. Maximum Safe Operating Area

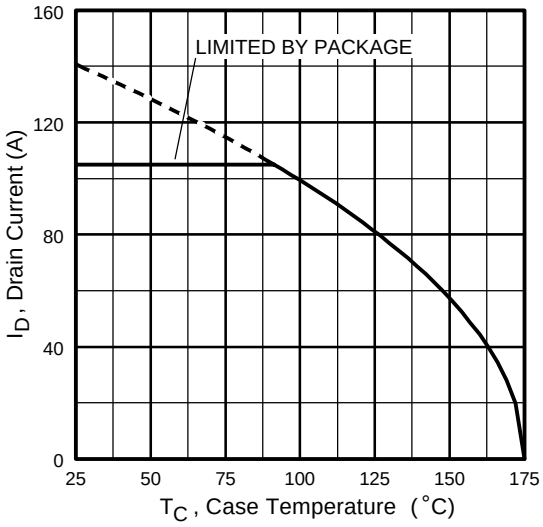
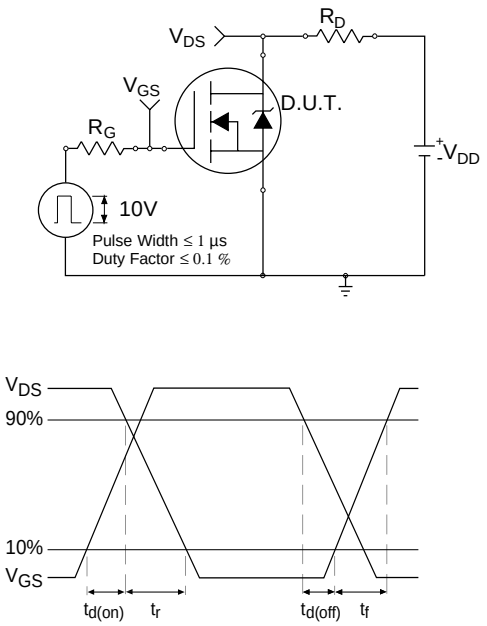


Fig 9. Maximum Drain Current Vs. Case Temperature



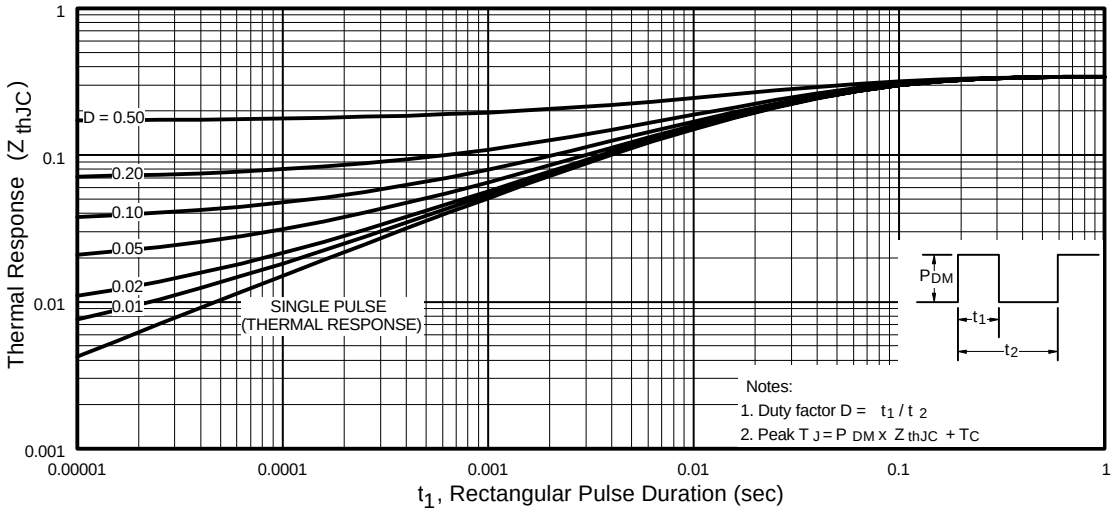


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

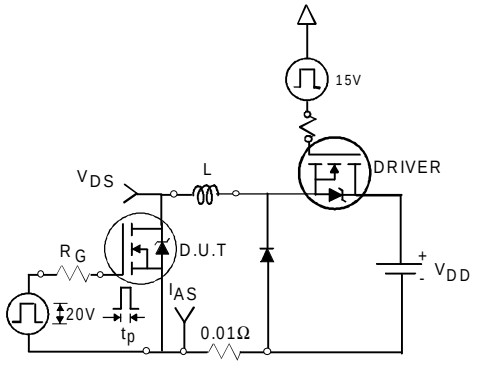


Fig 12a. Unclamped Inductive Test Circuit

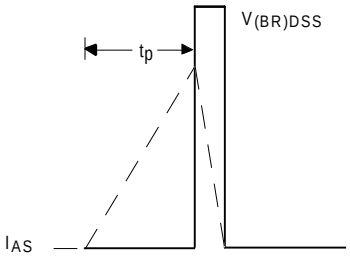


Fig 12b. Unclamped Inductive Waveforms

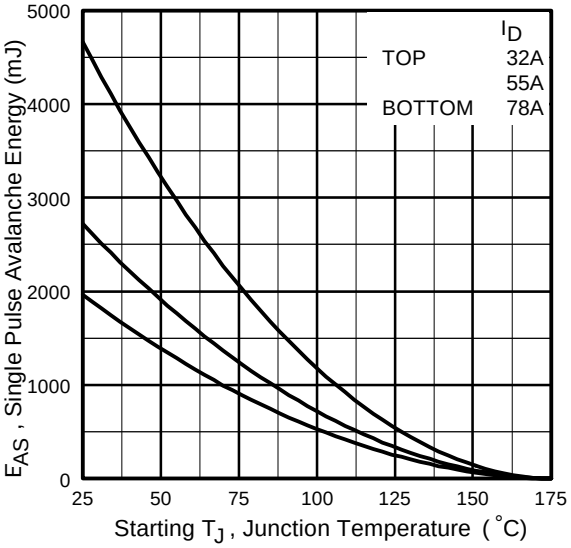


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

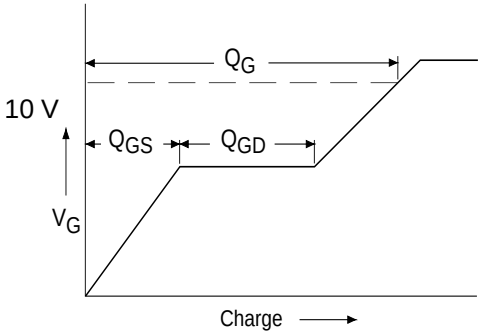


Fig 13a. Basic Gate Charge Waveform

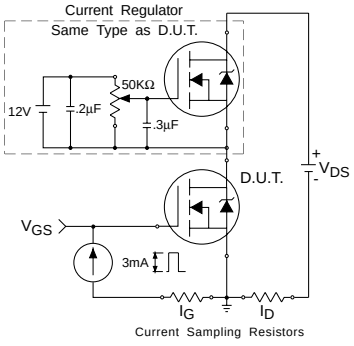
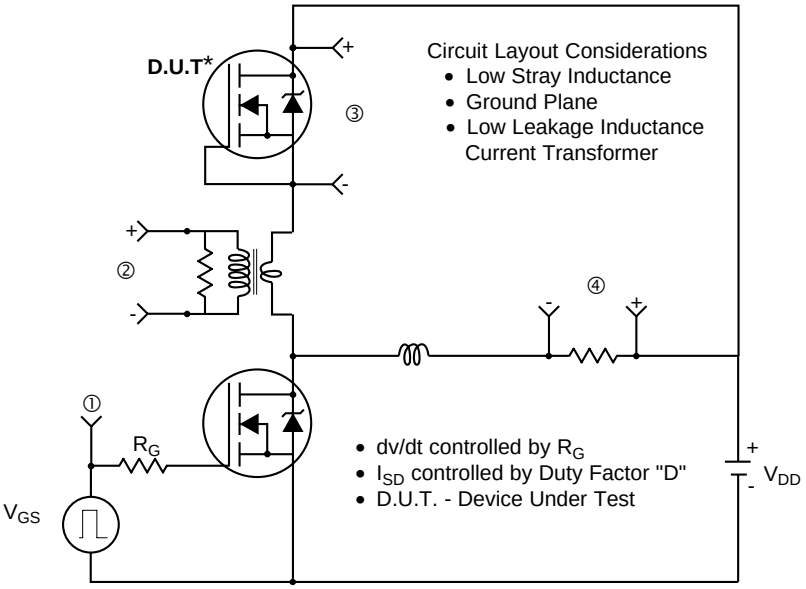
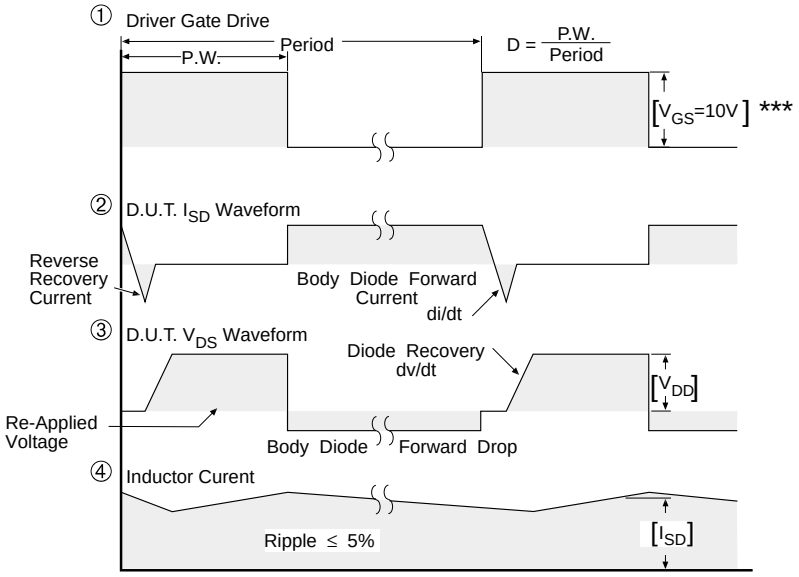


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

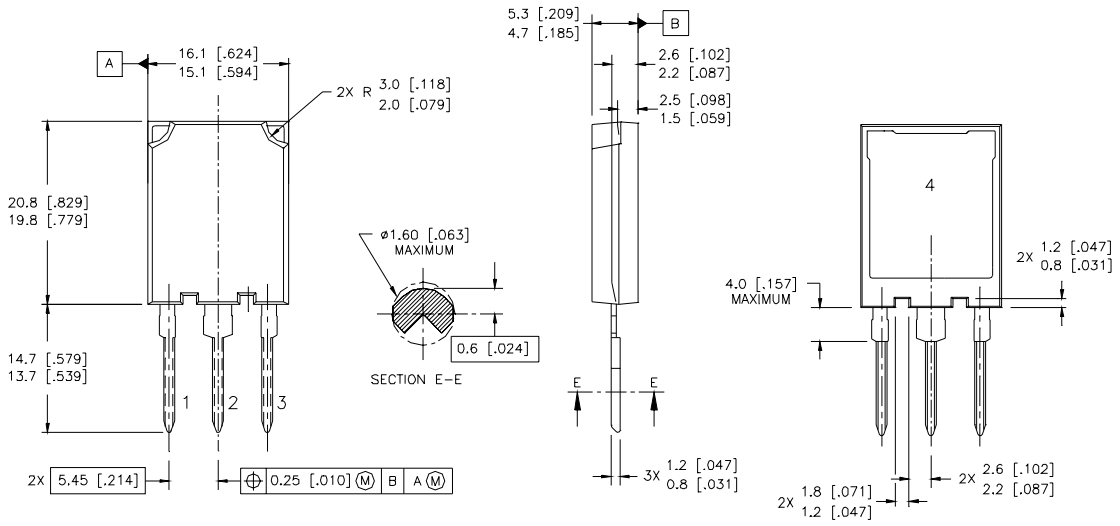


*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

Super-247™ Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONS & TOLERANCING PER ASME Y14.5M–1994
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETRES [INCHES]

LEAD ASSIGNMENTS

MOSFET	IGBT
1 – GATE	1 – GATE
2 – DRAIN	2 – COLLECTOR
3 – SOURCE	3 – EMITTER
4 – DRAIN	4 – COLLECTOR

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information. 2/01

International
IOR Rectifier

IR180SG..HCB SERIES

PHASE CONTROL THYRISTORS

- **Junction Size:** **Square 180 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **600 and 1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **n. a.**

Major Ratings and Characteristics

Parameters		Units	Test Conditions
V_{TM}	Maximum On-state Voltage	1.3 V	T_J = 25°C, I_T = 25 A
V_{RRM}	Reverse Breakdown Voltage	600 and 1200 V	T_J = 25°C, I_{RRM} = 300 µA **(1)**
I_{GT}	Max. Required DC Gate Current to Trigger	45 mA	T_J = 25° C, anode supply = 6 V, resistive load
V_{GT}	Max. Required DC Gate Voltage to Trigger	1.9 V	T_J = 25° C, anode supply = 6 V, resistive load
I_H	Holding Current Range	5 to 150 mA	Anode supply = 6 V, resistive load
I_L	Maximum Latching Current	400 mA	Anode supply = 6 V, resistive load

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	180 x 180 mils (see drawing)
Wafer Diameter	100 mm, with std. < 100 > flat
Wafer Thickness	350 µm ± 10 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	180	S	G	12	H	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: S = Solderable SCR

4 - Passivation Process: G = Glassivated MESA

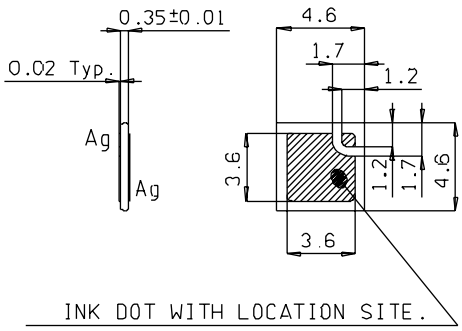
5 - Voltage code: Code x 100 = V_{RRM}

Available Class	
06 =	600 V
12 =	1200 V

6 - Metallization: H = Silver (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

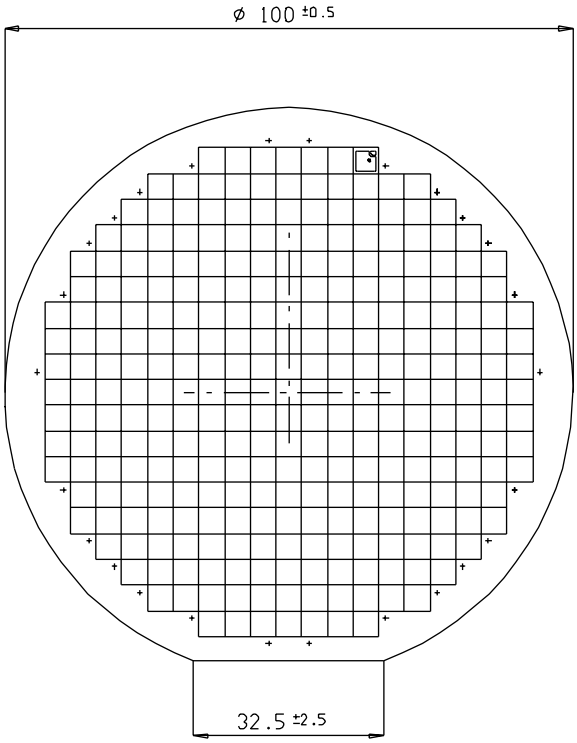


All dimensions are in millimeters

Wafer Layout

TOP VIEW

N° 293 Basic Cells



All dimensions are in millimeters

Bulletin I0209J rev. A 09/99

International
IOR Rectifier

IR185BG08DCB

PHASE CONTROL THYRISTORS

- **Junction Size:** **Square 185 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **800 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **25TTS Series**

Major Ratings and Characteristics

Parameters		Units	Test Conditions
V_{TM}	Maximum On-state Voltage	1.25 V	T_J = 25°C, I_T = 16 A
V_{RRM}	Reverse Breakdown Voltage	800 V	T_J = 25°C, I_{RRM} = 100 µA **(1)**
I_{GT}	Max. Required DC Gate Current to Trigger	60 mA	T_J = 25° C, anode supply = 6 V, resistive load
V_{GT}	Max. Required DC Gate Voltage to Trigger	2 V	T_J = 25° C, anode supply = 6 V, resistive load
I_H	Holding Current Range	5 to 100 mA	Anode supply = 6 V, resistive load
I_L	Maximum Latching Current	200 mA	Anode supply = 6 V, resistive load

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20µm)
Chip Dimensions	185 x 185 mils (see drawing)
Wafer Diameter	100 mm, with std. <110> flat
Wafer Thickness	350 µm ± 10 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	185	B	G	08	D	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: B = Wire Bondable SCR

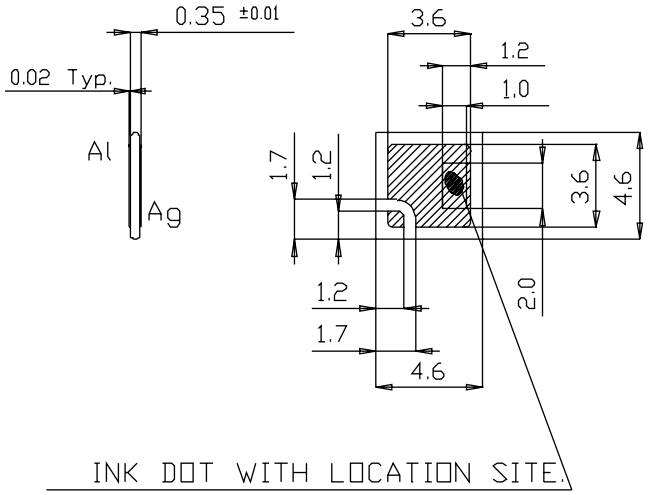
4 - Passivation Process: G = Glassivated MESA

5 - Voltage code: Code x 100 = V_{RRM}

6 - Metallization: D = Silver (Anode) - Aluminium (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

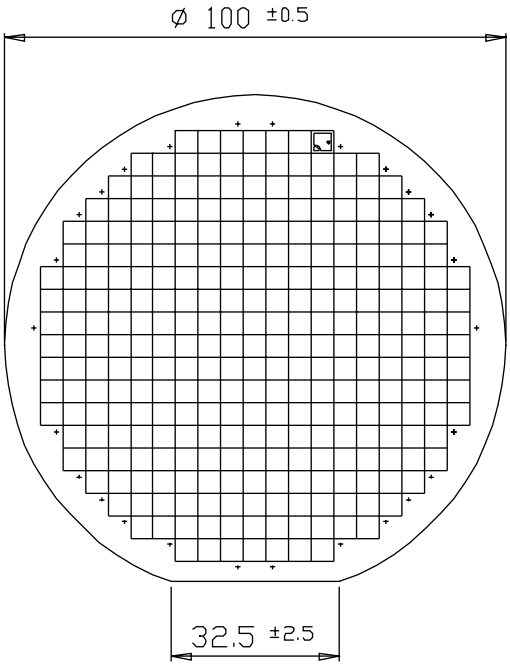


All dimensions are in microns

Wafer Layout

TOP VIEW

N° 293 Basic Cells



All dimensions are in millimiters

International
IOR Rectifier

IR185BG12DCB

PHASE CONTROL THYRISTORS

- **Junction Size:** **Square 185 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **25TTS Series**

Major Ratings and Characteristics

Parameters		Units	Test Conditions
V_{TM}	Maximum On-state Voltage	1.25 V	T_J = 25°C, I_T = 16 A
V_{RRM}	Reverse Breakdown Voltage	1200 V	T_J = 25°C, I_{RRM} = 100 µA **(1)**
I_{GT}	Max. Required DC Gate Current to Trigger	60 mA	T_J = 25° C, anode supply = 6 V, resistive load
V_{GT}	Max. Required DC Gate Voltage to Trigger	2 V	T_J = 25° C, anode supply = 6 V, resistive load
I_H	Holding Current Range	5 to 100 mA	Anode supply = 6 V, resistive load
I_L	Maximum Latching Current	200 mA	Anode supply = 6 V, resistive load

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20µm)
Chip Dimensions	185 x 185 mils (see drawing)
Wafer Diameter	100 mm, with std. <110> flat
Wafer Thickness	370 µm ± 10 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

International
IOR Rectifier

Ordering Information Table

Device Code

IR	185	B	G	12	D	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: B = Wire Bondable SCR

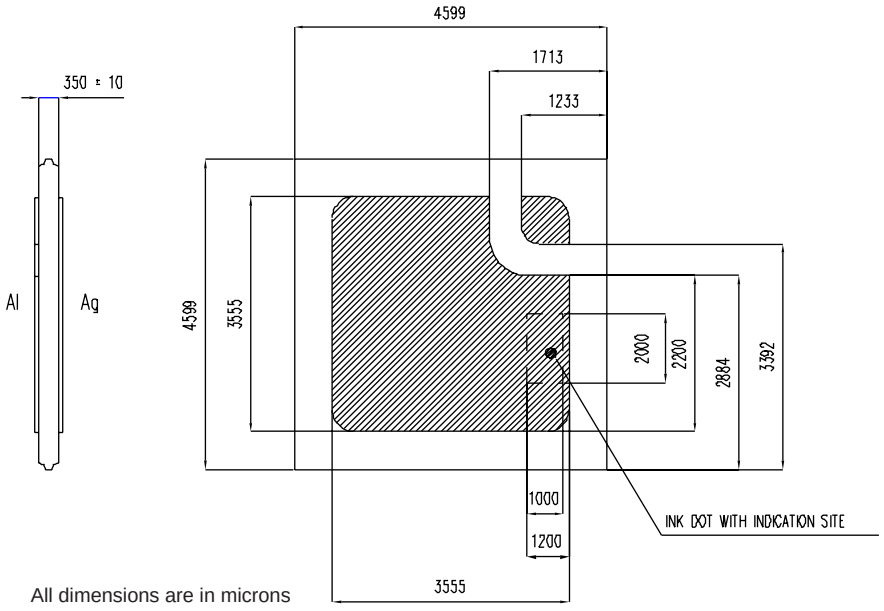
4 - Passivation Process: G = Glassivated MESA

5 - Voltage code: Code x 100 = V_{RRM}

6 - Metallization: D = Silver (Anode) - Aluminium (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

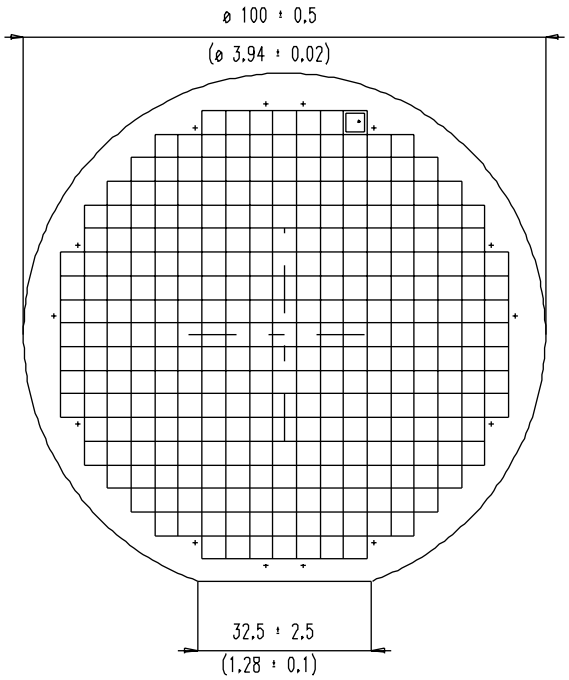


All dimensions are in microns

Wafer Layout

TOP VIEW

N° 293 Basic Cells



All dimensions are in millimiters (inches)

Bulletin I0204J 02/97

International
IOR Rectifier

IR210SG12HCB

PHASE CONTROL THYRISTORS

- **Junction Size:** **Square 210 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **25RIA Series**

Major Ratings and Characteristics

Parameters		Units	Test Conditions
V_{TM}	Maximum On-state Voltage	1.5 V	T_J = 25°C, I_T = 25 A
V_{RRM}	Reverse Breakdown Voltage	1200 V	T_J = 25°C, I_{RRM} = 100 µA **(1)**
I_{GT}	Max. Required DC Gate Current to Trigger	60 mA	T_J = 25° C, anode supply = 6 V, resistive load
V_{GT}	Max. Required DC Gate Voltage to Trigger	1.9 V	T_J = 25° C, anode supply = 6 V, resistive load
I_H	Holding Current Range	10 to 125 mA	Anode supply = 6 V, resistive load
I_L	Maximum Latching Current	200 mA	Anode supply = 6 V, resistive load

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	210 x 210 mils (see drawing)
Wafer Diameter	100 mm, with std. < 100 > flat
Wafer Thickness	370 µm ± 10 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

International
IOR Rectifier

Ordering Information Table

Device Code

IR	210	S	G	12	H	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: S = Solderable SCR

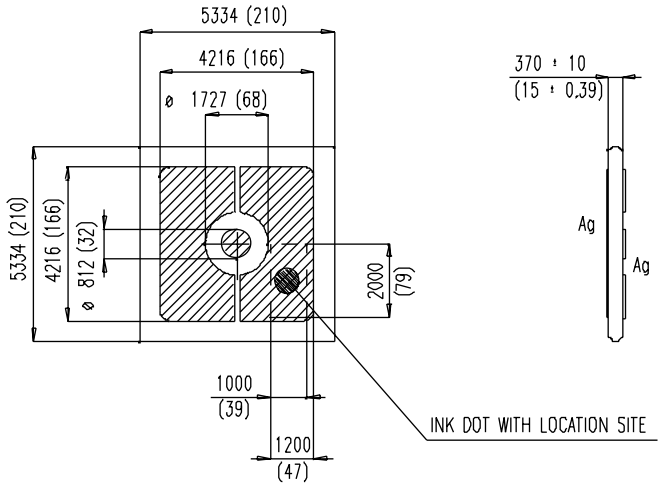
4 - Passivation Process: G = Glassivated MESA

5 - Voltage code: Code x 100 = V_{RRM}

6 - Metallization: H = Silver (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

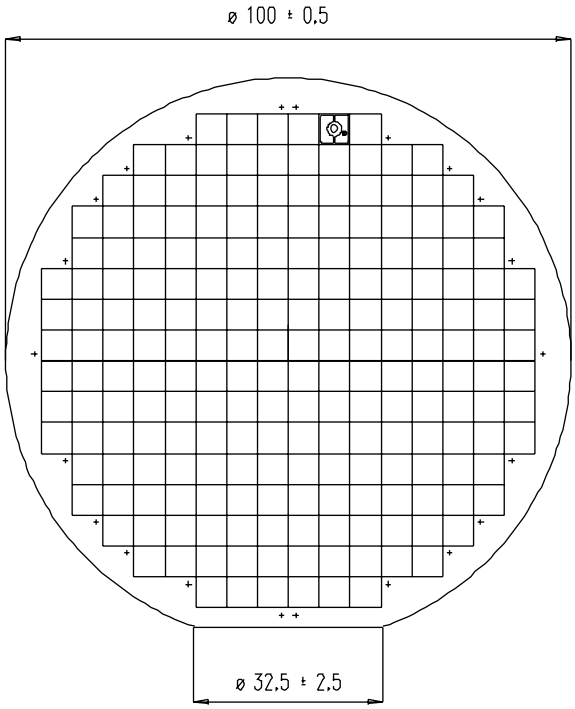


All dimensions are in microns (mils)

Wafer Layout

TOP VIEW

N° 208 Basic Cells



All dimensions are in millimiters

Bulletin I0205J 07/98

International
IOR Rectifier

IR230SG..HCB SERIES

PHASE CONTROL THYRISTORS

- **Junction Size:** **Square 230 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **600 and 1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **n. a.**

Major Ratings and Characteristics

Parameters		Units	Test Conditions
V_{TM}	Maximum On-state Voltage	1.3 V	T_J = 25°C, I_T = 25 A
V_{RRM}	Reverse Breakdown Voltage	600 and 1200 V	T_J = 25°C, I_{RRM} = 100 µA **(1)**
I_{GT}	Max. Required DC Gate Current to Trigger	60 mA	T_J = 25° C, anode supply = 6 V, resistive load
V_{GT}	Max. Required DC Gate Voltage to Trigger	1.9 V	T_J = 25° C, anode supply = 6 V, resistive load
I_H	Holding Current Range	5 to 150 mA	Anode supply = 6 V, resistive load
I_L	Maximum Latching Current	400 mA	Anode supply = 6 V, resistive load

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	230 x 230 mils (see drawing)
Wafer Diameter	100 mm, with std. < 100 > flat
Wafer Thickness	370 µm ± 10 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	230	S	G	12	H	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: S = Solderable SCR

4 - Passivation Process: G = Glassivated MESA

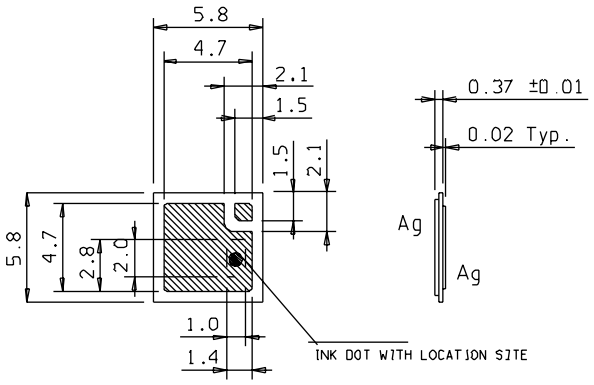
5 - Voltage code: Code x 100 = V_{RRM}

Available Class
06 = 600 V
12 = 1200 V

6 - Metallization: H = Silver (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

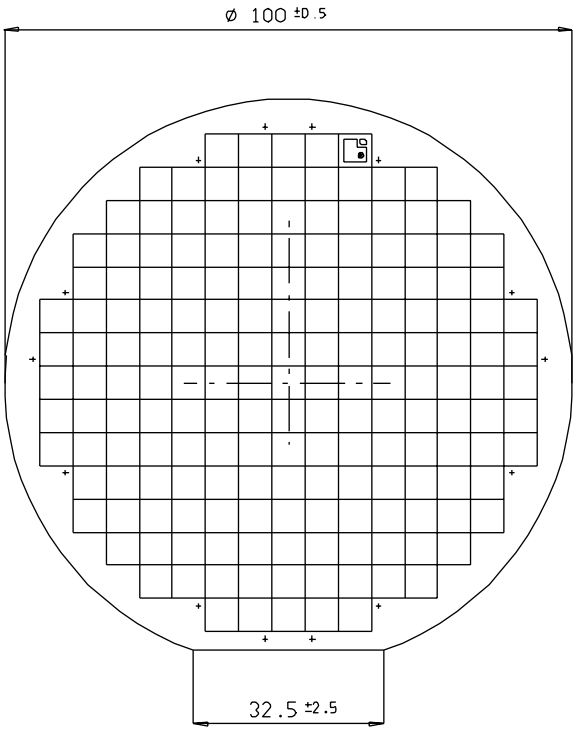


All dimensions are in millimeters

Wafer Layout

TOP VIEW

N° 177 Basic Cells



All dimensions are in millimeters

Bulletin I0200J rev. B 01/01

International
IOR Rectifier

IR250BG..DCB

PHASE CONTROL THYRISTORS

- **Junction Size** : **Square 250 mils**
- **Wafer Size** : **4"**
- **V_{RRM}/ V_{DRM} Class** : **600 to 1200 V**
- **Passivation Process** : **Glassivated MESA**
- **Reference IR Packaged Part** : **40TPS Series**

Major Ratings and Characteristics

Parameters		Units	Test Conditions
V_{TM}	Maximum On-state Voltage	1.3 V	T_J = 25°C, I_T = 25 A
V_{RRM}/V_{DRM}	Reverse Breakdown Voltage	600 to 1200 V	T_J = 25°C, I_{RRM} = 100 µA **(1)**
I_{GT}	Max. Required DC Gate Current to Trigger	150 mA	T_J = 25° C, anode supply = 6 V, resistive load
V_{GT}	Max. Required DC Gate Voltage to Trigger	2 V	T_J = 25° C, anode supply = 6 V, resistive load
I_H	Holding Current Range	5 to 200 mA	Anode supply = 6 V, resistive load
I_L	Maximum Latching Current	400 mA	Anode supply = 6 V, resistive load

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al, (20µm)
Chip Dimensions	250 x 250 mils (see drawing)
Wafer Diameter	100 mm, with std. <110> flat
Wafer Thickness	370 µm ± 10 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	250	B	G	12	D	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: B = Wire Bondable SCR

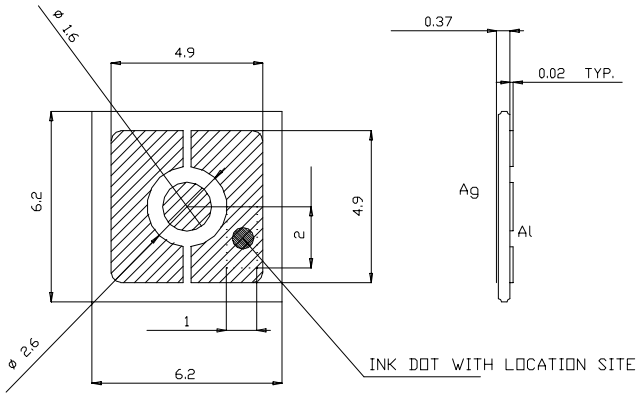
4 - Passivation Process: G = Glassivated MESA

5 - Voltage code: Code x 100 = V_{RRM}

6 - Metallization: D = Silver (Anode) - Aluminium (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

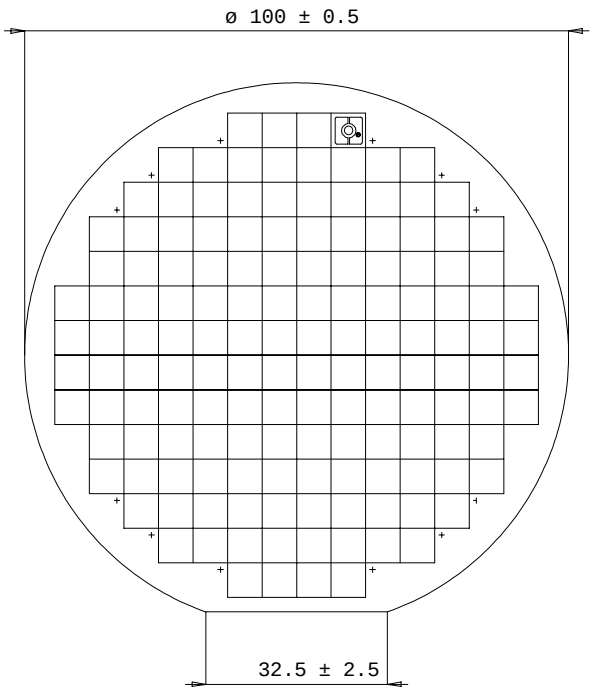


All dimensions are in millimeters

Wafer Layout

TOP VIEW

N° 148 Basic Cells



All dimensions are in millimiters

Bulletin I0210J 12/98

International
IOR Rectifier

IR250SG12HCB

PHASE CONTROL THYRISTORS

- **Junction Size:** **Square 250 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **n. a.**

Major Ratings and Characteristics

Parameters		Units	Test Conditions
V_{TM}	Maximum On-state Voltage	1.3 V	T_J = 25°C, I_T = 25 A
V_{RRM}	Reverse Breakdown Voltage	1200 V	T_J = 25°C, I_{RRM} = 100 µA **(1)**
I_{GT}	Max. Required DC Gate Current to Trigger	100 mA	T_J = 25° C, anode supply = 6 V, resistive load
V_{GT}	Max. Required DC Gate Voltage to Trigger	2 V	T_J = 25° C, anode supply = 6 V, resistive load
I_H	Holding Current Range	5 to 200 mA	Anode supply = 6 V, resistive load
I_L	Maximum Latching Current	400 mA	Anode supply = 6 V, resistive load

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	250 x 250 mils (see drawing)
Wafer Diameter	100 mm, with std. <110> flat
Wafer Thickness	370 µm ± 10 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	250	S	G	12	H	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: S = Solderable SCR

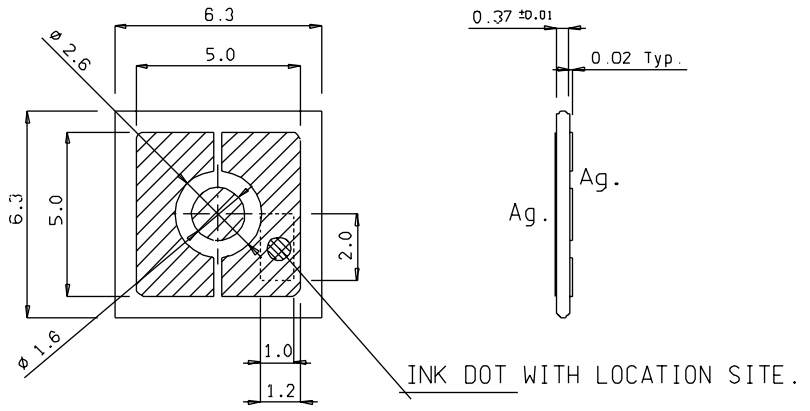
4 - Passivation Process: G = Glassivated MESA

5 - Voltage code: Code x 100 = V_{RRM}

6 - Metallization: H = Silver (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

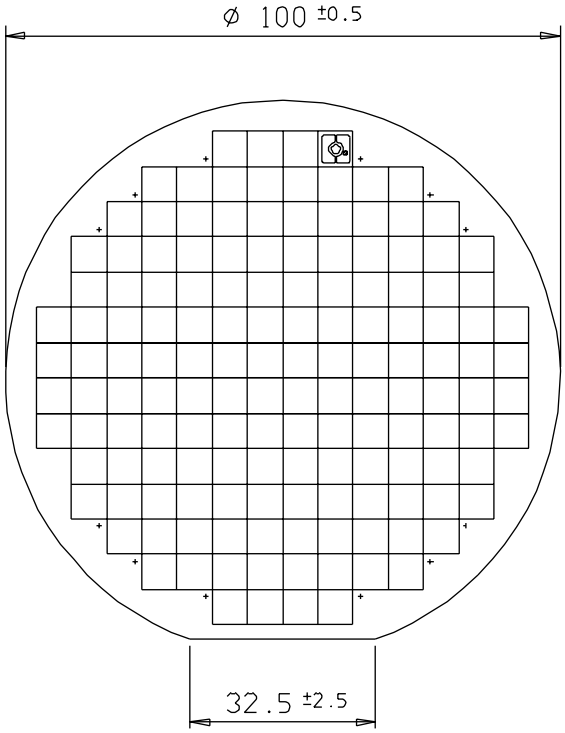


All dimensions are in millimiters

Wafer Layout

TOP VIEW

N° 148 Basic Cells



All dimensions are in millimiters

International
IOR Rectifier

IR255SG..HCB

PHASE CONTROL THYRISTORS

- **Junction Size:** **Square 250 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **600 to 1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **n. a.**

Major Ratings and Characteristics

Parameters		Units	Test Conditions
V_{TM}	Maximum On-state Voltage	1.25V	$T_J = 25°C$, $I_T = 25A$
V_{DRM}/V_{RRM}	Direct and Reverse Breakdown Voltage	600 to 1200 V	$T_J = 25°C$, $I_{DRM}/I_{RRM} = 100\mu A$ **(1)**
I_{GT}	Max. Required DC Gate Current to Trigger	80mA	$T_J = 25°C$, anode supply = 6V, resistive load
V_{GT}	Max. Required DC Gate Voltage to Trigger	2 V	$T_J = 25°C$, anode supply = 6V, resistive load
I_H	Holding Current Range	5 to 100 mA	Anode supply = 6V, resistive load
I_L	Maximum Latching Current	300mA	Anode supply = 6V, resistive load

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	250 x 250 mils (see drawing)
Wafer Diameter	100 mm, with std. <110> flat
Wafer Thickness	330μm ± 10μm
Maximum Width of Sawing Line	130μm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	255	S	G	12	H	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: S = Solderable SCR

4 - Passivation Process: G = Glassivated MESA

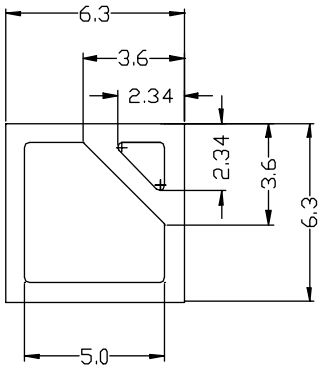
5 - Voltage code: Code x 100 = V_{RRM}

Available Class
06 = 600 V
08 = 800 V
12 = 1200 V

6 - Metallization: H = Silver (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

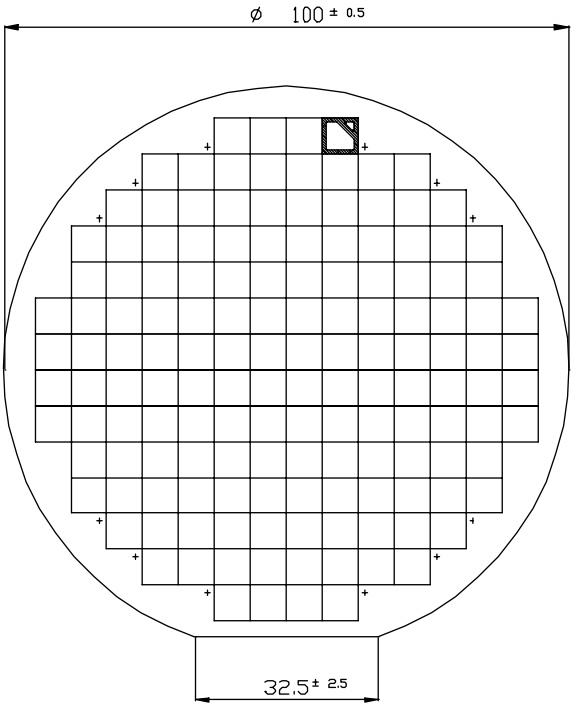


All dimensions are in millimeters

Wafer Layout

TOP VIEW

N° 148 Basic Cells



All dimensions are in millimiters

Bulletin I0108J 03/01

International
IOR Rectifier

IR343SG12H

PHASE CONTROL THYRISTORS

- **Junction Size** : **Square 343 mils**
- **Wafer Size** : **4"**
- **V_{RRM} / V_{DRM} Class** : **1200 V**
- **Passivation Process** : **Glassivated MESA**
- **Reference IR Packaged Part** : **n.a.**

Major Ratings and Characteristics

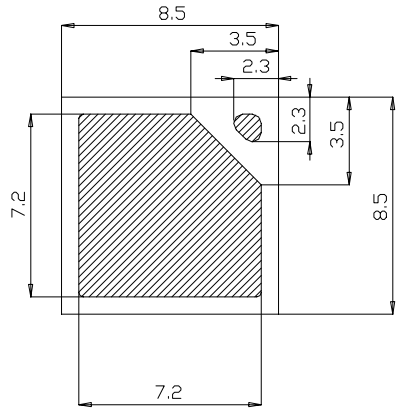
Parameters		Units	Test Conditions
V_{TM}	Typical On-state Voltage	1.2 V	$T_J = 25°C$, $I_T = 25$ A
V_{RRM}/V_{DRM}	Direct and Reverse Breakdown Voltage	1200 V	$T_J = 25°C$, I_{DRM} / $I_{RRM} = 100\,\mu$A **(1)**
I_{GT}	Required DC Gate Current to Trigger	5 to 100 mA	$T_J = 25°C$, anode supply = 6 V, resistive load
V_{GT}	Max. Required DC Gate Voltage to Trigger	2 V	$T_J = 25°C$, anode supply = 6 V, resistive load
I_H	Holding Current Range	5 to 200 mA	Anode supply = 6 V, resistive load
I_L	Maximum Latching Current	400 mA	Anode supply = 6 V, resistive load

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	340 x 340 mils (see drawing)
Wafer Diameter	100 mm, with std. <110> flat
Wafer Thickness	330 μm ± 10 μm
Maximum Width of Sawing Line	130 μm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Outline Table

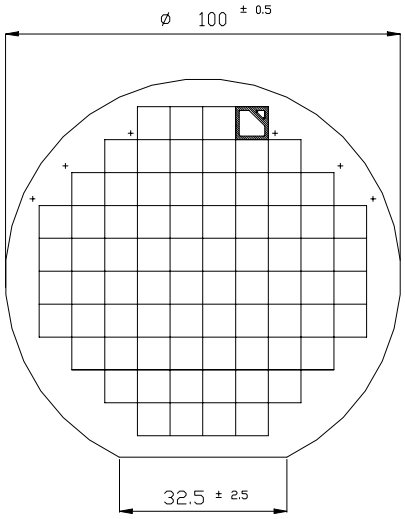


All dimensions are in millimeters

Wafer Layout

TOP VIEW

N° 76 Basic Cells



All dimensions are in millimiters

Bulletin I0206J 02/97

International
IOR Rectifier

IR350SG12HCB

PHASE CONTROL THYRISTORS

- **Junction Size:** **Square 350 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **50RIA Series**

Major Ratings and Characteristics

Parameters		Units	Test Conditions
V_{TM}	Maximum On-state Voltage	1.2 V	T_J = 25°C, I_T = 25 A
V_{RRM}	Reverse Breakdown Voltage	1200 V	T_J = 25°C, I_{RRM} = 100 µA **(1)**
I_{GT}	Max. Required DC Gate Current to Trigger	100 mA	T_J = 25° C, anode supply = 6 V, resistive load
V_{GT}	Max. Required DC Gate Voltage to Trigger	1.9 V	T_J = 25° C, anode supply = 6 V, resistive load
I_H	Holding Current Range	10 to 200 mA	Anode supply = 6 V, resistive load
I_L	Maximum Latching Current	400 mA	Anode supply = 6 V, resistive load

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	350 x 350 mils (see drawing)
Wafer Diameter	100 mm, with std. < 100 > flat
Wafer Thickness	370 µm ± 10 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	350	S	G	12	H	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: S = Solderable SCR

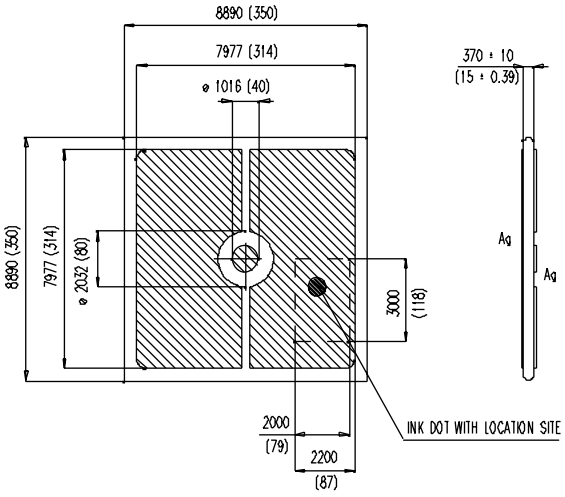
4 - Passivation Process: G = Glassivated MESA

5 - Voltage code: Code x 100 = V_{RRM}

6 - Metallization: H = Silver (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

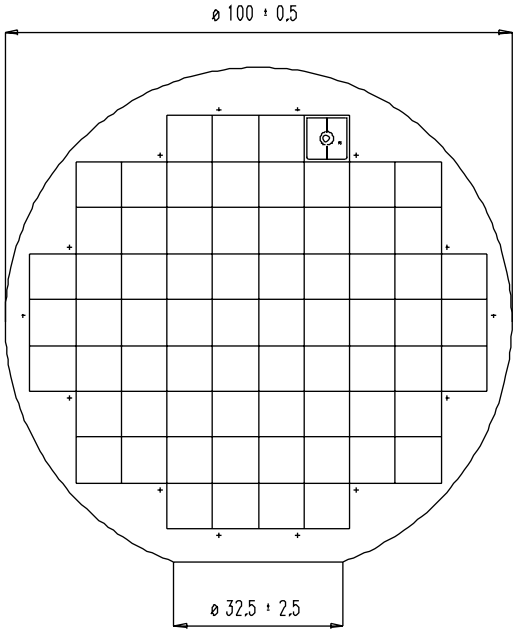


All dimensions are in microns (mils)

Wafer Layout

TOP VIEW

N° 70 Basic Cells



All dimensions are in millimeters

International
IOR Rectifier

IR370SG..HCB

PHASE CONTROL THYRISTORS

- **Junction Size:** **Square 370 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **600 to 1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **50RIA Series**

Major Ratings and Characteristics

Parameters		Units	Test Conditions
V_{TM}	Maximum On-state Voltage	1.2 V	$T_J = 25°C$, $I_T = 25$ A
V_{DRM}/V_{RRM}	Direct and Reverse Breakdown Voltage	600 to 1200 V	$T_J = 25°C$, $I_{DRM}/I_{RRM} = 100\mu A$ **(1)**
I_{GT}	Max. Required DC Gate Current to Trigger	150 mA	$T_J = 25°C$, anode supply = 6 V, resistive load
V_{GT}	Max. Required DC Gate Voltage to Trigger	2 V	$T_J = 25°C$, anode supply = 6 V, resistive load
I_H	Holding Current Range	5 to 200 mA	Anode supply = 6 V, resistive load
I_L	Maximum Latching Current	400 mA	Anode supply = 6 V, resistive load

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	370 x 370 mils (see drawing)
Wafer Diameter	100 mm, with std. <110> flat
Wafer Thickness	370 μm ± 10 μm
Maximum Width of Sawing Line	130 μm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	370	S	G	12	H	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: S = Solderable SCR

4 - Passivation Process: G = Glassivated MESA

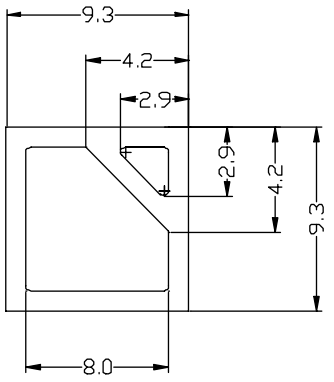
5 - Voltage code: Code x 100 = V_{RRM}

Available Class
06 = 600 V
08 = 800 V
12 =1200 V

6 - Metallization: H = Silver (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

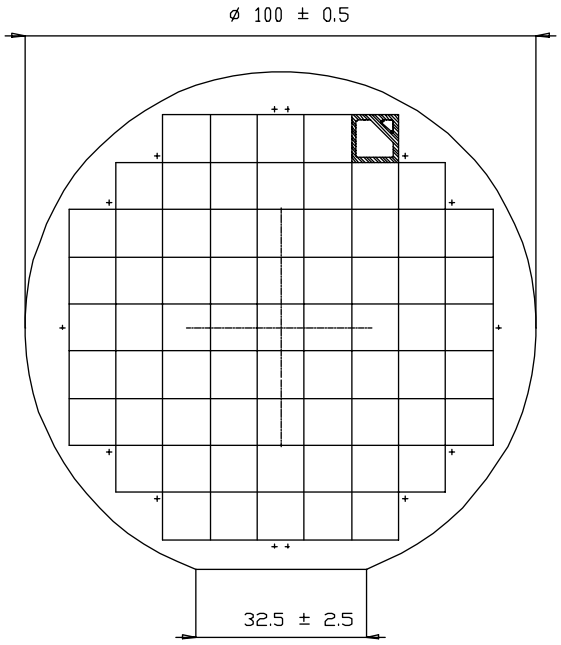


All dimensions are in millimeters

Wafer Layout

TOP VIEW

N° 69 Basic Cells



All dimensions are in millimiters

Bulletin I0208J rev. A 01/01

International
IOR Rectifier

IR480BG..DCB

PHASE CONTROL THYRISTORS

- **Junction Size** : **Square 480 mils**
- **Wafer Size** : **4"**
- **V_{RRM}/ V_{DRM} Class** : **600 to 1200 V**
- **Passivation Process** : **Glassivated MESA**
- **Reference IR Packaged Part** : **IRKT91 Series**

Major Ratings and Characteristics

Parameters		Units	Test Conditions
V_{TM}	Maximum On-state Voltage	1.2 V	T_J = 25°C, I_T = 25 A
V_{RRM}/ V_{DRM}	Reverse Breakdown Voltage	600 to 1200 V	T_J = 25°C, I_{RRM} = 100 µA (1)
I_{GT}	Max. Required DC Gate Current to Trigger	110 mA	T_J = 25° C, anode supply = 6 V, resistive load
V_{GT}	Max. Required DC Gate Voltage to Trigger	1.9 V	T_J = 25° C, anode supply = 6 V, resistive load
I_H	Holding Current Range	10 to 200 mA	Anode supply = 6 V, resistive load
I_L	Maximum Latching Current	400 mA	Anode supply = 6 V, resistive load

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	100% Al (20 µm)
Chip Dimensions	480 x 480 mils (see drawing)
Wafer Diameter	100 mm, with std. <100> flat
Wafer Thickness	370 µm ± 10 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	480	B	G	12	D	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: B = Wire Bonderable SCR

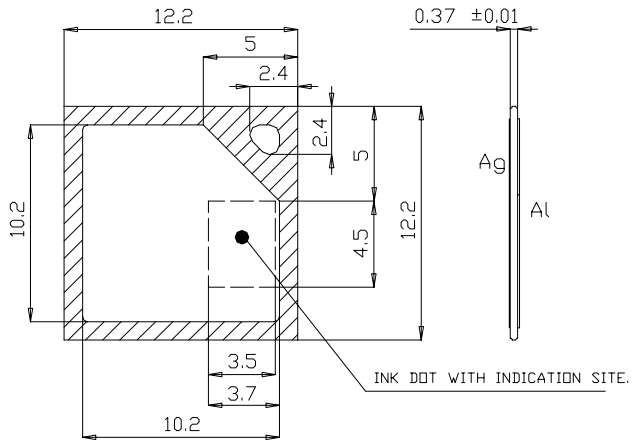
4 - Passivation Process: G = Glassivated MESA

5 - Voltage code: Code x 100 = V_{RRM}

6 - Metallization: D = Silver (Anode) - Aluminium (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

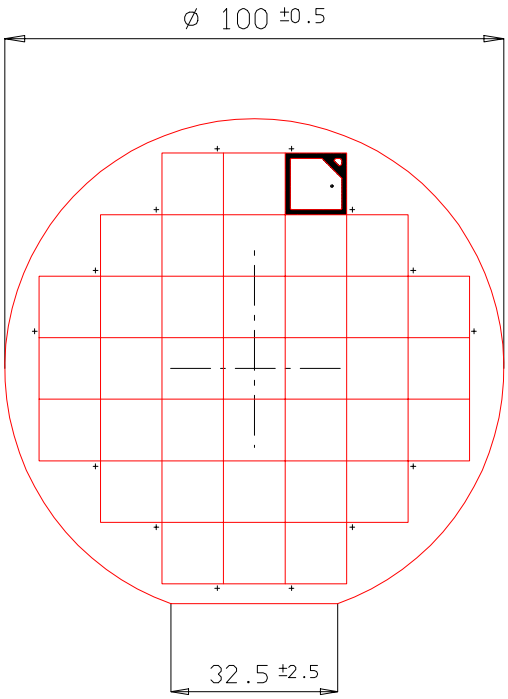


All dimensions are in millimeters

Wafer Layout

TOP VIEW

N° 37 Basic Cells



All dimensions are in millimiters

Bulletin I0207J rev. A 01/01

International
IOR Rectifier

IR480SG..HCB Series

PHASE CONTROL THYRISTORS

- **Junction Size:** **Square 480 mils**
- **Wafer Size:** **4"**
- **V_{DRM}/V_{RRM} Class:** **600 to 1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **T90RIA Series**

Major Ratings and Characteristics

Parameters		Units	Test Conditions
V_{TM}	Maximum On-state Voltage	1.2 V	T_J = 25°C, I_T = 25 A
V_{DRM}/V_{RRM}	Reverse Breakdown Voltage	600 to 1200 V	T_J = 25°C, I_{RRM} = 100 µA (1)
I_{GT}	Max. Required DC Gate Current to Trigger	110 mA	T_J = 25° C, anode supply = 6 V, resistive load
V_{GT}	Max. Required DC Gate Voltage to Trigger	1.9 V	T_J = 25° C, anode supply = 6 V, resistive load
I_H	Holding Current Range	10 to 200 mA	Anode supply = 6 V, resistive load
I_L	Maximum Latching Current	400 mA	Anode supply = 6 V, resistive load

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	480 x 480 mils (see drawing)
Wafer Diameter	100 mm, with std. <100> flat
Wafer Thickness	370 µm ± 10 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	480	S	G	12	H	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: S = Solderable SCR

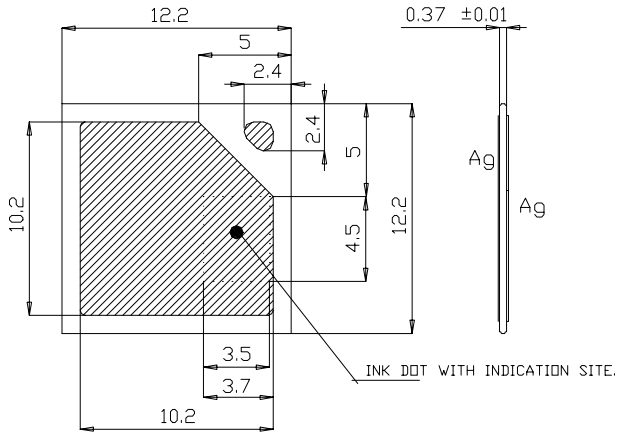
4 - Passivation Process: G = Glassivated MESA

5 - Voltage code: Code x 100 = V_{RRM}

6 - Metallization: H = Silver (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

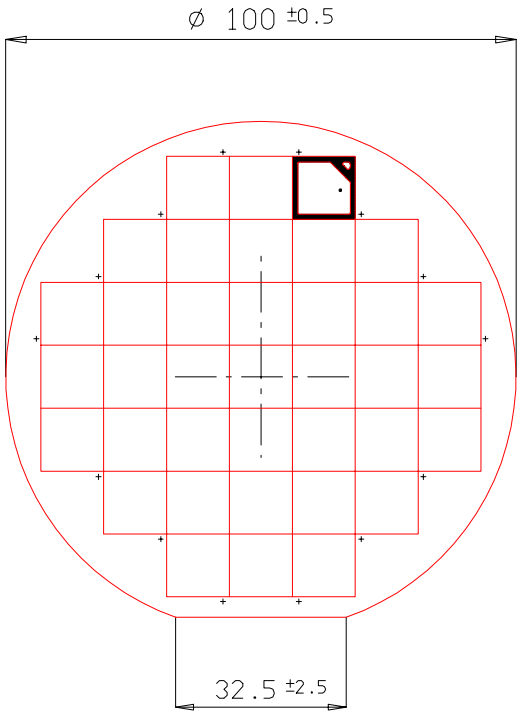


All dimensions are in millimeters

Wafer Layout

TOP VIEW

N° 37 Basic Cells



All dimensions are in millimiters

Bulletin I0213J 10/00

International
IOR Rectifier

IR590SG..HCB

PHASE CONTROL THYRISTORS

- **Junction Size:** **Square 590 mils**
- **Wafer Size:** **4"**
- **V_{RRM} Class:** **600 to 1200 V**
- **Passivation Process:** **Glassivated MESA**
- **Reference IR Packaged Part:** **181RKI Series**

Major Ratings and Characteristics

	Parameters	Units	Test Conditions
V_{TM}	Maximum On-state Voltage	1.2 V	T_J = 25°C, I_T = 25 A
V_{DRM}/V_{RRM}	Direct and Reverse Breakdown Voltage	600 to 1200 V	T_J = 25°C, I_{DRM}/I_{RRM} = 100 µA **(1)**
I_{GT}	Max. Required DC Gate Current to Trigger	140 mA	T_J = 25° C, anode supply = 6 V, resistive load
V_{GT}	Max. Required DC Gate Voltage to Trigger	2 V	T_J = 25° C, anode supply = 6 V, resistive load
I_H	Holding Current Range	5 to 180 mA	Anode supply = 6 V, resistive load
I_L	Maximum Latching Current	900 mA	Anode supply = 6 V, resistive load

(1) Nitrogen flow on die edge.

Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	590 x 590 mils (see drawing)
Wafer Diameter	100 mm, with std. <110> flat
Wafer Thickness	370 µm ± 10 µm
Maximum Width of Sawing Line	130 µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	See drawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

Ordering Information Table

Device Code

IR	590	S	G	12	H	CB
1	2	3	4	5	6	7

1 - International Rectifier Device

2 - Chip Dimension in Mils

3 - Type of Device: S = Solderable SCR

4 - Passivation Process: G = Glassivated MESA

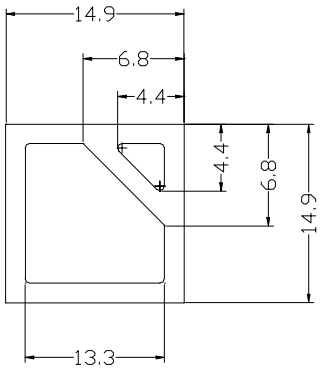
5 - Voltage code: Code x 100 = V_{RRM}

Available Class
06 = 600 V
08 = 800 V
12 = 1200 V

6 - Metallization: H = Silver (Anode) - Silver (Cathode)

7 - CB = Probed Uncut Die (wafer in box)
None = Probed Die in chip carrier

Outline Table

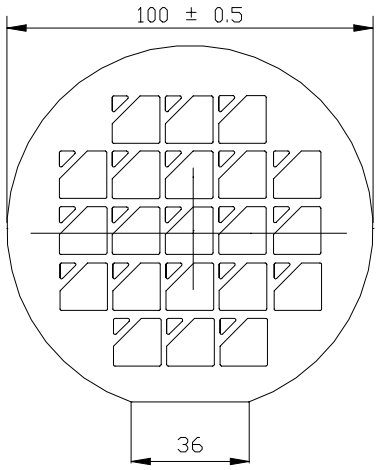


All dimensions are in millimeters

Wafer Layout

TOP VIEW

N° 21 Basic Cells



All dimensions are in millimiters

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 U.S.A. Tel: (310) 322 3331. Fax: (310) 322 3332.
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, U.K. Tel: ++ 44 1883 732020. Fax: ++ 44 1883 733408.
IR CANADA: 15 Lincoln Court, Brampton, Markham, Ontario L6T3Z2. Tel: (905) 453 2200. Fax: (905) 475 8801.
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg. Tel: ++ 49 6172 96590. Fax: ++ 49 6172 965933.
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino. Tel: ++ 39 11 4510111. Fax: ++ 39 11 4510220.
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171. Tel: 81 3 3983 0086.
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower,13-11, Singapore 237994. Tel: ++ 65 838 4630.
IR TAIWAN: 16 Fl. Suite D.207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan. Tel: 886 2 2377 9936.

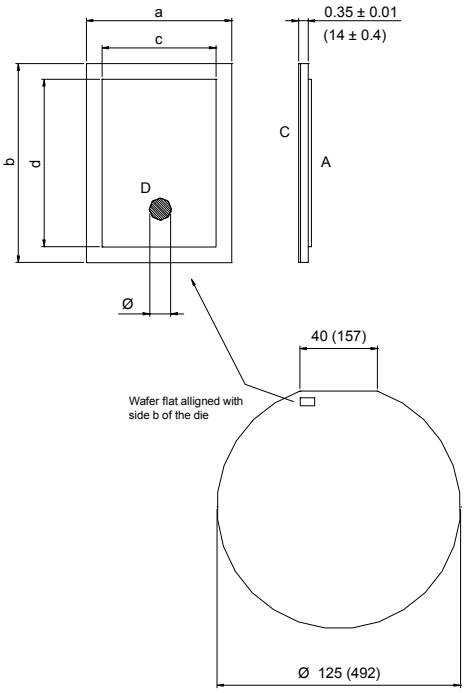
http://www.irf.com *Fax-On-Demand: +44 1883 733420* *Data and specifications subject to change without notice.*

Bulletin I0405J rev. A 05/01

International
IOR Rectifier

SC021.....5. Series

SCHOTTKY DIE 21 x 45 mils



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (MILS).

2. CONTROLLING DIMENSION: (MILS).

3. DIMENSIONS AND TOLERANCES:
   a = 0.53 + 0, - 0.01
   (21 + 0, - 0.4)
   b = 1.14 + 0, - 0.01
   (45 + 0, - 0.4)
   c = 0.38 + 0, - 0.01
   (15 + 0, - 0.4)
   d = 0.99 + 0, - 0.01
   (39 + 0, - 0.4)
   Ø = 0.4 ± 0.1
   (15 ± 4)

4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)
   D = Reject Ink Dot (only on non-conforming dies)
   (Sample Probe)

5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade
   Sawing Street
   0.05 + 0, -0.005
   (2 + 0, -0.2)

NOT TO SCALE

NOTE: 10 mils die thickness is available on specific request only.
Contact factory for information.

Electrical Characteristics

Device #	T_J Max. (°C)	V_R (V)	Typ. I_R @ 25°C (µA)	Typ. I_R @ 125°C (mA)	Max. V_F @ I_F (V)	Package Style
SC021**R**015x5x	125	15	n.a. contact factory			
SC021**S**020x5x	150	20	n.a. contact factory			
SC021**S**030x5x	150	30	n.a. contact factory			
SC021**S**045x5x	150	45	n.a. contact factory			
SC021**S**060x5x	150	60	n.a. contact factory			
SC021**H**045x5x	175	45	n.a. contact factory			
SC021**H**100x5x	175	100	n.a. contact factory			
SC021**H**150x5x	175	150	n.a. contact factory			

Mechanical Data

Device #		Metal Thickness Front Metal			Metal Thickness Back Metal		
SC021xxxx**A**5x	Bondable	–	Al/Si 30 kÅ	–	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ
SC021xxxx**S**5x	Solderable	Ti 2 kÅ	Ni 1 kÅ	Ag 35 kÅ	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ

Recommended Storage Environment: Store in original container, in dessicated nitrogen, with no contamination.
Shelf life for parts stored in above condition is 2 years.
If the storage is done in normal atmosphere shelf life is reduced to six months.

Packaging

Device #	Description	Minimum Order Quantity Die in Sale Package
SC021xxxxx5**B**	Inked Probed Unsawn Wafer (Wafer in Box)	17500
SC021xxxxx5**R**	Probed Die in Tape & Reel	n.a.
SC021xxxxx5**P**	Probed Die in Waffle Pack	n.a.
SC021xxxxx5**F**	Inked Probed Sawn Wafer on Film	17500

Ordering Information Table

Device Code

SC	021	S	030	S	5	B
1	2	3	4	5	6	7

1 - Schottky Die

2 - Chip Dimension in Mils

3 - Process (see Electrical Characteristics Table)

H = 830 Process
R = OR'ing Process
S = Standard Process

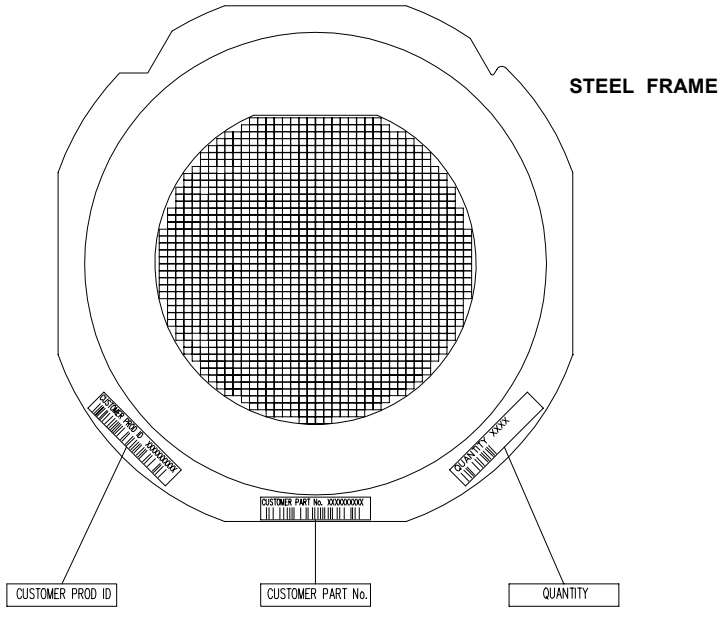
4 - Voltage code: Code = V_{RRM}

5 - Chip surface metallization (see Mechanical Data Table)

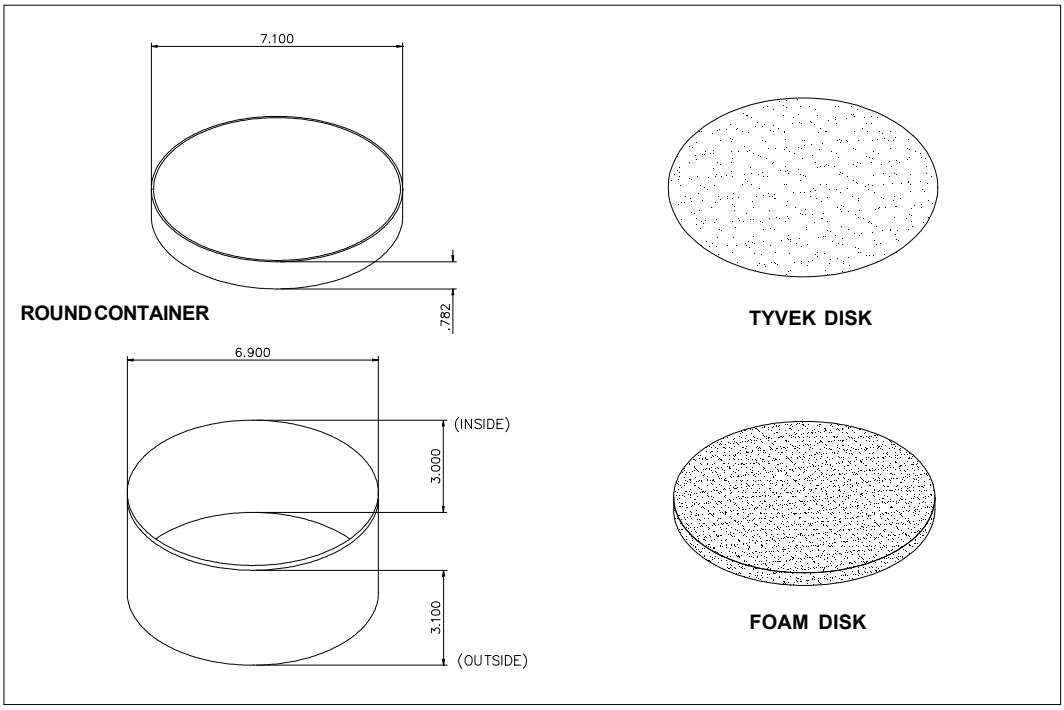
6 - Wafer Diameter in inches

7 - Packaging (see Packaging Table)

Wafer on Film



Wafer in Box



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IOR Rectifier

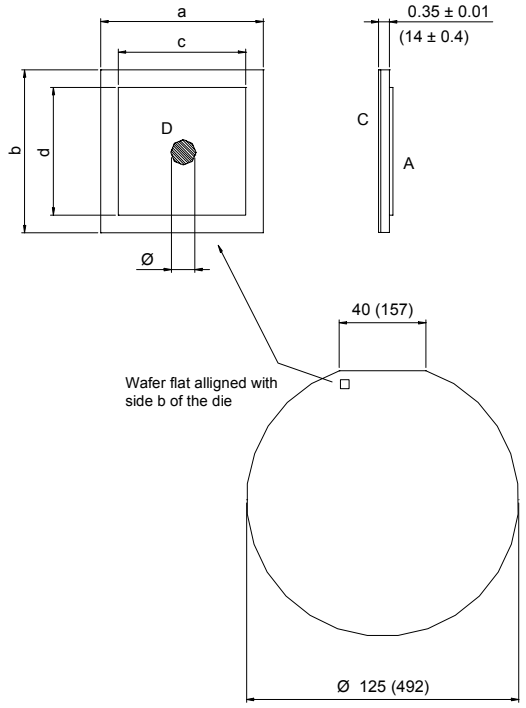
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7309
Visit us at www.irf.com for sales contact information. 03/01

Bulletin I0501J rev. D 05/01

International
IOR Rectifier

SC036.....5. Series

SCHOTTKY DIE 036 x 036 mils



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (MILS).

2. CONTROLLING DIMENSION: (MILS).

3. DIMENSIONS AND TOLERANCES:
   a = 0.91 + 0, - 0.01
   (36 + 0, - 0.4)
   b = 0.91 + 0, - 0.01
   (36 + 0, - 0.4)
   c = 0.76 + 0, - 0.01
   (30 + 0, - 0.4)
   d = 0.76 + 0, - 0.01
   (30 + 0, - 0.4)
   Ø = 0.5 ± 0.1
   (20 ± 4)

4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)
   D = Reject Ink Dot (only on non-conforming dies)

5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade
   Sawing Street
   0.05 +0, - 0.005
   (2 +0, - 0.2)

NOT TO SCALE

NOTE: 10 mils die thickness is available on specific request only.
Contact factory for information.

Electrical Characteristics

Device #	T_J Max. (°C)	V_R (V)	Typ. I_R @ 25°C (µA)	Typ. I_R @ 125°C (mA)	Max. V_F @ I_F (V)	Package Style
SC036**R**015x5x	125	15	200	12	0.34 @ 1A	SMB
SC036**S**020x5x	150	20	n.a. contact factory			
SC036**S**030x5x	150	30	15	6	n.a. contact factory	
SC036**S**045x5x	150	45	10	4	0.55 @ 1A	DO-41
SC036**S**060x5x	150	60	8	1.5	0.63 @ 1A	SMA
SC036**H**045x5x	175	45	n.a. contact factory			
SC036**H**100x5x	175	100	1	0.5	0.85 @ 1A	DO-41
SC036**H**150x5x	175	150	n.a. contact factory			

Mechanical Data

Device #		Metal Thickness Front Metal			Metal Thickness Back Metal		
SC036xxxx**A**5x	Bondable	–	Al/Si 30 kÅ	–	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ
SC036xxxx**S**5x	Solderable	Ti 2 kÅ	Ni 1 kÅ	Ag 35 kÅ	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ

Recommended Storage Environment: Store in original container, in dessicated nitrogen, with no contamination.
Shelf life for parts stored in above condition is 2 years.
If the storage is done in normal atmosphere shelf life is reduced to six months.

Packaging

Device #	Description	Minimum Order Quantity Die in Sale Package
SC036xxxxx5**B**	Inked Probed Unsawn Wafer (Wafer in Box)	13000
SC036xxxxx5**R**	Probed Die in Tape & Reel	n.a.
SC036xxxxx5**P**	Probed Die in Waffle Pack	n.a.
SC036xxxxx5**F**	Inked Probed Sawn Wafer on Film	13000

Ordering Information Table

Device Code

SC	036	S	060	A	5	B
1	2	3	4	5	6	7

1 - Schottky Die

2 - Chip Dimension in Mils

3 - Process (see Electrical Characteristics Table)

H = 830 Process
R = OR'ing Process
S = Standard Process

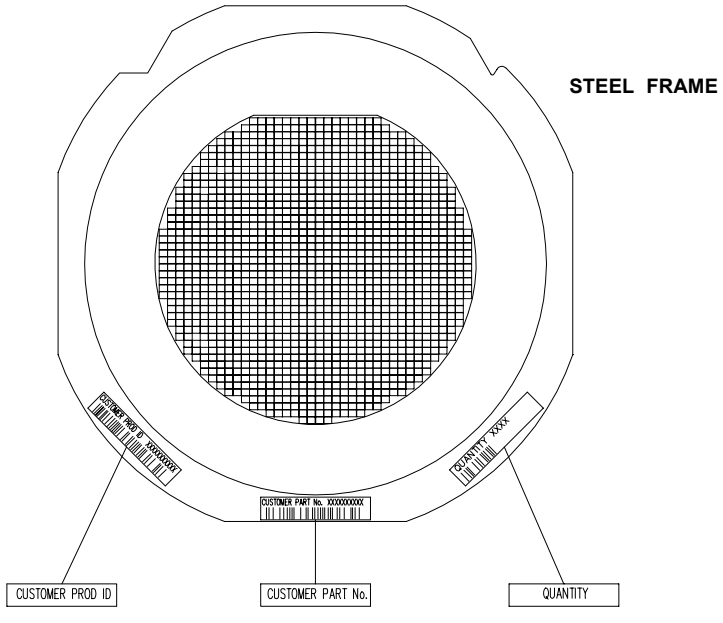
4 - Voltage code: Code = V_{RRM}

5 - Chip surface metallization (see Mechanical Data Table)

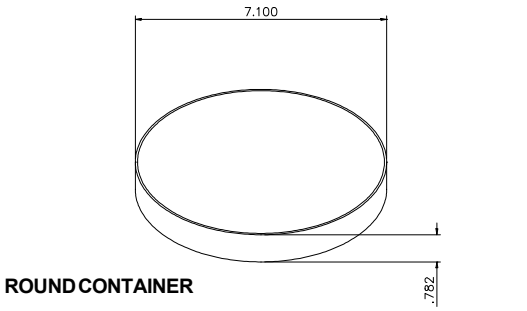
6 - Wafer Diameter in inches

7 - Packaging (see Packaging Table)

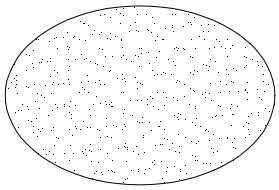
Wafer on Film



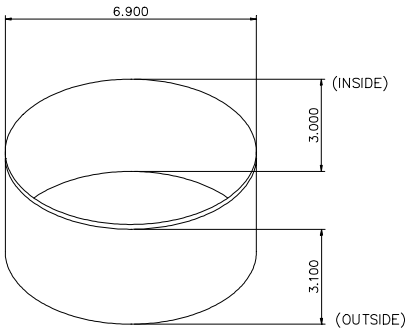
Wafer in Box

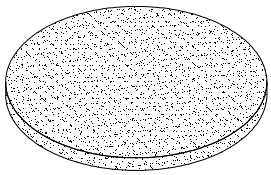


ROUND CONTAINER



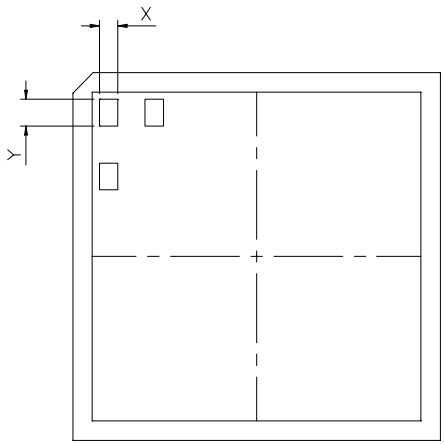
TYVEK DISK

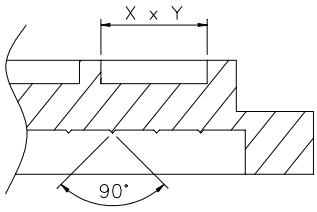




FOAM DISK

Die in Waffle Pack





CHIP TRAY POCKET

International
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WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 U.S.A. Tel: (310) 322 3331. Fax: (310) 322 3332.
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, U.K. Tel: ++ 44 1883 732020. Fax: ++ 44 1883 733408.
IR CANADA: 15 Lincoln Court, Brampton, Markham, Ontario L6T3Z2. Tel: (905) 453 2200. Fax: (905) 475 8801.
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg. Tel: ++ 49 6172 96590. Fax: ++ 49 6172 965933.
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino. Tel: ++ 39 11 4510111. Fax: ++ 39 11 4510220.
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171. Tel: 81 3 3983 0086.
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower,13-11, Singapore 237994. Tel: ++ 65 838 4630.
IR TAIWAN: 16 Fl. Suite D.207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan. Tel: 886 2 2377 9936.

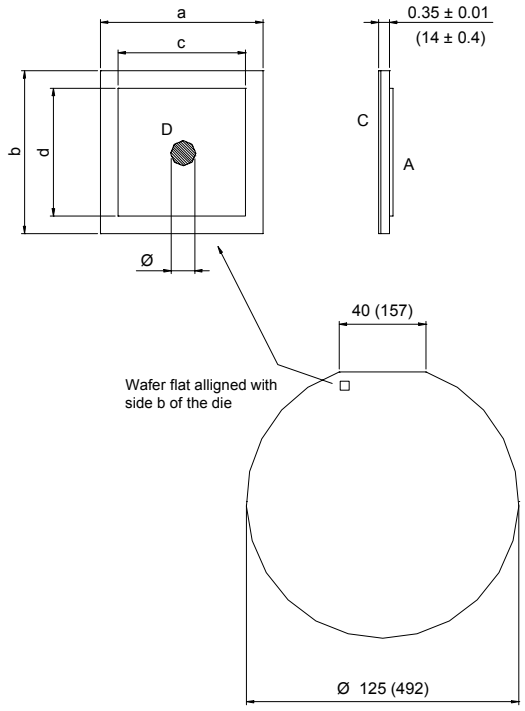
http://www.irf.com *Fax-On-Demand: +44 1883 733420* *Data and specifications subject to change without notice.*

Bulletin I0510J rev. A 05/01

International
IOR Rectifier

SC050.....5. Series

SCHOTTKY DIE 50 x 50 mils



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (MILS).

2. CONTROLLING DIMENSION: (MILS).

3. DIMENSIONS AND TOLERANCES:
   a = 1.27 + 0, - 0.01
   (50 + 0, - 0.4)
   b = 1.27 + 0, - 0.01
   (50 + 0, - 0.4)
   c = 1.12 + 0, - 0.01
   (44 + 0, - 0.4)
   d = 1.12 + 0, - 0.01
   (44 + 0, - 0.4)
   Ø = 0.7 ± 0.1
   (30 ± 4)

4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)
   D = Reject Ink Dot (only on non-conforming dies)

5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade
   Sawing Street
   0.05 + 0, - 0.005
   (2 + 0, - 0.2)

NOT TO SCALE

NOTE: 10 mils die thickness is available on specific request only.
Contact factory for information.

Electrical Characteristics

Device #	T_J Max. (°C)	V_R (V)	Typ. I_R @ 25°C (µA)	Typ. I_R @ 125°C (mA)	Max. V_F @ I_F (V)	Package Style
SC050**R**015x5x	125	15	n.a. contact factory			
SC050**S**020x5x	150	20	n.a. contact factory			
SC050**S**030x5x	150	30	30	12	0.47 @ 2A	SMB
SC050**S**045x5x	150	45	15	8	0.55 @ 2A	DO-41
SC050**S**060x5x	150	60	20	6	0.60 @ 2A	SMA
SC050**H**045x5x	175	45	n.a. contact factory			
SC050**H**100x5x	175	100	n.a. contact factory			
SC050**H**150x5x	175	150	n.a. contact factory			

Mechanical Data

Device #		Metal Thickness Front Metal			Metal Thickness Back Metal		
SC050xxxx**A**5x	Wire Bondable	–	Al 30 kÅ	–	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ
SC050xxxx**S**5x	Solderable	Ti 2 kÅ	Ni 1 kÅ	Ag 35 kÅ	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ

Recommended Storage Environment: Store in original container, in dessicated nitrogen, with no contamination.
Shelf life for parts stored in above condition is 2 years.
If the storage is done in normal atmosphere shelf life is reduced to six months.

Packaging

Device #	Description	Minimum Order Quantity Die in Sale Package
SC050xxxxx5**B**	Inked Probed Unsawn Wafer (Wafer in Box)	6300
SC050xxxxx5**R**	Probed Die in Tape & Reel	n. a.
SC050xxxxx5**P**	Probed Die in Waffle Pack	6300
SC050xxxxx5**F**	Inked Probed Sawn Wafer on Film	6300

Ordering Information Table

Device Code

SC	050	H	150	A	5	B
1	2	3	4	5	6	7

1 - Schottky Die

2 - Chip Dimension in Mils

3 - Process (see Electrical Characteristics Table)

H = 830 Process
R = OR'ing Process
S = Standard Process

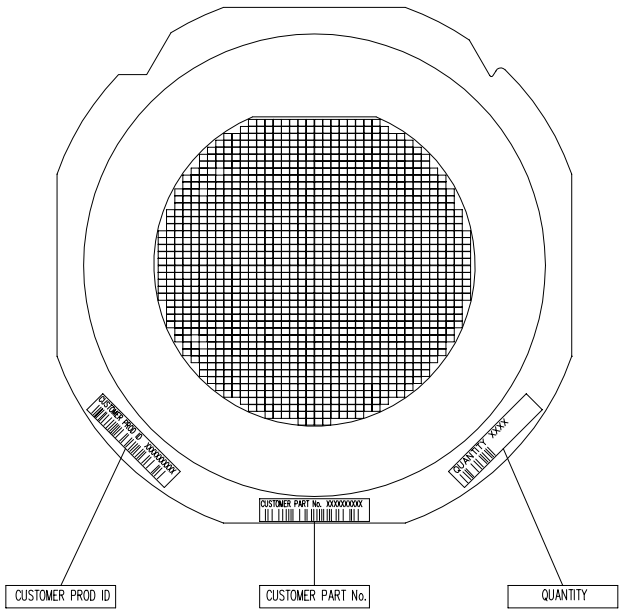
4 - Voltage code: Code = V_{RRM}

5 - Chip surface metallization (see Mechanical Data Table)

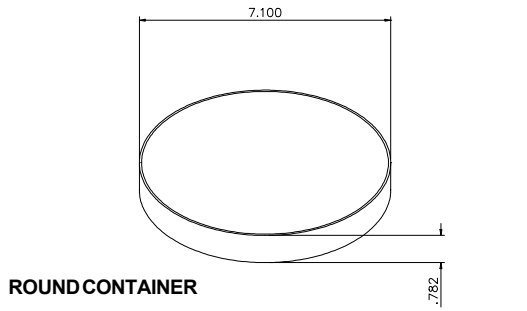
6 - Wafer Diameter in inches

7 - Packaging (see Packaging Table)

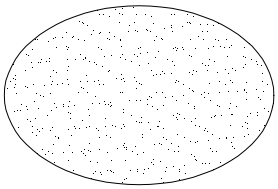
Wafer on Film



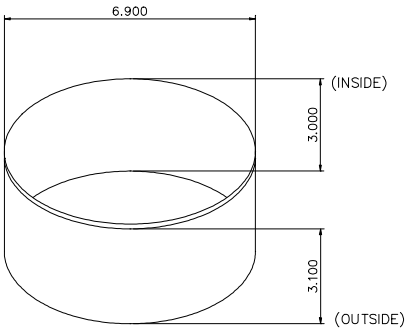
Wafer in Box

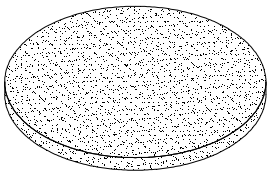


ROUND CONTAINER



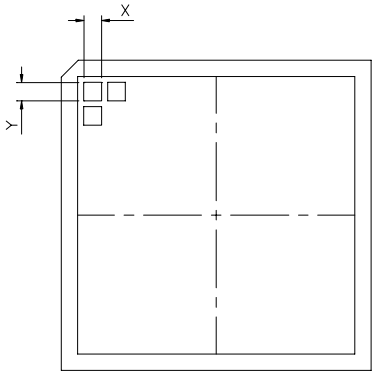
TYVEK DISK

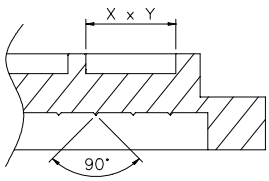




FOAM DISK

Die in Waffle Pack





CHIP TRAY POCKET

International
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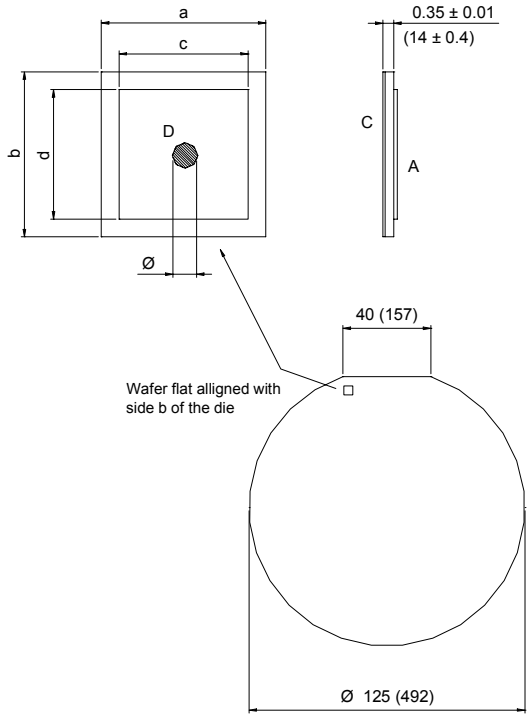
WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 U.S.A. Tel: (310) 322 3331. Fax: (310) 322 3332.
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International
IOR Rectifier

SC060.....5. Series

SCHOTTKY DIE 060 x 060 mils



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (MILS).
2. CONTROLLING DIMENSION: (MILS).
3. DIMENSIONS AND TOLERANCES:
   a = 1.52 + 0, - 0.01
   (60 + 0, - 0.4)
   b = 1.52 + 0, - 0.01
   (60 + 0, - 0.4)
   c = 1.37 + 0, - 0.01
   (54 + 0, - 0.4)
   d = 1.37 + 0, - 0.01
   (54 + 0, - 0.4)
   Ø = 0.7 ± 0.1
   (30 ± 4)
4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)
   D = Reject Ink Dot (only on non-conforming dies)
5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade
   Sawing Street
   0.05 + 0, - 0.005
   (2 + 0, - 0.2)

NOT TO SCALE

NOTE: 10 mils die thickness is available on specific request only.
Contact factory for information.

Electrical Characteristics

Device #	T_J Max. (°C)	V_R (V)	Typ. I_R @ 25°C (µA)	Typ. I_R @ 125°C (mA)	Max. V_F @ I_F (V)	Package Style
SC060**R**015x5x	125	15	800	50	0.35 @ 3A	SMC
SC060**S**020x5x	150	20	n.a. contact factory			
SC060**S**030x5x	150	30	40	15	0.45 @ 3A	DPAK (TO-252)
SC060**S**045x5x	150	45	30	13	0.53 @ 3A	DPAK (TO-252)
SC060**S**060x5x	150	60	25	12	0.61 @ 3A	DPAK (TO-252)
SC060**H**045x5x	175	45	n.a. contact factory			
SC060**H**100x5x	175	100	2.5	1.5	0.81 @ 3A	DPAK (TO-252)
SC060**H**150x5x	175	150	n.a. contact factory			

Mechanical Data

Device #		Metal Thickness Front Metal			Metal Thickness Back Metal		
SC060xxxx**A**5x	Wire Bondable	–	Al 30 kÅ	–	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ
SC060xxxx**S**5x	Solderable	Ti 2 kÅ	Ni 1 kÅ	Ag 35 kÅ	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ

Recommended Storage Environment: Store in original container, in dessicated nitrogen, with no contamination.
Shelf life for parts stored in above condition is 2 years.
If the storage is done in normal atmosphere shelf life is reduced to six months.

Packaging

Device #	Description	Minimum Order Quantity Die in Sale Package
SC060xxxxx5**B**	Inked Probed Unsawn Wafer (Wafer in Box)	4600
SC060xxxxx5**R**	Probed Die in Tape & Reel	n. a.
SC060xxxxx5**P**	Probed Die in Waffle Pack	n.a.
SC060xxxxx5**F**	Inked Probed Sawn Wafer on Film	4600

Ordering Information Table

Device Code

SC	060	S	060	A	5	B
1	2	3	4	5	6	7

1 - Schottky Die

2 - Chip Dimension in Mils

3 - Process (see Electrical Characteristics Table)

H = 830 Process
R = OR'ing Process
S = Standard Process

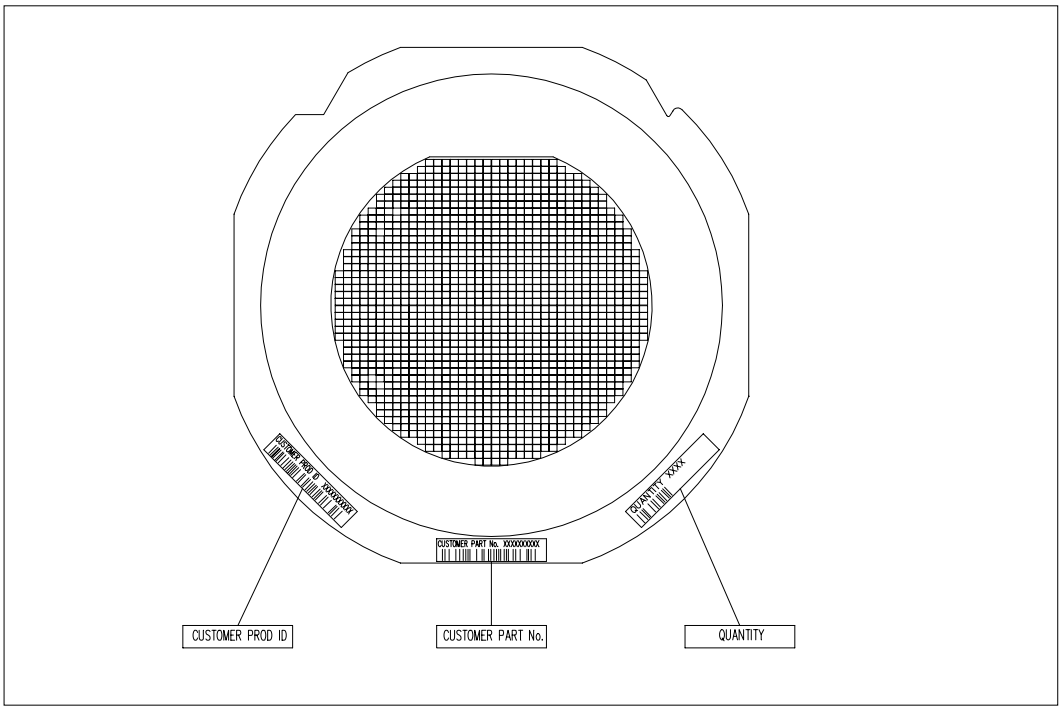
4 - Voltage code: Code = V_{RRM}

5 - Chip surface metallization (see Mechanical Data Table)

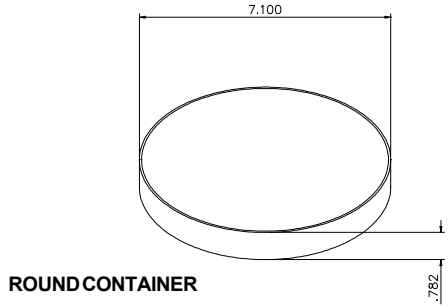
6 - Wafer Diameter in inches

7 - Packaging (see Packaging Table)

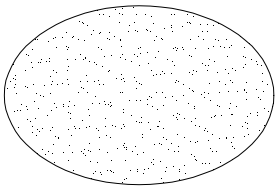
Wafer on Film



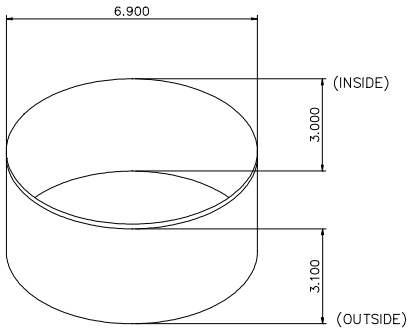
Wafer in Box

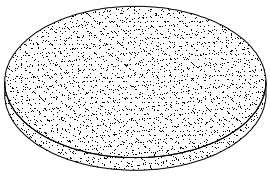


ROUND CONTAINER



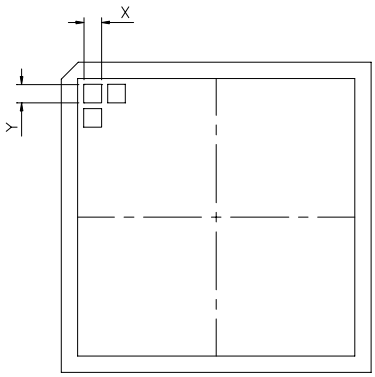
TYVEK DISK

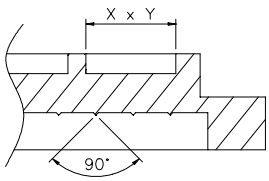




FOAM DISK

Die in Waffle Pack





CHIP TRAY POCKET

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 U.S.A. Tel: (310) 322 3331. Fax: (310) 322 3332.
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IR TAIWAN: 16 Fl. Suite D.207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan. Tel: 886 2 2377 9936.

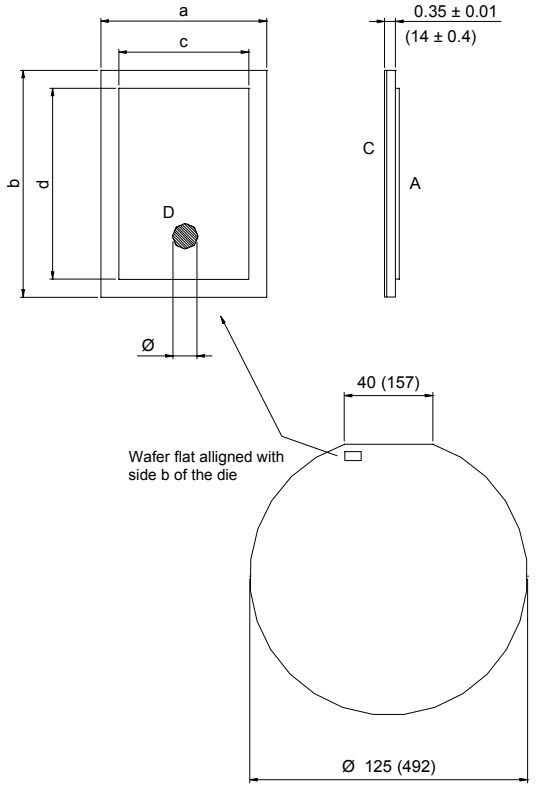
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Bulletin I0509J rev. A 05/01

International
IOR Rectifier

SC070.....5. Series

SCHOTTKY DIE 70 x 92 mils



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (MILS).
2. CONTROLLING DIMENSION: (MILS).
3. DIMENSIONS AND TOLERANCES:
   a = 1.78 + 0, - 0.01
   (70 + 0, - 0.4)
   b = 2.34 + 0, - 0.01
   (92 + 0, - 0.4)
   c = 1.63 + 0, - 0.01
   (64 + 0, - 0.4)
   d = 2.18 + 0, - 0.01
   (86 + 0, - 0.4)
   Ø = 0.7 ± 0.1
   (30 ± 4)
4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)
   D = Reject Ink Dot (only on non-conforming dies)
5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade
   Sawing Street
   0.05 + 0, - 0.005
   (2 + 0, - 0.2)

NOT TO SCALE

NOTE: 10 mils die thickness is available on specific request only.
Contact factory for information.

Electrical Characteristics

Device #	T_J Max. (°C)	V_R (V)	Typ. I_R @ 25°C (µA)	Typ. I_R @ 125°C (mA)	Max. V_F @ I_F (V)	Package Style
SC070**R**015x5x	125	15	n.a. contact factory			
SC070**S**020x5x	150	20	n.a. contact factory			
SC070**S**030x5x	150	30	90	38	0.55 @ 12A	DPAK (TO-252)
SC070**S**045x5x	150	45	70	32	0.70 @ 15A	TO-220
SC070**S**060x5x	150	60	n.a. contact factory			
SC070**H**045x5x	175	45	12	4	0.56 @ 15A	TO-220
SC070**H**100x5x	175	100	5	2.5	0.95 @ 12A	DPAK (TO-252)
SC070**H**150x5x	175	150	2	1.5	1.1 @ 10A	TO-220

Mechanical Data

Device #		Metal Thickness Front Metal			Metal Thickness Back Metal		
SC070xxxx**A**5x	Wire Bondable	–	Al 30 kÅ	–	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ
SC070xxxx**S**5x	Solderable	Ti 2 kÅ	Ni 1 kÅ	Ag 35 kÅ	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ

Recommended Storage Environment: Store in original container, in dessicated nitrogen, with no contamination.
Shelf life for parts stored in above condition is 2 years.
If the storage is done in normal atmosphere shelf life is reduced to six months.

Packaging

Device #	Description	Minimum Order Quantity Die in Sale Package
SC070xxxxx5**B**	Inked Probed Unsawn Wafer (Wafer in Box)	2500
SC070xxxxx5**R**	Probed Die in Tape & Reel	n.a
SC070xxxxx5**P**	Probed Die in Waffle Pack	2500
SC070xxxxx5**F**	Inked Probed Sawn Wafer on Film	2500

Ordering Information Table

Device Code

SC	070	S	045	A	5	B
1	2	3	4	5	6	7

1 - Schottky Die

2 - Chip Dimension in Mils

3 - Process (see Electrical Characteristics Table)

- H = 830 Process
- R = OR'ing Process
- S = Standard Process

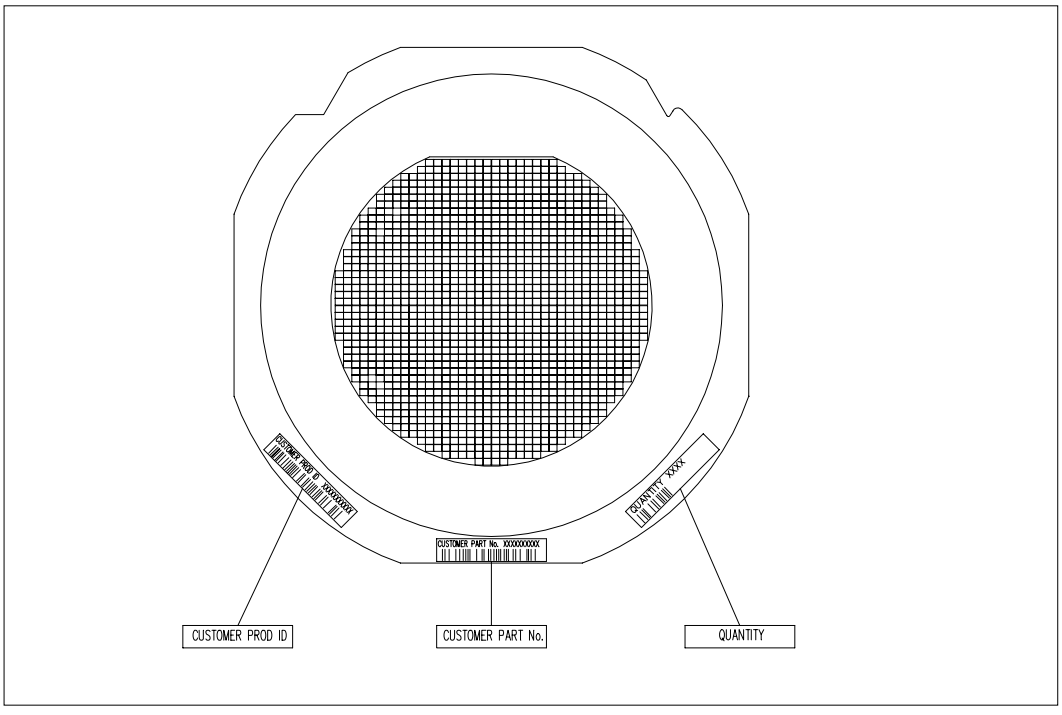
4 - Voltage code: Code = V_{RRM}

5 - Chip surface metallization (see Mechanical Data Table)

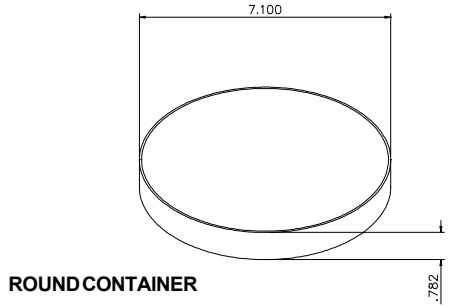
6 - Wafer Diameter in inches

7 - Packaging (see Packaging Table)

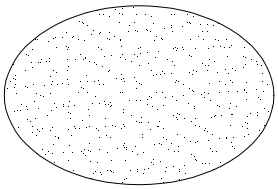
Wafer on Film



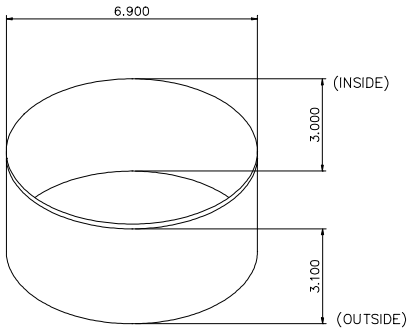
Wafer in Box

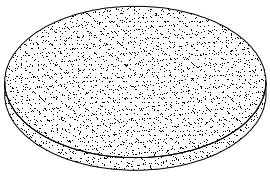


ROUND CONTAINER



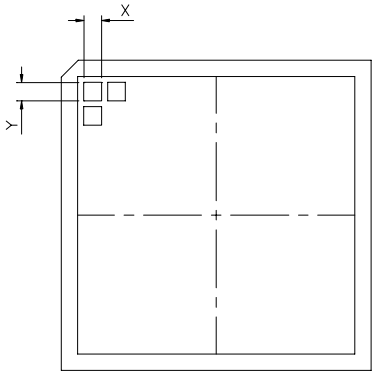
TYVEK DISK

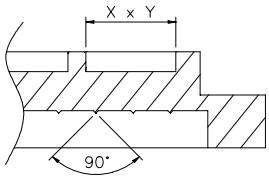




FOAM DISK

Die in Waffle Pack





CHIP TRAY POCKET

International
IOR Rectifier

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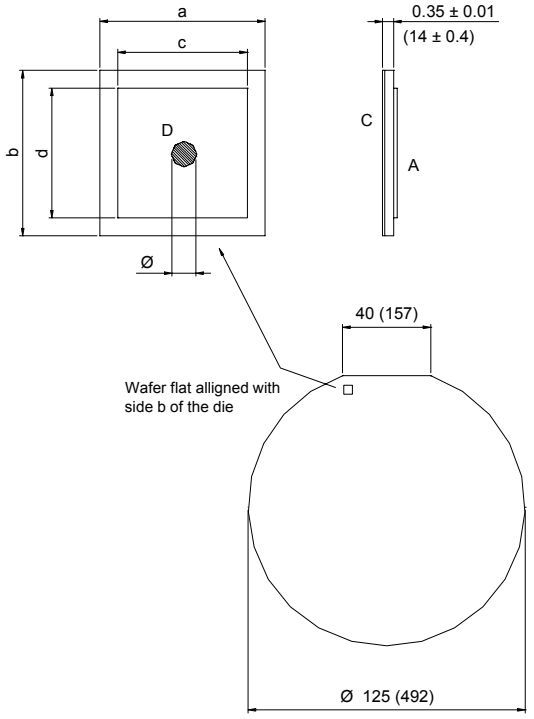
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Bulletin I0500J rev.A 05/01

International
IOR Rectifier

SC095.....5. Series

SCHOTTKY DIE 95 x 95 mils



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (MILS).

2. CONTROLLING DIMENSION: (MILS).

3. DIMENSIONS AND TOLERANCES:
   a = 2.41 + 0, - 0.01
   (95 + 0, - 0.4)
   b = 2.41 + 0, - 0.01
   (95 + 0, - 0.4)
   c = 2.26 + 0, - 0.01
   (89 + 0, - 0.4)
   d = 2.26 + 0, - 0.01
   (89 + 0, - 0.4)
   Ø = 1 ± 0.15
   (40 ± 6)

4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)
   D = Reject Ink Dot (only on non-conforming dies)

5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade
   Sawing Street
   0.05 + 0, - 0.005
   (2 + 0, - 0.2)

NOT TO SCALE

NOTE: 10 mils die thickness is available on specific request only.
Contact factory for information.

Electrical Characteristics

Device #	T_J Max. (°C)	V_R (V)	Typ. I_R @ 25°C (µA)	Typ. I_R @ 125°C (mA)	Max. V_F @ I_F (V)	Package Style
SC095**R**015x5x	125	15	n.a. contact factory			
SC095**S**020x5x	150	20	n.a. contact factory			
SC095**S**030x5x	150	30	n.a. contact factory			
SC095**S**045x5x	150	45	n.a. contact factory			
SC095**S**060x5x	150	60	n.a. contact factory			
SC095**H**045x5x	175	45	15	5	0.84 @ 20A	TO-220
SC095**H**100x5x	175	100	n.a. contact factory			
SC095**H**150x5x	175	150	n.a. contact factory			

Mechanical Data

Device #		Metal Thickness Front Metal			Metal Thickness Back Metal		
SC095xxxx**A**5x	Wire Bondable	–	Al 30 kÅ	–	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ
SC095xxxx**S**5x	Solderable	Ti 2 kÅ	Ni 1 kÅ	Ag 35 kÅ	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ

Recommended Storage Environment: Store in original container, in dessicated nitrogen, with no contamination.
Shelf life for parts stored in above condition is 2 years.
If the storage is done in normal atmosphere shelf life is reduced to six months.

Packaging

Device #	Description	Minimum Order Quantity Die in Sale Package
SC095xxxxx5**B**	Inked Probed Unsawn Wafer (Wafer in Box)	1545
SC095xxxxx5**R**	Probed Die in Tape & Reel	n. a.
SC095xxxxx5**P**	Probed Die in Waffle Pack	1545
SC095xxxxx5**F**	Inked Probed Sawn Wafer on Film	1545

Ordering Information Table

Device Code

SC	095	H	150	A	5	B
1	2	3	4	5	6	7

1 - Schottky Die

2 - Chip Dimension in Mils

3 - Process (see Electrical Characteristics Table)

H = 830 Process
R = OR'ing Process
S = Standard Process

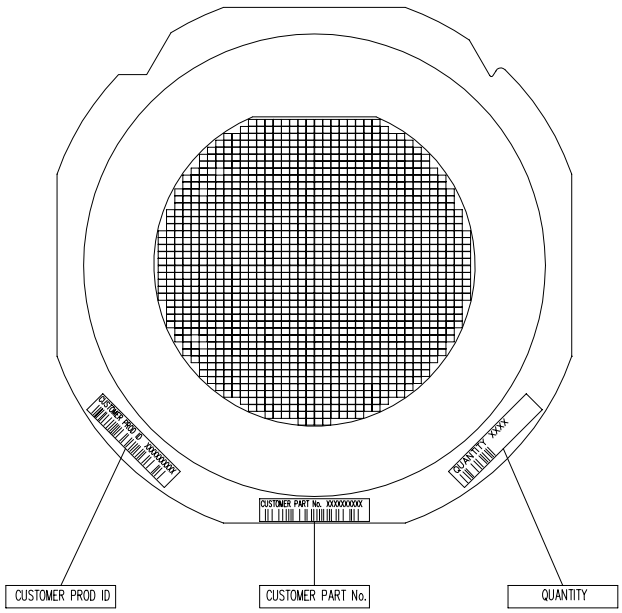
4 - Voltage code: Code = V_{RRM}

5 - Chip surface metallization (see Mechanical Data Table)

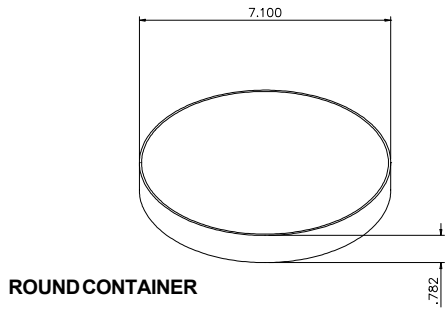
6 - Wafer Diameter in inches

7 - Packaging (see Packaging Table)

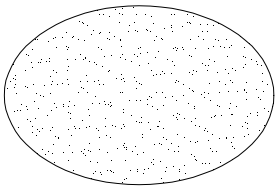
Wafer on Film



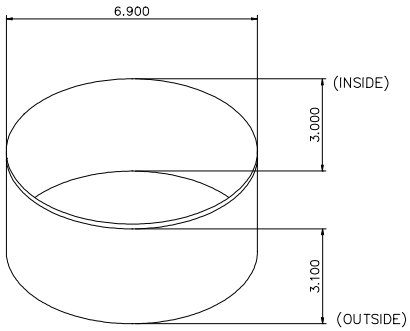
Wafer in Box

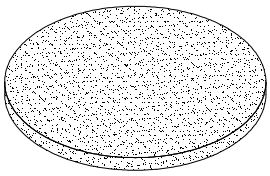


ROUND CONTAINER



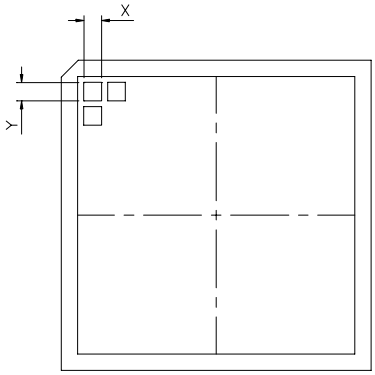
TYVEK DISK

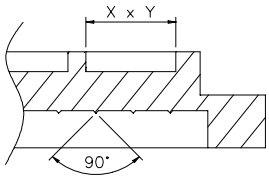




FOAM DISK

Die in Waffle Pack





CHIP TRAY POCKET

International
IOR Rectifier

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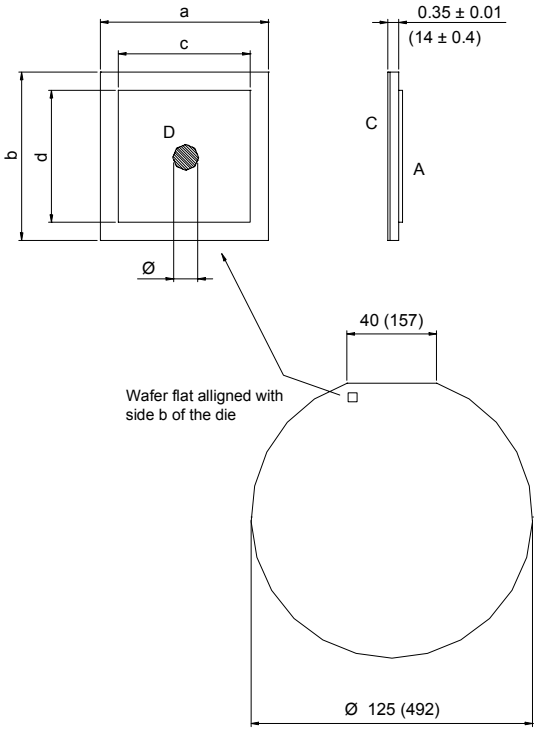
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Bulletin I0499J rev. A 05/01

International
IOR Rectifier

SC100.....5. Series

SCHOTTKY DIE 105 x 105 mils



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (MILS).

2. CONTROLLING DIMENSION: (MILS).

3. DIMENSIONS AND TOLERANCES:
   a = 2.67 + 0, - 0.01
   (105 + 0, - 0.4)
   b = 2.67 + 0, - 0.01
   (105 + 0, - 0.4)
   c = 2.51 + 0, - 0.01
   (99 + 0, - 0.4)
   d = 2.51 + 0, - 0.01
   (99 + 0, - 0.4)
   Ø = 1 ± 0.15
   (40 ± 6)

4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)
   D = Reject Ink Dot (only on non-conforming dies)

5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade
   Sawing Street
   0.05 + 0, - 0.005
   (2 + 0, - 0.2)

NOT TO SCALE

NOTE: 10 mils die thickness is available on specific request only.
Contact factory for information.

Electrical Characteristics

Device #	T_J Max. (°C)	V_R (V)	Typ. I_R @ 25°C (µA)	Typ. I_R @ 125°C (mA)	Max. V_F @ I_F (V)	Package Style
SC100**R**015x5x	125	15	n.a. contact factory			
SC100**S**020x5x	150	20	n.a. contact factory			
SC100**S**030x5x	150	30	n.a. contact factory			
SC100**S**045x5x	150	45	120	55	0.76 @ 30A	TO-220
SC100**S**060x5x	150	60		n.a. contact factory		
SC100**H**045x5x	175	45	n.a. contact factory			
SC100**H**100x5x	175	100	7	4.5	0.95 @ 20A	TO-220
SC100**H**150x5x	175	150	n.a. contact factory			

Mechanical Data

Device #		Metal Thickness Front Metal			Metal Thickness Back Metal		
SC100xxxx**A**5x	Wire Bondable	–	Al 30 kÅ	–	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ
SC100xxxx**S**5x	Solderable	Ti 2 kÅ	Ni 1 kÅ	Ag 35 kÅ	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ

Recommended Storage Environment: Store in original container, in dessicated nitrogen, with no contamination.
Shelf life for parts stored in above condition is 2 years.
If the storage is done in normal atmosphere shelf life is reduced to six months.

Packaging

Device #	Description	Minimum Order Quantity Die in Sale Package
SC100xxxxx5**B**	Inked Probed Unsawn Wafer (Wafer in Box)	1400
SC100xxxxx5**R**	Probed Die in Tape & Reel	8,000
SC100xxxxx5**P**	Probed Die in Waffle Pack	1400
SC100xxxxx5**F**	Inked Probed Sawn Wafer on Film	1400

Ordering Information Table

Device Code

SC	100	H	150	A	5	B
1	2	3	4	5	6	7

1 - Schottky Die

2 - Chip Dimension in Mils

3 - Process (see Electrical Characteristics Table)

H = 830 Process
R = OR'ing Process
S = Standard Process

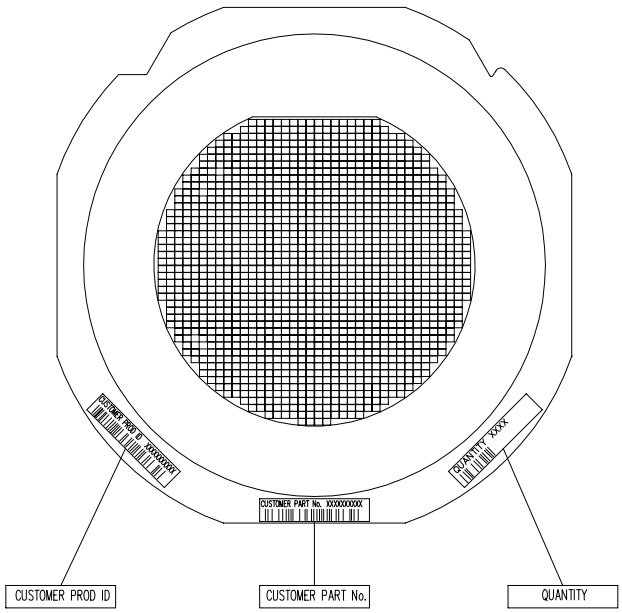
4 - Voltage code: Code = V_{RRM}

5 - Chip surface metallization (see Mechanical Data Table)

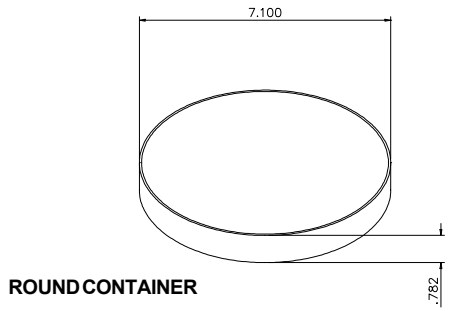
6 - Wafer Diameter in inches

7 - Packaging (see Packaging Table)

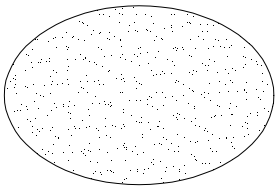
Wafer on Film



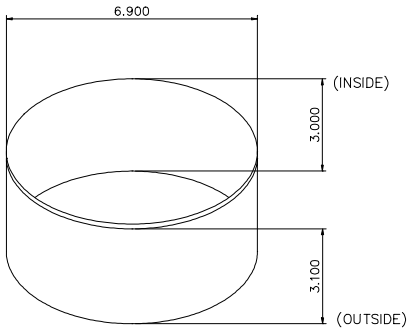
Wafer in Box

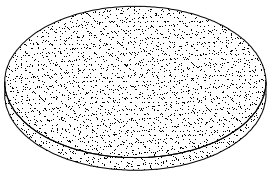


ROUND CONTAINER



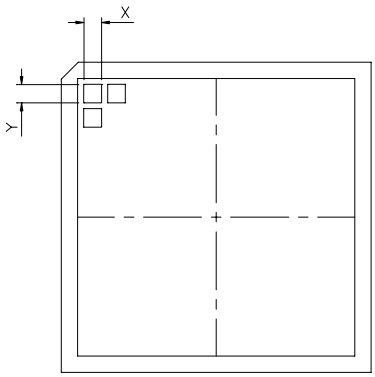
TYVEK DISK

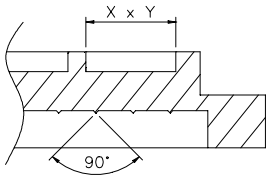




FOAM DISK

Die in Waffle Pack





CHIP TRAY POCKET

International
IOR Rectifier

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IR ITALY: Via Liguria 49, 10071 Borgaro, Torino. Tel: ++ 39 11 4510111. Fax: ++ 39 11 4510220.
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171. Tel: 81 3 3983 0086.
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower,13-11, Singapore 237994. Tel: ++ 65 838 4630.
IR TAIWAN: 16 Fl. Suite D.207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan. Tel: 886 2 2377 9936.

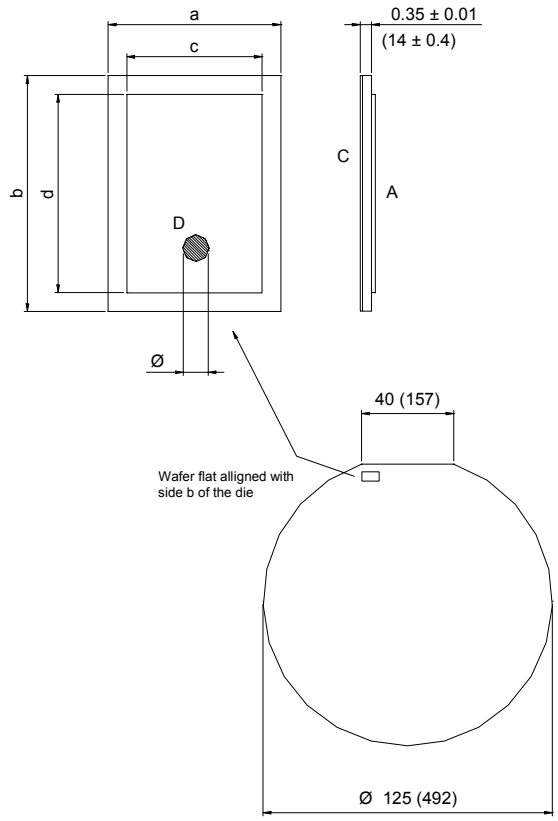
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Bulletin I0503J rev. C 05/01

International
IOR Rectifier

SC105.....5. Series

SCHOTTKY DIE 105 x 125 mils



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (MILS).

2. CONTROLLING DIMENSION: (MILS).

3. DIMENSIONS AND TOLERANCES:
   a = 3.18 + 0, - 0.01
   (125 + 0, - 0.4)
   b = 2.67 + 0, - 0.01
   (105 + 0, - 0.4)
   c = 3.02 + 0, - 0.01
   (119 + 0, - 0.4)
   d = 2.51 + 0, - 0.01
   (99 + 0, - 0.4)
   Ø = 1 ± 0.15
   (40 ± 6)

4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)
   D = Reject Ink Dot (only on non-conforming dies)

5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade
   Sawing Street
   0.05 + 0, - 0.005
   (2 + 0, - 0.2)

NOT TO SCALE

NOTE: 10 mils die thickness is available on specific request only.
Contact factory for information.

Electrical Characteristics

Device #	T_J Max. (°C)	V_R (V)	Typ. I_R @ 25°C (µA)	Typ. I_R @ 125°C (mA)	Max. V_F @ I_F (V)	Package Style
SC105**R**015x5x	125	15	n.a. contact factory			
SC105**S**020x5x	150	20	700	180	0.51 @ 40A	TO-220
SC105**S**030x5x	150	30	220	100	0.49 @ 15A	TO-220
SC105**S**045x5x	150	45	150	75	0.54 @ 15A	TO-247
SC105**S**060x5x	150	60	110	60	0.60 @ 15A	TO-247
SC105**H**045x5x	175	45	35	10	0.62 @ 15A	TO-220
SC105**H**100x5x	175	100	12	7	0.86 @ 15A	TO-247
SC105**H**150x5x	175	150	15	10	1.0 @ 15A	TO-220

Mechanical Data

Device #		Metal Thickness Front Metal			Metal Thickness Back Metal		
SC105xxxx**A**5x	Bondable	–	Al/Si 30 kÅ	–	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ
SC105xxxx**S**5x	Solderable	Ti 2 kÅ	Ni 1 kÅ	Ag 35 kÅ	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ

Recommended Storage Environment: Store in original container, in dessicated nitrogen, with no contamination.
Shelf life for parts stored in above condition is 2 years.
If the storage is done in normal atmosphere shelf life is reduced to six months.

Packaging

Device #	Description	Minimum Order Quantity Die in Sale Package
SC105xxxxx5**B**	Inked Probed Unsawn Wafer (Wafer in Box)	1170
SC105xxxxx5**R**	Probed Die in Tape & Reel	8,000
SC105xxxxx5**P**	Probed Die in Waffle Pack	1170
SC105xxxxx5**F**	Inked Probed Sawn Wafer on Film	1170

Ordering Information Table

Device Code

SC	105	H	100	S	5	B
1	2	3	4	5	6	7

1 - Schottky Die

2 - Chip Dimension in Mils

3 - Process (see Electrical Characteristics Table)

H = 830 Process
R = OR'ing Process
S = Standard Process

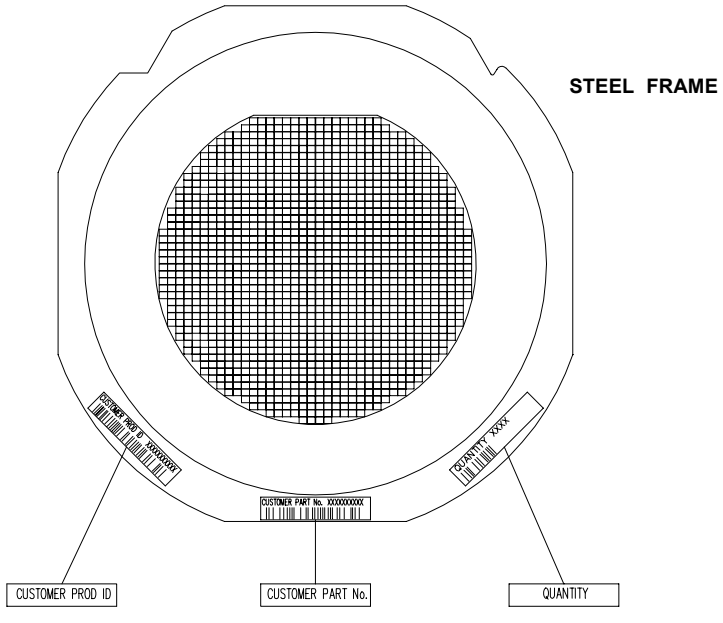
4 - Voltage code: Code = V_{RRM}

5 - Chip surface metallization (see Mechanical Data Table)

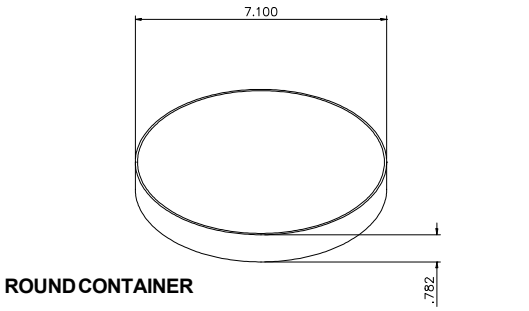
6 - Wafer Diameter in inches

7 - Packaging (see Packaging Table)

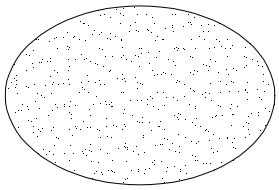
Wafer on Film



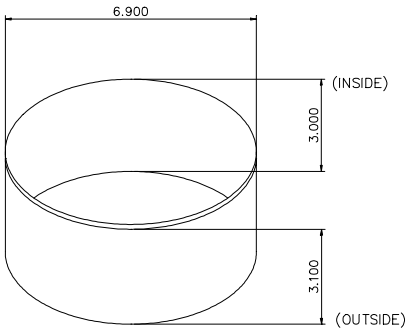
Wafer in Box

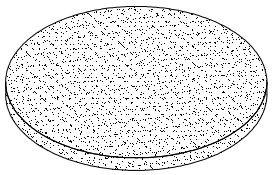


ROUND CONTAINER



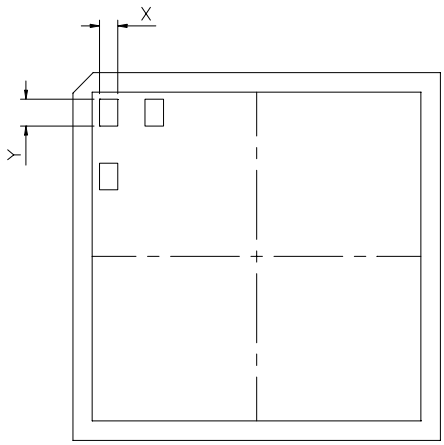
TYVEK DISK

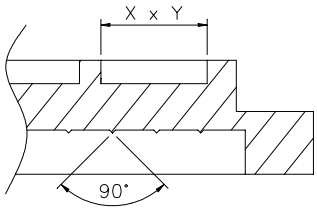




FOAM DISK

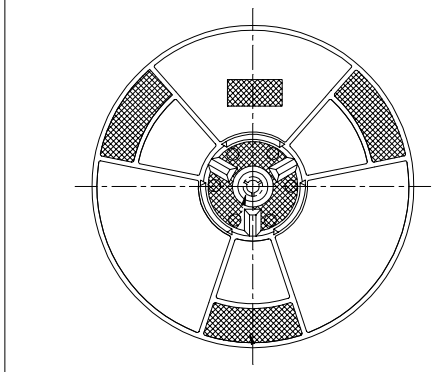
Die in Waffle Pack





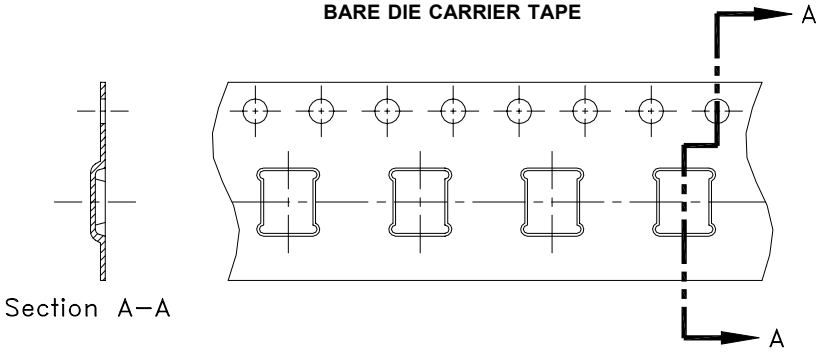
CHIP TRAY POCKET

Tape and Reel



REEL FRAME

BARE DIE CARRIER TAPE



International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 U.S.A. Tel: (310) 322 3331. Fax: (310) 322 3332.
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, U.K. Tel: ++ 44 1883 732020. Fax: ++ 44 1883 733408.
IR CANADA: 15 Lincoln Court, Brampton, Markham, Ontario L6T3Z2. Tel: (905) 453 2200. Fax: (905) 475 8801.
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg. Tel: ++ 49 6172 96590. Fax: ++ 49 6172 965933.
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino. Tel: ++ 39 11 4510111. Fax: ++ 39 11 4510220.
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171. Tel: 81 3 3983 0086.
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower,13-11, Singapore 237994. Tel: ++ 65 838 4630.
IR TAIWAN: 16 Fl. Suite D.207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan. Tel: 886 2 2377 9936.

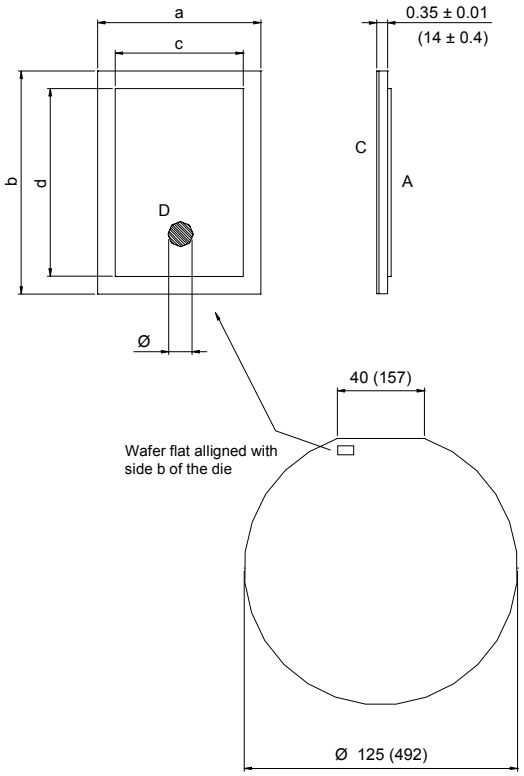
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Bulletin I0506J rev. C 05/01

International
IOR Rectifier

SC170.....5. Series

SCHOTTKY DIE 115 x 170 mils



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (MILS).
2. CONTROLLING DIMENSION: (MILS).
3. DIMENSIONS AND TOLERANCES:
   a = 4.32 + 0, - 0.01
   (170 + 0, - 0.4)
   b = 2.92 + 0, - 0.01
   (115 + 0, - 0.4)
   c = 4.17 + 0, - 0.01
   (164 + 0, - 0.4)
   d = 2.77 + 0, - 0.01
   (109 + 0, - 0.4)
   Ø = 1 ± 0.15
   (40 ± 6)
4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)
   D = Reject Ink Dot (only on non-conforming dies)
5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade
   Sawing Street
   0.05 + 0, - 0.005
   (2 + 0, - 0.2)

NOT TO SCALE

NOTE: 10 mils die thickness is available on specific request only.
Contact factory for information.

Electrical Characteristics

Device #	T_J Max. (°C)	V_R (V)	Typ. I_R @ 25°C (µA)	Typ. I_R @ 125°C (mA)	Max. V_F @ I_F (V)	Package Style
SC170**R**015x5x	125	15	5000	600	0.41 @ 19A	TO-220
SC170**S**020x5x	150	20	n.a. contact factory			
SC170**S**030x5x	150	30	350	140	0.48 @ 20A	TO-220
SC170**S**045x5x	150	45	250	100	0.57 @ 20A	TO-220
SC170**S**060x5x	150	60	140	70	0.61 @ 20A	TO-220
SC170**H**045x5x	175	45	40	14	0.60 @ 18A	TO-220
SC170**H**100x5x	175	100	15	8	0.80 @ 20A	TO-220
SC170**H**150x5x	175	150	n.a. contact factory			

Mechanical Data

Device #		Metal Thickness Front Metal			Metal Thickness Back Metal		
SC170xxxx**A**5x	Wire Bondable	–	Al 30 kÅ	–	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ
SC170xxxx**S**5x	Solderable	Ti 2 kÅ	Ni 1 kÅ	Ag 35 kÅ	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ

Recommended Storage Environment: Store in original container, in dessicated nitrogen, with no contamination.
Shelf life for parts stored in above condition is 2 years.
If the storage is done in normal atmosphere shelf life is reduced to six months.

Packaging

Device #	Description	Minimum Order Quantity Die in Sale Package
SC170xxxxx5**B**	Inked Probed Unsawn Wafer (Wafer in Box)	800
SC170xxxxx5**R**	Probed Die in Tape & Reel	n.a.
SC170xxxxx5**P**	Probed Die in Waffle Pack	800
SC170xxxxx5**F**	Inked Probed Sawn Wafer on Film	800

Ordering Information Table

Device Code

SC	170	H	100	S	5	B
1	2	3	4	5	6	7

1 - Schottky Die

2 - Chip Dimension in Mils

3 - Process (see Electrical Characteristics Table)

H = 830 Process
R = OR'ing Process
S = Standard Process

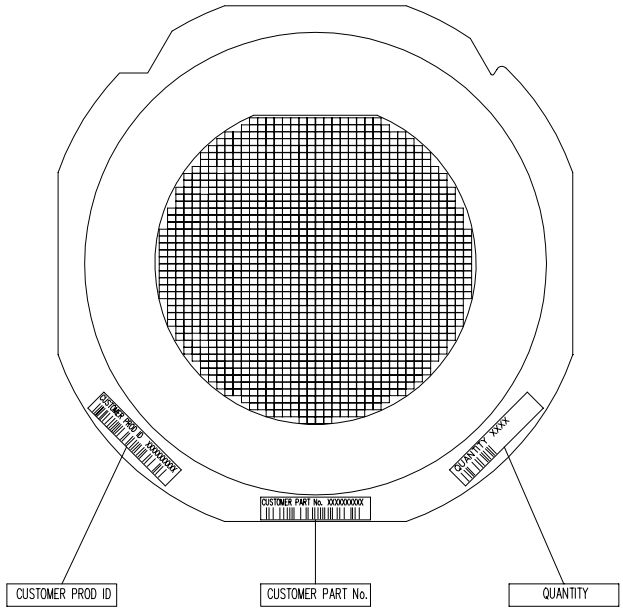
4 - Voltage code: Code = V_{RRM}

5 - Chip surface metallization (see Mechanical Data Table)

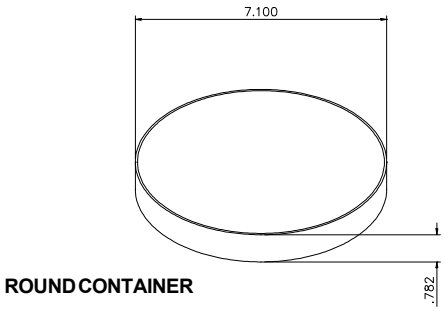
6 - Wafer Diameter in inches

7 - Packaging (see Packaging Table)

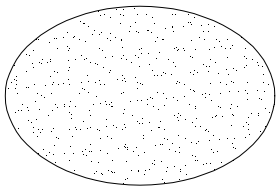
Wafer on Film



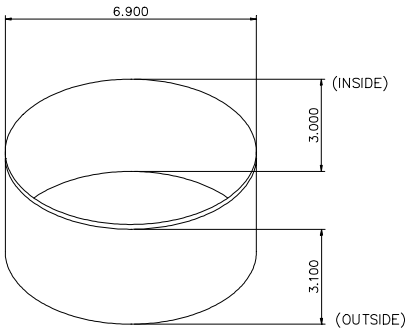
Wafer in Box

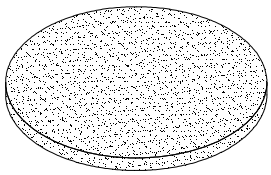


ROUND CONTAINER



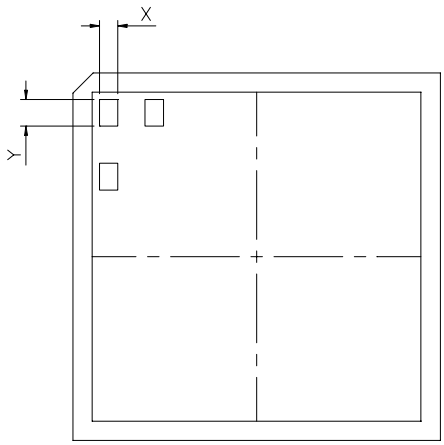
TYVEK DISK

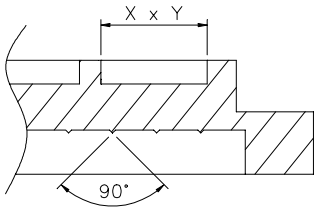




FOAM DISK

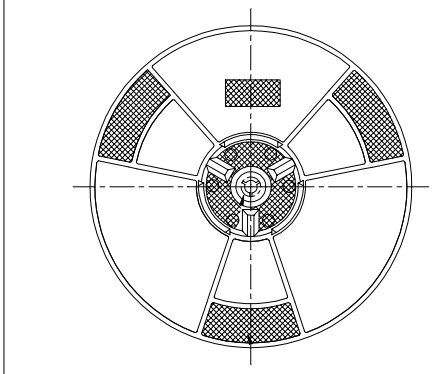
Die in Waffle Pack





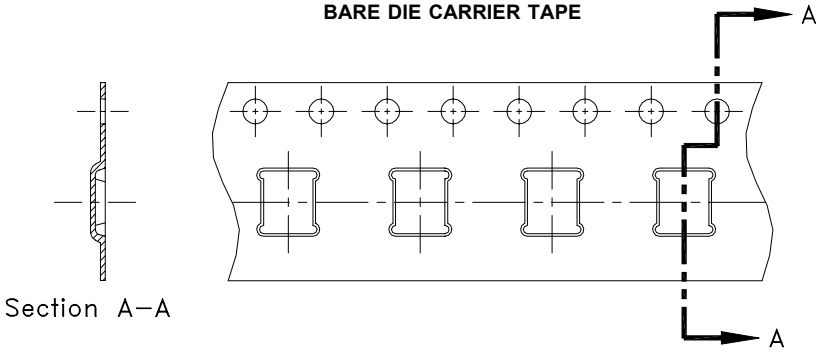
CHIP TRAY POCKET

Tape and Reel



REEL FRAME

BARE DIE CARRIER TAPE



International
IOR Rectifier

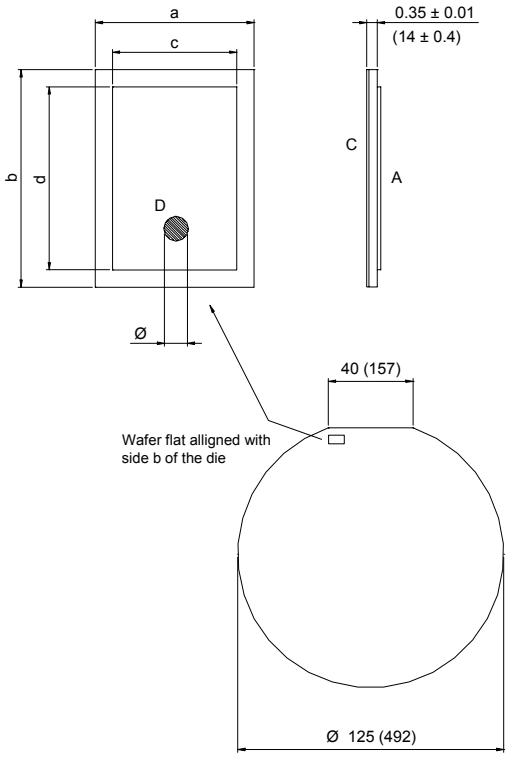
WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 U.S.A. Tel: (310) 322 3331. Fax: (310) 322 3332.
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, U.K. Tel: ++ 44 1883 732020. Fax: ++ 44 1883 733408.
IR CANADA: 15 Lincoln Court, Brampton, Markham, Ontario L6T3Z2. Tel: (905) 453 2200. Fax: (905) 475 8801.
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg. Tel: ++ 49 6172 96590. Fax: ++ 49 6172 965933.
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino. Tel: ++ 39 11 4510111. Fax: ++ 39 11 4510220.
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171. Tel: 81 3 3983 0086.
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower,13-11, Singapore 237994. Tel: ++ 65 838 4630.
IR TAIWAN: 16 Fl. Suite D.207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan. Tel: 886 2 2377 9936.

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Data and specifications subject to change without notice.

International
IOR Rectifier

SC180.....5. Series

SCHOTTKY DIE 150 x 180 mils



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (MILS).
2. CONTROLLING DIMENSION: (MILS).
3. DIMENSIONS AND TOLERANCES:
   a = 4.57 + 0, - 0.01
   (180 + 0, - 0.4)
   b = 3.81 + 0, - 0.01
   (150 + 0, - 0.4)
   c = 4.42 + 0, - 0.01
   (174 + 0, - 0.4)
   d = 3.66 + 0, - 0.01
   (144 + 0, - 0.4)
   Ø = 1 ± 0.15
   (40 ± 6)
4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)
   D = Reject Ink Dot (only on non-conforming dies)
5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade
   Sawing Street
   0.05 + 0, - 0.005
   (2 + 0, - 0.2)

NOT TO SCALE

NOTE: 10 mils die thickness is available on specific request only.
Contact factory for information.

Electrical Characteristics

Device #	T_J Max. (°C)	V_R (V)	Typ. I_R @ 25°C (µA)	Typ. I_R @ 125°C (mA)	Max. V_F @ I_F (V)	Package Style
SC180**R**015x5x	125	15	n.a. contact factory			
SC180**S**020x5x	150	20	n.a. contact factory			
SC180**S**030x5x	150	30	n.a. contact factory			
SC180**S**045x5x	150	45	300	145	0.49 @ 20A	TO-247
SC180**S**060x5x	150	60	250	130	0.53 @ 20A	TO-247
SC180**H**045x5x	175	45	40	35	0.64 @ 30A	DO-4
SC180**H**100x5x	175	100	20	13	0.77 @ 20A	TO-247
SC180**H**150x5x	175	150	n.a. contact factory			

Mechanical Data

Device #		Metal Thickness Front Metal			Metal Thickness Back Metal		
SC180xxxx**A**5x	Wire Bondable	–	Al 30 kÅ	–	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ
SC180xxxx**S**5x	Solderable	Ti 2 kÅ	Ni 1 kÅ	Ag 35 kÅ	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ

Recommended Storage Environment: Store in original container, in dessicated nitrogen, with no contamination.
Shelf life for parts stored in above condition is 2 years.
If the storage is done in normal atmosphere shelf life is reduced to six months.

Packaging

Device #	Description	Minimum Order Quantity Die in Sale Package
SC180xxxxx5**B**	Inked Probed Unsawn Wafer (Wafer in Box)	560
SC180xxxxx5**R**	Probed Die in Tape & Reel	n.a.
SC180xxxxx5**P**	Probed Die in Waffle Pack	560
SC180xxxxx5**F**	Inked Probed Sawn Wafer on Film	560

Ordering Information Table

Device Code

SC	180	H	100	S	5	B
1	2	3	4	5	6	7

1 - Schottky Die

2 - Chip Dimension in Mils

3 - Process (see Electrical Characteristics Table)

H = 830 Process
R = OR' ing Process
S = Standard Process

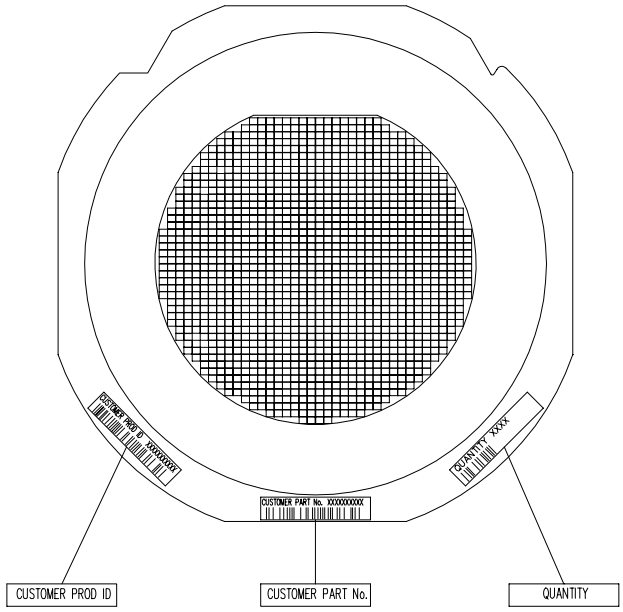
4 - Voltage code: Code = V_{RRM}

5 - Chip surface metallization (see Mechanical Data Table)

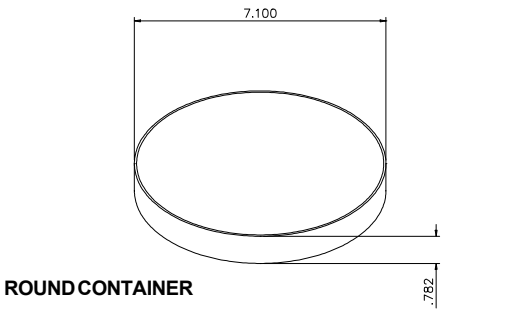
6 - Wafer Diameter in inches

7 - Packaging (see Packaging Table)

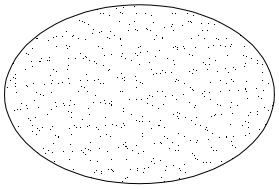
Wafer on Film



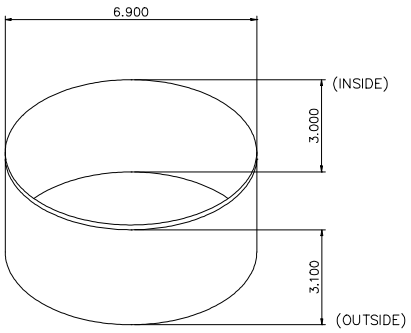
Wafer in Box

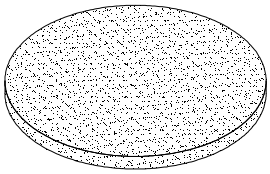


ROUND CONTAINER



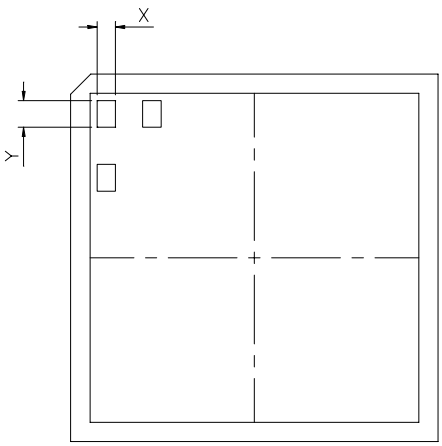
TYVEK DISK

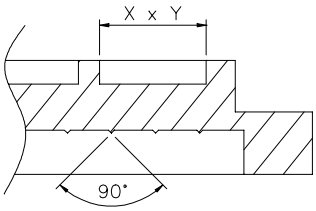




FOAM DISK

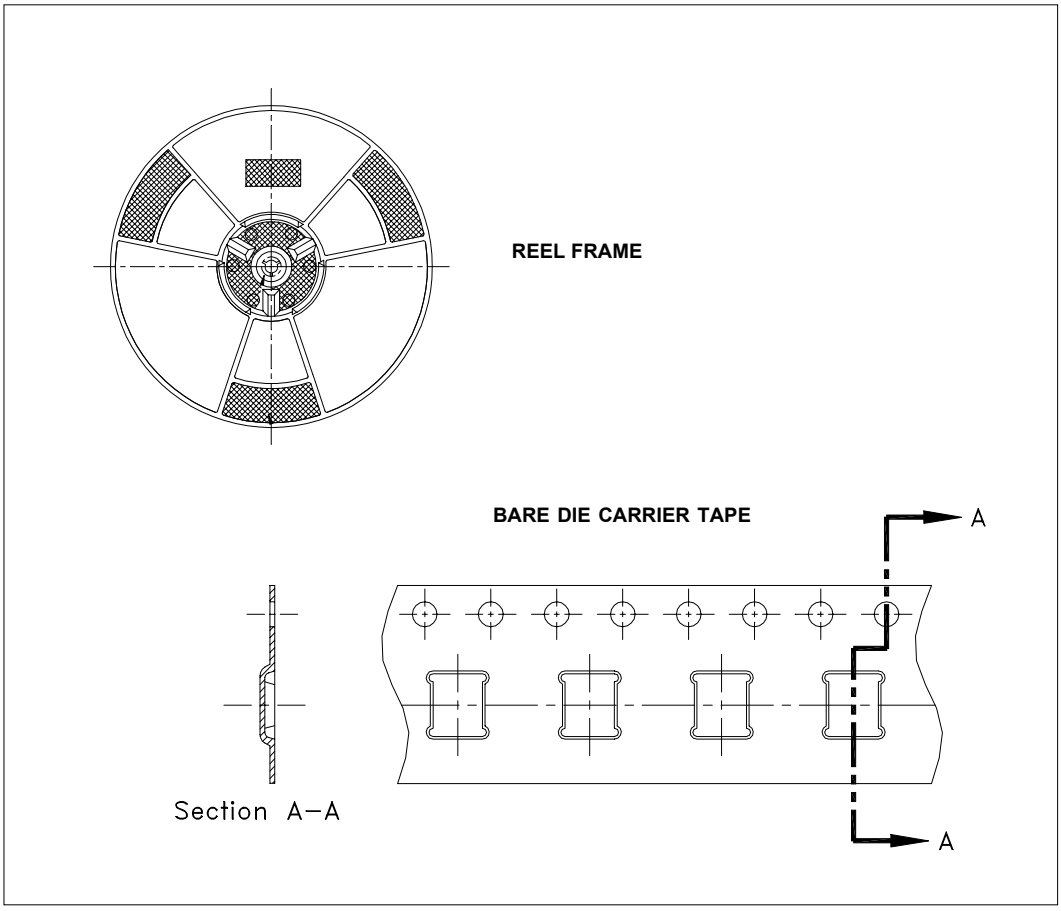
Tape and Reel





CHIP TRAY POCKET

Die in Waffle Pack



International
IOR Rectifier

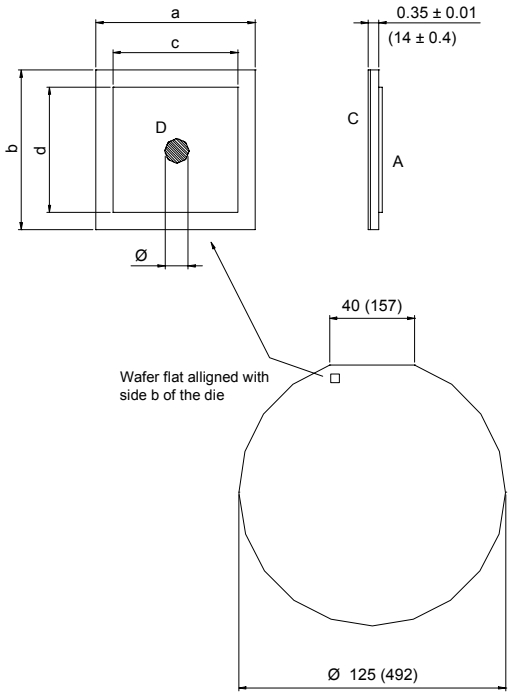
WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 U.S.A. Tel: (310) 322 3331. Fax: (310) 322 3332.
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, U.K. Tel: ++ 44 1883 732020. Fax: ++ 44 1883 733408.
IR CANADA: 15 Lincoln Court, Brampton, Markham, Ontario L6T3Z2. Tel: (905) 453 2200. Fax: (905) 475 8801.
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg. Tel: ++ 49 6172 96590. Fax: ++ 49 6172 965933.
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino. Tel: ++ 39 11 4510111. Fax: ++ 39 11 4510220.
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171. Tel: 81 3 3983 0086.
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower,13-11, Singapore 237994. Tel: ++ 65 838 4630.
IR TAIWAN: 16 Fl. Suite D.207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan. Tel: 886 2 2377 9936.

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International
IOR Rectifier

SC200.....5. Series

SCHOTTKY DIE 200 x 200 mils



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (MILS).

2. CONTROLLING DIMENSION: (MILS).

3. DIMENSIONS AND TOLERANCES:
   a = 5.08 + 0, - 0.01
   (200 + 0, - 0.4)
   b = 5.08 + 0, - 0.01
   (200 + 0, - 0.4)
   c = 4.57 + 0, - 0.01
   (180 + 0, - 0.4)
   d = 4.57 + 0, - 0.01
   (180 + 0, - 0.4)
   Ø = 1 ± 0.15
   (40 ± 6)

4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)
   D = Reject Ink Dot (only on non-conforming dies)

5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade
   Sawing Street
   0.05 + 0, - 0.005
   (2 + 0, - 0.2)

NOT TO SCALE

NOTE: 10 mils die thickness is available on specific request only.
Contact factory for information.

Electrical Characteristics

Device #	T_J Max. (°C)	V_R (V)	Typ. I_R @ 25°C (µA)	Typ. I_R @ 125°C (mA)	Max. V_F @ I_F (V)	Package Style
SC200**R**015x5x	125	15	7500	900	0.45 @ 80A	D-61
SC200**S**020x5x	150	20	1200	450	0.51 @ 80A	D-61
SC200**S**030x5x	150	30	600	270	0.55 @ 80A	D-61
SC200**S**045x5x	150	45	400	210	0.66 @ 80A	D-61
SC200**S**060x5x	150	60	n.a. contact factory			
SC200**H**045x5x	175	45	70	26	0.74 @ 80A	D-61
SC200**H**100x5x	175	100	30	18	0.89 @ 60A	D-61
SC200**H**150x5x	175	150	15	10	1.14 @ 80A	D-61

Mechanical Data

Device #		Metal Thickness Front Metal			Metal Thickness Back Metal		
SC200xxxx**A**5x	Wire Bondable	–	Al 30 kÅ	–	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ
SC200xxxx**S**5x	Solderable	Ti 2 kÅ	Ni 1 kÅ	Ag 35 kÅ	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ

Recommended Storage Environment: Store in original container, in dessicated nitrogen, with no contamination.

Shelf life for parts stored in above condition is 2 years.

If the storage is done in normal atmosphere shelf life is reduced to six months.

Packaging

Device #	Description	Minimum Order Quantity Die in Sale Package
SC200xxxxx5**B**	Inked Probed Unsawn Wafer (Wafer in Box)	350
SC200xxxxx5**R**	Probed Die in Tape & Reel	8,000
SC200xxxxx5**P**	Probed Die in Waffle Pack	350
SC200xxxxx5**F**	Inked Probed Sawn Wafer on Film	350

Ordering Information Table

Device Code

SC	200	S	100	A	5	B
1	2	3	4	5	6	7

1 - Schottky Die

2 - Chip Dimension in Mils

3 - Process (see Electrical Characteristics Table)

H = 830 Process
R = OR'ing Process
S = Standard Process

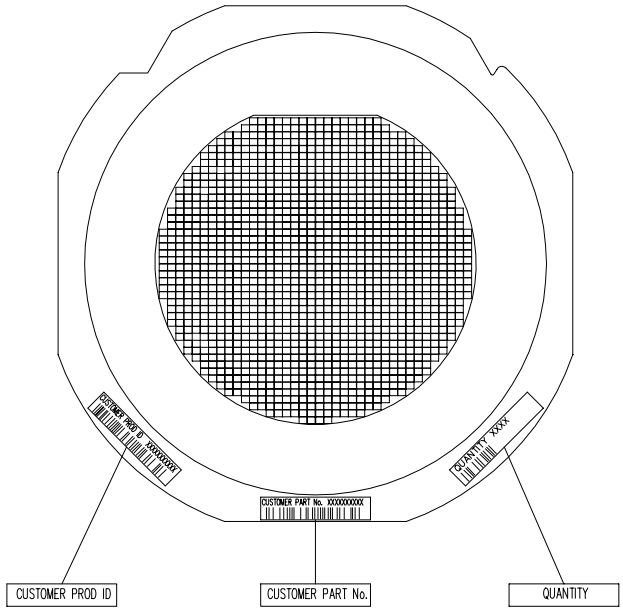
4 - Voltage code: Code = V_{RRM}

5 - Chip surface metallization (see Mechanical Data Table)

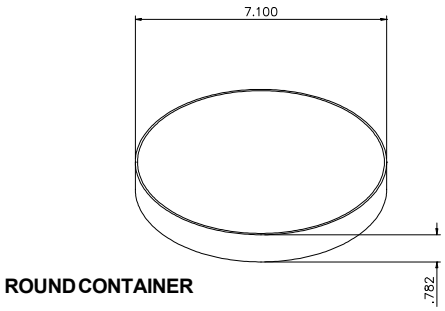
6 - Wafer Diameter in inches

7 - Packaging (see Packaging Table)

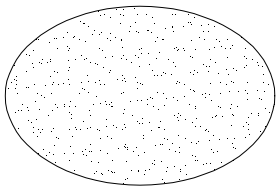
Wafer on Film



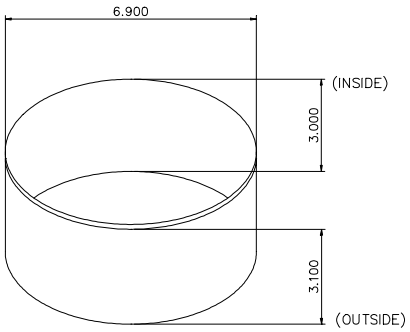
Wafer in Box

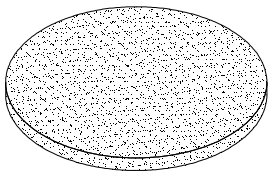


ROUND CONTAINER



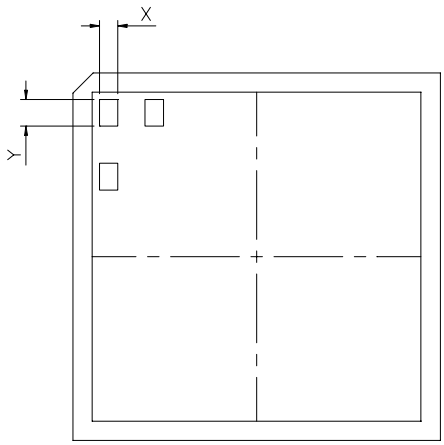
TYVEK DISK

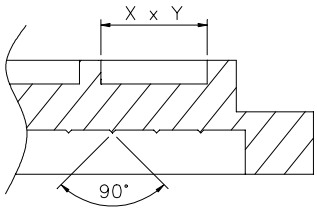




FOAM DISK

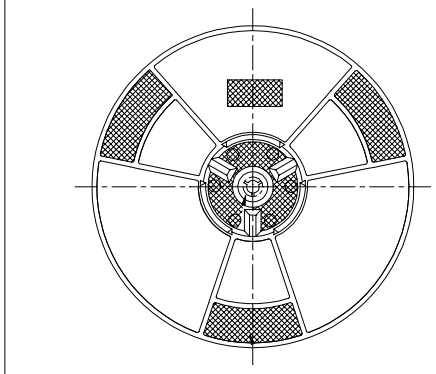
Die in Waffle Pack





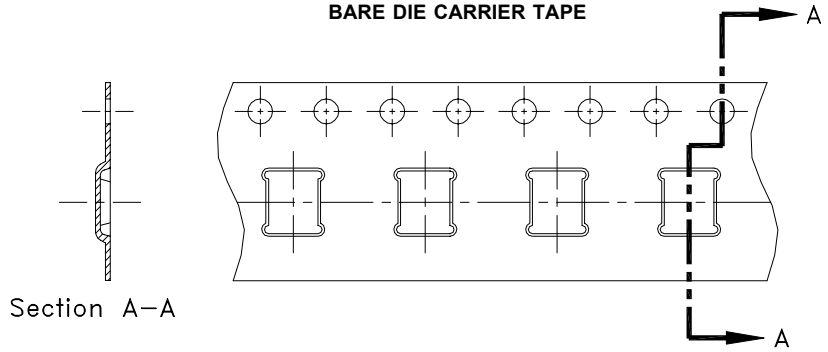
CHIP TRAY POCKET

Tape and Reel



REEL FRAME

BARE DIE CARRIER TAPE



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IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171. Tel: 81 3 3983 0086.
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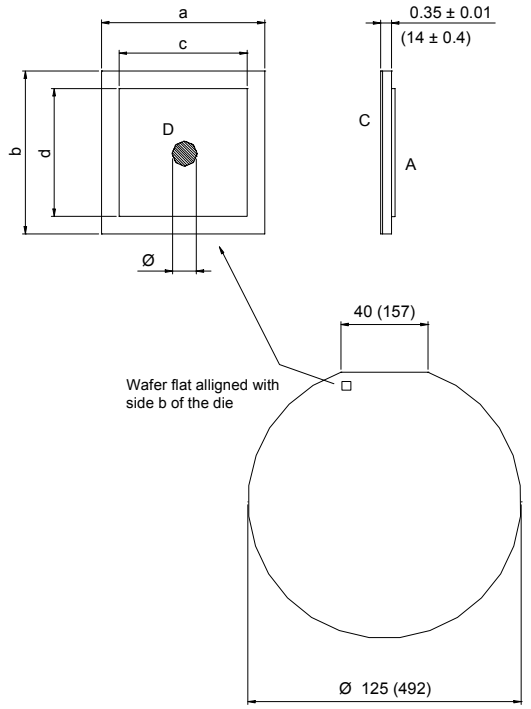
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Bulletin I0118J rev. A 05/01

International
IOR Rectifier

SC275.....5. Series

SCHOTTKY DIE 275 x 275 mils



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (MILS).
2. CONTROLLING DIMENSION: (MILS).
3. DIMENSIONS AND TOLERANCES:
   a = 6.98 + 0, - 0.01
   (275 + 0, - 0.4)
   b = 6.98 + 0, - 0.01
   (275 + 0, - 0.4)
   c = 6.48 + 0, - 0.01
   (269 + 0, - 0.4)
   d = 6.48 + 0, - 0.01
   (269 + 0, - 0.4)
   Ø = 1.5 ± 0.2
   (60 ± 8)
4. LETTER DESIGNATION:
   A = Anode (Top Metal)
   C = Cathode (Back Metal)
   D = Reject Ink Dot (only on non-conforming dies)
5. SAWING:
   Recommended Blade
   SEMITEC S1025 QS00 Blade
   Sawing Street
   0.05 + 0, - 0.005
   (2 + 0, - 0.2)

NOT TO SCALE

NOTE: 10 mils die thickness is available on specific request only.
Contact factory for information.

Electrical Characteristics

Device #	T_J Max. (°C)	V_R (V)	Typ. I_R @ 25°C (µA)	Typ. I_R @ 125°C (mA)	Max. V_F @ I_F (V)	Package Style
SC275**R**015x5x	125	15	n.a. contact factory			
SC275**S**020x5x	150	20	n.a. contact factory			
SC275**S**030x5x	150	30	1350	550	0.55 @ 150A	TO-249AA
SC275**S**045x5x	150	45	n.a. contact factory			
SC275**S**060x5x	150	60	n.a. contact factory			
SC275**H**045x5x	175	45	n.a. contact factory			
SC275**H**100x5x	175	100	n.a. contact factory			
SC275**H**150x5x	175	150	n.a. contact factory			

Mechanical Data

Device #		Metal Thickness Front Metal			Metal Thickness Back Metal		
SC275xxxx**A**5x	Bondable	–	Al/Si 30 kÅ	–	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ
SC275xxxx**S**5x	Solderable	Ti 2 kÅ	Ni 1 kÅ	Ag 35 kÅ	Cr 1 kÅ	Ni 2 kÅ	Ag 3 kÅ

Recommended Storage Environment: Store in original container, in dessicated nitrogen, with no contamination.
Shelf life for parts stored in above condition is 2 years.
If the storage is done in normal atmosphere shelf life is reduced to six months.

Packaging

Device #	Description	Minimum Order Quantity Die in Sale Package
SC275xxxxx5**B**	Inked Probed Unawn Wafer (Wafer in Box)	180
SC275xxxxx5**R**	Probed Die in Tape & Reel	n.a.
SC275xxxxx5**P**	Probed Die in Waffle Pack	366
SC275xxxxx5**F**	Inked Probed Sawn Wafer on Film	180

Ordering Information Table

Device Code

SC	275	S	030	S	5	B
1	2	3	4	5	6	7

1 - Schottky Die

2 - Chip Dimension in Mils

3 - Process (see Electrical Characteristics Table)

H = 830 Process
R = OR'ing Process
S = Standard Process

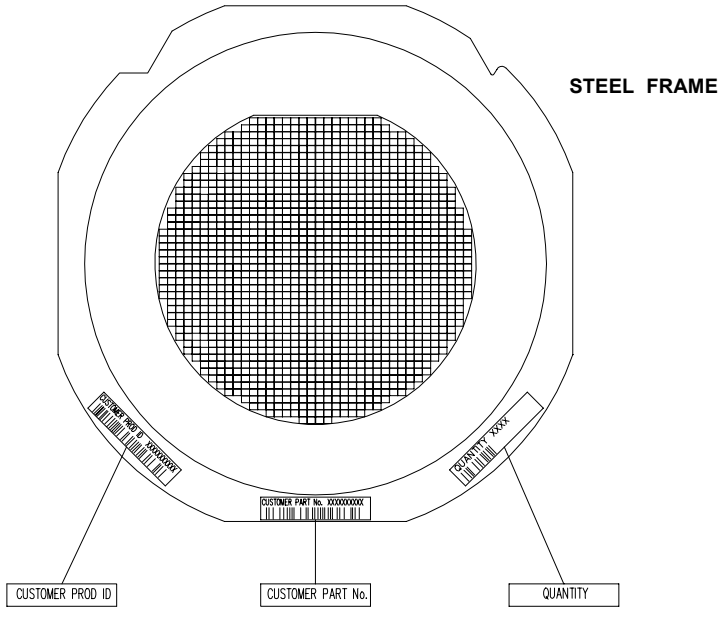
4 - Voltage code: Code = V_{RRM}

5 - Chip surface metallization (see Mechanical Data Table)

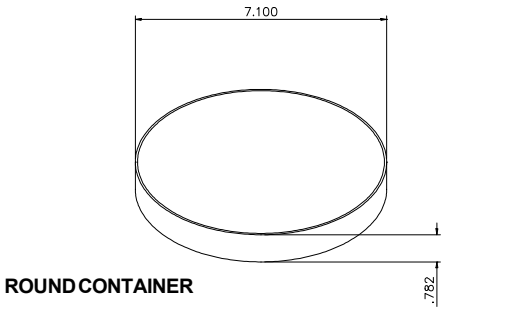
6 - Wafer Diameter in inches

7 - Packaging (see Packaging Table)

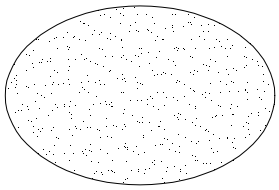
Wafer on Film



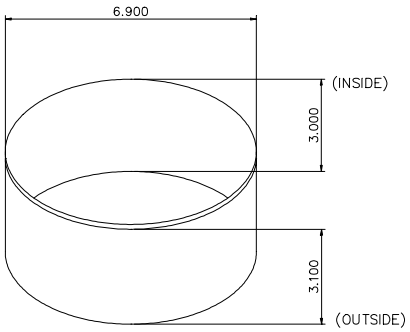
Wafer in Box

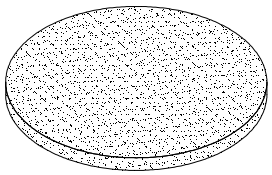


ROUND CONTAINER



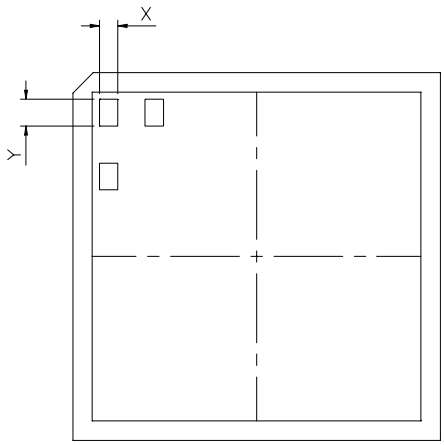
TYVEK DISK

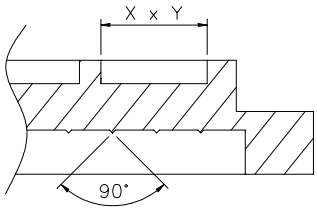




FOAM DISK

Die in Waffle Pack





CHIP TRAY POCKET

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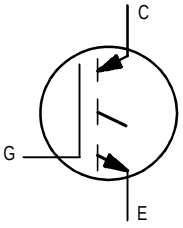
International
IOR Rectifier

IRG4IBC20W

INSULATED GATE BIPOLAR TRANSISTOR

Features

- Designed expressly for Switch-Mode Power Supply and PFC (power factor correction) applications
- 2.5kV, 60s insulation voltage ⑥
- Industry-benchmark switching losses improve efficiency of all power supply topologies
- 50% reduction of Eoff parameter
- Low IGBT conduction losses
- Latest-generation IGBT design and construction offers tighter parameters distribution, exceptional reliability
- Industry standard Isolated TO-220 Fullpak™ outline



n-channel

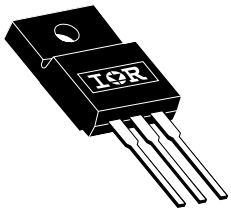
$V_{CES} = 600V$

$V_{CE(on)\ typ.} = 2.16V$

$@V_{GE} = 15V, I_C = 6.5A$

Benefits

- Lower switching losses allow more cost-effective operation than power MOSFETs up to 150 kHz ("hard switched" mode)
- Of particular benefit to single-ended converters and boost PFC topologies 150W and higher
- Low conduction losses and minimal minority-carrier recombination make these an excellent option for resonant mode switching as well (up to >>300 kHz)



TO-220 FULLPAK

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	11.8	A
I_C @ T_C = 100°C	Continuous Collector Current	6.2	
I_{CM}	Pulsed Collector Current ①	52	
I_{LM}	Clamped Inductive Load Current ②	52	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	200	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	34	W
P_D @ T_C = 100°C	Maximum Power Dissipation	14	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	——	3.7	°C/W
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	65	
Wt	Weight	2.0 (0.07)	——	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.48	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.16	2.6	V	I_C = 6.5A V_{GE} = 15V
		—	2.55	—		I_C = 13A See Fig.2, 5
		—	2.05	—		I_C = 6.5A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-8.8	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	5.5	8.3	—	S	V_{CE} = 100 V, I_C = 6.5A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	26	38	nC	I_C = 6.5A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	3.7	5.5		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	10	15		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	22	—	ns	
t_r	Rise Time	—	14	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	110	160		I_C = 6.5A, V_{CC} = 480V
t_f	Fall Time	—	64	96		V_{GE} = 15V, R_G = 50Ω
E_{on}	Turn-On Switching Loss	—	0.06	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.08	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	0.14	0.2		
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	T_J = 150°C,
t_r	Rise Time	—	15	—		I_C = 6.5A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	150	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	150	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.34	—	mJ	See Fig. 10, 11, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	490	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	38	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	8.8	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 50Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

⑥ t = 60s, f = 60Hz

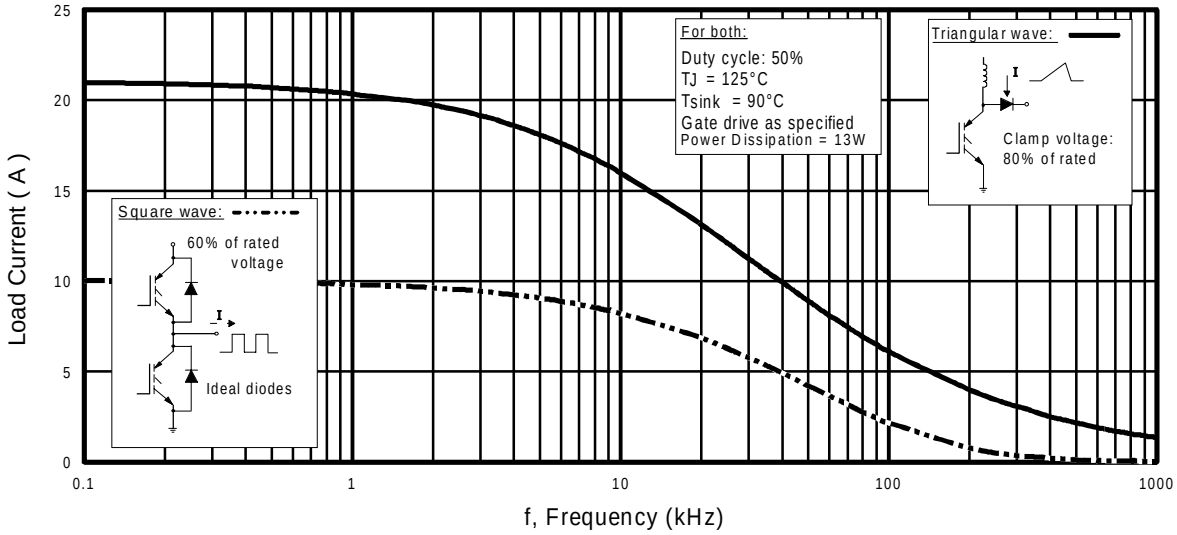


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

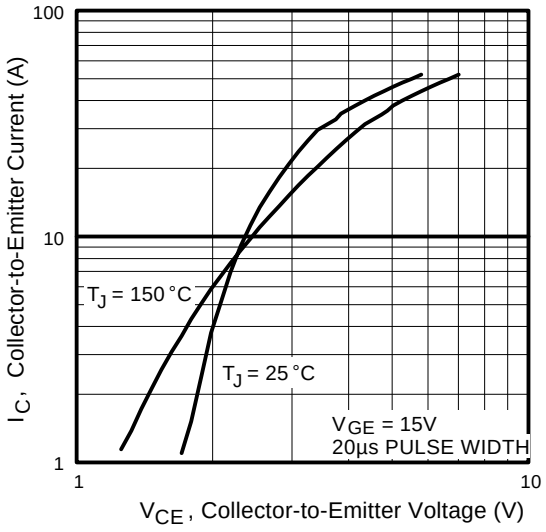


Fig. 2 - Typical Output Characteristics

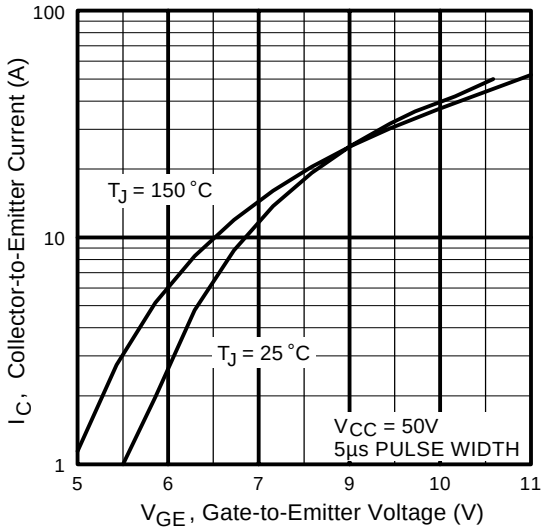


Fig. 3 - Typical Transfer Characteristics

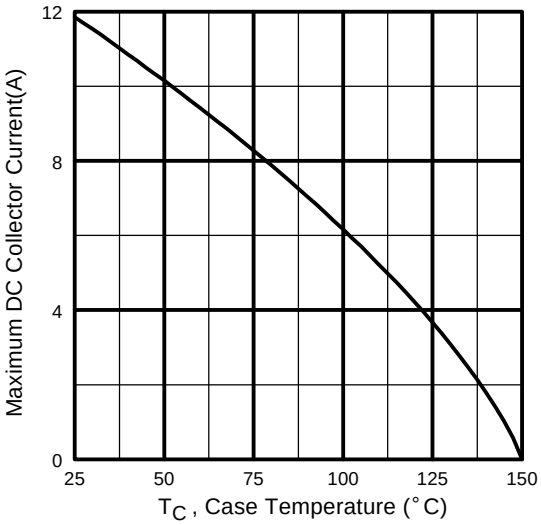


Fig. 4 - Maximum Collector Current vs. Case Temperature

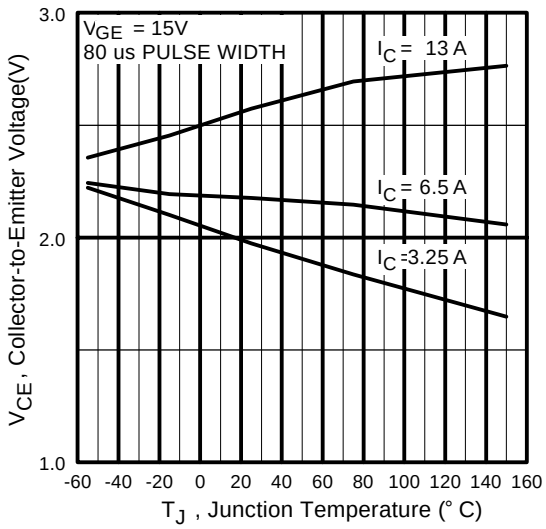


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

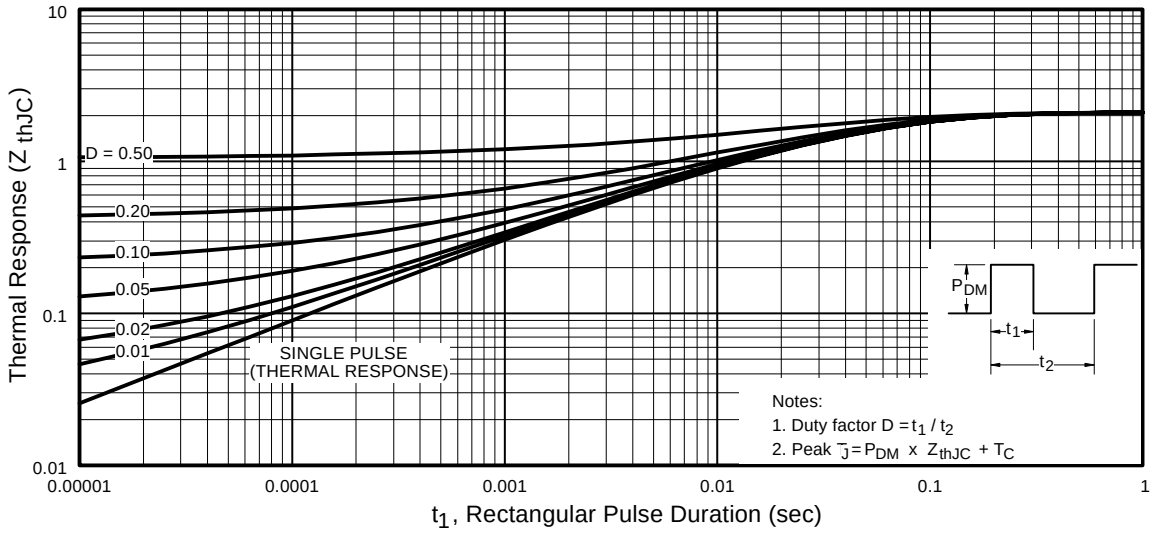


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

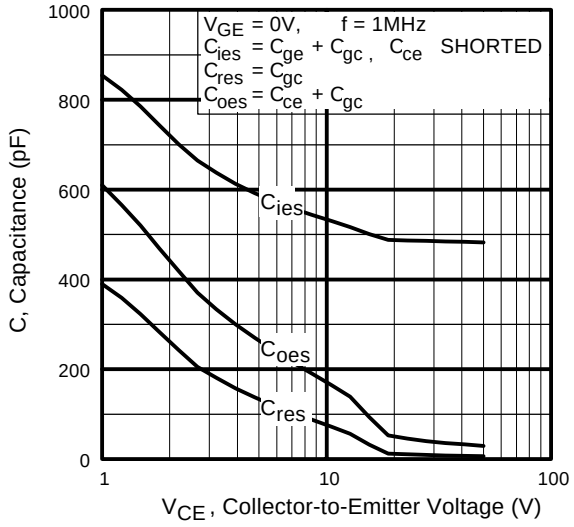


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

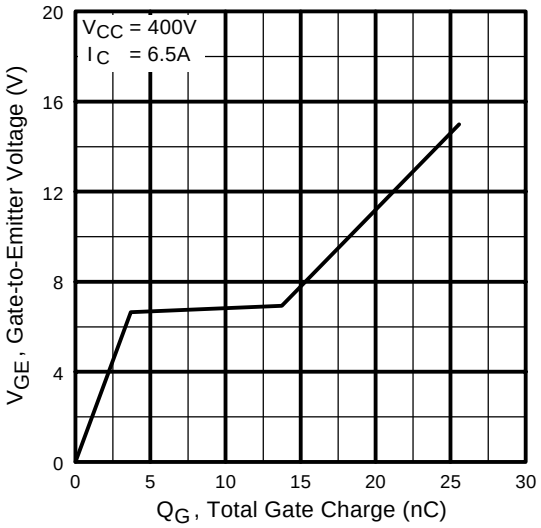


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

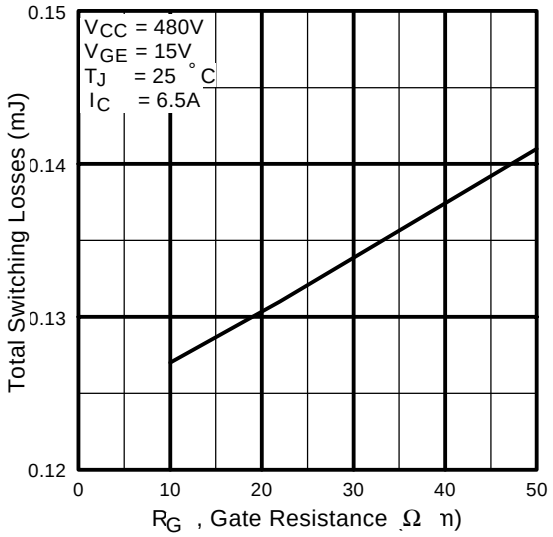


Fig. 9 - Typical Switching Losses vs. Gate Resistance

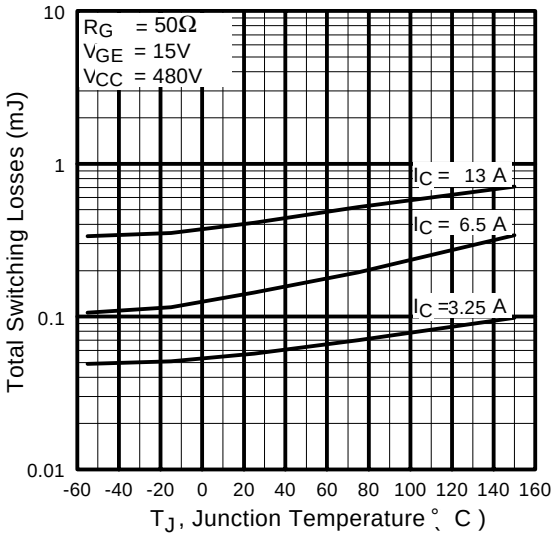


Fig. 10 - Typical Switching Losses vs. Junction Temperature

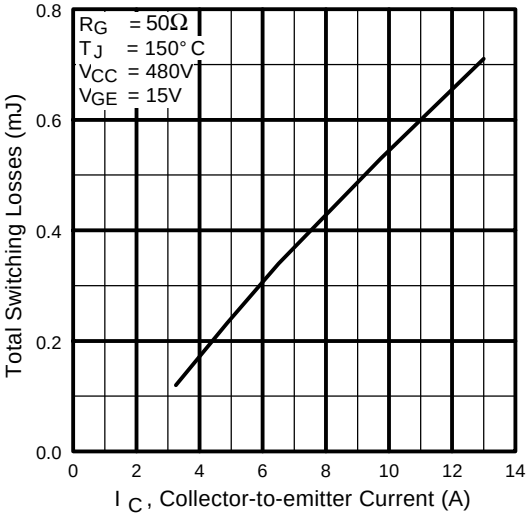


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

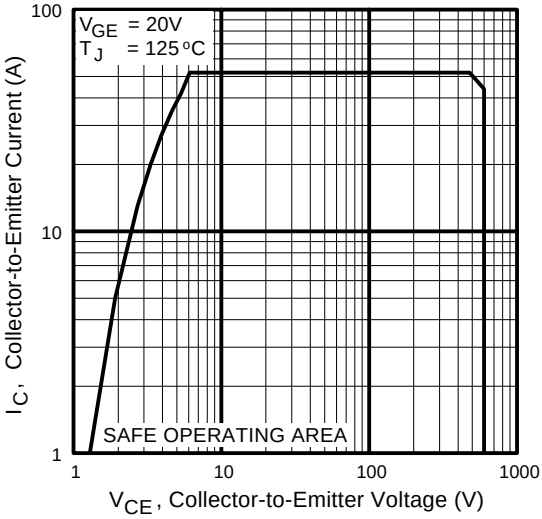


Fig. 12 - Turn-Off SOA

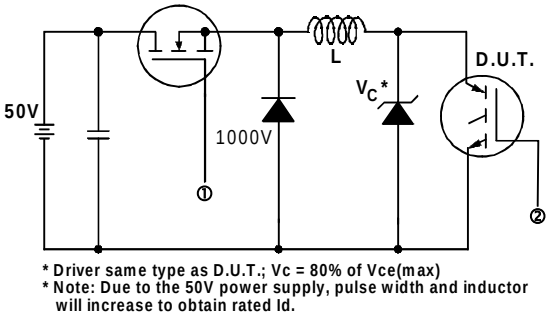


Fig. 13a - Clamped Inductive Load Test Circuit

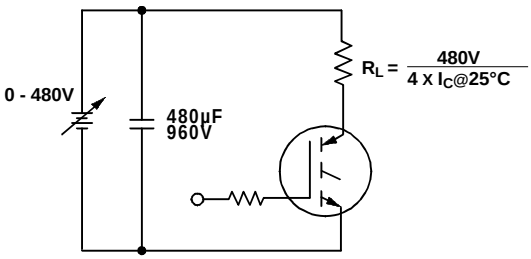


Fig. 13b - Pulsed Collector Current Test Circuit

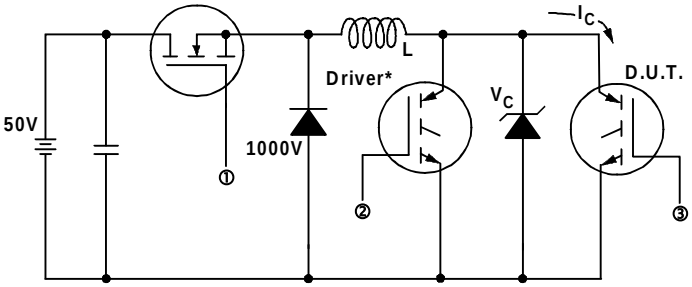


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

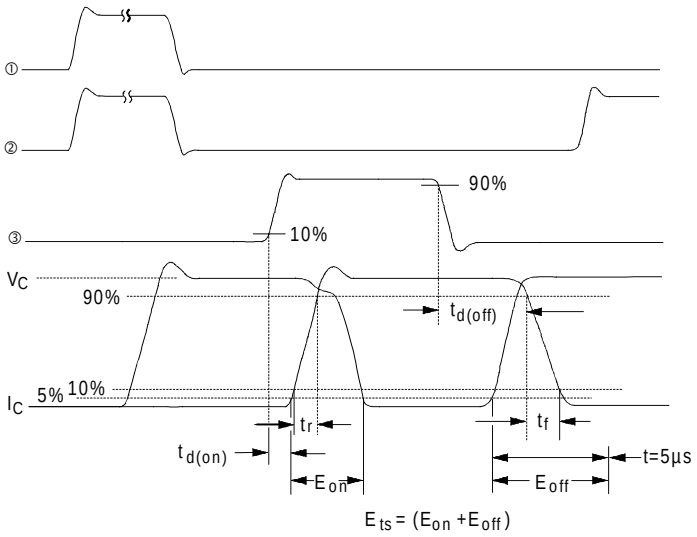
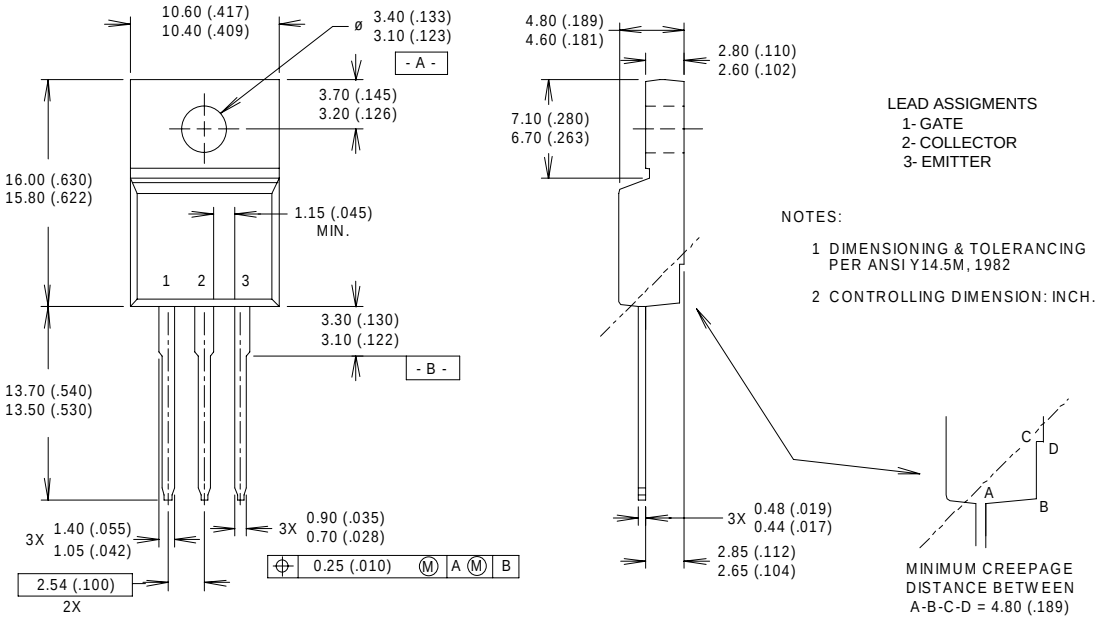


Fig. 14b - Switching Loss Waveforms

Case Outline — TO-220 FULLPAK



IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.

Data and specifications subject to change without notice. 12/00

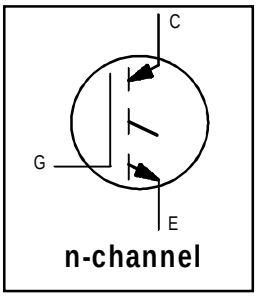
International
IOR Rectifier

IRG4BC20W

INSULATED GATE BIPOLAR TRANSISTOR

Features

- Designed expressly for Switch-Mode Power Supply and PFC (power factor correction) applications
- Industry-benchmark switching losses improve efficiency of all power supply topologies
- 50% reduction of Eoff parameter
- Low IGBT conduction losses
- Latest-generation IGBT design and construction offers tighter parameters distribution, exceptional reliability



n-channel

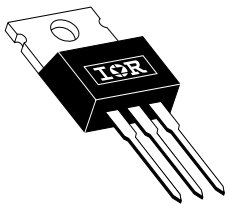
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.16V

@V_{GE} = 15V, I_C = 6.5A

Benefits

- Lower switching losses allow more cost-effective operation than power MOSFETs up to 150 kHz ("hard switched" mode)
- Of particular benefit to single-ended converters and boost PFC topologies 150W and higher
- Low conduction losses and minimal minority-carrier recombination make these an excellent option for resonant mode switching as well (up to >>300 kHz)



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	13	A
I_C @ T_C = 100°C	Continuous Collector Current	6.5	
I_{CM}	Pulsed Collector Current ①	52	
I_{LM}	Clamped Inductive Load Current ②	52	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	200	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	60	W
P_D @ T_C = 100°C	Maximum Power Dissipation	24	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	80	
Wt	Weight	2.0 (0.07)	—	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.48	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.16	2.6	V	I_C = 6.5A V_{GE} = 15V
		—	2.55	—		I_C = 13A See Fig.2, 5
		—	2.05	—		I_C = 6.5A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-8.8	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	5.5	8.3	—	S	V_{CE} = 100 V, I_C = 6.5A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	26	38	nC	I_C = 6.5A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	3.7	5.5		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	10	15		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	22	—	ns	
t_r	Rise Time	—	14	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	110	160		I_C = 6.5A, V_{CC} = 480V
t_f	Fall Time	—	64	96		V_{GE} = 15V, R_G = 50Ω
E_{on}	Turn-On Switching Loss	—	0.06	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.08	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	0.14	0.2		
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	T_J = 150°C,
t_r	Rise Time	—	15	—		I_C = 6.5A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	150	—		V_{GE} = 15V, R_G = 50Ω
t_f	Fall Time	—	150	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.34	—	mJ	See Fig. 10, 11, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	490	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	38	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	8.8	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 50Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

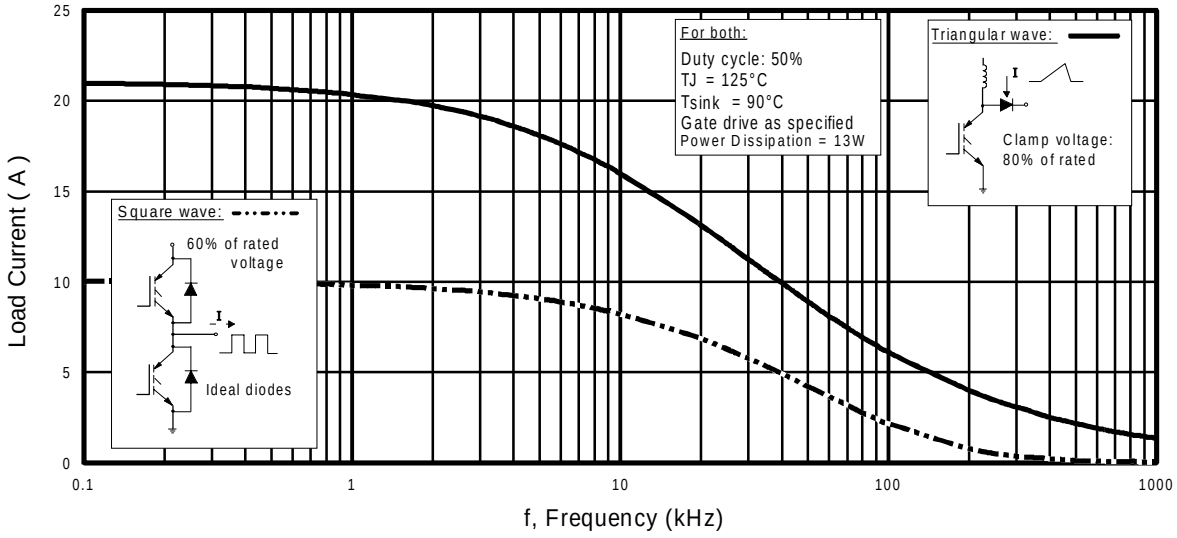


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

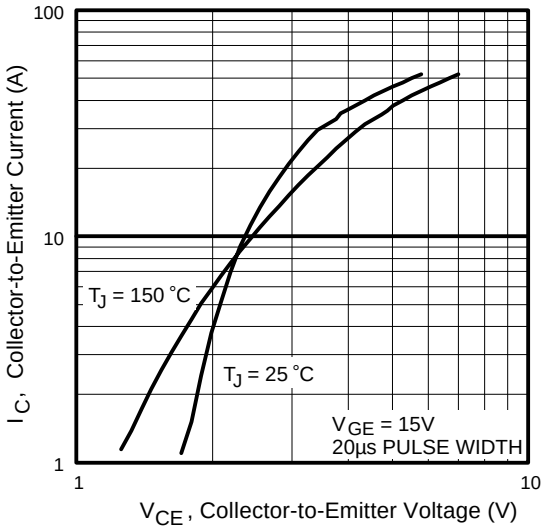


Fig. 2 - Typical Output Characteristics

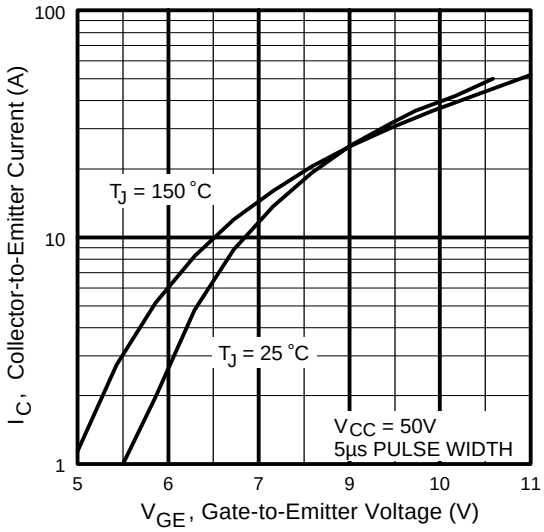


Fig. 3 - Typical Transfer Characteristics

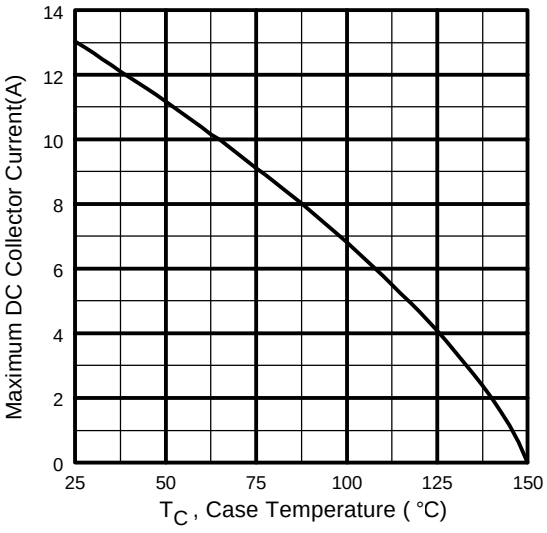


Fig. 4 - Maximum Collector Current vs. Case Temperature

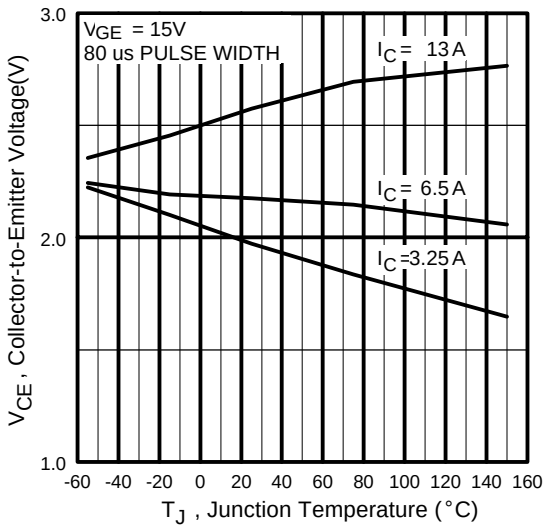


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

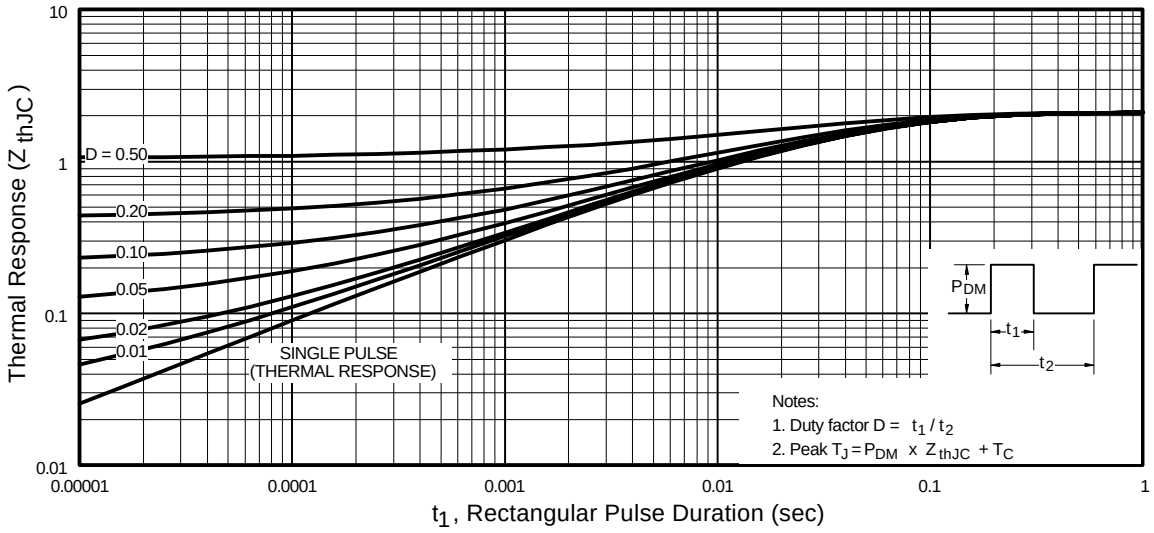


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

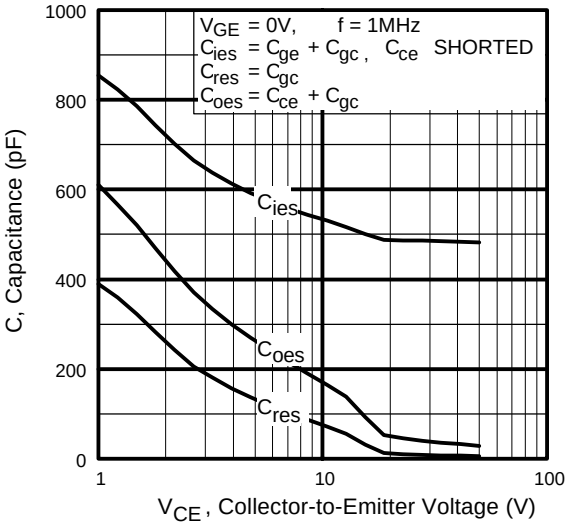


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

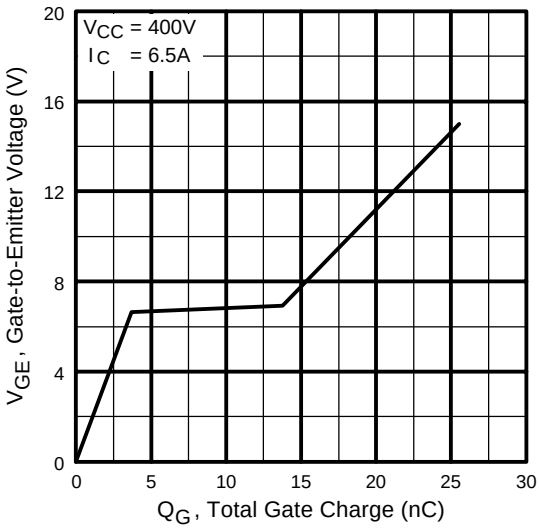


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

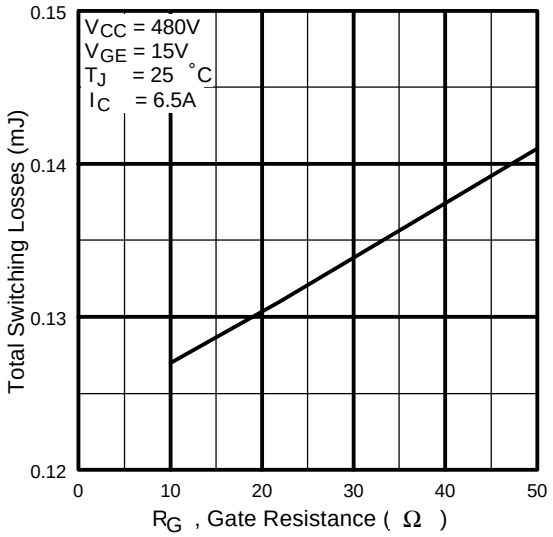


Fig. 9 - Typical Switching Losses vs. Gate Resistance

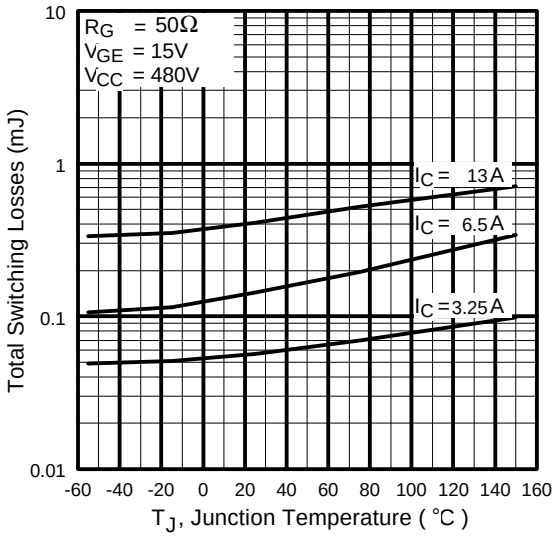


Fig. 10 - Typical Switching Losses vs. Junction Temperature

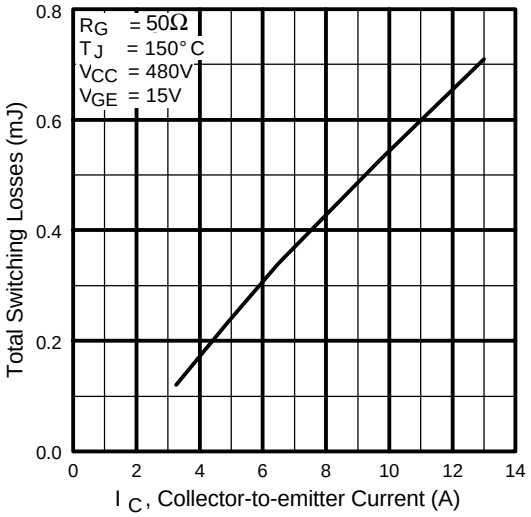


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

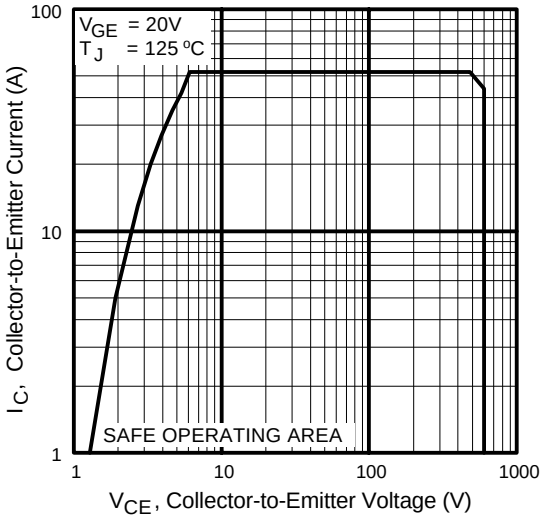


Fig. 12 - Turn-Off SOA

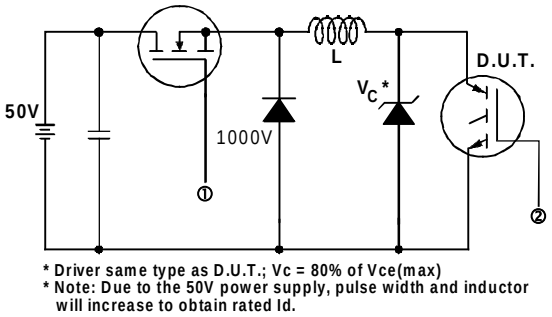


Fig. 13a - Clamped Inductive Load Test Circuit

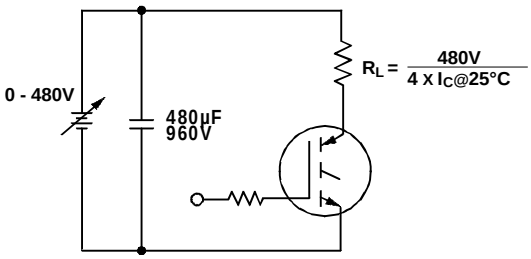


Fig. 13b - Pulsed Collector Current Test Circuit

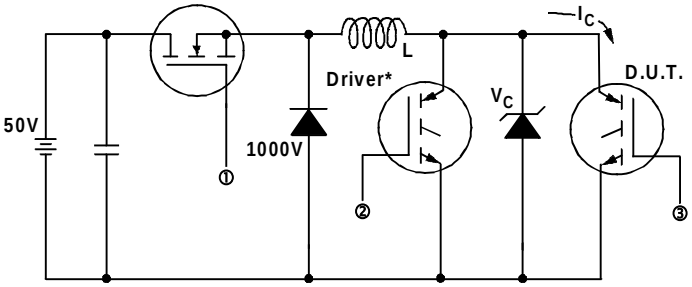


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

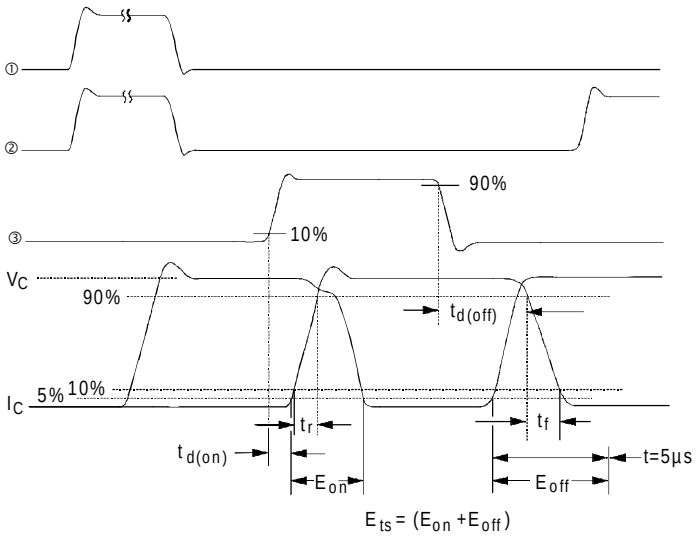
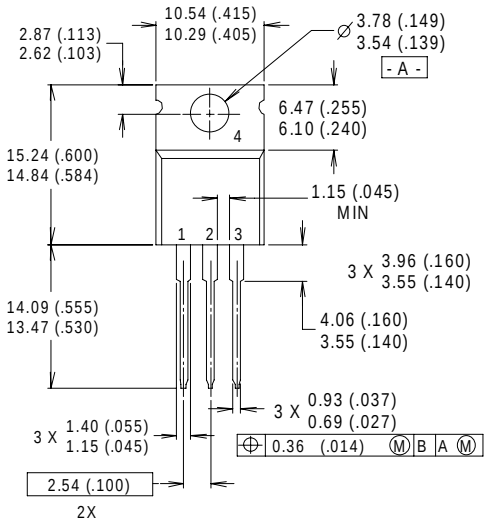
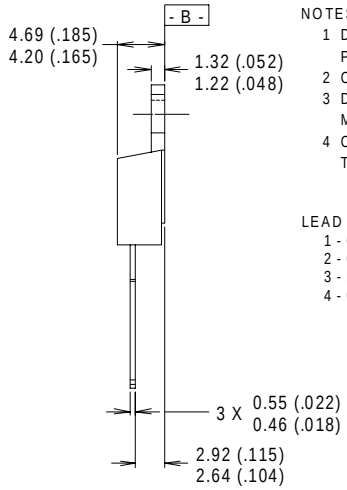


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-220AB





NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-220AB.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

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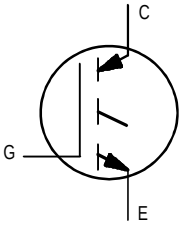
International
IOR Rectifier

IRG4IBC30W

INSULATED GATE BIPOLAR TRANSISTOR

Features

- Designed expressly for Switch-Mode Power Supply and PFC (power factor correction) applications
- 2.5kV, 60s insulation voltage ⑥
- Industry-benchmark switching losses improve efficiency of all power supply topologies
- 50% reduction of Eoff parameter
- Low IGBT conduction losses
- Latest-generation IGBT design and construction offers tighter parameters distribution, exceptional reliability
- Industry standard Isolated TO-220 Fullpak™ outline



n-channel

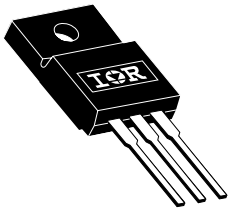
$V_{CES} = 600V$

$V_{CE(on)\ typ.} = 2.1V$

$@V_{GE} = 15V, I_C = 12\ A$

Benefits

- Lower switching losses allow more cost-effective operation than power MOSFETs up to 150 kHz ("hard switched" mode)
- Of particular benefit to single-ended converters and boost PFC topologies 150W and higher
- Low conduction losses and minimal minority-carrier recombination make these an excellent option for resonant mode switching as well (up to >>300 kHz)



TO-220 FULLPAK

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	17	A
I_C @ T_C = 100°C	Continuous Collector Current	8.4	
I_{CM}	Pulsed Collector Current ①	92	
I_{LM}	Clamped Inductive Load Current ②	92	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	180	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	45	W
P_D @ T_C = 100°C	Maximum Power Dissipation	18	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	2.8	°C/W
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	65	
Wt	Weight	2.0 (0.07)	—	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.34	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.1	2.7	V	I_C = 12A V_{GE} = 15V
		—	2.45	—		I_C = 23A See Fig.2, 5
		—	1.95	—		I_C = 12A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	11	16	—	S	V_{CE} = 100 V, I_C = 12A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	51	76	nC	I_C = 12A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	7.6	11		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	18	27		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	
t_r	Rise Time	—	16	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	99	150		I_C = 12A, V_{CC} = 480V
t_f	Fall Time	—	67	100		V_{GE} = 15V, R_G = 23Ω
E_{on}	Turn-On Switching Loss	—	0.13	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.13	—		See Fig. 9, 10, 13, 14
E_{ts}	Total Switching Loss	—	0.26	0.35		
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	T_J = 150°C,
t_r	Rise Time	—	17	—		I_C = 12A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	150	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	150	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.55	—	mJ	See Fig. 11,13, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	980	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	71	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	18	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 23Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

⑥ t = 60s, f = 60Hz

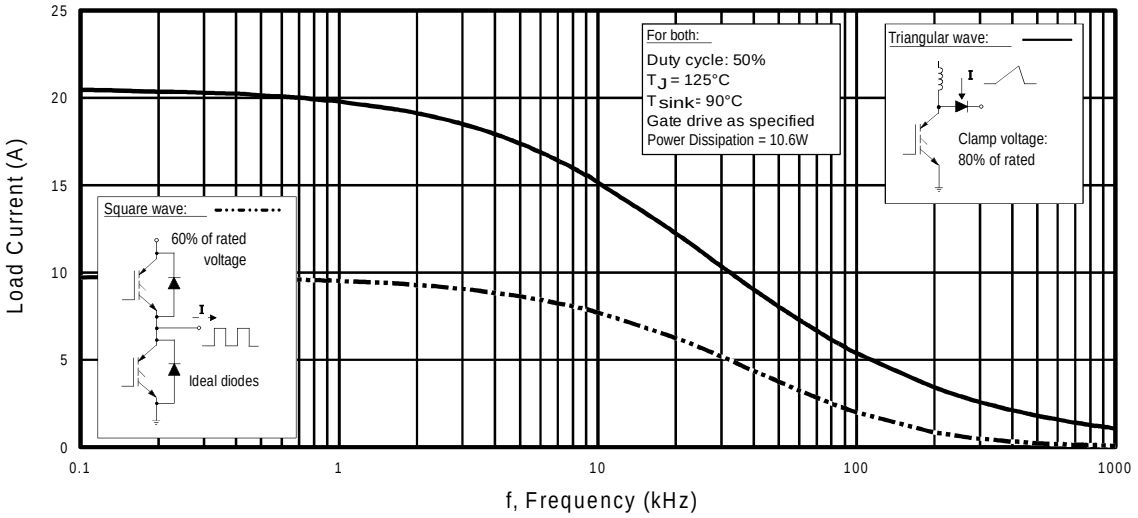


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

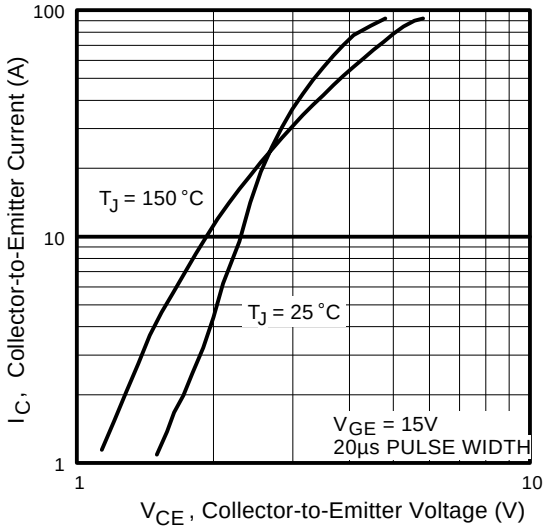


Fig. 2 - Typical Output Characteristics

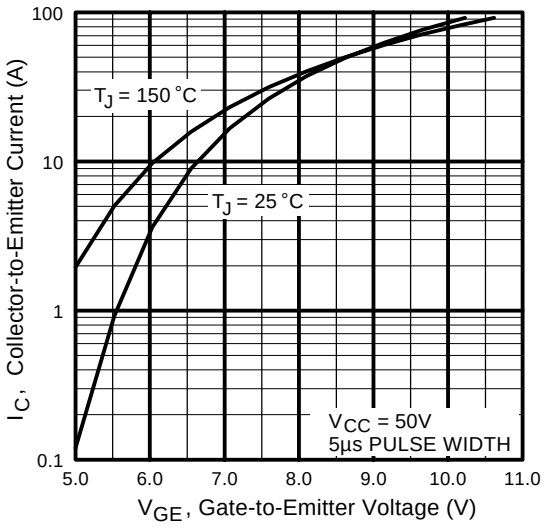


Fig. 3 - Typical Transfer Characteristics

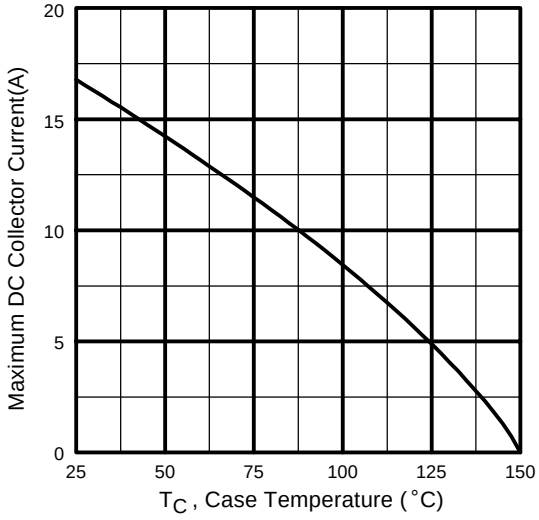


Fig. 4 - Maximum Collector Current vs. Case Temperature

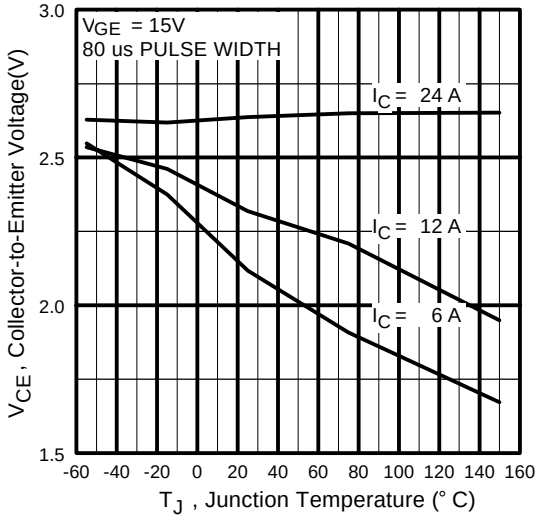


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

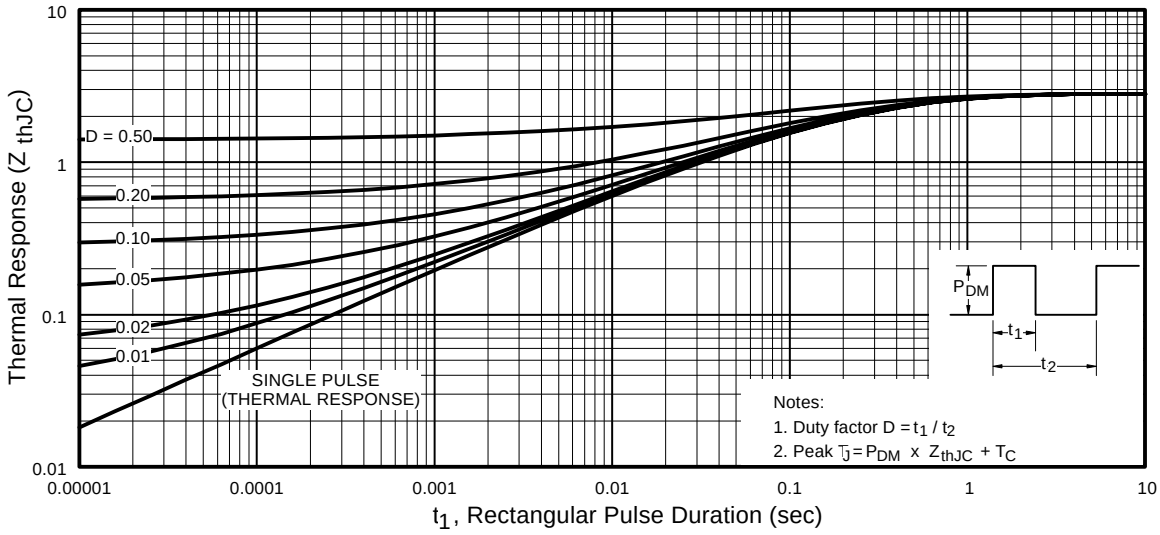


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

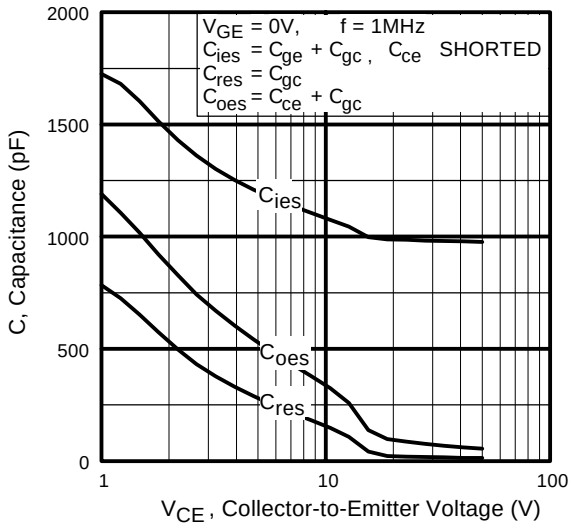


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

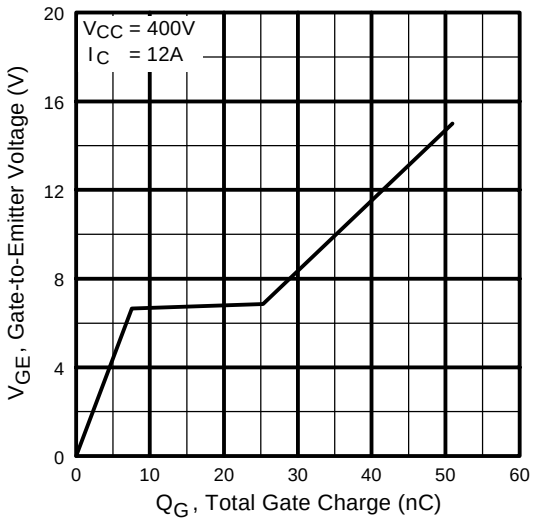


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

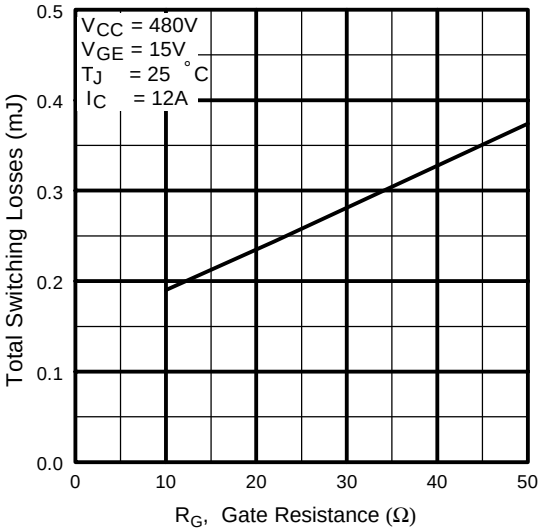


Fig. 9 - Typical Switching Losses vs. Gate Resistance

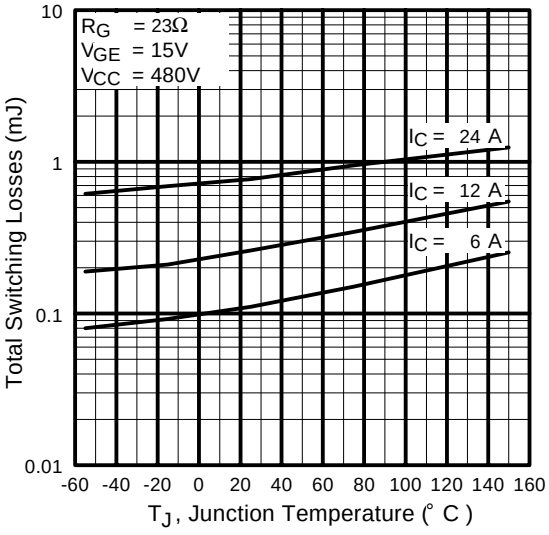


Fig. 10 - Typical Switching Losses vs. Junction Temperature

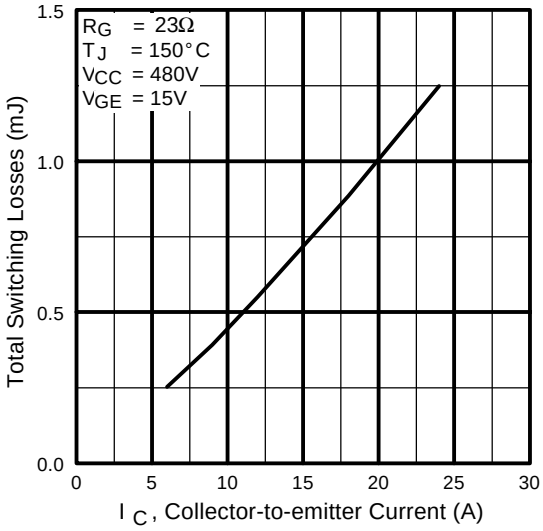


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

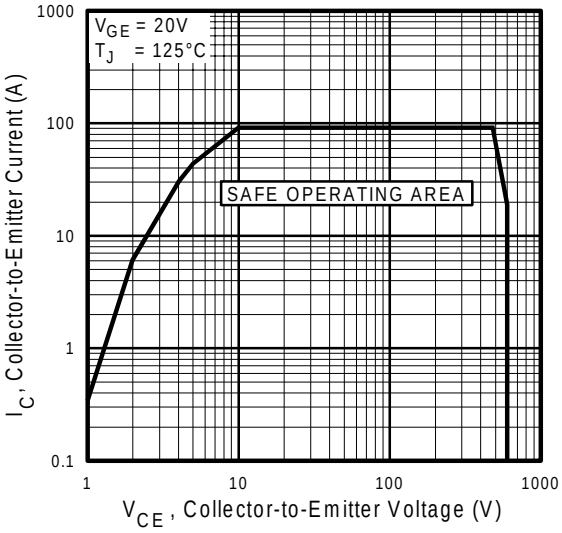


Fig. 12 - Turn-Off SOA

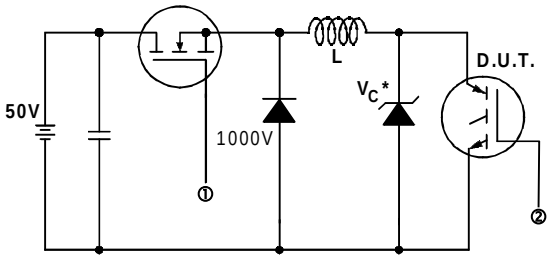


Fig. 13a - Clamped Inductive Load Test Circuit

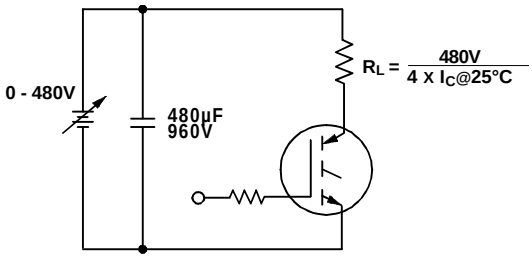


Fig. 13b - Pulsed Collector Current Test Circuit

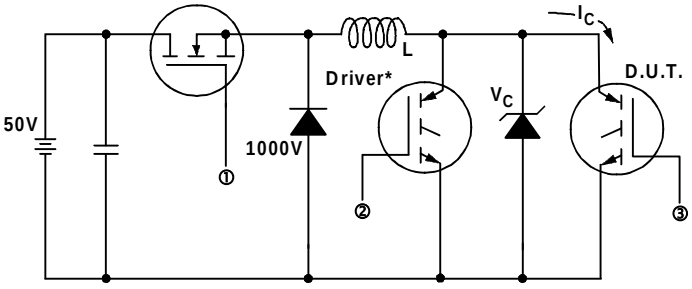


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

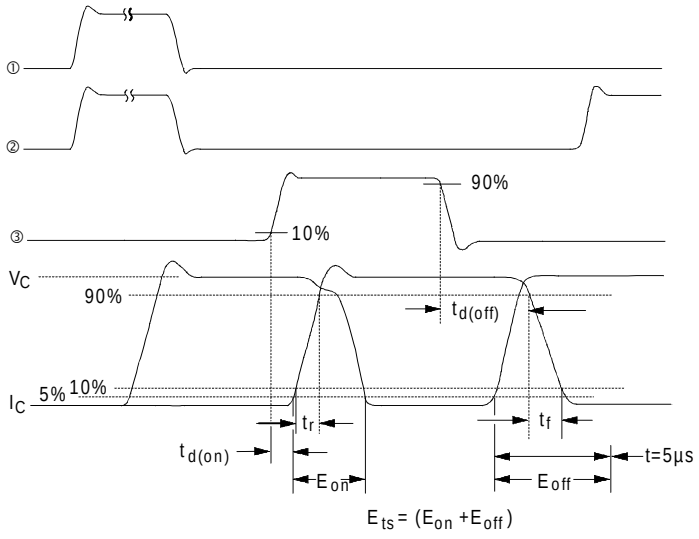
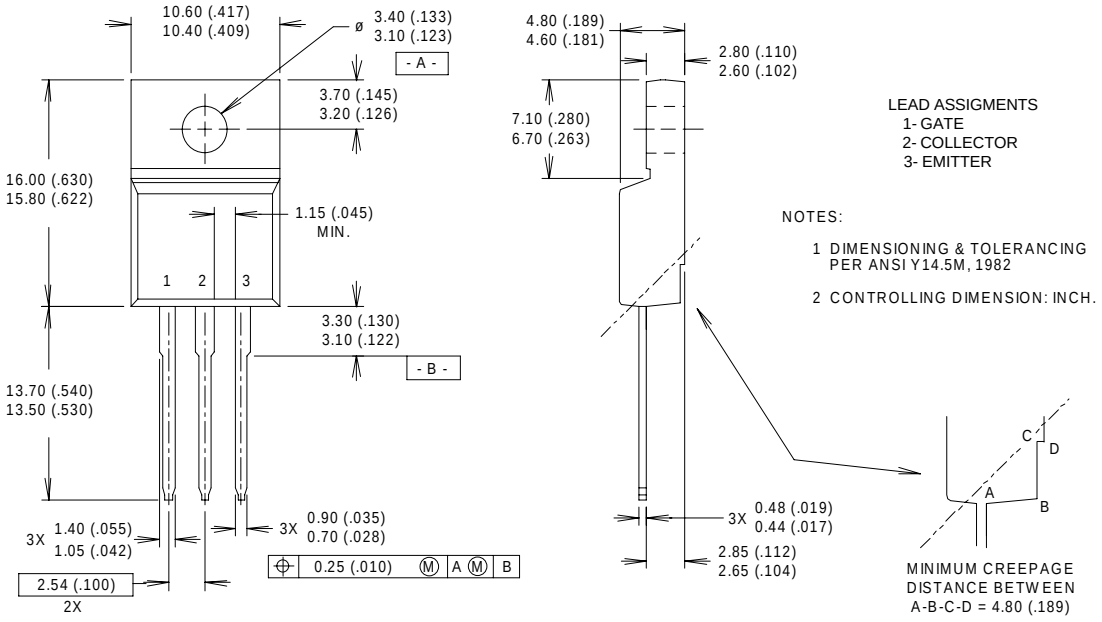


Fig. 14b - Switching Loss Waveforms

Case Outline — TO-220 FULLPAK



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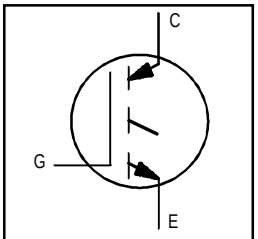
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IRG4BC30W

INSULATED GATE BIPOLAR TRANSISTOR

Features

- Designed expressly for Switch-Mode Power Supply and PFC (power factor correction) applications
- Industry-benchmark switching losses improve efficiency of all power supply topologies
- 50% reduction of Eoff parameter
- Low IGBT conduction losses
- Latest-generation IGBT design and construction offers tighter parameters distribution, exceptional reliability



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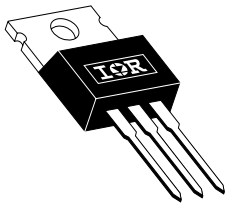
$V_{CES} = 600V$

$V_{CE(on)\ max.} = 2.70V$

$@V_{GE} = 15V, I_C = 12A$

Benefits

- Lower switching losses allow more cost-effective operation than power MOSFETs up to 150 kHz ("hard switched" mode)
- Of particular benefit to single-ended converters and boost PFC topologies 150W and higher
- Low conduction losses and minimal minority-carrier recombination make these an excellent option for resonant mode switching as well (up to >>300 kHz)



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	23	A
I_C @ T_C = 100°C	Continuous Collector Current	12	
I_{CM}	Pulsed Collector Current ①	92	
I_{LM}	Clamped Inductive Load Current ②	92	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	180	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	℃
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	80	
Wt	Weight	1.44	—	g

4/24/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.34	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.1	2.7	V	I_C = 12A V_{GE} = 15V
		—	2.45	—		I_C = 23A See Fig.2, 5
		—	1.95	—		I_C = 12A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	11	16	—	S	V_{CE} = 100 V, I_C = 12A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	51	76	nC	I_C = 12A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	7.6	11		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	18	27		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	T_J = 25°C
t_r	Rise Time	—	16	—		I_C = 12A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	99	150		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	67	100		Energy losses include "tail"
E_{on}	Turn-On Switching Loss	—	0.13	—	mJ	See Fig. 9, 10, 13, 14
E_{off}	Turn-Off Switching Loss	—	0.13	—		
E_{ts}	Total Switching Loss	—	0.26	0.35		
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	T_J = 150°C,
t_r	Rise Time	—	17	—		I_C = 12A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	150	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	150	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.55	—	mJ	See Fig. 11,13, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	980	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	71	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	18	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 23Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

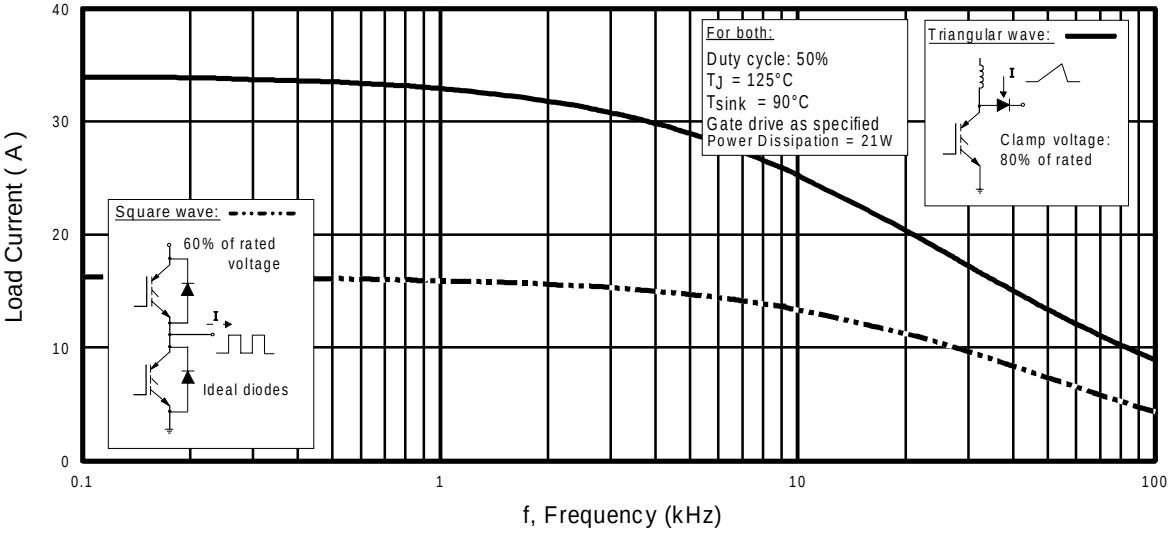


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

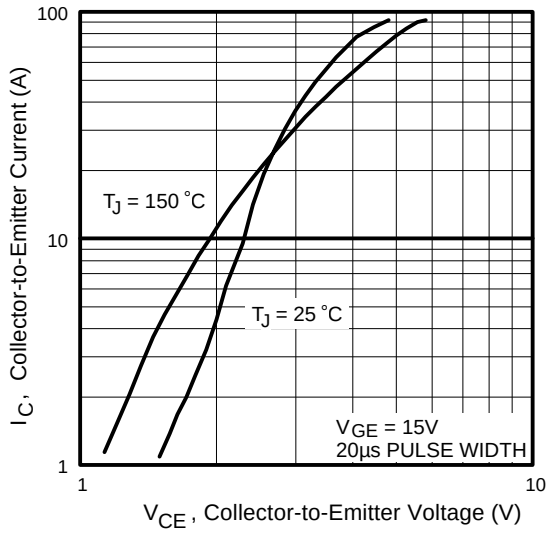


Fig. 2 - Typical Output Characteristics

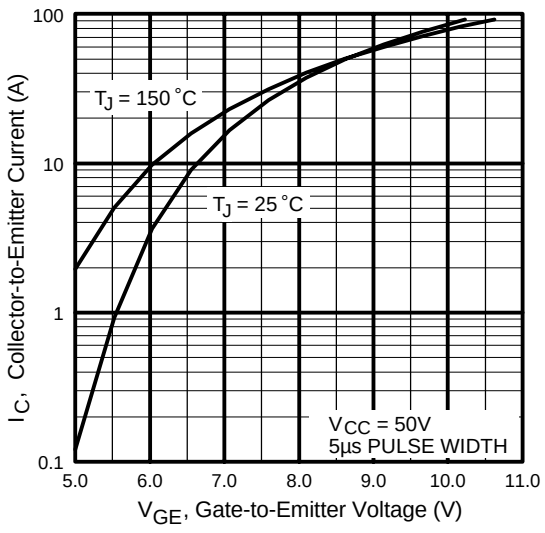


Fig. 3 - Typical Transfer Characteristics

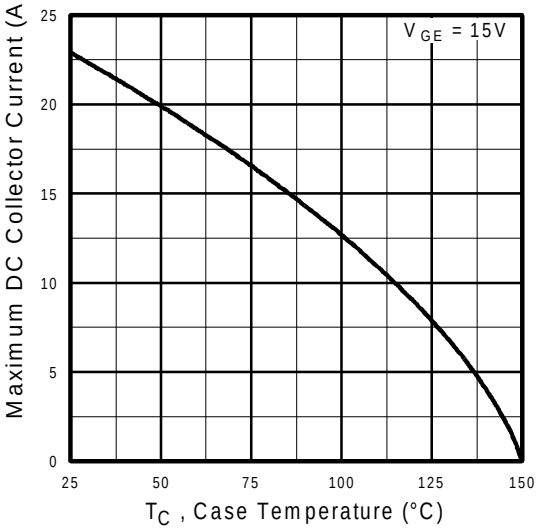


Fig. 4 - Maximum Collector Current vs. Case Temperature

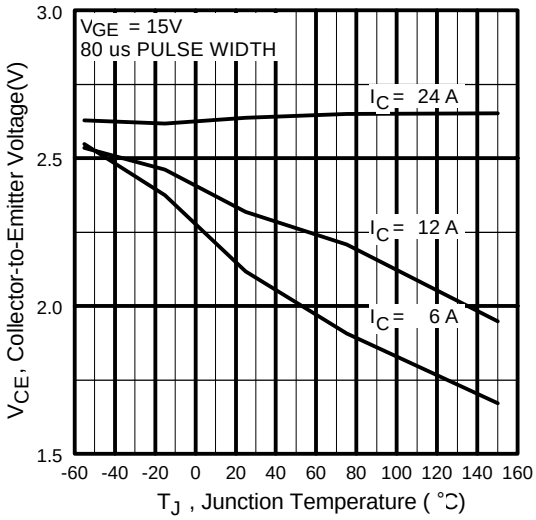


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

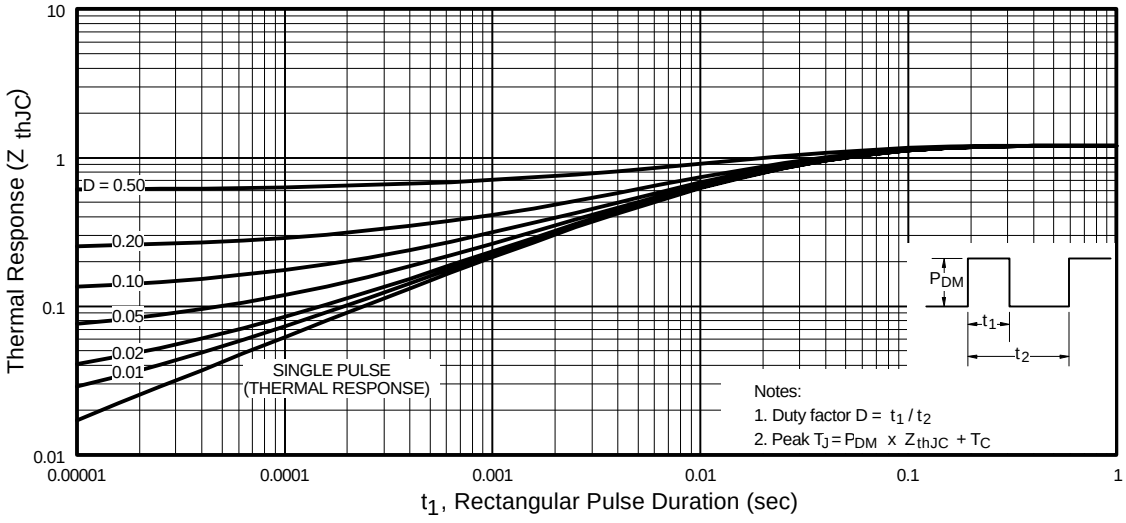


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

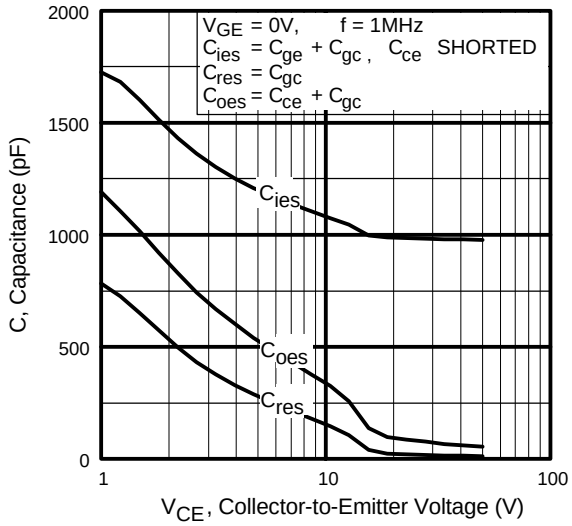


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

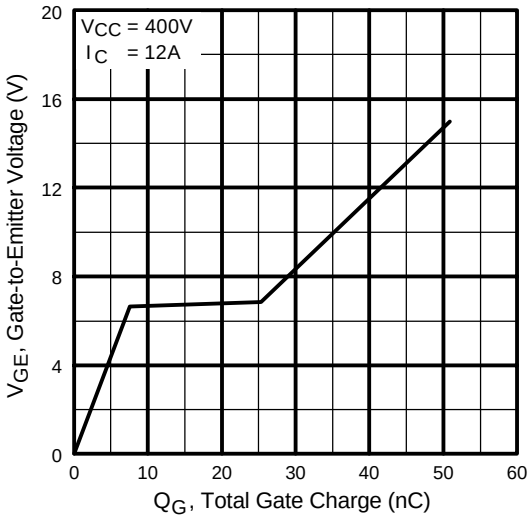


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

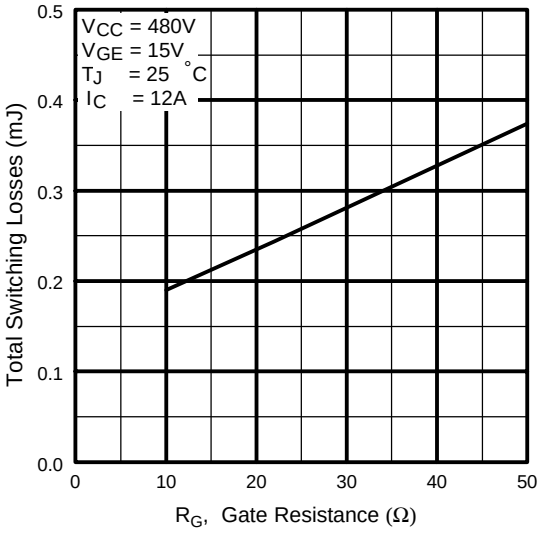


Fig. 9 - Typical Switching Losses vs. Gate Resistance

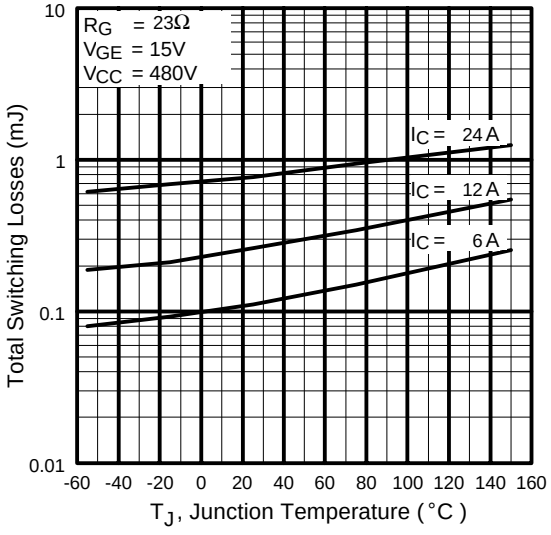


Fig. 10 - Typical Switching Losses vs. Junction Temperature

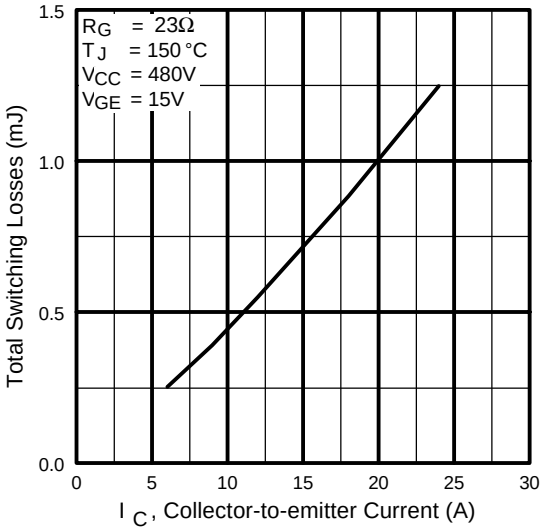


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

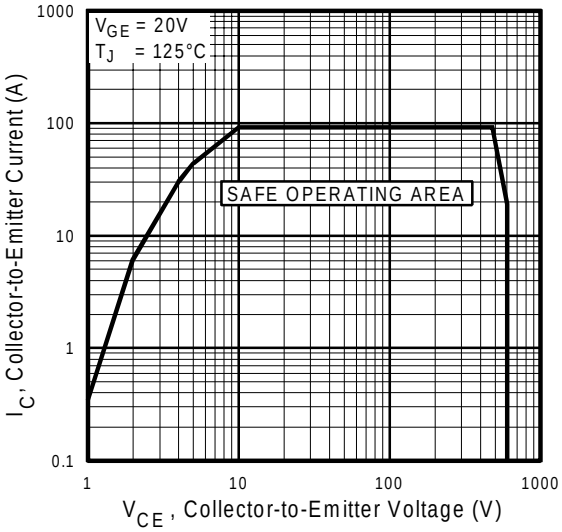


Fig. 12 - Turn-Off SOA

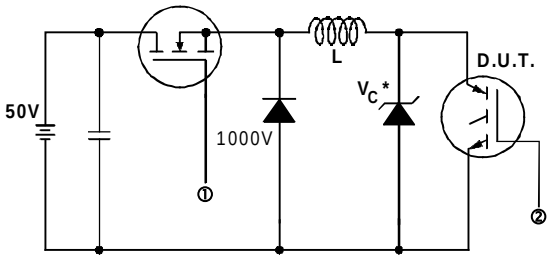


Fig. 13a - Clamped Inductive Load Test Circuit

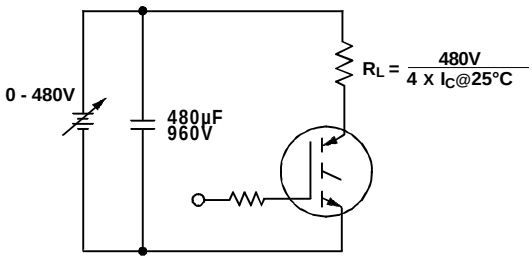


Fig. 13b - Pulsed Collector Current Test Circuit

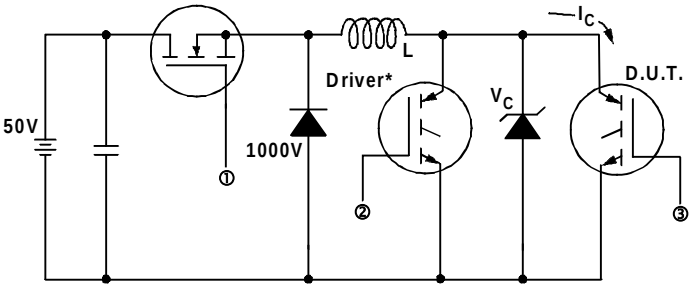


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

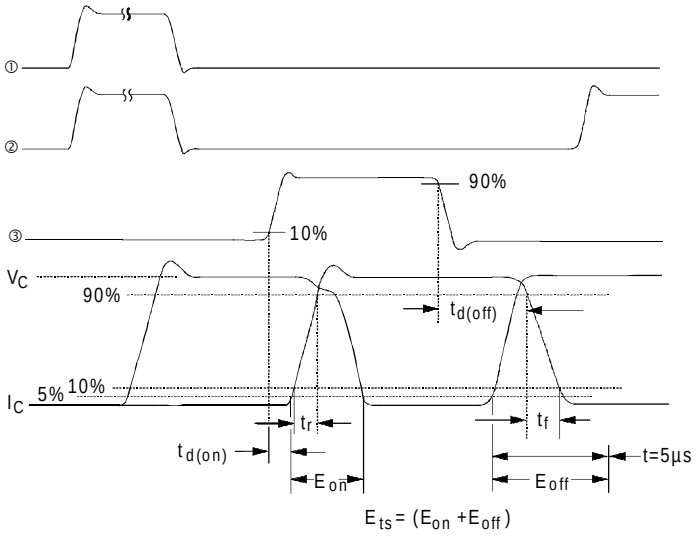
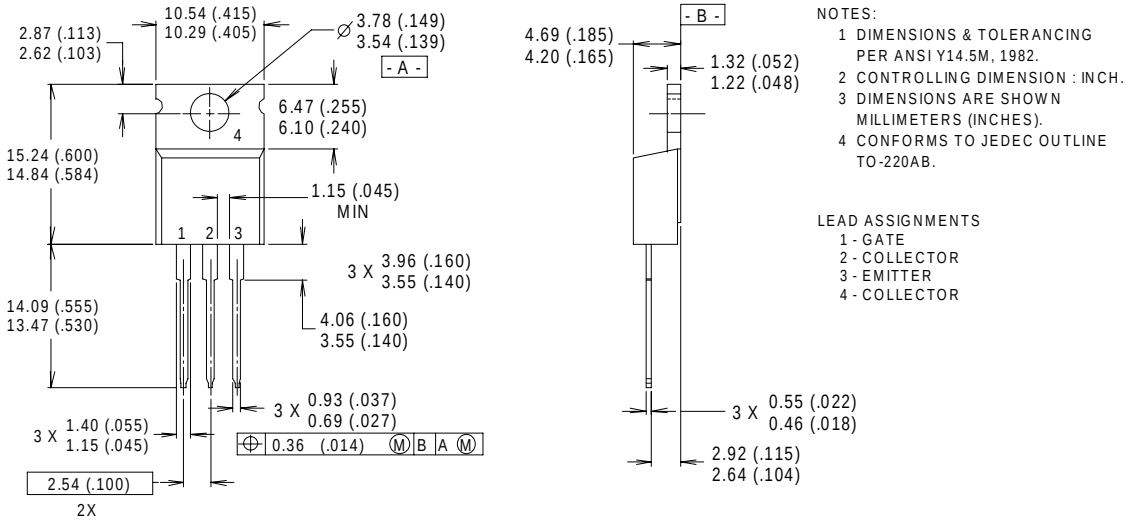


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-220AB



CONFORMS TO JEDEC OUTLINE TO-220AB
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

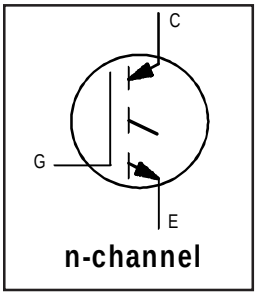
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 10/00

PD - 91790

International
IOR Rectifier

IRG4BC30W-S

INSULATED GATE BIPOLAR TRANSISTOR



n-channel

V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.10V

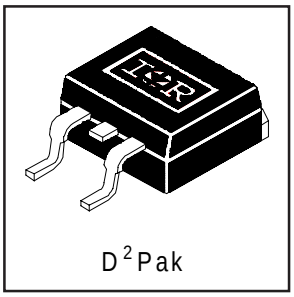
@V_{GE} = 15V, I_C = 12A

Features

- Designed expressly for Switch-Mode Power Supply and PFC (power factor correction) applications
- Industry-benchmark switching losses improve efficiency of all power supply topologies
- 50% reduction of Eoff parameter
- Low IGBT conduction losses
- Latest-generation IGBT design and construction offers tighter parameters distribution, exceptional reliability

Benefits

- Lower switching losses allow more cost-effective operation than power MOSFETs up to 150 kHz ("hard switched" mode)
- Of particular benefit to single-ended converters and boost PFC topologies 150W and higher
- Low conduction losses and minimal minority-carrier recombination make these an excellent option for resonant mode switching as well (up to >>300 kHz)



D^2Pak

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	23	A
I_C @ T_C = 100°C	Continuous Collector Current	12	
I_{CM}	Pulsed Collector Current ①	92	
I_{LM}	Clamped Inductive Load Current ②	92	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	180	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient, (PCB Mounted,steady-state)*	—	40	

* When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

8/13/98

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.34	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.1	2.7	V	I_C = 12A V_{GE} = 15V
		—	2.45	—		I_C = 23A See Fig.2, 5
		—	1.95	—		I_C = 12A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	11	16	—	S	V_{CE} = 100 V, I_C = 12A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	1000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	51	76	nC	I_C = 12A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	7.6	11		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	18	27		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	T_J = 25°C
t_r	Rise Time	—	16	—		I_C = 12A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	99	150		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	67	100		Energy losses include "tail"
E_{on}	Turn-On Switching Loss	—	0.13	—	mJ	See Fig. 9, 10, 13, 14
E_{off}	Turn-Off Switching Loss	—	0.13	—		
E_{ts}	Total Switching Loss	—	0.26	0.35		
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	T_J = 150°C,
t_r	Rise Time	—	17	—		I_C = 12A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	150	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	150	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.55	—	mJ	See Fig. 11,13, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	980	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	71	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	18	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 23Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

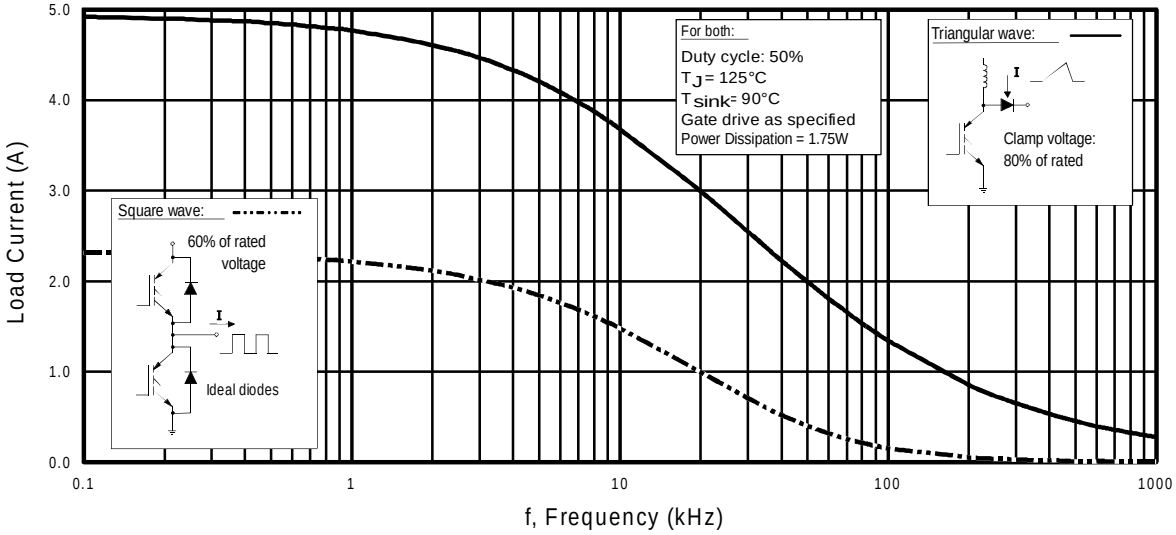


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

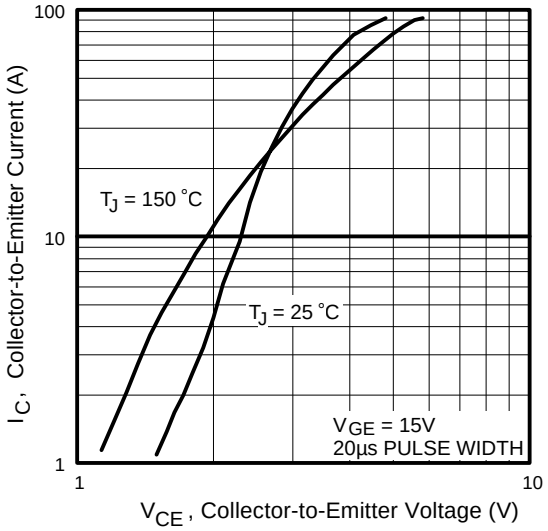


Fig. 2 - Typical Output Characteristics

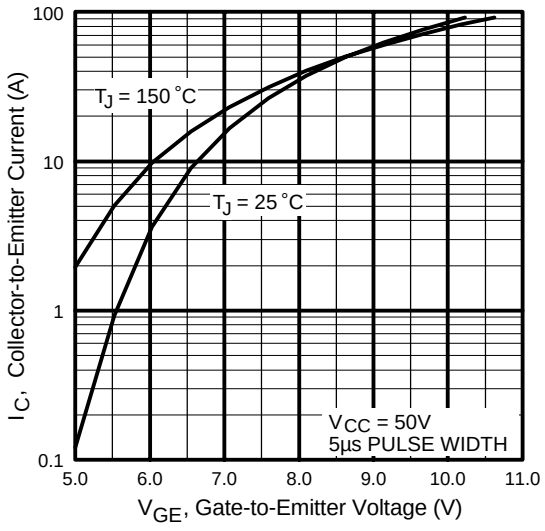


Fig. 3 - Typical Transfer Characteristics

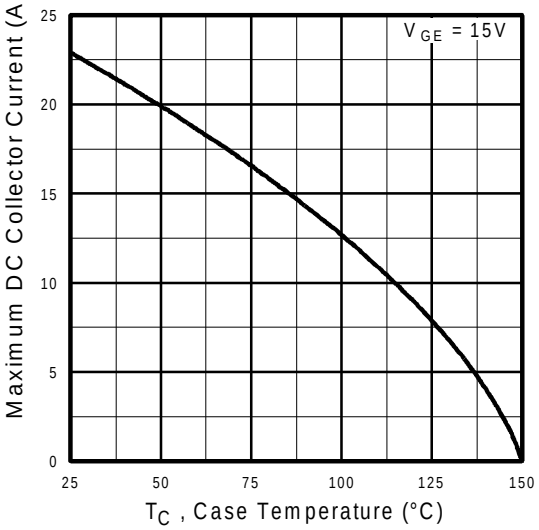


Fig. 4 - Maximum Collector Current vs. Case Temperature

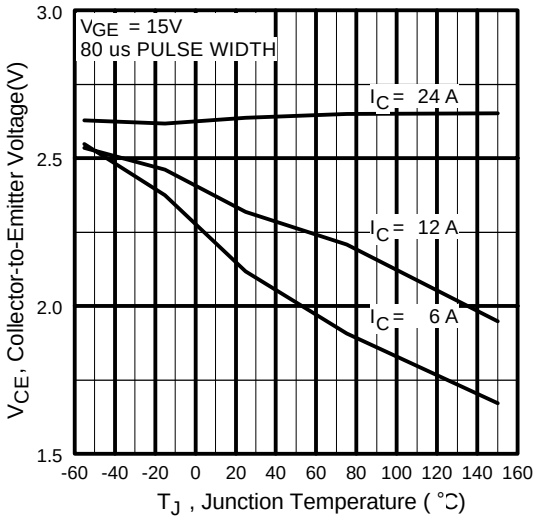


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

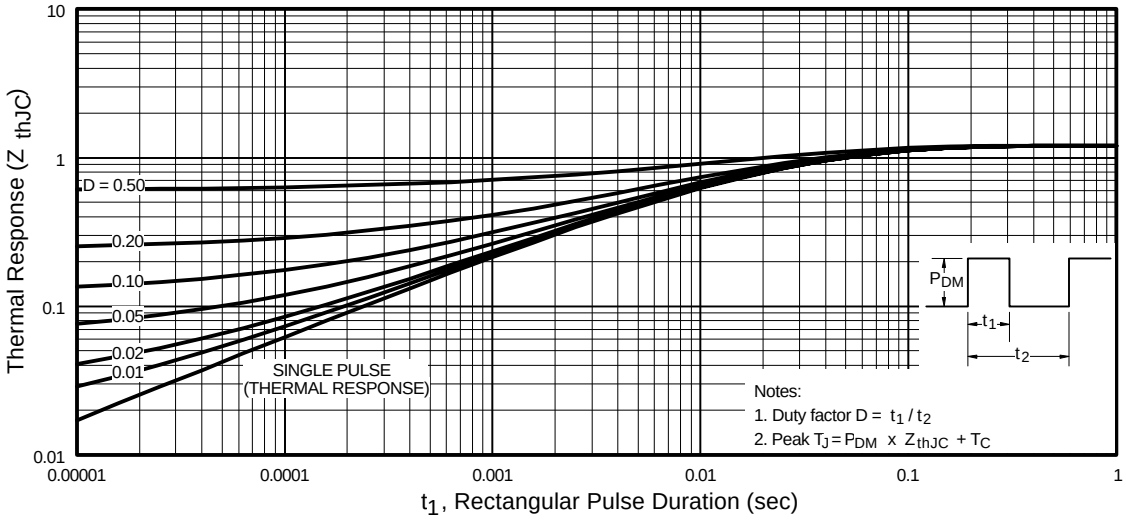


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

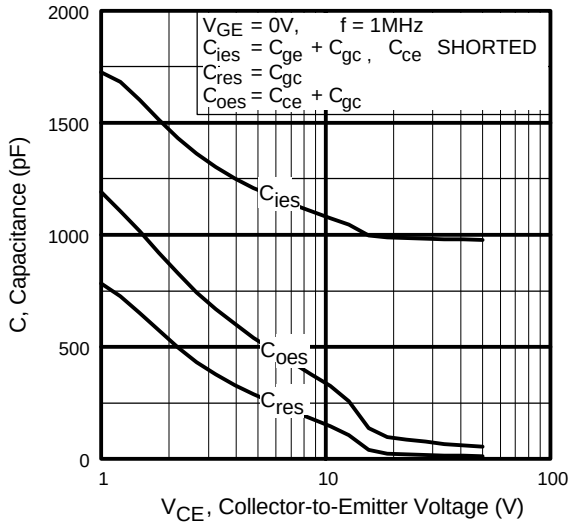


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

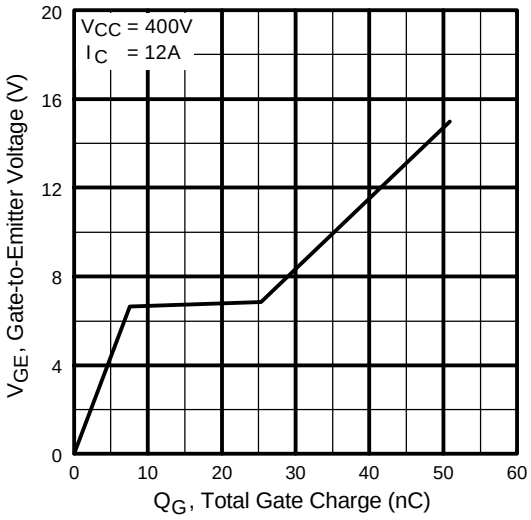


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

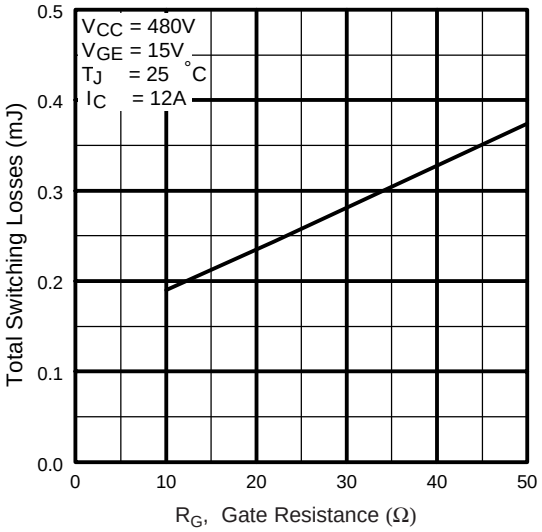


Fig. 9 - Typical Switching Losses vs. Gate Resistance

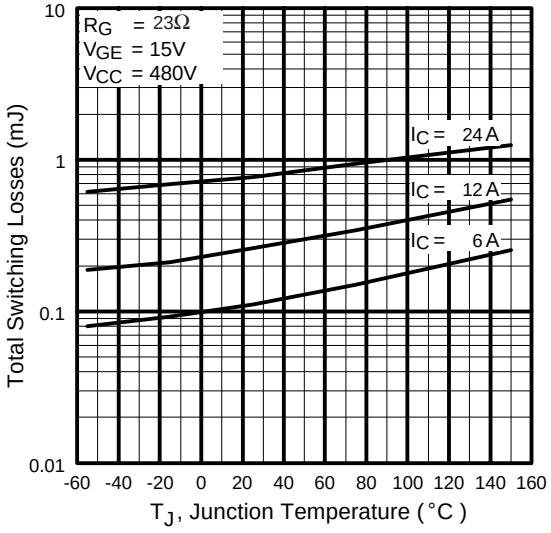


Fig. 10 - Typical Switching Losses vs. Junction Temperature

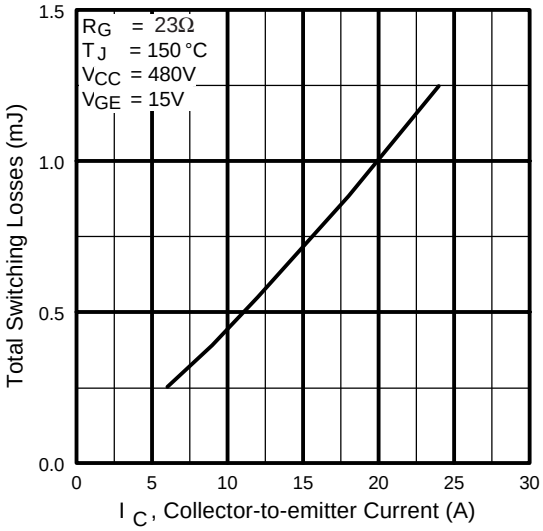


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

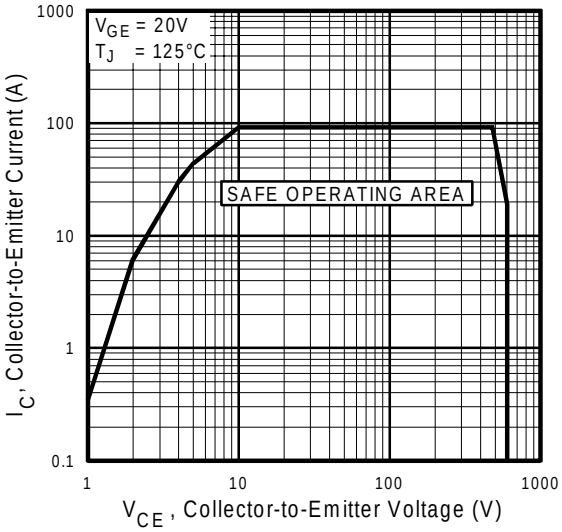


Fig. 12 - Turn-Off SOA

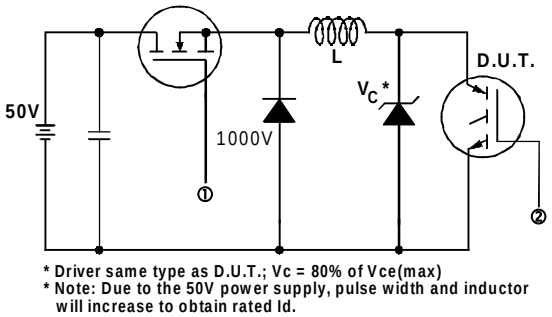


Fig. 13a - Clamped Inductive Load Test Circuit

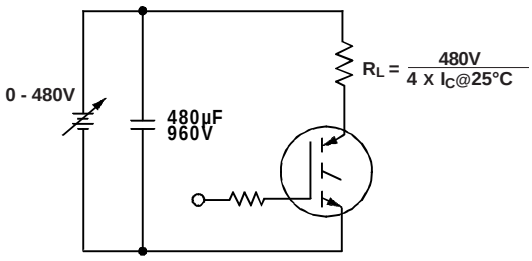


Fig. 13b - Pulsed Collector Current Test Circuit

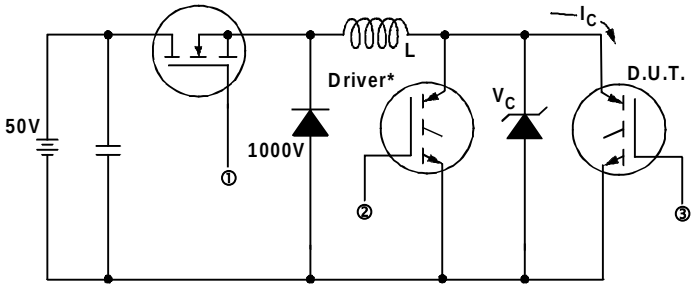


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

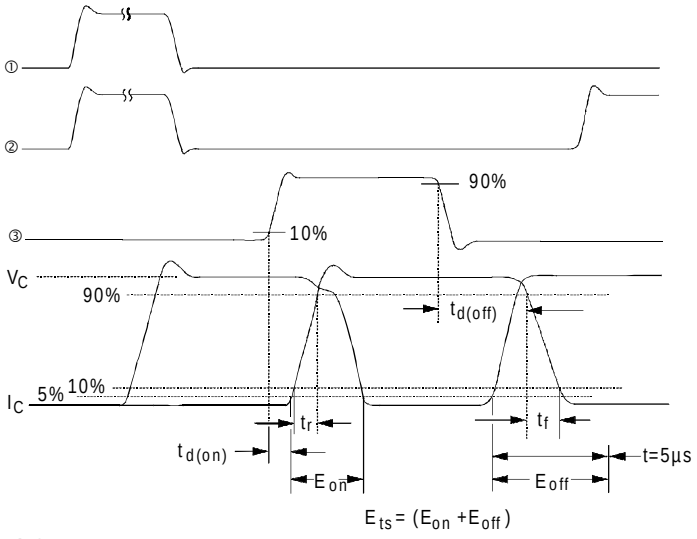
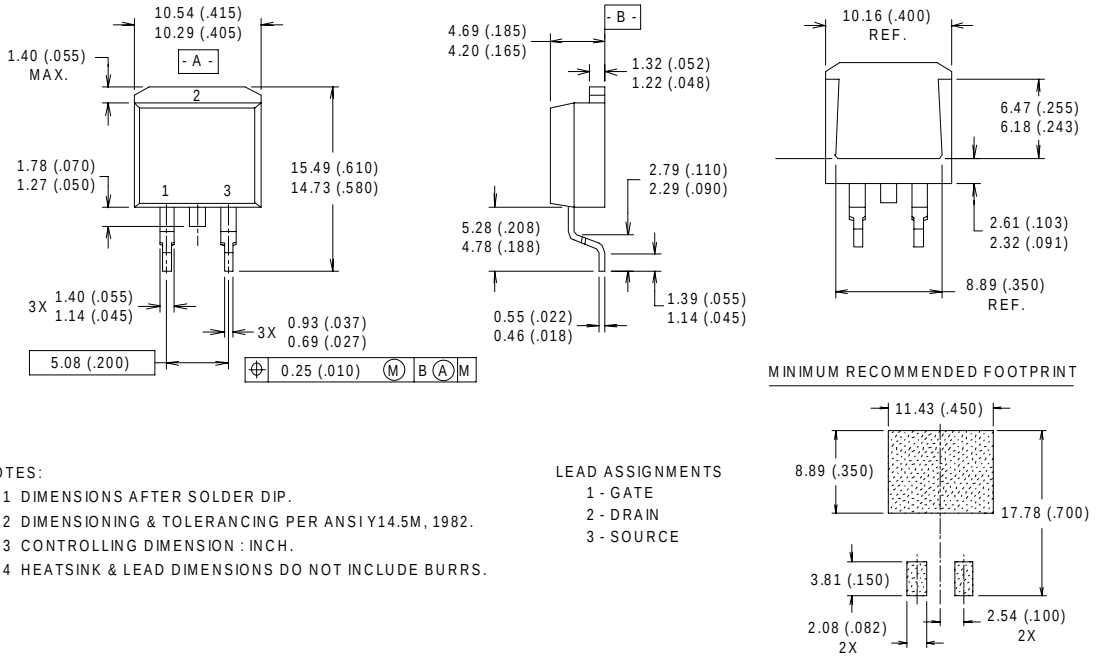


Fig. 14b - Switching Loss Waveforms

D^{2}Pak Package Outline



NOTES:

1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

1 - GATE
2 - DRAIN
3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371
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International
IOR Rectifier

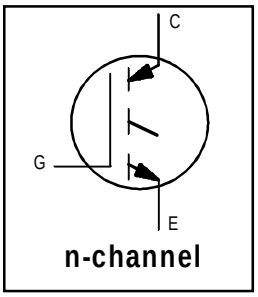
PD - 91654A

IRG4BC40W

INSULATED GATE BIPOLAR TRANSISTOR

Features

- Designed expressly for Switch-Mode Power Supply and PFC (power factor correction) applications
- Industry-benchmark switching losses improve efficiency of all power supply topologies
- 50% reduction of Eoff parameter
- Low IGBT conduction losses
- Latest-generation IGBT design and construction offers tighter parameters distribution, exceptional reliability



n-channel

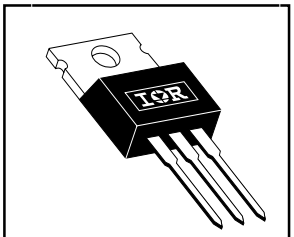
V_{CES} = 600V

$V_{CE(on)\ typ.}$ = 2.05V

@V_{GE} = 15V, I_C = 20A

Benefits

- Lower switching losses allow more cost-effective operation than power MOSFETs up to 150 kHz ("hard switched" mode)
- Of particular benefit to single-ended converters and boost PFC topologies 150W and higher
- Low conduction losses and minimal minority-carrier recombination make these an excellent option for resonant mode switching as well (up to >>300 kHz)



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	40	A
I_C @ T_C = 100°C	Continuous Collector Current	20	
I_{CM}	Pulsed Collector Current ①	160	
I_{LM}	Clamped Inductive Load Current ②	160	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	160	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.77	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	80	
Wt	Weight	2.0 (0.07)	—	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.44	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.05	2.5	V	I_C = 20A V_{GE} = 15V
		—	2.36	—		I_C = 40A See Fig.2, 5
		—	1.90	—		I_C = 20A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	13	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	18	28	—	S	V_{CE} = 100 V, I_C =20A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	2500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	98	147	nC	I_C =20A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	12	18		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	36	54		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	27	—	ns	
t_r	Rise Time	—	22	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	100	150		I_C = 20A, V_{CC} = 480V
t_f	Fall Time	—	74	110		V_{GE} = 15V, R_G = 10Ω
E_{on}	Turn-On Switching Loss	—	0.11	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.23	—		See Fig. 9,10, 14
E_{ts}	Total Switching Loss	—	0.34	0.45		
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	T_J = 150°C,
t_r	Rise Time	—	23	—		I_C = 20A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	170	—		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	—	124	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.85	—	mJ	See Fig. 10,11, 14
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1900	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	140	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	35	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 10Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

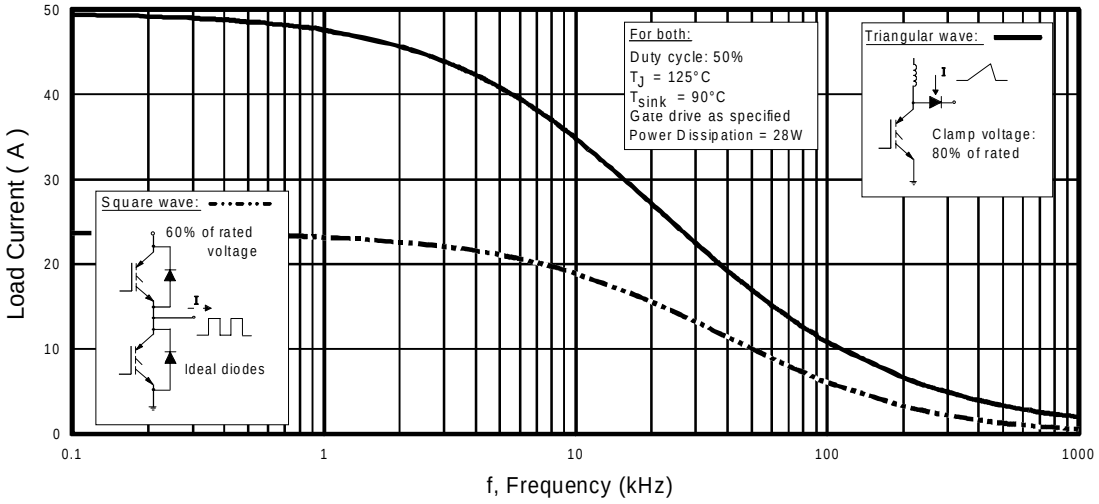


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

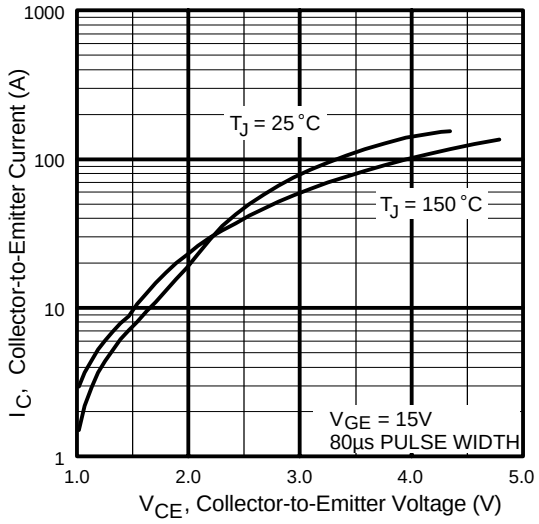


Fig. 2 - Typical Output Characteristics

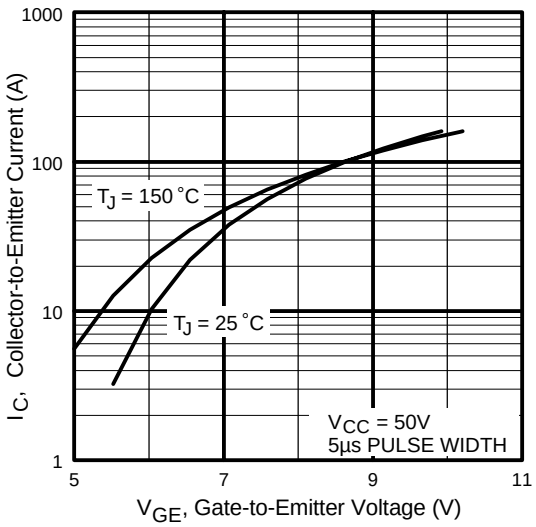


Fig. 3 - Typical Transfer Characteristics

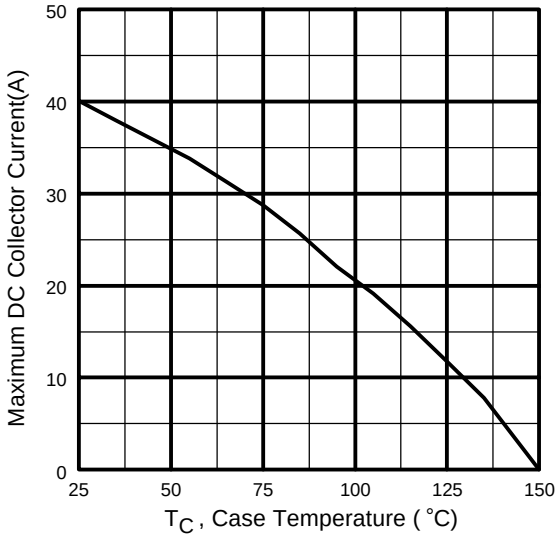


Fig. 4 - Maximum Collector Current vs. Case Temperature

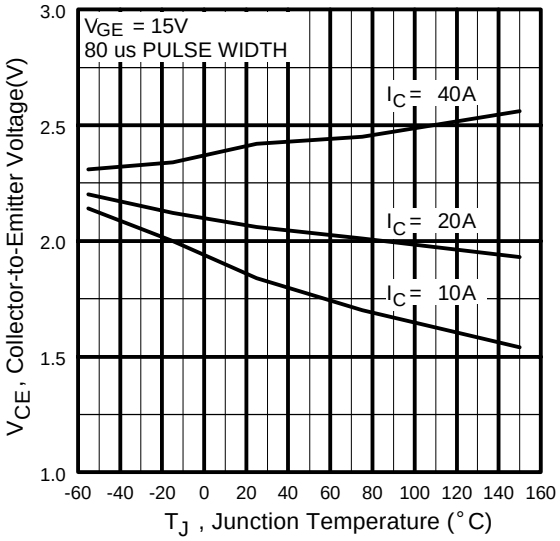


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

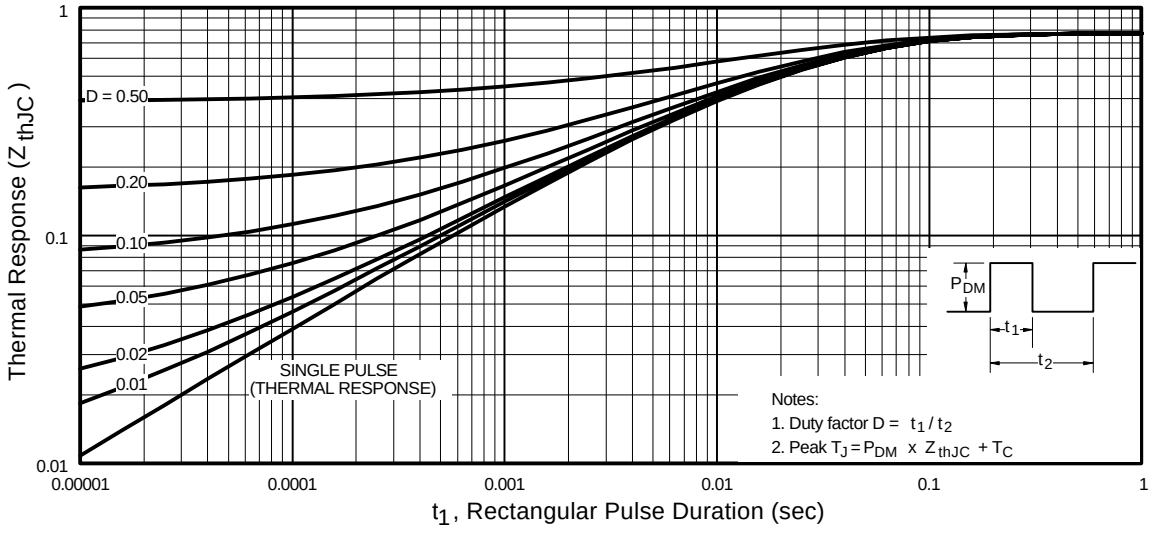


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

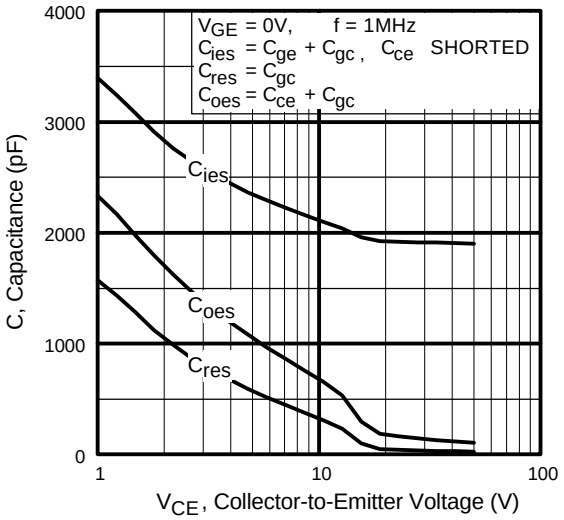


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

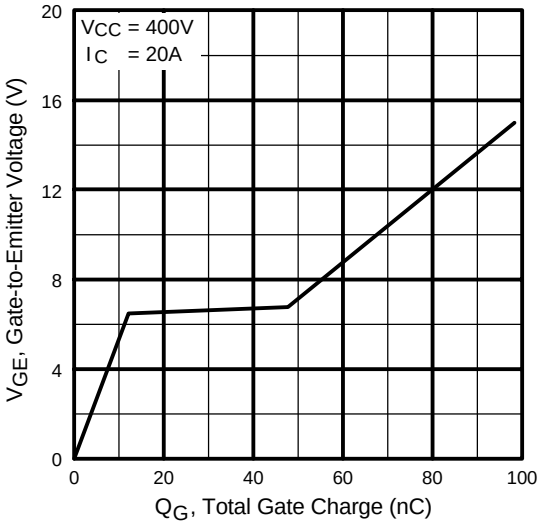


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

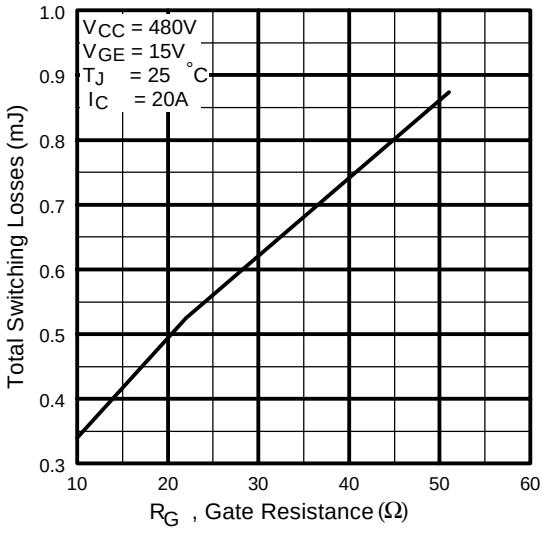


Fig. 9 - Typical Switching Losses vs. Gate Resistance

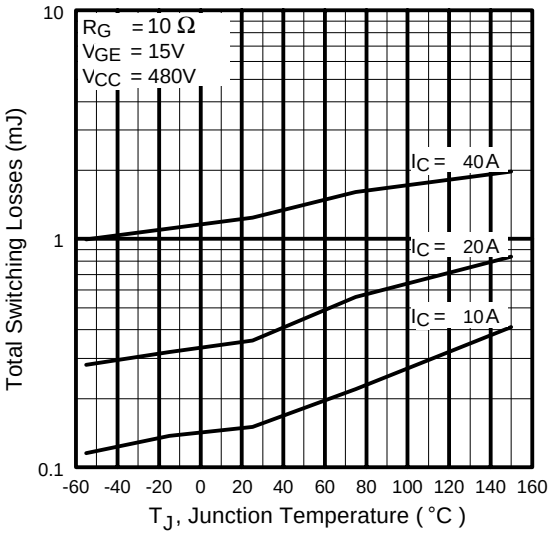


Fig. 10 - Typical Switching Losses vs. Junction Temperature

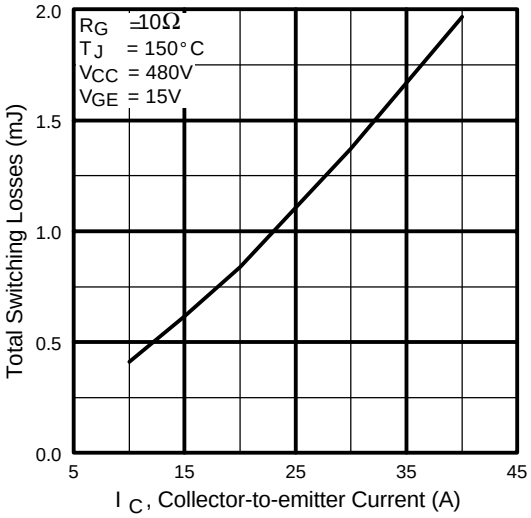


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

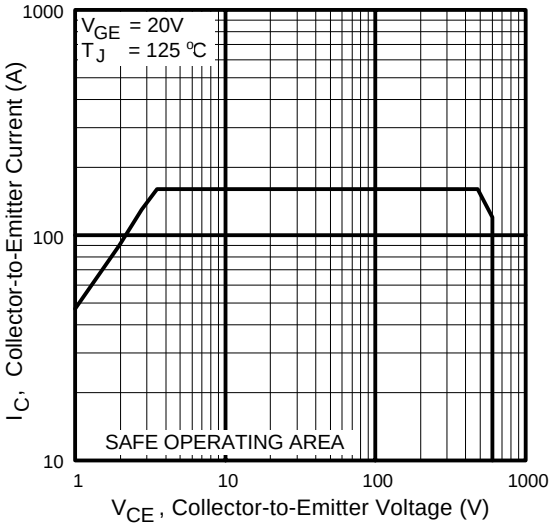


Fig. 12 - Turn-Off SOA

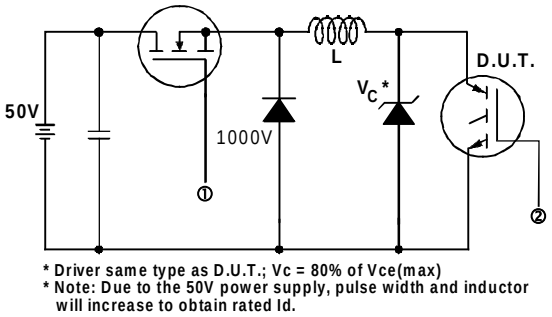


Fig. 13a - Clamped Inductive Load Test Circuit

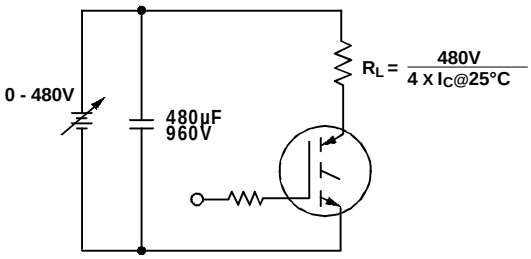


Fig. 13b - Pulsed Collector Current Test Circuit

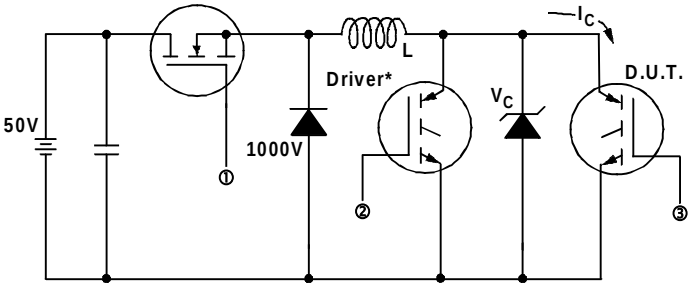


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

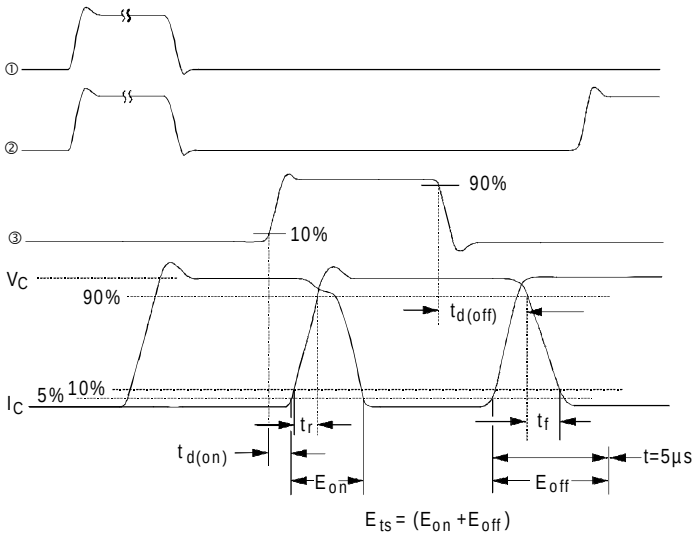
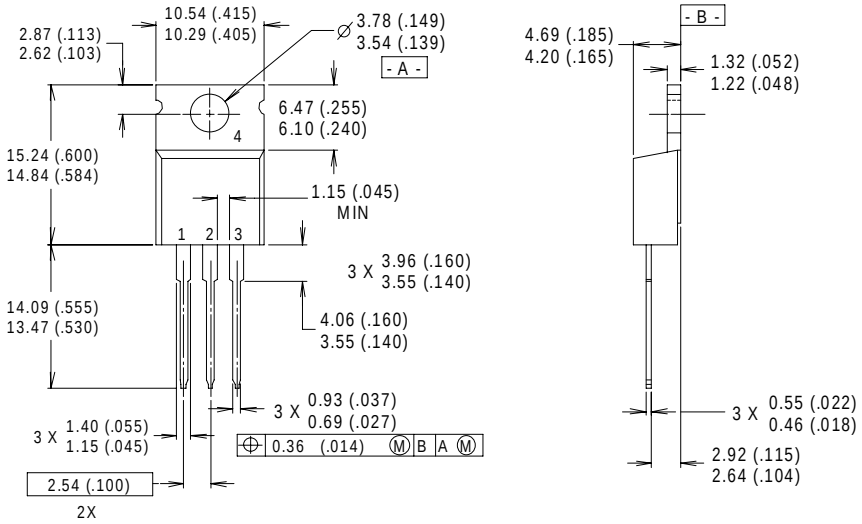


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-220AB



International
IOR Rectifier

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IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 10/00

PD -91656C

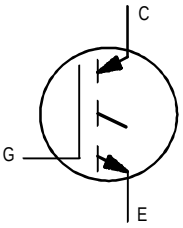
International
IOR Rectifier

IRG4PC40W

INSULATED GATE BIPOLAR TRANSISTOR

Features

- Designed expressly for Switch-Mode Power Supply and PFC (power factor correction) applications
- Industry-benchmark switching losses improve efficiency of all power supply topologies
- 50% reduction of Eoff parameter
- Low IGBT conduction losses
- Latest-generation IGBT design and construction offers tighter parameters distribution, exceptional reliability



n-channel

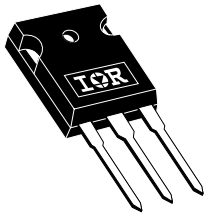
$V_{CES} = 600V$

$V_{CE(on)\ typ.} = 2.05V$

$@V_{GE} = 15V, I_C = 20A$

Benefits

- Lower switching losses allow more cost-effective operation than power MOSFETs up to 150 kHz ("hard switched" mode)
- Of particular benefit to single-ended converters and boost PFC topologies 150W and higher
- Low conduction losses and minimal minority-carrier recombination make these an excellent option for resonant mode switching as well (up to >>300 kHz)



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	40	A
I_C @ T_C = 100°C	Continuous Collector Current	20	
I_{CM}	Pulsed Collector Current ①	160	
I_{LM}	Clamped Inductive Load Current ②	160	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	160	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	℃
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.77	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

4/15/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.44	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.05	2.5	V	I_C = 20A V_{GE} = 15V
		—	2.36	—		I_C = 40A See Fig.2, 5
		—	1.90	—		I_C = 20A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	13	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	18	28	—	S	V_{CE} = 100 V, I_C =20A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	2500		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	98	147	nC	I_C = 20A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	12	18		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	36	54		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	27	—	ns	
t_r	Rise Time	—	22	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	100	150		I_C = 20A, V_{CC} = 480V
t_f	Fall Time	—	74	110		V_{GE} = 15V, R_G = 10Ω
E_{on}	Turn-On Switching Loss	—	0.11	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.23	—		See Fig. 9,10, 14
E_{ts}	Total Switching Loss	—	0.34	0.45		
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	T_J = 150°C,
t_r	Rise Time	—	23	—		I_C = 20A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	170	—		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	—	124	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	0.85	—	mJ	See Fig.10,11, 14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1900	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	140	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	35	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 10Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

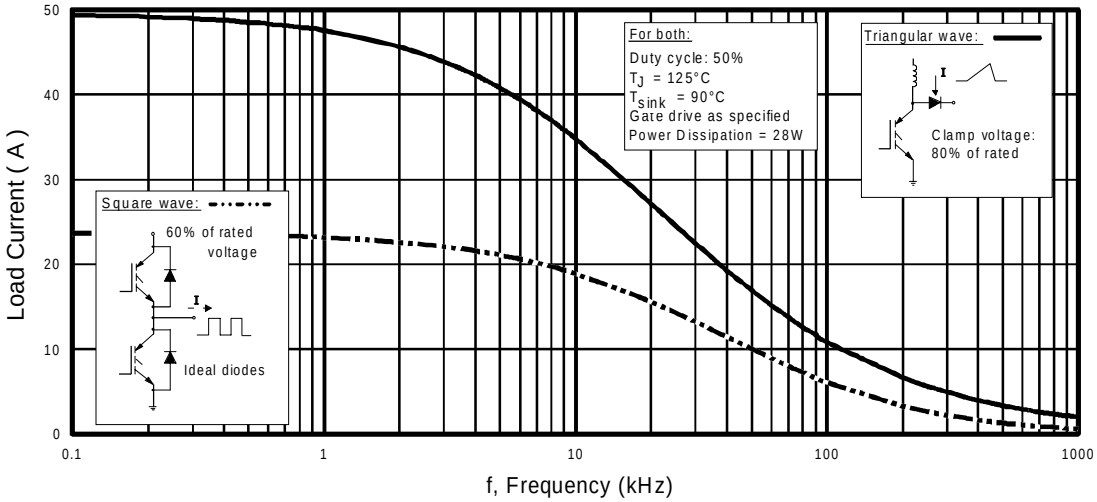


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

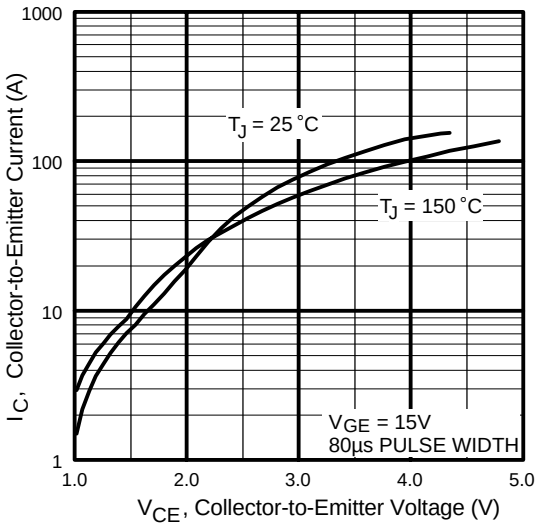


Fig. 2 - Typical Output Characteristics

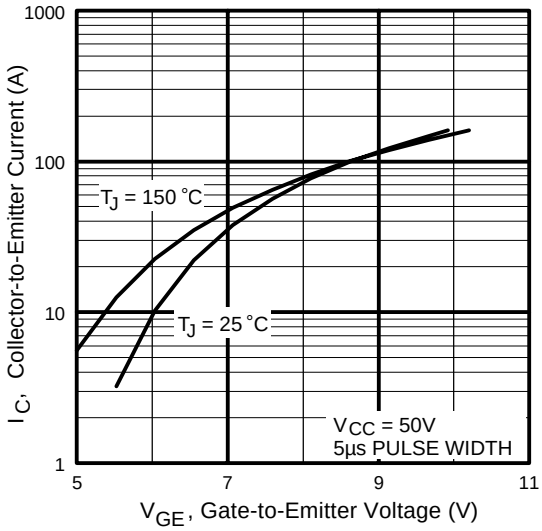


Fig. 3 - Typical Transfer Characteristics

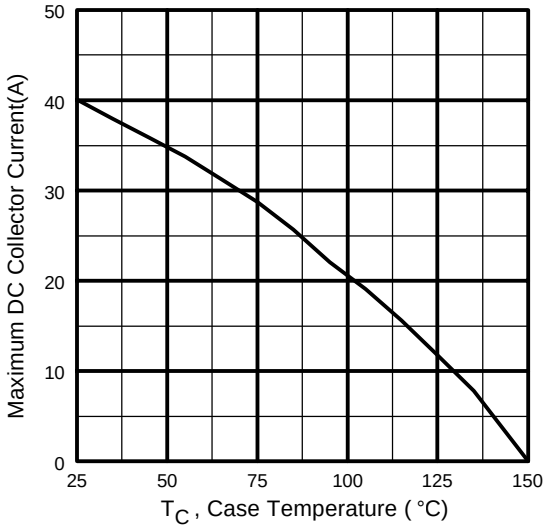


Fig. 4 - Maximum Collector Current vs. Case Temperature

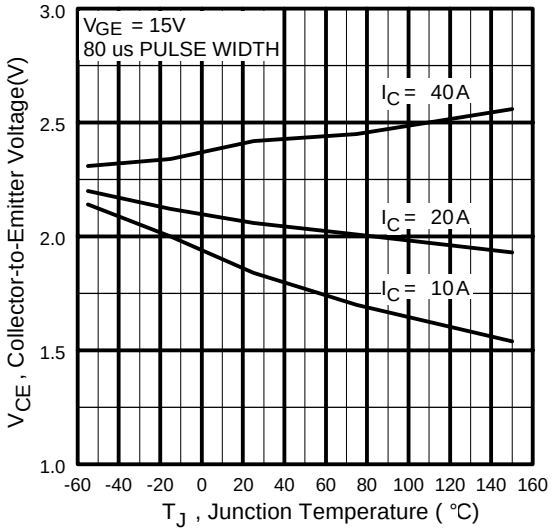


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

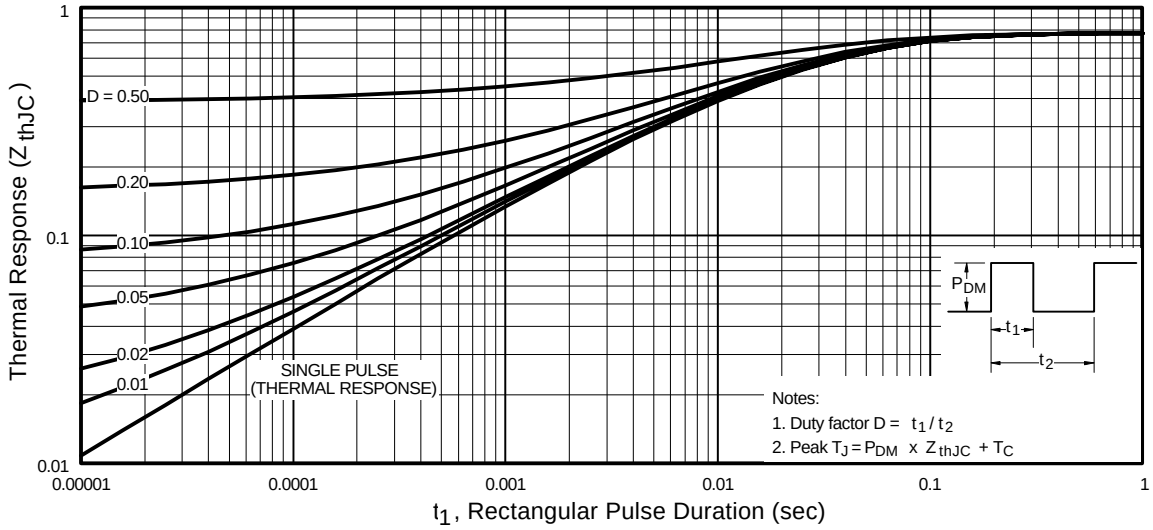


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

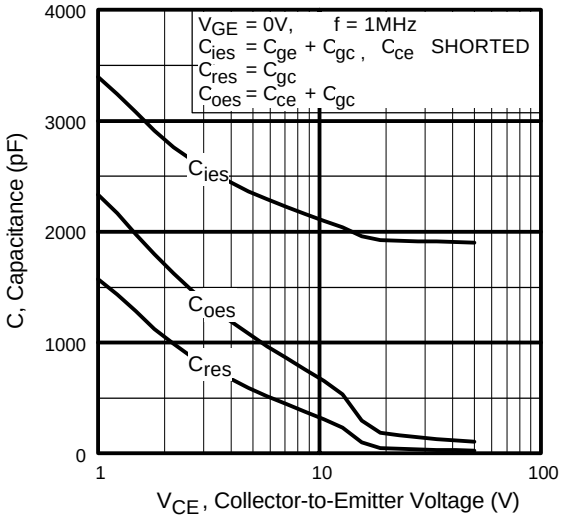


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

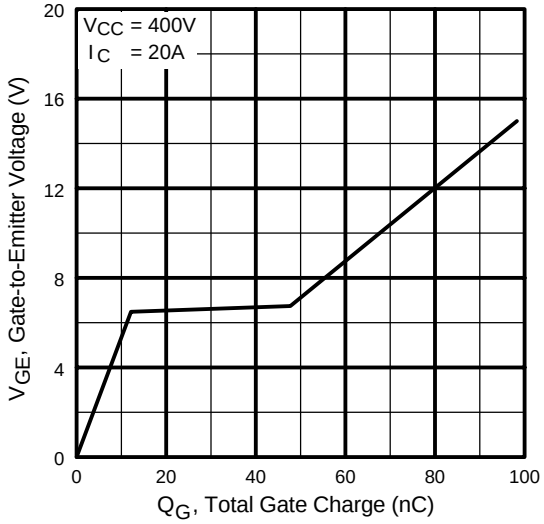


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

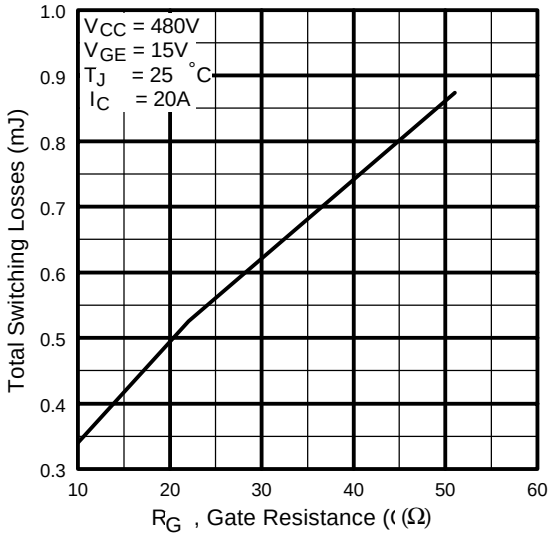


Fig. 9 - Typical Switching Losses vs. Gate Resistance

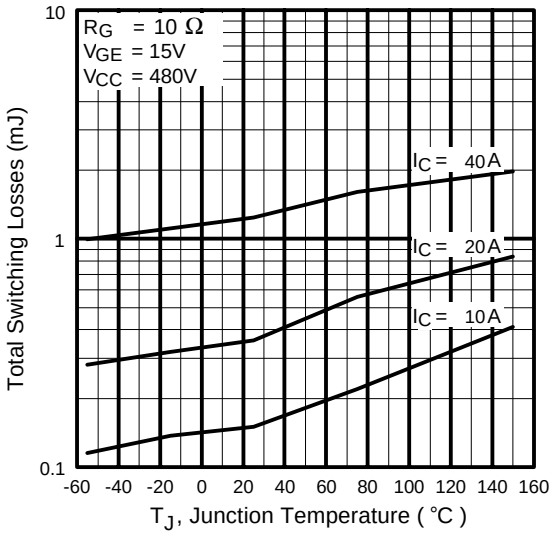


Fig. 10 - Typical Switching Losses vs. Junction Temperature

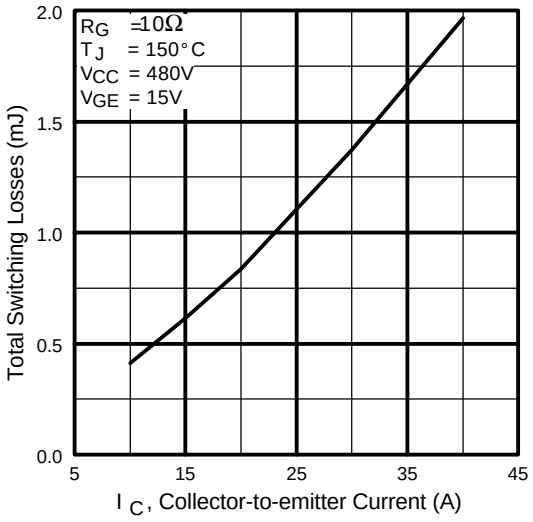


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

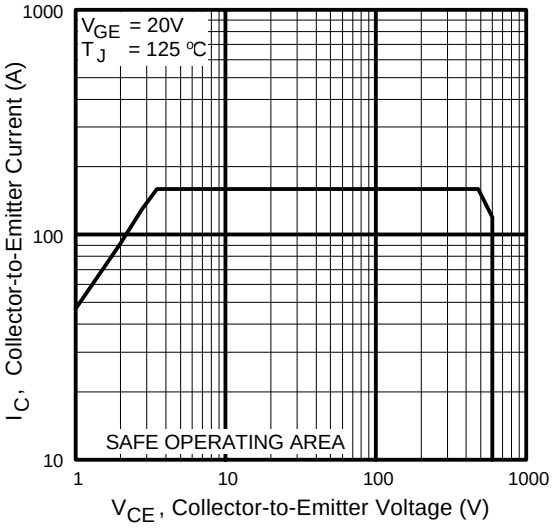


Fig. 12 - Turn-Off SOA

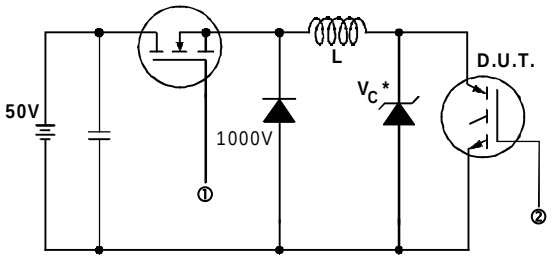


Fig. 13a - Clamped Inductive Load Test Circuit

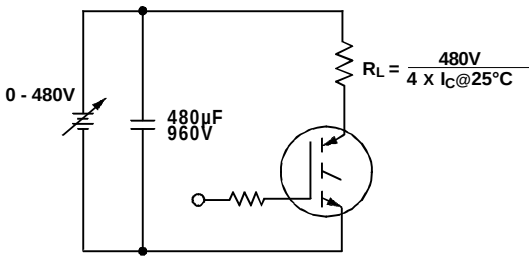


Fig. 13b - Pulsed Collector Current Test Circuit

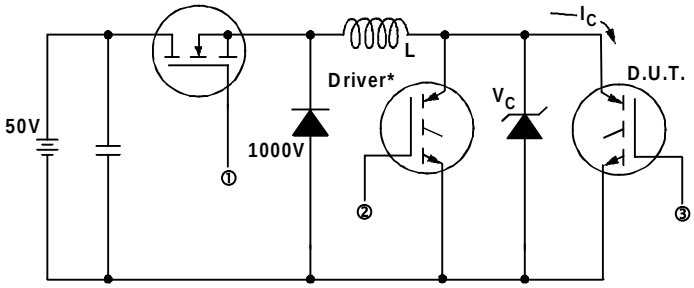


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

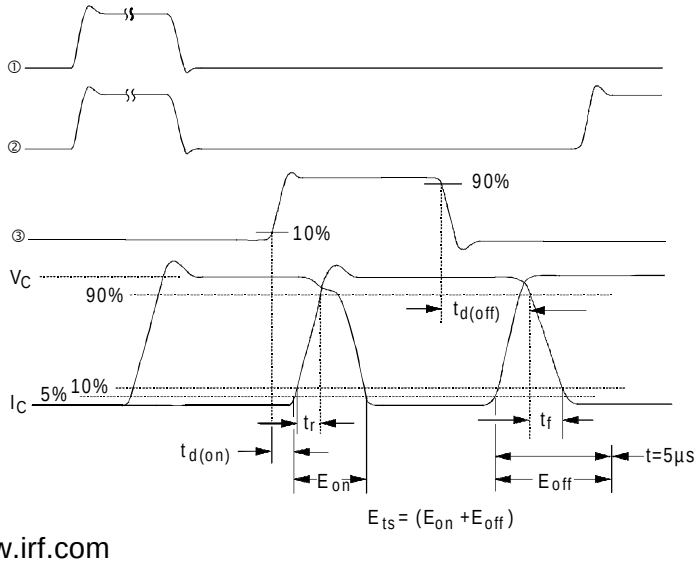
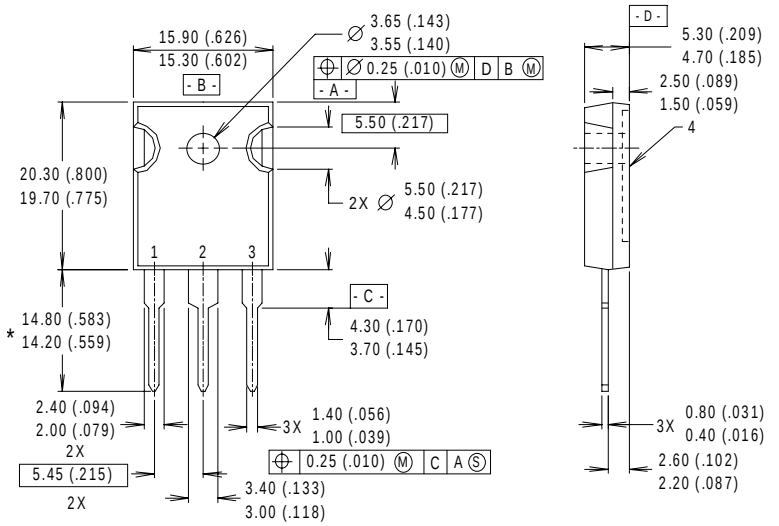


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

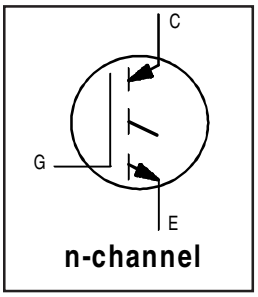
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 4/00

PD - 91657B

International
IOR Rectifier

IRG4PC50W

INSULATED GATE BIPOLAR TRANSISTOR



n-channel

V_{CES} = 600V

$V_{CE(on)\ max.}$ = 2.30V

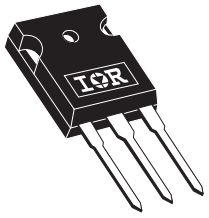
@V_{GE} = 15V, I_C = 27A

Features

- Designed expressly for Switch-Mode Power Supply and PFC (power factor correction) applications
- Industry-benchmark switching losses improve efficiency of all power supply topologies
- 50% reduction of Eoff parameter
- Low IGBT conduction losses
- Latest-generation IGBT design and construction offers tighter parameters distribution, exceptional reliability

Benefits

- Lower switching losses allow more cost-effective operation than power MOSFETs up to 150 kHz ("hard switched" mode)
- Of particular benefit to single-ended converters and boost PFC topologies 150W and higher
- Low conduction losses and minimal minority-carrier recombination make these an excellent option for resonant mode switching as well (up to >300 kHz)



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	55	A
I_C @ T_C = 100°C	Continuous Collector Current	27	
I_{CM}	Pulsed Collector Current ①	220	
I_{LM}	Clamped Inductive Load Current ②	220	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	170	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.64	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

2/7/2000

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)CES}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.41	—	V/°C	V_{GE} = 0V, I_C = 5.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.93	2.3	V	I_C = 27A V_{GE} = 15V
		—	2.25	—		I_C = 55A See Fig.2, 5
		—	1.71	—		I_C = 27A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.0mA
g_{fe}	Forward Transconductance ⑤	27	41	—	S	V_{CE} = 100 V, I_C = 27A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	5000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	180	270	nC	I_C = 27A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	24	36		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	63	95		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	46	—	ns	
t_r	Rise Time	—	33	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	120	180		I_C = 27A, V_{CC} = 480V
t_f	Fall Time	—	57	86		V_{GE} = 15V, R_G = 5.0Ω
E_{on}	Turn-On Switching Loss	—	0.08	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.32	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	0.40	0.5		
$t_{d(on)}$	Turn-On Delay Time	—	31	—	ns	T_J = 150°C,
t_r	Rise Time	—	43	—		I_C = 27A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	210	—		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	62	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.14	—	mJ	See Fig. 10,11, 14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	3700	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	260	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	68	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 5.0Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

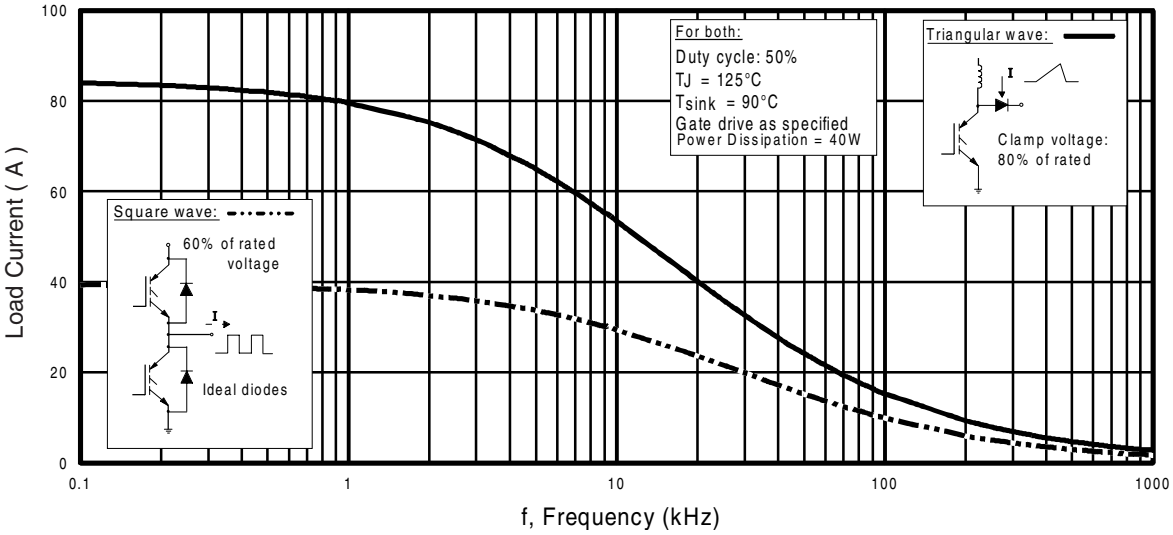


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

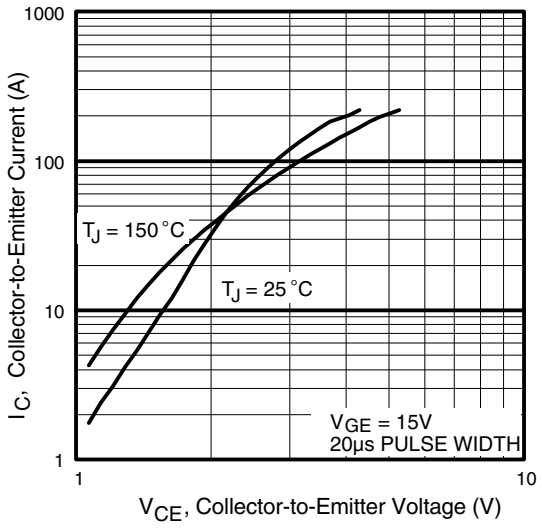


Fig. 2 - Typical Output Characteristics

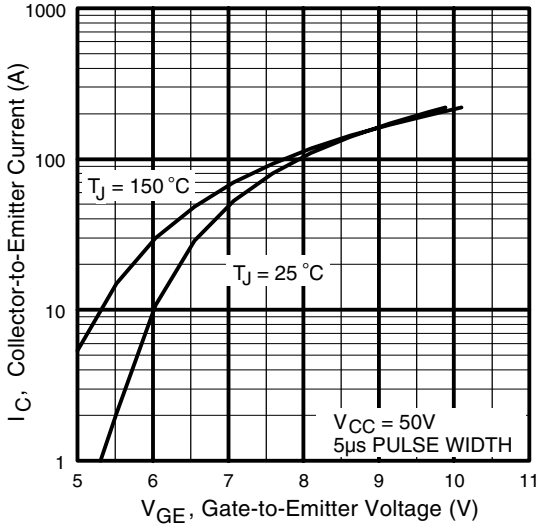


Fig. 3 - Typical Transfer Characteristics

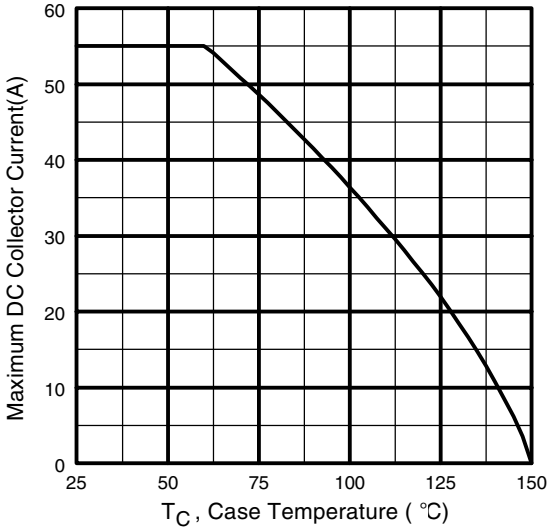


Fig. 4 - Maximum Collector Current vs. Case Temperature

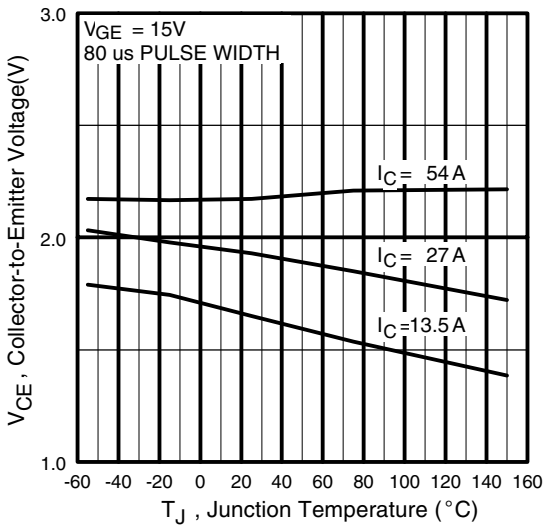


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

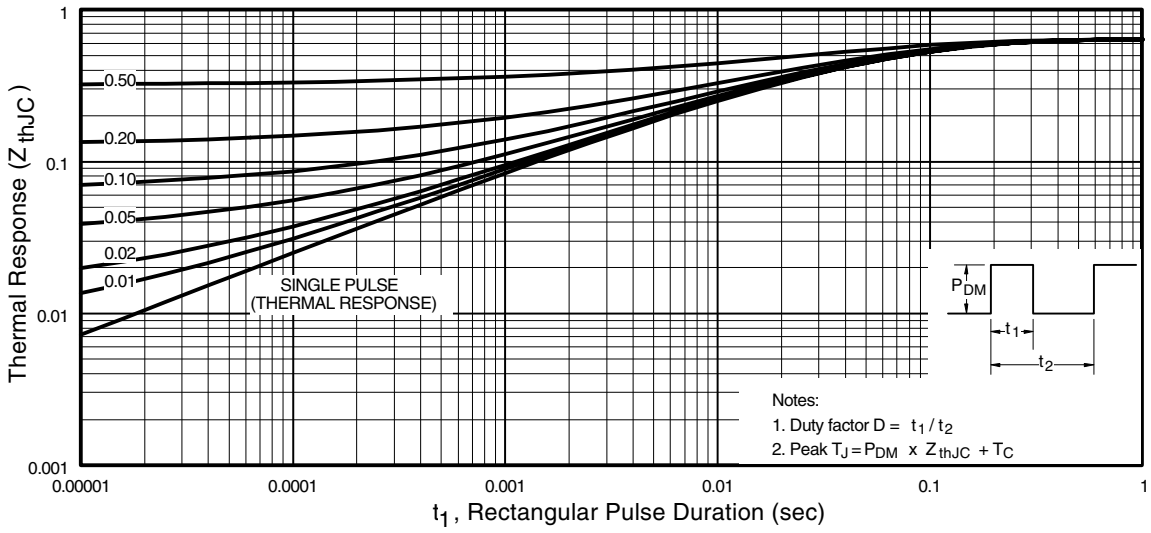


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

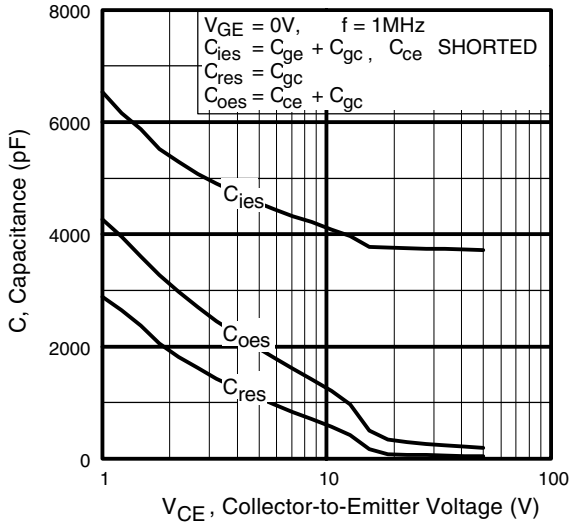


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

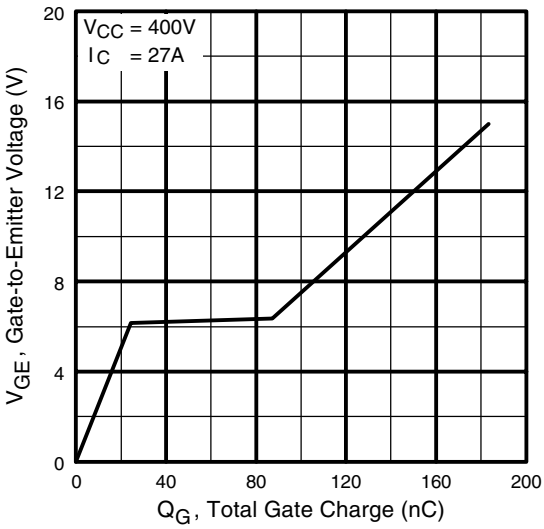


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

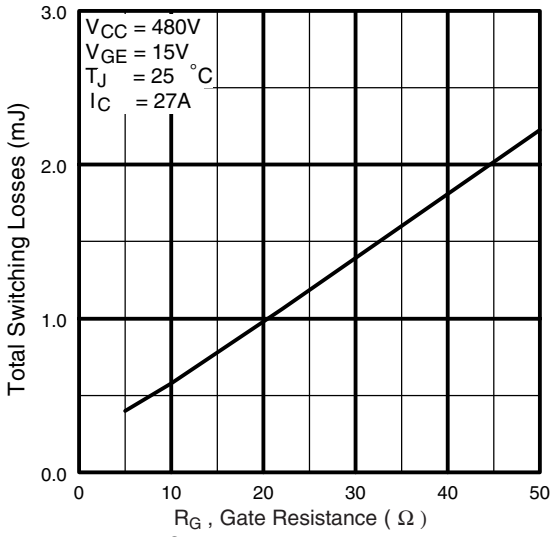


Fig. 9 - Typical Switching Losses vs. Gate Resistance

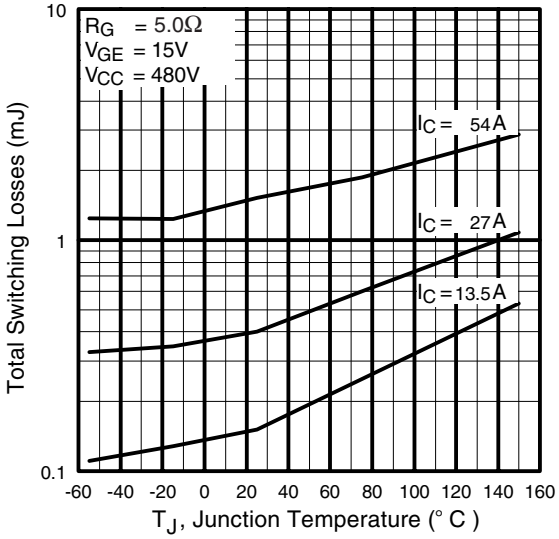


Fig. 10 - Typical Switching Losses vs. Junction Temperature

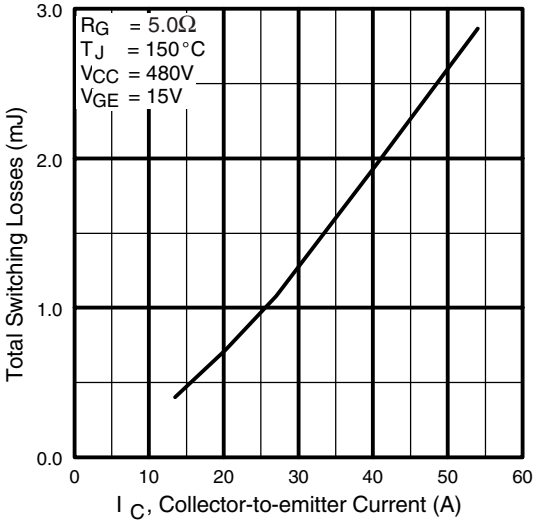


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

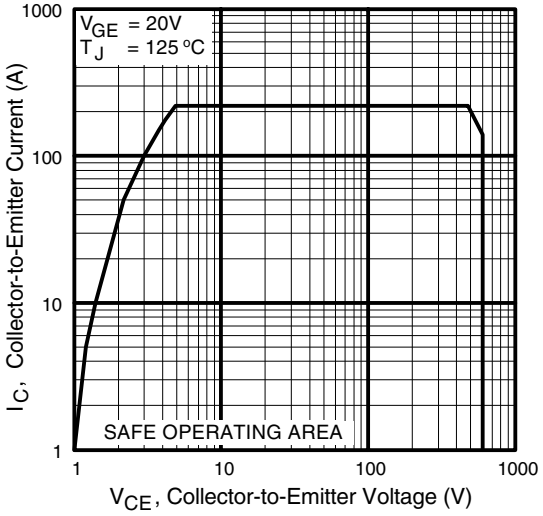


Fig. 12 - Turn-Off SOA

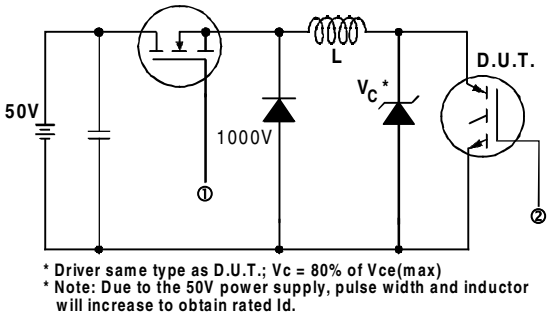


Fig. 13a - Clamped Inductive Load Test Circuit

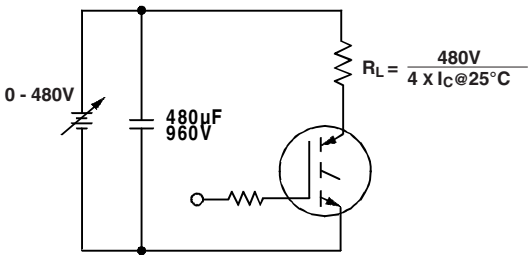


Fig. 13b - Pulsed Collector Current Test Circuit

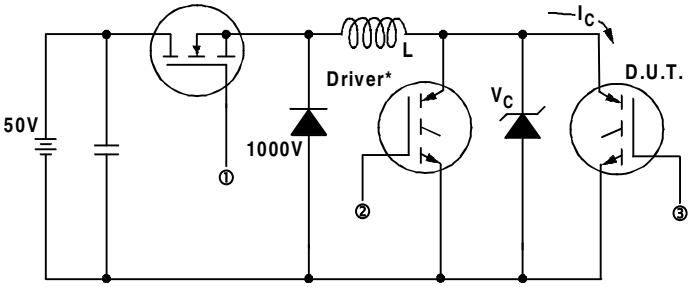


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 480V**

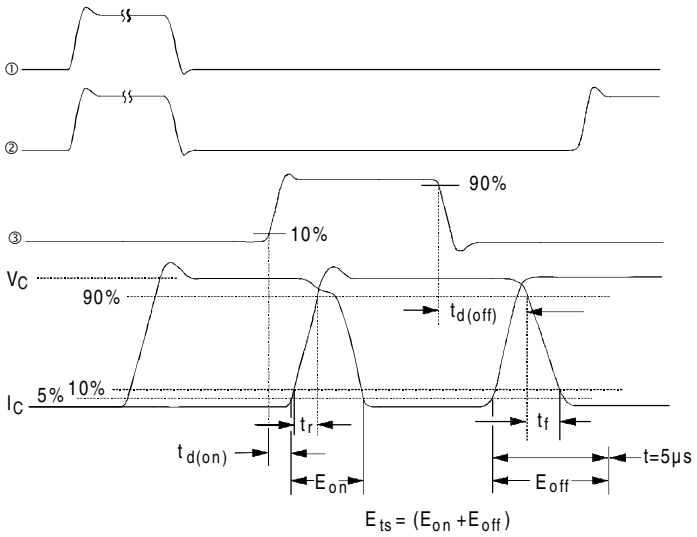
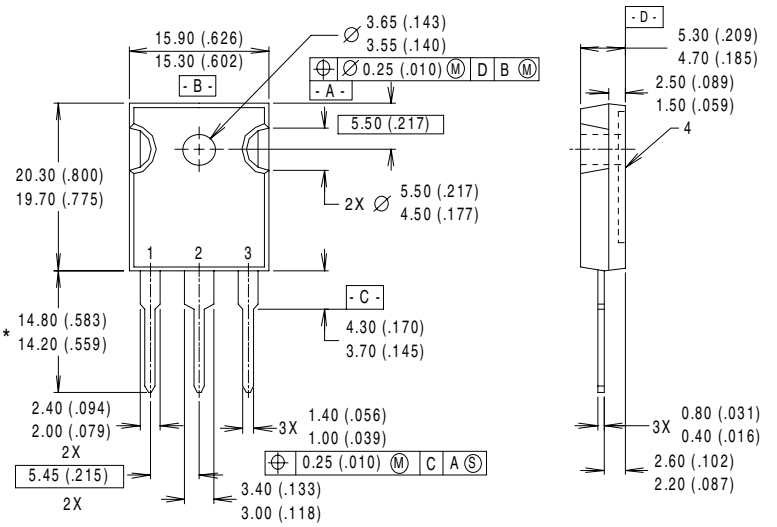


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
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3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
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LEAD ASSIGNMENTS
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2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
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International
IOR Rectifier

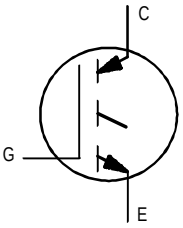
PD - 91710

IRG4PF50W

INSULATED GATE BIPOLAR TRANSISTOR

Features

- Optimized for use in Welding and Switch-Mode Power Supply applications
- Industry benchmark switching losses improve efficiency of all power supply topologies
- 50% reduction of Eoff parameter
- Low IGBT conduction losses
- Latest technology IGBT design offers tighter parameter distribution coupled with exceptional reliability



n-channel

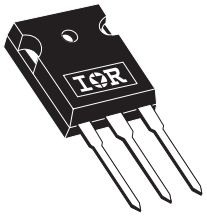
V_{CES} = 900V

$V_{CE(on)\ typ.}$ = 2.25V

@V_{GE} = 15V, I_C = 28A

Benefits

- Lower switching losses allow more cost-effective operation and hence efficient replacement of larger-die MOSFETs up to 100kHz
- Of particular benefit in single-ended converters and Power Supplies 150W and higher
- Reduction in critical Eoff parameter due to minimal minority-carrier recombination coupled with low on-state losses allow maximum flexibility in device application



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	900	V
I_C @ T_C = 25°C	Continuous Collector Current	51	A
I_C @ T_C = 100°C	Continuous Collector Current	28	
I_{CM}	Pulsed Collector Current ①	204	
I_{LM}	Clamped Inductive Load Current ②	204	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	186	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.64	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	——	40	
Wt	Weight	6 (0.21)	——	g (oz)

4/15/98

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	900	——	——	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	——	——	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	——	0.295	——	V/°C	V_{GE} = 0V, I_C = 3.5mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	——	2.25	2.7	V	I_C = 28A V_{GE} = 15V
		——	2.74	——		I_C = 60A See Fig.2, 5
		——	2.12	——		I_C = 28A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	——	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	——	-13	——	mV/°C	V_{CE} = V_{GE}, I_C = 1.0mA
g_{fe}	Forward Transconductance ⑤	26	39	——	S	V_{CE} ≥ 15V, I_C = 28A
I_{CES}	Zero Gate Voltage Collector Current	——	——	500	µA	V_{GE} = 0V, V_{CE} = 900V
		——	——	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		——	——	5.0	mA	V_{GE} = 0V, V_{CE} = 900V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	——	——	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	——	160	240	nC	I_C = 28A
Q_{ge}	Gate - Emitter Charge (turn-on)	——	19	29		V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	——	53	80		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	——	29	——	ns	
t_r	Rise Time	——	26	——		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	——	110	170		I_C = 28A, V_{CC} = 720V
t_f	Fall Time	——	150	220		V_{GE} = 15V, R_G = 5.0Ω
E_{on}	Turn-On Switching Loss	——	0.19	——	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	——	1.06	——		See Fig. 10, 11, 13, 14
E_{ts}	Total Switching Loss	——	1.25	1.7		
$t_{d(on)}$	Turn-On Delay Time	——	28	——	ns	T_J = 150°C,
t_r	Rise Time	——	26	——		I_C = 28A, V_{CC} = 720V
$t_{d(off)}$	Turn-Off Delay Time	——	280	——		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	——	90	——		Energy losses include "tail"
E_{ts}	Total Switching Loss	——	3.45	——	mJ	See Fig. 13, 14
L_E	Internal Emitter Inductance	——	13	——	nH	Measured 5mm from package
C_{ies}	Input Capacitance	——	3300	——	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	——	200	——		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	——	45	——		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 5.0Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

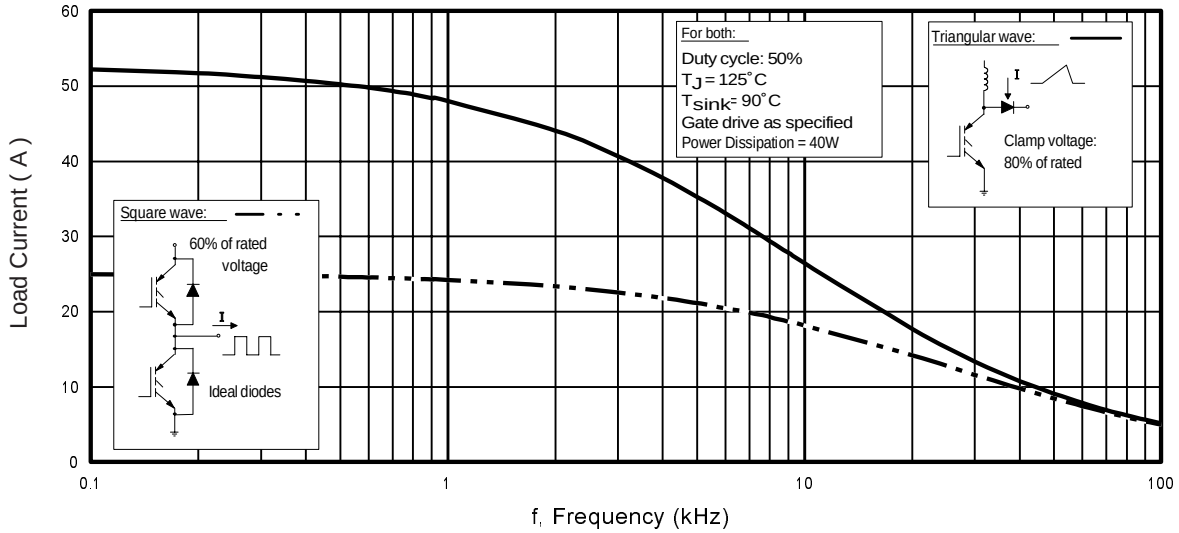


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I=I_{RMS}$ of fundamental; for triangular wave, $I=I_{PK}$)

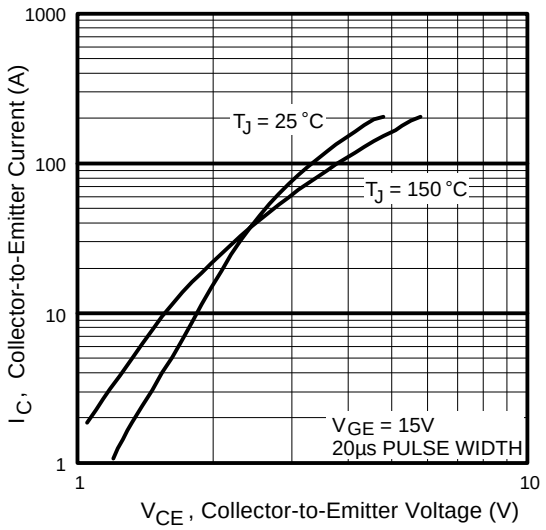


Fig. 2 - Typical Output Characteristics

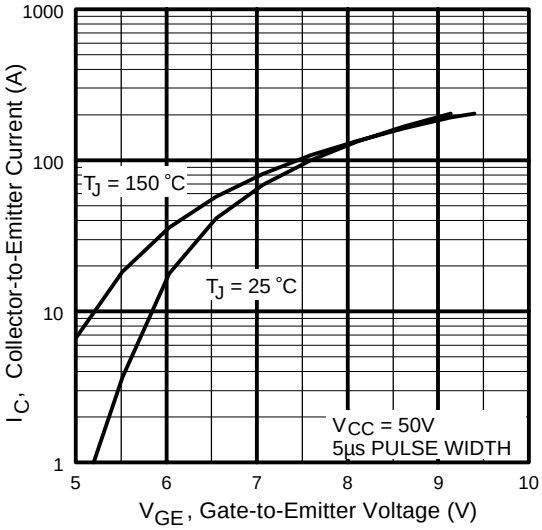


Fig. 3 - Typical Transfer Characteristics

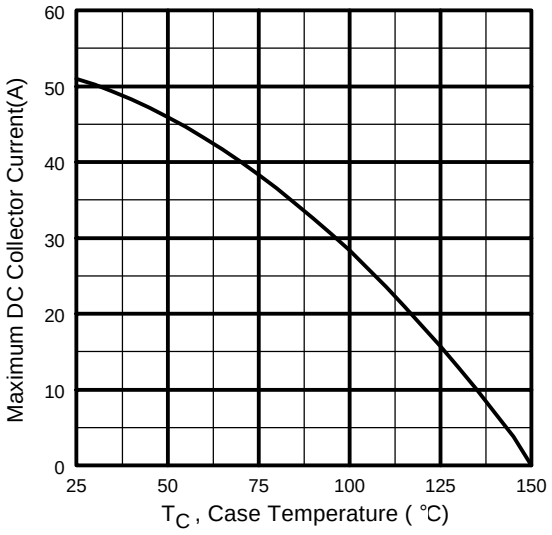


Fig. 4 - Maximum Collector Current vs. Case Temperature

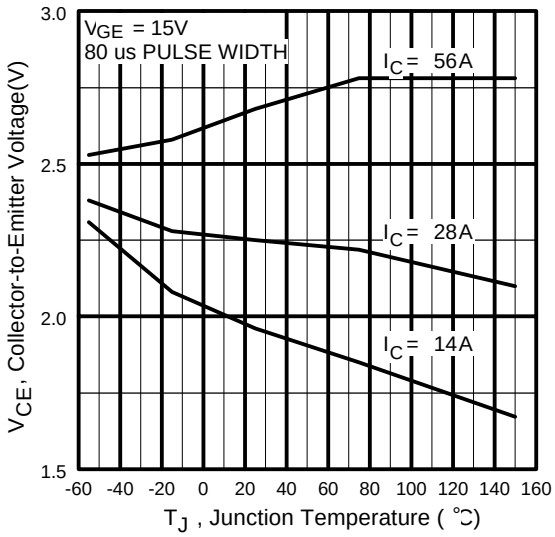


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

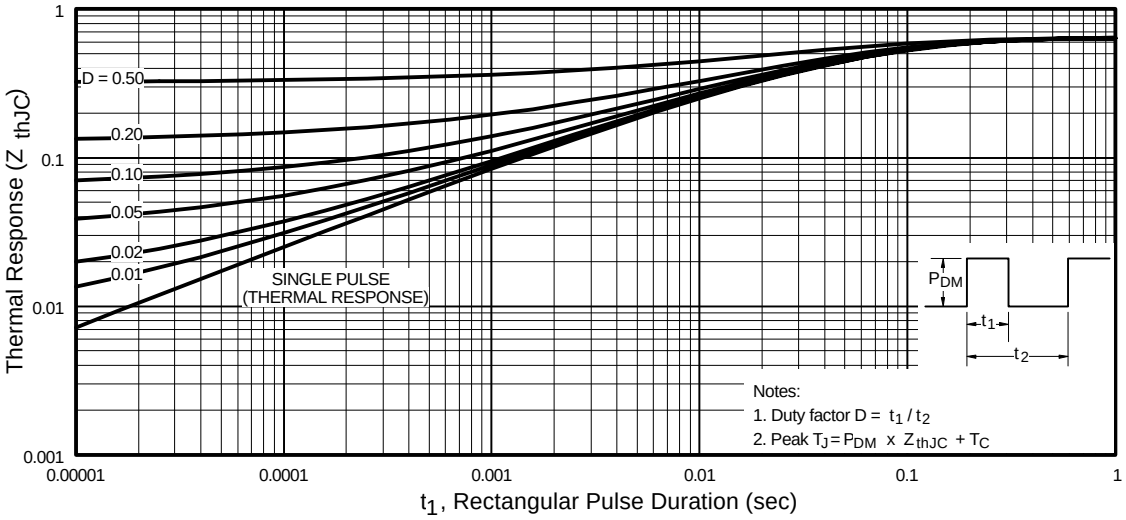


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

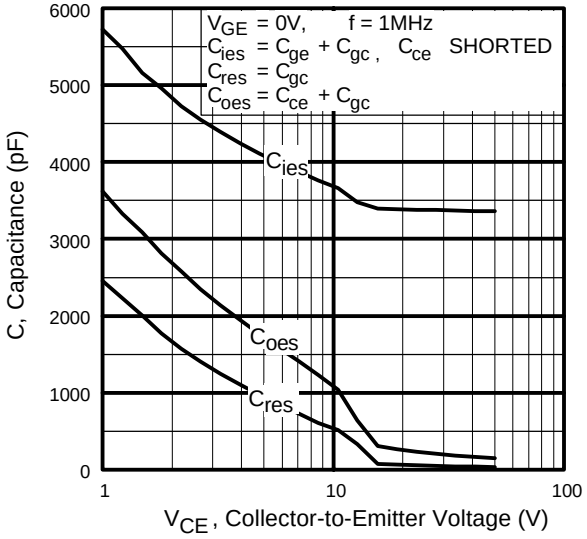


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

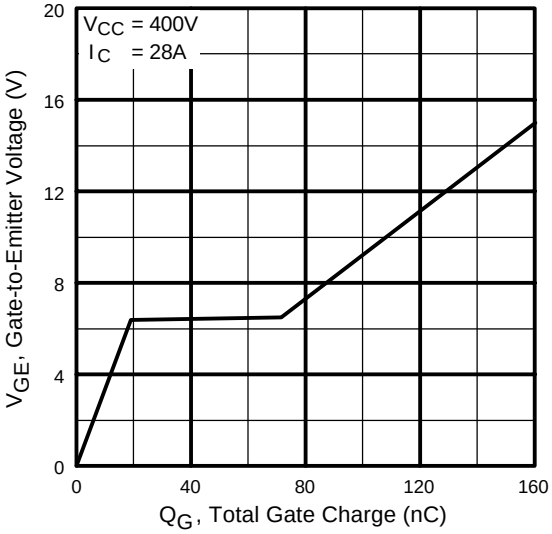


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

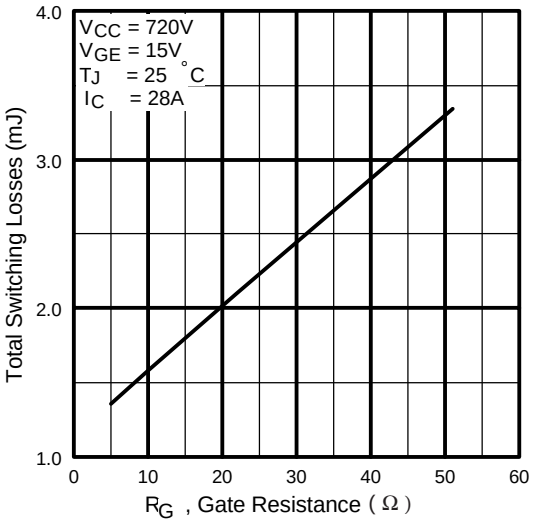


Fig. 9 - Typical Switching Losses vs. Gate Resistance

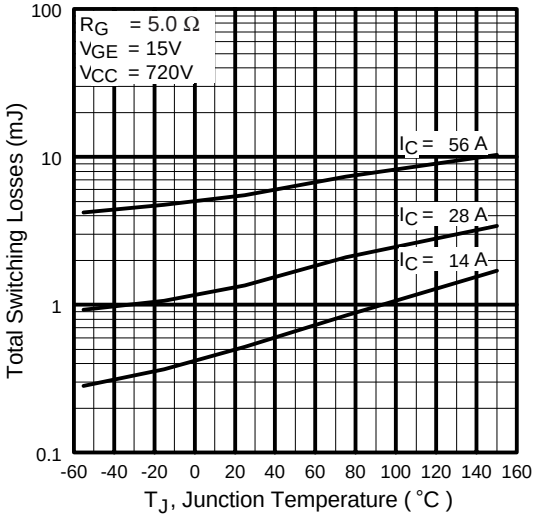


Fig. 10 - Typical Switching Losses vs. Junction Temperature

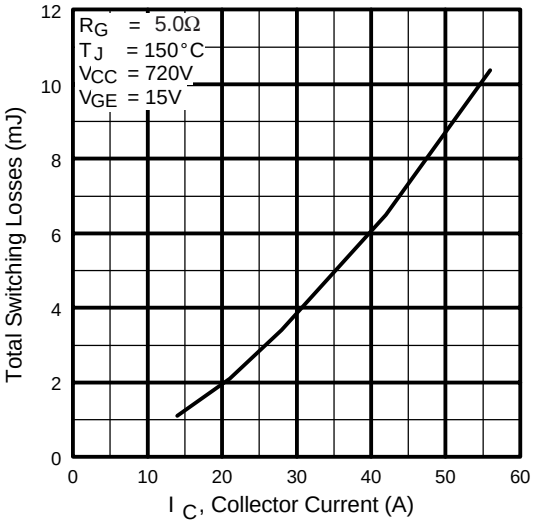


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

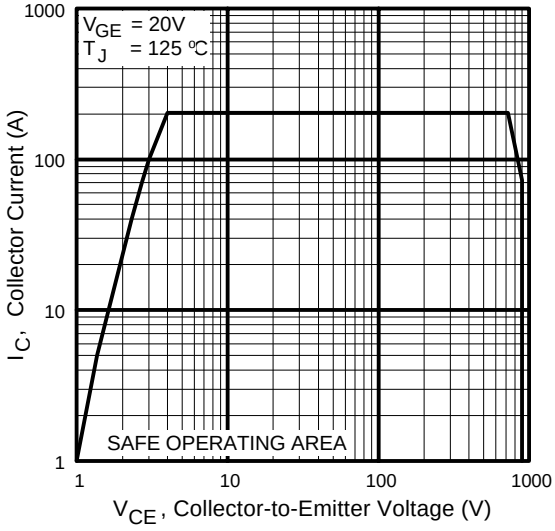


Fig. 12 - Turn-Off SOA

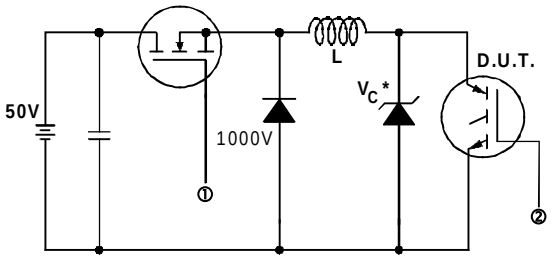


Fig. 13a - Clamped Inductive Load Test Circuit

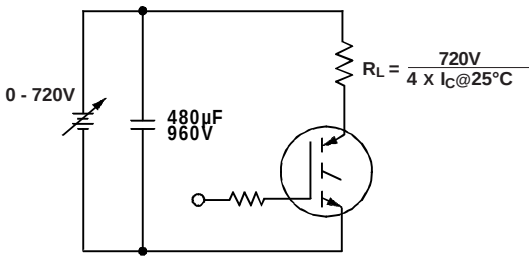


Fig. 13b - Pulsed Collector Current Test Circuit

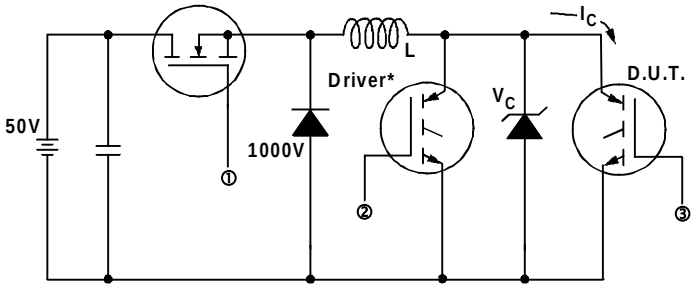


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 720V**

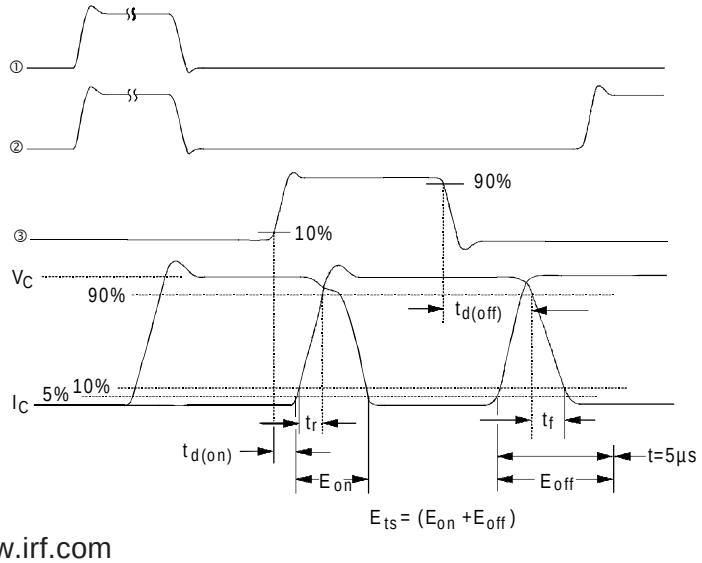
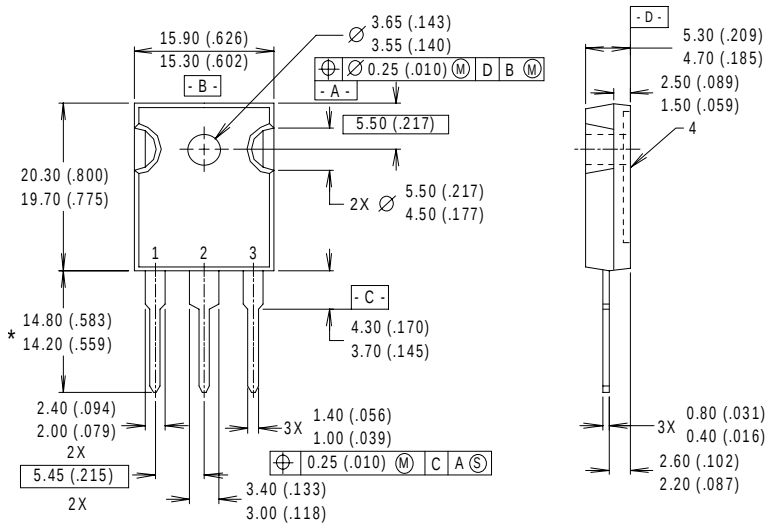


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T 3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: 171 (K&H Bldg.) 30-4 Nishi-ikebukuro 3-chome, Toshima-ku, Tokyo Japan Tel: 81 33 983 0086
IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 16907 Tel: 65 221 8371

Data and specifications subject to change without notice.

Application Note

International
IOR Rectifier

AN-1027

ADD-A-Pak Module Mounting Instructions

Proper mounting and exchanger surface preparation are generally very important to optimize the heat transfer from module to heatsink. The following procedure is recommended:

Heatsink Preparation

The contact surface of heatsink must be flat, with a recommended tolerance of < 0.03mm (1.18 mil) and a leveling depth of < 0.02mm (0.79 mil), according to DIN/ISO 1302.
In general, a milled or machined surface is satisfactory if prepared with tools in good working condition.

The heatsink mounting surface must be clean, with no dirt, corrosion, or surface oxides. It is very important to keep the mounting surface free from particles exceeding in thickness 0.05mm (2 mils), provided thermal compound is used

Visual Inspection

Inspect the power i-nodule to insure that the contact surface of the base is clean, that there are no lumps or bulges on the base plate that could damage the base or reduce heat transfer across the surfaces.

Thermal Compound

Coat uniformly the heatsink mounting surfaces and power module base plate with a good quality thermal compound.
Apply uniform pressure on the package to force the compound to spread over the entire contact area.

Module Fastening

Bolt the module to the heatsink using the two fixing holes. The recommended torque is 5Nm ± 10%. An even amount of torque should be applied for each individual mounting screw.

A torque wrench, accurate in the specified range, must be used in mounting module, in order to achieve optimum results. The mounting screws must be tightened in sequence.

After a period of about 3 hours, recheck the torque with a final tightening in opposite sequence to allow the spread of the compound.
Remove the excess thermal grease around the base of the module with a soft lint-free cloth soaked in alcohol.

Electrical Connection

Tighten the M5 screws to the power terminals applying a torque of 4Nm ± 10% avoiding any pressure on the module.
The gate and auxiliary cathode connections should be made via the flying leads as supplied. If International Rectifier hardware is not available, use only fast-on connectors 2.8mm x 0.8mm. The length of the flying leads should be kept as short as is physically possible.

Gate circuit return connection should always be accomplished by way of the auxiliary cathode connection.

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Surface Mounting of Larger Devices

By Pamela Dugdale and Arthur Woodworth

Introduction

The increasing trend to board mounted power devices has brought a demand for Surface Mount Devices (SMD) larger than the commonly available D-Pak and D²Pak packages. A series of devices have been introduced to enable this higher power levels to be achieved in SMD. This application note details some of the solutions presently available from International Rectifier, ranging from D²pak and solderable versions of the Super-220™ and TO-247 packages that can accommodate larger die (table 1).

The Super-220 and SMD-247™ are each with available either with long straight leads suitable for mounting to a daughter board or short gull wing leads suitable for traditional surface mounting. Larger devices need somewhat more care at the surface mount assembly due to the greater thermal masses and higher thermal mismatches which are potentially present and not all the techniques described in AN-994 'Maximising the Effectiveness of Your SMD Assemblies' are applicable.

Package	Max Die Size (mils)
Super220™ (TO-273AA)	257 x 257
SMD – 247™	257 x 360

Table 1

Board Materials

At the higher power levels associated with these larger devices significant amounts of heat can be generated. Simple FR4 boards may be unable to deal with this and alternative materials such as multilayer FR4 with vias, IMS or DBC on Alumina will be required. The assembly methods and especially the times must take account of the substantial thermal mass that they represent.

Thermal Resistance

The exact value of board mounted thermal resistance is dependant on the surrounding environment, board layout, orientation, airflow etc. Table 2 provides a guideline for comparison between some of the commonly used materials. The reference device is an IRFP450-S SMD-247™.

	Rth j-a for IRFP450-S mounted:	
Board Material	In free air	Mounted to large Aluminium block
Single FR4 – 1.6mm, 2oz Cu	25	10
Al. IMS –3mm, 3oz Cu	6	1
DBC – 0.38mm, 0.3mm Cu	24	1

Table 2

The thermal performance of PCB structures can be improved by choice of material (e.g. weight of copper) and layout. Some examples of typical improvements that can be achieved are:

- Extended copper areas on board reduces thermal resistance by ~ 20%
- Multilayer board with groundplane reduces thermal resistance by ~ 50%
- Multilayer board with vias to groundplane reduces thermal resistance by ~ 66%

Board Mounting

The SMD packages described are supplied with exposed rear face and leads specially treated to give good solderability during reflow. A suitable mounting pad must be defined on the substrate to accommodate the package. The package outlines and minimum footprints for the 3 large are shown in appendices 1&2. The correct amount of solder paste is dispensed onto the substrate via a stencil. Recommended thickness is 8 – 10 mils.

Board Attach Materials

Reflow soldering paste consists of particles of solder and flux together with binder, solvents and additives. An ideal solder paste would have good printing properties, be slump-free, have good 'tack' to hold the components and remove oxides without leaving obstinate residues.
Recommended solder paste alloys for reflow are shown in table 3.

Solder Alloy	Solidus	Liquidus	Peak Reflow
63Pb/37Sn	183°C	183°C	225°C
60Pb/40Sn	183°C	190°C	230°C
62Pb/36Sn/2Ag	180°C	189°C	230°C

Table 3

Board Attachment Methods

Convection Oven: Devices and substrates pass through a convection heating tunnel on a conveyer belt. The 4-5 zones for preheating, reflowing and cooling are independently temperature controlled. This is a preferred method, especially with substrates of significant thermal inertia.

Infra Red Reflow: Infra red radiating lamps provide the heat source. There is a danger that the relatively large 'black bodies' of the power semiconductors are overheated before the board temperature is raised sufficiently to reflow the solder. Can be successfully combined with the previous method.

Conduction Reflow: Heat is applied from hotplates to the bottom of the boards. 'Walking beams' or 'brown belts' transport the boards. Effective when used with materials like IMS.

Vapour Phase Reflow: The populated boards are lowered into the vapour cloud above a boiling fluorocarbon liquid. Provides precise temperature control but is inefficient when used with high thermal mass assemblies, resulting in slow throughput and loss of the expensive fluid.

Wave Soldering: Not recommended for large devices with high thermal mass and large interface areas to reflow. Large package devices tend to create 'shadow' areas that create difficulties for other smaller SMD parts to be soldered on the same board.

Reflow Profile

The optimum profile for a given application will depend on the materials used for board and solder and on the degree of population. However, the following guidelines will provide a satisfactory result.

Preheat phase: The subassembly is raised to and stabilised at a temperature of 105°C - 150°C at a ramp rate of < 6°C/s (typ.2.5°C/s). Volatile components of the solder paste are driven off and the flux is activated. If the ramp is too steep it could result in thermal shock damage. The required stabilisation time will vary depending on the mass of the subassembly. Excessive dwell can over bake the solder and reduce the effectiveness of the flux.

Reflow phase: The temperature is raised above the melting point of the solder. Peak temperature is chosen to achieve good solder fluidity. Excessively high peak temperatures can cause die damage. Time above 183°C should not exceed 150 seconds. (typ. ~100 secs).

Cooling phase: The temperature is brought down again close to ambient and the assembly exits the furnace. Mechanical shock should be avoided during this phase. Rapid cooling rates promote small grain size in the solder layer, which is desirable for improved thermal fatigue performance. However extremely rapid cooling rates can result in excessive shock. Ramp rates of
< 6°C/s are recommended. (typ.2.5°C/s).

A typical reflow profile for any of the large power devices is shown in fig. 1

Board cleaning

If an RA, RMA or water soluble flux has been used a cleaning phase should follow reflow. The solder paste vendors will advise appropriate materials and process. Although 'no clean' fluxes are available from a number of sources,

in high voltage applications a cleaning stage is still recommended - especially if a conformal coating or potting process is to be used.

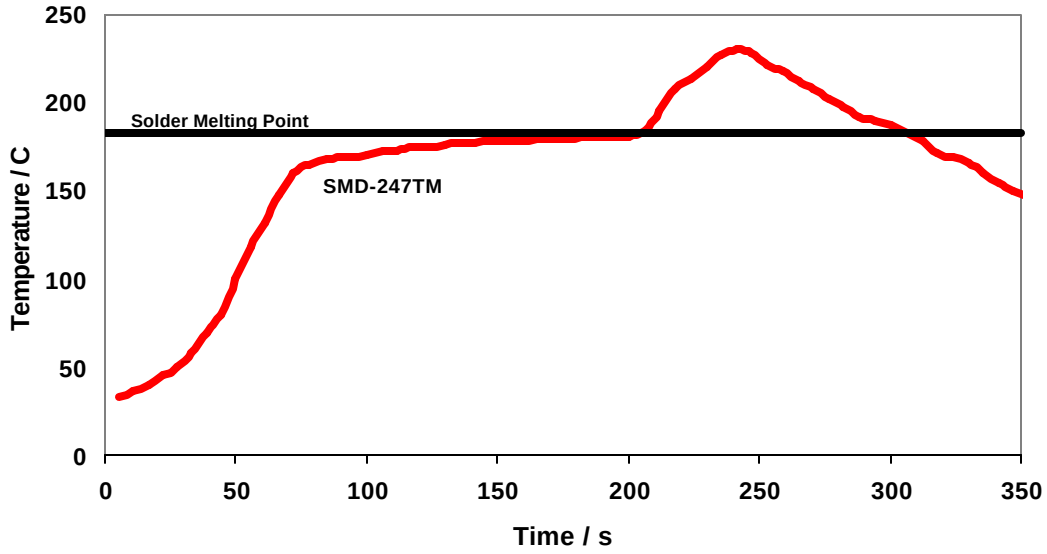
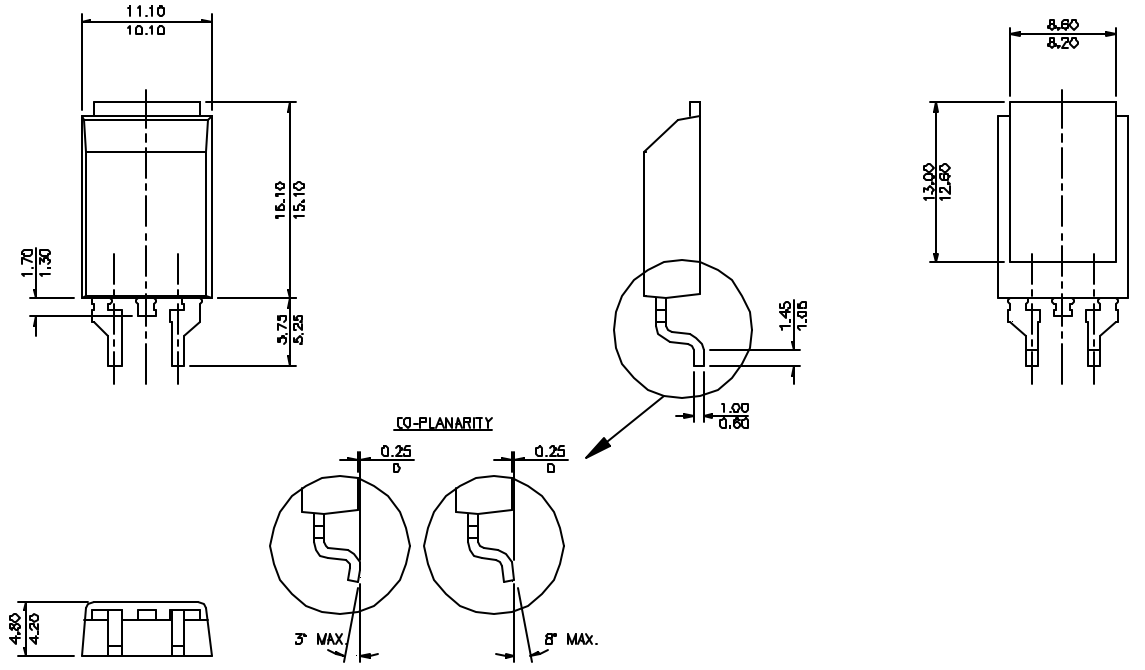


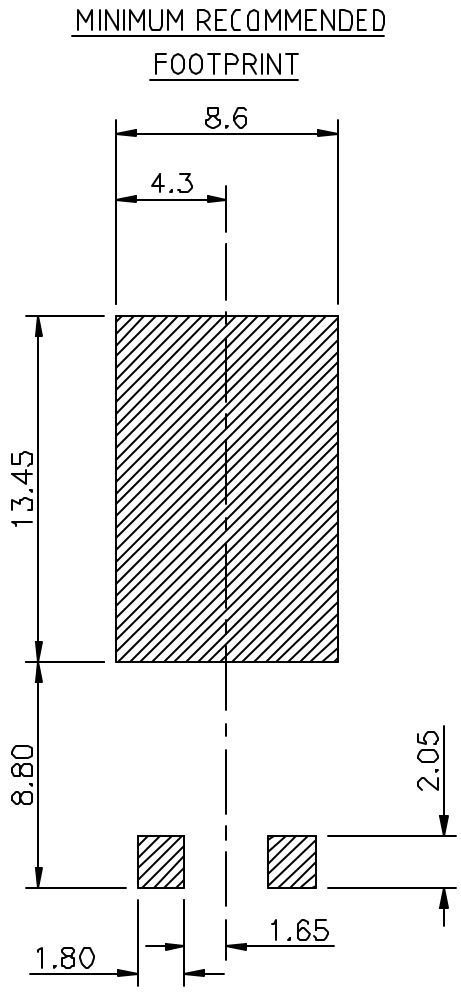
Fig.1 Typical reflow profile for SMD-247™

Conclusion

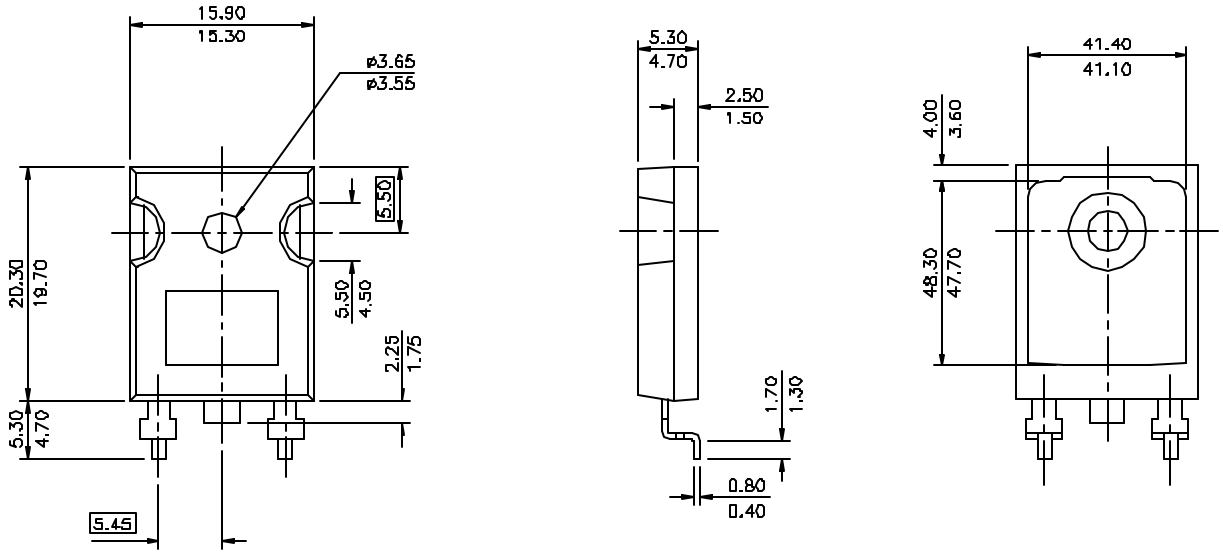
International Rectifier has developed a range of higher power surface mount packages. Following the industry standard guidelines described in this note will ensure trouble free mounting and performance.



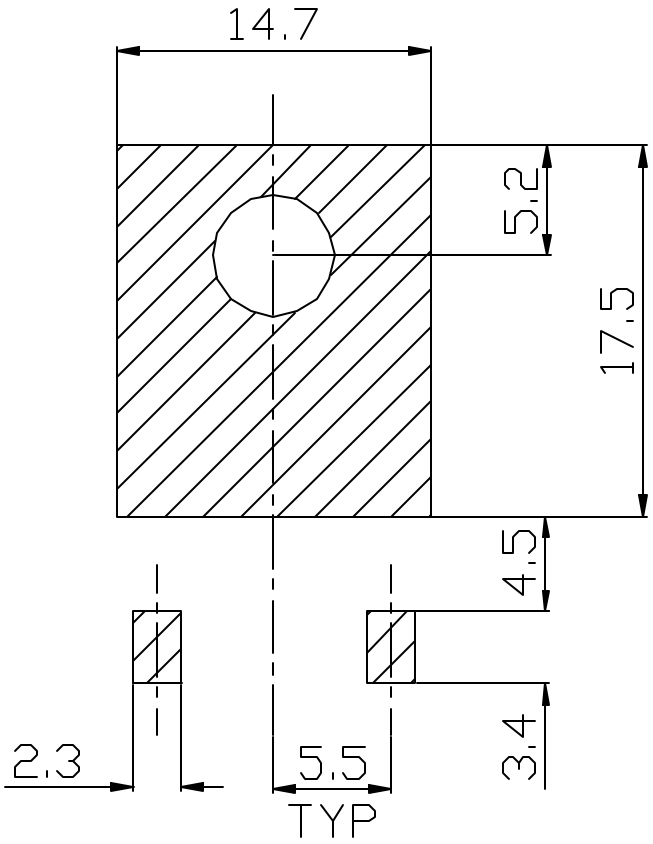
Appendix 1a Super-220™ Outline drawing



Appendix 1b Super-220™ minimum footprint



Appendix 2a SMD-247™ Outline drawing



Appendix 2b SMD-247™ Minimum Footprint

Mounting Guidelines for the SUPER-247

by Andrew Sawle and Arthur Woodworth

Introduction

Born from the need to accommodate ever increasing amounts of silicon in smaller, space saving packages, the SUPER-247 now allows the same die sizes that can be put in a much larger TO-264. The SUPER-247 has the same outer dimensions as the industry standard TO-247 but can dissipate more power than the TO-247 whilst occupying less space than the TO-264. This package also allows the use of efficient and reliable clip mounting methods to heatsinks. This allows designers to reduce both the size and the cost of their systems.

This Application Note will examine the subjects involved with clip mounting the SUPER-247 to heatsinks.

Topics Covered:

A breakdown of system thermal resistance.
The minimum force for a good thermal contact and the maximum force allowable before device parameter degradation.
Wet and dry contact conditions and the effect on thermal resistance.
The effect on thermal resistance of using an electrical isolator between the device and the heatsink.
Typical clip types, how they work and the forces that they impart. Conclusion.

1. A Breakdown of System Thermal Resistance

The thermal resistance ($Rth_{(junction\text{-}ambient)}$) of a system (system = package through to heatsink) is made up from a number of component parts as shown in Figure 1.1 below.

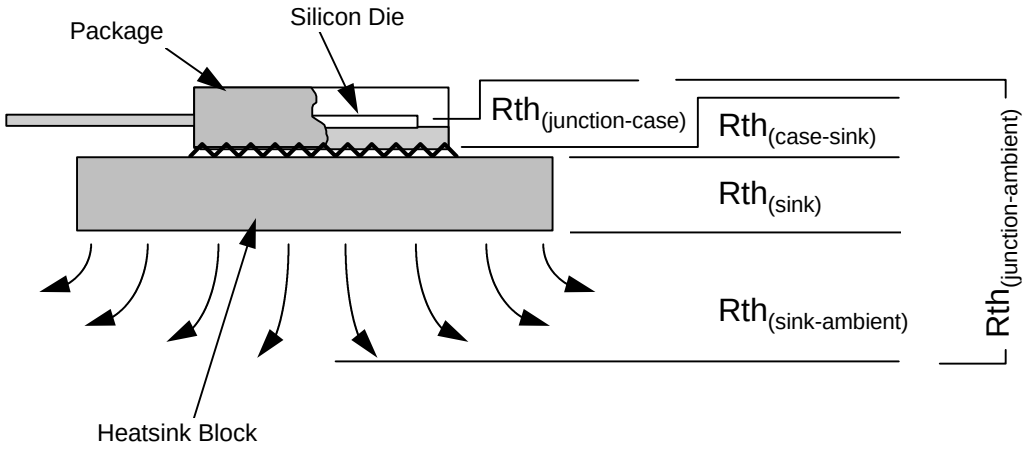


Figure 1.1 - Build-up of Thermal Resistance in a System

The designer of a system has varying amounts of influence over the component parts of the overall thermal resistance of his design:

- $\mathbf{R_{th(junction\text{-}case)}}$ - this has been determined during the design and manufacture of the product. The system designer has no direct influence.
- $\mathbf{R_{th(case\text{-}sink)}}$ **(or Contact Thermal Resistance)** - determined by the size and quality of the contact areas between the package and the sink, the use of intermediate materials and the contact pressure. Hence, the system designer can have a large influence over this parameter.
- $\mathbf{R_{th(sink)}}$ **and** $\mathbf{R_{th(sink\text{-}ambient)}}$ - determined by heatsink design, *i.e. material and shape.* System designer will choose optimum sink matching both performance and cost requirements.

Thermal resistances for packages and heatsinks can be determined from datasheets and although the contact thermal resistances can also be taken from manufacturer's data, this figure is generally 'TYPICAL' and for a single set of specified conditions. Hence, it is possible for a designer to gain better or worse contact thermal resistances depending on parameters that he prescribes. The following sections include some information to help the designer in improving rather than worsening contact thermal resistances in their systems.

2. Minimum and Maximum Contact Forces

As previously mentioned, there are a number of factors that affect the contact thermal resistance, one of the factors being the contact force with which the package is pushed against the heatsink.

Why and How Does Contact Force Affect Thermal Resistance?

Package cases and heatsink surfaces can never be perfectly flat. Hence contact between the two will only occur at several points allowing an air gap between the surfaces (as illustrated in Figure 1.2). Since air is a very good thermal insulator this means that the contact thermal resistance is much greater than it would be if the two surfaces were in perfect contact (no air gap). However, as the contact force (pushing the two surfaces together) increases then so will the number of points at which the two surfaces contact one another and the air-gap will be reduced, in turn reducing the contact thermal resistance.

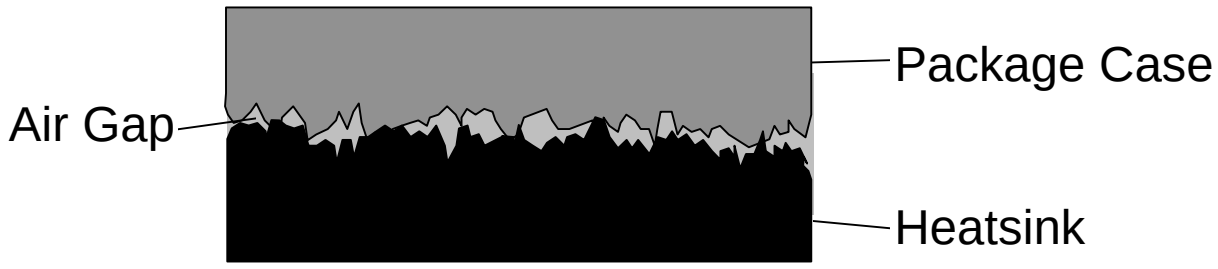


Figure 1.2 - Diagram Showing the Effect (Under High Magnification) When Two Non-Perfect Surfaces Meet.

What is the Minimum Force that Should be Applied to Gain Good Thermal Contact?

As the contact force is increased, the contact thermal resistance decreases. However, this does NOT follow a linear relationship and shows diminishing returns in thermal resistance reduction for increases in the contact force (as shown in Figure 1.3). A rapid initial fall-off in contact thermal resistance is replaced by a more gradual reduction with increased contact force. The minimum contact force should therefore be no lower than the point at which these rapid reductions in thermal resistance end - this occurs at approximately 20N.

Maximum Contact Force

The minimum contact force of 20N mentioned above is purely that, the MINIMUM force. Any force applied above that figure will still show gains in reduced contact thermal resistance until the maximum force that the package can withstand before the device characteristics are altered or the package is destroyed. This maximum limit figure has been measured to be 200N TYP. However, these gains are not free, for in general terms a greater contact force means a larger, more expensive clamping system. A contact force should therefore be chosen that optimises both the thermal and the cost requirements of the system.

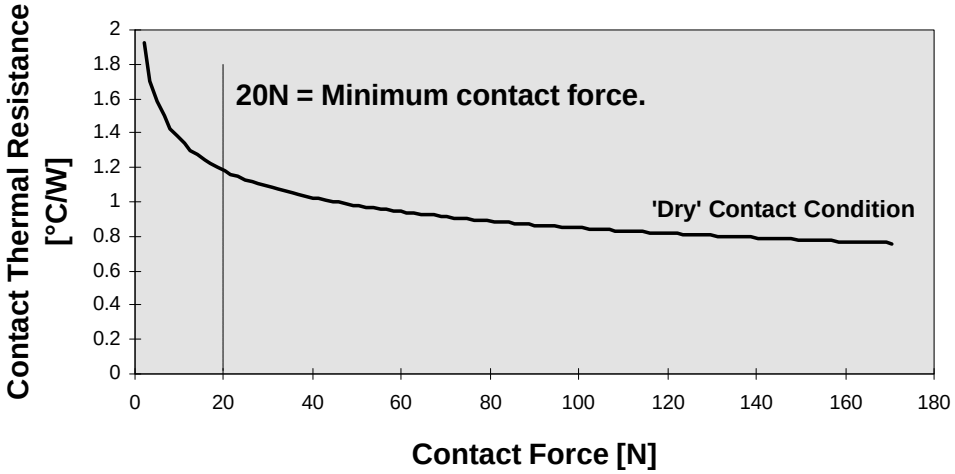


Figure 1.3 - Minimum Contact Force

3. Contact Conditions

As mentioned previously, the contact conditions between the package and the heatsink will affect the contact thermal resistance. Contact conditions encompass a number of areas including: surface roughness, surface cleanliness, paint finishes and intermediate materials. The surface roughness of the heatsinking material should be no greater than 0.02mm over the area where the device is to be mounted. Surface cleanliness during assembly of package and heatsink is imperative, even if a thermal grease or other material is subsequently added. Unclean surfaces can be held apart by dirt or grease thus increasing the thermal resistance. However, normal paint finishes (up to 50 µm thick) have been shown to have little effect on thermal resistance, this therefore leaves intermediate materials as an area for discussion.

Intermediate Materials

Contact between two non-perfect surfaces will result in an air gap between them. The most common method of overcoming this is to use a thermally conductive heatsinking compound to fill the gaps between the surfaces and hence lower the contact thermal resistance. This compound also has the advantage that it prevents moisture from penetrating between the surfaces.

A number of different companies offer heatsinking compound, these usually consist of silicon grease loaded with some electrically insulating, good thermally conducting material such as alumina. Thinly applied, these compounds are advantageous as they fill the air gaps and do not further increase the distances between the surfaces. Thickly applied they can hold the two surfaces apart and increase the contact thermal resistance. The following graph displayed in Figure 1.4 shows the contact thermal resistance for ‘dry’ conditions (no compound) and the thermal resistance using compound, both are plotted against contact force.

The metal heatspreader on the back of the SUPER-247 package is non-electrically isolated from the pinouts of the device within, *i.e. in the case of a MOSFET the heatspreader is the drain contact, for an IGBT the collector*. Hence in cases where devices are not electrically paralleled but share the same heatsink, it is necessary to insert an electrically isolating material between the package and the heatsink block. The isolator usually takes the form of a pad and many companies offer a range of pad material types and sizes dependant on requirements.

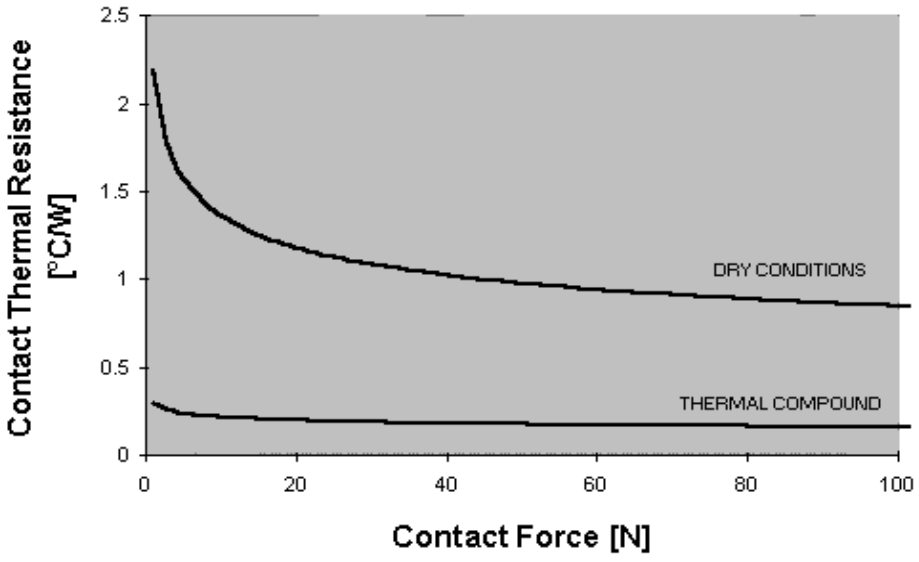


Figure 1.4 - Contact Thermal Resistance for 'Dry' and Compound Conditions, Plotted Against Contact Force.

At the minimum stated contact force of 20 N the following contact resistances can be achieved:

Contact Conditions	$Rth_{(c-s)}$ @ 20N Contact Force
'Dry' (no compound)	1.2°C/W
Thermal Compound	0.2°C/W

The pad obviously has a direct and detrimental effect on the contact resistance as insertion adds an extra resistance into the build-up. Again, the contact thermal resistance is dependant on contact pressure. The following graph, shown in Figure 1.5, illustrates the higher thermal resistance when using an isolator pad, adding a new line to the thermal resistance curve. The isolator used to plot the line was a typical silicone loaded pad. Therefore, it should be noted that when electrically isolating a device from a heatsink the thermal resistance of the system will increase.

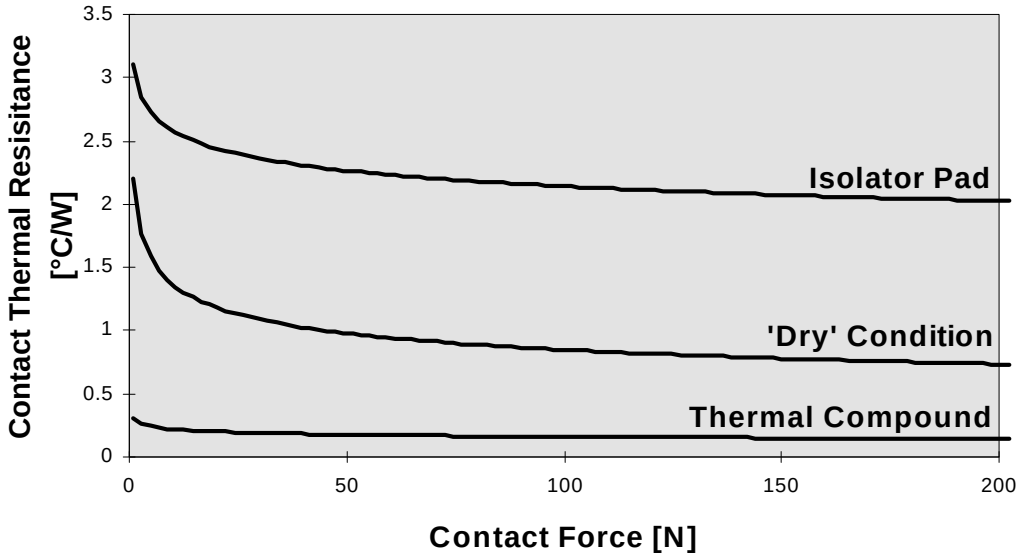


Figure 1.5 - Contact Thermal Resistance Plotted Against Contact Force

4. Typical Clips and What They Do

Why Clips?

The use of clips for providing the contact pressure is quickly becoming popular. Clip mounting provides a number of advantages over the more traditional screw mounting techniques:

- **Clips provide a more uniform pressure** over the entirety of the mating surfaces. Although screw mounting can provide a higher pressure, the force is centred at one end of the package and there is often a loss of coplanarity between package and heatsink.
- **Clips are faster to apply** than aligning and tightening screws.
- **Clips regulate the force applied** and ensure that the same force is applied to each package/heatsink pair. Hence there is no danger of over-tightening (deforming the package and/or heatsink) or under-tightening (increasing the contact thermal resistance).

Clip Types

There are a number of different clip types available on the market that can be used dependant on the application. Following are some examples of clips and the way in which they are typically used. The ideas shown by no mean encompass all the solutions available and do not prescribe the only ways in which the clips can be used.

Saddle Clips

An example of a SUPER-247 mounted to a heatsink using a saddle clip is shown in Figure 1.6.

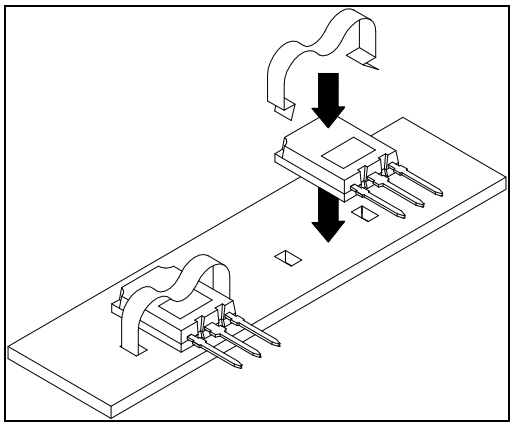


Figure 1.6 - SUPER-247 Mounted to Heatsink Using Saddle Clip

When using saddle clip type solutions, the heatsink materials are thin in cross-section, typically less than 5mm in thickness. The clips push into holes cut into heatsink material and lock against the back face of the heatsink. These clips produce contact forces in the range 20-60N.

‘U’ Clips

An example of a ‘U’ Clip assembly is shown in Figure 1.7.

This clip type clamps the device and the heatsink material together. Variations on this clip type allow devices to be clamped to the front and back of the heatsink block using the same clip. ‘U’ clips typically impart forces in the 20N-40N range. This force is partly dependent of the thickness of the heatsink material, *i.e. thicker the material, the greater the force*.

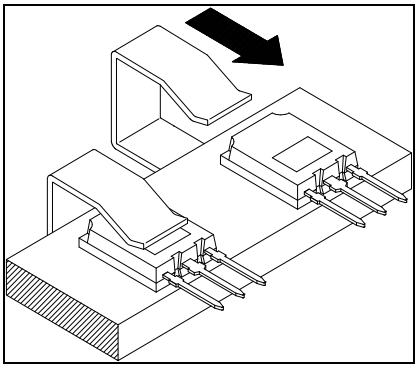


Figure 1.7 - ‘U’ Clip Assembly

Extrusion Mounted Clips

There are a number of proprietary clip solutions offered where the clip is anchored in a feature in the extruded heatsink. Figure 1.8 shows one solution type where the clip fits into a shaped slot in the heatsink material.

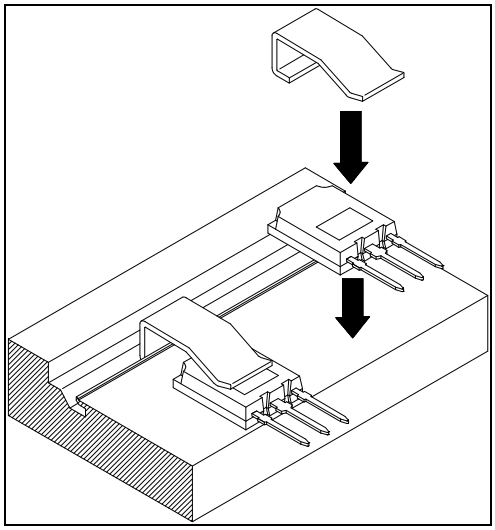


Figure 1.8 - Extrusion Mounted Clip (Slot Anchorage)

This solution can produce contact forces in the range 15 - 25N. However the shaped slot is an expensive addition to the heatsink and this solution type is being replaced in favour of clips mounted between shortened heatsink fins or clip rails (as shown in Figure 1.9 below). The extruded heatsinks are less costly and the forces that can be applied are higher, typically in the range 25 - 50N

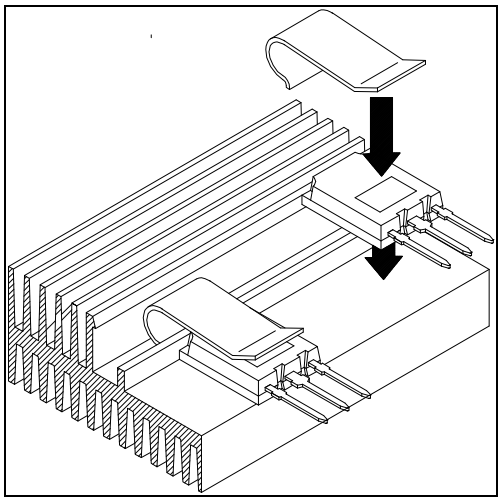


Figure 1.9 - Extrusion Mounted Clip (Rail Anchorage)

Other Solutions

Heatsink manufacturers offer a wide range of heatsink types, usually extrusions or formed metal and at a cost are willing to produce customised solutions. Some manufacturers will supply the heatsink with integrated clip both in extruded and formed metal varieties or a combination of the two. It is also possible to have heatsink solutions supplied with thermal compound or isolator materials already applied in the correct places to aid assembly.

Sources for Clip Solutions

The following are companies who can supply the types of clips/solutions discussed in this Application Note:

Redpoint Thermalloy,
Cheney Manor,
Swindown,
Wiltshire.
SN2 2QN

Avvid Thermal Technologies,
Corporate Headquarters,
One Kool Path,
Laconia,
New Hampshire
USA

Austerlitz Electronic gmbh,
Ludwig Feuerbach -Straβe 38,
90961 Nüenburg, Postfach 1048,
GERMANY

Relevance to TO-247 Heatsink Mounting

The clipping/mounting concepts covered in this application note for the SUPER-247 can also be applied to the standard TO-247 package. However, it should be noted that due to the screw mounting capability of the standard TO-247 the package to heatsink contact area is reduced and hence the contact thermal resistance is **INCREASED** from 0.2°C/W(SUPER-247) to 0.24°C/W(TO-247). Therefore, whilst the minimum clamping force of 20N still applies, the contact thermal resistance graph for the SUPER-247 will not.

Conclusion

The SUPER-247 package can now dissipate more power and encapsulate more silicon than the industry standard TO-247, a package with the same footprint. It also allows for faster and less costly clip mounting to heatsinks. However, the way in which the device is mounted to the heatsink will affect the thermal performance of the system (silicon, package and heatsink). The designer can have a direct affect on the contact thermal resistance and the design parameters that he sets can have either a positive or adverse effect on system performance. This Application Note has discussed the need for an adequate force (20N) for good thermal contact and the fact that intermediate materials also affect the thermal resistance. Thinly applied thermal compound will improve the contact thermal resistance whilst electrical isolators are likely to cause deterioration in this parameter.

There are many clip/heatsink solutions available and some have been indicated in this Application Note. The chosen solution will depend on the application in which it is used and should be chosen to optimise both cost and thermal performance characteristics.

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APPLICATION NOTES

PUBLISHED BY INTERNATIONAL RECTIFIER, 233 KANSAS STREET, EL SEGUNDO, CA 90245, (310) 322-3331

AN-993

Utilizing HEXFRED® Ultra-Fast Recovery Diode Die In Assembly

(HEXFRED is a trademark of International Rectifier)

by Keith Weinrich

Introduction

This application note describes the HEXFRED® Ultra-Fast Recovery Epitaxial Diode available from International Rectifier in die and wafer form. These epitaxial diode die feature a proprietary, high reliability planar technology utilizing a guard ring structure for maximized ruggedness. Hybrid packaging of these die results in substantial savings in weight and volume compared to standard packaging, as well as significant improvements in electrical performance, particularly lead inductance. Most of the same parts are available in finished packages; thus, development work and evaluation can be easily performed before converting the design for die application. A cross reference of packaged product to die part numbers is included in this application note. HEXFRED die sizes presently available from International Rectifier are summarized in Table 1. Sizes less than or equal to 1.68 millimeters (0.066 inches) square are available in wafer form while all others are available in both wafer and die forms.

Probing

Because of limitations when electrical probing in die form, some of the specifications of equivalent packaged devices cannot be tested or guaranteed in die form. Typically, these are high current forward characteristics and t_{rr}, high temperature characteristics, surge capability (I_{FSM}), thermal resistance (R_{thJC})and series inductance (L_S). However, each wafer is 100% probed at room temperature for maximum reverse voltage (V_R), maximum reverse leakage current (I_R), and low current forward voltage drop (V_F).

During electrical probing, the rejected die are inked for identification. The wafer is then cut and the die mechanically separated. The rejected die are discarded and the remaining die are 100% visually inspected, loaded into waffle pack trays, and packed for shipment.

Handling and Shipping

HEXFRED die from International Rectifier are classified as non-static sensitive devices but are packaged in conductive trays for convenience. The chip tray capacities for each die size are shown in Table 1. These trays are then sealed in electrostatic shielding bags for shipment. Wafers are shipped in non-conductive, polyethylene wafer carriers.

Once opened, the die must be stored in a dry, inert atmosphere, such as nitrogen, prior to assembly. Die should be handled with DuPont Teflon®-tipped vacuum pencils to prevent mechanical damage. Any non-conformance to the electrical or visual inspection specifications in this application note must be reported in writing to International Rectifier within 30 days after shipment of the lot. International Rectifier assumes no responsibilities for die which have been subjected to further processing, such as mount-down, wire-bonding, or encapsulation. In the interest of product improvement, International Rectifier reserves the right to make design or processing changes without prior notice.

Visual Inspection of Die

International Rectifier HEXFRED die are designed to meet the visual inspection criteria of Mil-Standard 750, Method 2072, and are visually screened to a 0.04% AQL level.

Mounting Backside (Cathode) of Die

The HEXFRED die have a aluminum/titanium/nickel/silver cathode metallization which is suitable for either solder paste or solder preform mounting using solders such as 92.5%/5%/2.5% Pb/In/Ag solder. It is recommended that solders containing silver are used due to silver dissolution of the backside metal in the absence of silver in the solder.

Any of the commonly used header or substrate materials, such as copper and copper-plated beryllia or alumina, are acceptable. The substrate must be free of oxides prior to assembly either by chemical cleaning or hydrogen pre-firing techniques. Mounting of HEXFRED die is generally accomplished in a profiled belt furnace or by using a hotplate reflow technique. Infrared or vapor phase reflow are also acceptable methods for die mounting. If using solder paste, cleaning must always be performed afterwards.

The furnace zone settings will depend upon hybrid mass, material, fixturing, and belt speed. HEXFRED die characteristics are sensitive to maximum temperatures during the die attach process. The maximum temperature and duration above 300°C is critical for its performance. The suggested profile is 345°C (+15°, -5°C) peak with the duration above 300°C to be no more than 7.0 minutes (+/-0.5). See Profile 1 and 2 for typical profiles of the die and furnace ambient temperatures during die attach. Trade-offs of higher temperatures are 1) decreasing the V_F and I_R and 2) increasing the t_{rr}, I_{RRM}, and Q_{rr}. A clean furnace of hydrogen atmosphere is recommended, although an atmosphere of nitrogen or forming gas (nitrogen-hydrogen, 85%-15%) is acceptable.

It is also possible to mount the die using conductive adhesives, although this is not currently used in production at International Rectifier.

Molybdenum Tabs

In solder applications, due to thermal expansion stresses exerted on the larger die sizes (200 mil/side and greater), International Rectifier recommends the use of molybdenum or other thermally matched tabs on the anode and cathode. The selection of tab material and/or plating must be such that it can be soldered to the silver metallization of the top and bottom metals.

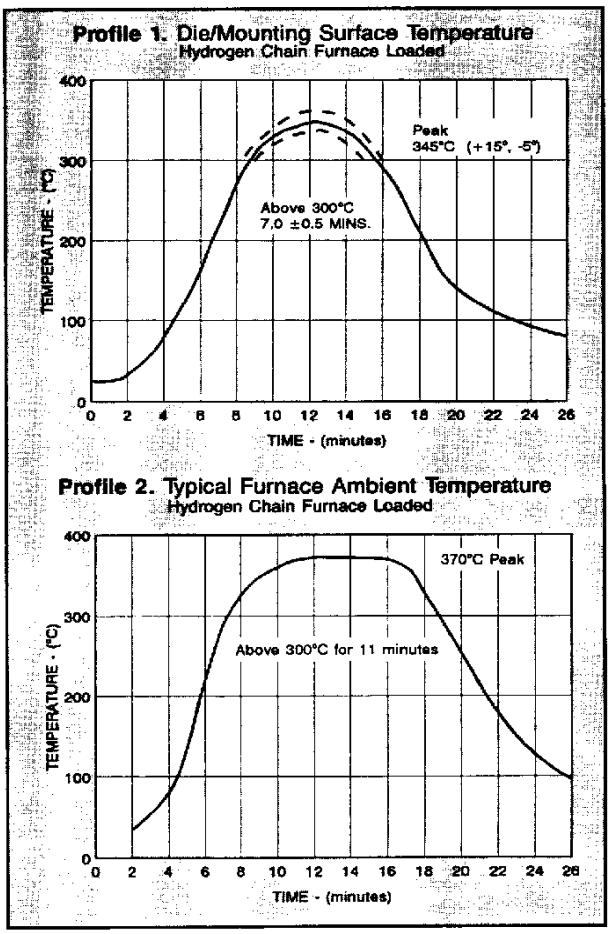
Anode Connection

Electrical connection to the anode should be a solder connection for all devices with silver top metallization. For all parts with aluminum top metallization, electrical connection to the anode is by ultrasonic bonding with aluminum wire. The wire diameter and number of wires should be chosen to suit the current requirements. For enhanced reliability, all copper piece parts that come into contact with the anode metallization must be nickel-clad or nickel-plated to eliminate copper contact with the anode.

Caution must be exercised during wire bonding to ensure that the bonding footprint remains within the bonding pad area; otherwise, device failure can result. The bonding pad area is centered on the die and the outside edges of the die are not part of the bonding area so neither solder, in the case of silver metallization, nor wire, in the case of aluminum metallization, may make contact with the perimeter or oxide passivation. The bonding pad area is different for each die size and the dimensions of each are listed in Table 1.

Likewise, wire bonding equipment settings should be optimized and a wire pull test performed (e.g., see Method 2037, Mil Standard 750) to monitor wire bond strength

Note: Teflon is a trademark of DuPont.



uniformity. Destructive sample testing and 100% non-destructive testing is recommended. Re-bonding of wire bond rejects can be performed although decreased yield can be expected from such reworks.

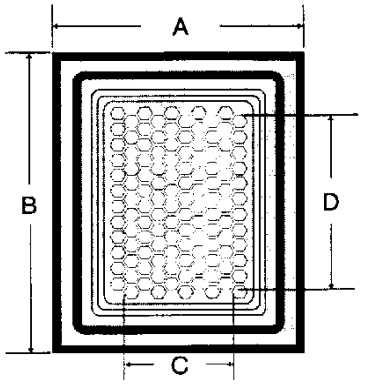
Encapsulation

Prior to encapsulation, the die or assembly should be kept in a moisture-free environment. For non-hermetic packaging, a semiconductor grade silicone elastomer may be applied. Cleaning of the die or assembly prior to coating is recommended. Immediately prior to encapsulation, especially for hermetic packages, a 150°C, two-hour bake should be performed to remove any surface moisture. Capping of hermetic packages should be performed in a dry-nitrogen atmosphere.

Conclusion

The use of HEXFRED die for hybrid assemblies can result in significant reduction in overall package size and significant improvements in performance and efficiency. In addition, several HEXFRED die can readily be mounted on the same heatsink to form circuit configurations or to parallel devices. The operational advantages of International Rectifier HEXFRED Ultra-Fast Recovery Epitaxial Diodes, thereby, can be realized in very compact, custom package configurations. □

FIGURE 1. HEXFRED Die Outline (shaded area simulates the passivation).



NOTES:
1) All dimensions correspond to TABLE 1.
2) Dimensions are referenced from die center.
3) Die thickness is (0.0145) 0.3683 +/–(0.0005) 0.0127
4) Die length and width tolerance is +/–(0.003) 0.0762

TABLE 1. HEXFRED Die

Wafer (1) Part Number	Die (2) Part Number	Die Size	Die "A x B" Length/Side (in.)mm	Bond Pad "C x D" (in.)mm	Anode Metallization (topside)	Tray Quantity
HFAW06-60A	N/A	06	(0.066x0.066) 1.68x1.68	(0.037x0.037) 0.94x0.94	Aluminum	N/A
HFAW06-60S	N/A	06	(0.066x0.066) 1.68x1.68	(0.037x0.037) 0.94x0.94	Silver	N/A
HFAW10-60A	HFAC10-60A	10	(0.090x0.090) 2.29x2.29	(0.062x0.062) 1.58x1.58	Aluminum	196
HFAW10-60S	HFAC10-60S	10	(0.090x0.090) 2.29x2.29	(0.062x0.062) 1.58x1.58	Silver	196
HFAW20-60A	HFAC20-60A	20	(0.107x0.130) 2.72x3.30	(0.056x0.080) 1.42x2.03	Aluminum	100
HFAW30-60A	HFAC30-60A	30	(0.115x0.155) 2.92x3.94	(0.064x0.104) 1.63x2.64	Aluminum	100
HFAW40-60A	HFAC40-60A	40	(0.169x0.220) 4.29x5.59	(0.117x0.169) 2.97x4.29	Aluminum	35
HFAW40-120A	HFAC40-120A	40	(0.169x0.220) 4.29x5.59	(0.112x0.163) 2.85x4.14	Aluminum	35
HFAW42-40A	HFAC42-40A	42	(0.200x0.200) 5.08x5.08	(0.170x0.170) 4.32x4.32	Silver	49
HFAW42-40S	HFAC42-40S	42	(0.200x0.200) 5.08x5.08	(0.180x0.180) 4.57x4.57	Aluminum	49

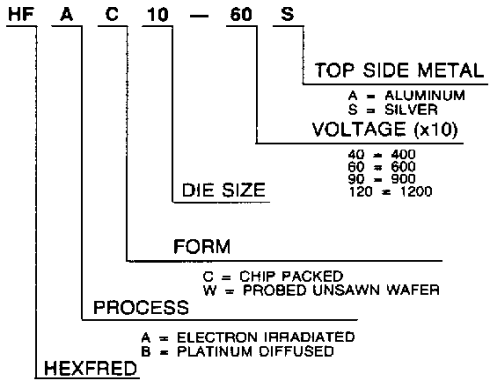
(1) Die in probed un-cut, wafer form
(2) Die in probed waffle pack form

TABLE 2. HEXFRED Die

Die Number	Wafer Probe Limits			Cross Reference Part Number (1)
	V_{RRM} 100μA min. (V)	I_R @ V_{RRM} max. (μA)	V_{FM} @ 1.0A max. (V)	
HFAC06-60A	600	5	1.3	HFA04TB60 HFA08TA60C
HFAC06-60S	600	5	1.3	HFA04AC60
HFAC10-60A	600	5	1.1	HFA08TB60 HFA16TB60C
HFAC10-60S	600	5	1.1	HFA06AD60
HFAC20-60A	600	10	1.1	HFA08SD60
HFAC30-60A	600	10	1.1	HFA15TB60 HFA30TA60C
HFAC40-60A	600	20	0.85	HFA25TB60
HFAC40-120A	1200	20	1.2	HFA20TB120
HFAC42-40A	400	20	0.85	NA
HFAC42-40S	400	20	0.85	NA

(1) Cross reference to packaged devices for general information only.

Chart 1. Nomenclature Code for HEXFRED Die



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Application Characterization of IGBTs

(HEXFRED® is a trademark of International Rectifier)

Topics Covered:

Gate drive for IGBTs
Safe Operating Area
Conduction losses
Statistical models
Switching losses
Device selection and optimization
Spreadsheets to calculate power losses and junction temperature
Thermal design
How to replace a power MOSFET
Paralleling
How to select devices for paralleling
Curve fitting methods to derive model parameters

SCOPE:

This application note covers some of the major issues normally encountered in the design of an IGBT power conditioning circuit. It is the companion to INT-983, "IGBT Characteristics," which covers the details of the device, rather than its application.

I. GATE DRIVE REQUIREMENTS

A . Impact of the impedance of the gate drive circuit on switching losses

The gate drive circuit controls directly the MOSFET channel of the IGBT and, through the drain current of the MOSFET, the base current of its bipolar portion. Since the turn-on characteristics of an IGBT are determined, to a large extent, by its MOSFET portion, the turn-on losses will be significantly affected by the gate drive impedance. Turn-off characteristics, on the other hand, are chiefly determined by the minority carrier recombination mechanism, which is only indirectly affected by the MOSFET turn-off. An increase in gate drive impedance prolongs the Miller effect and causes a delay in the current fall time that is similar to a storage time. This delay is emphasized in Figure 1 with the addition of a 47W gate resistor. The impact of the gate drive impedance on total switching losses depends on the basic design of the IGBT and its speed. The impact on *turn-on losses* is appreciable for all IGBTs from International Rectifier, regardless of speed. The impact on *turn-off* losses depends on the speed of the device: the faster the IGBT the greater its sensitivity to the gate drive impedance. In any event, *additional* gate drive impedance has a *marginal* impact, i.e. the same amount of additional drive impedance will have a lower effect if the gate drive impedance is already high.

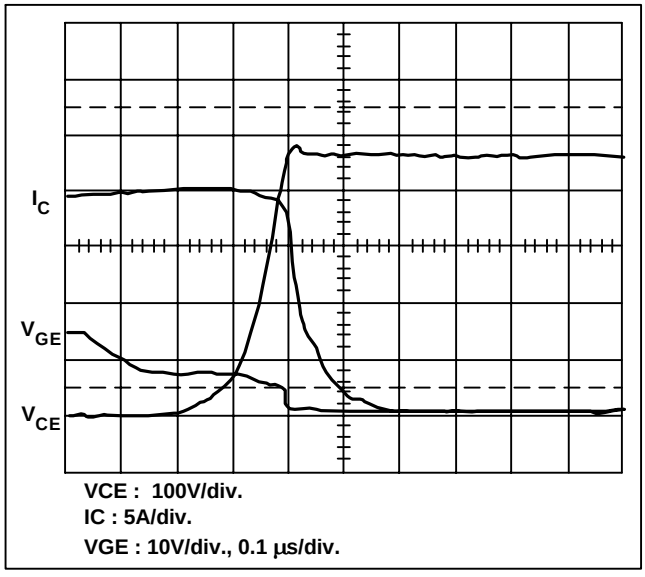


Figure 1. Turn-off waveform of an IRGBC40F with a 47W gate resistor. Notice the turn-off delay of the current waveform during the Miller effect.

It follows that the *total switching losses* of Fast IGBT will be less affected by the characteristics of the gate drive circuit than the Ultrafast IGBTs. These last ones are more sensitive to it and stand to benefit the most from a low impedance gate drive. The specific dependence of the switching energy on gate drive resistance is shown in the data sheet.

B. Impact of the gate drive impedance on noise sensitivity

As explained in INT-936, in a MOS Gated transistor, any dv/dt that appears on the collector/drain is coupled to the gate through a capacitive divider consisting of the Miller capacitance and the gate-to-source/emitter capacitance. If the gate is not solidly clamped to the source/emitter, a large enough dv/dt will take the gate voltage beyond its threshold and the transistor will conduct. As it goes into conduction it clamps the dv/dt that is causing it to conduct so that the gate voltage never goes much beyond its threshold. The end result is a limited amount of "shoot-through" current, with an increase in power dissipation. To reduce noise sensitivity and the risk of this dv/dt-induced turn-on, the gate must be shorted to the emitter through a very low impedance. Frequently a negative gate bias is used to improve noise immunity. An effective alternative is to design a layout that minimizes the inductance of the gate charge/discharge loops with parallel tracks or twisted wires for the gate drive.

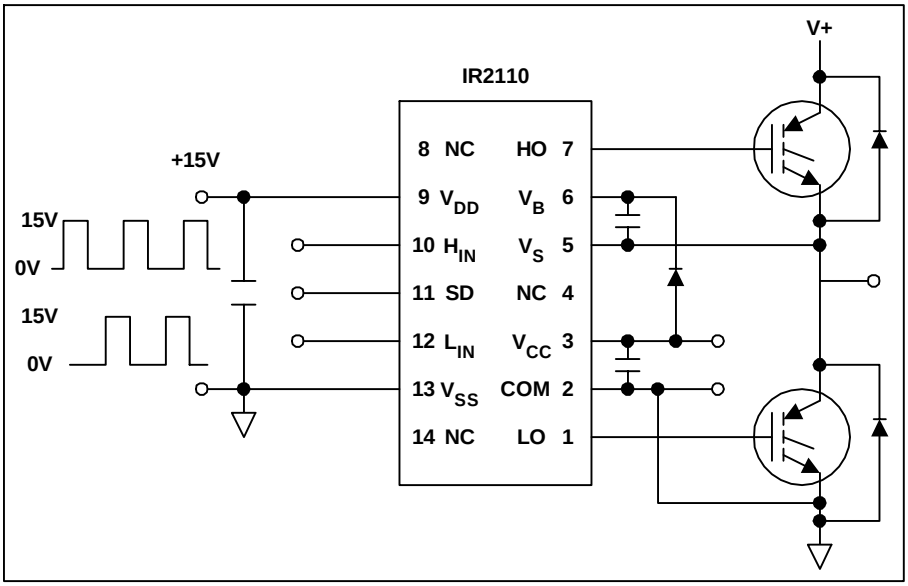


Figure 2. The IR2110 provides a simple, high performance, low cost solution to the problem of driving a Half-Bridge.

This can be as effective in taking care of this problem as the negative bias, eliminating the need for isolated negative supplies. In many cases the effects of a contained amount of dv/dt induced turn-on, i.e. a small increase in power dissipation, can be an appealing alternative to the added complexity of the negative gate bias.

C. Impact of gate drive impedance on "dynamic latching"

Some manufacturers suggest the use of significant amounts of gate resistance to reduce the possibility of "dynamic latch-up" (see INT-983, Section I.d), particularly when short circuit currents have to be switched off. This increases the switching energy and the sensitivity to dv/dt induced turn-on. Under these conditions a negative gate bias may be required.

Although IGBTs from International Rectifier will not latch even with no gate resistance, there may be practical reasons to add them, mainly to reduce the current spike at turn-on due to reverse recovery of the diode and reduce ringing.

This resistance can be safely bypassed with an anti-parallel diode to reduce the turn-off losses and the amount of dv/dt induced turn-on, as explained in INT-978, Section 3.b. For most applications, the circuit shown in Figure 2 provides a simple, low cost, high performance solution to the gate drive requirements of most applications.

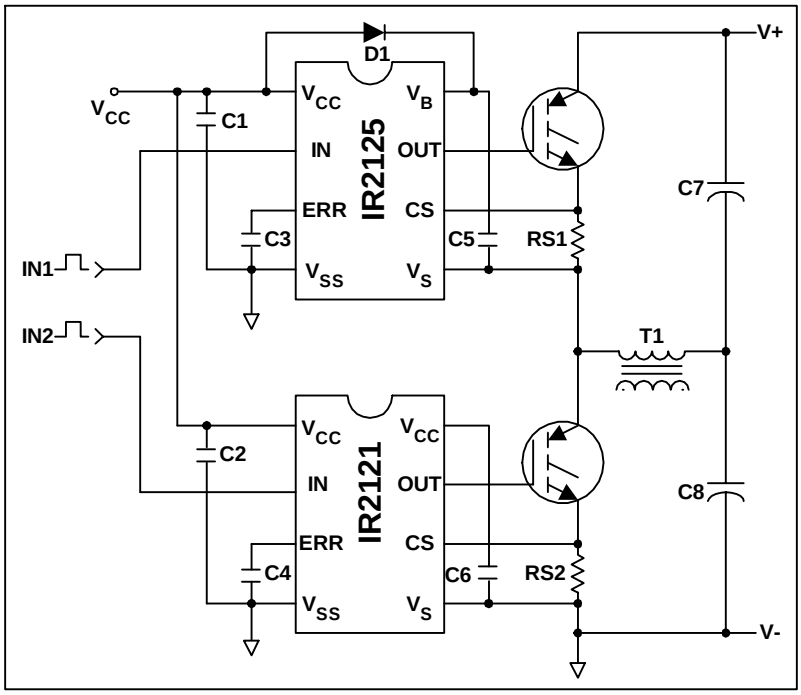


Figure 3. Short circuit protection performed with MOS gate driver ICs

D. Using gate voltage to improve short circuit capability

The gate terminal can be advantageously used to control the short-circuit withstand capability of the IGBT. A lower gate drive voltage reduces the collector current and the power dissipation during short circuit, at the expenses of a higher conduction drop. As an alternative, simple circuits can be implemented to reduce the gate voltage within 1-3 ms from the inception of the short circuit. INT-984 provides an example of how this function can be performed.

MOS-Gate Driver integrated circuits are available to perform the current limiting and short circuit protection function by means of the gate voltage. One such example is shown in Figure 3.

E. Contribution of "common emitter inductance" to the impedance of the gate drive circuit

The "common emitter inductance" is the inductance that is common to the collector circuit and the gate circuit (Figure 4a). This inductance establishes a feedback from the collector circuit to the gate circuit that is proportional to Ldi_C/dt. The voltage developed across this inductance subtracts from the applied gate voltage during the turn-on transient and adds to it during turn-off. In so doing, it slows down the switching.

This phenomenon is similar to the Miller effect, except that it is proportional to the di/dt of the collector current rather than the dv/dt of its voltage. In both cases the feedback is proportional to the transconductance of the IGBT, which is much larger than that of a MOSFET of the same die size. A di_C/dt of 0.5A/ns is quite common in IGBT circuits and voltages in the order of 10V could be expected in 20 nH of common emitter inductance, except that the feedback mechanism slows down the turn-on process and limits the dic/dt.

No additional common emitter inductance should be added to what is already in the package. Separate wires to the emitter pin should be provided for the emitter and the gate return, as shown in Figure 4b. The gate lead and the gate return lead should be twisted or run on parallel tracks to minimize inductance in the gate drive path. This improves immunity to dv/dt induced turn-on and reduces ringing in the gate.

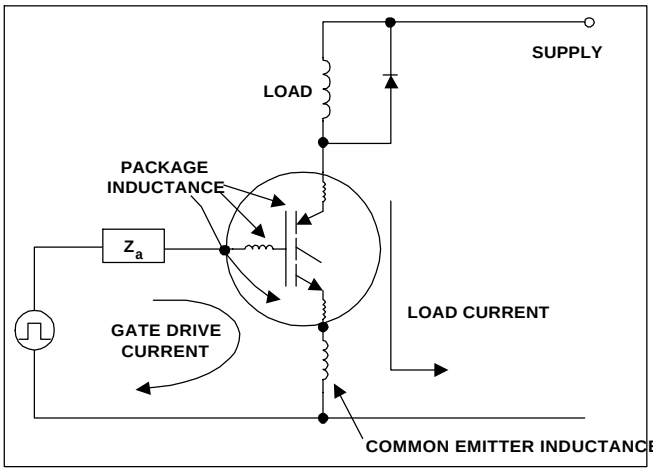


Figure 4a. " Common Emitter Inductance" is the inductance that is common to the collector current and the gate drive current

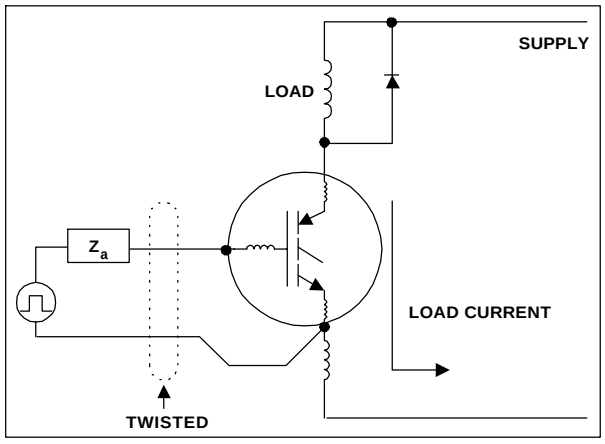


Figure 4b. " Common Emitter Inductance" can be eliminated by running separate wires to the emitter pin, one for the emitter, the other for the gate drive return.

F. Gate charge vs. input capacitance

The difference between gate capacitance and gate charge is covered in INT-944. Designers that are familiar with the limited usefulness of the input capacitance concept can safely skip this section.

Input capacitance is frequently used for two purposes:

- as a figure of merit of switching performance;
- as a reference point to design a gate drive circuit.

On both counts, the use of data sheet capacitance values gives results that are wrong or misleading.

As shown in Figure 5, IGBT capacitances change significantly with collector voltage to the point that no capacitance number is, in itself, meaningful unless a voltage is associated with it.

Even disregarding the voltage dependence, input capacitance is not a good figure of merit of switching performance, neither for MOSFETs, nor for IGBTs. As far as MOSFETs go, a device with lower input capacitance can be slower than one with higher input capacitance, depending on threshold, transconductance and total gate charge (see Figure 6 of INT-944). A conspicuous example of this is the fact that logic level devices are faster than their standard gate counterparts, in spite of a larger input capacitance [1].

In the specific case of IGBTs, which are minority carrier devices, the switching behavior is dominated by injection and recombination phenomena and only the turn-on behavior is affected by gate drive conditions in a significant way.

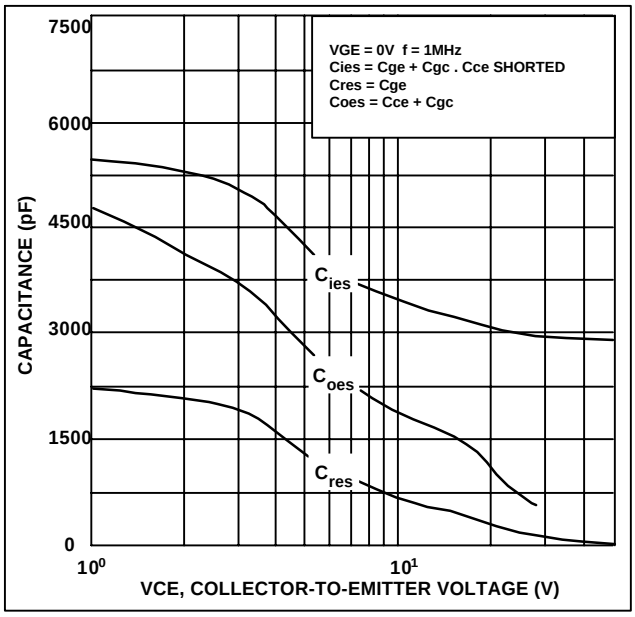


Figure 5. Typical capacitance vs VCE, IRGPC50U. The variation of Cres and Cies with collector voltage makes the concept of capacitance virtually useless.

As a guideline to design the gate drive circuit, the input capacitance underestimates the gate drive requirements. Normally, the charge required by the gate for one switching operation corresponds to an input capacitance that is two to three times larger than the data sheet value. As explained in INT-944, this is due to the Miller component of the input capacitance.

Thus, gate drive circuits designed on the basis of input capacitance are generally inadequate and result in poor switching operation and noise susceptibility. The sizing of the gate drive circuit is more appropriately done using the gate charge specified in the data sheet.

II. SWITCHING TRAJECTORIES AND SAFE OPERATING AREA CONSIDERATIONS

Minority carrier devices, when subjected to high levels of voltage and current, can experience uneven current distributions within the die that, taken beyond safe limits, can cause device failure. The current distribution takes different forms, depending on the sign of the di/dt associated with it. Hence, the Safe Operating Area curve, which was devised as a convenient representation of this limitation, is frequently differentiated into "Forward Biased SOA" and "Reverse-Biased SOA".

The Forward Biased SOA curve applies to linear operation in Class A or Class B or during short circuit, which can be considered an extreme case of Class B operation. Thermal limitations for pulsed operation are frequently included in this curve, even though the Transient Thermal Response curve provides this same information in a more comprehensive and accurate way. Due to the limited use of these devices in linear operation, the FBSOA curve has been omitted from the data sheet. The Reverse Biased SOA applies when switching off a clamped inductive load, including the turn-off from a short circuit condition.

Figure 6 shows the importance of the Reverse Biased SOA. During the turn off of a clamped inductive load, the voltage across the transistor goes from the low value of $V_{CE(sat)}$ to the full supply voltage while the collector current stays constant. After the collector voltage exceeds the supply voltage by a diode drop, the diode starts to conduct, thereby taking over the inductor current from the transistor. Thus the trajectory of the operating point moves along a constant current line until it intercepts the supply voltage, at which point a voltage overshoot normally occurs, whose magnitude depends on the amount of stray inductance L_S and the turn-off speed. A more detailed explanation of the switching trajectories can be found in Ref. [2].

It will be appreciated that, for a safe commutation of the load current, the entire trajectory must lay within the turn-off SOA and that any limitation to the SOA will translate into a limitation of turn-off capability of inductive loads. Load-shaping snubbers have been used in conjunction with bipolar transistors to lower the trajectory below the second breakdown limit.

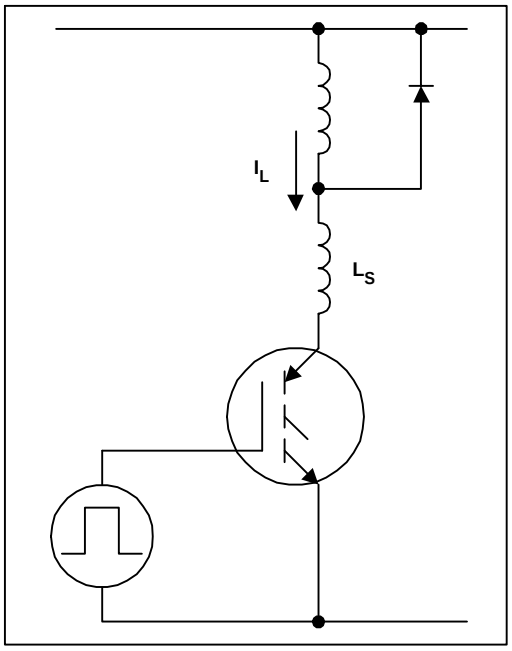


Figure 6a. Typical clamped inductive load

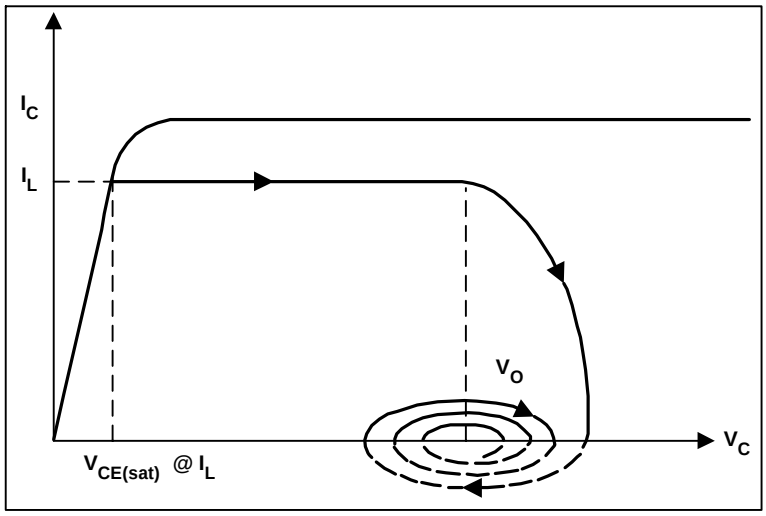


Figure 6b. During a turn-off transient, the trajectory of the operating point traverses the SOA curve. Second breakdown would place limits to the free evolution of the trajectory.

Due to the wide base and, hence, low gain of its bipolar portion, the second breakdown of International Rectifier's IGBTs occur at current and voltage levels that are significantly higher than what is normally encountered in a practical application, as shown in the data sheets. Notice that the values therein contained apply at 125°C and that load-shaping snubbers are not necessary, as long as the switching trajectory is confined within the turn-off SOA. During an inductive turn-off, a bipolar-mode device can undergo a partial loss of blocking capability, similar in many respects to second breakdown. This phenomenon is generally explained as being due to excessive concentration of minority carriers in the base region [3], rather than lateral thermal instability. For the IGBTs available from International Rectifier at the time of writing, this phenomenon occurs well beyond the SOA limits published in the data sheet. In addition to load shaping, snubbers can be used to limit overshoots and/or reduce EMI. This function is not related to SOA and is covered in more detail in INT-936.

III. CONDUCTION LOSSES

At any given time, the energy dissipated in the IGBT can be obtained with the following expression:

$$E = \int_0^t V_{CE}(i)i(t)\,dt$$

where t is the length of the pulse. Power is obtained by multiplying energy by frequency, if applicable. When the transistor is off i(t) » 0 and losses are negligible. Unfortunately, no simple expression can be found for the voltage and current functions during a switching transient. Hence, for analytical expediency, we resort to a somewhat artificial distinction between conduction and switching losses.

We define conduction losses the losses that occur between the end of the turn-on interval and the beginning of the turn-off interval, as defined for the switching losses characterization. Since the turn-on energy is measured from 5% of the test current to 5% of the test voltage and the turn-off energy is measured starting from 5% of the test voltage, conduction losses occur when the voltage across the IGBT is less than 5% of the test, or supply, voltage (see INT-983, Section 8.5). The function $V_{CE}(i)$ in the formula above expresses the conduction behavior of the IGBT. International Rectifier characterizes the conduction losses in the following ways:

- with tabular information in the data sheet;
- with graphs in the data sheet;
- with the model Parameters of INT-MODEL.

A. Calculating the voltage drop from data sheet parameters

The tabular information in the data sheet provides a few limit points that, with the help of the graphs, can be used to generate the information necessary to calculate the conduction losses. To obtain the max voltage drop at any current and temperature, from the data sheet supplied values, a two step procedure can be followed. First a typical value is obtained by interpolating a curve in Figure 5 of the data sheet at the desired current level. Then, to obtain a maximum value, the voltage drop read from this curve at the appropriate junction temperature is multiplied by the ratio between maximum and typical from the Table of Electrical Characteristics. If the current waveform is not constant during the conduction interval, it should be broken up into smaller intervals, calculating the losses for each sub-interval and summing the results, rather than averaging or taking its RMS value. An appealing alternative, for those cases where the current waveform has a simple mathematical expression, e.g. sinusoidal or triangular or trapezoidal, is to calculate the conduction losses with the integral above, with the help of the conduction model.

B. Conduction model

The solution of the integral requires a mathematical expression for the current waveform and one for the voltage drop. The expression shown below for the voltage drop as a function of current was found to be more than satisfactory for the general accuracy that is expected from these calculations.

$$V_{CB} = V_t + a\, I^b$$

Information on the accuracy of the model and how it was derived is contained in Appendix 1.
The specific parameters for the families of IGBTs from International Rectifier can be found in INT-MODEL. The purpose of this model, as well as the one presented in Section IV.B is to accurately predict the junction temperature of the IGBT in order to get the most out of the device. They differ from the common SPICE model in significant ways:

- they are representative of a population of devices, characterized by averages and sigmas, rather than an *undefined* "typical" device;
- they model electrical magnitudes that are time-independent, hence increments, and convergence are not an issue;
- temperature is an integral part of the model, not an after thought;
- the models are integrateable to calculate averages or losses in complex modulation schemes;
- the model is suited to provide aggregate values, like average power, average temperature, average peak reverse recovery.

These models do not provide information on the details of collector or gate waveforms. It should be kept in mind, however, that these waveforms are determined by circuit parasitics that cannot be modeled without breadboard characterization.

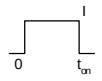
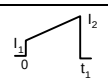
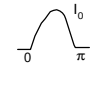
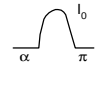
CURRENT WAVEFORM	MATHEMATICAL EXPRESSION	$E = \int V_{CE}(i)\, i(t)\, dt,\ V_{CE}(i) = V_t + a i^b \quad E = \int \left[V_t i(t) + a i(t)^{(b+1)} \right] dt$
	$i(t) = I$	$E = \int_0^{t_{on}} \left(IV_t + aI^{(b+1)} \right) dt = \left(IV_t + aI^{(b+1)} \right) t_{on}$
	$i(t) = I_1 + (I_2 - I_1)\frac{t}{t_1}$	$E = \int_0^{t_1} \left[V_T \left(I_1 + \frac{(I_2 - I_1)}{t_1} \right) + a \left(I_1 + \frac{(I_2 - I_1)}{t_1} t \right)^{(b+1)} dt = V_t \frac{(I_2 + I_1)}{2} t_1 + \frac{I_2^{(b+2)} - I_1^{(b+2)}}{(I_2 - I_1)} \frac{at_1}{b+2} \right.$
	$i(t) = I \frac{t}{t_1}$	$E = \int_0^{t_1} \left(V_t I_0 \sin \omega t + a I_0^{(b+1)} \sin^{(b+1)} \omega t \right) dt = \frac{2I_0}{\omega} \left[V_t + \frac{\sqrt{\pi}}{2} a I_0^b \frac{\Gamma\left(\frac{b+2}{2}\right)}{\Gamma\left(\frac{b+3}{2}\right)} \right]$
	$i(t) = I_0 \sin \omega t$	$E = \int_0^{t_1} \left(V_t I_0 \sin \omega t + a I_0^{(b+1)} \sin^{(b+1)} \omega t \right) dt = \frac{2I_0}{\omega} \left[V_t + \frac{\sqrt{\pi}}{2} a I_0^b \frac{\Gamma\left(\frac{b+2}{2}\right)}{\Gamma\left(\frac{b+3}{2}\right)} \right]$
	$i(t) = I_0 \sin \omega t$	for $\alpha \frac{\pi}{2}$ $E = \frac{I_0}{\omega} \left[V_t + \frac{\sqrt{\pi}}{2} a I_0^b \frac{\Gamma\left(\frac{b+2}{2}\right)}{\Gamma\left(\frac{b+3}{2}\right)} \right]$ otherwise $E = \frac{I_0}{\omega} \left[V_t (1 + \cos \alpha) + a I_0^b \int_\alpha^\pi \sin^{(b+1)} \alpha\, d\alpha \right]$

Table I. Conduction Energy for Simple Waveforms

Table I shows the expressions to calculate conduction energy for five simple current waveforms, assuming that the conduction behavior is accurately expressed by the model presented.

As shown in Sections V and VI, this model, as well as the companion switching model that will be described in the next Section, is extremely useful in performing comparative evaluations for device optimization. Section VI shows how it can be used to simplify and automate the calculation of junction temperature for any operating condition.

IV. LOSSES IN HARD SWITCHING

Like conduction losses, "hard switching" operation is characterized in the following ways:

- with tabular information in the data sheet;
- with graphs in the data sheet;
- with the model parameters of Table INT-MODEL.

As explained in INT-983, Section 8.5, the Switching Energy reported in the data sheet makes specific reference to a test circuit that simulates a clamped inductive load operated with an ideal diode. Hence, it does not include the losses in the IGBT when, in turning on, it carries the full load current, plus the reverse recovery current of the freewheeling diode.

It follows that, to obtain the total turn-on losses or the total switching losses, two components have to be calculated:

- turn-on or total losses with an ideal diode
- the additional turn-on losses in the IGBT due to the reverse recovery of the freewheeling diode.

The following sections show how to calculate these two components. It should be kept in mind that active devices in flyback converters do not normally have turn-on losses, nor are they subject to recovery transients. The same is true for those bridge circuits where the output voltage and duty cycle is controlled by phase shifting the output of one leg with respect to the other, both being 50% duty cycle.

A. Calculation of switching losses with an ideal diode from data sheet information

Total switching losses with an ideal diode for any given current and temperature can be obtained from data sheet information following a three step procedure, similar to the one for obtaining the on-state voltage drop.

First a typical value is obtained, by interpolating a curve in Figure 10 of the data sheet for the desired current. From this typical value a maximum value can be obtained by multiplying the typical by the ratio between maximum and typical that is in the Table of Switching Characteristics.

Finally, since the switching energy is proportional to voltage, the result is scaled by the ratio of the actual circuit voltage to the test voltage (normally 80% of device rated voltage).

An additional correction may be necessary to account for the gate resistor. This can be done with the help of Figure 9 of the data sheet.

B. Calculation of switching losses with an ideal diode from switching model

A simpler alternative to the method outlined below is to make use of the simple model shown in Table III, together with the specific parameters for the three families of IGBTs from International Rectifier. Losses calculated with these parameters assume the following:

- supply voltages equal to 80% of rated $V_{(BR)CES}$.
- a gate drive circuit similar to the one in the data sheet.
- ideal diode.

The results should be scaled linearly for the appropriate supply voltage and should be scaled according to Figure 9 of the data sheet to take into account a different gate drive impedance.

C. Contribution of the diode reverse recovery

In a typical clamped inductive load in continuous current mode, the turn-on of a switch causes a reverse recovery in the freewheeling diode and a large current spike in the device that is being turned on (Figure 7). This increases the turn-on losses in the IGBT with respect to the calculations of the previous sections and data sheet characterization. The *forward recovery* of the diode, on the other hand, has a secondary impact on the turn-off losses and will not be analyzed here.

No simple expression can be provided for these additional losses, as they depend on a number of factors: turn-on speed di/dt, stray inductance and diode characteristics. Several have been proposed, based on simplifying assumptions. The following assumes that the voltage across the diode stays close to 0V during the length of t_a, rising to the supply voltage during t_b.

$$E = VI_L[(1+\frac{1}{2}\frac{I_{rr}}{I_L})t_a + \frac{1}{4}\frac{I_{rr}}{I_L}t_b]$$

$$= V(I_L t_a + Q_a + \frac{1}{2}Q_b)$$

where V and I_L are supply voltage and load current, I_{rr} is the peak reverse recovery current, t_a and t_b are the two components of t_{rr} and Q_a and Q_b the charges associated with them. The first two terms represent the losses during t_a, one due to the load current, the other due to the reverse recovery current. The third term represents the losses during t_b, which are partly in the IGBT, partly in the diode.

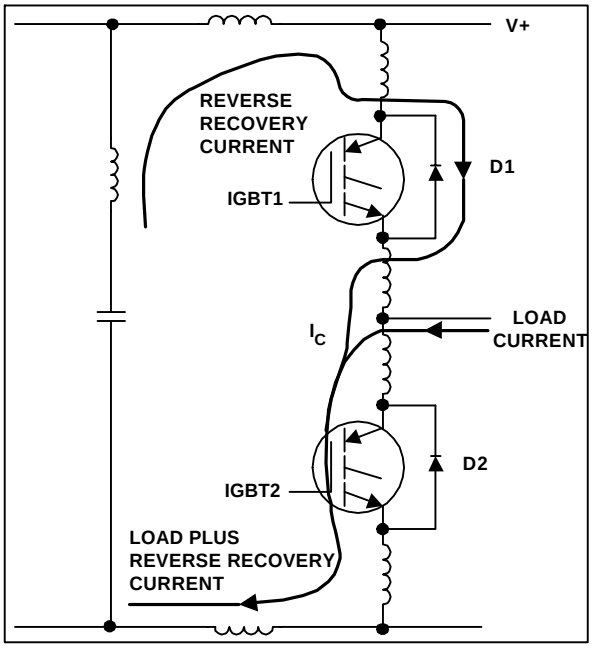


Figure 7a. Typical clamped inductive load showing stray circuit inductances. Load current was flowing in D1 previous to IGBT2 turning on. At turn-on IGBT2 takes over load current and reverse recovery current of D1

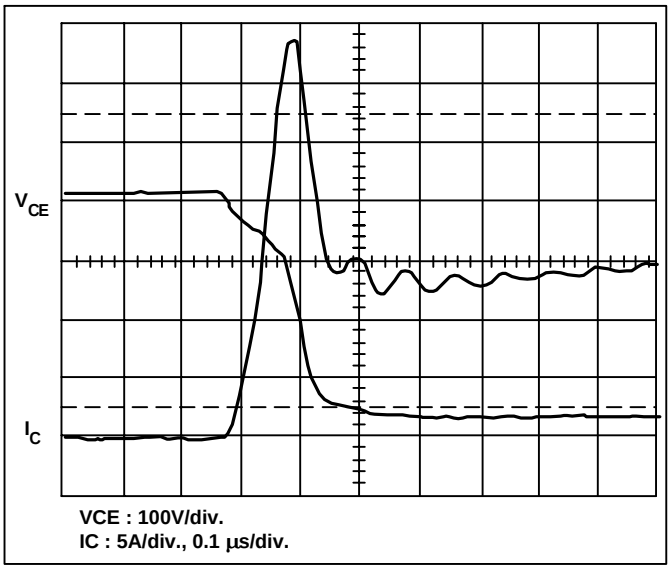


Figure 7b. Turn-on current in IGBT2.

V. TRADE-OFF BETWEEN CONDUCTION AND SWITCHING LOSSES: DEVICE OPTIMIZATION

To compare different devices or technologies, silicon designers often resort to curves of voltage drop vs. current density like those shown in Figure 8. These curves ignore the dynamic behavior of the device and, since in a typical Switchmode application a significant portion of the temperature rise is due to the switching losses, they are not useful in the device selection.

Furthermore, it is frequently inferred, from those curves, that a technology is superior if it is capable of operating at higher current densities. In a specific application, operation at higher current densities means smaller die sizes and, consequently, higher thermal resistances. If total losses stay the same, this implies higher operating junction temperature, with all its negative connotations.

It follows that, for a given thermal design, operation at higher current densities will be advantageous only if the higher thermal resistance is compensated by lower total losses.

To quantify these considerations a simple method has been developed comparing different power devices in a typical Switchmode environment. This method takes all critical aspects into account: thermal constraints, conduction and switching losses.

The popular half-bridge operated with a clamped inductive load was chosen as the benchmark circuit to compare the Performance of different IGBTs. Operating conditions are listed in Figure 9. None of the operating conditions are critical and they can all be changed as necessary. Flyback or resonant circuits could be used in place of the half-bridge to obtain results that are specifically tailored to a given application.

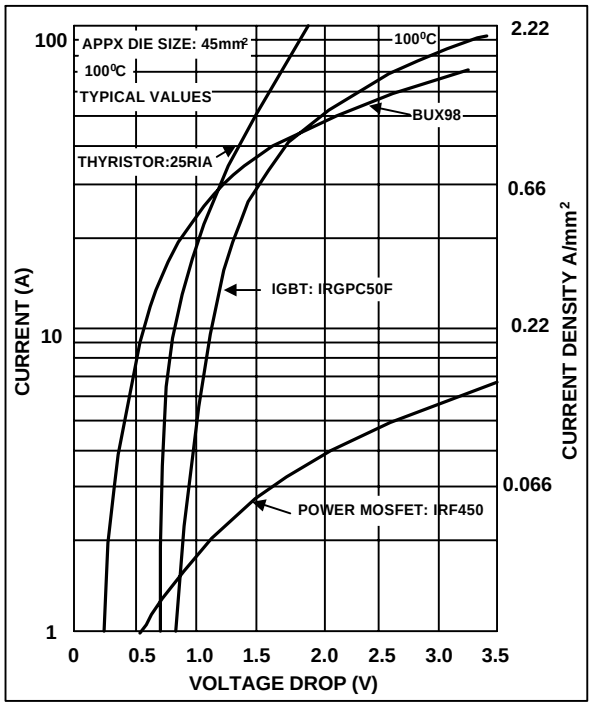


Figure 8. Conduction characteristics for devices of similar die size implemented in different technologies.

This figure shows in a clear and concise way to what extent higher switching frequencies impact the current output of the pair.

It also provides a simple way of selecting the optimum device for the application, which is the one that gives the highest output current at the frequency of Operation.

Once the thermal constraints are properly factored into the operating conditions, the graph carries important application information. In a motor control, the RMS component of the fundamental is directly related to torque.

In a power supply, on the other hand, the total RMS content of the square wave contributes to power. The ratio between the two is 1.11. Although the graph shown in Figure 9 can be generated with a relatively simple test circuit, we have made use of the model presented in the previous sections and of a spreadsheet like the one shown in Figure 10. Starting from the top, the IGBT model parameters are entered first, as appropriate for the junction temperature at which the performance is being evaluated.

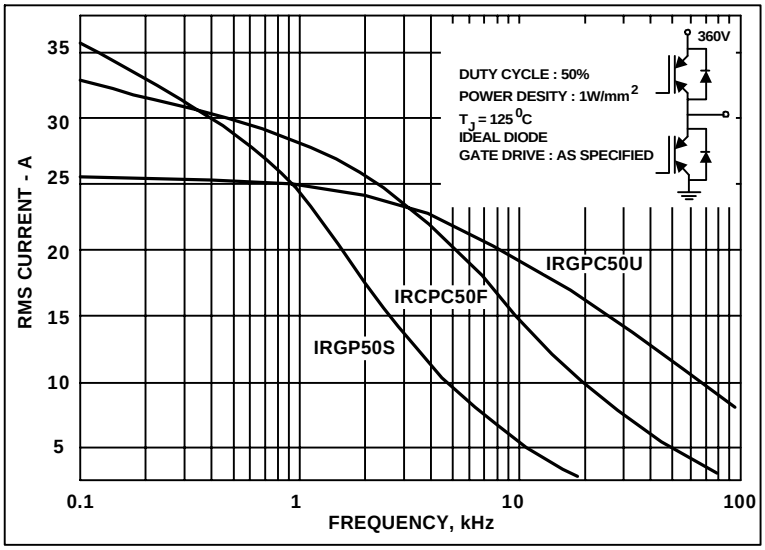


Figure 9. RMS current vs. frequency for a Half Bridge with two IGBTs of same die size, same package, different speed, operated in the conditions indicated in the inset.

Next the diode model is entered, which will be used to calculate the component of turn-on losses in the IGBT due to the reverse recovery of the diode. The conduction model for the diode can also be entered for completeness and to calculate its conduction losses. This will not affect the losses in the IGBT but could provide useful information related to the total losses, efficiency, etc.

The reference voltage for the switching loss model (normally 80% of device rated voltage) is entered next, followed by the actual operating voltage that, for a rectified 220V line, would be approximately 360V. Finally the thermal information is entered in the form of thermal resistance and ambient temperature, from which the allowable Power dissipation is calculated.

The value "Current for balanced losses" is the current at which the conduction losses equal the switching losses for the specific thermal operating conditions. The corresponding frequency is shown at the bottom of the first column under "frequency, ideal diode". These values are calculated by means of a "solve for" function in the spreadsheet and are accurate to the number indicated on the right of the current value. The rest of the spreadsheet performs the calculations of losses for different levels of current. Losses are broken down into two classes: conduction and switching. The formulas in the spreadsheet are described in the next Section. All the losses are summarized at the bottom.

These values are used to generate the Current vs Frequency graph that is reported in each data sheet as Figure 1. If the diode is co-packaged with the IGBT its losses cannot be dissociated from the losses in the main switching device. In this case the thermal information and allowable power dissipation should be for the combination of both devices. Losses should include conduction and switching losses of both devices and the formulas should be modified accordingly.

Part Number:

IGBT MODEL

Tj = 125

Conduction model:	Vt = 0.86	a = 0.1834	b = 0.6999
Turn-on model, ideal diode		h = 0.0028	k = 1.6741
Turn-off model:		m = 0.018	n = 1.2486

DIODE MODEL

Tj = 125

Conduction model:	Vt = 1.00	a = 0.040	b = 1.000
Switching model:	Peak Irr/If = 1.00	ta = 0.035	tb = 0.030µs

Switching parameters at	480 V
Operating voltage:	360 V
Thermal resistance j-c	0.77 K/W
Thermal resistance c-s	0.24 K/W
Thermal resistance s-a	1.5 K/W
Allowable power dissipation	27.89 ^Ta = 55
Current for balanced losses	13.85 1E-05

Peak Current	**A**	**13.85**	**8**	**10**	**15**	**17.5**	**19.5**

CONDUCTION

Voltage drop	V	2.01	1.65	1.78	2.08	2.22	2.33
Losses (50% duty cycle)	W	13.94	6.58	8.89	15.6	19.42	22.68

SWITCHING LOSSES

Turn-on, ideal diode	mJ	0.1685	0.0673	0.0977	0.1927	0.2494	0.299
IGBT losses due to diode	mJ	0.2991	0.1728	0.216	0.324	0.378	0.4212
Turn-off losses	mJ	0.3595	0.1812	0.2394	0.3972	0.4815	0.5512
Diode, switching losses	mJ	0.0374	0.0216	0.027	0.405	0.0473	0.0527

SUMMARY:

Conduction losses	W	13.94	6.58	8.89	15.6	19.42	22.68
Sw. losses, ideal diode	mJ	0.53	0.25	0.34	0.59	0.73	0.85
Pole RMS Current (fund.)	A	12.46	7.200	9.000	13.5	15.75	17.55
Frequency, ideal diode	kHz	26.41	85.74	56.33	20.82	11.58	6.12
Sw. losses, real diode	mJ	0.83	0.42	0.55	0.91	1.11	1.27
Frequency, real diode	kHz	16.86	50.57	34.34	13.44	7.64	4.09

Figure 10. Spreadsheet to calculate Output current vs. Frequency

Part Number: IRGPC50U

THERMAL OPERATING CONDITIONS

Ambient temperature	°C	60.0
Thermal resistance j-to-c	°C/W	0.640
Thermal resistance c-to-s	°C/W	0.240
Thermal resistance s-to-a	°C/W	1.400

		Allowable current at stated Tj		Junction Temperature for state current	
Power dissipation	W	28.5		29.16	
Junction temperature	°C	125	*	126.50	

IGBT MODEL

Vt, Vt1, Vt2	V	0.8000		0.7958	1.0994	-2.40E-03
a, a1, a2	Ohm	0.1120		0.1136	0.2021	-7.00E-04
b, b1, b2		0.7117		0.7085	0.4656	1.92E-03
h, h1, h2	mJ/A	0.0038		0.0037	0.0045	-6.10E-06
k, k1, k2		1.6376		1.6399	1.6162	1.87E-04
m, m1, m2	mJ/A	0.0128		0.0155	-0.0114	2.13E-04
n, n1, n2		1.3382		1.336	1.9457	-4.82E-03
Reference Voltage	V	480		480		

DIODE MODEL

Vt		0.8		0.8	
a, b		0.04	1	0.04	1
Ratio Irr/If		1		1	
ta, tb	µS	0.04	0.03	0.04	

ELECTRICAL OPERATING CONDITIONS **RECT. WAVEFRM, CLAMPED IND. LOAD**

Switching voltage	V	360	360
Operating frequency	kHz	40	40
Duty cycle		0.45	0.45
Peak current	A	9.82	9.82
Voltage drop at peak current	V	1.37	1.37
Conduction losses	W	6.05	6.05
Turn-on losses	W	4.76	4.76
Correction factor for gate resistance		1.00	1.00
Corrected turn-on losses	W	4.76	4.76
Turn-off losses	W	8.14	9.87
Correction factor for gate resistance	W	1.00	1.00
Corrected turn-off losses		8.14	9.87
Turn-on losses due to diode recovery	W	9.55	8.48
Total losses	W	28.50	29.16
Junction temperature	°C		126.49

RMS current, fundamental	A	8.84	15.6
RMS current, total	A	9.82	9.82
Output voltage, RMS funda mental	V	162.000	162.00
Output power, fundamental	kVA	1.59	1.59
Output power, total	kVA	1.77	1.77

* Data entered

Figure 11. Analysis of the operating conditions of an IGBT in a clamped inductive load.

VI. THE ANALYSIS: METHODS TO CALCULATE JUNCTION TEMPERATURE AND POWER DISSIPATION FOR A GIVEN OPERATING CONDITION.

In the previous section we have developed an application related tool to compare the performance of different devices over temperature and frequency. In this section we present a different tool, aimed at analyzing the operating conditions of the power devices, particularly its junction temperature, *in a specific application environment.*

Since temperature affects conduction and switching losses which, in turn, affect temperature, a direct mathematical solution is not possible. However, the models introduced in Sections III and IV, applied iteratively, permit the characterization of a given operating condition with relative ease.

Figure 11 shows an example of such a spreadsheet. It provides junction temperature for a given a value of load current and a given operating environment. It also provides a comprehensive analysis of the losses and temperatures in the thermal system.

This spreadsheet is quite general and applicable to any Switchmode conditioner. It is customized to our application, by entering in the appropriate cells the expressions for power losses that characterize its operation.

In this example they represent a clamped inductive load, typically a Buck converter of Dual Forward. Equivalent spreadsheets for motor drives and UPS would look similar, while containing different formulas to reflect a different relationship between voltage, current, modulation and output power.

A spreadsheet has several advantages over other circuit analysis software:

- can be easily customized for specific applications without special programming expertise;
- all the operating conditions that are important to the designer are summarized in less than half a page;
- energy, power, peak and average currents and voltages are calculated and displayed, as opposed to waveforms on nanosecond scales;
- it is guaranteed to converge and provides a result in a fraction of a second
- it allows true real-time interactive design: the impact of a change in voltage or current or frequency or heatsink is assessed in a fraction of a second without printing stacks of waveforms.

The spreadsheet is divided in the three sections described below.

Input, output and gate drive conditions

All the parameters marked with an "X", like supply voltage, frequency, duty cycle, line current and turn-on gate resistor, should be entered, the others are calculated from the data supplied. Within reasonable limits, the gate resistor at turn-off is not as important, as the turn-off mechanism of an IGBT is mostly dictated by minority carrier recombination

Thermal operating conditions

Ambient temperature and thermal resistances must be entered. Junction temperature is calculated from the losses listed in the last box of the spreadsheet. Junction temperature is used to calculate the device parameters which, in turn, are used to calculate the losses.

This is the fundamental iteration process that yields the operating junction temperature.
The thermal calculations would be somewhat different, depending on whether the inverter is implemented with discrete devices, co-packaged IGBT-diodes or modules.

Fig. 11 applies to discrete devices sharing the same heatsink with additional heat sources. The junction temperature is calculated for IGBTs and diodes.

For power modules this box would be modified to take into consideration the fact that the IGBTs and diodes contribute both to raise the base temperature of the module. Except for the modules which are already isolated, discrete and co-packaged devices are assumed to be isolated from the heatsink. The thermal resistance of the insulating interface is entered in this box.

IGBT and diode model parameters

The third box contains the IGBT model parameters for the specific device, as explained in Section III.B, IV.B and XI. These parameters are used to calculate the voltage drop and switching energy as a function of current *at the specific temperature* indicated in the previous box. They are automatically fetched from a table that is part of the spreadsheet but not shown in Fig. 11.

The diode conduction model is shown in the right-hand side of this box. Recovery parameters are calculated here from the turn-on di/dt of the IGBT which is, in turn, a function of the turn-on gate resistor entered in the first box. The recovery parameters are important to calculate the turn-on losses of the IGBT and the switching losses of the diode.

Power losses

The fourth box lists the components of power losses and junction temperature for one IGBT and the freewheeling diode.

Although the most important information provided by the spreadsheet is the operating junction temperature of the IGBT and of the diode, the additional information provided in the last box is also very useful in optimizing the choice of the power devices. The following observations can be used as examples:

♦ If the switching losses are much larger than the conduction losses, a faster IGBT is desirable. If none is available, it may be advisable to lower the junction temperature to avoid the risk of thermal run-away due to the fact that turn-off losses increase significantly with temperature. This can be done by improving the thermal system, e.g. by increasing the size of the heatsink or isolating the heatsink rather than the IGBT.

The risk of thermal runaway can be easily checked with the help of the spreadsheets by increasing ambient temperature by a few degrees. If junction temperature increases by more than the increase in ambient temperature, there is cause for concern.

♦ If, on the other hand, conduction losses are the dominant component, a slower device may reduce the overall losses and operate at a lower junction temperature.

♦ If a large share of the IGBT losses are due to the diode recovery, a faster diode should be used or faster turn-on of the IGBT. This increases the turn-on spike, but reduces the turn-on losses.

♦ In a well balanced thermal design the case temperature of the active devices is between one-half and three-fourths the temperature rise between ambient and junction. If it lower than that, the heatsink could be reduced. If it is higher, it may be too small.

♦ When a suitable device cannot be found, designers frequently turn to paralleling, a method that has proven quite successful with power MOSFETs. It is somewhat less successful with IGBTs because their dominant losses are switching and switching losses do not decrease with paralleling. They may, in fact, increase, if the gate drive is not adequate. The generally negative temperature coefficient of the conduction drop complicates the task of paralleling, as indicated in Section IX and X. The main advantage in paralleling IGBTs is in the reduction of the thermal resistance between junction and sink, hence junction temperature and turn-off losses.

This spreadsheet allows convenient analysis of the same circuit in different operating points, e.g. under stresses of transitory nature, like shorts in the output, where the junction temperature could be allowed to go to, say, 150°C. In this case the duty cycle would probably be lower and peak current higher.

The spreadsheet contains several formulas, most of them requiring no explanation. From the top:

- ☞ Power dissipation: the ratio between temperature rise and thermal resistance between junction and ambient.
- ☞ The voltage drop is calculated from the model (Section III.B).
- ☞ Conduction losses depend on the specific application. Table I provides some common expressions.
- ☞ Turn-on and turn-off losses are calculated as explained in Sections III and IV
- ☞ The turn-on losses due to diode recovery can be calculated as explained in Section IV.C.
- ☞ The total losses are the sum of conduction and switching losses, including losses due to diode recovery.

VII. BRIEF NOTES ON THERMAL DESIGN

Quite unlike bipolar transistors, whose fundamental limitation in a practical circuit is its limited gain, IGBTs, power MOSFETs and thyristors are thermally limited. Hence, a good thermal design is the key to its cost effective utilization.

When the objective of the thermal design is just the selection of the heatsink that keeps the junction at, or below, a given temperature, the following expression provides the answer.

$$R_{\theta S-A} = \frac{\Delta T}{P_D} - R_{\theta J-C} - R_{\theta C-S}$$

The power dissipation can be calculated with the help of the spreadsheet of Figure 11.

In general, the objective of the thermal design is the selection of the best device-heatsink combination and may require an iterative use of the spreadsheet of Figure 11.

In order to obtain a thermal resistance case-to-sink that is close to the data sheet value, the mounting torque should be close to the maximum specified in the data sheet. An excessive mounting torque causes the package to bow and may crack the die. An inadequate mounting torque, on the other hand, gives poor thermal performance.

The temperature rise due to pulses of short duration can be calculated with the transient thermal response curves (Data sheet Figure 6). The section "Peak Current Rating" in INT-949, describes the procedure in detail.

For short pulses (50ms or less) the temperature rise calculated with the transient thermal response curve tends to be too conservative. A more accurate method to calculate temperature rise can be found in Ref. [4].

VIII. REPLACING MOSFETS WITH IGBTS:

International Rectifier' s 500V IGBTs have switching characteristics that are very close to those of power MOSFETs, without sacrificing the superior conduction characteristics of IGBTs. They offer advantages over MOSFETs in high voltage, hard-switching applications. These advantages include lower conduction losses and smaller die area for the same output power. The smaller die area results in lower input capacitance and lower cost.

Because the package style and the pinout of MOSFETs and IGBTs are identical, no mechanical or layout changes are required.

The gate drive requirement for IGBTs is similar to MOSFETs. A gate voltage between 12V and 15V is sufficient for turn-on, and no negative voltage required at turn-off. The value of the series gate resistor may have to be increased to avoid ringing at the gate of IGBT due to smaller die size.

VIII.A. Power Dissipation

In high voltage MOSFETs, the power dissipation is mostly due to conduction losses; the switching losses being negligible up to 50kHz. On the other hand, the conduction losses in the IGBT are less than in the MOSFET, but the switching losses become significant above 10kHz. The following design example illustrates the point.

Switched DC Current	=	7.5A
Duty cycle	=	0.5
Bus voltage	=	310V
Junction temperature	=	125°C
MOSFET used	=	IRFP450
$R_{DS(on)}$ (25 °C)	=	0.4Ω
Operating frequency	=	50kHz
Current waveform	=	square wave

The on-resistance of the IRFP450 MOSFET at 125°C is (from the data sheet):

$R_{DS(on)}$ (125°C) = 0.816Ω.

The conduction loss in the MOSFET at 125°C:

$P_D = R_{DS(On)}$ (125°C) * I^2 * D = 23W

Assuming 75ns switching times and 50kHz switching frequency, the switching losses in the MOSFET at 7.5A are approximately:

P_{SW}= 6.5 W

The total power loss in the MOSFET is:

P_{tot} = 29.5W

Replacing the MOSFET with a IRGP430U IGBT, the conduction loss in the IGBT is:

$P_c = V_{CE}$ (125°C) * I_c * D

The on-state collector-emitter voltage at 125°C and 7.5 A is from Figure 5 on the data sheet:

$V_{CE\ @\ 125°C}$ = 2.03V.

The conduction loss in the IGBT is:

P_c = 2.03V * 7.5A * 0.5 = 7.62W

Due to the IGBT's higher usable current density, the same power dissipation in the IGBT and MOSFET results higher junction temperature for the IGBT because of higher junction to case thermal resistance.

To maintain the junction temperature parity, the power dissipation in the IGBT needs to be reduced to:

$P_{DIGBT} = P_D * (R_{\theta SA} + R_{\theta CSM} + R_{\theta JCM}) / (R_{\theta SA} + R_{\theta SI} + R_{\theta JCI})$

Where:

$R_{\theta SA}$ Heatsink to ambient thermal resistance.
$R_{\theta CSM}$ MOSFET case to sink thermal resistance.
$R_{\theta JCM}$ MOSFET junction to case thermal resistance.
$R_{\theta SI}$ IGBT case to sink thermal resistance.
$R_{\theta JCI}$ IGBT, junction to case thermal resistance.

The total power dissipation is composed of both conduction and switching losses. Conduction losses were calculated above. Using the formula above yields P_{DIGBT} = 23.2W.

The maximum allowable power loss due to switching losses:

$P_{SW} = P_{TOT} - P_{COND}$
P_{SW} = 23.2W - 7.6W = 15.6W

The maximum switching frequency for same junction temperature in same thermal environment:

f_{max} = 10.3W/0.226mJ = 56.4kHz

The switching energy number comes from data sheet information. It will be appreciated that, being operated with lower losses, the IGBT design is more efficient.

The sources of power dissipation in the IRFP450 MOSFET and IRGP430U IGBT are shown in Figure 12.

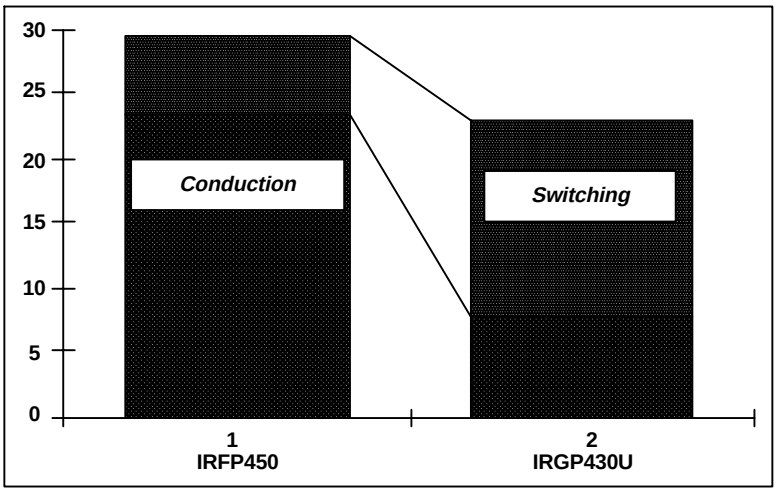


Figure 12. Power losses in an IRGPC450 MOSFET and a IRGP430U IGBT at 7.5A current both switching at 50kHz.

VIII.B Selecting IGBT:

Figure 13 provides an easy method to select an IGBT which can replace IRFP460, IRFP450 or IRFP440 MOSFET in hard-switching applications. The first step is to find the proper curve in the chart, based on the MOSFET's part number.

The part number of the recommended replacement IGBT is shown next to the curve. In general, a given MOSFET can be replaced with a two die size smaller 500V IGBT (e.g. IRFP450 → IRGP430U). The IGBT's die size is typically approximately 40% of the MOSFET's die size.

Next step is to find the maximum operating frequency for the IGBT. By definition, at the maximum operating frequency the IGBT operates at the same junction temperature as the replaced MOSFET.

To find the maximum operating frequency, select the operating current on the horizontal axis and read the maximum operating frequency on the vertical axis.

Using the power dissipation values for the IGBT in Figure 13, the heatsink can be sized for a given ambient temperature.

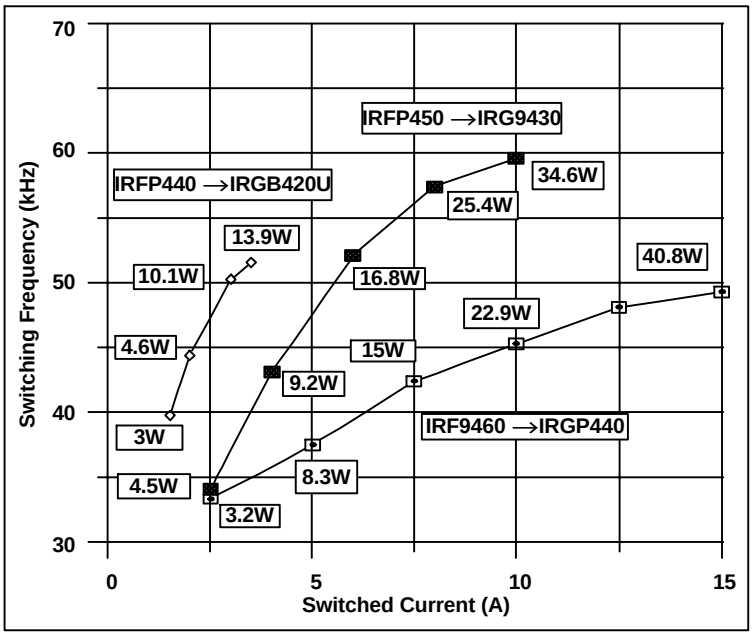


Figure 13. Maximum operating frequency of the IGBT vs. switched current. The IGBT replaces a two size bigger MOSFET in hard-switching application. Operating the IGBT at the frequency indicated by the graph, the junction temperature of the IGBT will be the same to the junction temperature of the MOSFET it replaces.
($T_{ambient}$ = 65^{0}C, T_j = 125^{0}C, Duty cycle = 0.5)

VIII.C. Gate Resistor and Snubber:

The smaller die size and input capacitance of the IGBT may result in faster switching speed than the MOSFET replaced. A larger value gate resistor slows down the turn-on speed, but has little effect on turn-off. Unlike the MOSFET, the turn-off speed of the IGBT cannot be controlled with the series gate resistor.

The high turn-off speed can generate excessive ringing and voltage spikes in the circuit. If a snubber is used, resizing the components helps reducing the noise. Minimizing the stray inductances in the wiring and in the transformer is the most effective way of reducing noise in new designs.

VIII.D. Emitter-Collector Diode:

In applications where the body diode of the MOSFET is used, IGBT-HEXFRED® diode co-packs improve performance and efficiency, while reducing current spikes. This is due to better diode performance.

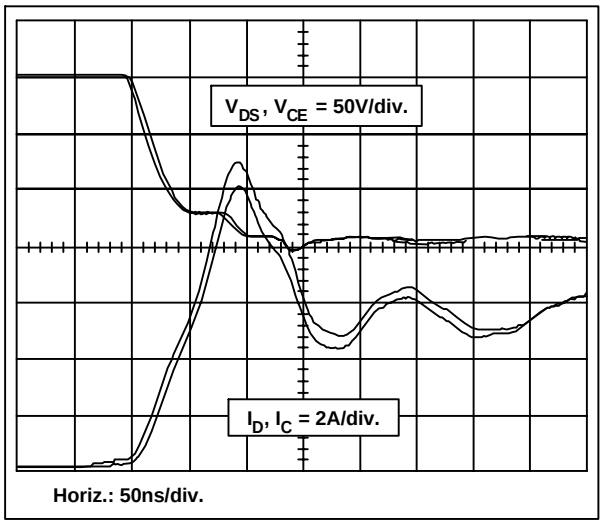


Figure 14. Turn-on waveforms. The IRFP450 and IRGP430 are switching 5.5A at 160V

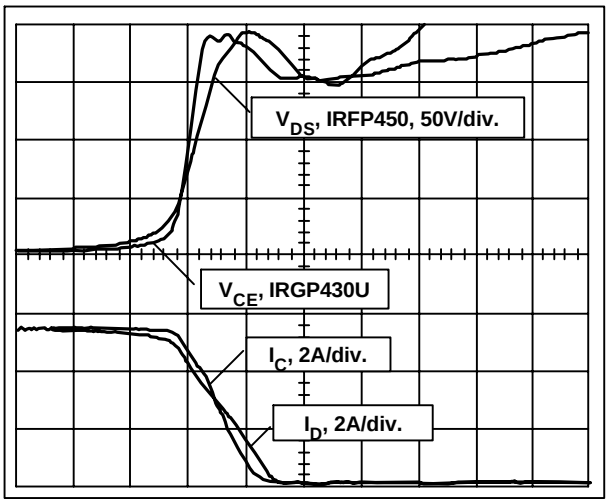


Figure 15. Turn-Off Waveforms, 5.5A at 160V.

VIII.E. Test Results

Figure 14 and Figure 15 show the turn-on and turn-off waveforms for a IRFP450 MOSFET and an IRGP430U IGBT, both switching 5.5A at 160V. The switching waveforms were taken in a 400W, single ended forward converter. Because of different die sizes, a 10 Ohm gate resistor was used for the MOSFET and 33 Ohm for the IGBT. The waveforms show same turn-on speed and faster turn-off for the IGBT.

IX. GUIDELINES ON PARALLELING

Whenever devices are operated in parallel, due consideration should be given to the sharing between devices to ensure that the individual units are operated within their limits. Items that must be considered to successfully parallel IGBTs are: gate circuitry, layout considerations, current unbalance, and temperature unbalance between devices. Paralleling helps to reduce conduction losses and junction to case thermal resistance.

However, switching losses remain the same, or may even increase. If they are the dominant losses, only a thermal resistance improvement will be achieved by paralleling. Paralleling to take advantage of lower price of smaller devices should not be attempted without due consideration of the technical risks. Experimental results should be obtained at the extremes of the manufacturing tolerances.

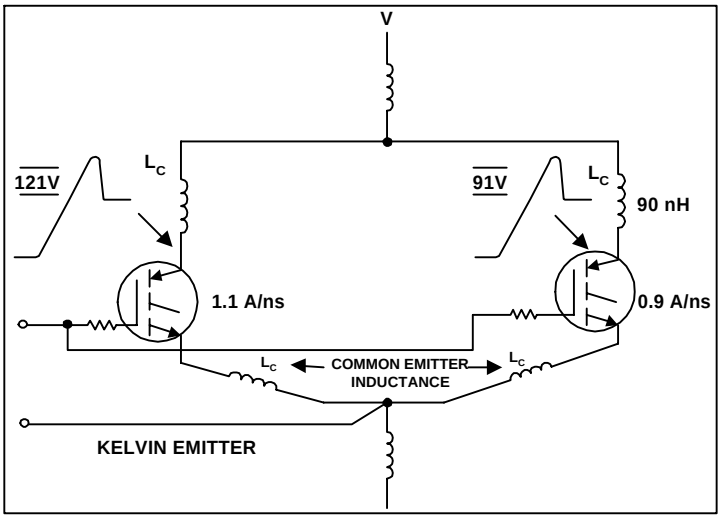


Figure 16. The effect of different di/dt and stray inductances on collector voltages.

Power MOSFETs parallel relatively well due to their positive temperature coefficient. The IGBT, being a combination of a power MOSFET and BJT, cannot be simply described as having either a negative or positive temperature coefficient. The temperature coefficient is dependent on the technology used in the IGBT's design; even within the same technology, it changes depending on the current density.

The three most important parameters from this point of view are: voltage, current and junction temperature. Voltage unbalances will be briefly examined in a qualitative way in the next section with other general considerations. The effects of current and temperature unbalances will be analyzed in detail in the following sections.

A. General paralleling guidelines

Generally speaking, voltage equality is ensured by the fact that the devices are in parallel. However, under transient conditions, voltage differentials can appear across devices, due to di/dt effects in unequalized stray inductances.

The stray inductances of a typical power circuit, like the one shown in Figure 16, have different effects, depending on where they are situated. The effects of the emitter and collector inductances that are common to the paralleled pair have been analyzed in INT-936 and will be ignored here.

An unbalance of 10% in the stray inductances that are in series with each collector, combined with a di/dt unbalance of 10% translates in an unbalance of 20% in the overshoot seen at turn-off (81 vs. 121V). To minimize these differentials both di/dt's and stray inductances have to be matched. However, if the overshoot does not violate the ratings of the IGBT, the differential in the turn-off losses is negligible.

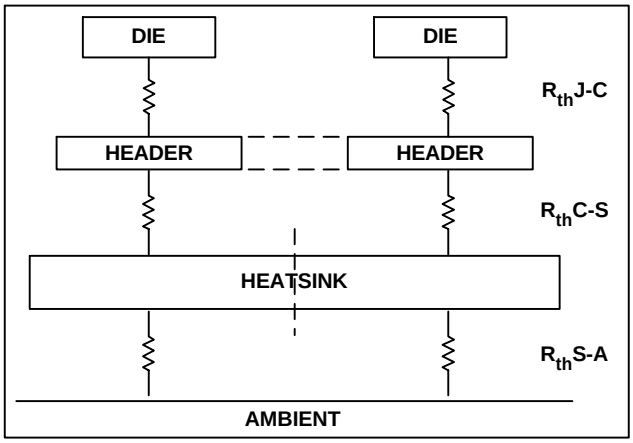


Figure 17. The characteristics of the thermal system of the paralled IGBTs.

The impact of the common emitter inductance on switching energy, on the other hand, is far from negligible, as explained in Section I.E. Furthermore, the IGBT with lower common source inductance turns off before the other, which is left to shoulder the entire load current during the turn-off transient [5]. It follows that Switchmode operation of paralleled IGBTs should not be undertaken unless the common emitter inductances are matched in value.

Finally, like power MOSFETs, parasitic oscillation have been observed on paralleled IGBTs without individual gate resistors. It is assumed that the cause for this oscillation is the same as that reported in Ref. [5], Figure 17.

In summary, the following general guidelines should be followed when paralleling IGBTs:

- Use individual gate resistors to eliminate the risk of parasitic oscillation;
- Equalize common emitter inductance and reduce it to a value that does not greatly impact the total switching losses at the frequency of operation;
- Reduce stray inductance to values that give acceptable overshoots at the maximum operating current.
- Ensure the gate of the IGBT is looking into a stiff (voltage) source with as little impedance as practical. This advice applies equally well to both paralleled and single device designs.
- Zener diodes in gate drive circuits may cause oscillations. Do not place them directly gate to emitter/source to control gate overvoltage, instead place them on the driver side of the gate isolation resistor(s), if required.
- Capacitors in gate drive circuits may also cause oscillations. Do not place them directly gate to emitter/source to control switching times, instead increase the gate isolation resistor. Capacitors slow down switching, thereby increasing the switching unbalance between devices.

Stray components are minimized by a tight layout and equalized by symmetrical position of components and routing of connections.

These guidelines ensure that the voltage and switching unbalances due to the layout are negligible with respect to those due to the IGBTs themselves, analyzed in the next section.

B. Current and temperature unbalance

In this section we will examine the steady state conduction and temperature unbalance due to the IGBTs themselves and the effects of frequency and duty cycle. When paralleling power semiconductors, the first issue that comes to mind is how well they share the total current. But, semiconductors are more sensitive to temperature than to current, so the real issue is how closely they are matched in junction temperature and whether or not one of the devices approaches the rated junction temperature. As junction temperature directly correlates to reliability, it should be of primary concern to the designer

Given two different IGBTs, each $V_{CE(on)}$ for any given current level will be slightly different. When these two IGBTs are operated in parallel, the $V_{CE(on)}$ across both devices is forced to be the same.

Thus, for a given load current, one IGBT will carry more current than the other, resulting in a current unbalance. *As long as the current remains below the maximum specified on the data sheet, current unbalance is not critically important.* At lower currents, it can be 75-100%.

Since the voltage drop is the same for both IGBTs, the device that carries more current has a higher junction temperature that may exceed the maximum rated junction temperature of 150°C. Combined with reliability issues, this factor should focus the designer's primary concern on temperature unbalance.

Current unbalance may not be affected significantly by thermal coupling. This is shown in the figures in the following section depicting current unbalance for IGBTs mounted on both separate and common heat sinks. However, the more important criteria, temperature unbalance, is affected significantly. In fact, the figures in the following section show that the maximum current is limited by the hotter device exceeding the 150°C maximum junction temperature rating. See Reference [1] Section VIII.B.3 for more information.

The complexity of the algebraic equations does not allow a direct, closed form solution of general applicability. However, with the help of the models presented in Sections III and IV and a spreadsheet, we can establish the operating conditions of two paralleled IGBTs in a given application environment. The results, although specific to the application, provide a useful insight into the factors that come into play and their respective effects.

1. Selection Criteria For The IGBTs

As far as this analysis goes, two IGBTs (IRGPC50U) have been selected from a population of 15 devices from three different lots. The two IGBTs were at the two extremes of the distribution of voltage drop, one being the highest (IGBT 1), the other being the lowest (IGBT 2). Temperature and current were not a factor since both IGBTs remained, respectively, the highest and the lowest throughout the temperature and current range.

The conduction and switching parameters were generated for both IGBTs and are listed in the spreadsheets we will use to calculate the operating conditions, together with the average parameters for the entire population.

Notice that the analysis carried out in the following sections is based on two extreme but real IGBTs, chosen from a given population. As it should be expected, the IGBT with better conduction characteristics has worse switching characteristics.

From that same population we could have constructed the model for *two fictitious* IGBTs with extreme conduction *and* switching behavior. This, however, would have been at odds with the fundamental trade-off between conduction and switching characteristics, typical of the device itself.

2. The Thermal System

The heat generated by the two IGBTs is transmitted to a sink and, ultimately, to a common ambient. Two cases will be examined: common and separate heatsinks (Figure 17).

A common heatsink establishes a thermal coupling between the two dice that limits their temperature differential. As it will be seen later, if the thermal coupling is tight, as with dice mounted on the same spreader, the temperature differential is in the order of few degrees.

3. Steady State Operating Conditions

Being in parallel, the voltage drop across the IGBTs is the same. Hence, the IGBT with better conduction characteristics carries a larger share of the load current to make its voltage drop the same as the other. Its power dissipation and junction temperature are higher by an amount that depends on the thermal design, as we will now see.

IGBT MODEL PARAMETERS

	IGBT 1 high drop		IGBT 1 high drop	nominal
Vt1	1.1784		1.0128	1.0994
Vt2	-0.0024		-0.0023	-0.0024
a1	0.3804		0.106	0.2021
a2	-0.0019		-7.00E-05	-0.0007
b1	0.3111		0.6148	0.4656
b2	0.0029		0.00	0.00

APPLICATION ENVIRONMENT

Current	25	
Ta	45	
Rth s-a	1.20	
Rth subs-sink	0.35	
Rth j-subs	0.30	(single die)

OPERATING CONDITIONS

Tj	107.79		112.38	109.9
Vt	0.9197		0.7543	0.8356
a	0.1756		0.0984	0.1252
b	0.6194		0.7222	0.6766
Delta I	39.98%	5.00	-39.98%	
I	7.50		17.50	12.50
Voltage drop	1.53		1.53	1.53
Cond. losses W	11.49		26.80	19.09
Delta T j-subs	3.45		8.04	5.73
Delta T subs-a		59.35		59.17
Tj	107.79		112.38	109.90
%	-1.91%		2.26%	0%

Alt-S	{for b35, 1, 6, 1, b37} 7
Iterate	{/ Math; Solve Go} {/Block; Values} b29..d29~ b17~

Figure 18. Spreadsheet used to establish the operating conditions of two specific IGBTs in parallel. Model parameters are shown at the top. The parameters for the entire population are also listed for reference.

For a given set of thermal conditions and a given common current, the individual currents and junction temperature can be calculated with a spreadsheet like the one shown in Figure 18. The spreadsheet is laid out to establish the operating point in the following way:

- Reasonable junction temperatures appear at the top of the Operating Conditions.
- The model parameters for that temperature are calculated.
- The current unbalance is calculated by means of the "solve" function. The equations that govern this relationship can be found in Appendix 2.
- Calculate conduction losses and temperature rise between junction and common sink for both IGBTs.
- Calculate temperature rise between common sink and ambient.
- Calculate both junction temperatures.
- Enter the junction temperatures thus calculated to the top of the box and repeat the process until the two temperatures become the same.

The results of this analysis are shown in Figure 19. For low currents the conduction unbalance can be as high as 100%, i.e. one IGBT takes the entire current, operating, however, well within its limits.

As the load current increases the current unbalance decreases and, long as the IGBTs are mounted on a common heatsink, the two temperatures stay within ±10°C.

The use of separate heatsinks causes large current unbalances and very significant temperature differentials..

The first factor that keeps the unbalance in check is the thermal feedback between the two junctions. The one with higher power dissipation increases the sink temperature and, consequently, the junction temperature of the other, by an amount that is inversely proportional to the thermal resistance between the junctions.

If the thermal coupling between dice is tight, the temperature differential cannot be significant. The other factor that reduces the current unbalance is the temperature coefficient of the voltage drop.

Although they are both negative, the IGBT with lower voltage drop has a lower temperature coefficient.

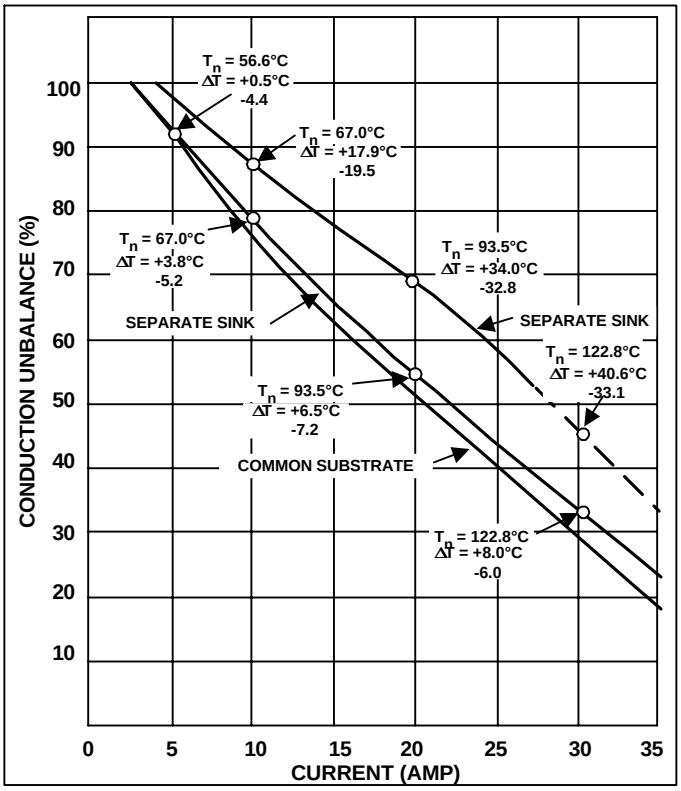


Figure 19. Conduction unbalance for two paralleled IGBTs as a function of current for three different thermal designs.

As current and temperature increase, its voltage drop changes little, while the voltage drop of the IGBT that was carrying little current comes down significantly, thereby closing the gap in current, as well as temperature.

There is a third balancing mechanism: as collector current increases, the voltage drop of the two IGBTs converge toward the average of the distribution. This intrinsically reduces the unbalance at higher currents.

4. The Effect of Frequency and Duty Cycle

In a practical applications the two IGBTs would be operated at some frequency and the losses in both devices would have a switching component.

The IGBT that carries more current will also be switching a higher current. Hence, it has higher conduction, as well as higher switching losses. The unbalance in losses is further compounded by the fact that, as we have mentioned previously, this same IGBT exhibits a worse switching behavior, which further increases its switching losses.

Thus, it would appear that a regenerative process is in place that will quickly take the junction temperature of the IGBT with lower conduction losses beyond its rated limits and that this regenerative process is accelerated by the operating frequency. In practice this does not happen and frequency helps bring about balanced operation, as we are about to see.

One additional unbalancing element, disregarded in the following calculations, is due the fact that, with a clamped inductive load, the IGBT that goes off last, ends up carrying the entire load current. This turn-off unbalance can be disregarded only to the extent that the turn-off times of the devices is short compared to the individual stray inductances, which tends to reduce this source of unbalance.

The operating conditions can be calculated with a spreadsheet similar to that shown in Figure 18, except that additional entries are required for the switching losses (Figure 20).

IGBT MODEL PARAMETERS

	IGBT 1 high drop		IGBT 1 high drop	nominal
Vt1	1.1784		1.0128	1.0994
Vt2	-0.0024		-0.0023	-0.0024
a1	0.3804		0.106	0.2021
a2	-0.0019		-7.00E-05	-0.0007
B1	0.3111		0.6148	0.4656
b2	0.0029		0.00	0.00
p1	-0.0033		-0.01	0.00
p2	0.0001		0.00	0.00
q1	1.8428		1.7941	1.7994
q2	-0.0027		-0.0029	-0.0026

APPLICATION ENVIRONMENT

Duty cycle	0.5		
Operating voltage	360		
Ipeak	44.43	Irms, pole, fund.	40
Ta	45		
Rth s-a	1.20		
Rth c-s	0.24		
Rth j-c	0.64		
Frequency (kHz)	0.4		

OPERATING CONDITIONS

Tj	115.64		123.13	118.43
Vt	0.9009		0.7296	0.8152
a	0.1607		0.0976	0.1192
b	0.6418		0.7325	0.693
p	0.0127		0.0186	0.0148
q	1.5306		1.4407	1.4915
I	16.15	-27.31%	28.28	22.21
Voltage drop	1.86		1.86	
Cond. losses W	15.01		26.29	20.41
Sw losses W	0.27		0.69	0.45
Delta T j-subs	9.78		17.26	13.35
Delta T subs-a		60.85		60.07
Tj	115.62		123.11	118.42
%	-2.37%		3.96%	0%
Delta T	-2.8°C		4.7°C	0.0

Figure 20. Spreadsheet to calculate the operating conditions of two paralleled IGBTs operated in switchmode.

Curves of current and temperature unbalance have been generated for the popular "half-bridge" circuit, as shown in Figure 21a. From these curves we observe the following:

1. As the frequency increases the current unbalance decreases. The rate of decrease increases with frequency.

2. As the current increases the amount of unbalance decreases. This result is consistent with the observations made in the Previous section.

3 . As the frequency increases the temperature differential increases. then decreases rapidly.

The key balancing mechanism in this, as in the steady state mode of operation, is the different temperature coefficients of the voltage drop.

As we have seen in the previous section, an increase in current causes an increase in temperature which, in turn, causes a reduction in voltage drop that is larger for the IGBT with a higher voltage drop. Hence, an increase in temperature results in a reduction in current unbalance.

Switching losses increase junction temperature of both IGBTs and contribute to reduce the current unbalance.

However, the increase in temperature is higher for the IGBT which carries the higher current, on account of its higher conduction and switching losses.

This delays the balancing mechanism and causes the increase in temperature differential noticeable in Figure 21 between 10 and 30 kHz ($I = 20A_{RMS}$). The thermal coupling and the difference in temperature coefficients gradually cause a reduction in the current unbalance.

This, in turn, reduces conduction and switching losses in the IGBT that was carrying more current, thereby bringing about a more balanced operating condition at an exponential rate. For the specific IGBTs we have modeled the point of current balance occurs at a temperature that is somewhat higher than 150°C.

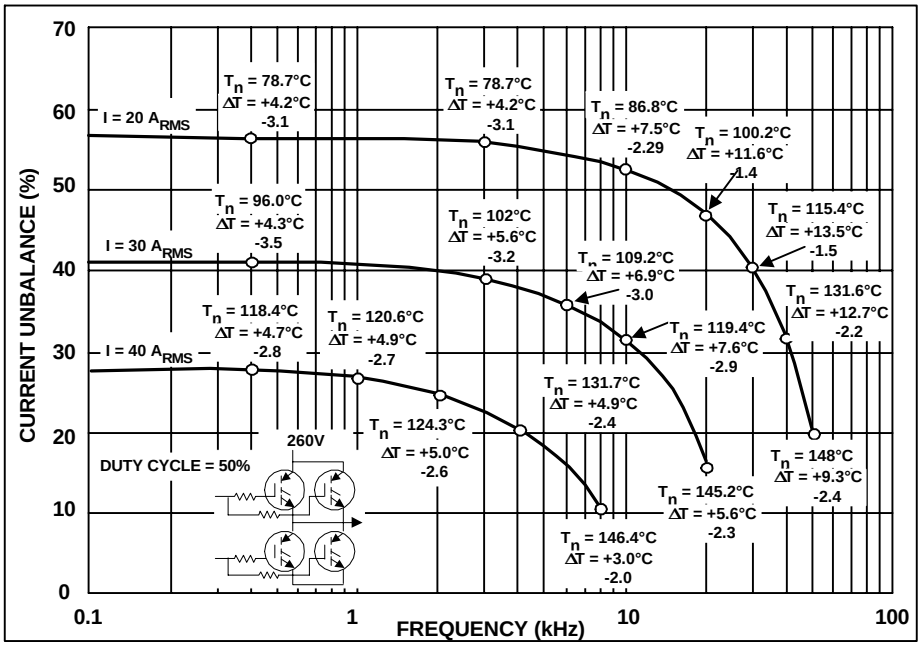


Figure 21a. Duty cycle at 50%

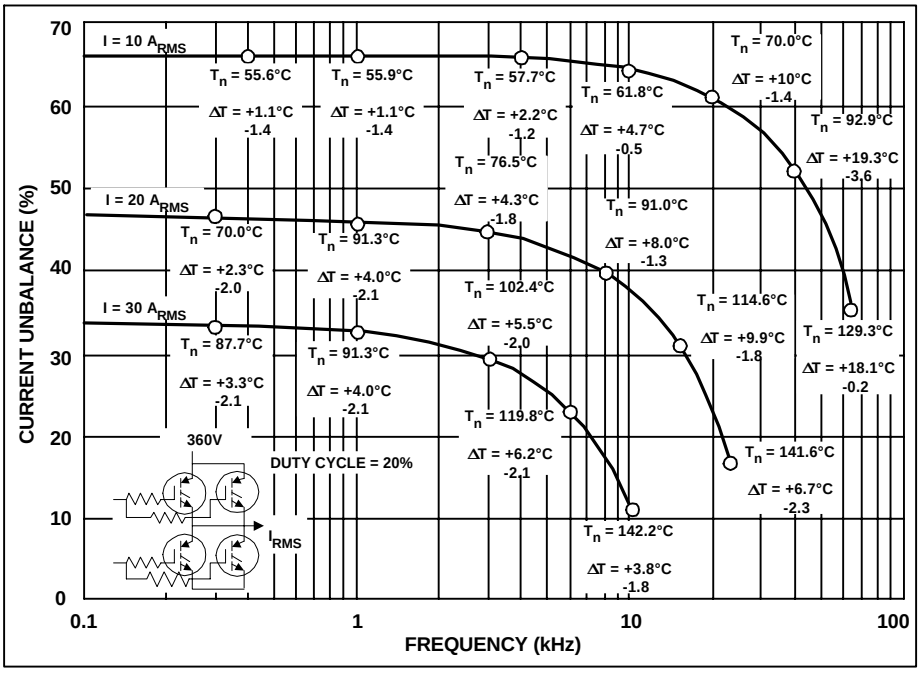


Figure 21b. Current and temperature unbalance as a function of frequency of two IGBTs operated in parallel.

At this point there will still be a temperature differential, on account of different switching losses. It is entirely possible that IGBTs with different characteristics may reach current balance at a lower temperature, beyond which the unbalance would reverse.

Operation at lower duty cycles is not significantly different from what we have just described (Figure 21b), except that the current unbalance for a given output current is lower.

This is due to the third balancing mechanism, whereby the voltage drops converge at higher currents. To generate the same output current with a lower duty cycle a higher peak current is necessary, with intrinsically better current sharing.

C. Conclusions

Although the analysis presented in the previous sections is limited to one specific type of IGBTs in a specific operating mode, the results have been found to be equally applicable to the other families of IGBTs available from International Rectifier at the time of writing. They can he summarized as follows:

1. Paralleled IGBTs will operate with a current unbalance that, in a practical application, can be as high as 50 to 70% at low currents. Temperature unbalance, on the other hand, is generally less than 10°C, provided they are on the same heatsink.

2. Three balancing mechanisms tend to reduce the current unbalance:

    * thermal feedback;
    * different temperature coefficients of the voltage drop;
    * converging voltage drop characteristics at higher currents.

3. The tighter the thermal coupling, the lower the unbalance. Operation of paralleled IGBTs on separate heatsinks should be avoided.

4. An increase in junction temperature reduces the unbalance, on account of the different temperature coefficients of the voltage drop. An increase in frequency has the same effect, for the same reason.

5. An increase in current reduces the unbalance, due to converging dynamic resistances. It would also cause an increase in temperature and, consequently, a further reduction in unbalance.

6. For a given output current, a decrease in duty cycle causes an increase in peak current, hence a reduction in unbalance.

X. SCREENING OF IGBTS FOR PARALLELING

In this section we will cover the following:

* Discuss one method of device selection to achieve better sharing, and compare performance achieved for IR's 600V Fast IGBTs.
* Compare performance achieved for IR's 600V UltraFast™ IGBTs.
* Discuss multiple (> 2) parallel IGBT designs.

X.A. Screening method for IR' 600V Fast IGBT

Device selection is an effective method to reduce derating that is intrinsically associated with paralleling and ensure that IGBTs are operated within data sheet limits. As a selection criteria, the voltage across each IGBT was measured at a certain current level. The configuration of this measurement is what we call "diode mode" (Figure 22) which means the gate is tied to the collector, and voltage is applied across that combined terminal and the emitter.

The voltage is increased until the desired current is conducted through the IGBT. This measurement must be done in pulse mode to avoid device self-heating. The voltage required for this amount of current is recorded. This measurement not only takes into account variations in $V_{CE(on)}$, but also threshold, as well as g_{fs}. This "diode mode" voltage results in a convenient way to select IGBTs that will be paralleled.

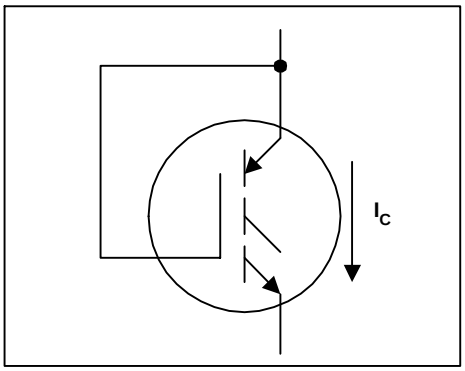


Figure 22. Connection for Measuring "Diode Mode" Voltage, V diode

Matching only $V_{CE(on)}$ would be more appropriate for IGBTs not operated in Switchmode. In the following two sections, simulations have been run on different pairs of IGBTs to compare temperature unbalance and current unbalance versus device variation measured using the "diode mode" voltage of the IGBT.

Using this device selection strategy, we set out to devise a method of determining how well various pairs of IGBTs parallel in a typical half-bridge configuration. To this end, an empirical model was used for our IGBTs that models conduction and switching loss described in Sections III.B and IV.B.

Five devices from each lot, using three lots, were examined and ranked in order of conduction voltage. Using this information, it is possible to obtain the operating point of IGBTs in parallel operation.

To compare performance of various sets of IGBTs, graphs of percent current unbalance versus total current were developed. These graphs depict how much D.C. current unbalance can be expected for a given total current, for a particular pair of IGBTs.

Two cases are plotted - devices mounted on separate heat sinks and devices mounted on a common heat sink. Also generated were graphs of junction temperature of the higher of the two junctions versus total current. In these graphs, three curves are plotted: 1) perfectly matched devices with no unbalance, 2) devices unmatched by a value of ΔV_{diode}, mounted on the same heat sink, and 3) devices unmatched by a value of ΔV_{diode}, mounted on separate heat sinks.

Figure 23 depicts the percent current unbalance at different current levels for the two IRGPC50Fs at both ends of the spectrum: one has the lowest $V_{CE(on)}$, while the other has the highest $V_{CE(on)}$ of all the devices tested. The ΔV_{diode} for this pair of IGBTs was 0.69V. The operating conditions were: two devices mounted on either a common heat sink with an $R_{\theta SA}$ of 2°C/W, or separate heat sinks with $R_{\theta SA}$s of 4°C/W, with an ambient temperature of 45°C.

As Figure 23 shows, at low currents, one IGBT carries all the current. As the current increases, the unbalance improves due to the three balancing mechanisms we mentioned above for the lower curve (same heat sink, therefore tight thermal coupling) and just the two related to current for the upper curve (separate heat sink).

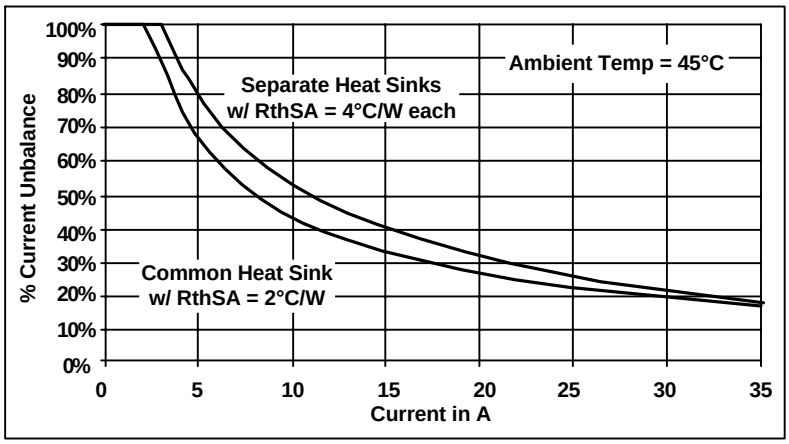


Figure 23. Percent Current Unbalance versus Total Current, IRGPC50F with ΔVdiode = 0.69V

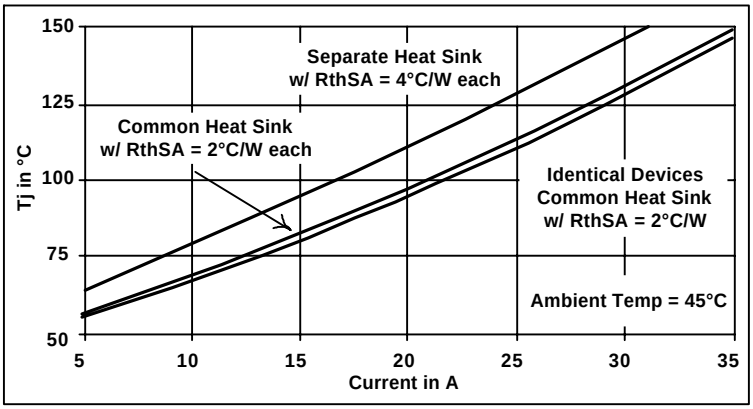


Figure 24. Junction Temperature versus Total Current, IRGPC50F with DVdiode = 0.69V

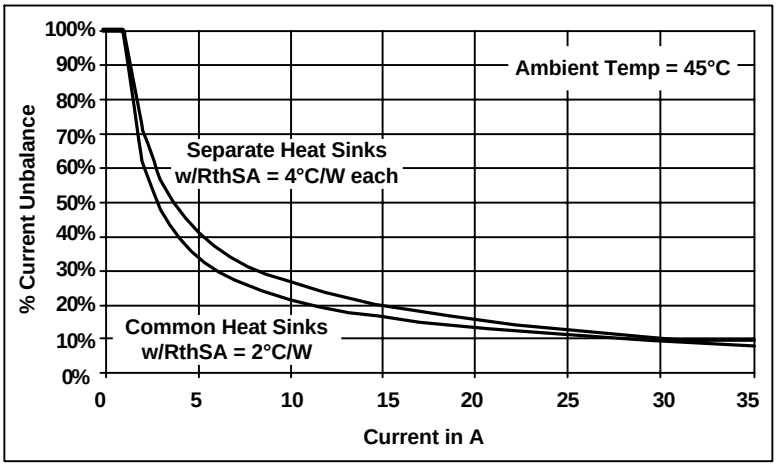


Figure 25. Percent Current Unbalance versus Total Current, IRGPC50F with ΔVdiode = 0.33V

Figure 24 depicts the higher junction temperature of the two IGBTs in parallel for three different cases: perfectly matched devices, the above two devices mounted on the same heat sink and the above two devices mounted on different heat sinks. This figure provides the strongest argument for placing separate devices on the same heat sink: while conducting 20 A, the two worst case IGBTs' junction temperatures are within 2.5°C of the ideal case of perfectly matched IGBTs. However, the junction temperature of one of these same two devices mounted on separate heat sinks operates at an increased junction temperature of 16°C. Also note that the maximum allowable current is reduced from 35 A to 31 A. All solely due to the devices' being mounted on separate heat sinks.

The two devices in Figures 23 and 24 exhibited the largest range in V_{diode} of all 15 devices tested. The difference in "V_{diode}" voltages was 0.69 V measured at 20 A.

For two devices that had a difference of 0.33 V at 20A, the graphs are shown in Figures 25 and 26. These devices, mounted on separate heat sinks, are limited to a maximum current of 33 A, while devices on a common heat sink can operate to 35 A.

While conducting 20 A, the two IGBTs' junction temperatures are within 1.5°C of the ideal case of perfectly matched IGBTs when mounted on a common heat sink. The same two devices mounted on separate heat sinks operate at an increased junction temperature of 8.3°C.

Figures 27 and 28 depict the correlation of current unbalance and junction temperature to the "Vdiode" screening parameter.

From these two figures, it is possible to predict the operation of a parallel pair of IGBTs given the difference in their "diode mode" voltages.

Figure 29 depicts the reduction in output current in a half-bridge circuit due to junction temperature limitations between unmatched IGBTs.

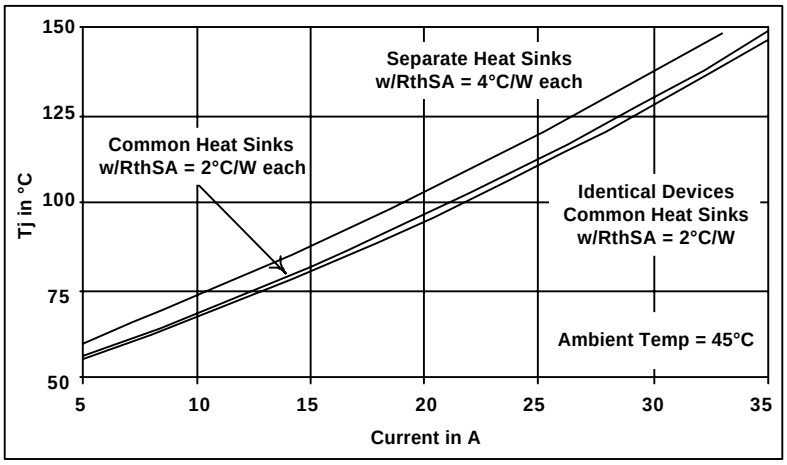


Figure 26. Junction Temperature versus Total Current, IRGPC50F with ΔVdiode = 0.33V

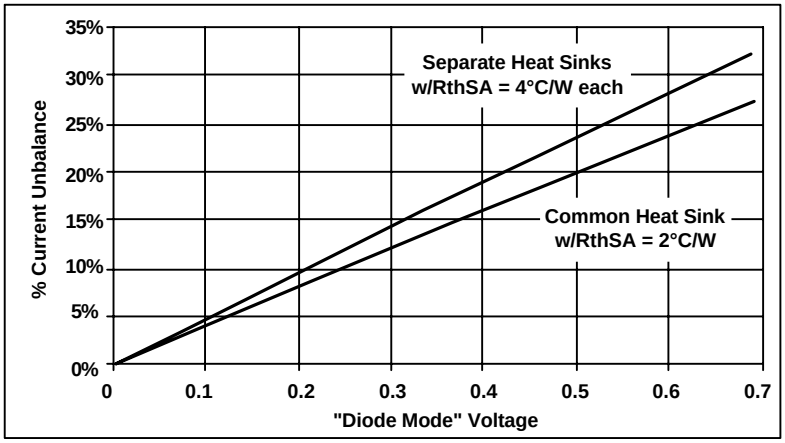


Figure 27. Percent Current Unbalance versus ΔVdiode, IRGPC50F

The circuit is operated under the same conditions as the previous ones, but instead of the current being fixed, the junction temperature is fixed at 125°C. Neither IGBT is allowed to exceed 125°C. The graph plots the maximum output current versus switching frequency. Notice that little or no derating is necessary under common applications or conditions.

The curves in Figure 29 were calculated assuming the two devices were mounted on a common heat sink. The case of separate heat sinks was not addressed due to concerns previously mentioned.
The output current would be significantly reduced if the devices were on different heat sinks.

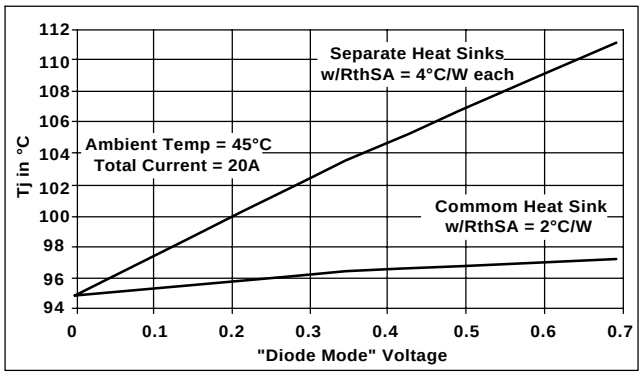


Figure 28. Junction Temperature versus ΔVdiode, IRGPC50F

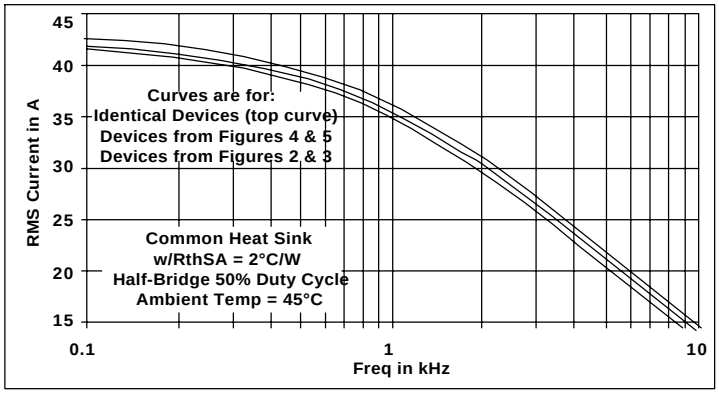


Figure 29. Current versus Frequency Graph for Three Pairs of IRGPC50Fs with ΔVdiode = 0.00, 0.33, & 0.69V

X.B. Device Selection for IR's 600V Ultra Fast IGBT

The method presented in the previous section was found to be inappropriate when the amount of lifetime killing has a significant impact on the behavior of the device. For these devices, a simple $V_{CE(on)}$ matching scheme has been implemented. The following figures describe the performance achieved using various pairs of paralleled UltraFast IGBTs.

Figure 30 depicts the percent current unbalance at different current levels for the two IRGPC50Us at both ends of the spectrum: lowest and highest $V_{CE(on)}$s of the entire population of 15 devices from three lots. The $\Delta V_{CE(on)}$ for these was 0.55 volts measured at 30 amps. The operating conditions were: two devices mounted on a common heat sink with an $R_{\theta SA}$ of 2°C/W with an ambient temperature of 45°C.

While the current sharing displayed in Figure 30 may appear to be unacceptable, as discussed in the previous section, the more important factor is the junction temperature, which is shown in Figure 31. The upper curve in Figure 10 is for the devices in Figure 30, while the lower curve is for two identical (i.e., $\Delta V_{CE(on)}$ is zero). For any current the penalty resulting from mismatched devices is only a few degrees Celsius.

To compare closer matched devices, the above two figures were repeated using two devices with a $\Delta V_{CE(on)}$ = 0.36V measured at 30 amps. Figure 32 depicts the percent current unbalance at different current levels for two mismatched IRGPC50Us. The operating conditions are the same as the previous two figures.

Figure 33 depicts the junction temperature versus current. The upper curve in Figure 33 is for the devices in Figure 32, while the lower curve is for two identical (i.e., $\Delta V_{CE(on)}$ is zero).

Figure 34 depicts the higher of the two junction temperatures for the parallel combination of several different pairs of IRGPC50Us with increasing $\Delta V_{CE(on)}$s. This graph shows that screening is not very effective and that it is critically important that paralleled devices be mounted on a common heat sink.

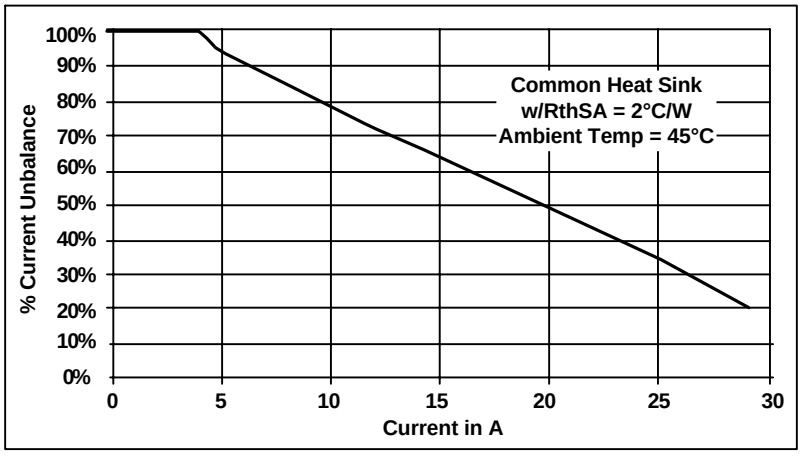


Figure 30. Percent Current Unbalance versus Total Current, IRGPC50U with $\Delta V_{CE(on)}$ = 0.55V

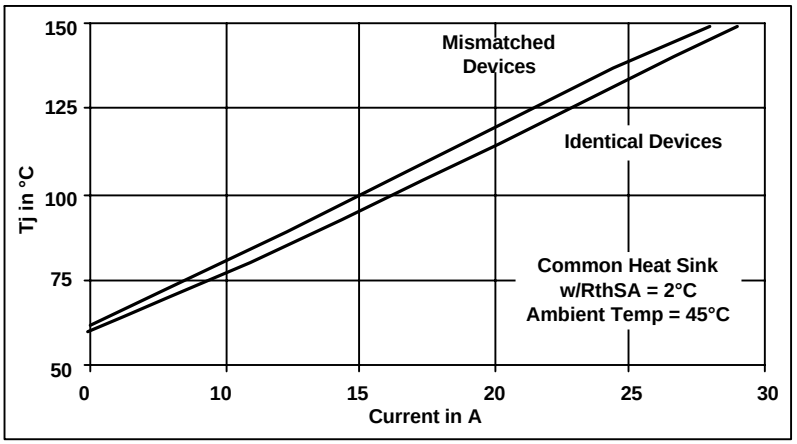


Figure 31. Junction Temperature versus Total Current, IRGPC50U with ΔVCE(on) = 0.55V

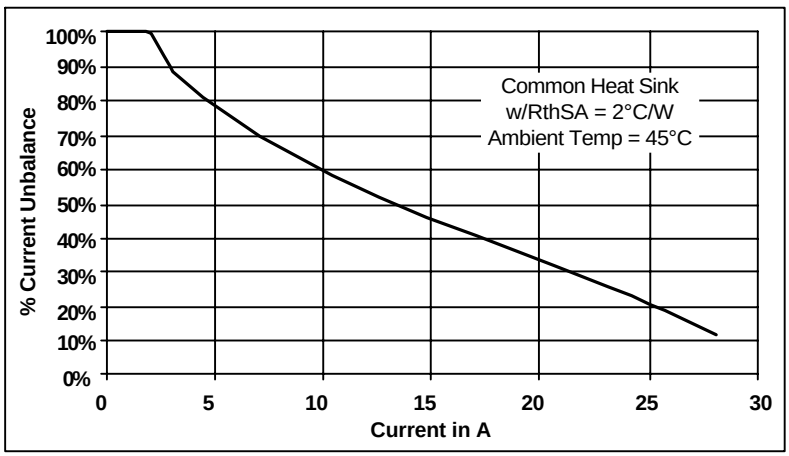


Figure 32. Percent Current Unbalance versus Total Current, IRGPC50U with $\Delta V_{CE(on)}$ = 0.36V

The final graph, Figure 14, depicts the RMS current versus switching frequency for a parallel pair of IRGPC50Us operated in a typical half-bridge configuration with 50% fixed duty cycle. The devices are mounted on a common heat sink with a thermal resistance of 2°C/W with an ambient temperature of 45°C. Neither IGBT is allowed to exceed a junction temperature of 125°C.

The upper curve is for identical devices, the next curve is for the devices described in Figures 11 and 12, while the lower curve is for the devices described in Figures 9 and 10.

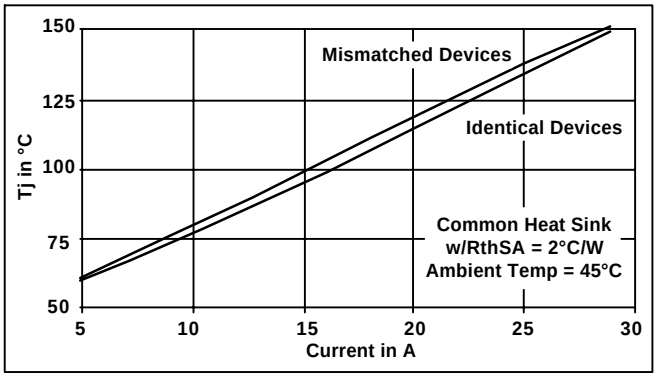


Figure 33. Junction Temperate versus Total Current, IRGPC50U with $\Delta V_{CE(on)}$ = 0.36V

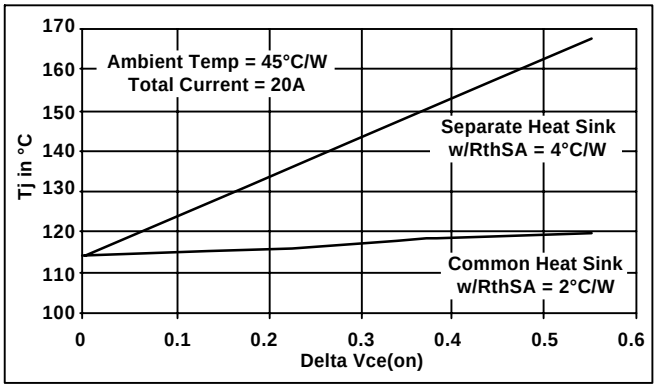


Figure 34. Junction Temperature versus ΔVCE(on), for IRGPC50Us

Comparing the output current vs frequency of the IRGPC50U (Figure 35) with that of the IRGPC50F (Figure 29) we notice that:
- Current output of Ultrafast devices operated in parallel degrades more that that of Fast IGBTs
- $\Delta V_{CE(on)}$ screening is more effective on the Fast IGBTs than on the Ultrafast

X.C. Multiple Paralleled Devices

The previous discussions have been limited to two paralleled devices, the only case that can be treated with simple analytical tools.

This does not limit the generality of the conclusions, however, as in any group of paralleled devices, there will be two with extreme voltage drops.

As explained in Section IX.B.1., these two are also likely to have extreme switching characteristics. The selection criteria, would apply to these two extreme devices, with all others falling in between.

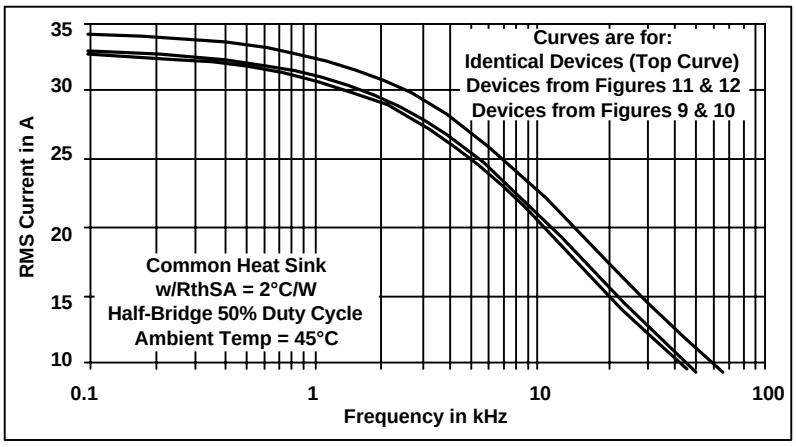


Figure 35. Current versus Frequency Graph for Three Pairs of IRGPC50Us with ΔVdiode = 0.00, 0.36, & 0.55V

References:

[1] Switching Waveforms of the L^2FET, by C.F. Wheatley and H.R. Ronan IEEE Transactions on Power Electronics. April 1987 p. 81

[2] Analysis and characterization of power MOSFET switching performance, by S.M. Clemente, A. Isidori, B.R. Pelly. Proceedings of Powercon 8, 1981, H2.

[3] Nondestructive RBSOA characterization of IGBTs and MCTs by Dan Y. Chen, VPI Current, Fall 91

[4] Transient Thermal Response of Power Semiconductors to Short Power pulses, by S. Clemente, Proceedings of the European Power Conference, Florence 1991.

[5] AN-941: A Chopper for Motor Speed Control

APPENDIX 1: DESCRIPTION OF THE CURVE FITTING METHODS USED TO DERIVE THE MODEL PARAMETERS.

The conduction model presented in Section III fulfills the basic requirements of accuracy and simplicity. As it shown in Table II, it lends itself to easy integration, thus providing a closed form expression for the conduction losses of common waveforms.

The parameters of the model are extracted from the averages and standard deviations taken at a given temperature on a population of IGBTs from three different lots, as shown in Table A.1.

VCE(ON)
DEVICE BC40F
LOT #'S: FS4
FQ8
FB3

TEMP 100°C

IC (A) >	0.6	8	16	32	50
1	0.694	1.127	1.418	1.925	2.46
2	0.678	1.114	1.413	1.94	2.5
3	0.677	1.097	1.382	1.885	2.4
4	0.685	1.112	1.399	1.899	2.42
5	0.711	1.178	1.485	2.01	2.57
6	0.743	1.263	1.604	2.19	2.83
7	0.732	1.223	1.541	2.09	2.67
8	0.723	1.206	1.524	2.08	2.66
9	0.746	1.264	1.602	2.19	2.81
10	0.731	1.223	1.543	2.09	2.67
11	0.694	1.157	1.47	2.01	2.6
12	0.714	1.193	1.513	2.06	2.65
13	0.714	1.189	1.506	2.05	2.65
14	0.7	1.147	1.512	1.98	2.55
1 5	0.706	1.1 51	1.47	1.99	2.56
MINIMUM	0.677	1.097	1.382	1.885	2.400
MAXIMUM	0.746	1.264	1.604	2.190	2.830
AVERAGE	0.71	1.176	1.492	2.026	2.600
STD	0.021	0.051	0.066	0.091	0.122
AVG + 6STD	0.838	1.484	1.888	2.572	3.331
AVG-6STD	0.581	0.868	1.097	1.480	1.869

Table A.1. Conduction Characteristics of a Population of IGBTs from three different slots

To calculate a and b the model is manipulated as follows:

$V_{ce} = V_t + a\, I^b$
$V_{ce} - V_t = a\, I^b$
$\ln (V_{ce} - V_t) = \ln a + b \ln I$

This last expression is a straight line fit to the natural logarithms of I and $V_{ce} - V_t$.

Using the least square method, the values of ln a and b can be obtained by the following formulas:

$$b = \frac{n\sum\left\{(\ln)_i \, x\left[\ln\left(V_{CE} - V_t\right)\right]_i\right\} - \left[\sum(\ln I)_i\right] x \sum\left[\ln\left(V_{CE} - V_t\right)_i\right]}{n\sum(\ln I)_i^2 - \left[\sum(\ln I)_i\right]^2}$$

$$\ln = \frac{\sum \ln\left(V_{CE} - V_t\right)_i}{n} - b\frac{\sum(\ln I)_i}{n}$$

$$a = {}_e\ln_a$$

The value of V_t has been defined as the voltage drop at a current density of approximately 0.035 a/mm2, which, for the IGBT of Table A.1, corresponds to 0.6A. With this in mind, Table A.2 shows the calculations and the error.

A	V	V cal	V-Vcal	Error	V-vt	ln(V-Vt)	ln(I)	(XiYi)
0.60	0.71	0.77	-0.0645	-9.08%				
8.00	1.18	1.17	0.0026	0.22%	0.4660	-0.7636	2.0794	-1.5878
16.00	1.49	1.50	-0.0035	-0.23%	0.7820	-0.2459	2.7726	-0.6818
32.00	2.03	2.04	0.0155	-0.76%	1.3160	0.2746	3.4657	0.9517
50.00	2.60	2.58	0.0198	0.76%	1.8900	0.6366	3.9120	2.4903
				n =	4	-0.0983	12.2298	1.1724
						Sum Yi	Sum Xi	Sum XiYi
						Varian	0.4837	

b = 0.7614 ln a = -2.3524

a = 0.0951

Table A.2. Calculation of the Voltage Drop Parameters

The values entered in Table A.2 correspond to the averages of Table A.1. If the average-plus-three-sigma values had been entered, the model parameters would correspond to the data entered.

This process can be repeated for different temperatures and a set of model parameters would be obtained. Each element of the set provides an accurate model of the specific IGBT at a specific temperature.

Temp	a	a (calc)	Error	b	b (calc)	Error	Vt	Vt Calc	Error
25		0.0778			0.7391			0.85	
50	0.0814	0.0832	-2.23%	0.7523	0.7469	0.72%	0.80	0.80	-0.40%
75	0.0899	0.0886	1.27%	0.7496	0.754-	-0.69%	0.76	0.76	0.28%
100	0.0951	0.0941	1.13%	0.7614	0.7626	-0.16%	0.71	0.71	0.34%
125	0.1009	0.0995	1.40%	0.7668	0.7704	-0.48%	0.66	0.66	0.26%
150	0.103	0.1049	-1.86%	0.7829	0.7733	0.59%	0.61	0.61	-0.49%
500	0.4703			3.8129			3.5380	6.83E-02	
(XiYi) =	48.3873		(XiYi) =	383.2507			(XiYi) = 341.7250		
Sxi^2 =	56250								

a = a1 + a2*T a1 = 0.0724 a2 = 2.17E-04
b = b1 + B2*T b1 = 0.7313 b2 = 3.13E-04
Vt = Vt1 + Vt2*T Vt1 = 0.9008 Vt2 = -1.9E-03

Table A.3. Linear Regression for Temperature Coefficient of Voltage Drop Parameters

Unfortunately, in most design problems the junction temperature is the unknown (see Figure 11, 18 and 20) and fixed temperature parameters, like those shown in Table A.2 are not useful.

Assuming that these parameters have a simple temperature dependence, a linear regression has been done, as shown in Table A.3.

This provides the expression of the voltage drop as a function of current and temperature with which we have analyzed the operating conditions of Figure 11, 18 and 20. As shown in Table A.3 the accuracy of the parameter obtained with the linear regression is within few Percent.

The switching model parameters are obtained in a very similar way, using the same type of expression, except for the threshold. The accuracy of the linear regression to calculate the temperature coefficients is acceptable for some IGBTs, particularly the Standard and the Fast, while an exponential regression is more accurate for the Ultrafast. For the sake of simplicity, only the linear regression is listed in Tables I and III.

APPENDIX 2: Equations to identify the operating point of paralleled IGBTs.

In the system described in sections IX.B.1 and B.2 the parameters listed in the two top boxes of Figure 20 are known, while those listed in the third box have to be calculated. The two fundamental constraints that determine the current distribution between the IGBTs are the following:

* voltage drop across the two IGBTs is the same;
* the sum of the currents is the same and equal to the load current.

Imposing these two constraints to the voltage drop model we obtain the following:

$$V_{CE-1} = V_{CE-2}$$

$$V_{T-1} + a_{-1} I_{-1}^{(b_{-2}1)} = V_{T-2} + a_{-2} I_{-2}^{(b_{-2})}$$

$$\left(\frac{I_L}{2} + \Delta I\right) = \exp\left\{\frac{1}{b_{-2}} \ln\left[\frac{V_{T-1} - V_{T-2}}{a_{-2}} + \frac{a_{-1}}{q_{-2}}\left(\frac{I_L}{2}\right)^{(b-1)}\right]\right\}$$

where the index after the dash identifies the IGBT, while the index before the dash identifies the model parameter, e.g. VTI 2 identifies the first threshold parameter (see Figure 18) of the second IGBT.

Since the key unknowns are ΔI, T l and T 2, we need two additional expressions, which can be obtained from the thermal equations:

$$T_{-2} = T_A + I_L\left(V_{T-2} - a_{-2}I_{-2}^{(b-2)}\right)\theta_{SA} + \left(I_{-2}V_{T-2} + a_{-2}I_{-2}^{b-2+1}\right)\theta_{JS}$$

$$T_{-1} = T_A + I_L\left(V_{T-2} + a_{-2}I_{-2}^{b-2}\right)\theta_{SA} + \left[I\left(V_{T-2} + a_{-2}I^{(b-2)}\right) - \left(I_{-2}V_{T-2} + a_{-2}I_{-2}^{b+1}\right)\right]\theta_{JS}$$

The first of these expression is calculated in the cell shown on the right of the Operating Conditions box with the "solve for" function, with the parameters shown in the box. Successive calculations of current and temperature yield the final result. For these calculations the following simplification was made in the first expression:

$$V_{T-1} - V_{T-2} \cong (V_{T2-1} - V_{T2-2})(T_1 - T_2)$$

of minimal impact on overall accuracy.

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APPLICATION NOTES
PUBLISHED BY INTERNATIONAL RECTIFIER, 233 KANSAS STREET, EL SEGUNDO, CA 90245, (310) 322-3331

AN-989

The HEXFRED™ Ultrafast Diode in Power Switching Circuits

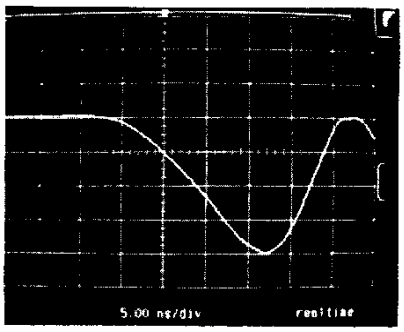
(HEXFRED is a trademark of International Rectifier)

by Y. Khersonsky, M. Robinson, D. Gutierrez

Introduction

This application note describes the benefits of using the International Rectifier 600 volt, 15 amp, ultra-fast recovery epitaxial diode (FRED) in power switching circuits. This device, the first from a broad product family covering a wide range of current and voltage ratings, is based on the new HEXFRED technology developed by International Rectifier. Diodes produced using this technology exhibit extremely fast reverse recovery times (t_{rr}), very low values of reverse recovery current (I_{RRM}), unusually "soft" recovery characteristics, and guaranteed avalanche (see Figures 1a and 1b).

The essentials of reverse recovery are covered, followed by laboratory measurements taken from an IGBT chopper circuit. Finally, guidelines are provided for calculating power losses in ultra-fast rectifiers.



I_F = 1A
diF/dt = 200A/µs
T_J = 25°C
V_R = 30V
t_{rr} = 19ns
I_{RRM} = 3A
Q_{rr} = 28.5nC
di(rec)M/dt = 570A/µs

Figure 1(a). Oscilloscope display of recovery characteristic for the HFA15TB60 HEXFRED

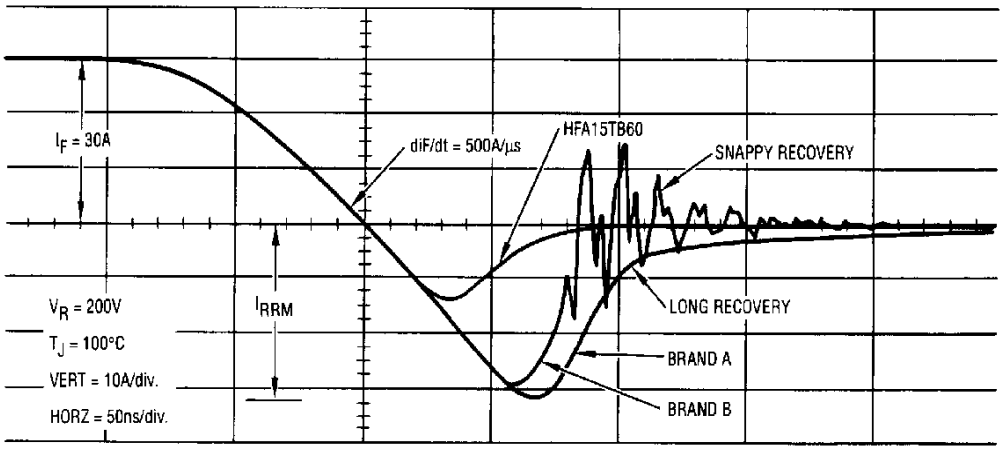


Figure 1(b). Typical t_{rr} comparison results of the HFA15TB60 HEXFRED and conventional FREDs

HEXFRED Technology

HEXFRED stands for HEXagonal Ultra-Fast Recovery Epitaxial Diode. The HEXFRED technology incorporates special high voltage epitaxial silicon, a hexagonal cellular structure, planar design, and a proprietary minority carrier lifetime control process. The result is a startling improvement in recovery characteristics when compared to conventional ultrafast diodes.

HEXFREDs are pin-for-pin compatible with conventional diodes and can therefore be used as direct replacements with no design modifications. However, the designer can achieve the greatest cost benefits and efficiency improvements by taking full advantage of both the low reverse recovery current which will cause the power switches to run at much lower temperatures, and the ultra-soft recovery which will result in lower RFI, EMI, and reduction or elimination of snubber components.

Diode Recovery Characteristics

In any power conversion equipment there are usually more diodes than transistors. They are typically labeled as "catch diodes," "flyback diodes," "freewheeling diodes," and "clamp diodes." A detailed knowledge of how "fast" and how "soft" the diode recovery should be is necessary to properly design an efficient switching circuit. By properly choosing the optimum diode the designer can significantly reduce losses in the power switch, the diode, and many other circuit elements. Additionally, the optimum diode will reduce voltage spikes, RFI and EMI caused by snappy diodes allowing for the reduction or even the elimination of snubber circuits.

The Cause of Recovery Losses

All PN junction diodes, when conducting forward current will store charge in the form of excess minority carriers. Minority carrier injection is the mechanism for conductivity modulation which results in lowering the forward voltage drop (V_F), and in this sense it is beneficial. However, when the circuit commutates the diode, the stored charge must be completely extracted or neutralized before the diode is said to be "off." The time it takes for this to occur is defined as reverse recovery time (t_{rr}). The recovery time is composed of two distinct intervals, t_a and t_b as shown in Figure 2. More will be said about t_a and t_b later.

A diode conducting forward current (I_F) has a corresponding forward voltage drop (V_F) and an amount of stored charge (Q_O) which is proportional to I_F. When the diode current commutates, a portion of the internal stored charge is quickly neutralized via internal recombination. The remaining stored charge (Q_{rr}) is reduced by continued recombination and by reverse current (I_{RR}) circulating through the diode and associated circuit elements.

When the power switch commutates the diode, forward current (I_F) decreases at a rate (diF/dt) determined by the circuit inductance and the applied voltage. When the diode current decreases to zero, Q_{rr} causes reverse current (I_{RR}) to flow until it is fully depleted. It is this unwanted and unavoidable reverse current that causes increased power dissipation in the power switch (IGBT, MOSFET, etc).

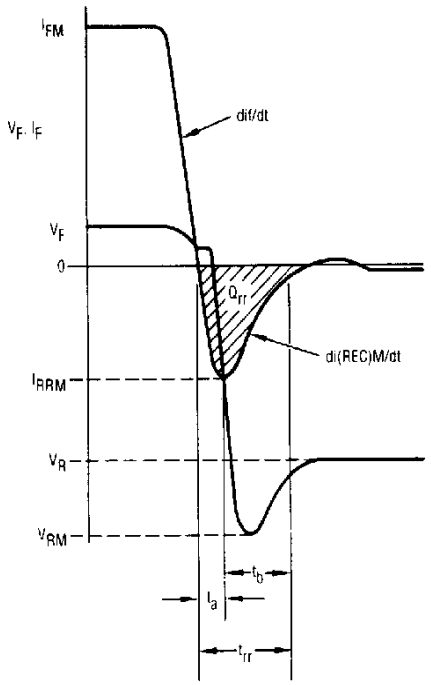


Figure 2. Diode current and voltage waveform definitions

t_{rr}

The total time required to deplete the stored charge is defined as t_{rr} where $t_{rr} = t_a + t_b$. The t_{rr} of a device is generally used as the measure of its switching speed and will determine it's suitability for a given application. The t_{rr} specifications on power diodes given at one amp are for comparison purposes only. International Rectifier HEXFREDs are specified with both typical and maximum t_{rr} at rated current and two times rated current, as well as at 25°C and 125°C. See Figures 3 and 4.

t_a

The time required for the diode reverse current (I_{RR}) to increase (shown in Figure 2) from zero to its peak (I_{RRM}) negative value is defined as "t_a." During this portion of t_{rr}, the voltage drop across the diode is still positive; however, it is less than the value of V_f during forward conduction. The current flowing during t_a can be significant, especially in conventional diodes. Thus, due to the low voltage across the diode, power dissipation in the diode during t_a is minimal. However, power dissipation in the switch may be very high because it carries the full diode reverse current while it supports the full voltage of the circuit. In short, a diode with lower

reverse current will allow the power switch to operate at a lower temperature. In some designs, this savings may result in using a smaller, lower cost IGBT or MOSFET switch.

t_b

The time required for t_{rr} to fall from its peak value (I_{RRM}) to zero (shown in Figure 2) is defined as "t_b." During this time the voltage across the diode goes from a small positive value to the full applied reverse voltage. Because there is simultaneous reverse current flow through the diode and high voltage across it during t_b, there will be significant power dissipation in the diode. Intuitively one would reason that to minimize the power loss during t_b one should use the diode with the shortest t_b. However, as will be shown, the actual shape of the t_b curve is more critical than the absolute value of t_b.

Q_{rr}

The total reverse recovered charge (Q_{rr}) is defined as the area under the current-time curve during t_{rr}. This charge represents the energy that must be dissipated in the power switching side of the circuit. International Rectifier HEXFRED data sheets provide typical and maximum values for Q_{rr} at worst case operating conditions (see Figures 5 and 6).

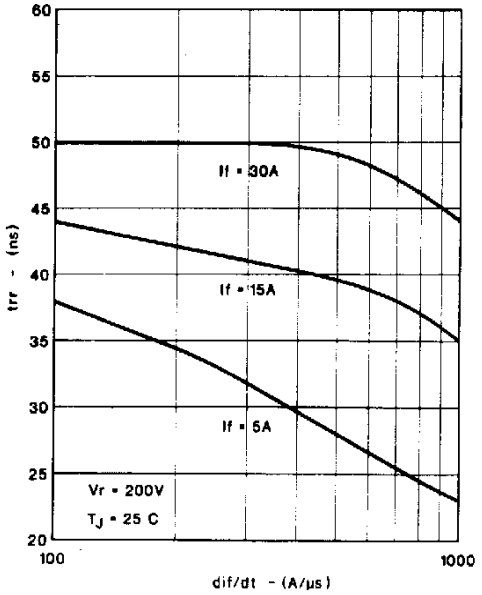


Figure 3. Typical Reverse Recovery Time vs. dif/dt

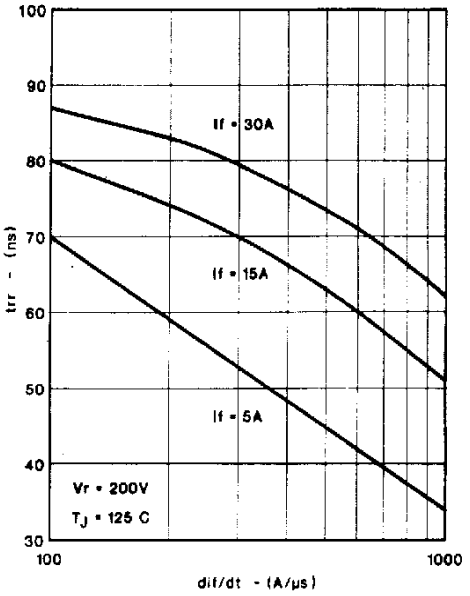


Figure 4. Typical Reverse Recovery Time vs. dif/dt

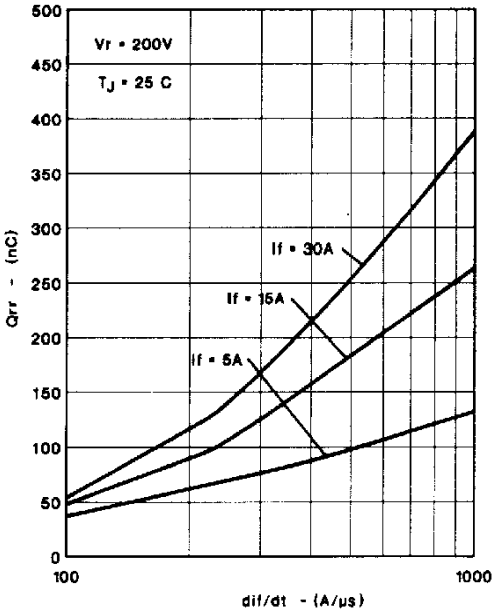


Figure 5. Typical Stored Charge vs. dif/dt

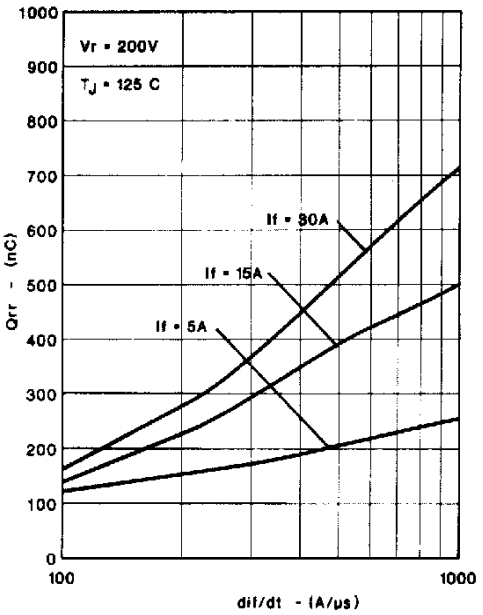


Figure 6. Typical Stored Charge vs. dif/dt

Softness, di(rec)M/dt, and t_b/t_a

When specifying *softness,* semiconductor manufacturers generally use either the ratio of t_b/t_a (softness factor) or the peak slope of t_b. The latter called di(rec)M/dt is the more useful in predicting the magnitude of the voltage spikes that will be generated by the FRED device.

Using the ratio of t_b/t_a as the softness factor can be misleading. Ultra-fast recovery epitaxial diodes with the same softness ratio may cause different values of RFI and over-voltage spikes. Figure 7 shows the waveforms of three FRED devices all with the same ratio of t_b/t_a. Notice that each FRED has a different softness and a different di(rec)M/dt. This clearly illustrates that t_b/t_a used as a softness factor is misleading. Further more, armed with the knowledge of di(rec)M/dt and the inductance of the circuit one can predict the magnitude of the voltage spike:

$$V_{RM} = V_R + L \bullet \text{di(rec)M/dt}$$

Where L is the total circuit inductance.

Care should be taken since the voltage spike resulting from a snappy recovery may exceed the voltage rating of the power switch.

International Rectifier specifies its HEXFRED typical values of di(rec)M/dt at the same test conditions as t_{rr} as shown in Figures 8 and 9.

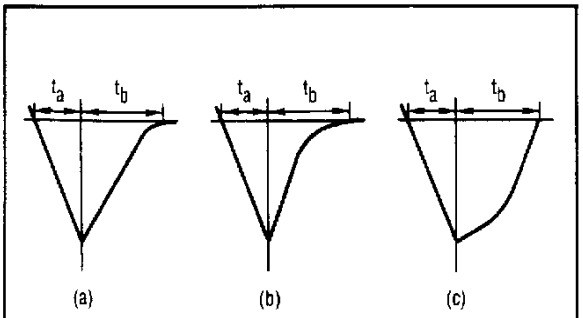


Figure 7. Different diode di(rec)M/dt rates for same softness factor

The HEXFRED vs. Conventional Diodes in a Chopper Circuit

The 15 Amp, 600 Volt TO-220 HEXFRED, part number HFA15TB60, was compared to conventional diodes from two manufacturers. All diodes were rated at 600V and 12 to 15 amps. All were packaged in the industry standard TO-220 plastic case.

Two comparisons were performed. One was simply to measure the devices' dynamic performance in an IGBT chopper circuit (Figure 10) in order to establish a baseline. Table 1 reflects this data.

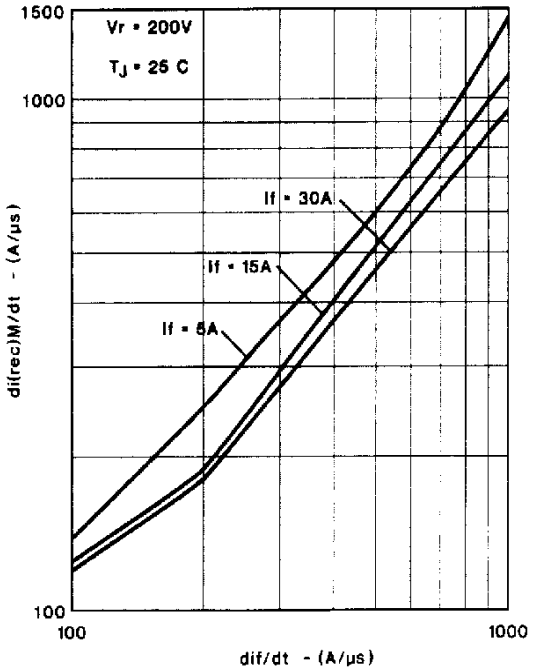


Figure 8. Typical di(rec)M/dt vs. dif/dt

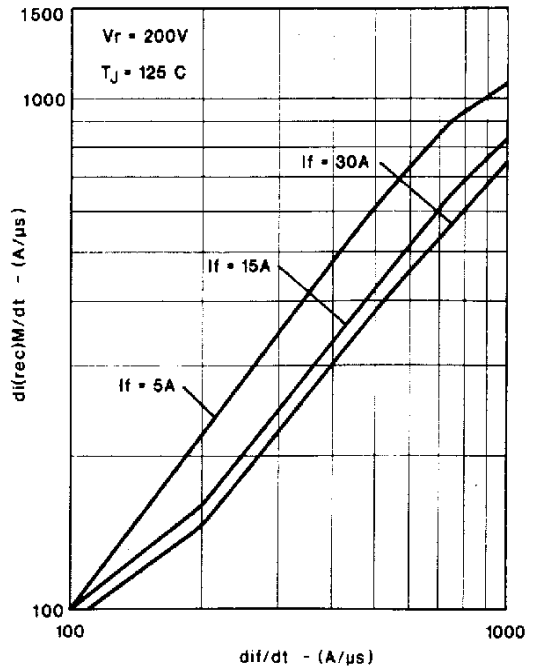


Figure 9. Typical di(rec)M/dt vs. dif/dt

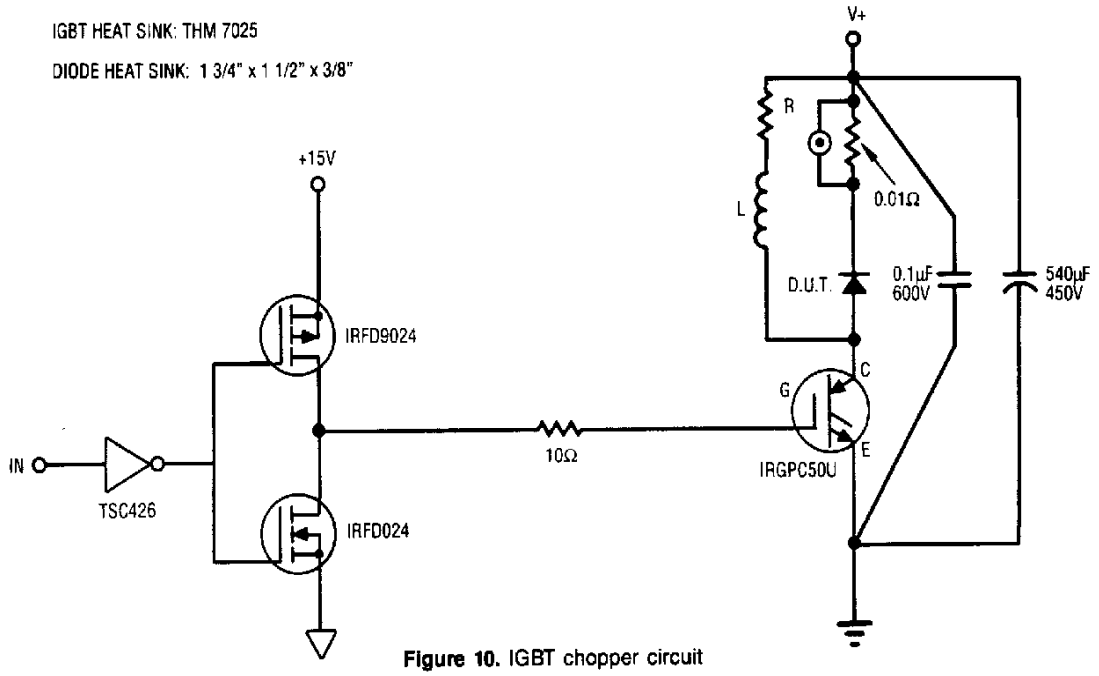


Figure 10. IGBT chopper circuit

Table 1. Baseline Comparisons

FRED Devices	t_{rr} (nsec)	Softness di(rec)M/dt (A/μs)	I_{RRM} (Amp)	t_{rr} (nsec)	Softness di(rec)M/dt (A/μs)	I_{RRM} (Amp)
	@ 25°C	@ 25°C	@ 25°C	@ 125°C	@ 125°C	@125°C
HFA15TB60	65	645	27	75	825	27
Brand A	105	1400	54	140	1480	69
Brand B	85	2210	48	120	2300	61

Conditions:
V_R = 400V L = 100μH
I_F = 20 Amps R = 0Ω
diF/dt = 1200A/μs
T_j = as shown on table

The most significant difference between these ultrafast diodes are:

1) The HEXFRED has less than 1/2 of the reverse recovery current when compared to conventional ultrafast diodes rated at similar voltage and forward current.

2) t_{rr} on the conventional diodes increased by as much as 41% with temperature. The HEXFRED increased only 15%.

3) HEXFRED softness (di(rec)M/dt) was twice as soft as the diode from Brand B, and three times as soft as Brand A which is a very popular but snappy diode.

The second comparison was to measure power losses via case temperature, in the same circuit.

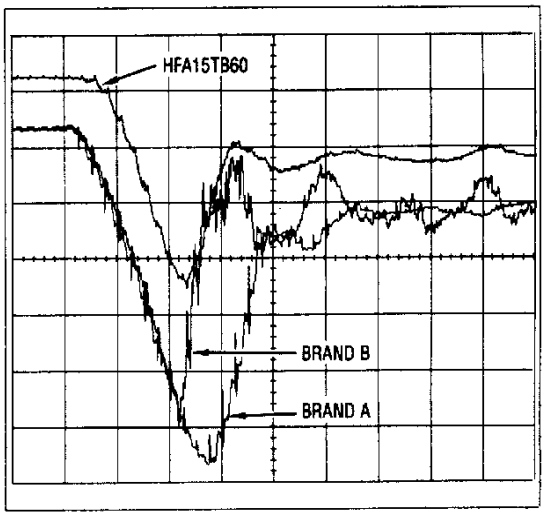


Figure 11. Oscillogram of diode current waveforms in IGBT chopper circuit at 10 kHz. (Traces are offset for clarity)

Each diode was mounted with the same screw on the same aluminum heatsink 1.75" x 1.5" x 0.375". The IRGPC50U was used in every test as the IGBT switch. The IGBT was mounted on a standard heatsink (THM 7025). Both heatsinks were standing in free air in the vertical position.

Case temperature was measured separately for the diode and the transistor. Each thermocouple was attached to the identical location on the heatsink.

Results of the chopper circuit test at switching frequency 10 kHz, are shown in Table 2. An oscillogram of the current waveforms for all three devices is shown in Figure 11.

Table 2. Switching Frequency @ 10 kHz

FRED Devices	Softness di(rec)M/dt (A/μs)	Diode I_{RRM} (Amp)	Diode T_C (°C)	IGBT T_C (°C)
HFA15TB60	998	15	65	37.5
Brand A	1405	23	78.5	41.5
Brand B	2210	38	67	48

Test conditions for each ultra-fast recovery diode test were maintained unchanged as follows:

Load current 6 Amp dc, transistor duty cycle 50%;
Load inductance 8000μH, V_R = 200V.
R = 15Ω, diF/dt = 650A/μs

In this case, the most noticeable difference is not so much in the temperature of the diode but in the temperature of the IGBT. This is attributed to the low reverse recovery current of the HFA15TB60 HEXFRED.

Finally, the operating frequency of the circuit was increased from 10 kHz to 20 kHz. In this test the HEXFRED caused the IGBT to run from 10% to 28% cooler. Even more noticeable was the amount of noise generated by Brand B (see Figure 12). No snubber was used.

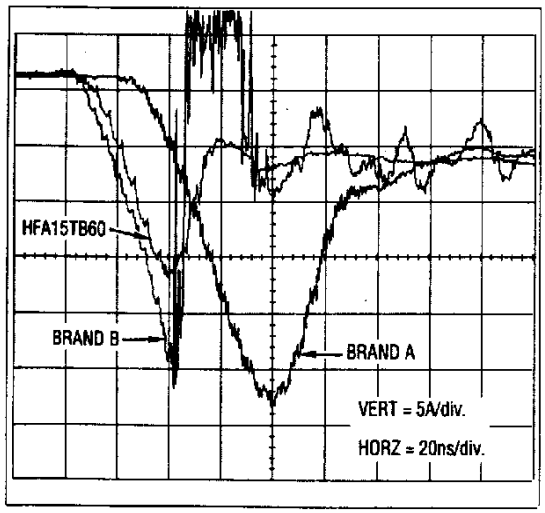


Figure 12. Oscillogram of diode current waveforms in IGBT chopper circuit at 20 kHz. (Traces are offset for clarity)

Table 3. Switching Frequency @ 20 kHz

FRED Devices	Softness di(rec)M/dt (A/μs)	Diode I_{RRM} (Amp)	Diode T_C (°C)	IGBT T_C (°C)
HFA15TB60	998	15	66.5	64.3
Brand A	1405	23	81.5	71.5
Brand B	2210	38	67	81

At 20 kHz, the difference becomes even more noticeable. Snappy Brand B caused the IGBT to run 16.7°C hotter.

Calculating Losses in Switching Circuit

From the foregoing discussion and product comparison it is evident that the diode in a switching circuit will play a major role in the overall performance of the circuit. Modern switching circuits, operating at high frequency are very sensitive to switching losses in the IGBT, MOSFET, etc. switch and in the associated diode(s).

Conduction and off-state losses in the diode are generally easy to predict using straight forward calculations. These losses, although significant, usually do not cause any surprises and they do not have any undue influence on the associated power switch.

This is not the case with diode switching losses as they usually have a major influence on the power dissipation and junction temperature levels of both the diode and the power switch.

Total power losses due to the diode can be calculated as:

$$P_R = P_{con} + P_{off} + P_{sw} \quad (1)$$

Where:

P_{con} = conduction loss $\quad P_{con} = V_F I_F \frac{t_{on}}{T}$ (2)

P_{off} = off-state loss $\quad P_{off} = V_R \bullet I_R \bullet \frac{t_{off}}{T}$ (3)

P_{sw} = switching power loss due to reverse recovery $\quad P_{sw} = E_{rr} \bullet f$ (4)

E_{rr} = switching energy loss due to reverse recovery

f = operating frequency

P_{con} and P_{off} are calculated using data sheet values and circuit operating parameters;

CIRCUIT PARAMETERS	DATA SHEET VALUES
t_{on} = diode on-time	V_F @ I_F @ T_j
t_{off} = diode off-time	I_R @ V_R @ T_j
T = switching period	
V_r = applied voltage	
I_f = forward current	

A more accurate estimation of P_{con} can be made if the exact current wave shape and the diode junction temperature are known (Ref. 1 & 2).

Switching losses, P_{sw}, are more difficult to determine since their calculation requires a good understanding of the diode dynamic recovery characteristics. In a typical half-bridge or buck regulator the total charge associated with diode recovery represents energy that will be dissipated among various components of the circuit and can be expressed as:

$$E_{rr} = \int_0^{t_{rr}} I(t) \bullet V(t)\, dt \quad (5)$$

Assuming linear V and I transition (Ref. 1 & 2), a practical diode with finite t_a, t_b and I_{RRM} will cause switching energy dissipation in the transistor, and is calculated as:

$$E_t = V_R \left(\frac{I_{RRM}}{2} t_a + \frac{I_{RRM}}{4} t_b \right) \quad (6)$$

Energy dissipated in the diode is calculated as:

$$E_d = \frac{V_r \, I_{RRM} \, t_b}{4} \quad (7)$$

Total switching losses due to diode reverse recovery are:

$$E_{sw} = (E_t + E_d) \quad (8)$$

DETERMINING t_a, t_b, t_{rr} and I_{RRM}:

In order to use equations 6 and 7 it is necessary to first determine the values for reverse recovery parameters t_a, t_b, t_{rr} and I_{RRM} at the applicable operating conditions. The HEXFRED data sheet contains the appropriate dynamic performance curves that are used for this purpose. The procedure used here is adequate for a good first order approximation.

1. Ascertain that the operating conditions in question are not the same as those specified in the data sheet for t_{rr} 1, 2 or 3.

2. Use data sheet typical characteristic curves for t_{rr} and I_{RRM} to determine values that correspond to the operating conditions in question. For conditions that are not graphed, use linear interpolation.

3. Use t_{rr} and I_{RRM} calculated values to determine t_a and t_b.

4. Use calculated values of t_a, t_b, t_{rr} and I_{RRM} in equations 6 and 7.

Example:

Determine t_a, t_b, t_{rr} and I_{RRM} for the International Rectifier HFA15TB60 operating at;

$I_F = 10$ A., dif/dt = 800A/μ
$V_R = 200$V., $T_j = 125°C$

1a. Using t_{rr} vs dif/dt @ 125°C curves of the data sheet and interpolating, determine t_{rr} at $I_f = 10$A and dif/dt = 800A/μs.

$$t_{rr(10)} = t_{rr(5)} + \frac{t_{rr(15)} - t_{rr(5)}}{I_{F(15)} - I_{F(5)}} (I_{F(10)} - I_{F(5)})$$

$$t_{rr} = 37 + \frac{55 - 37}{15 - 5} (10 - 5) = 46\text{ns}$$

b. Using I_{rr} vs dif/dt @ 125°C curves of the data sheet and interpolating; determine I_{RRM}.

$$I_{RRM(10)} = I_{RRM(5)} + \frac{I_{RRM(15)} - I_{RRM(5)}}{I_{F(15)} - I_{F(5)}} (I_{F(10)} - I_{F(5)})$$

$$I_{RRM} = 13 + \frac{17 - 13}{15 - 5} (10 - 5) = 15\text{A}$$

2. Determine t_a and t_b.

$$t_a = \frac{I_{RRM}}{\frac{dI_F}{dt}} = \frac{15}{800} = 18.75\ \eta\text{s} \quad (9)$$

$$t_b = t_{rr} - t_a = 46 - 18.75 = 27.25\eta\text{s} \quad (10)$$

3. Substitute values in equations 5 and 6;

Energy loss in transistor;

$$E_t = 200 \left(\frac{15}{2} 18.75 + \frac{15}{4} 27.25 \right) = 48.56\ \mu\text{J}$$

Energy loss in diode;

$$E_d = \frac{200 \bullet 15 \bullet 27.25}{4} = 20.44\ \mu\text{J}$$

Total losses due to the diode;

$$E_{sw} = E_d + E_t = 69\ \mu\text{J}$$

Alternatively;

$$E_{sw} = V_r \times Q_{rr} \quad (11)$$

In this case, Q_{rr} at $I_f = 10$A would be determined from the data sheet curves for Q_{rr} vs dif/dt @ 125°C using interpolation as before:

$$Q_{rr(10)} = Q_{rr(5)} + \frac{Q_{rr(15)} - Q_{rr(5)}}{I_{F(15)} - I_{F(5)}} \quad I_{F(10)} - I_{F(5)}$$

$$Q_{rr} = 220 + \frac{460 - 220}{15 - 5} (10 - 5) = 340\eta\text{C}$$

Substituting in equation (11):

$$E_{sw} = 200 \bullet 340 \bullet 10^{-9} = 68\mu\text{J}$$

In both cases the result is virtually the same and either method may be used.

Summary

It has been shown that the new HEXFRED technology exhibits unusually low reverse recovery current, very fast t_{rr}, and exceptional softness when compared to conventional ultrafast diodes. This improved device performance translates into increased efficiency and reduced snubbing, as well as reduced RFI and EMI in power conversion circuits.

Test results showed that the major beneficiary of the reduced recovery current and the soft recovery waveform was the MOSFET or IGBT switch which saw significantly reduced operating temperatures, caused simply by replacing the conventional diode with the International Rectifier HEXFRED ultra-fast recovery epitaxial diode.

An example was provided for calculating the total switching loss in both the diode and the switching transistor, in this case an IGBT. □

References

(1) International Rectifier Application Note AN-967, "Using HEXFET III in PWM Inverters for Motor Drives and UPS Systems."

(2) International Rectifier Application Note AN-983, "IGBT Characteristics and Applications."

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Printed in U.S.A. 0492-M10

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IGBT Characteristics

(HEXFET® is a trademark of International Rectifier)

Topics covered:

How the IGBT complements the MOSFET
Silicon structure and equivalent circuit
Conduction characteristics and "switchback"
Switching characteristics
Latching
Safe Operating Area
Transconductance
How to read the data sheet
Families of IGBTs

1. HOW THE IGBT COMPLEMENTS THE POWER MOSFET

Switching speed, peak current capability, ease of drive, wide SOA, avalanche and dv/dt capability have made power MOSFETs the logical choice in new power electronic designs. These advantages, a natural consequence of being majority carrier devices, are partly mitigated by their conduction characteristics which are strongly dependent on temperature and voltage rating.

Furthermore, as the voltage rating goes up, the inherent reverse diode displays increasing Q_{rr} and T_{rr} which leads to increasing switching losses.

IGBTs on the other hand, being minority carrier devices, have superior conduction characteristics, while sharing many of the appealing features of power MOSFETs such as ease of drive, wide SOA, peak current capability and ruggedness. Generally speaking, the switching speed of an IGBT is inferior to that of power MOSFETs. However, as detailed in INT-990 Sec VIII, a new line of IGBTs from International Rectifier has switching characteristics that are very close to those of power MOSFETs, without sacrificing the much superior conduction characteristics.

The absence of the integral reverse diode gives the user the flexibility of choosing an external fast recovery diode to match a specific requirement or to purchase a "co-pak", i.e. an IGBT and a diode in the same package. The lack of an integral diode can be an advantage or a disadvantage, depending on the frequency of operation, cost of diodes, current requirement, etc.

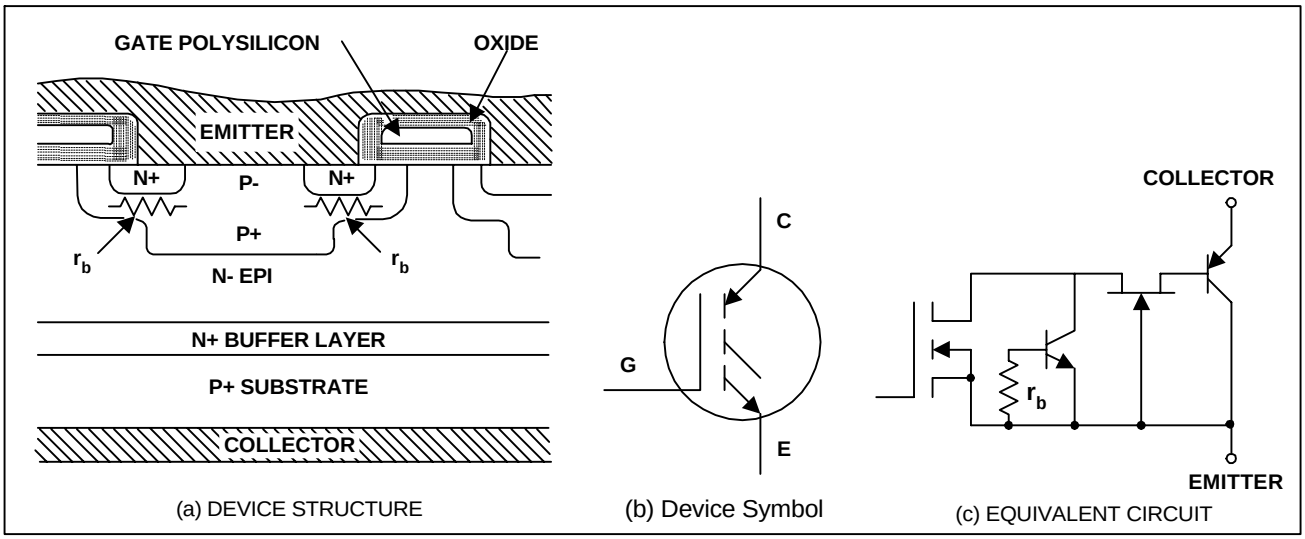


Figure 1. Silicon cross-section of an IGBT with its equivalent circuit and symbol (N-Channel, enhancement mode). The terminal called collector is, actually, the emitter of the PNP. In spite of its similarity to the cross-section of a power MOSFET, operation of the two transistors is fundamentally different, the IGBT being a minority carrier device.

2. SILICON STRUCTURE AND EQUIVALENT CIRCUIT

Except for the P+ substrate, the silicon cross-section of an IGBT (Figure 1) is virtually identical to that of a power MOSFET. Both devices share a similar polysilicon gate structure and P wells with N+ source contacts. In both devices the N- type material under the P wells is sized in thickness and resistivity to sustain the full voltage rating of the device.

However, in spite of the many similarities, the physical operation of the IGBT is closer to that of a bipolar transistor than to that of a power MOSFET. This is due to the P+ substrate which is responsible for the minority carrier injection into the N-region and the resulting conductivity modulation. In a power MOSFET, which does not benefit from conductivity modulation, a significant share of the conduction losses occur in the N-region, typically 70% in a 500V device.

As shown in the equivalent circuit of Figure 1, the IGBT consists of a PNP driven by an N-Channel MOSFET in a pseudo-Darlington configuration. The JFET has been included in the equivalent circuit to represent the contriction in the flow of current between adjacent P-wells. The cell density of the MOSFET structure is higher than that of a high-voltage, comparable technology MOSFET and, consequently, has better Resistance-Area product.

The base region of the PNP is not brought out and the emitter-base PN junction, spanning the entire extension of the wafer cannot be terminated nor passivated. This influences the turn-off and reverse blocking behavior of the IGBT, as will be explained later. The breakdown voltage of this junction is about 20V and is shown in the IGBT symbol as an unconnected terminal (Figure 1).

3. CONDUCTION CHARACTERISTICS

As it is apparent from the equivalent circuit, the voltage drop across the IGBT is the sum of two components: a diode drop across the P-N junction and the voltage drop across the driving MOSFET. Thus, unlike the power MOSFET, the on-state voltage drop across an IGBT never goes below a diode threshold. The voltage drop across the driving MOSFET, on the other hand, has one characteristic that is typical of all low voltage MOSFETs: it is sensitive to gate drive voltage. This is apparent from Figures 12 and 13 where, for currents that are close to their rated value, an increase in gate voltage causes a reduction in collector-to-emitter voltage. This is due to the fact that, within its operating range, the gain of the PNP increases with current and an increase in gate voltage causes an increase in channel current, hence a reduction in voltage drop across the PNP. This is quite different from the behavior of a high voltage power MOSFET that is largely insensitive to gate voltage.

As the final stage of a pseudo-Darlington, the PNP is never in heavy saturation and its voltage drop is higher than what could be obtained from the same PNP in heavy saturation. It should be noted, however, that the emitter of an IGBT covers the entire area of the die, hence its injection efficiency and conduction drop are much superior to that of a bipolar transistor of the same size.

Two options are available to the device designer to decrease the conduction drop:

1. Reduce the on-resistance of the MOSFET. This can be done by increasing the die size and/or the cell density.

2. Increase the gain of the PNP. As explained later, this option is limited by latch-up considerations and voltage withstanding capability.

International Rectifier has been pursuing the optimization of the MOSFET component of the IGBT to the point where its devices can be correctly referred to as a "conductivity modulated MOSFET" with its characteristic features of high speed, low voltage drop and efficient silicon utilization. Other semiconductor companies, on the other hand, have concentrated on the optimization of the bipolar part and the resulting product should be more correctly referred to as a "MOSFET-driven transistor" with a different set of characteristics.

The dramatic impact of conductivity modulation on voltage drop can be seen from Figure 2 which compares a HEXFET® power MOSFET and an IGBT of the same die size. Temperature dependence, very significant in a power MOSFET, is minimal in an IGBT, just enough to ensure current sharing of paralleled devices at high current levels under steady state conditions, as shown in Figure 14 for the IRGBC20U. This same figure shows that the temperature dependence of the voltage drops is different at different current levels. This is because the diode component of this drop has a temperature coefficient that is initially negative becoming positive at higher current levels. The MOSFET component, on the other hand, is positive. The problem is made more complex by the fact that these two components are weighted differently at different current and temperatures.

In addition to reducing the voltage drop and its temperature coefficient, conductivity modulation virtually eliminates its dependence on the voltage rating. This is shown in Table I, where the conduction drops of four IGBTs of different voltage ratings are compared with those of HEXFET®s at the same current density. A common misconception is that power MOSFETs exhibit a voltage dependence of the $R_{DS(on)}$ of the following type:

$$R = R_O V^{\alpha} \text{ with } \alpha = 2.5,$$

i.e., the on-resistance increases with the voltage rating at a higher rate than a square law. In reality, assuming that a power law is a true representation of the underlying physical phenomena, the correct value would be ≈ 1.6, as can be easily verified from the data sheets of any manufacturer. These data sheets will also contradict the common misconception that power MOSFETs have better silicon utilization at low voltage. In actual fact they achieve their highest power handling capability per unit area between 400V and 600V, even if they are unbeatable at low voltages, on account of their resistive voltage drop. The voltage drop of a conductivity modulated device with minority lifetime killing may exhibit a peculiar behavior frequently referred to as 'switchback': the voltage drop at low current and low temperature is higher than expected, suddenly dropping to its expected value if current or temperature are increased. The term comes from the fact that, when measuring voltage drop with a curve tracer, the trace suddenly 'switches' to the left of the screen as the current increases. This behavior is ascribed to lifetime killing which, in so far as it facilitates recombination, delays the onset of conductivity modulation. Hence, the voltage drop for current levels below conductivity modulation is higher than for a somewhat higher collector current, after conductivity modulation is established. This phenomenon is one of the causes of the "forward recovery" of fast (reverse recovery) diodes and of higher values of latching current in minority lifetime killed thyristors. A trace of this phenomenon can be seen in the "bump" in the $V_{CE(Sat)}$ portion of Figure 12. Notice that the bump disappears in Figure 13 because temperature increases the lifetime of the charges and speeds up the onset of conductivity modulation. Notice, also, that only the Ultrafast IGBTs exhibit this phenomenon, because of higher levels of lifetime killing.

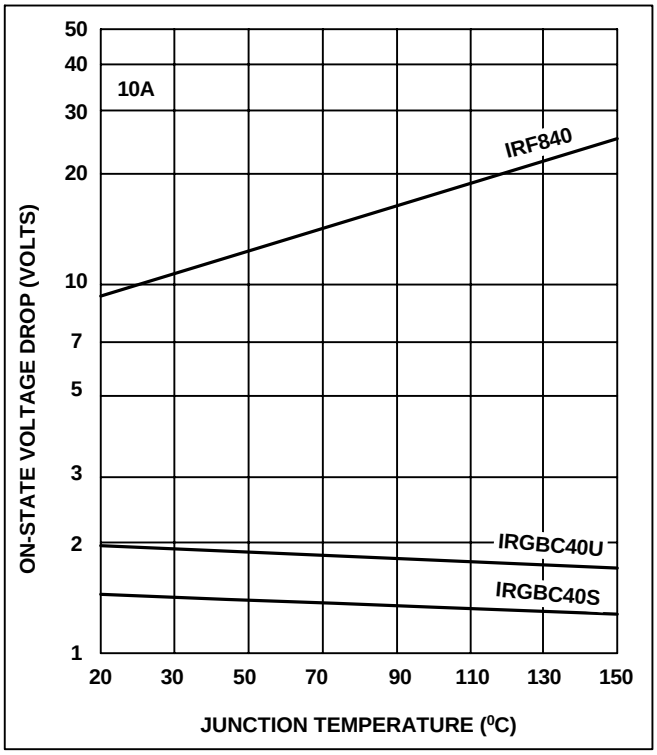


Figure 2. On-state voltage drop as temperature of two IGBTs of different switching characteristics compared to those of a HEXFET of the same die size (IRGBC40S and IRGBC40U vs IRF840). Conductivity modulation causes a dramatic improvement in the on-state voltage drop. To take the avalanche capability of the HEXFET into account, a 500V device is compared with 600V IGBTs.

Rated Voltage	IGBT	100	300	600	1200
	HEXFET®	100	250	500	1000
Typical Voltage Drop @ 1.7A/mm^2, 100^{0}C	IGBT	1.5	2.1	2.4	3.1
	HEXFET®	2.0	11.2	26.7	100

Table 1: Dependence of Voltage Drop From Voltage Rating

The voltage rating of the HEXFET® power MOSFETs used in this comparison are lower than the IGBTs to take into account their avalanche capability.

4. SWITCHING CHARACTERISTICS

The biggest limitation to the turn-off speed of an IGBT is the lifetime of the minority carriers in the N- epi, i.e., the base of the PNP. Since this base is not accessible, external drive circuitry cannot be used to improve the switching time. It should be remembered, though, that since the PNP is in a pseudo-Darlington connection, it has no storage time and its turn-off time is much faster than the same PNP in heavy saturation. Even so, it may still be inadequate for many high frequency applications.

The charges stored in the base cause the characteristic “tail” in the current waveform of an IGBT at turn-off (Figure 3). As the MOSFET channel stops conducting, electron current ceases and the IGBT current drops rapidly to the level of the hole recombination current at the inception of the tail.

This tail increases turn-off losses and requires an increase in the deadtime between the conduction of two devices in a half-bridge. Traditional lifetime killing techniques and/or an N+ buffer layer to collect the minority charges at turn-off are commonly used to speed-up recombination time.

Insofar as they reduce the gain of the PNP, these techniques increase the voltage drop. Pushed to the extreme, minority lifetime killing causes a quasi-saturation condition at turn-on, as shown in Figure 4, where the turn-on losses have become larger than the turn-off losses.

Thus, the gain of the PNP is constrained by conduction and turn-on losses on one hand, and by latching considerations on the other, as explained in the next section. Like all minority carrier devices, the switching performance of an IGBT degrades with temperature.

IGBTs operated in zero current switching may exhibit quasi-saturation losses at turn-on that are somewhat higher than in switchmode circuits.

The low di/dt that is characteristic of this mode of operation emphasizes the "switchback" phenomenon described in the previous section. Similarly, with zero-voltage turn-off, the IGBT may experience a short burst of current if the complementary device is turned on soon after the current has ceased in the one that was conducting.

This is due to the fact that the turn-on of the complementary device causes the supply voltage to appear across the first IGBT, thereby depleting its base region and causing a final sweep-out of the minority carriers that were still left there. There is, however, a component of current that is due to the charging of the device capacitances and is totally unrelated to minority carriers.

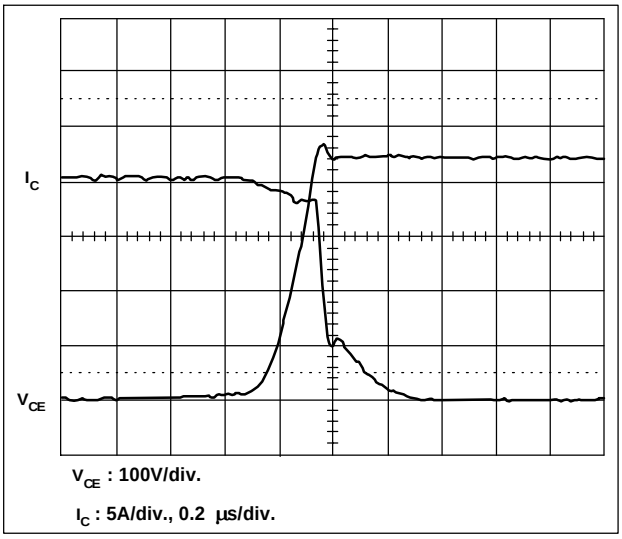


Figure 3. Turn-off waveform of a commercial IGBT at 250C, rated current. Notice the clean break at the inception of the "tail". Switching circuit as in Figure 16.

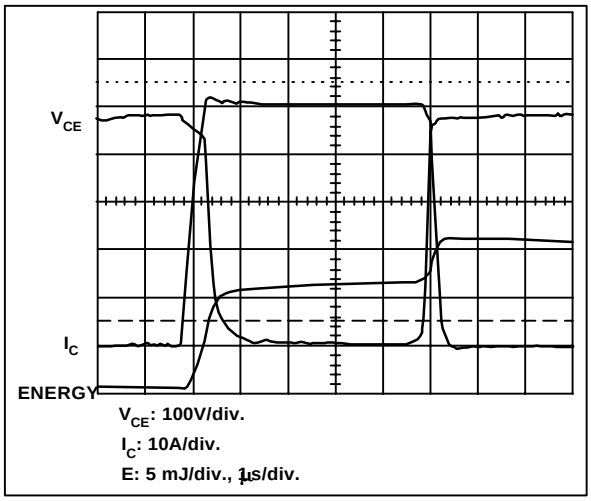


Figure 4. Switching waveforms of a commercially available IGBT with heavy lifetime killing. It takes approximately 0.5ms for the voltage to drop the last 50V. The energy plot shows that the losses at turn-on are twice as high as those at turn-off. Switching circuit as in Figure 16.

5. LATCHING

As shown in the cross-section of Figure 1, the IGBT is made of four alternate P-N-P-N layers. Given the necessary conditions ($\alpha_{NPN} + \alpha_{PNP} > 1$) the IGBT could latch-up like a thyristor. The N+ buffer layer and the wide epi base reduce the gain of the PNP, while the gain of the NPN, which is the parasitic bipolar of the MOSFET, can be reduced with the same techniques [1] that are commonly employed to give HEXFET®s their avalanche and dv/dt capability, mainly a drastic reduction of the r'_b. If this r'_b is not adequately reduced, "dynamic latching" could occur at turn-off when a high density of hole current flows in r'_b, taking the gain of the parasitic NPN to much higher values.

6. SAFE OPERATING AREA

The safe operating area (SOA) describes the capability of a transistor to withstand significant levels of voltage and current at the same time. The three main conditions that would subject an IGBT to this combined stress are the following:

1. Operation in short circuit. The current in the IGBT is limited by its gate voltage and transconductance and can reach values well in excess of 10 times its continuous rating. The level of hole current that flows underneath the N+ source contact can cause a drop across r'_b, large enough to turn on the NPN parasitic bipolar with possible latching. This is normally prevented by a reduction in r'_b, as mentioned in the previous section or by a reduction of the total device transconductance. Since this second technique increases conduction losses and reduces switching speed, two families of IGBTs have been made available by IR, one optimized for low conduction losses, the other for short circuit operation, as indicated in Section 9.

2. Inductive turn-off, sometimes referred to as "clamped I_L." In an inductive turn-off the voltage swings from a few volts to the supply voltage with constant current and with no channel current. These conditions are different from those described in the previous section in so far as the load current is totally made up of holes flowing through r'_b. For this reason some manufacturers suggest the use of gate drive resistors to slow down the turn-off dv/dt and maintain some level of electron current, thereby avoiding a potential "dynamic latching" condition. IGBTs from International Rectifier can be operated at their maximum switching speed without any problem. Reasons to limit the switching speed should be external to the device (e.g., overshoots due to stray inductance), rather than internal.

3. Operation as a linear amplifier. Linear operation exercises the SOA of the IGBT in a combination of the two modes described above. No detailed characterization of IGBTs as linear amplifiers has been carried out by IR, given the limited use of IGBTs in this type of application.

7. TRANSCONDUCTANCE

The current handling capability of a semiconductor can be limited by thermal constraints or by gain / transconductance constraints. While the "headline current rating" of power semiconductors is based solely on thermal considerations, it is entirely possible, as is frequently the case with bipolar transistors, that the device cannot operate at the current level it is thermally capable of, because its gain has fallen to very low values. As shown in Figure 5, the transconductance of an IGBT tops out at current levels that are well beyond its thermal capability, while the gain of a bipolar of similar die size is on a steep downslope within its current operating range. The flattening out of transconductance occurs when the saturation effects in the MOSFET channel, that reduce the base current of the PNP, combine with the flattening of the gain of the PNP. Since temperature reduces the MOSFET channel current more than it increases the gain of the PNP, the saturation in transconductance occurs at lower current as the temperature increases.

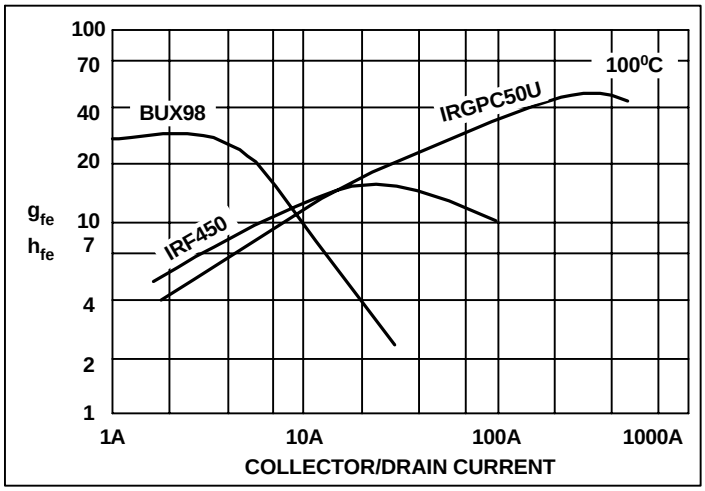


Figure 5. Current dependence of the transconductance of an IGBT compared to that of a HEXFET and to the gain of a bipolar of approximately the same die size. The IGBT, like te power MOSFET, is not "gain limited."

Since lifetime killing reduces the gain of the PNP, the transconductance of fast IGBTs peaks at a lower level than those without lifetime killing. This, however, is a second order effect because the gain of the PNP is determined mainly by the N+ buffer layer. The decrease in transconductance at very high current and its additional decrease with temperature helps protect the IGBT under short circuit conditions. With a gate voltage of 15V, the current density of a standard IGBT from International Rectifier reaches values of 10-20A/mm2 in short circuit. This high transconductance is partly responsible for their superior switching and conduction characteristics.

8. HOW TO READ THE DATA SHEET

International Rectifier prides itself on having one of the most comprehensive IGBT data sheets in the industry, with all the information required to operate the IGBT reliably. However, like all technical documents it requires a good understanding by the user of the different terms and conditions. These are briefly explained in the following sections.

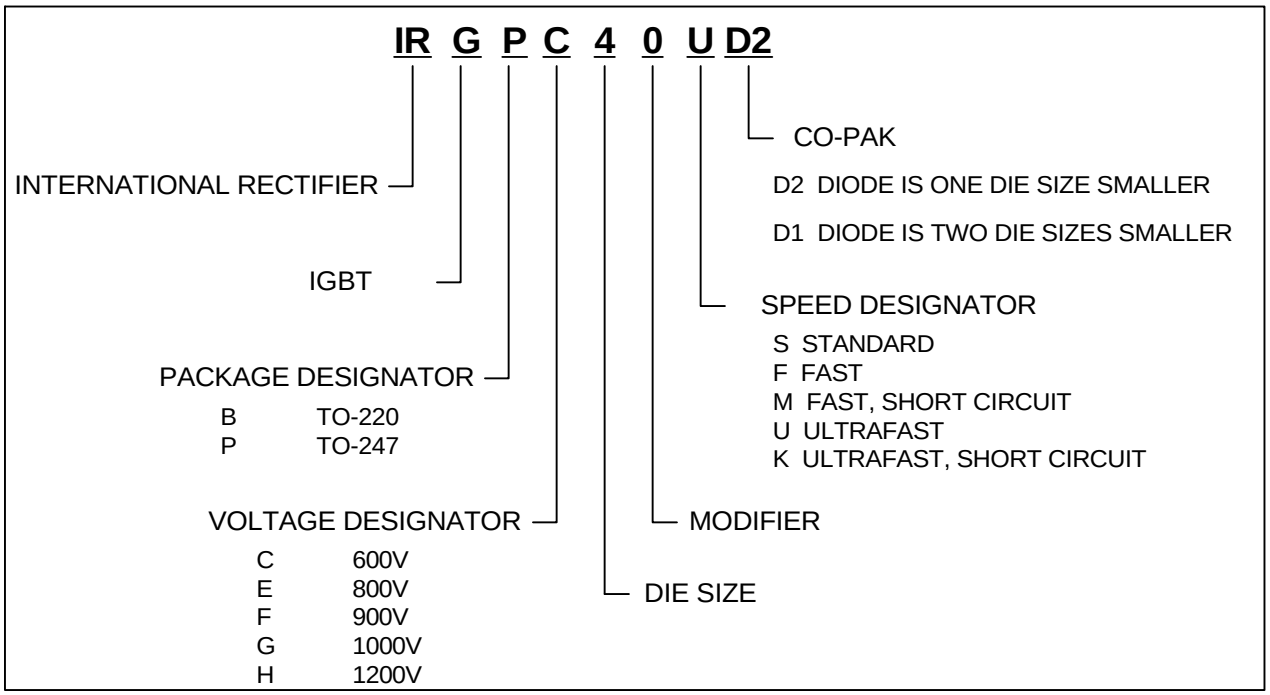


Figure 6. Simplified nomenclature code for commercial IGBTs from International Rectifier

8.1. The Headline Information

In addition to the mechanical layout, the front page gives the voltage drop at the 100ºC current ratings. The part number itself contains in coded form the key features of the IGBT, as explained in Figure 6.

8.2. The Absolute Maximum Ratings

This table sets up a number of constraints on device operation that apply under any circumstance.

Continuous Collector Current @ T_C = 25°C and 100°C (I_C). This represents the dc current level that will take the junction to its rated temperature from the stipulated case temperature. It is calculated with the following formula:

$$I_C = \frac{\Delta T}{\theta_{j-c} \bullet V_{CE(on)} @ I_C}$$

where ΔT is the temperature rise from the stipulated case temperature to the maximum junction temperature (150°C) . Notice that $V_{CE(On)}$ @ I_C is not known because I_C is not known. 1t can be found with few iterations **.**

It is clear, from this formula, that a current rating has no meaning without a corresponding junction and case temperature. Since in normal applications the case temperature is much higher than 25°C, the associated rating is of no practical value and is only reported because transistors have been traditionally rated in this way. Figure 7 shows how this rating changes with case temperature, with a junction temperature of 150°C, for a specific device.

Pulsed Collector Current (I_{CM}). Within its thermal limits, the IGBT can be used to a peak current well above the rated continuous DC current. The temperature rise during a high current transient can be calculated as indicated in Section **Y**. The test circuit is shown in Figure 8.

Collector-to-Emitter Voltage (V_{CE}). Voltage across the IGBT should never exceed this rating, to prevent breakdown of the collector-emitter junction. The breakdown itself is guaranteed in the Table of Electrical Characteristics .

Maximum Gate-to-Emitter Voltage (V_{GE}). The gate voltage is limited by the thickness and characteristics of the gate oxide layer. Though the gate dielectric rupture is typically around 80 volts, the user is limited to 20V to limit current under fault conditions and to ensure long term reliability.

Clamped Inductive Load Current (I_{LM}). This rating guarantees that the device is able to repetitively turn off the specified current with a clamped inductive load, as encountered in most applications. In fact, the test circuit (Figure 9) exposes the IGBT to the peak recovery current of the free-wheeling diode, which adds a significant component to the turn-on losses (Figure 10). This rating guarantees a square switching SOA, i.e., that the device can sustain high voltage and high current simultaneously. The I_{LM} rating is specified at 150°C, 80% of the rated voltage. This complements the information supplied by the RBSOA.

Reverse Avalanche Energy (E_{ARV}). This subject is covered in detail in the BV_{ECS} section of the electrical characteristics .

Maximum Power Dissipation @ 25°C and 100°C (P_D). It is calculated with the following formula:

$$P_D = \frac{\Delta T}{\theta_{j-c}}$$

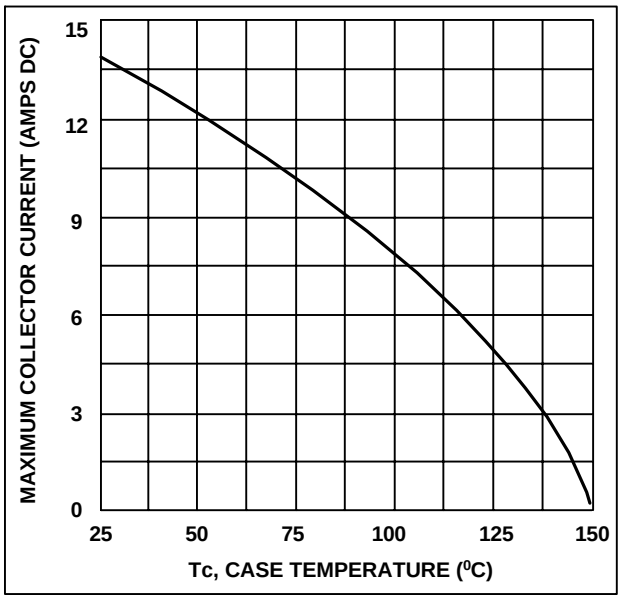


Figure 7. Maximum Collector Current vs. Case Temperature

The same comments that were made on the Continuous Collector Current apply to Power Dissipation.

Junction Temperature (Tj): the device can be operated in the industry standard range of -55°C to 150°C.

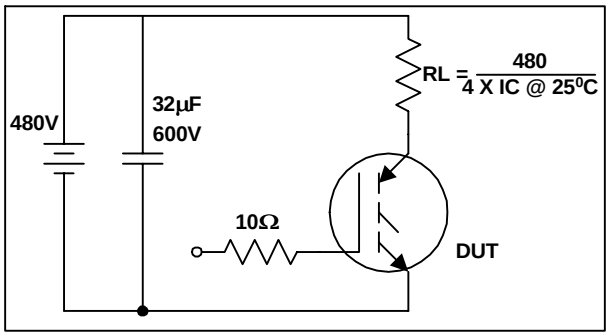


Figure 8. Pulsed Collector Current Test Circuit

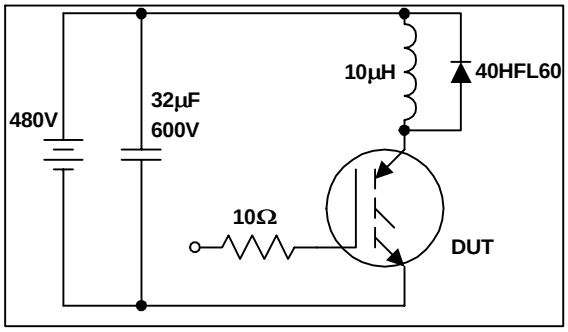


Figure 9. Clamped Inductive Load Test Circuit

8.3. Thermal Resistance

R_{thjc}, R_{thcs}, R_{thja} are needed for the thermal design, as explained in INT-949

8.4. Electrical Characteristics

The purpose of this section is to provide a detailed characterization of the device so that the designer can predict with accuracy its behavior in a specific application.

Collector-to-Emitter Breakdown Voltage (BV_{CES}). This parameter guarantees the lower limit of the distribution in breakdown voltage. Breakdown is defined in terms of a specific leakage current and has a positive temperature coefficient (listed in the table as $BV_{CES}/\Delta T$) of about 0.63V/°C. This implies that a device with 600V breakdown at 25°C would have a breakdown voltage of 550V at -55°C.

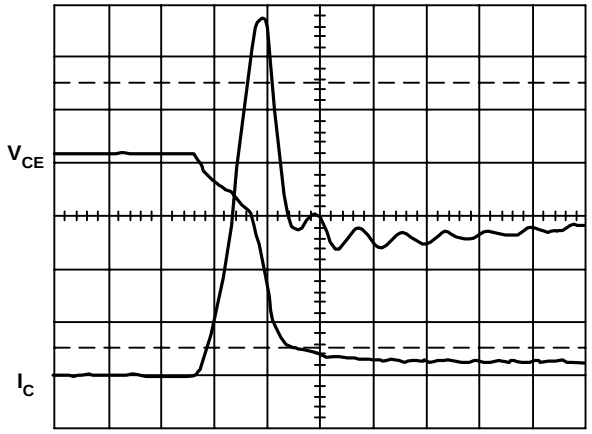


Figure 10a. Turn-on with a clamped inductive load and a fast recovery diode. Test circuit as in Figure 9.

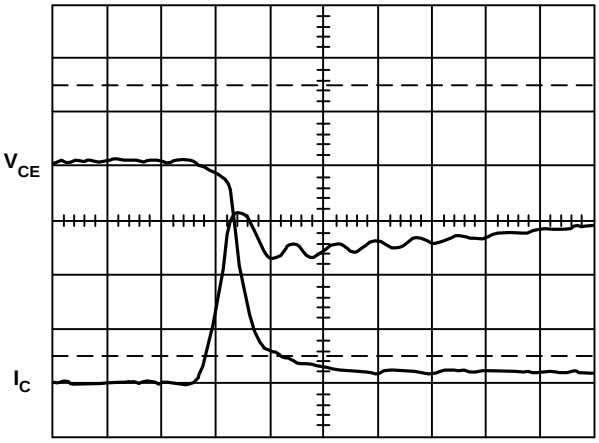


Figure 10b . Turn-on with an ideal diode (zener clamp). Test circuit as in Figure 16.

The reverse recovery is a significant contributor to turn-on losses. To discriminate between the losses that are intrinsic to the IGBT and those due to the diode reverse recovery, the test circuit shown in Figure 16 has been used to generate the data sheet values.

Emitter-to-Collector Breakdown Voltage (BV_{ECS}). This rating characterizes the reverse breakdown of the unterminated collector-base junction of the PNP. The relevance of this specification and its associated reverse avalanche energy can be better understood with reference to Figure 11. When an IGBT turns off and current is transferred to the diode across the complementary device, the turn-off di/dt in the stray inductance that is in series with the diode generates a reverse voltage spike across the IGBT (i.e., the collector voltage goes negative with respect to the emitter). This reverse voltage is typically less than 10V, though higher voltages can result from very high di/dt or poor layout. Since this reverse voltage can cause avalanche in the junction, International Rectifier IGBTs have an energy rating, given in the Absolute Maximum Ratings table, that is more useful to the designer than a traditional diode characterization. This rating is typically an order of magnitude more than what would be required by the user.

Collector-to-Emitter Saturation Voltage ($V_{CE(on)}$). Being the key rating to calculate conduction losses, this value is supported by three figures that provide a detailed characterization in temperature, current and gate voltage (Figures 14, 15, and 16 for the IRGBC20U). These replace the older format shown in Figure 12 and 13.

Gate Threshold Voltage ($V_{GE(th)}$). This is the range of voltage on the gate at which collector current starts to flow. The variation in gate threshold with temperature is also specified ($\Delta V_{GE(th)} / \Delta T_j$). Typically the coefficient is -11 mV/°C, leading to a reduction of about 1.4V in the threshold voltage at high temperature.

Forward Transconductance (g_{FE}). This parameter is measured by superimposing a small variation on a gate bias that takes the IGBT to its 100°C rated current in "linear" mode. As mentioned in Section 7, transconductance increases significantly with current so that the "current throughput" of an IGBT is not limited by gain, as a bipolar, but by thermal considerations.

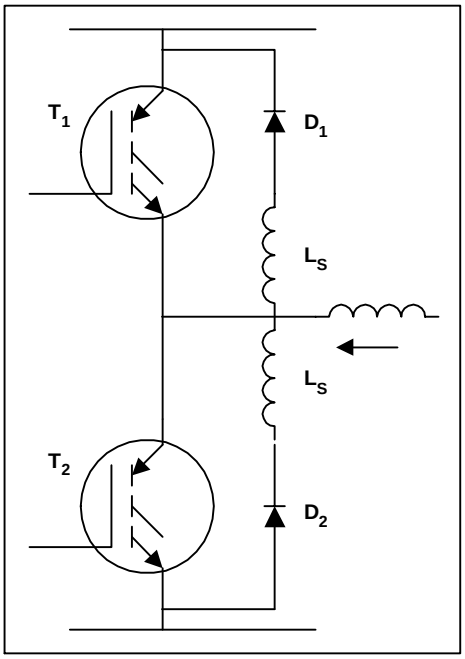


Figure 11. When T2 goes off, load current flows into the diode in parallel with T1. The reverse turn-off di/dt of T2 developes a voltage across the stray inductance in series with D1 which reverse biases T1. IR's IGBTs have a specified reverse blocking capability (BV_{CES}) and an avalanche rating (E_{RV})

Zero-Gate-Voltage Collector Current (I_{CES}). This parameter guarantees the upper limit of the leakage distribution at the rated voltage and two temperatures. It complements the BV_{CES} rating seen above.

8.5. Switching Characteristics

GateChargeParameters(Q_g, Q_{ge}, Q_{gc}). Gate charge values of an IGBT are useful to size the gate drive circuit and estimating gate drive losses. Unfortunately they cannot be used to predict switching times, as for a power MOSFET, because of the minority carrier nature of this device. The test method and the characteristics described in the application note INT-944. Figure 17 gives the typical value of the total gate charge as a function of the voltage applied to the gate. The shape of the curve is explained in detail in INT-944.

Switching Times (t_d, t_r, t_f). The switching times for a simple IGBT are defined with reference to the Switching Loss Test Circuit of Figure 18. Those for co-paks are defined with reference to the Clamped Inductive Load of Figure 19.

For a simple device, they are defined as follows:

- Turn-on delay time: 10% of gate voltage to 10% of collector current
- Rise time: 10 to 90% of collector current
- Turn-off delay time: 90% of gate voltage to 90% of collector current
- Fall time: 90 to 10% of collector current.

For a copak, they are defined as follows:

- Turn-on delay time: 10% of gate voltage to 10% of collector current
- Rise time: 10 to 90% of collector current
- Turn-off delay time: 90% of gate voltage to 10% of collector voltage
- Fall time: 90 to 10% of collector current.

Switching times provide a useful guideline to establish the appropriate deadtime between the turn-off and subsequent turn-on of complementary devices in a half bridge configuration and the minimum and maximum pulse widths. They provide a very unreliable indication of switching losses. Because of the current tail mentioned in Section 8.2, a significant part of the turn-off energy may be dissipated as the current is below 10%. The voltage fall time, on the other hand, is not characterized in any way. Thus, two significant contributors to losses are not properly accounted for by the switching times. Switching losses are fully characterized as such in the data sheet, as explained in the next paragraph.

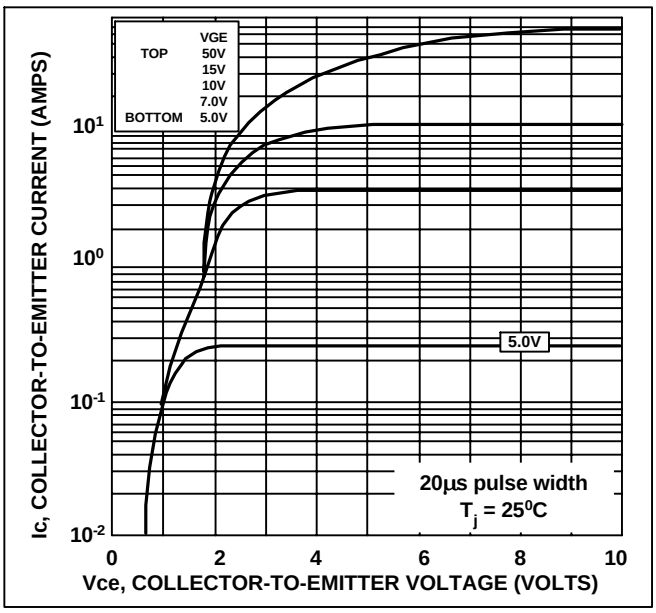


Figure 12. Typical Output Characteristics. Tc = 25°C

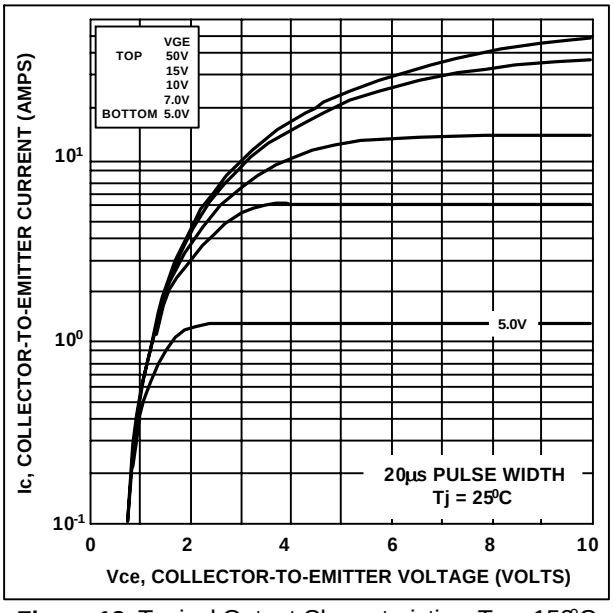


Figure 13. Typical Output Characteristics, Tc = 150°C

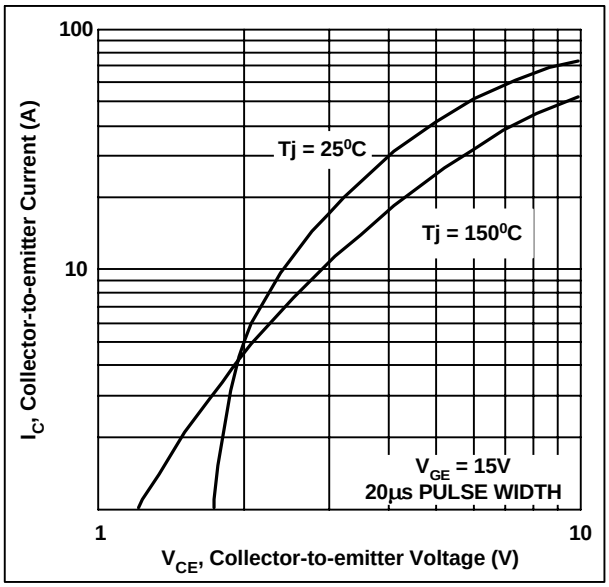


Figure 14.

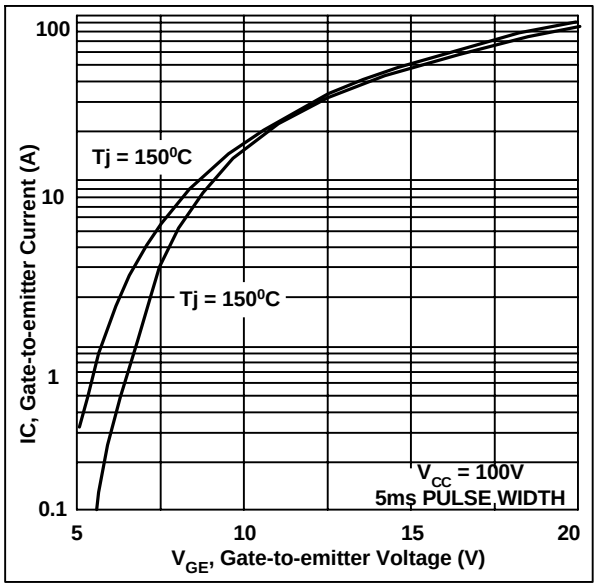


Figure 15.

It should be remembered that IGBTs, like power MOSFETs, do not have a storage time. The turn-off delay is due to the Miller effect, as explained in Section I.A of INT-990.

Switching Energy (E_{on}, E_{off}, E_{ts}). IGBTs from International Rectifier have a guaranteed switching energy providing a full characterization in terms of temperature, collector current and gate resistance (Figures 20, 21 and 22 for the IRGBC20U). This allows the designer to calculate the switching losses, without worrying about the actual current and voltage waveshapes, the tail and the quasi-saturation.

Any test circuit for measuring switching losses has to satisfy two fundamental requirements:

1. It must simulate the switching conditions as they are encountered in a practical application, i.e., a clamped inductive load with continuous current flow.

2. It must reflect the losses that are attributable to the IGBT, and must be independent from those due to other circuit components, like the reverse recovery of the freewheeling diode.

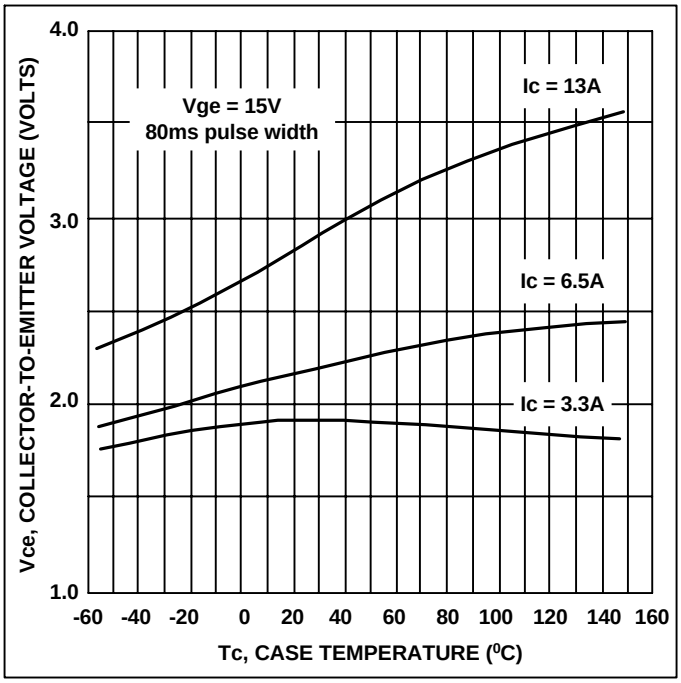


Figure 16. Collector-to-Emitter Saturation Voltage vs. Case Temperature

The test *circuit* that meets these requirements for a simple IGBT is shown in Figure 18. Its operation is as follows:
The driver IGBT builds the test current in the inductor. When it is turned off, current flows in the zener. At this point the switching time and switching energy test begins, by turning on and off the device under test (DUT). The DUT will see the test current that was flowing into the inductor and the voltage across the zener, *without* any reverse recovery component from a freewheeling diode. This test can exercise the IGBT to its full voltage and current without any spurious effect due to diode reverse recovery.

The test *method*, on the other hand, must account for all losses that occur because of the switching operation, including the quasi-saturation at turn-on and the tail at turn-off. To fulfill this requirement, the energy figures reported in the data sheet are defined as follows:

E_{on}: From 5% of test current to 5% of test voltage. We feel that 5% is a reasonable compromise between the resolution of the instrumentation and the need to account for the quasi-saturation that could occur in some devices.

E_{off}: This energy is measured over a period of time that starts with 5% of test voltage and goes on for 5 µsec. While the current tail of most IGBTs would be finished well before that time, it was felt that the contribution of the leakage losses to the total energy is minimal.

E_{ts}: This is the sum of the turn-on and turn-off losses. As shown in Figure 22, switching energy for International Rectifier IGBTs is closely proportional to current. This is not necessarily true for IGBTs from other manufacturers. The test circuit for a co-pack, on the other hand, should include the losses due to the diode, assuming a clamped inductive load with an identical device in a complementary position (Figure 19). The definitions are as follows:

E_{on}: From 10% of test current to 5% of test voltage.

E_{off}: This energy is measured over a period of time that starts with 10% of test voltage and goes on for 5 µsec.

Internal Emitter Inductance (L_E)

This is the package inductance between the bonding pad on the die and the electrical connection at the lead. This inductance slows down the turn-on of the IGBT by an amount that is proportional to the di/dt of the collector current, just like the Miller effect slows it down by an amount that is proportional to the collector dv/dt. With a di/dt of 1000 A/µsec, the voltage developed across this inductance is in excess of 7V.

Device Capacitances (C_{iee}, C_{oee}, C_{ree}).

The test circuit and a brief explanation of the test method can be found in Figure 20. The output capacitance has the typical voltage dependence of a P-N junction. The reverse transfer (Miller) capacitance is also strongly dependent on voltage (inversely proportional), but in a more complex way than the output capacitance. The input capacitance, which is the sum of the gate-to-emitter and of the Miller capacitance, shows the same voltage dependence of the Miller capacitance but in a very attenuated form since the gate-to-emitter capacitance is much larger and voltage independent.

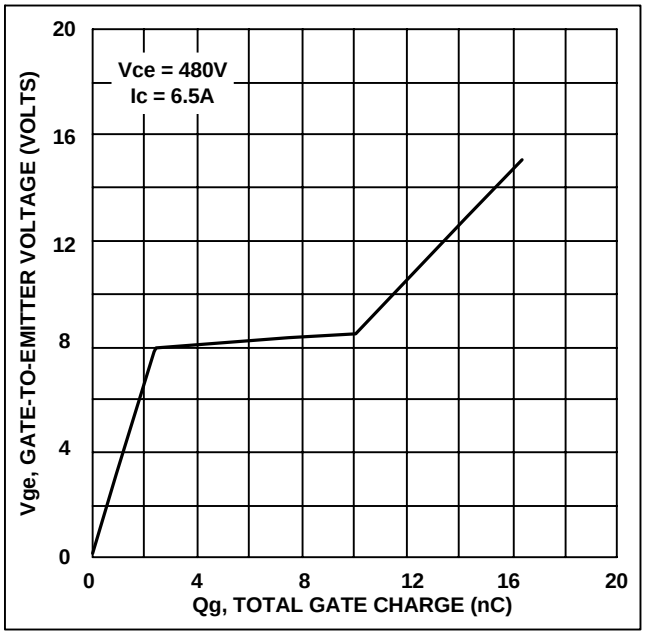


Figure 17. Typical Gate Charge vs. Gate - to - Emitter Voltage

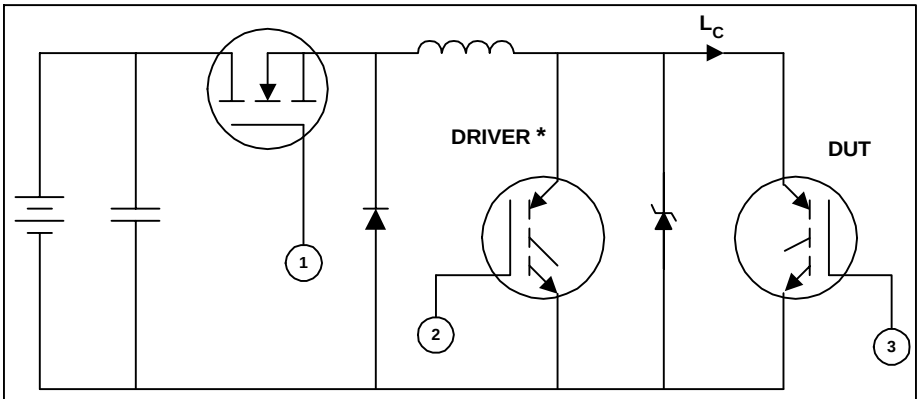


Figure 18a

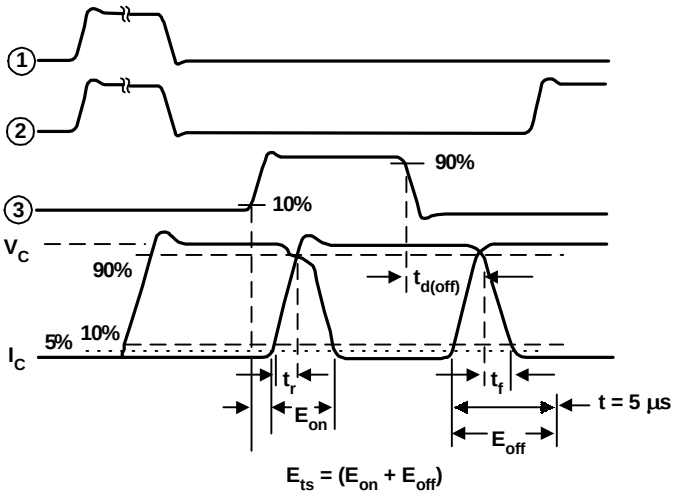


Figure 18b.

Figure 18. Switching Loss Test Circuit and Waveforms

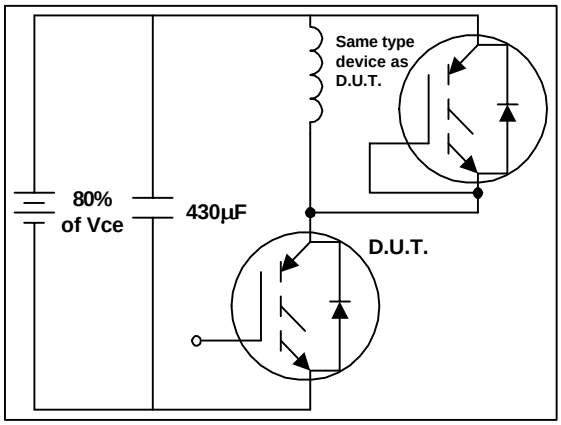


Figure 19a.

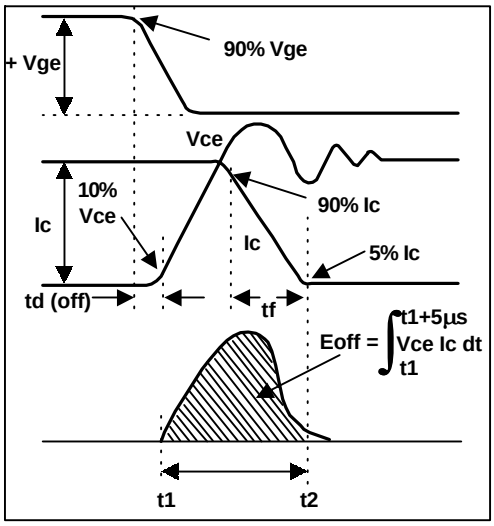


Figure 19b.

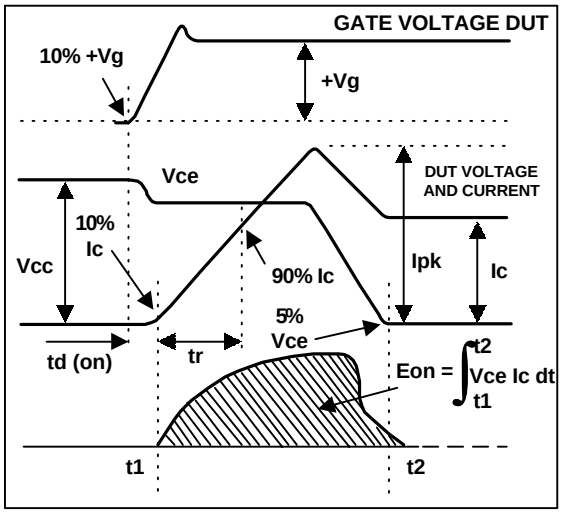


Figure 19c.

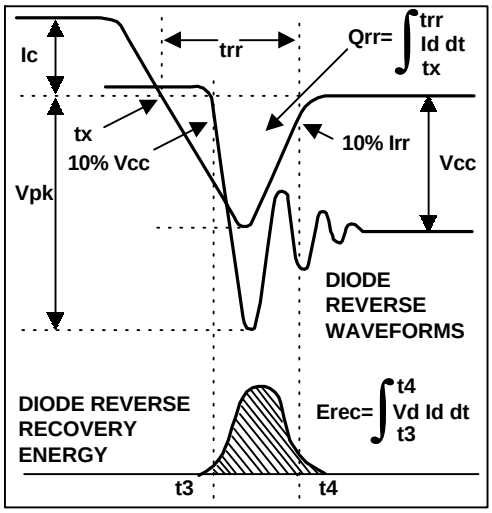


Figure 19d.

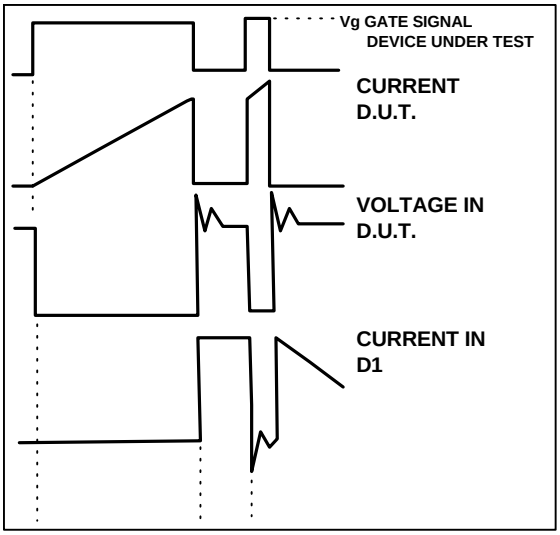


Figure 19e.

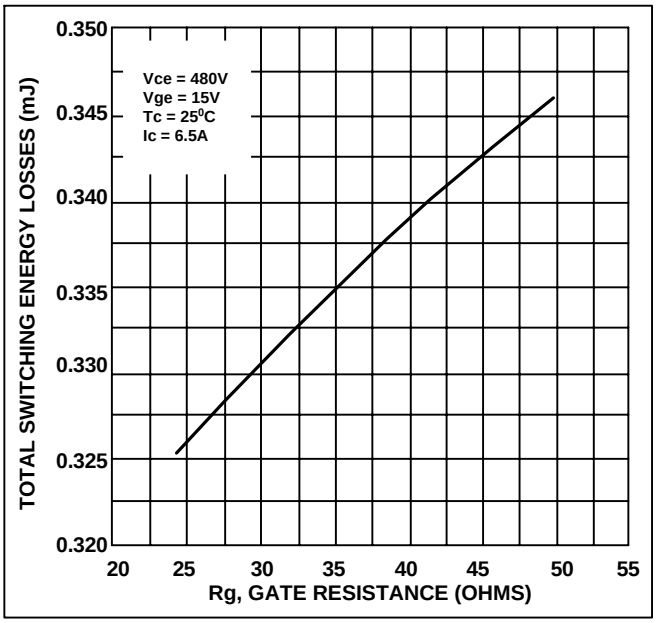


Figure 20. Typical Switching Losses vs. Gate Resistance

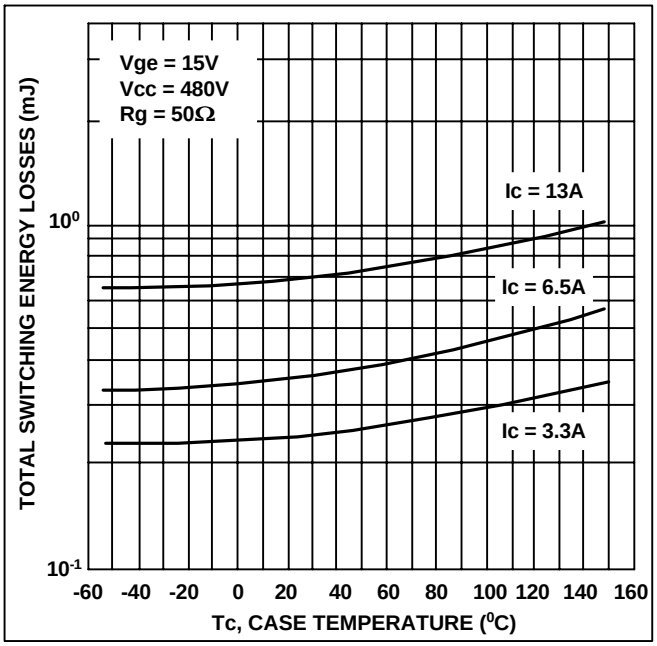


Figure 21. Typical Switching Losses vs. Case Temperature

The Transfer Characteristic (Figure 15 for the IRGBC20U). This curve deviates from the traditional definition of transfer characteristic in one detail: the drain is not connected to the gate but to a fixed (100V) supply. When gate and drain are tied together, the curve is the boundary separating operation in full enhancement from operation in linear mode (sometimes referred to as "sat mode"). Figure 15 provides an indication of current when operated in short circuit. In the normal range of operation this curve shows a slight negative dependence on temperature and is largely independent from applied voltage.

The Short-Circuit Withstand Time (for short-circuit rated IGBTs) defines the guaranteed minimum time the IGBT can be in short circuit in the specified conditions. Notice that the gate resistor cannot be any lower than specified and the overvoltage at turn-off has to be maintained to the indicated value by an appropriate clamp.

If a diode is copackaged with the IGBT, its characteristics are included in this table, together with their associated graphs. The parameters included in the table are defined in application note AN-989.

9: The IGBT Families from IR

Table II may be useful in placing different power transistors in the proper perspective. In general, the IGBT offers clear advantages in high voltage (>300V), high current (1-3 A/mm^2 of active area), and medium speed (to 5-50 kHz). International Rectifier's technology is characterized by very low voltage drop per unit of current density. This allows higher levels of minority lifetime killing and, consequently, much lower switching losses.

To maximize the value to the user of its technological breakthrough, International Rectifier has introduced three different families of devices with different crossover frequency: *Standard*, *Fast* and *UltraFast*.
IR's *Standard* IGBTs have been optimized for voltage drop and conduction losses and have the lowest voltage drop per unit of current density that is presently available in the market.

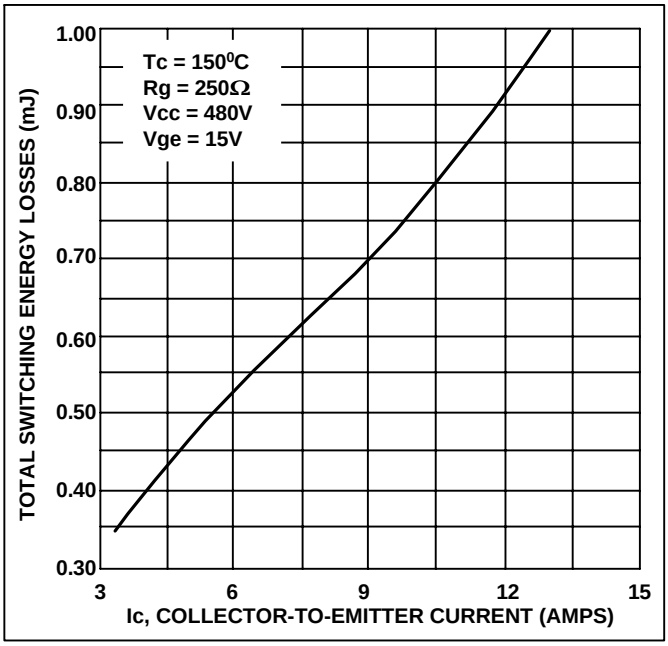


Figure 22. Typical Switching Losses vs. Collector Current

IR's *UltraFast* IGBTs have been optimized for switching losses and have the lowest switching losses per unit of current density presently available in the market.

As it is apparent from Figure 24, these devices have switching speeds that are comparable to those of power MOSFETs in practical applications. They can operate comfortably at 50 kHz in PWM and well over 100 kHz in resonant or ZVS/ZCS circuits.

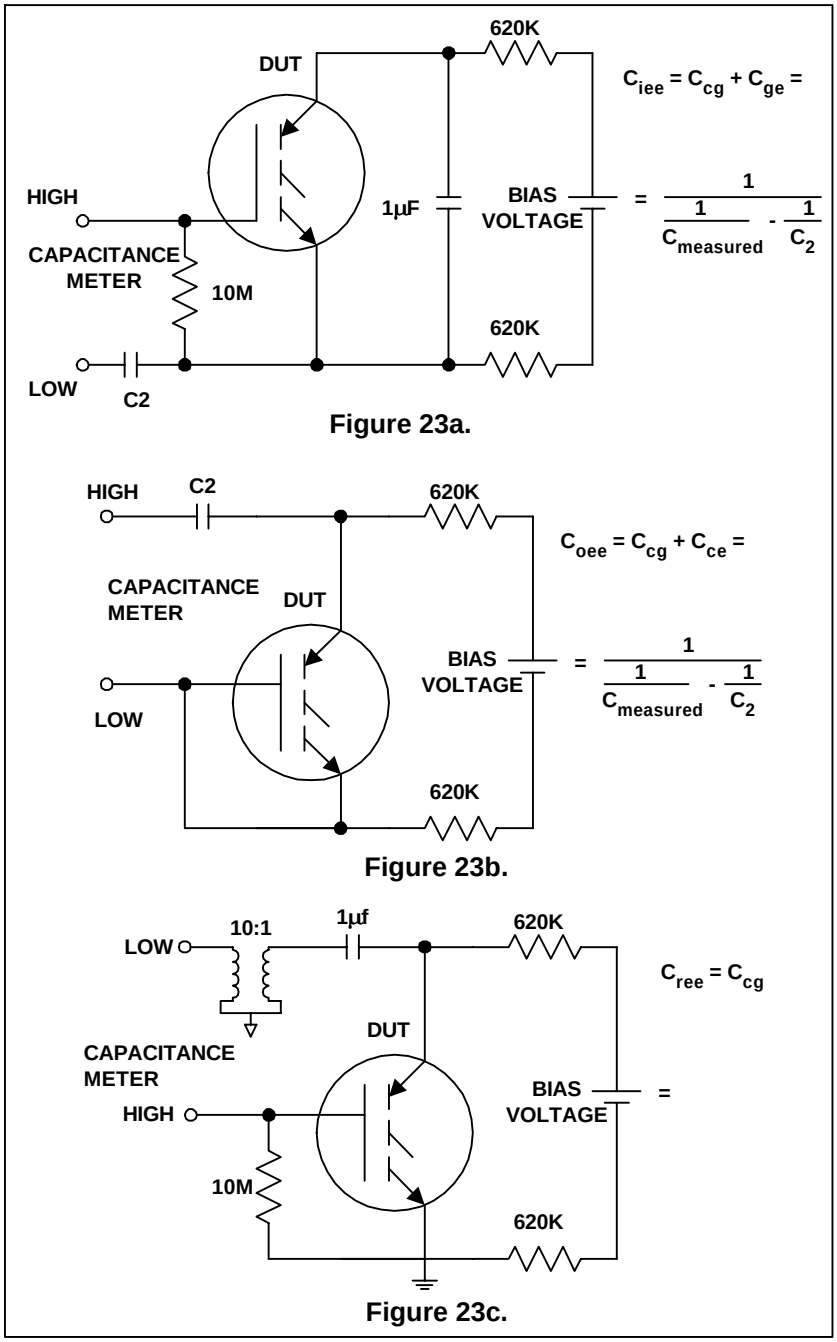


Figure 23. Capacitance test circuits

The IGBT is biased with 25V between collector and emitter. Two of its terminals are ac shorted with a large value capacitor. Capacitance is measured between these two terminals and the third.

IR's *Fast* devices offer a combination of low switching and low conduction losses that closely matches the switching characteristics of many popular bipolar transistors. Table III shows the key features of the three families. The Fast and Ultrafast IGBTs are also available in short-circuit rated versions for those applications, like motor drives, that require it. The short circuit capability comes at the expenses of a slight increase in conduction losses.

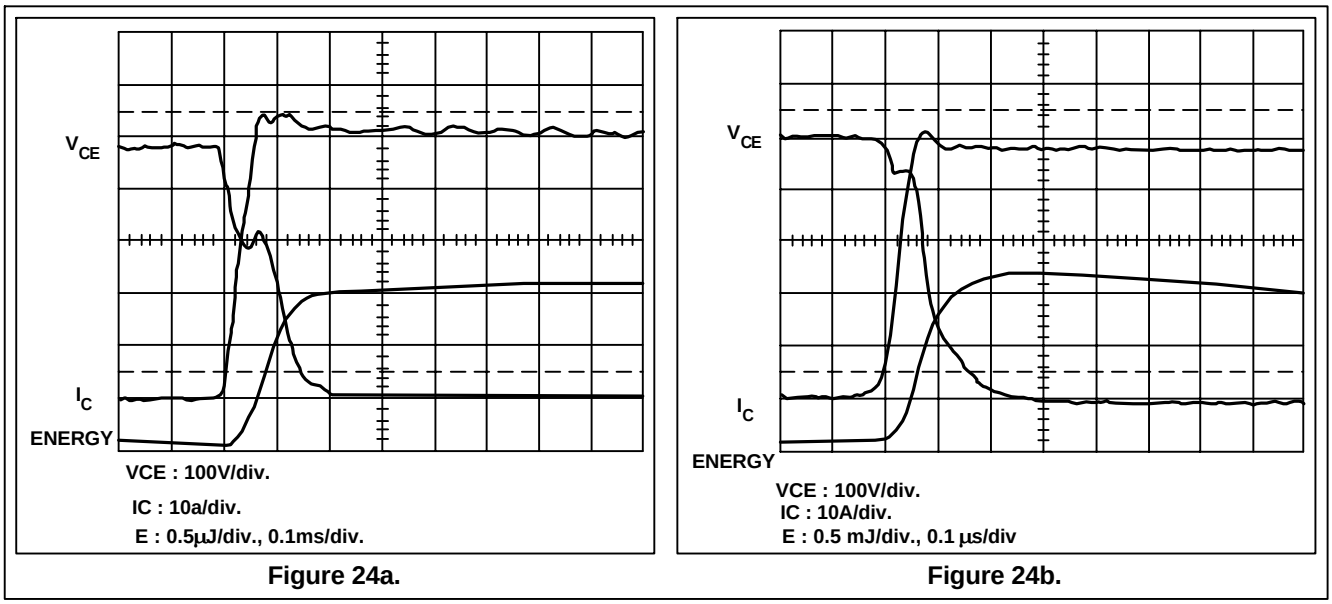


Figure 24a. **Figure 24b.**

Figure 24. IRGPC50U switching 50A at 480V, 1250C. Test circuit is as shown in Figure 16.

	POWER MOSFETs	IGBTs	Bipolars	Darlingtons
Type of Drive	Voltage	Voltage	Current	Current
Drive Power	Minimal	Minimal	Large	Medium
Drive Complexity	Simple	Simple	High Large positive and negative currents are required	Medium
Current Density For Give Voltage Drop	High at low voltages Low at high voltages	Very High Small trade-off with switching speed	Medium Severe trade-off with switching speed	Low
Switching Losses	Very Low	Low to Medium depending on trade-off with conduction losses	Medium to High depending on trade-off with conduction losses	High

Table II: Comparative Table of Power Transistor Characteristics

References:

1. U.S. Patents No. 4,376,286 and 4,642,666

Characteristic	Standard	Fast	Ultrafast
V_{CE}	1.3V	1.5V	1.9V
Switching Energy	0.54 mJ/A mm^2	0.16 mJ/A mm^2	0.055mJ/A mm^2
Conduction Losses (50% dc)	0.625W	0.75W	0.95W

Table III. International Rectifier IGBT Families

$1A/mm^2$, 100^0C, Typical Values

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 3-30-4 Nishi-Ikeburo 3-Chrome, Toshima-Ki, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371
Data and specification subject to change without notice.

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IGBTs vs HEXFET® Power MOSFETs For Variable Frequency Motor Drives

(HEXFET is a trademark of International Rectifier)

by Ajit Dubhashi, Brian Pelly

Summary

This application note compares International Rectifier IGBTs and HEXFET power MOSFETs for efficiencies as well as system costs for a range of 3-phase sinusoidal PWM motor drives. Losses are calculated for two different carrier frequencies and the system costs include heatsink costs. Aluminum vs. silicon tradeoff is discussed along with relevant examples. Results are presented in a graphical format, allowing designers to choose an optimum device for their motor drive application.

Introduction

Insulated Gate Bipolar Transistors (IGBTs) have recently entered the field of power electronics as serious contenders for power processing sockets. The IGBT has shed its image as an unreliable lab curiosity and is now beginning to compete seriously with established devices such as the power MOSFET. Designers are concerned with the choices available based on complexity, efficiency, and overall system cost. The aim of this application note is to compare MOSFETs and IGBTs in terms of system costs and efficiencies in typical 3-phase 220V motor control applications ranging from one-quarter horsepower to 5 hp.

The first section compares the characteristics and the structures of International Rectifier devices. The next section deals with the assumptions made and the methods used in the comparison. The results of the comparison are then provided graphically. This is followed by a closer look at a couple of specific power ratings. This application note concludes with a chart showing the tradeoffs between cost and efficiency across the board, indicating the "optimum" devices for each horsepower range, and a set of general conclusions.

Background

The field of 3-phase 220V PWM motor drives has had mainly bipolars and power MOSFETs competing with one another. Power MOSFETs have been the choice of power electronic designers, especially at power levels below 5 hp because of the ease of drive and their rugged operation. Since FETs are voltage-controlled devices, they require only very small gate current pulses to turn them off and on. The average currents necessary for controlling the device state are often magnitudes lower than those required by bipolar devices of similar ratings. What's more, the FET's wide switching safe operating area (SOA), avalanche and dv/dt capabilities allow for snubberless operation, often a great advantage over bipolars. The $R_{DS(on)}$ of the FET does, however, rise exponentially with voltage rating.

The IGBT combines the best of both worlds. It is a voltage-controlled device (like the MOSFET) allowing designers to greatly simplify their drive circuits. It is a rugged device with a square switching SOA and high peak current capability. In addition, it exhibits low forward voltage characteristics similar to bipolars, reducing the conduction loss. Also, as it does not have an internal reverse diode, designers can choose an external fast recovery diode to suit a specific application. All this indicates that the IGBT will be the device of choice for applications requiring high current densities at high voltages coupled with switching frequencies up to 20 to 50 kHz.

Comparison of the Device Structures

The IGBT is a spinoff from power MOSFET technology. Both devices have similar cross sections as can be seen from Figures 1a and 1b. Each shares a similar gate structure with polysilicon gate buses and P wells with N tubs. The N type material under the P wells form the drain region for the HEXFET power MOSFET and its resistivity is responsible for its BV_{dss} rating. Consequently, as the required breakdown voltage for HEXFETs goes up, so does the resistivity of this region, leading to an exponential increase in the on-resistance of the device. The manner in which the IGBT differs from the HEXFET power MOSFET is that it has two additional layers under the high resistivity N region. The first is a thin N+ region for decreasing the lifetime

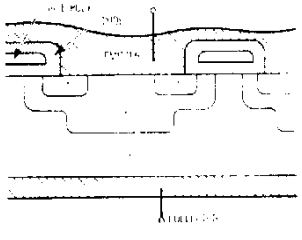


Figure 1a. HEXFET cross section

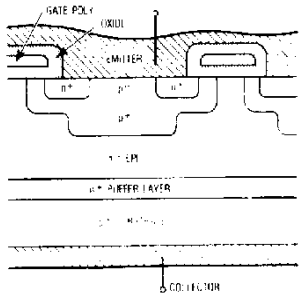


Figure 1b. IGBT cross section

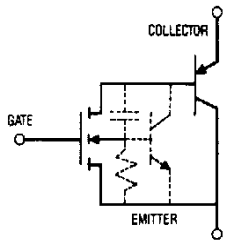


Figure 2. Equivalent circuit

of stored charges. The second is a P region which is responsible for the low on-state voltage drop. This P region floods the N region with carriers whenever the device is turned on and this process of conductivity modulation lowers the normally high resistivity of the N region. Figure 2 shows the approximate equivalent circuit which can be used to describe the operation of the device. The structure is similar to a FET input Darlington with a PNP output device.

As is evident from the device structure, the base region of the PNP is not brought out of the device and, consequently one cannot actively get rid of the carriers in the base region to effect a fast turn-off. This is why the N + layer is required to reduce the lifetime of carriers. It also serves to reduce the gain of the output PNP structure which is important to prevent device latch-up.

Figure 3 shows a comparison of forward voltage characteristics of 600V-rated devices. An IGBT of the same size as that of a MOSFET would have nearly one-tenth the conduction losses. This reduced on-state drop is, however, at the expense of an increase in switching energy as the IGBT displays a distinctly slower turn-off. Another feature of the IGBT is the

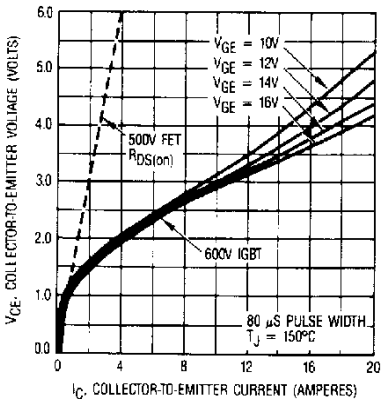


Figure 3. Comparison of forward voltages

Table 1

IGBTs	MOSFETs
1. Minority/majority carrier Conduction	Majority Carrier Conduction
2. Low Forward Drop	High $R_{DS(on)}$
For similar die size, voltage rating and current	
3. Turn-off time 500 ns	Turn-off time <100 ns MHz operation possible.
4. No internal diode	Reverse internal parasitic diode
5. 4-layer device	3-layer device

absense of an inherent diode, whose recovery losses add to the total loss, as in the case of a power MOSFET. Designers, however, can select an external reverse diode to suit the application. Table 1 summarizes the comparison between IGBTs and MOSFETs.

Comparison of Losses in a Three-Phase AC Drive Application

For various applications the relative importance of switching loss and conduction loss can be very different. This application note compares the performance of IGBTs and MOSFETs in 3-phase motor drive applications, where a 3-phase sinusoidal waveform is constructed using a PWM technique. The devices are assumed to operate from a rectified 220V line.

Various horsepowers from one-quarter to 5 hp are analyzed. Each hp is evaluated at PWM switching frequencies of 5 kHz and 20 kHz. Various die sizes are evaluated at every current rating to yield the most cost effective solution. External fast recovery freewheeling diodes are assumed around the IGBTs (HEXFETs already have a built-in reverse diode).

The total losses are calculated over a cycle. These include the conduction losses in the device, the conduction losses in the diode, the turn-on and turn-off losses due to the device, and the switching losses associated with the Q_{rr} and t_{rr} of the diode.

To calculate conduction losses over a cycle (with a sinusoidally varying "chopped up" current waveform as shown in Figure 4), a knee voltage + dynamic resistance type of model is assumed for all the switches. For HEXFET power MOSFETs which are purely resistive (unlike the IGBTs or the diodes) the knee voltage is zero. As the die size goes up, the dynamic resistance decreases proportionately and thus the conduction losses decrease.

The turn-on and turn-off losses are assumed to be linearly dependent on current. The losses related to t_{rr} and Q_{rr} depend on the current in a non-linear way, and thus a linearization is resorted to, for easier manipulation of the equations.

The resulting conduction and switching losses are converted into a bar graph format, Figures 5b thru 12b, where losses for all devices evaluated at a particular hp can be compared. The bars are divided into switching and conduction losses for ease of comparison.

The next step is to evaluate the costs of the various solutions as it is usually the prime criterion for device selection. The user costs assumed for the devices are projected mature high volume market prices.

To the device costs is added the cost of the heatsink required to cool the device to a maximum T_j of 110°C at normal full load operating power. The heatsink cost represents a significant part of the total costs and, in fact, can often result in a larger size of silicon being chosen to reduce the heatsink size and cost, as will be seen later. Mounting and wiring costs have not been included.

Finally, the cost information relating to each hp is put together in a per unit bar graph format, Figures 5a thru 12a, similar to that for losses. The costs are split up into per unit device (IGBT + diode or HEXFET) and per unit heatsink costs, so that the user can appreciate the significance of the heatsink costs. Thus, the information presented in the cost and loss graphs provides the designer with a spectrum of choices that can be exercised.

A Closer Look at the 0.75 HP Example

A total of four different devices as shown in Figures 7a and 7b (two HEXFETs and two IGBTs) are investigated at each frequency. As would be expected, the total losses decrease as the device size goes up. Obviously, increasing the silicon content implies increasing device costs, but this can be offset by decreasing heatsink cost. This implies that the smallest silicon size may not automatically be the lowest cost solution.

For example, an IRF830 HEXFET can be used in a 0.75 hp inverter at 20 kHz, but as is shown in the charts the power dissipated is so large that a hugh heatsink is required to keep the die temperature within design limits. The IRF840 HEXFET turns out to be a much more inexpensive solution, with the added advantage of increasing the system efficiency. However, the IGBT 1 size device turns out to be even less expensive than HEXFET power MOSFETs at 20 kHz, with even better system efficiency.

The picture is slightly different at 5 kHz as the IRF830 can handle the power loss with a relatively smaller heatsink cost which turns out to be the lowest cost solution (though the one with the highest losses). Looking at the IRF840 costs, it is apparent that the price penalty to be paid for going from 5 kHz to 20 kHz is less than 20%, which is not very significant in terms of the overall drive cost.

Crossover Point for IGBTs and HEXFETs

If the cost figures are normalized with respect to their horsepower ratings, and arranged as shown in Figures 13 and 14, the crossover points between IGBTs and HEXFETs becomes apparent. At 5 kHz, IGBTs tend to be the lowest cost solution above 1 hp and HEXFETs are most cost effective below 1 hp. At 20 kHz the crossover point shifts down and IGBTs tend to be most cost effective above 0.75 hp. This is because the IRF830, the device of choice at 5 kHz, cannot handle the extra switching loss at 20 kHz and therefore, cannot be used. The next higher die size costs more than the IGBT solution, making the IGBT the most cost effective solution at 20 kHz. The crossover points are a function of device and heatsink pricing available to the designer; in the immediate future they will probably be a bit higher than 1 hp.

Cost Efficiency Trade Off

In most designs, cost as well as efficiency is very important. This application note has attempted to provide a complete overview of the cost-efficiency tradeoff for the designer. Figures 15 and 16 present the summary of this exercise. Each set of bar graphs represent two different switching frequencies. On the X-axis are the various horsepowers, and on the Y-axis are the efficiencies that can be achieved with various implementations at those horsepowers. Each hp column has two sub bars. The left one represents the HEXFET solution and the right one represents the IGBT solution. As there are usually two or three die sizes being evaluated, these are represented by several horizontal lines with the smallest die size (lowest efficiency) circled. Each horizontal line has a number associated with it which represents the normalized cost associated with that implementation. For example, if a designer would like to see a comparison of devices at 1 hp and plans to use 20 kHz switching frequency, he would see that three HEXFET die sizes have been evaluated, (3, 4, 5) and two IGBTs (1, 2) have been evaluated. The lowest cost solution would be the IGBT 2 (with 1.57 per unit dollar cost) at about 95% efficiency. The IGBT 2 solution is less expensive than the IGBT 1 solution as the heatsink cost has boosted the system cost, tilting the tradeoff towards silicon rather than aluminum. This is true even for the FETs where the HEX-4 solution (at 2.41 per unit dollars) is more economical than a HEX-3 solution (at 5.81 per unit dollars).

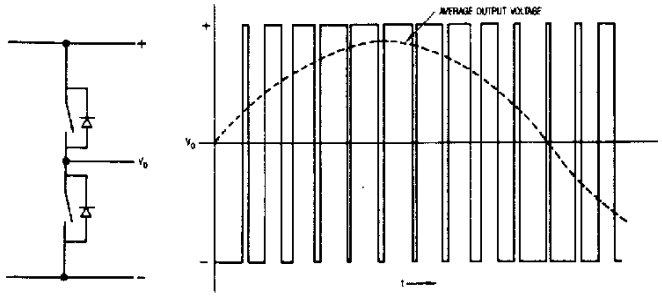


Figure 4a. Output voltage

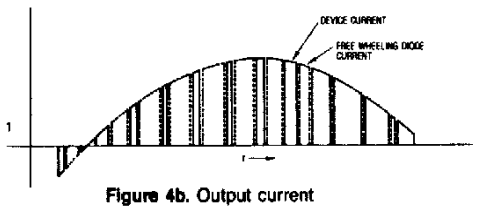


Figure 4b. Output current

Conclusions

There are two main conclusions resulting from this comparison analysis of insulated gate bipolar transistors versus power MOSFETs:

1. For most power conversion applications, there exists a tradeoff between silicon and aluminum i.e., a smaller die size could be used (with its higher losses and poorer thermal performance) coupled with a big heatsink *or* a larger die size could be used (leading to lower losses and better R_{thjc}) and a smaller heatsink. The choice depends upon the relative costs of the components, and any constraints on the size, weight, or cost of the final system. Often it is more cost effective to choose silicon rather than aluminum.

2. IGBTs tend to be more cost effective than MOSFETs in motor drive/UPS applications above 1 hp. This study has focused on inverters consisting of discrete components to arrive at the 1 hp crossover point. However, if all the power components were to be packaged together in a single module, the crossover point could, in fact, be at a lower power because a much smaller IGBT can do the job of a HEXFET power MOSFET. As the cost of a module significantly depends on its size, an IGBT module could be less expensive than a HEXFET module, thus driving the crossover point down. □

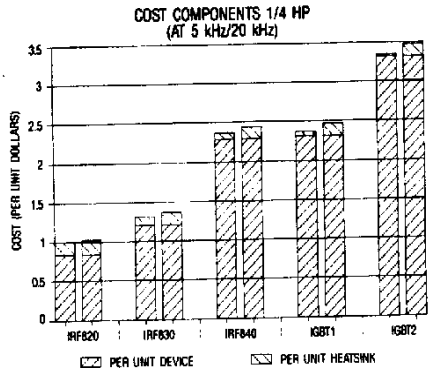


Figure 5a

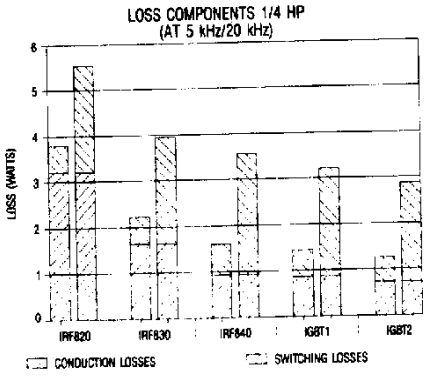


Figure 5b

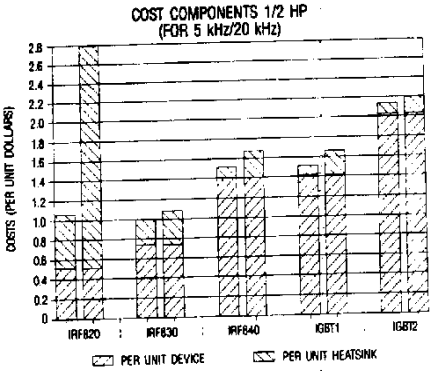


Figure 6a

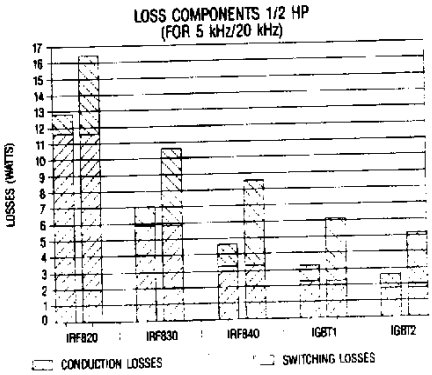


Figure 6b

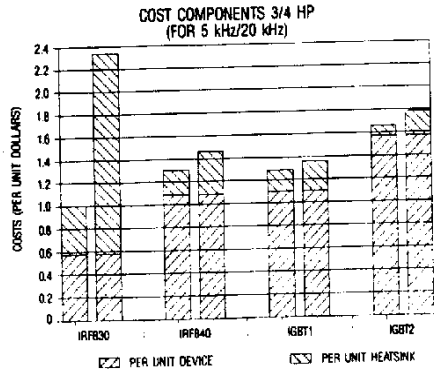


Figure 7a

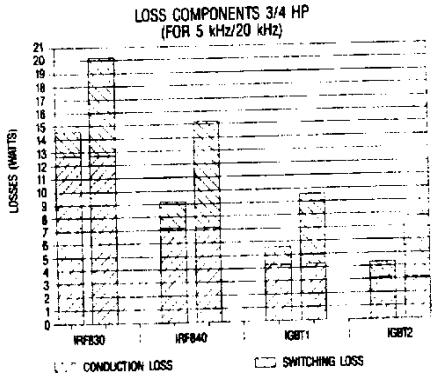


Figure 7b

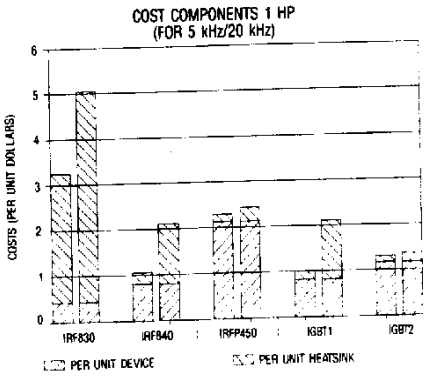


Figure 8a

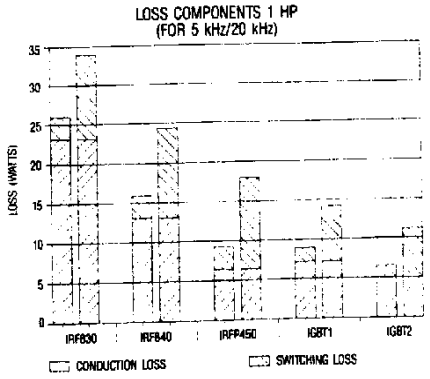


Figure 8b

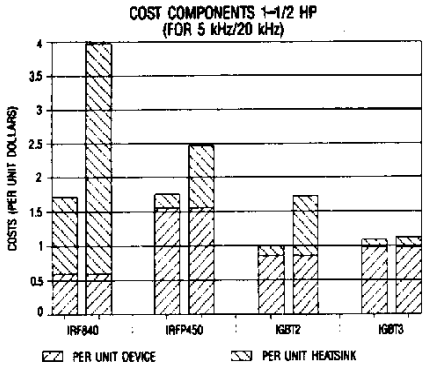


Figure 9a

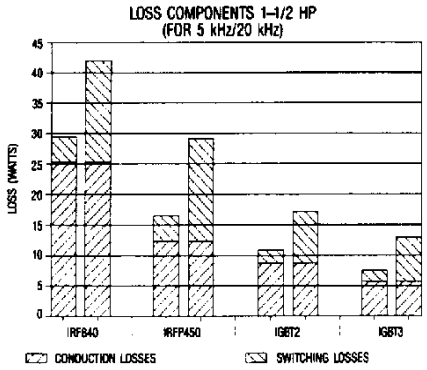


Figure 9b

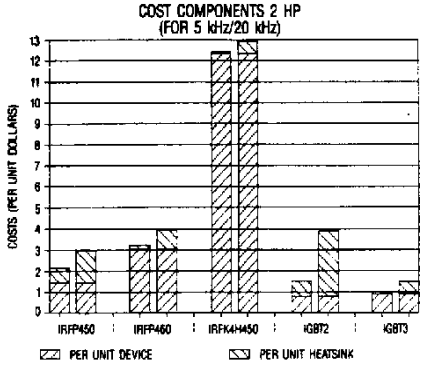


Figure 10a

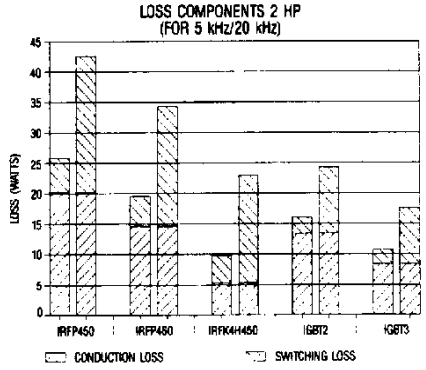


Figure 10b

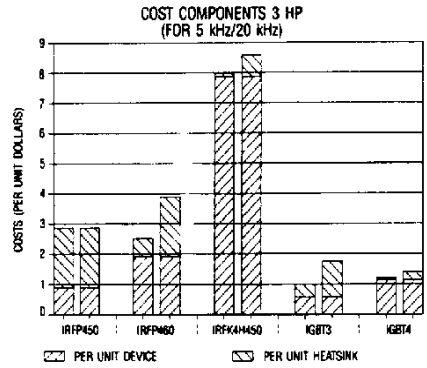


Figure 11a

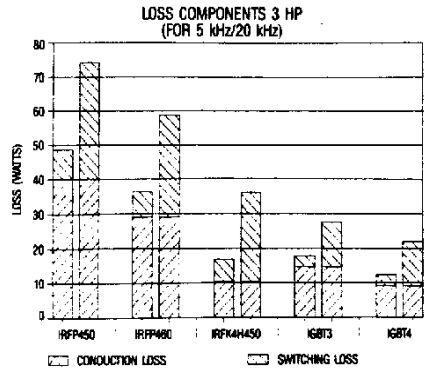


Figure 11b

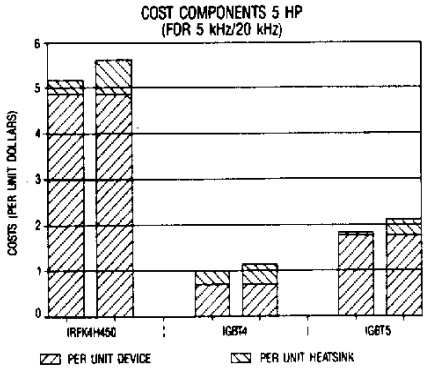


Figure 12a

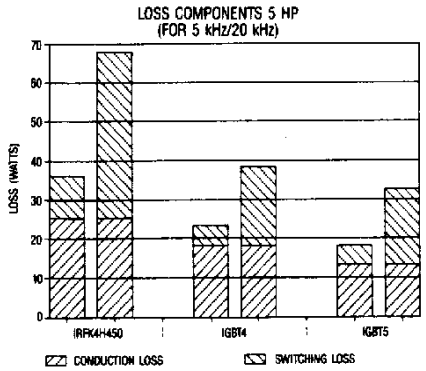


Figure 12b

COST COMPARISON: HEXFETs VS. IGBTs
(AT 5 kHz PWM)

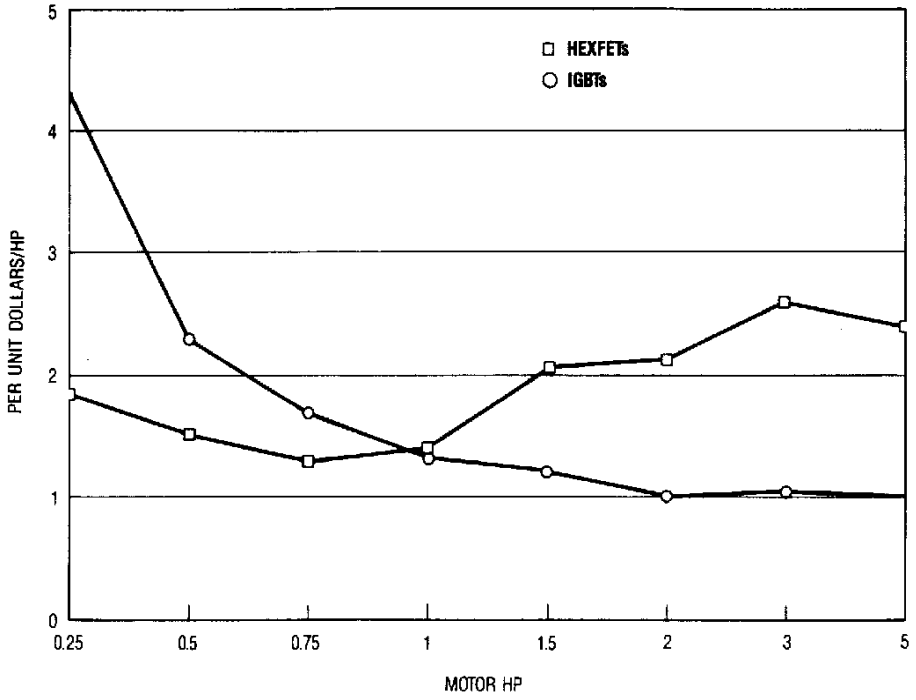


Figure 13

COST COMPARISON: HEXFETs VS. IGBTs
(AT 20 kHz PWM)

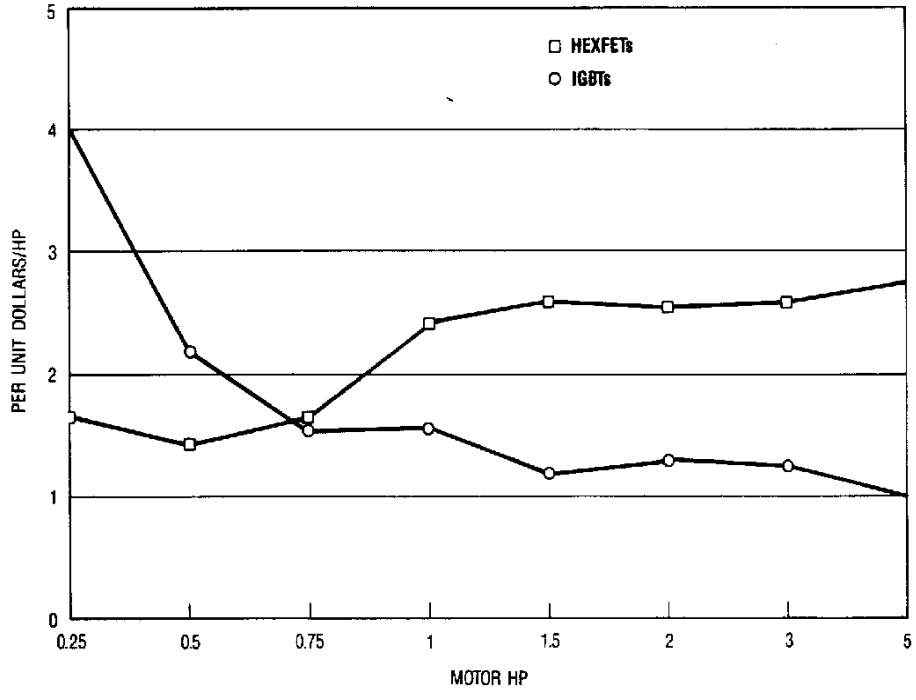
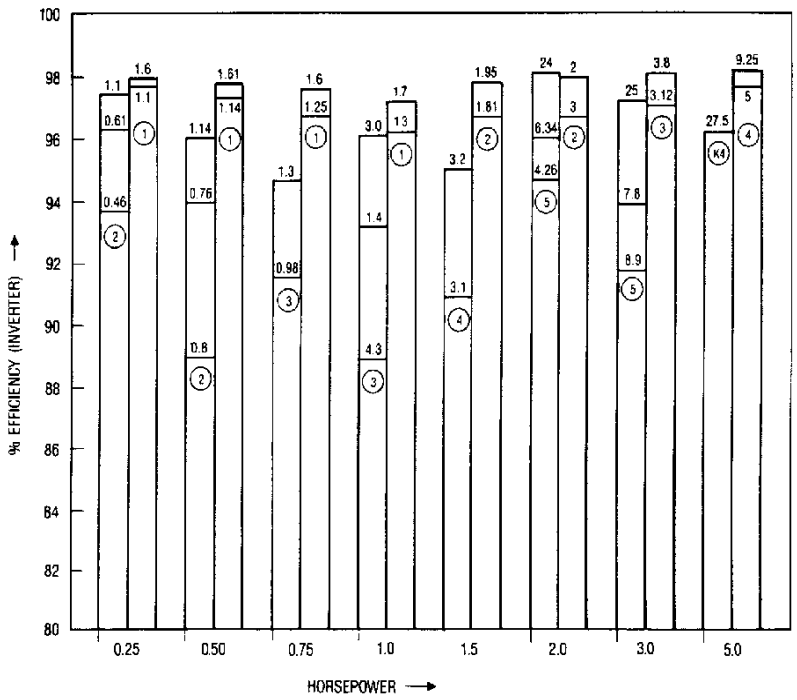


Figure 14

SYSTEM COST/EFFICIENCY TRADEOFF: HEXFETs AND IGBTs AT 5 kHz PWM



LEGEND (Figures 15 and 16)

1) Each pair of bars indicate HEXFET choices available (left bar) and IGBTs available (right bar) for a given inverter hp rating.

2) ② – Indicates smallest HEX die size evaluated. Subsequent bar extensions represent next die size (apprx. 2x larger). Die progression is ② ③ ④ ⑤ ⑥ (K4). For a detailed description of HEX die sizes, see Application Note AN-964.

3) (K4) – HEXpak module containing four HEX-5 die in parallel.

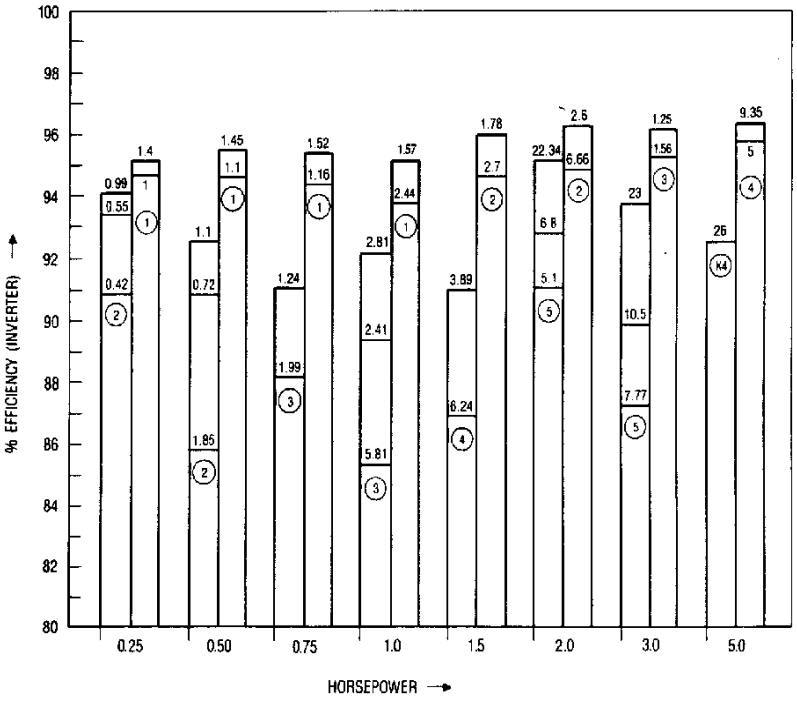
4) ① ② ③ ④ – Indicates smallest IGBT die size evaluated.

5) Normalized per unit dollar cost (e.g., 1.45) is shown at each horizontal level.

6) See page 3 for further explanation.

Figure 15

SYSTEM COST/EFFICIENCY TRADEOFF: HEXFETs AND IGBTs AT 20 kHz PWM



See Legend above for explanation of bar symbols.

Figure 16

International
IOR Rectifier

APPLICATION NOTE

AN978

International Rectifier · 233 Kansas Street El Segundo CA 90245 USA

HV Floating MOS-Gate Driver ICs

(HEXFET is a trademark of International Rectifier)

Topics Covered:

Gate drive requirements of high side devices
Block diagram of a typical MGD
Bootstrap operation
How to select the bootstrap components
How to calculate the power dissipation in the MGD
How to deal with negative transients
Layouts and other guidelines
How to isolate the logic from the power circuit
How to boost the output current of an MGD to drive modules
How to provide a continuous gate drive
How to provide a negative gate drive
Driving Buck converters
Driving Dual-Forwards and switched reluctance motor controllers
Cycle-by-cycle current control by means of the SD pin
Brushless and induction motor drives
Push-pull and other low-side applications
Driving a high-side P-Channel MOSFET
How to drive thyristor gates
Troubleshooting guidelines

1. GATE DRIVE REQUIREMENTS OF HIGH-SIDE DEVICES

The gate drive requirements for a power MOSFET or IGBT utilized as a high side switch (drain connected to the high voltage rail, as shown in Figure 1) driven in full enhancement, i.e., lowest voltage drop across its terminals, can be summarized as follows:

1. Gate voltage must be 10-15V higher than the drain voltage. Being a high side switch, such gate voltage would have to be higher than the rail voltage, which is frequently the highest voltage available in the system.
2. The gate voltage must be controllable from the logic, which is normally referenced to ground. Thus, the control signals have to be level-shifted to the source of the high side power device, which, in most applications, swings between the two rails.
3. The power absorbed by the gate drive circuitry should not significantly affect the overall efficiency.

With these constraints in mind, several techniques are presently used to perform this function, as shown in principle in Table I. Each basic circuit can be implemented in a wide variety of configurations.

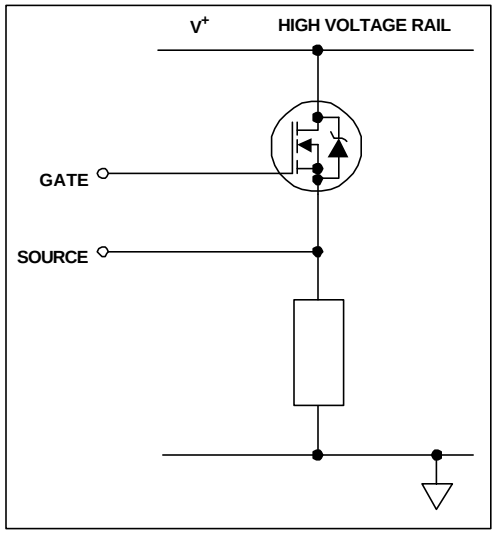


Figure 1. Power MOSFET in high side configuration

International Rectifier's family of MOS-gate drivers (MGDs) integrate most of the functions required to drive one high side and one low side power MOSFET or IGBT in a compact, high performance package. With the addition of few components, they provide very fast switching speeds, as shown in Table II for the IR2110, and low power dissipation. They can operate on the bootstrap principle or with a floating power supply. Used in the bootstrap mode, they can operate in most applications from frequencies in the tens of Hz up to hundreds of kHz.

2. A TYPICAL BLOCK DIAGRAM

The block diagram of the IR2110 will be used to illustrate the typical structure of most MGDs (Figure 2). It comprises a drive circuit for a ground referenced power transistor, another for a high side one, level translators and input logic circuitry.

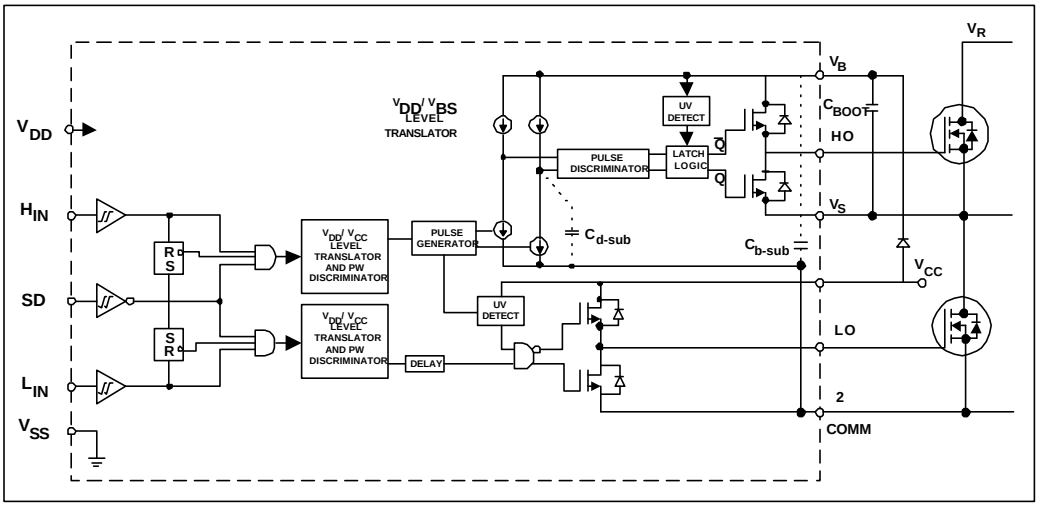


Figure 2. Block Diagram of the IR2110

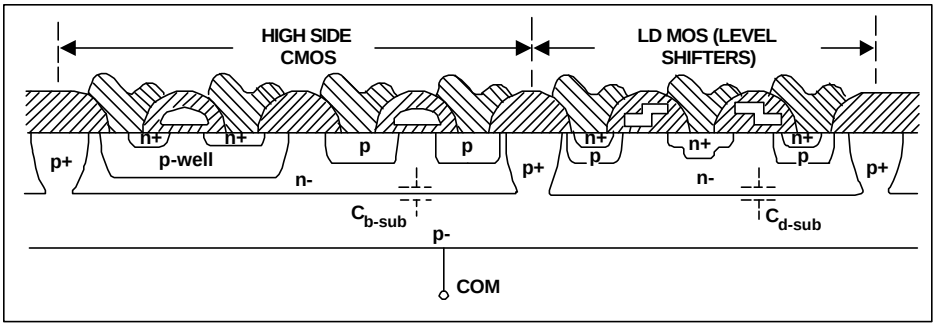


Figure 3. Silicon crossection showing the parasitic capacitances.

2.1 Input logic

Both channels are controlled by TTL/CMOS compatible inputs. The transition thresholds are different from device to device. Some MGDs, (IR211x and IR215x) have the transition threshold proportional to the logic supply V_{DD} (3 to 20V) and Schmitt trigger buffers with hysteresis equal to 10% of V_{DD} to accept inputs with long rise time. Other MGDs (IR210x, IR212x, IR213x) have a fixed transition from logic 0 to logic 1 between 1.5 to 2 V. Some MGDs can drive only one high-side power device. Others can drive one high-side and one low-side power device. Others can drive a full three-phase bridge. It goes without saying that any high-side driver can also drive a low side device. Those MGDs with two gate drive channel can have dual , hence independent, input commands or a single input command with complementary drive and predetermined deadtime.
Those application that require a minimum deadtime should use MGDs with independent drive and relay on a few passive components to build a deadtime, as shown in Section 12. The propagation delay between input command and gate drive output is approximately the same for both channels at turn-on (120ns) as well as turn-off (95ns) with a temperature dependence characterized in the data sheet. The shutdown function is internally latched by a logic 1 signal and activates the turn off of both power devices.

The first input command after the removal of the shutdown signal clears the latch and activates its channel. This latched shutdown lends itself to a simple implementation of a cycle-by-cycle current control, as exemplified in Section 12. The signals from the input logic are coupled to the individual channels through high noise immunity level translators. This allows the ground reference of the logic supply (V_{SS} on pin 13) to swing by ±5V with respect to the power ground (COM). This feature is of great help in coping with the less than ideal ground layout of a typical power conditioning circuit. As a further measure of noise immunity, a pulse-width discriminator screens out pulses that are shorter than 50ns or so.

2.2 Low Side Channel

The output stage is implemented either with two N-Channel MOSFETs in totem pole configuration (source follower as a current source and common source for current sinking), or with an N-Channel and a P-Channel CMOS inverter stage. Each MOSFET can sink or source gate currents from 0.12 to 2A, depending on the MGD. The source of the lower driver is independently brought out to pin 2 so that a direct connection can be made to the source of the power device for the return of the gate drive current. The relevance of this will be seen in Section 5. An undervoltage lockout prevents either channel from operating if V_{CC} is below the specified value (typically 8.6/8.2V).
Any pulse that is present at the input command for the low-side channel when the UV lockout is released turns on the power transistor from the moment the UV lockout is released. This behavior is different from that of the high-side channel, as we will see in the next section.

2.3 High side channel

This channel has been built into an “isolation tub” (Figure 3) capable of floating from 500 or 600V to -5V with respect to power ground (COM). The tub “floats” at the potential of V_S, which is established by the voltage applied to V_B. Typically this pin is connected to the source of the high side device, as shown in Figure 2 and swings with it between the two rails.

f an isolated supply is connected between this pin and V_S , the high side channel will switch the output (HO) between the positive of this supply and its ground in accordance with the input command.
One significant feature of MOS-gated transistors is their capacitive input characteristic, i.e., the fact that they are turned on by supplying a charge to the gate rather than a continuous current. If the high side channel is driving one such device, the isolated supply can be replaced by a capacitor, as shown in Figure 2.

I The gate charge for the high side MOSFET is provided by the bootstrap capacitor which is charged by the 15V supply through the bootstrap diode during the time when the device is off (assuming that V_S swings to ground during that time, as it does in most applications). Since the capacitor is charged from a low voltage source the power consumed to drive the gate is small. The input commands for the high side channel have to be level-shifted from the level of COM to whatever potential the tub is floating at which can be as high as 500V. As shown in Figure 2 the on/off commands are transmitted in the form of narrow pulses at the rising and falling edges of the input command. They are latched by a set/reset flip-flop referenced to the floating potential.

The use of pulses greatly reduces the power dissipation associated with the level translation. The pulse discriminator filters the set/reset pulses from fast dv/dt transients appearing on the V_S node so that switching rates as high as 50V/ns in the power devices will not adversely affect the operation of the MGD. This channel has its own undervoltage lockout (on some MGDs) which blocks the gate drive if the voltage between V_B and V_S, i.e., the voltage across the upper totem pole is below its limits (typically 8.7/8.3V). The operation of the UV lockout differs from the one on V_{CC} in one detail: the first pulse *after* the UV lockout has released the channel changes the state of the output. The high voltage level translator circuit is designed to function properly even when the V_S node swings below the COM pin by a voltage indicated in the datasheet, typically 5 V. This occurs due to the forward recovery of the lower power diode or to the Ldi/dt induced voltage transient. Section 5 gives directions on how to limit this negative voltage transient.

3. HOW TO SELECT THE BOOTSTRAP COMPONENTS

As shown in Figure 2 the bootstrap diode and capacitor are the only external components strictly required for operation in a standard PWM application. Local decoupling capacitors on the V_{CC} (and digital) supply are useful in practice to compensate for the inductance of the supply lines.

The voltage seen by the bootstrap capacitor is the V_{CC} supply only. Its capacitance is determined by the following constraints:

1. Gate required to enhance MGT
2. I_{qbs} - quiescent current for the high side driver circuitry
3. Currents within the level shifter of the control IC
4. MGT gate-source forward leakage current
5. Bootstrap capacitor leakage current

Factor 5 is only relevant if the bootstrap capacitor is an electrolytic capacitor, and can be ignored if other types of capacitor are used. Therefore it is always better to use a non-electrolytic capacitor if possible. For more detailed information on bootstrap component selection see **DT98-2 "Bootstrap Component Selection for Control IC's"**.

The minimum bootstrap capacitor value can be calculated from the following equation:

where:

$$C = 15 \times \frac{2\left[2Q_g + \frac{I_{qbs(\max)}}{f} + Q_{ls} + \frac{I_{Cbs(leak)}}{f}\right]}{V_{cc} - V_f - V_{LS}}$$

Q_g=Gate charge of high side FET
$I_{cbs(leak)}$=Bootstrap capacitor leakage current
V_f= Forward voltage drop across the bootstrap diode
Q_{ls} = level shift charge required per cycle = 5nC (500V/600V IC's) or 20nC (1200V IC's)
f=frequency of operation
I_{lson}=20mA, I_{lsoff}=20mA, t_w=200ns
V_{LS}= Voltage drop across the low side FET or load

The bootstrap diode must be able to block the full voltage seen in the specific circuit; in the circuits of Figures 25, 28 and 29 this occurs when the top device is on and is about equal to the voltage across the power rail. The current rating of the diode is the product of gate charge times switching frequency. For an IRF450 HEXFET power MOSFET operating at 100kHz it is approximately 12mA.

The high temperature reverse leakage characteristic of this diode can be an important parameter in those applications where the capacitor has to hold the charge for a prolonged period of time. For the same reason it is important that this diode be ultrafast recovery to reduce the amount of charge that is fed back from the bootstrap capacitor into the supply.

4. HOW TO CALCULATE THE POWER DISSIPATION IN AN MGD

The total losses in an MGD result from a number of factors that can be grouped under high voltage and low voltage static and dynamic.

a) Low voltage static losses ($P_{D(1v)q}$) are due to the quiescent currents from the three low voltage supplies V_{DD}, V_{CC} and V_{SS}. In a typical 15V application these losses amount to approximately 3.5mW at 25°C, going to 5mW at T_J = 125 °C .

b) Low voltage dynamic losses ($P_{D(lv)SW}$) on the V_{CC} supply are due to two different components:

b1) Whenever a capacitor is charged or discharged through a resistor, half of energy that goes into the capacitance is dissipated in the resistor. Thus, the losses in the gate drive resistance, internal and external to the MGD, for one complete cycle is the following:

$$P_G = V \bullet Q_G \bullet f$$

For two IRF450 HEXFETs operated at 100kHz with Vgs = 15V, we have:

$$PG = 2 \bullet 15 \bullet 120 \text{ E } 10^{-9} \bullet 100 \text{ E } 10^3 = 0.36W$$

The factor 2 in the formula is valid in the assumption that two devices are being driven, one per channel. If V_{SS} is generated with a bootstrap capacitor/diode, this power is supplied from V_{CC}. The use of gate resistors reduces the amount of gate drive power that is dissipated inside the MGD by the ratio of the respective resistances. If the internal resistance is 6 Ohms, sourcing or sinking, and if the gate resistor is 10 Ohms, only 6/16 of P_G is dissipated within the MGD. These losses are not temperature dependent.

b2)Dynamic losses associated with the switching of the internal CMOS circuitry. They can be approximated with the following formula:

$$P_{CMOS} = V_{CC} \bullet Q_{CMOS} \bullet f$$

with Q_{CMOS} between 5 and 30nC, depending on MGD. In a typical 100kHz application these losses would amount to tens of mW, largely independent from temperature.

c) High voltage static losses ($P_{D(hv)q}$) are mainly due to the leakage currents in the level shifting stage. They are dependent on the voltage applied on the V_S pin and they are proportional to the duty cycle, since they only occur when the high side power device is on. If Vs were kept continuously at 400V they would typically be 0.06mW at 25°C, going to 2.25mW at 125°C. These losses would be virtually zero if V_S is grounded, as in a push-pull or similar topology.

d) High voltage switching losses ($P_{D(hv)sw}$) comprise two terms, one due to the level shifting circuit (Figure 2) and one due to the charging and discharging of the capacitance of the high side p-well ($C_{b\text{-}sub}$ in Figure 3).

d1) Whenever the high side flip-flop is reset, a command to turn-off the high side device (i.e., to set the flip-flop) causes a current to flow through the level-shifting circuit. This charge comes from the high voltage bus through the power device and the bootstrap capacitor. If the high side flip-flop is set and the low side power device is on, a command to reset it causes a current to flow from Vcc, through the diode. Thus, for a half-bridge operating from a rail voltage V_R, the combined power dissipation is:

$$(V_R + V_{CC}) \bullet Q_P \bullet f$$

with Qp the charge absorbed by the level shifter, and f the switching frequency of the high side channel. Q_P is approximately 4nC at V_R = 50V, going to 7nC as the rail voltage increases to 500V. In a typical 400V, 100kHz application these losses would amount to approximately 0.3W. This includes the charging and discharging of $C_{d\text{-}sub}$. There is a third possible source for Q_P, when the high side flip-flop is being reset (i.e., the power device is being turned on) and the low side power device is off. In this case the charge comes from the high voltage bus, through the device capacitances and leakages or through the load. The power dissipation is somewhat higher than what would be calculated from the above expression. In a push-pull or other topology where V_S (pin 5) is grounded, both level shifting charges are supplied from V_{CC} with significantly lower losses.

d2) In a high-side/low-side power circuit the well capacitance $C_{b\text{-}sub}$ is charged and discharged every time V_S swings between V_R and COM. Charging current is supplied by the high voltage rail through the power device and the epi resistance. Discharge occurs through the lower device and the epi resistance. The losses incurred in charging or discharging a capacitor through a resistor are equal to QV/2, regardless of the value of resistance. However, much of these losses occur outside the bridge driver, since the epi resistance is negligible compared to the internal resistance of the power devices during their switching transitions. Assuming a charge value of 7nC at 450V and an operating frequency of 100kHz, the *total* losses caused by the charging and discharging of this capacitance amount to:

$$Q \bullet V \bullet f = 7 \bullet 10^{-9} \bullet 450 \bullet 10^{5} = 0.31W$$

almost totally outside the IR2110. For all practical purposes, $C_{b\text{-}sub}$ cannot be distinguished from the output capacitance of the lower power device.
If V_S is grounded the capacitor is charged at a fixed voltage and these losses would be zero. $C_{b\text{-}sub}$ (like $C_{d\text{-}sub}$) is a reverse biased junction and its capacitance is a strong function of voltage. These charges are not temperature dependent.

The above discussion on losses can be summarized as follows:

· The dominant losses are switching and, in high voltage applications at 100kHz or above, the static losses in Item a and Item c can be neglected outright.

· The temperature dependence of the switching losses is not significant;

· The combined losses are a function of the control mode, as well as the electrical parameters and temperature.

Knowing the power losses in the MGD, the maximum ambient temperature can be calculated (and vice-versa) from the following expression:

$$T_{a\ max} = T_{j\ max} - P_D \bullet R_{thj\text{-}a}$$

where $R_{th\ j\text{-}a}$ is the thermal resistance from die to ambient.

The following example shows a typical breakdown of losses for two IRF830s in a half-bridge, from a 400 V rail, 100 kHz, no load, no gate resistors.

$P_{D(lv)q}$ 0.004W

$P_{D(lv)SW}$: $P_{CMOS} = 15 \cdot 16 \cdot 10^{-9} \cdot 100 \cdot 10^{3} = 0.024$

$P_{G} = 2 \cdot 15 \cdot 28 \cdot 10^{-9} \cdot 100 \cdot 10^{3} = 0.084$

$P_{D(hv)q}$ 0.002

$P_{D(hv)sw}$: $(400 + 200) \cdot 7 \cdot 10^{-9} \cdot 100 \cdot 10^{3} = 0.42$

Total 0.534

The value of 200V in the formula to calculate $P_{D(hv)sw}$ is appropriate at no load, since this case would be the third in Section 4.2.d.l, i.e. the output of the half-bridge settles on a voltage that is between the two rails.

The actual junction temperature can be measured while in operation by pulling lmA from the Shutdown pin with the help of an adjustable current source, like the LM334. The voltage at the pin is 650mV at 25°C, decreasing by 2mV/°C.

5. HOW TO DEAL WITH NEGATIVE TRANSIENTS ON THE V_S PIN

Of the problems caused by parasitics, one of the main issues for control ICs is a tendency for the V_S node to undershoot ground following switching events. Conversely, overshoot does not generally cause a problem due to the high differential voltage capability of International Rectifier's proven HVIC process.

International Rectifier control ICs are guaranteed completely immune to V_S undershoot of at least 5V, measured with respect to COM. If undershoot exceeds this level, the high side output will temporarily latch in its current state. Provided V_S remains within absolute maximum limits the IC will not suffer damage, however the high-side output buffer will not respond to input transitions while undershoot persists beyond 5V. This mode should be noted but proves trivial in most applications, as the high-side is not usually required to change state immediately following a switching event.

The signals listed below should be observed both in normal operation and during high-stress events such as short circuit or over-current shutdown, when di/dt is highest. Readings should always be taken directly across IC pins as shown in figure 4, so that contributions from parasitics in the drive coupling are included in the measurement.

(1) High side offset with respect to common; V_S-COM
(2) The floating supply; V_B - V_S

The following guidelines represent good practice in control IC circuits and warrant attention regardless of the observed latch-up safety margin.

Minimize the parasitics

1a. Use thick, direct tracks between switches with no loops or deviation.
1b. Avoid interconnect links. These can add significant inductance.
1c. Reduce the effect of lead-inductance by lowering package height above the PCB.
1d. Consider co-locating both power switches to reduce track lengths.

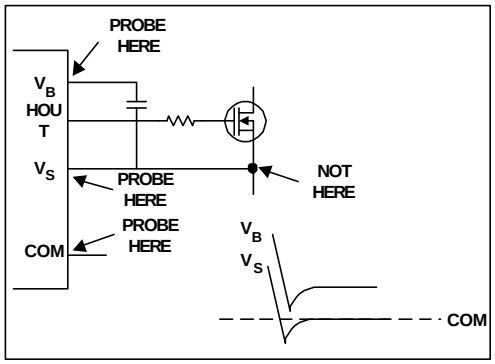


Figure 4. Look at the VS spike during the revers recovery. Always probe right at the IC pin.

Reduce control IC exposure.

2a. Connect V_S and COM as shown in figure 6.
2b. Minimize parasitics in the gate drive circuit by using short, direct tracks.
2c. Locate the control IC as close as possible to the power switches.

Improve local decoupling.

3a. Increase the bootstrap capacitor (Cb) value to above 0.47mF using at least one low-ESR capacitor. This will reduce overcharging from severe Vs undershoot.
3b. Use a second low-ESR capacitor from Vcc to COM. As this capacitor supports both the low-side output buffer and bootstrap recharge, we recommend a value at least ten times higher than Cb.
3c. Connect decoupling capacitors directly across appropriate pins as shown in figure 7.
3d. If a resistor is needed in series with the bootstrap diode, verify that V_B does not fall below COM, especially during start-up and extremes of frequency and duty cycle.

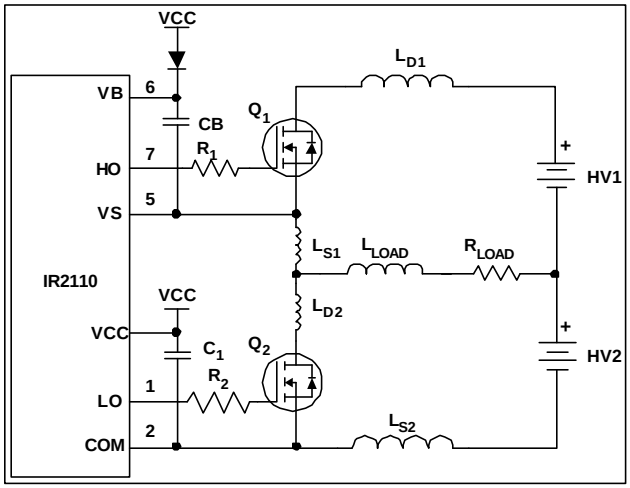


Figure 5a. A typical half-bridge circuit with stray inductances.

Granted proper application of the above guidelines, the effects of V_S undershoot will be minimized at source. If the level of undershoot is still considered too high, then some reduction of dv/dt may be necessary.

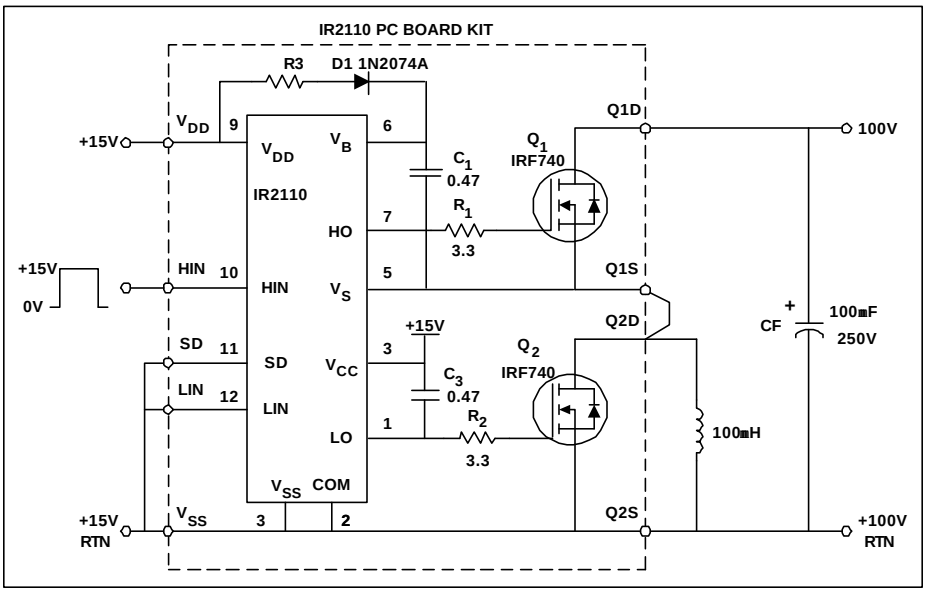


Figure 5b. Test Circuit

External snubbing and/or increasing gate drive resistance may be used to trade efficiency for lower switching rate. If the system will not tolerate this, then fast anti-parallel clamping diodes may be considered appropriate. HEXFRED diodes are ideal for this purpose.

For More detailed information on managing transients see **DT97-3 "Managing Transients in Control IC Driven Power Stages"**

6. LAYOUT AND OTHER GENERAL GUIDELINES

A typical half-bridge circuit is shown in Figure 5a, together with its stray inductances. It shows critical stray inductances located in the high current path which affect the operation of the circuit. L_{D1} and L_{S2} are in a "dc path" and are due to the wiring inductance between the MOSFETs and the decoupling capacitors; L_{S1} and L_{D2} are in an "ac path" and are due to the wiring inductance between the MOSFETs. The stray inductance in a dc path can be cancelled with a capacitor, those in an ac path cannot be compensated for.

This circuit has been implemented with the printed circuit board included in the IR2110 Bridge Driver Designer's Kit (part number IR2119), as shown in Figure 5b. To eliminate the effects of the inductance of the wiring between the power supply and the test circuit, a 100mF/250V electrolytic capacitor was connected between Q1D and Q2S terminals, as shown in Figures 6 and 7. This virtually eliminates any stray inductance in the dc path.

The associated waveforms are shown in Figure 8. When Q_1 turns off, the body diode of Q_2 carries the freewheeling current. The voltage spike across the freewheeling diode is approximately 10V, as shown in the top trace, due to the forward recovery of the diode and the internal packaging inductances.

However, the corresponding negative spike at pin 5 of the IR2110 is 50V, as shown by the lower trace. This is caused by the di/dt in the stray inductances L_{D2} and L_{S2} in the ac path and the fact that these inductances effectively isolate pin 5 from the clamping action of the freewheeling diode. The severity of the problem can be understood considering that by switching 10A in 20ns with a stray inductance of 50nH, a 25V spike is generated. A small paper clip has an inductance of 50 nH.
The most effective way of dealing with this spike is to reduce the stray inductance in the ac path. This can be done by mounting the source or emitter of the high-side device very close to the drain or collector of the low-side device, as shown in the layout of Figure 10.

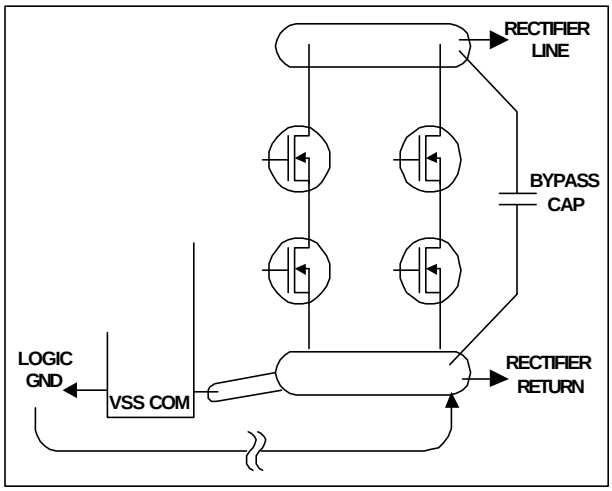


Figure 6. Ground connections and layout

After this inductance has been reduced to the lowest practical limit, the di/dt may have to be reduced by reducing the switching speed by means of the gate resistor. Driving MOS-gated power transistors directly from the IR2110 or similar MGD can result in unnecessarily high switching speeds. The circuit shown in figure 5b produced 4ns turn-off time with 0W series gate resistance and generated a negative spike of 90V at pin 5 of the IR2110. A graph of the negative spike and the turn-off time versus series gate resistance is shown in Figure 9.

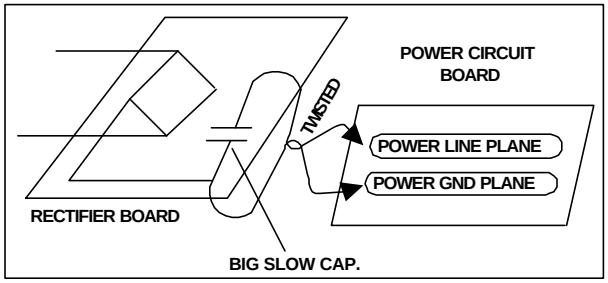


Figure 7. Power Bypass Capacitor

Increasing the value of the series gate resistor, the amplitude of the negative spike decreases rapidly, while the turn-off time is a linear function of the series gate resistance. Selecting a resistor value just right from the "knee" in Figure 9 provides a good trade-off between the spike amplitude and the turn-off speed. A 27W speed gate resistor was selected for the test circuit which resulted in an 18V spike amplitude and set the turn-off time to 48ns. A parallel diode, with the anode towards the gate, across the gate resistor is also recommended. The diode is reverse biased at turn-on but holds the gate down at turn-off, and during the off state. The reduction in the turn-on speed reduces the spike of reverse recovery, as explained in Section 12 (see also Ref 2). The value of gate resistor should be as low as the layout allows, in terms of overvoltage on the device and negative spikes on the V_S pin.

The layout should also minimize the stray inductance in the charge/discharge loops of the gate drive to reduce oscillations and to improve switching speed and noise immunity, particularly the "dv/dt induced turn-on". To this end, each MOSFET should have a dedicated connection going directly to the pin of the MGD for the return

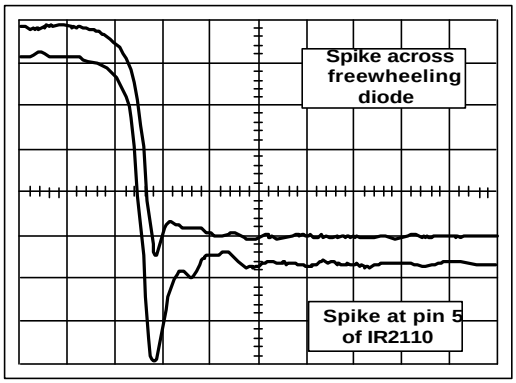


Figure 8. Waveform while Q1 turning off 20A inductive load (20ns/div and 20V/div)

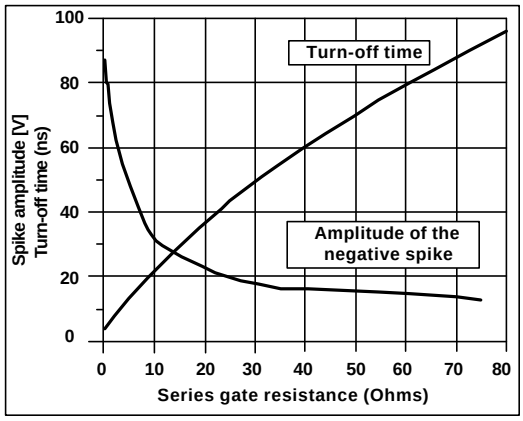


Figure 9. Series gate resistance vs. the amplitude of the negative voltage spike and the turn-off time.

of the gate drive signal. Best results are obtained with a twisted pair connected, on one side, to gate and source, on the other side, to gate drive and gate drive return.

On PC boards parallel tracks should be used. The layout shown in Figure 10 is reduces the stray inductances in the ac path, in the dc path, as well as the stray inductance in the gate drive loop. In this circuit the voltage differential measured between the gate pin of the power MOSFET and the drive pin of the IR2110 during a fast transient was in excess of 2V.

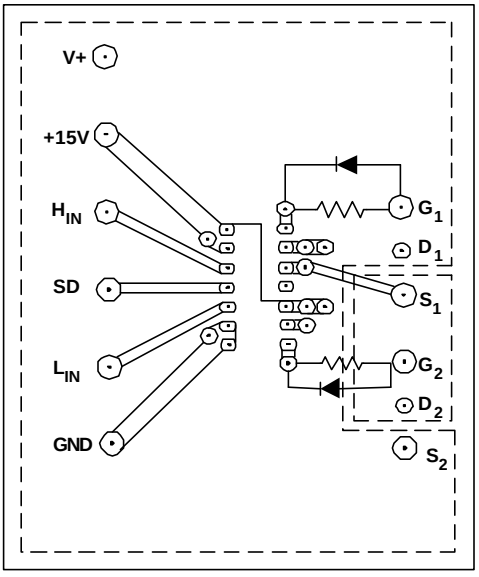


Figure 10. IR2110 test circuit Note: Dotted lines represent pads on bottom side of board. V+, GND, D1, S1, D2, S2, terminals have plated through holes

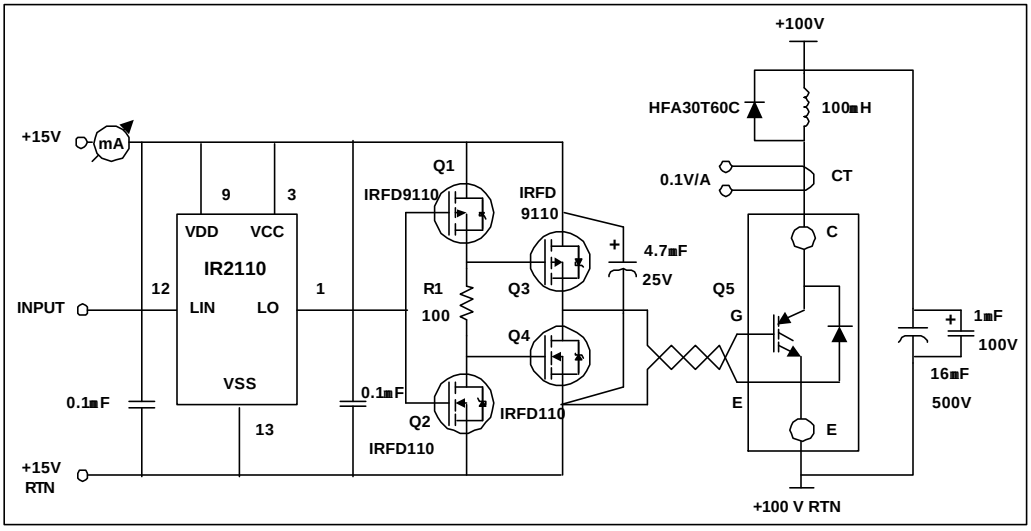


Figure 11. Test Circuit

7. HOW TO BOOST GATE DRIVE CURRENT TO DRIVE MODULES

Modules and other paralleled MOS-gated power transistors require significantly more current and lower gate drive impedance than what a typical MGD can provide. The high input impedance power buffer shown in Figure 11 delivers 8A peak output current. It can be mounted close to the power module, thus reducing the inductance of the gate drive loop and improving the immunity to dv/dt induced turn-on. It draws negligible quiescent current and can still be supplied by a bootstrap capacitor. The buffer receives its drive signal from the IR2110 or, preferably, an MGD with lower gate drive capability, and drives an IGBT module which has a total gate charge of 600 nC. Q1 and Q2 are low current drivers for Q3 and Q4 which can be sized to suit the peak output current requirement. When the input signal changes state, R1 limits the current through Q1 and Q2 for the few nanoseconds that both transistors are on. When the input settles to its new state, the driver transistor quickly discharges the gate capacitance of the conducting output transistor forcing it into off-state. Meanwhile the gate of the other output transistor will be charged through R1; the turn-on will be delayed by the RC time constant formed by R1 and the input capacitance of the output transistor.

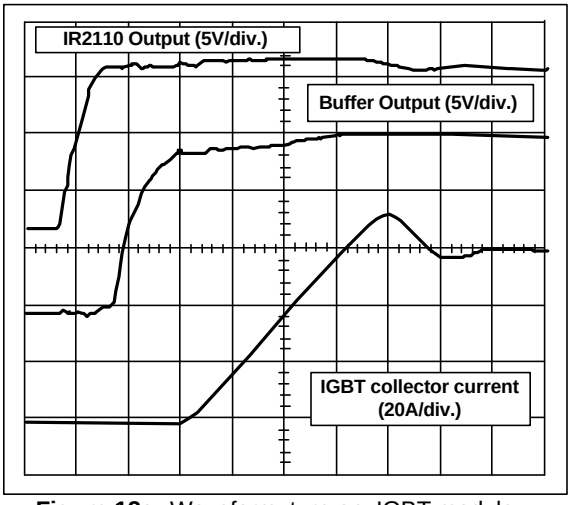


Figure 12a. Waveform, turn-on, IGBT module switching inductive load of 60A. (50ns/div.)

The typical switching performance while driving an inductive load current of 60A is shown in Figure 12. Turn-on and turn-off delays are 50nS. Rise and fall times are less than 40nS. The buffer was tested with a 0.1mF capacitive load, as shown in Figure 13. The ringing was due to the resonant circuit at the output, formed by the capacitive load and the stray inductances. The current consumption vs. frequency plot is shown in Figure 14. It is possible to use lower on-resistance, lower voltage HEXFETs in the booster stage, but it was found that the large reduction in $R_{DS(on)}$ gave rise to large peak currents which caused a great deal of noise and ringing in the circuit.

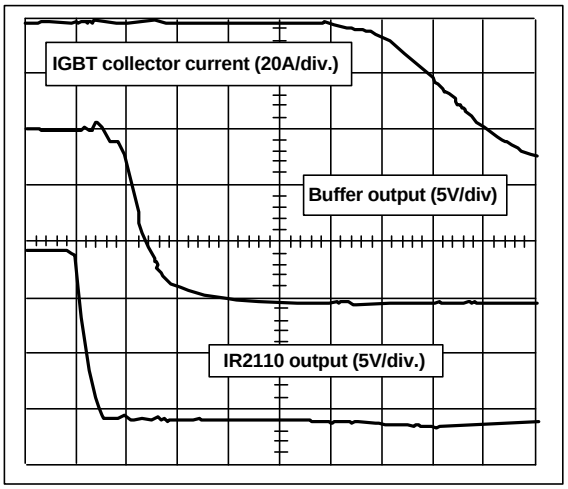


Figure 12b. Waveform, turn-off. Propagation delay is 50ns, fall time is less than 40ns when driving 600nC gate charge of the module 50ns/div.

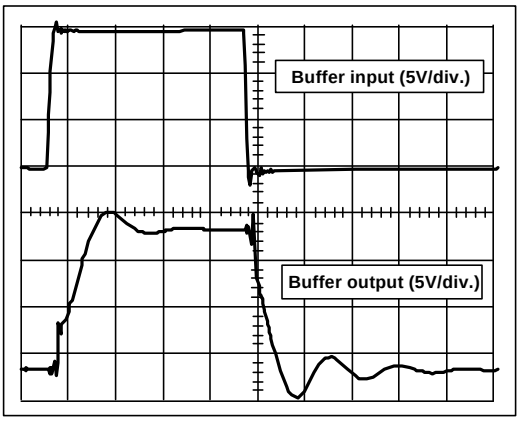


Figure 13. Waveform driving 0.1mF capacitor (250nS/div.)

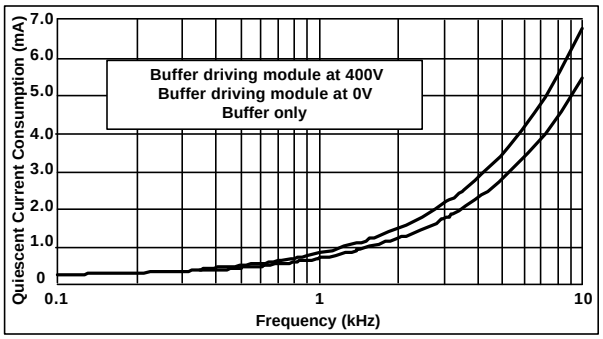


Figure 14. Current consumption vs. frequency

A typical use for this buffer is shown in Figure 15. Use good quality 10 mF tantalum or 10 mF electrolytic and 0.l mF ceramic capacitors at the output of the buffer. These decoupling capacitors should be mounted physically close to the output HEXFETs to nullify the effects of stray inductance. They reduce the ringing at the gate during turn-on.

Use short, tightly twisted wires between the output of the buffers and the modules. Use a single point ground at the emitter of the bottom IGBT module. In a bridge configuration, connect the emitters of the bottom IGBT modules to a common point with short heavy wires. Use this point as a common ground.

8. HOW TO PROVIDE A CONTINUOUS GATE DRIVE

Some applications, like brushless dc motors, require that the high-side device be on for an indefinite period of time. Under these conditions the charge in the bootstrap capacitor. Isolated supplies are normally used for this purpose.

They add cost and are frequently responsible for spurious turn-on of the power devices due to the coupling of the switching dv/dt through the interwinding capacitance of their transformer. An inexpensive alternative to an isolated supply is the charge pump circuit shown in Figure 16. The IR2125 MGD was selected to demonstrate the cooperation of the charge pump and the bootstrap circuits. The IR2125 also has linear current limiting and time-out shut down capability, providing protection for the MOS-gated device. To provide the low operating current requirement of the IR2125, the charge pump employs a CMOS version of the 555 timer.

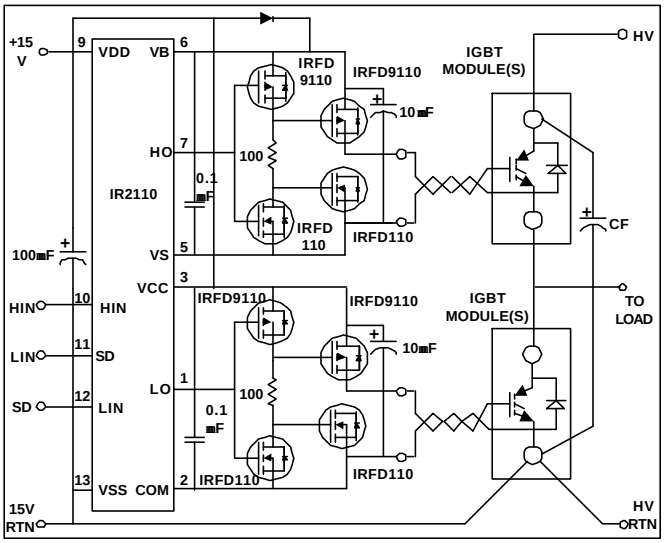


Figure 15. Application circuit schematic

When the IGBT is off, the bootstrap capacitor is charged through the bootstrap diode and the load resistor. When the IGBT is on, the 100k resistor connected to ground charges the 100nF capacitor connected between pins 1 and 8 of the 555 timer generating -15V referenced to pin 5 of the IR2125. The charge pump circuit formed by the two lN4148 diodes and the 10nF capacitor which converts the 7.5kHz square wave at pin 3 of the 555 timer to + 15V referenced to V_S and charges the bootstrap capacitor.
Figure 17 shows the circuit waveforms at start-up. As the IGBT turns on, the bootstrap diode disconnects pin 8 of the IR2125 from the +12V power supply, and the voltage across the bootstrap capacitor starts dropping. At the same time the 100k resistor located between pin 1 of the 555 timer and ground starts charging the 100nF capacitor connected to it and generates supply voltage for the CMOS (MAXIM ICL71555IPA) timer. The output voltage of the charge pump increases with increasing supply voltage. The charge pump maintains the voltage in the bootstrap capacitor, keeping the voltage above the undervoltage threshold level of the IR2125.

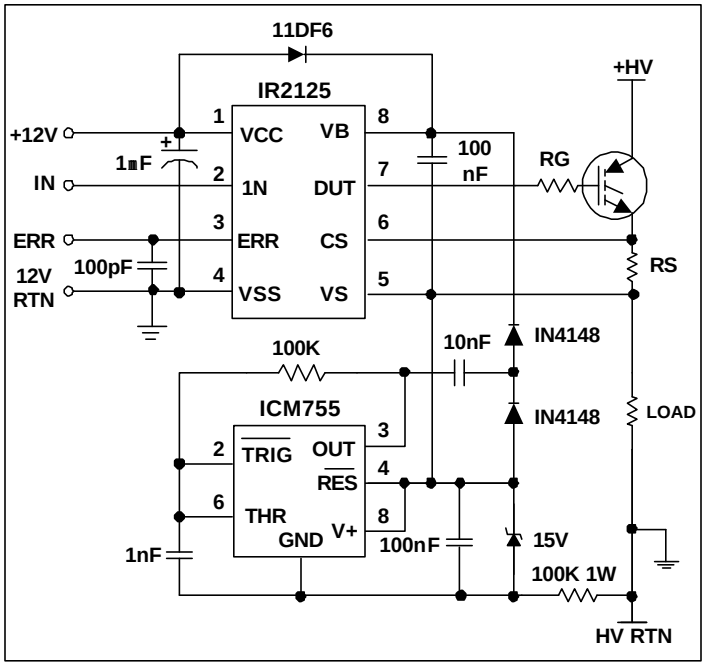


Figure 16. High-side drive provides fast switching, continuous on-time and switching device protection .

The following considerations should be kept in mind in the selection of the components:

- In selecting the zener, consider that he absolute maximum voltage supply voltage for the 555 is 18V

- The 100k lW (value valid for a 500V +HV supply) resistor should be sized according to the maximum supply current at the high side of the IR2125, the minimum operating power supply voltage and the timing requirements

- The supply current at the V_B pin (I_{QBS}) of the IR2125 increases with increasing temperature

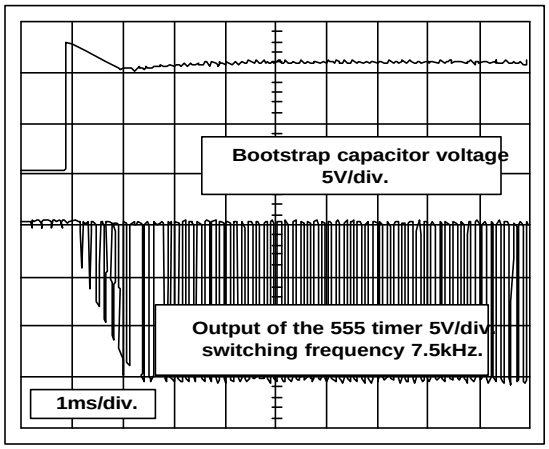


Figure 17. Waveform at start-up.

9. HOW TO GENERATE A NEGATIVE GATE BIAS

Inherently neither the MOSFET nor the IGBT requires negative bias on the gate. Setting the gate voltage to zero at turn-off insures proper operation and virtually provides negative bias relative to the threshold voltage of the device. However, there are circumstances when a negative gate drive or an other alternative may be necessary.

- The semiconductor manufacturer specifies negative gate bias for the device,
- When the gate voltage can not be held safely below the threshold voltage due to noise generated in the circuit.
- The ultimate in switching speed is desired

Although reference will be made to IGBTs, the information contained is equally applicable to power MOSFETs. The IGBTs made by International Rectifier do not require negative bias. The switching times and energy loss values that are published on the data sheets for both discretes and modules were measured at zero gate voltage turn-off. The problem of "dv/dt induced turn-on" arises when the voltage increases rapidly between the collector-emitter terminals of the IGBT.

During the transient, the gate-collector (Miller) capacitance delivers charge to the gate, increasing the gate voltage. The height and width of the voltage 'blip' at the gate is determined by the ratio of the gate-collector and gate-emitter capacitances, the impedance of the drive circuit connected to the gate, and the applied dv/dt between the collector-emitter terminals.

The following test was conducted to determine the threshold voltage and the effect of the series gate resistance in high dv/dt applications. The test circuit is shown in Figure 18. The positive bias to the upper IGBT was increased until the switching losses in the bottom IGBT indicated excessive shoot-through current. The turn-on loss was measured at 15A inductor current and 6V/ns switching speed. The results are shown in Figure 19.

The threshold voltage levels increasing the turn-on losses are 4V, 5V and 5.6V with 47W, 10W, and 0W series gate resistance, respectively. A parallel diode across the series gate resistor (anode toward the gate) helps clamp the gate low, so the series gate resistor can be sized according to the turn-on requirements.

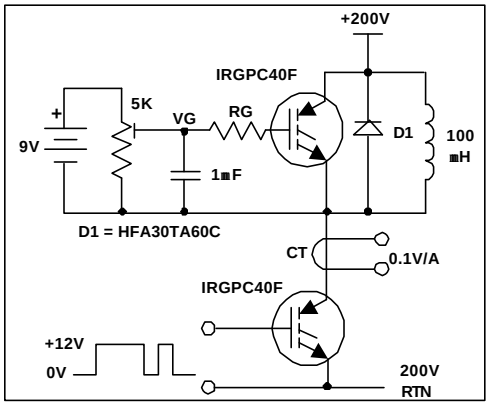


Figure 18. Test circuit

The current 'blip' due to charging the output capacitance (C_{oes}) of the IGBT is frequently mistaken for conduction current. The amplitude of the current 'blip' is approximately 5A for a IRGPC50F IGBT at a dv/dt of 20V/ns. The amplitude of the 'blip' does not change with the applied negative bias.

The basic buffer circuit and the negative charge pump are shown in Figure 20. The buffer circuit employs two p-channel and two n-channel MOSFETs. Resistor R1 between the gates of Q3 and Q4 slows down the turn-on of the output transistor and limits the shoot-through current in the drivers.

D1 reduces the voltage to the gate of Q3 and Q4. D2, C2 and R2 form a level shifter for Q2. C3, C4, D3 and D4 convert the incoming signal to negative DC voltage. After turn-on, the negative voltage settles in a few cycles even at extremely low or high duty cycles (1-99%). The settling time and the stiffness of the negative voltage are affected by the output impedance of the signal source.

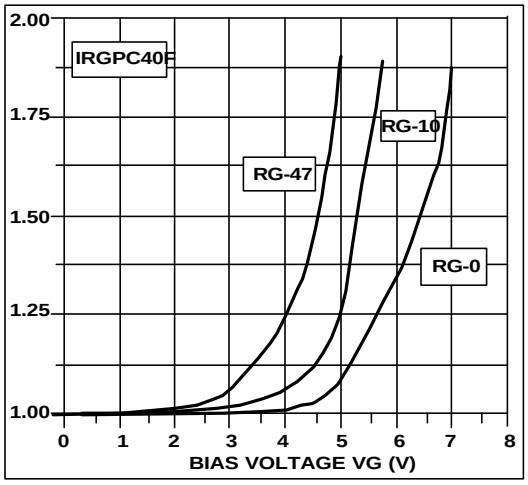


Figure 19. Turn-on losses vs. VG

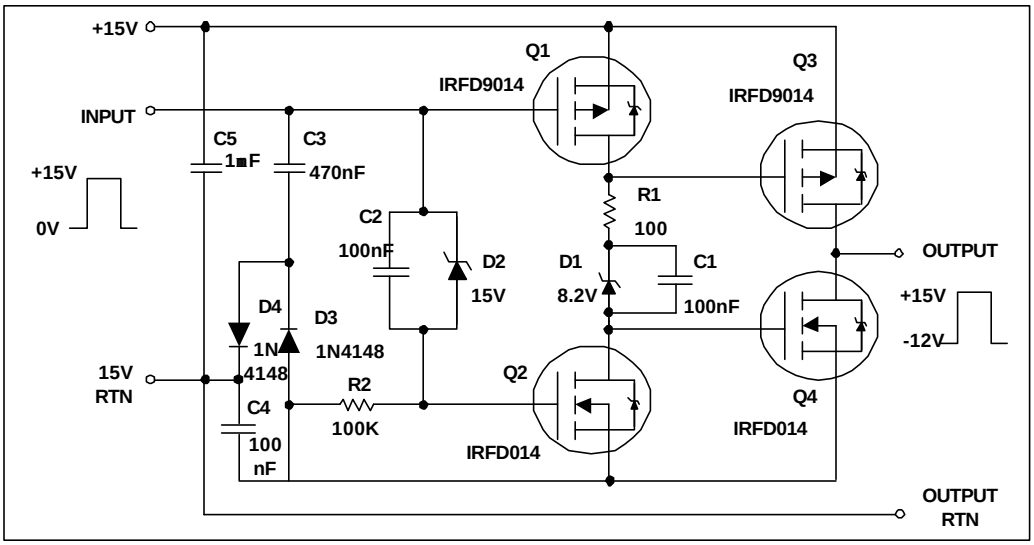


Figure 20. Buffer with negative charge pump

The circuit shown in Figure 21 utilizes the high voltage level shifting capability of the IR2110 combined with the drive capability and negative bias of the MOS buffer shown in Figure 20. The circuit was tested with two 270 A IGBT modules with 600 nC of gate charge. The waveforms are shown in Figure 22. The turn-on delay of the circuit is 1 mS, the turn-off delay is 0.2 mS .

The settling time of the negative bias voltage is about 10ms at 5kHz switching frequency at 50% duty cycle. At start-up, the circuit delivers some negative gate voltage even after the first cycle. During power down, the gate voltage remains negative until the reservoir capacitor discharges.

IMPORTANT NOTE: A negative gate drive is not required for IR IGBTs and IGBT modules. Also for NPT type IGBTs the negative gate drive is required to account for the significant change in the Ccg to Cge capacitance ratio. It is possible to eradicate the need for negative gate drive by adding gate capacitance, which reduces the Ccg to Cge ratio, and hence swamps out the miller effect, eliminating the false turn-on caused by the induced miller voltage on the gate.

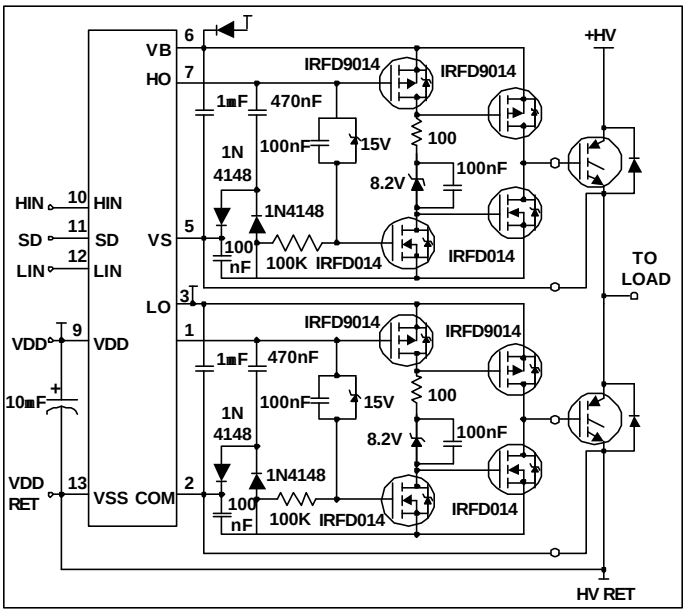


Figure 21. Half-Bridge drive that generates negative bias

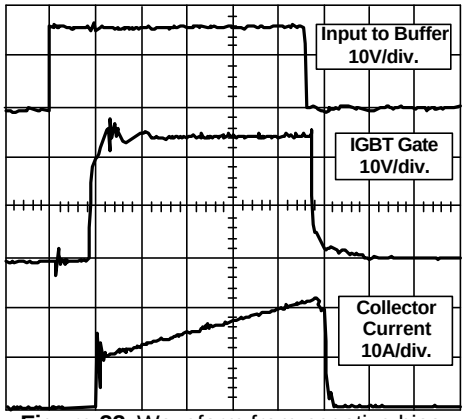


Figure 22. Waveform from negative bias Half-Bridge driver (1ms/div.)

10. HOW TO DRIVE A BUCK CONVERTER

Figure 25 shows a typical implementation of a buck converter with the high side drive function performed by the IR2117. The diode connected on COM prevents the negative spikes from affecting the operation of the IC and provides an extra measure of noise immunity. As mentioned before, COM *should not* be connected together.

At start-up the bootstrap capacitor is discharged and, in most applications would charge through the inductor and the filter capacitor. The same is true under no-load conditions, when the freewheeling diode may not conduct at all. This alternative path works, as long as the filter capacitor is at least 10 times larger than the bootstrap capacitor. The Q of this resonant circuit should be low enough to insure that the bootstrap capacitor does not get charged beyond the limits of V_{SS} (20V). If this is not so, a zener in parallel with the bootstrap capacitor would take care of possible overvoltages. This is true whether the dc-to-dc converter performs the function of a supply or speed control for a dc motor.

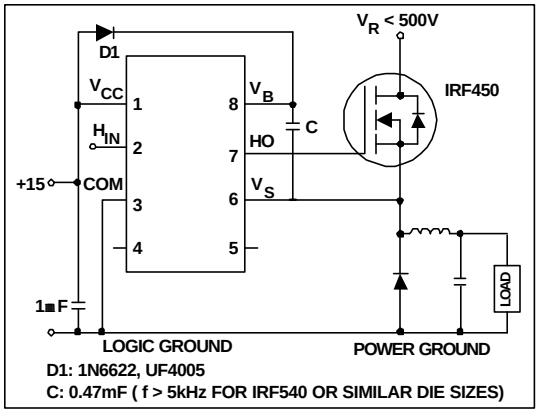


Figure 25. Buck Converter

In the following two cases, however, the recharging current for the bootstrap capacitor cannot flow neither in the diode, nor in the load:

1. In a typical battery charger applications, as the one shown in Figure 26, the +12V from the output appears at the V_S pin and reduces the voltage across bootstrap capacitor at start-up and the undervoltage protection in the MGD inhibits the operation.

2. When the regular PWM operation of the buck is interrupted due excessive voltage at the output. This is normally due to a sudden removal of a heavy load at the output which results in higher output voltage than the set value due to the limited speed of the control loop and the stored energy in the Ll inductor. With no load or light load at the output, the filter capacitor can keep the output high for long time while the CB is being discharged at faster rate by the leakage current of the high-side driver.

As shown in Figure 27, the addition of R1 provides an alternative charging path for the bootstrap capacitor. Because V_{IN} is higher than V_O,

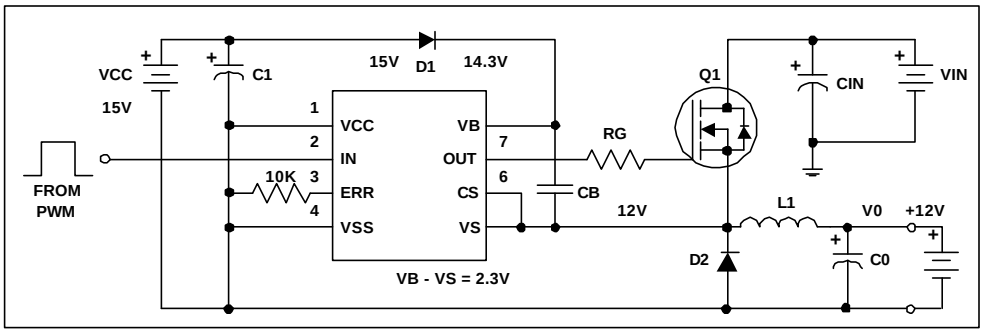


Figure 26. In battery charger applications, the +12V from the output appears at the V_S pin and reduces the voltage across CB at start-up and the undervoltage protection in the IR21XX inhibits the operatic

some charging current always flows through R1 even if V_S pin is sitting at V_O potential.

To keep CB charged the average current through R1 should be higher than the worst case leakage current. D3 should be a low level zener diode with sharp knee at low currents. The recommended part numbers for 12V and 15V are respectively: lN4110 and lN4107.

This technique can also be used in place of a dedicated supply to power the PWM controller, as well as the IR2110 and other auxilliary circuits, if the output voltage of the buck converter is between 10 and 20V.

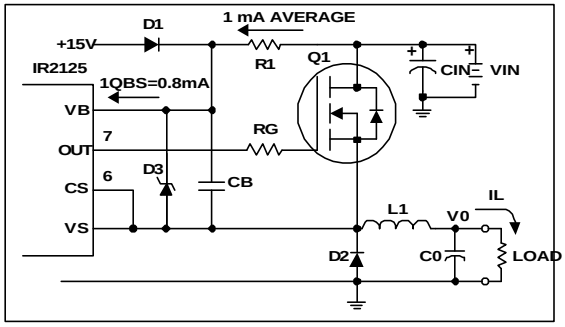


Figure 27. Adding R1 to the circuit, charging current can be derivated from VIN.

11. DUAL FORWARD CONVERTER AND SWITCHED RELUCTANCE MOTOR DRIVES

Figure 28 shows a bridge arrangement that is frequently used to drive the windings of a switched reluctance motor or a transformer in a dual forward converter.

The use of the IR2110 requires the addition of four to insure that the bootstrap capacitor is charged at turn on and in subsequent cycles, should the conduction time of the freewheeling diodes become very short.

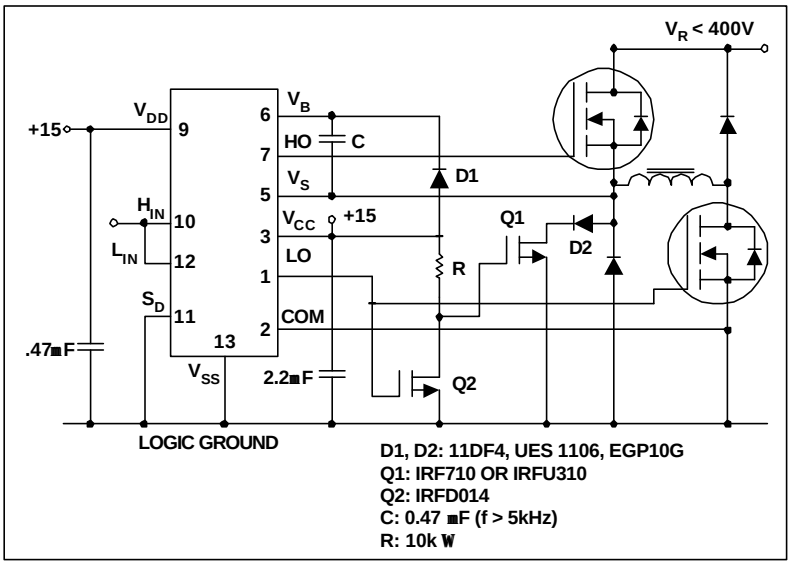


Figure 28. Dual forward converter and switched reluctance motors

12. FULL BRIDGE WITH CURRENT MODE CONTROL

Figure 29 shows an H bridge with cycle-by-cycle current control implemented with current sensing devices on the low side in combination with the shutdown pin of the IR2110. The detailed implementation of the current sensing circuit is dependent on the PWM technique used

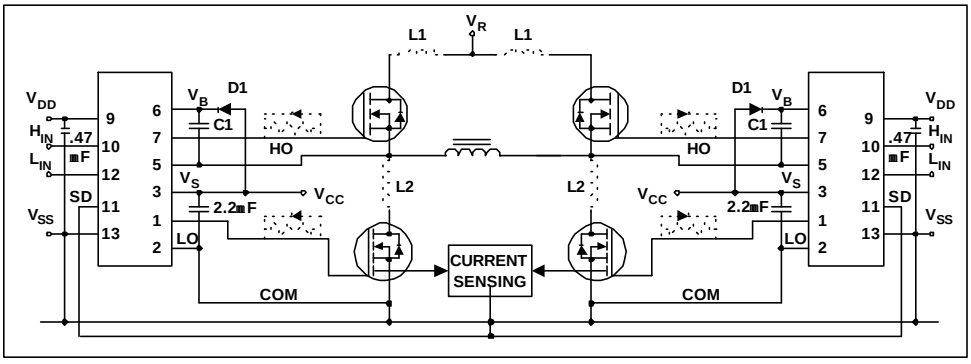


Figure 29. Typical implementation of all H-Bridge with cycle-by-cycle current mode control

to generate the desired output voltage, the accuracy required, the availability of a negative supply, bandwidth, etc. (Ref. 3, 4 and 5 cover these aspects in greater detail). As explained in Section 2.1, the shutdown function is latched so that the power MOSFETs will remain in the off-state as the load current decays through their internal diodes. The latch is reset at the beginning of next cycle, when the power devices are once again commanded on. As shown in Figures 6 and 7, decoupling capacitors mitigate the negative effects of L_1 . L_2 , on the other hand, must be reduced with a tight layout, as per Figure 10. The turn-on and turn-off propagation delays of the IR2110 are closely matched (worst case mismatch: 10ns), with the turn-on propagation delay 25ns longer than the turn-off. This, by itself, should insure that no conduction overlap of the power devices would occur, even if the on and off input command coincide. As an added safety margin a resistor diode network can be added to the gate, as shown with dashed lines in Figure 29. The purpose of this network is to further delay the turn-on, without affecting the turn-off, thereby inserting some additional dead-time. The resistor-diode network is also useful in reducing the peak of the current spike during the reverse recovery time. As explained in Ref. 2, this has an impact on power losses, as well as dv/dt and EMI. Figure 30 shows the waveforms taken from a test circuit laid out as shown in Figure 10. Operation at 500kHz with the IRF830 HEXFET did not present any problem nor cause any noticeable heating of the IR2110.

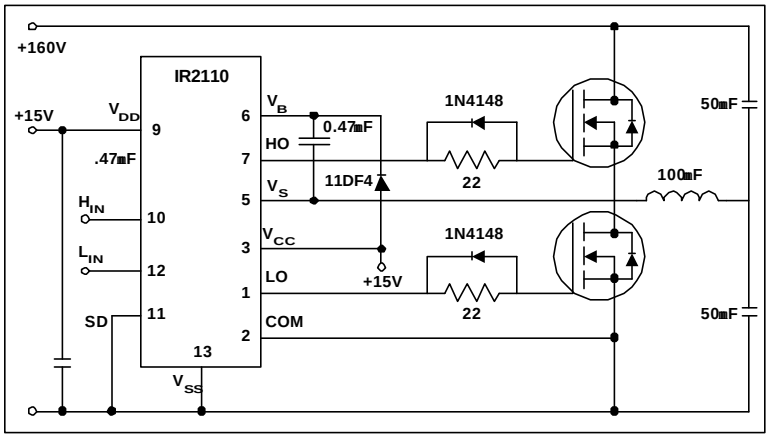


Figure 30a. Test circuit for waveforms shown in Figure 30b. IRF450 operated approximately 100kHz in a 100 mH inductor.

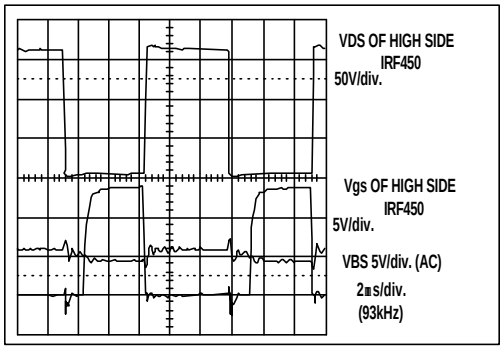


Figure 30b.

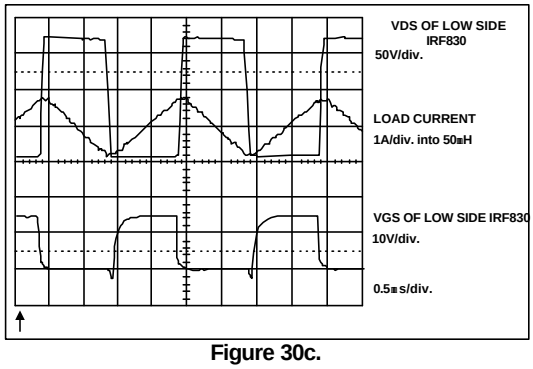


Figure 30c.

13. BRUSHLESS AND INDUCTION MOTOR DRIVES

The implementation of a three-phase bridge for motor drives requires a more careful attention to the layout due to the large di/dt components in the waveforms. In particular, the driver furthest away from the common grounding point will experience the largest voltage differential between COM and the ground reference (Ref. 1).

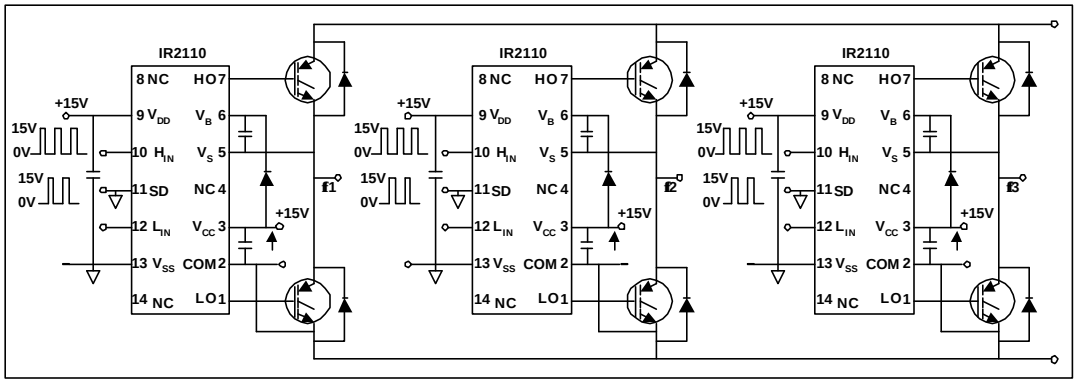


Figure 31. Three-Phase Inverter using three IR2110 devices to drive six IGBTs

In the case of the three-phase drivers, like the IR213x, the guidelines of Sections 5 and 6 should be complemented with the following: Three separate connections should go from the COM pin of the MGD to the three low-side devices. Furthermore, there are several operating conditions that require close scrutiny as potential problem areas.

One such condition could occur when a brushless dc motor is operated with locked rotor for an indefinite period of time with one leg of the bridge being off.
In this condition the bootstrap capacitor could eventually discharge, depending on the voltage seen by V_S during this period of time. As a result the top power device would shut off and would not go on when commanded to do so. In most cases this would not be a cause for malfunction, since the lower device would be commanded on next and the bootstrap capacitor would be charged and ready for next cycle. In general, if the design cannot tolerate this type of operation, it can be avoided in one of four ways:

a. a charge pump could be implemented, as described in Section 8;

b. the control could be arranged to have a very short “normal” duty cycle with a minimum pulse width of a couple of microseconds;

c. if a pole can be inactive for a limited and known period of time, the bootstrap capacitor could be sized to hold up the charge for that time.

d. Isolated supplies could be provided for the high-side, in addition to the bootstrap capacitor.

If the bridge is part of an induction motor drive that use a PWM technique to synthesize a sine wave, each pole goes through prolonged periods of time with zero or very low duty cycle at low frequency. The bootstrap capacitor should be sized to hold enough charge to go through these periods of time without refreshing. In circuits like the one shown in Figure 31, galvanic isolation between the high voltage supply and the logic circuitry is frequently mandated by safety considerations or desirable as a form of damage containment in case of inverter failure.

Optoisolators or pulse transformers are frequently used to perform this function. For drives up to 5 kW, the circuit shown in INT-985 is probably the simplest and most cost-effective way of providing isolation. The use of an MGD shields the optoisolator from the high-voltage dv/dt and reduces their cost while providing a high performance gate drive capability.

14. PUSH-PULL

High-voltage MGDs can still make a very useful contribution in applications that do not capitalize on their key feature, the high voltage level shifting and floating gate drive.

Convenience, noise resilience between V_{SS} and COM and high speed drive capability are appealing features in most power conditioning applications. They can perform the interface and gate drive function with the simple addition of the decoupling capacitors, as shown in Figure 32.

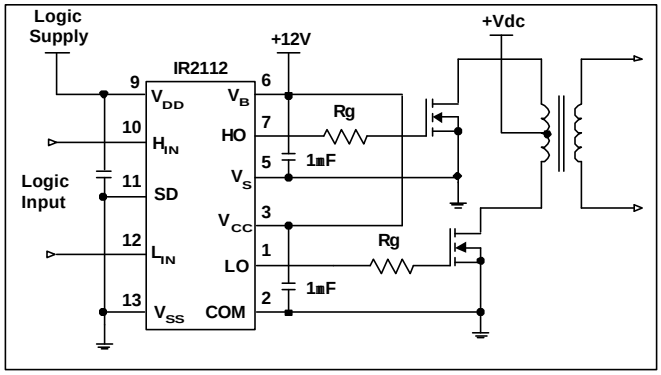


Figure 32. Push Pull Drive Circuit

15. HIGH-SIDE P-CHANNEL

MGDs can also drive a P-Channel device as a high side switch, provided that a negative supply referenced to the positive rail is available, as shown in Figure 33. When operated in this mode, the H_{IN} input becomes active low, i.e. a logic 0 at the input turns on the PChannel MOSFET. Whenever V_S (or V_B) are at fixed potential with respect to ground, the power losses mentioned in Section 4.2.d.2 would be zero.

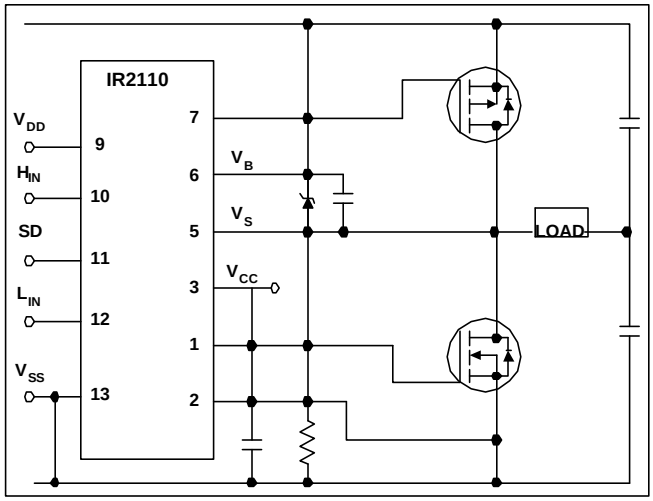


Figure 33. IR2110 driving a high side P-Channel

16. THYRISTOR GATE DRIVE

The circuit shown in Figure 34 can provide isolated gate drive to a thyristor, with status feedback. The 2:1 ratio in the gate drive transformer doubles the current available to the gate from what is delivered by the MGD.

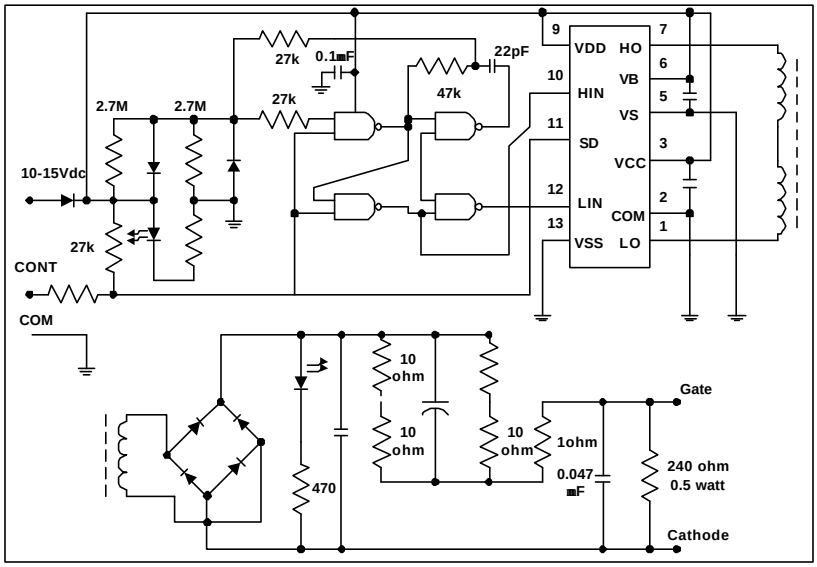


Figure 34. Isolated SCR Gate Drive Circuit

17. TROUBLESHOOTING GUIDELINES

To analyze the waveforms of the floating channel of the IR2110 a differential input oscilloscope is required. It is assumed that any voltage differential not referenced to ground is measured in this way.

It is also assumed that obvious checks have been made, for example:

- Pins are correctly connected and power supplies are decoupled.
- The bootstrap charging diode is ultra-fast, rated for the rail voltage.
- The shutdown pin is disabled.
- Logic inputs do not cause simultaneous conduction of devices, unless the topology requires it.

SYMPTOM	POSSIBLE CAUSE
No gate drive pulses	Verify that Vcc is above the UV lockout value
Gate drive pulses on lower channel only	Measure voltage across bootstrap capacitor; it should be above the lockout level. If it is not, check why capacitor doesn't get charged. Insure that capacitor is charged at turn-on
Erratic operation of top channel	Verify that VS doesn't go below COM by more than 5-10V. Verify that high side channel does not go in UV lockout. Verify that dv/dt on VS with respect to COM does not exceed 50V/ns. If so, switching may need slowing down. Verify that logic inputs are noise-free with respect to VSS Verify that input logic signals are longer than 50ns
Excessive ringing on gate drive signal	Reduce inductance of gate drive loop. Use twisted wires, shorten length. If reduction of loop inductance does not bring ringing to acceptable level, add gate resistors.

TABLE 1

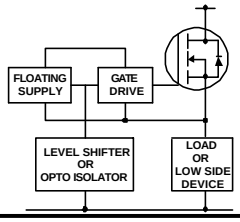
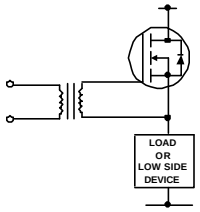
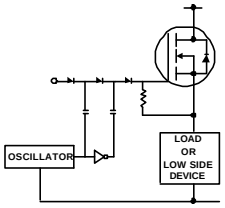
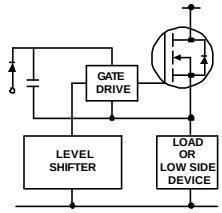
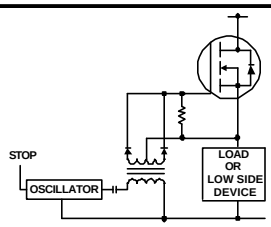
METHOD	BASIC CIRCUIT	KEY FEATURES
FLOATING GATE DRIVE SUPPLY		Full gate control for indefinite periods of time. Cost impact of isolated supply is significant (one required for each high side MOSFET). Level shifting a ground referenced signal can be tricky: Level shifter must sustain full voltage, switch fast with minimal propagation delays and low power consumption. Opto isolators tend to be relatively expensive, limited in bandwidth and noise sensitive.
PULSE TRANSFORMER		Simple and cost effective but limited in many respects. Operation over wide duty cycles requires complex techniques. Transformer size increases significantly as frequency decreases. Significant parasitics create less than ideal operation with fast switching waveforms.
CHARGE PUMP		Can be used to generate an "over-rail" voltage controlled by a level shifter or to "pump" the gate when MOSFET is turned on. In the first case the problems of a level shifter have to be tackled. In the second case turn on times tend to be too long for switching applications. In either case, gate can be kept on for an indefinite period of time. Inefficiencies in the voltage multiplication circuit may require more than two stages of pumping.
BOOTSTRAP		Simple and inexpensive with some of the limitations of the pulse transformer: duty cycle and on-time are both constrained by the need to refresh the bootstrap capacitor. If the capacitor is charged from a high voltage rail, power dissipation can be significant. Requires level shifter, with its associated difficulties.
CARRIER DRIVE		Gives full gate control for an indefinite period of time but is somewhat limited in switching performance. This can be improved with added complexity.

TABLE II			
	Die Size	**Rise Time**	**Fall Time**
Typical switching times for different HEXFET die sizes (Vcc=15V, test circuit as in Figure 9, without gate network)	HEX-2	25ns	17ns
	HEX-3	38ns	23ns
	HEX-4	53ns	34ns
	HEX-5	78ns	54ns
	HEX-6	116ns	74ns

References:

1. "New High Voltage Bridge Driver Simplifies PWM Inverter Design," by D. Grant, B. Pelly. PCIM Conference 1989
2. Application Note AN-967 "PWM Motor Drive with HEXFET III"
3. Application Note AN-961 "Using HEXSense in Current-Mode Control Power Supplies"
4. Application Note AN-959 "An Introduction to the HEXSense"
5. "Dynamic Performance of Current Sensing Power MOSFETs" by D. Grant and R. Pearce, Electronic Letters, Vol. 24 No. 18, Sept 1, 1988

INTERNATIONAL RECTIFIER IOR

POWER MOSFET APPLICATION NOTES

PUBLISHED BY INTERNATIONAL RECTIFIER, 233 KANSAS STREET, EL SEGUNDO, CA 90245, (213) 772-2000

Understanding and Using Power MOSFET Reliability Data

by Steve Clemente and Ken Teasdale

Abstract

It could reasonably be argued that a design is not complete until its long term performance is known. Design engineers will only be able to calculate it, to the extent that they are, in turn, supplied with reliability information on the devices they are using. This information has previously not been generally available for discrete power semiconductors and only recently power MOSFET manufacturers have begun to publish data that defines the reliability of their products.

This section will attempt to explain the mysteries surrounding manufacturers' power MOSFET reliability data, and will show how this data is derived, what it means, and how it can be used. Actual practical examples will be presented which demonstrate how the manufacturers' data can be used to design for in-circuit reliability of power MOSFETs.

Introduction

As quality and reliability (Q&R) are perceived more and more as a key feature of a successful electronic product, the task of the design engineer becomes more complex.

The circuit designer's attitude typically was that his function was to design the simplest and most economical circuit to do the job, with the components available. He assumed that the components he chose would be adequate and the QPL (if he happened to work for a large company) relieved him of any responsibility on the subject. Those who wanted to tackle the problem found that reliability information was basically unavailable and this made the task of calculating the system reliability a frustrating exercise. This is probably the chief reason why the vast majority of engineers have chosen to ignore the problem or relegate it to a well defined group of specialized people whose results he basically mistrusted.

Over the last few years things have been slowly changing. On the one hand, a number of developments have provided a better understanding of failure behavior of components as well as equipment. On the other hand, components manufacturers have realized that the cheapest way to offer products which — in the long term — will be the most cost effective and have the greatest longevity in the marketplace, is to spare no expense to optimize Q & R through rigorous quality control and long term reliability test programs. An important outcome is the publication by the semiconductor manufacturer of user-oriented data that quantifies failure rates under actual application conditions.

Hopefully this paper will induce some engineers to step from a tridimensional world of design constraints and functional specs into a four dimensional one where performance is looked at over a specified time span.

Power MOSFET Reliability

The conceptual steps to generate reliability information on a device are the following:

(a) Establish — or search for — the dominant failure mechanisms. To do this, the reliability engineer draws from a number of sources like established knowledge on that particular manufacturing technology, literature and his own intuition. Experience and intuition will help him to establish the testing priorities by which he will determine the failure mechanisms.

(b) Run accelerated stress tests aimed at activating the specific failure mechanism being tested for. This is a long, expensive and painful process. To be meaningful it must be done for a very large number of device hours, at elevated temperature, with expensive equipment and on an adequate number of part numbers.

(c) Establish, if possible, a "meaningful" mathematical model for the hazard function and determine its parameters. A model is "meaningful" to the extent that it has a physical underpinning. The availability of such a function can be of great help in understanding the nature of the failure mechanism. As we will see, such a good model is seldom available.

(d) Compute and present the reliability estimates for the different failure mechanisms in a form that can be readily used by design or component engineers.

At this point the work of the reliability engineer is only apparently complete: the key task he still has to accomplish is to relate his results back to R & D or Production Engineering, as appropriate, so that the process can be improved in light of his findings.

In general, failure modes fall into two broad categories — those related to defects within the silicon die itself, and those related to the packaging of the die. The failure mechanisms identified to date for HEXFETs within each of these categories, and the tests that are used to activate them, are discussed in the following sections.

Work is continuing to identify other acceleration factors that would apply, for instance, to drain or gate current, drain voltage, power, etc.

Die Defects

These may be one of two kinds: field distortion defects, or oxide defects. Failure mechanisms such as electromigration or microcracking of aluminum conductors, slow trapping, surface charge or polarization, though potential problems with MOSFETs have not been detected in HEXFETs yet.

Field Distortion

The presence of polar molecules, such as water and ionic contaminants from the atmosphere, on top of the passivation surface and along the edge of the die, will distort the electric field when a high voltage is applied to the MOSFET, giving increased local leakage current and possible eventual thermal runaway. Failures occur in the random and wearout region, and can be accelerated by high temperature reverse bias burn-in.

In this test, the device is 'reverse biased' by applying voltage between the drain and source — typically 80% of the rated drain-to-source breakdown voltage — with the gate and source grounded (Figure 1). The tests is run at elevated temperature — typically 150°C — and the test runs for several thousand hours. As of June 1987, a total of 13,487 devices had accumulated over 1.9 billion device hours. Section 1.3 of "Reliability Program and Test Results" (also Ref. 1) relates the test results.

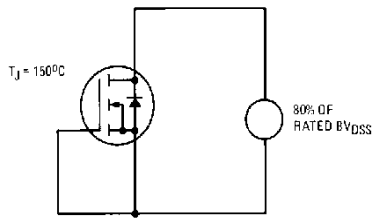


Fig. 1 — High Temperature Reverse Bias Test

For failures in the random region (failure rate substantially constant) the exponential model provides a good approximation:

$$\lambda = Ae^{-\frac{E}{KT}} \quad (1)$$

where λ is the failure rate, E is the activation energy, K is Boltzmann's constant, T is absolute temperature and A is a scaling factor. The activation energy in the above expression is determined by repeating the tests at two different temperatures and solving for E in the expression for the ratio:

$$\frac{\lambda_{T_1}}{\lambda_{T_2}} = \exp\left[-\frac{E}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right] \quad (2)$$

Once E is known, A can be calculated from (1) in correspondence of a known failure rate and known temperature.

To predict the actual failure rate associated with this failure mechanism under a specific set of operating conditions the design engineer would use the expression (1) together with the appropriate parameter. In doing so he would be implicitly disregarding the fact that these figures are statistical in nature and are valid within some "confidence level" that is a function of the amount of data that has been collected. The plot in Figure 2 presents that same information with the appropriate confidence level.

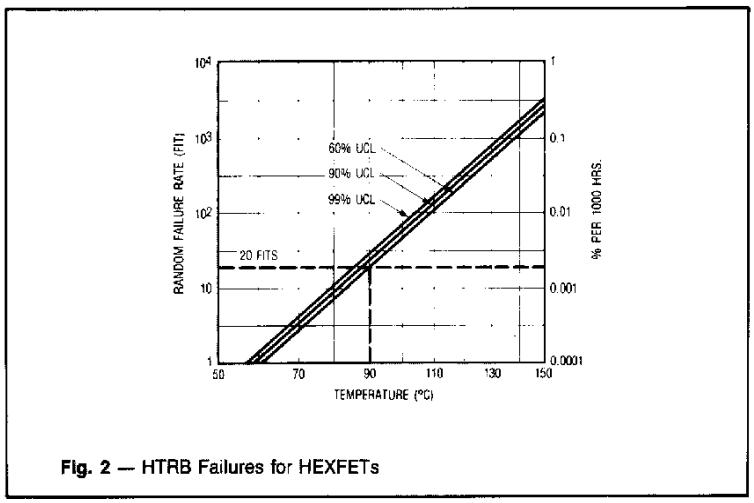


Fig. 2 — HTRB Failures for HEXFETs

It may be worth pointing out that device burn-in will not reduce the failure rate due to field distortion for two reasons:

(1) These failures occur in the random region, which is typical of strong population. No trace was found of a "weak" population that could be weeded out by burn-in.
(2) The failure rates are such that any reasonable burn-in (168 hours) will not have any noticeable effect.

Oxide Defects

Micro-defects in the devices's gate-oxide layer cause random failures, at a very low rate, in the infant and random regions. These defects lead to failures in the form of a gate-to-source short-circuit. They can be activated by high-temperature gate-stress burn-in testing (Figure 3).

In this test, a forward bias voltage is applied between gate and source, while drain and source are connected to ground. The test is run at elevated

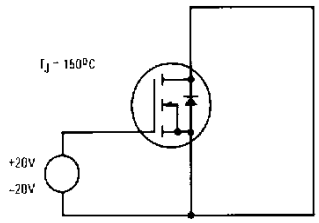


Fig. 3 — Gate Stress Test

temperature. As of June 1987, 3856 devices on long-term gate stress test accumulated over 4.7 million device-hours. Test results are shown in Section 1.3 of "Reliability Program and Test Results" (also Ref. 1).

For the failures, D. L. Crook (Reference 2) proposes an acceleration expression made up of two components:

$$\frac{\lambda_1}{\lambda_2} = \exp\left[-\frac{E_A}{K}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right] \times \exp\left[-\frac{(E_2 - E_1)}{E_c}\right] \quad (3)$$

The first being a thermal acceleration factor according to the Arrhenius model, the second a voltage dependent factor, with $E_2 - E_1$ the electric field differential between the two test conditions and E_C an electric field constant,

equivalent to the activation energy. To determine these constants the test was run at two different temperatures (100 and 205°C) and two different gate voltages (28 and 30V). The electric field constant came out to be 6.5 10^6 V/m which is very close to the value of 6.2 mentioned in Reference 2.

The Expression 3 or Figure 4 can be used interchangeably to predict the actual failure rate as a function of gate voltage. This does disregard the statistical nature of the data and, in doing so, we will be assuming that the results obtained from a given population are 100% applicable to the entire population. Confidence levels for these results will be calculated later on.

The data from the thermal acceleration portion of the experiment are shown in Figure 5 together with their linear regressions. The fact that these two lines intersect indicates that there is not a good basis for the application of the Arrhenius model to the results in their present form. After some searching, it was found that his "aberrant" behavior was due to more than one failure mechanism in the test population. A closer scrutiny of the data presented in Figure 5 showed that the data points could be divided into two groups, those below 8% and those above 10% accumulated fails. Linear regression applied independently to both failures yielded parallel lines thereby confirming the validity of the assumption (Figures 6 and 7). The resulting parameters for the lognormal distribution are shown in Table I.

The significant difference between the two activation energies underscores the distinction between the two failure mechanisms, one for a weaker population and one for a stronger population. This implied that the first failures were caused by both failure mechanisms while the failures over 10% were only due to the lower activation.

Table I

Population	Leg	Temperature T (°C)	σ	μ	Activation Energy Ea (J)
< 8% of Accumulated Failures	3	100	1.7	8.4	.65 10^{-19}
	4	205	1.7	5.7	
> 10% of Accumulated Failures	3	100	4.6	16.3	.19 10^{-19}
	4	205	4.6	15.7	

To purge the first fails from the second failure mechanisms we write the acceleration factor for the two combined:

$$\exp\left[\frac{E_t}{K}\left(\frac{1}{T_2}-\frac{1}{T_1}\right)\right] = \exp\left[\frac{E_1}{K}\left(\frac{1}{T_2}-\frac{1}{T_1}\right)\right] \times \exp\left[\frac{E_2}{K}\left(\frac{1}{T_2}-\frac{1}{T_1}\right)\right]$$

where E_t and E_1 are known (.65 10^{-19} and .19 10^{-10} respectively) while $E_1 = E_t - E_2$ = .46 10^{-19} joules which is in close agreement with the .3eV published in Reference 2. The final result of the above evaluation is presented in Figure 8 in a form that can be directly utilized by design engineers.

Such a clear-cut distinction between the stronger and the weaker component of the population could conceivably make burn-in a most effective tool to weed out the weaker component.

However, a quick glance at Figure 4 will show that a standard gate burn-in test (150°C, V_{GS} = 80% of max. rated) will take 10^{10} second to weed out a tiny 1% of the population, i.e. some 3200 years! This amounts to saying that burn-in, under those conditions, is a waste of time and money and it should be strongly questioned, unless it is mandated by powers that are beyond our control. The linear regression line for 100°C (Figure 7) shows virtually no distortion from the higher activation energy failure mechanism we would like to weed out. If that failure mechanism hardly makes its presence felt at 100°C, which is a fairly high operating temperature for all but the most demanding applications, why bother weeding it out? Whenever, on the other hand, burn-in is mandated, the possibility of using voltages and temperatures above those normally used should be seriously considered. With reasonable values like T_J = 175°C and V_{GS} = 28V the acceleration factor with respect to the 20V line of Figure 4 is 1.34 × 10^6 which means that in 48 hours (1.728 × 10^5 secs) more than 12% of the devices would fail, devices that, as we pointed out before, might not have failed in a practical application.

Packaging Defects

The main problems of the silicon interfaces are the following:

(A) Die attach fatigue that is normally caused by the temperature differential between the die and the header and by the different thermal

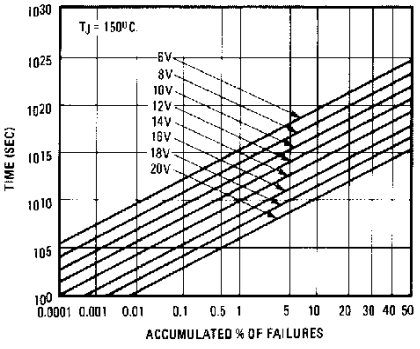


Fig. 4 — Projected Log Normal Accumulated Failures as a Function of Gate Voltage

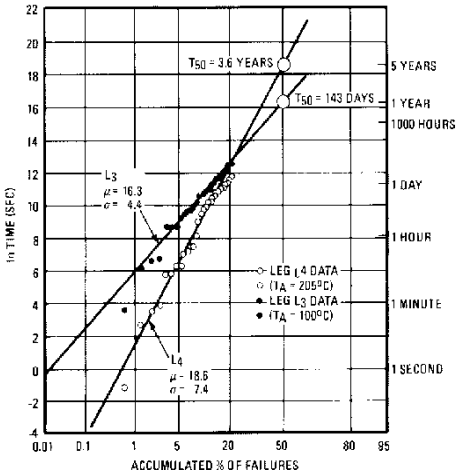


Fig. 5 — Data Points From The Thermal Acceleration Portion of the Gate Stress Test

expansion coefficients of silicon and the header material. This shows up as cracking or separation of the die or voiding the die attach, resulting in degraded on-resistance and/or thermal resistance, and eventual thermal runaway. These failures largely occur in the wearout region. The susceptibility of a given die attach to thermal fatigue is normally ascertained with a power cycling test (Figure 9). In this test, drain current is supplied until the case temperature rises a given amount — typically 70°C. Power is then shut down and cooling fans force the temperature back to ambient. The cycle is repeated until significant degradation starts to occur. Each cycle typically takes about two to six minutes.

(B) Wire bond fatigue. This program is similar to the previous one and shows up as a separated wire bond. It can also be tested by power cycling the parts although simpler but less effective tests are sometimes used (temperature cycling, without any power being applied).

(C) Metal corrosion. When the die is packaged in a non-hermetic package it is subject to a deterioration process that will be described later. The standard test to accelerate this failure mode it 85/85; 85°C and 85% relative humidity. We found this test to give only a superficial indication of meaningful operating conditions in so far as it disregards the applied bias that is normally present in a circuit. The test circuit we have used (Figure 10) includes a bias voltage as an accelerating factor.

Power Cycling Tests

Since the results of these tests are comprehensive of the two failure modes A and B, the search for a model would not be appropriate.

Test results to this date (June, 1987) established two key points:
- The dependency of the power cycling capability on die size, package and bonding wire size;
- the adequacy of the Arrhenius model to provide acceleration factors that are consistent with the test result.

Further evaluation is required to fully qualify all dice and all packages. Tests at different power levels would also be required to obtain a larger number of die attach failures. This involves a substantial amount of work that is being carried out now.

In light of the above, the cumulative failure shown in Figures 11 and 12 should be taken as in indication of device capability more than actual design parameters. The activation energies appear to be 0.59 10^{-19} joules

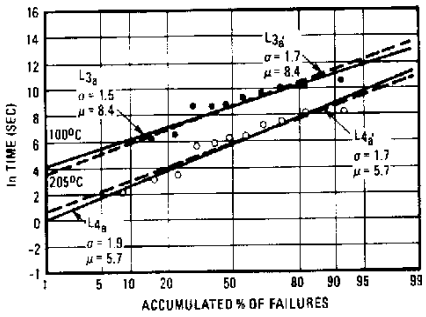


Fig. 6 — Regression Lines for the Weaker Population (Gate Stress)

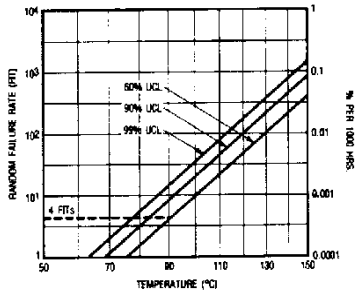


Fig. 8 — Time to Accumulated 1% Gate Failures Versus Temperature and Gate Voltage

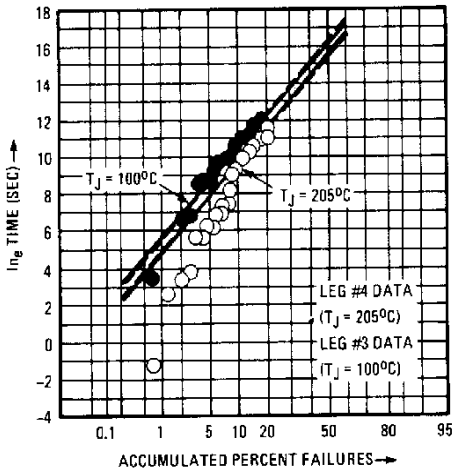


Fig. 7 — Regression Analysis for the Stronger Population

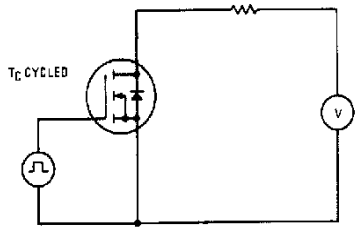


Fig. 9 — Power Cycling Test Circuit

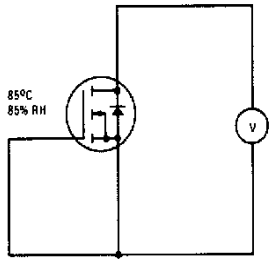


Fig. 10 — 85/85 With Bias

for the IRF330 and 0.464 10^{-19} for the IRF350. Here too, device/equipment burn-in will not improve the reliability of the devices because this type of failure is characteristic of the wearout region.

Metal Corrosion with Bias Acceleration

Under the environmental stress conditions of humidity/temperature/bias, it is expected that one of two failure modes will normally predominate: 1) excess leakage currents under reverse bias will increase to the point of causing a parametric failure of I_{DSS} or, 2) corrosion of the internal metallization will result in a parametric shift in the on-resistance. $R_{DS(on)}$, eventually resulting in an open circuit condition. The cause of both of these phenomena is the ingression of water into the plastic package from the ambient atmosphere to the chip surface, forming external surface leakage paths. This can lead to excessive drain current and eventually parametric failure.

The application of reverse bias under blocking conditions ($V_G = V_S$) can result in cathodic corrosion of the source bond pad. As the corrosion proceeds, the aluminum source pad slowly dissolves causing intermittent continuity between the source wire and the top metallization of the chip. Eventually, the continuity goes altogether and the device presents an open circuit. The cathodic corrosion process is electrochemical in nature and is governed by the following equations (a and b) as described by van de Ven and Koelmans (Reference 3):

(a) $e^- + H_2O \rightarrow OH^- + \frac{1}{2} H_2$

(b) $OH^- + Al + H_2O \rightarrow AlO_2^- + 3/2\ H_2 \rightarrow$

Electronic current, externally leaking from the source metallization to the drain, reacts with water according to the first equation, liberating hydrogen gas and creating hydroxyl radicals in the immediate neighborhood of the aluminum source pad. The hydroxyl radicals then reacts with the aluminum, in the presence of water, to form a soluble oxide of aluminum as in the second equation. The rate at which this process proceeds under 85°C/85% RH conditions is regulated by the amount of surface leakage current and by availability of water. The water must not only be present on the aluminum bond pad, but also on the sides of the chip, forming a conductive leakage path.

Once water is present on the chip, the electronic current available to take part in the corrosion will depend on the amount of applied bias. To evaluate this dependance various applied drain potentials were used on several groups of HEXFETs as described previously.

From the test result the acceleration factor due to the applied bias is shown in Figure 13. The resulting set of lines allow the projection of cumulative failures in time for any particular applied bias on a HEX-3 device in a TO-220 package in 85°C/85% RH conditions. The reader might notice that under these conditions, if the applied bias is substantial, plastic devices would not last too long. It might be argued, though, that the 85/85 conditions are unduly severe and do not reflect a realistic operating condition.

The results obtained to this date (June 1987) seem to confirm the accelertion factor reported in Reference 4:

$$AF = \left(\frac{RH_2}{RH_1}\right)^n \exp\left[\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

With:

RH = relative humidity (1 is lower, 2 is higher)

T = absolute temperature (1 is lower, 2 is higher)

E_a = experimental thermal activation energy

k = Boltzman constant

n = experimental humidity power parameter

E_a is in the order of 0.8eV and n is estimated to be 2.7

Here too, it may be worth pointing out that device or equipment burn-in would not accomplish anything since the failure mechanism is associated to device wearout.

Using the Failure Data To Calculate Circuit Reliability

In those applications where the devices would be subjected to a dominant stress that happens to be one of those we tested for, the reliability information supplied in our Reliability Report could provide a fairly straight forward answer. Two examples are shown in the next section. If, on the other hand, there is no dominant stress calculations have to take in account all factors as shown in the section entitled

"The Effects of Combined Stresses."

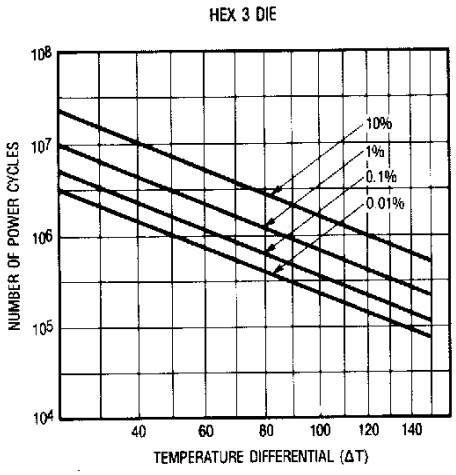


Fig. 11 — Temperature vs. Number of Power Cycles to Achieve 0.01%, 0.1%, 1% and 10% Cumulative Failures

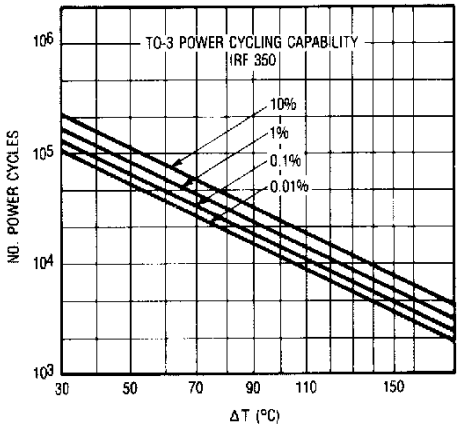


Fig. 12 — Temperature vs. Number of Power Cycles to Achieve 0.01%, 0.1%, 1% and 10% Cumulative Failures

Dominant Stress

The following examples illustrate how the failure-rate data can be used by the designer to calculate incircuit reliability.

Example 1 — 250W Switching Power Supply

A high-rel power supply is to be designed that will provide a continuous output of 250W to a dedicated load, 24 hours per day. A HEXFET and heatsink are to be selected that will keep HEXFET-related power supply failure rate to just 0.1% over a 5 year period. The maximum applied gate voltage is 12V, (meaning that gate failure rates are so low that they can be ignored). The principal failure mechanism will be governed by temperature and failure rates are quantified in Ref. 1. Maximum ambient temperature is 45°C.

Number of operating hours in 5 years = 43,800

Number of device operating hours per 1000 power supplies in 5 years (.1% of device failure permitted) = 8.76×10^7

Permitted failures per 10^9 hours = 11.4 FITs

From the HEXFET's FIT's curve:
Max. permitted T_J (Ref. 1) 84°C

Assuming a half bridge circuit operating from 220V minus 15% (low line) and an efficiency of only 80%, the rectifier current is 1.2A and a peak current in each device is 2.7A at a duty cycle of 45%. With these assumption, the following two alternatives are possible.

(a) The IRF430. The junction to sink thermal resistance is 1.8 deg. C/W and the maximum $R_{DS}(on)$ is 2.4 ohms at T_J = 84°C. Figure 14(a)

(b) The IRF440, which is a larger HEXFET die in the same TO-3 package. This has a maximum $R_{DS}(on)$ of 1.36 ohms at T_J = 84°C, and a junction to sink thermal resistance of 1.1 deg. C/W. Figure 14(b)

(a) IRF430

Conduction losses = $2.7^2 \times 2.4 \times 0.45$
= 7.8W
Temperature rise, junction-to-ambient = 84 − 45
= 39°C
Thermal resistance, junction-to-ambient = 39/7.8
= 5°C/W
Thermal resistance, sink-ambient = 5 − 1.8
= 3.2°C/W

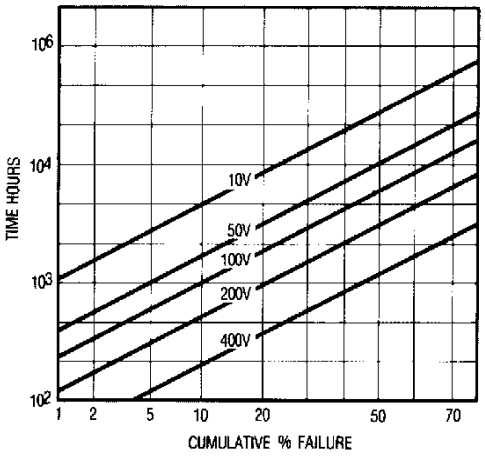


Fig. 13 — Voltage Acceleration Factor in 85/85 Environment

(b) IRF440

Conduction losses = 2.7 × 1.36
= 4.46W
Thermal resistance, junction-ambient = 39/4.46
= 8.7°C/W
Thermal resistance, sink-ambient = 8.7 − 1.1
= 7.6°C/W

Example 2: Failure rates in relation to gate voltage

One of the major features of power HEXFETs is that they can handle very high peaks of current. The fundamental design limitations on the peak current handling capability are junction heating and maximum gate voltage.

The HEXFET is a "linear" device, and greater the peak current, the greater the gate drive voltage needed to ensure that the device is "fully enhanced." Figure 4 shows that increasing gate voltage produces increasing failure rates, particularly at gate voltage about 16V or so. Therefore, operation at very high peak current, while being operationally practical, will have an effect on long-term reliability, in as much as high peak drain current of necessity requires relatively high peak gate voltage.

The effect will be most significant for devices with relatively low drain-source voltage rating. This is because low voltage devices have low on-resistance with correspondingly high peak current handling capability, and need more gate drive voltage to achieve their high peak current ratings. To take an example (Figure 15) an IRF330, rated 400V, is fully enhanced at rated peak current of 22A with just 12V gate voltage. The IRF130, rated 100V, needs virtually 20V gate voltage for full enhancement at its rated peak current of 56A.

To see how operation with high peak currents impacts the reliability let's take, as an example, a buck converter operating from a 48V bus with a nominal output current of 7A. Reliability requirements are the same as those seen in the previous example and the following conditions also apply.

Device mounted on heatsink with total $R_{th}J\text{-}A$ = 4°C/W

Maximum ambient temperature = 45°C

Maximum average power dissipation = $7^2 \times .18 \times 1.75$
= 15.4W

Maximum junction temperature = 15.4 × 4 + 45 = 106.7°C

Notice that since the buck converter has only one device, twice as many FITs are permitted in this application as opposed to the previous one and the operating conditions indicated above satisfy the reliability requirements (Figure 1.1.1 of Ref. 1). Because of delays in the current sensing loop, the minimum duty cycle under short circuit conditions is 4% with a peak current of 40A. Under these conditions, maximum junction temperature is not to exceed 150°C. It follows that:

Max. power that can be dissipated ($\Delta T/R_{th}$) = (150 − 45)/4
= 26.25W

Max. allowable $R_{DS}(on)$ @ 150°C = $P/(I^2pk * D.C.)$
= $26.25/ (40^2 \times .04)$
= .41 ohm

Max. allowable $R_{DS(on)}$
@ 25°C = .23 ohm

Figure 16 shows the relationship between drain current, on-resistance, and gate voltage at T_J = 25°C. Table II shows the maximum achievable peak drain current for a given gate voltage with the specified limitation of .23 ohm. It appears that, with some margin, a gate voltage of 18V will satisfy the peak current requirements and the gate drive circuit has to be designed to provide that voltage on a continuous basis. For these conditions (107°C and V_{GS} = 18V) we find, (Ref. 1) that it takes a few days to accumulate a .1% of failures so that the reliability criteria are definitely not met and a bigger device has to be considered. Going through the same procedure for an IRF142, we find that the peak current requirements are satisfied with a gate voltage of less than 12V, so that all conditions would be met.

The Effects of Combined Stresses

In an ideal design there should not be a dominant stress, nor should there be a dominant failure mechanism in a given device. The consequences of such a statement are far reaching: It implies that the device manufacturer should be well versed with the applications for his devices and keeps them in mind when he designs them. It also implies that the design engineer is intimately familiar with the device and chooses its operation point to get the most out of it.

Of course this is far from being a real condition and the previous examples are more typical of what occurs in practice. For the sake of completeness, though, we shall touch briefly on the effects of combined stresses.

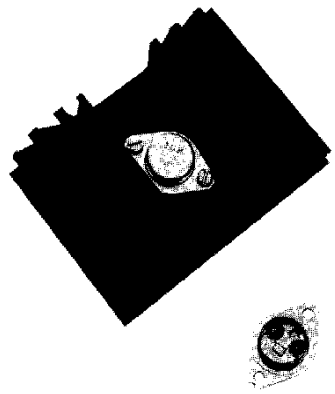


Figure 14(a): IRF430 on a "large heatsink

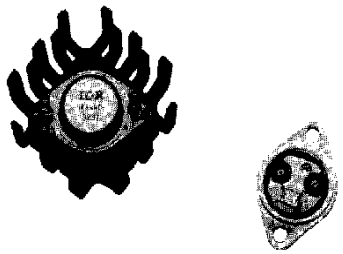


Figure 14(b): IRF440 on a "small" heatsink

Figure 14: Reliability trade-offs. These HEXFET/heatsink combinations are for a high-rel 250W switching power supply with a calculated HEXFET related failure rate of just 0.1% over 5 years continuous operation. The same reliability can be achieved with the "small" HEXFET and "large" heatsink in (a) or with the "large" HEXFET and "small" heatsink in (b).

A group of devices operating at 125°C with 16V on the gate will experience a constant failure rate of approximately .5 10^{-6} device failures/our due to field distortion and it will accumulate 1% of failure in approximately 5 10^9 secs due to gate stress (10 failures in 5 10^9 seconds, i.e. 7.2 10^{-9} devices/hour). On a 1000 unit sample, over a five year period, (42,720 hours) there will be:

21.36 failures due to field distortion
.31 failures due to gate stress

By raising the gate voltage to 17V the gate stress failure would go to 2.4 10^{-7} device failures per hour and the corresponding gate failures for that stress would be 10.25, which is comparable to the number of field distortion failures.

These failures are summable to the extent that their number is small compared to the total population otherwide they should be corrected to take into consideration the fact that the population decreases as failures occur and that, once a device has failed, it cannot fail again.

Table II

V_{GS} V	Peak Current (A)
20	55
18	45.5
16	35.5
14	28.5
12	24.0
10	20.5

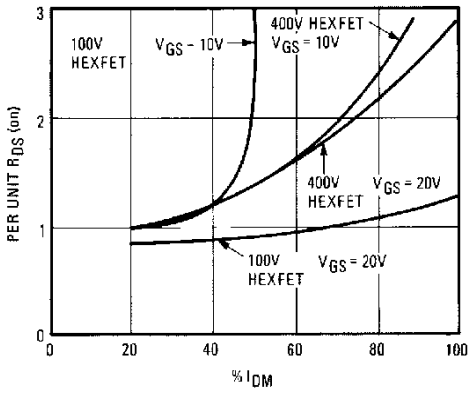


Figure 15: Variation of On-Resistance with Drain Current in Devices of the Same Die Size but Different Voltage Ratings

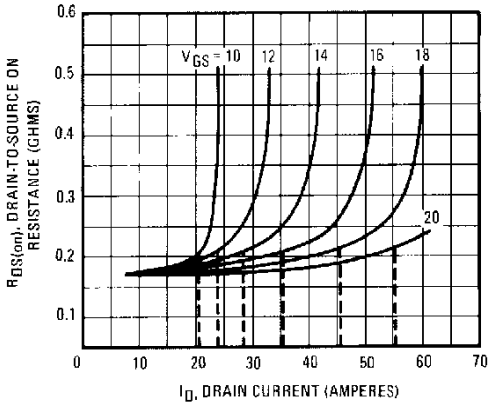


Figure 16: On-resistance vs. Drain Current and Gate Voltage

Cost Considerations

It may be appropriate, at this point to clarify the terminology a bit by defining quality and reliability:

— Quality is a measure of the relative amount of defective parts at the time of shipment. Statistical sampling techniques are normally employed to measure quality directly (AOQL = actual outgoing quality level, or PPM) or indirectly (AQL = acceptance quality level).
— Reliability measures the capability of a device to perform as specified over a period of time, as we have seen in the previous section.

The tools available to **components manufacturers** to achieve the objective of a higher quality and more reliable device are basically the following:

— incoming material, process and assembly monitoring
— lot certification
— outgoing quality control
— long term reliability programs

Equipment manufacturers, on other hand, have been following one or more of the following procedures:

— incoming inspection
— device and/or equipment burn-in
— device/vendor qualification
— design auditing to established procedures

It is easily realized that the items listed above make up a very expensive shopping list and, as every engineer knows, the concern for quality and reliability has to be tempered by the economical considerations dictated by the competitive environment the product will face.

Unfortunately substantial costs are also incurred in renouncing Q & R.

Components of poor quality will require board reworking or scrapping. Poor reliability will increase warranty repairs, down time, and customer dissatisfaction.

The only rational way of solving this dilemma is to look at Q & R as a capital investment and determine its payback. In order to do this its costs have to be quantified.

If we subscribe to the traditional notion that to improve Q & R action should be intensified on the items listed above we would find that beyond a certain level the costs become very high and do not provide commensurate results. Interestingly enough, of the two most expensive procedures, incoming inspection becomes detrimental once the AOQL goes below .04% because of the additional handling of the parts, while device burn-in, as shown in the previous section, serves no purpose if good long term reliability information is available. In other words, a component manufacturer that can supply parts to a very low AOQL and has appropriately researched their long term reliability will be able to save the customer a significant amount of money in incoming inspection (Ship to Stock), board reworking, scrap, and burn-in.

Vendor qualification and design auditing procedures would still be left in place, but with a different emphasis.

Since the equipment manufacturer is now relying on data supplied by the vendor it should periodically check on how they are generated and that the lot qualification procedures are adhered to. Furthermore he must provide accurate and timely feedback on in-plant and field failures to correct any potential problem before it develops. He may also want to consult with Application Engineeering in setting up proper design auditing procedures. It will be appreciated that the costs associated with vendor qualification and auditing procedures are negligible compared to a high quality incoming inspection and device or equipment burn-ins.

Conclusion

User-oriented failure rate data for MOSFETs is a new design tool available to the user. They enable MOSFET reliability performance to be calculated and optimized at the design stage. The data presented show that HEXFETs, applied within their ratings, exhibit extremely low failure rates. This, coupled with a very low AOQL figure substantially reduces the cost of building quality and reliability into a product.

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3. van de Ven, E. P. G. T., Koelmans, H., "The Cathodic Corrosion of Aluminum," *J. Electrochem, Soc.,* Vol. 123, no. 1, pp 143-144, 1976.
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Printed in U.S.A. 987-M10

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APPLICATION NOTES

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AN-972B

Thermal and Mechanical Considerations For FullPak Applications

(HEXFET is a trademark of International Rectifier)

by Peter Wood, Donald A. Dapkus II

Plastic Packages

Plastic molded semiconductors have been available for decades and have become the preferred packages for all commercial and industrial equipment. The most popular power package by far is the TO-220AB, but recently, as higher power requirements have emerged, the TO-247AC has gained popularity.

While both of these packages have excellent thermal characteristics, they are non-isolated and in most instances need to be isolated from the grounded framework of the equipment that uses them.

Three methods for providing electrical isolation are frequently used:

1. Isolated heatsink inside the grounded enclosure,

2. Insulating mica or plastic film mounting to grounded heatsink, or

3. Elastomeric thermally conductive insulation material such as Sil-Pad® manufactured by The Bergquist Company.

All methods raise the system cost and additionally cause EMI/RFI problems due to the capacitance to ground of the isolation scheme.

Whenever an additional component such as a mounting insulator is used, there is a consequent reduction in system reliability, especially if there is a high voltage across the insulator.

A need for self isolated TO-220 and TO-247 packages is clearly indicated. The requirements for such packages are listed below:

1. Same physical outline as the TO-247 or TO-220.

2. Same pin spacing and pinout as the TO-247 or TO-220.

3. Same mounting hole dimensions as the TO-247 or TO-220.

4. Similar thermal characteristics to non-isolated version with insulating hardware.

5. Minimum capacitance to mounting surface.

6. Adequate creepage distance pin-to-heatsink to meet current safety codes (UL, CSA, VDE, etc.).

7. Maximum corona-free isolation voltage.

International Rectifier FullPaks

Careful consideration of the aforementioned requirements for both the TO-220 and TO-247 fully isolated plastic packages led to the International Rectifier FullPak case styles manufactured to the outline diagrams shown in Figures 1 through 4.

International Rectifier FullPak HEXFET power MOSFET devices are identified by the letter "I" which is added to the standard part number immediately following the "IRF" portion of the part number. For example, the standard TO-220 device, IRFZ44, becomes IRFIZ44G in the FullPak package; the standard TO-247 device, IRFP054, becomes IRFIP054. As shown above, the TO-220 FullPak part numbers end in the letter "G". This is a manufacturing code; it designates that the device was packaged at IR Great Britain. Figures 5 and 6 describe the various marking on both FullPak devices.

Thermal Characteristics

As with non-isolated devices, thermal resistance from the semiconductor die to the surface of the package is inversely proportional to the area of the die and directly proportional to the sum of the components of thermal resistance within the package. The picture is further complicated by the amount of heat spreading that takes place within the header on which the die is mounted.

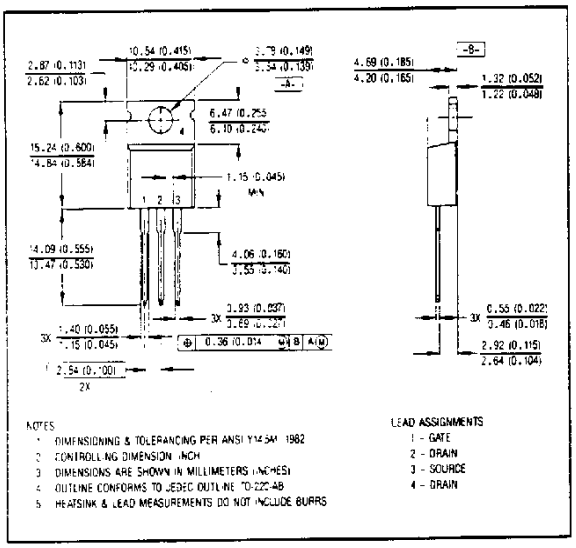


Figure 1. Standard TO-220AB plastic package

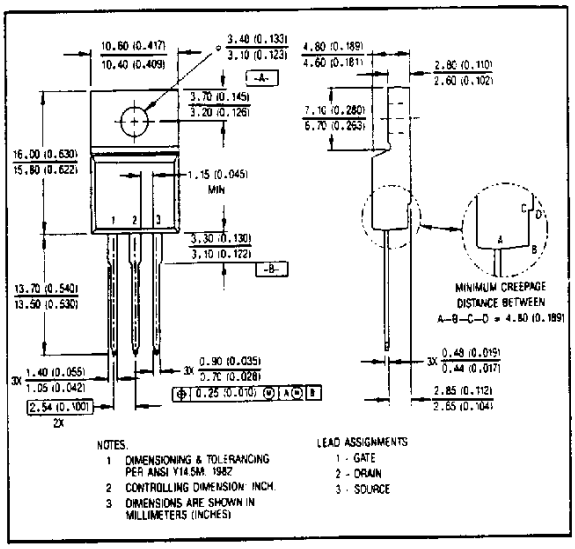


Figure 2. The fully isolated FullPak plastic case style of the TO-220

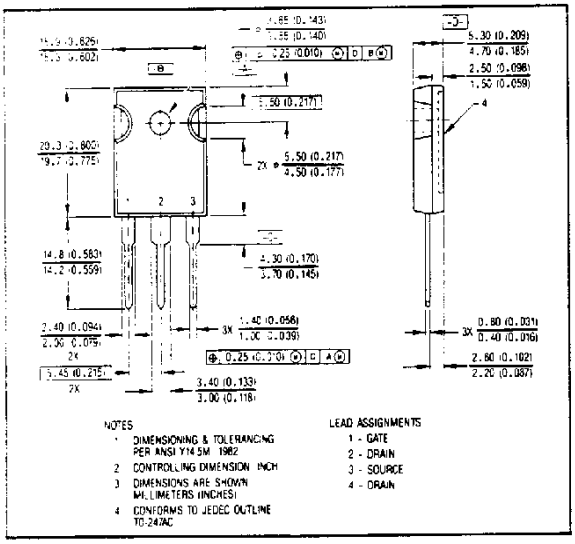


Figure 3. Standard TO-247AC plastic package

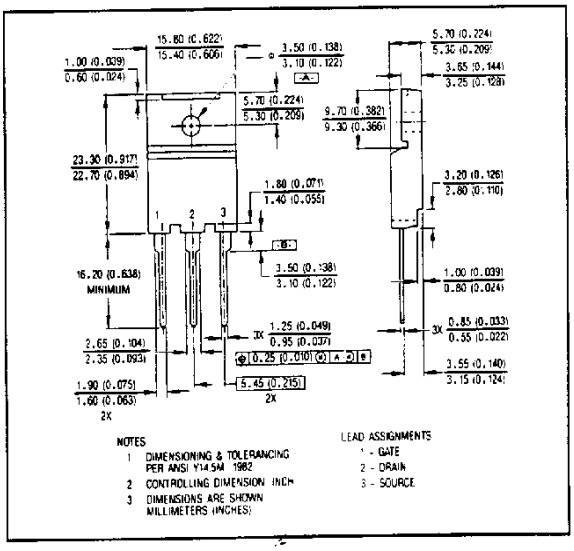


Figure 4. The fully isolated FullPak plastic case style of the TO-247

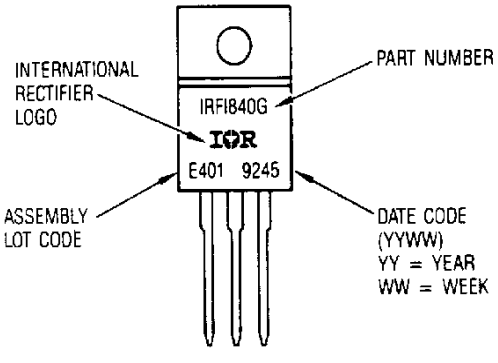


Figure 5. TO-220 FullPak package marking

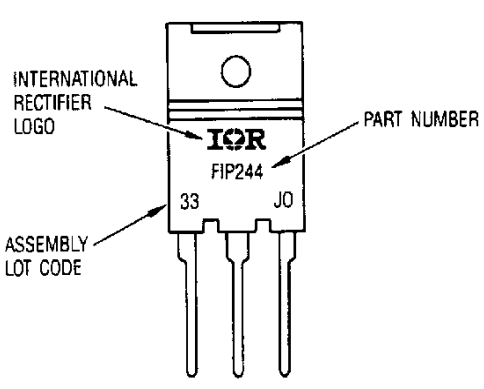


Figure 6. TO-247 FullPak package marking

Thus, a thin header will cause only minimal heat spreading and, therefore, the effective area of thermal injection to the heatsink will be limited to approximately the actual die area. With a thicker header, the effective injection area becomes significantly larger than the die area even though the actual thermal resistance per unit area of the header is larger due to the increased thickness.

Within the package, junction temperature becomes a function of power and thermal resistance:

$$T_J \propto P_D \cdot R_{\theta JC}$$

For a thermally efficient package it is therefore necessary to design with the following objectives to minimize $R_{\theta JC}$:

1. Maximum copper header thickness.
2. Maximum copper header area.
3. Minimum insulation thickness consistent with isolation voltage and capacitance requirements.
4. Maximum thermal conductivity of package material.
5. Surface flatness for best heat transfer to heatsink.

Table 1 lists thermal resistances junction-to-sink ($R_{\theta JS}$) for both the TO-220 and TO-247 standard devices mounted with Sil-Pad K-6® which is a Kapton-based thermally conductive insulator pad manufactured by The Berquist Company. The TO-220 also requires an insulating shoulder washer as the screw hole is not isolated as is the TO-247. Table 1 also lists the thermal resistances for both International Rectifier FullPaks (TO-220 and TO-247) when mounted using thermal grease.

The mounting method requires mentioning. In order to obtain more uniformly distributed and consistent mounting pressure, we use a metal bar across the plastic body instead of using a screw. Five pounds-force • inch of torque is applied to both ends of the bar. Thermal resistance measurements using this mounting method are more consistent than mounting using the intended screw hole.

The typical impact on junction temperature rise of the higher thermal resistance values of International Rectifier FullPak packages is summarized in Table 2. This table shows typical design values of full load power dissipation in the various HEXFET® power MOSFET sizes, and the corresponding *additional* temperature rise of the junction in the FullPak fully isolated case style, versus standard packages with Sil-Pad® insulating material.

Table 1. Average values of samples measured

MOUNTED WITH BAR ACROSS BODY 5LBF • IN. TORQUE				DIE SIZE
TO-220 + Sil-Pad	TO-220 FullPak	TO-247 + Sil-Pad	TO-247 FullPak	
3.7°C/W	4.2°C/W	—	—	HEX-1
3.1	3.6	—	—	HEX-2
2.5	2.8	—	—	HEX-3
2.1	2.7	1.4	1.7	HEX-4
—	—	0.9	1.3	HEX-5

Table 2. Typical additional junction temperature rise in FullPak case style vs non-isolated package

HEXFET Die Size	FullPak Package	Typical Full-Load Power	Approx Additional Junction Temp Rise in FullPak
HEX-1	TO-220	2W	1.0°C
HEX-2	TO-220	5	2.5
HEX-3	TO-220	8	2.4
HEX-4	TO-220	12	7.2
HEX-4	TO-247	15	4.5
HEX-5	TO-247	22	8.8

Note: This table compares the FullPak with the non-isolated package with external Sil-Pad® insulation, and same external heatsink. Note that the additional junction temperature rise in the FullPak is generally not too significant.

As the size of the heatsink decreases, the junction's operating temperature increases due to the increase in $R_{\theta SA}$. As a result, the *percentage* increase of the junction temperature decreases when comparing the FullPak to a Sil-Pad® -insulated standard TO-220. In other words, smaller heatsinks with larger $R_{\theta SA}$'s tend to mask the additional temperature rise caused by the FullPak. In designs with these conditions, there is usually less than 5% degradation in current capability due to the FullPak.

Electrical Performance

Two of the most important properties of the FullPak are its ability to provide electrical isolation while still maintaining adequate thermal conductivity.

Unfortunately these two requirements are in direct conflict with each other since the thicker insulation required for high voltage isolation and lower capacitance also has greater thermal resistance.

As a compromise the isolation voltage is specified at 2.5 kV RMS for the TO-220 and 2.0 kV RMS for the TO-247 FullPaks. As stated earlier the thermal resistances of the FullPaks are somewhat comparable to the non-isolated cases mounted with insulating films. Figure 7 details the test configuration for Hipot testing of the FullPak.

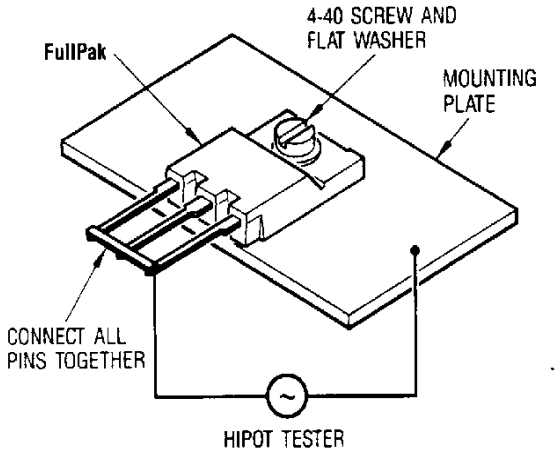


Figure 7. FullPak mounting set-up for Hipot tester

Capacitance

A standard TO-220 mounted to a heatsink with a mica insulator of 0.002'' (0.05mm) thickness has a capacitance (tab to heatsink) of approximately 40 pF. A TO-247 mounted the same way is approximately 60 pF. Similar values were measured using Sil-Pad K-6® as the insulator.

Comparable values for the FullPaks are 12 pF and 26 pF typical for the two outlines.

In practical terms the reduced capacitance of FullPaks versus standard types means that capacitively-coupled switching currents are greatly reduced and hence the EMI/RFI problems associated with standards such as VDE, UL, CSA, etc., are minimized.

Creepage Distance

International Rectifier FullPak devices are designed to present sufficient creepage distance from pin-to-mounting surface to meet the requirements of the various safety standards. The lower half of Table 3 shows actual voltage capability pin-to-mounting surface based on the UL formula of 0.5mm per 100V +0.58mm.

Mounting and Mechanical Considerations

International Rectifier FullPak devices are intended to be mounted by screws as shown in Figure 8, spring clips or even POP® brand blind rivets (Figure 9). Because of their unique construction, non-insulated hardware can be used with the certainty that when mounted, FullPaks can withstand at least 2.0kV RMS impressed from device to heatsink. Recommended mounting torques are shown in Figure 8.

In many low cost applications HEXFET FullPaks can be attached to sheet metal by means of blind rivets. Some words of caution should be heeded. Most ordinary blind rivets are aluminum *with a steel break stem mandrel. These should not be used* as they exert too much force on the FullPak body.

Aluminum soft-set rivets with aluminum break stem mandrels are ideally suited to this application and provide about 100 lb force between the FullPak and the sheet metal heatsink.

The mounting hole in both the TO-220 and TO-247 FullPak is the same size (0.130 inches) which is just right for a 1/8-inch blind rivet inserted from the device side only. The hole in the heatsink should be 0.129 to 0.133 inch (#30 drill).

When attaching an International Rectifier TO-220 or TO-247 FullPak to a heatsink with a blind rivet it is important that the configuration shown in Figure 9 be used, otherwise, if the blind rivet is expanded into the FullPak hole, i.e., inserted from the back of the heatsink, the FullPak will be damaged or the HEXFET die cracked.

Conclusion

The FullPak power MOSFET devices described in this application note are a superior package to any other isolated devices on the market today. The combination of International Rectifier HEXFET reliability and FullPak packaging technology make these power MOSFET devices the quality choice for virtually any

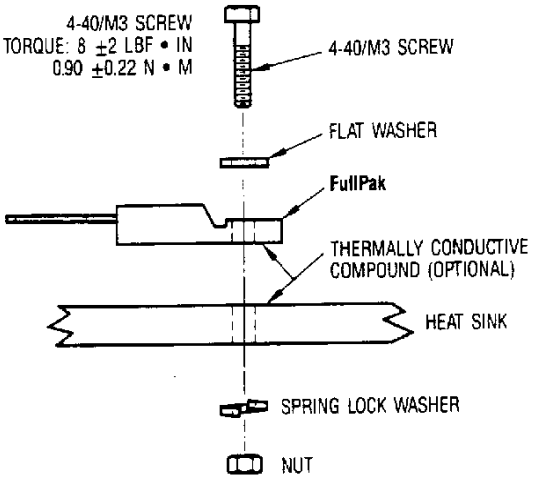


Figure 8. Screw mounting of FullPak

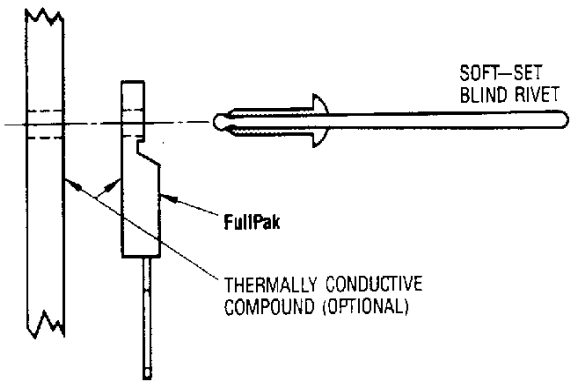


Figure 9. Blind rivet mounting of FullPak

industrial or commercial application. This is especially true when the equipment requirements of industrial safety specifications such as VDE, UL, CSA, etc., have to be met.

The electrical performance of International Rectifier FullPaks mirrors exactly the specifications of the familiar non-isolated TO-220 and TO-247 devices. Only the mechanical and thermal capabilities are different. Thus, it is easy to retrofit existing equipment circuits with the fully isolated FullPak devices since the type numbers correlate to the non-isolated HEXFET device. For example, the IRFP450 becomes the IRFIP450 FullPak, and the IRF830 becomes the IRFI830G, etc.

For complete performance characteristics and specifications consult the FullPak data sheets which are available from International Rectifier. □

Table 3. Creepage comparisons for TO-220 and TO-247 FullPaks

TO-220 FullPak	TO-247 FullPak
Minimum Creepage Pin-to-HS = 4.8mm	Minimum Creepage Pin-to-HS = 3.15 + 2.8 = 6.0mm
Calculations using the UL formula of 0.58mm + 0.5mm/100V per UL 1012 Table 26.5 yield actual minimum voltage ratings as follows:	
Pin-to-HS = 4.8mm Voltage Rating $= \frac{(4.8-0.58) \times 100}{0.5}$ = 844V Pin-to-HS	Pin-to-HS = 6.0mm Voltage Rating $= \frac{(6.0-0.58) \times 100}{0.5}$ = 1084V Pin-to-HS

Table 4. Recommended POP® brand blind rivet part numbers for FullPak applications

Heatsink Thickness	TO-220 FullPak	TO-247 FullPak
1/32 to 1/16	PAD43ABS	PAD43ABS
1/8	PAD44ABS	PAD46ABS
3/16	PAD46ABS	PAD46ABS
1/4	PAD46ABS	PAD48ABS

Note: The above rivets are available from

POP Fasteners Division
Emhart Fastening Systems Group
510 River Road
Shelton, Connecticut 06484

Phone: (203) 924-9341
FAX: (203) 924-8741

See Emhart catalog # P265 (2/92) for additional POP® rivet applications information.

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Using HEXFET III in PWM Inverters for Motor Drives and UPS Systems

(HEXFET is a registered trademark of International Rectifier)

by D. Grant

Introduction

The advantages of MOSFETs for high frequency pulse-width modulated (PWM) inverters and choppers for variable speed motor drives, uninterruptible power supplies (UPS) and similar applications, covering power outputs to tens of kilowatts, include the ability to operate at frequencies above the audible range, low output distortion, high overload capability, fast response, and simple drive circuitry.

It has only been recently, however, that MOSFETs are becoming generally popular in these applications. MOSFETs were not previously always the automatic device of choice, because they had to supplant bipolar transistors which were already well entrenched. Often there was not sufficient incentive to change to MOSFETs, which were still descending the price learning curve. Also the MOSFET's internal body-diode, while superficially offering itself as a needed circuit component, in reality caused circuit difficulties, which often could be solved only by using additional discrete diodes, adding circuit complexity and cost.

In cases where designers did manage to use the MOSFET's internal body diode, they had to establish the allowable limits of operation by painful experience, without any firm guarantee from the manufacturer that the devices were being operated within their capabilities.

The introduction of International Rectifiers HEXFET III generation power MOSFETs eliminates the previous barriers to the use of MOSFETs in PWM motor drives and similar applications. HEXFET America's high volume in-line manufacturing facility now makes HEXFETs decidedly cost-competitive. And HEXFET III incorporates several major design improvements. Its body diode is far more rugged than that of previous power MOSFETs, and can be used without fear of failure.

This means that a three-phase bridge inverter can be constructed using just six HEXFETs, without the need for external diodes or snubbers. The HEXFET III diode rating allows the designer to exploit the presence of the integral diode with confidence, thereby greatly simplifying the design and minimizing overall system cost.

The PWM Inverter

The technique of pulse-width modulation, by which an inverter operating from a fixed-voltage dc supply can generate an ac output voltage of variable frequency and voltage, is well known. Figure 1 shows the basic power circuit for operation from a single-phase ac supply. The load is switched alternately between the positive and negative rails of the dc supply. By appropriate control of the switching instants of the power devices, an output voltage waveform can be produced whose fundamental is of the required frequency and amplitude (Figure 2). The details of PWM waveform generation are discussed in Appendix 1.

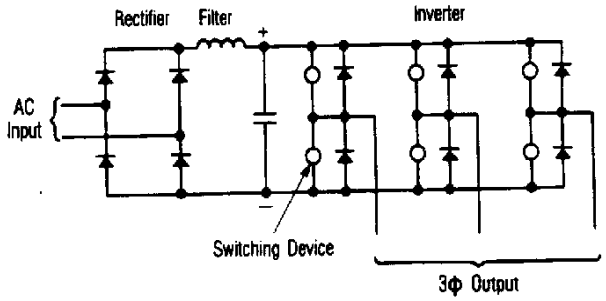


Figure 1. Inverter circuit

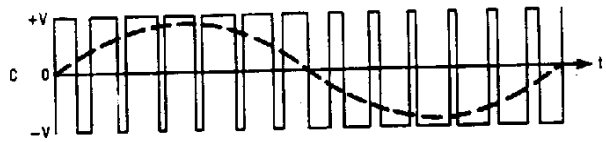


Figure 2. Pulse-width modulated waveform (line to neutral).

Power MOSFET switching speeds permit the use of a switching frequency outside of the audible frequency range. Since in a typical application the switching frequency is a least an order of magnitude higher than the output frequency, output filtering is a practical proposition. This makes variable-frequency ac supplies possible that are virtually free of harmonics and RFI problems. Audible acoustic noise is also eliminated, making such systems acceptable for use in home and office. Applications include variable frequency ac motor drives and uninterruptible power supplies.

The Need For An Inverse Diode

Figure 1 shows a diode connected in inverse parallel across each switching device. These diodes are variously referred to as "feedback," "reactive," "reactive feedback," "freewheeling," "clamp," or even "protection" diodes. Whatever they're called, their presence is fundamentally necessary to the circuit operation.

The load connected to the output of each phase of the inverter will generally be either the filter inductor or an inductive load, such as one phase of the stator winding of a motor. Due to the wide separation of the switching frequency and the output frequency, the load will appear highly inductive relative to the switching frequency and, therefore, the load current will be approximately constant and continuous within each switching cycle. That means that during a switching cycle within each "leg" (or "pole") of the bridge the load current commutates between one of the switching devices and one of the freewheeling diodes.

If the switching devices are HEXFETs, the integral body-drain diode contained within the HEXFET structure may be used as the freewheeling diode. Therefore, only six HEXFETs are required to form a complete three-phase bridge, as Figure 3 shows.

The output current and voltage waveforms for one leg of such an inverter at various points during the output cycle are shown in Figure 4. When load current is flowing out of the center point of the bridge the top HEXFET and bottom diode conduct alternately. When load current is flowing into the center point, the bottom HEXFET and top diode conduct.

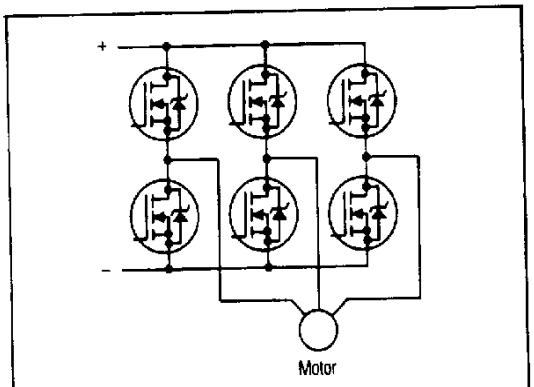


Figure 3. A three-phase inverter using HEXFETS

Problem With Using The Body-Drain Diode

Whichever direction the load current is flowing, each switching cycle sees the commutation of the load current from the body-drain diode of one HEXFET to the channel of the other. This occurs when the previously non-conducting HEXFET turns on and results in a pulse of diode recovery current flowing between the rails of the dc power supply. The magnitude of the "short-circuit" current is limited by parasitic circuit inductance and by the transconductance of the HEXFET. Figure 5 shows the waveforms associated with turn-on of one of the HEXFETs in a bridge inverter.

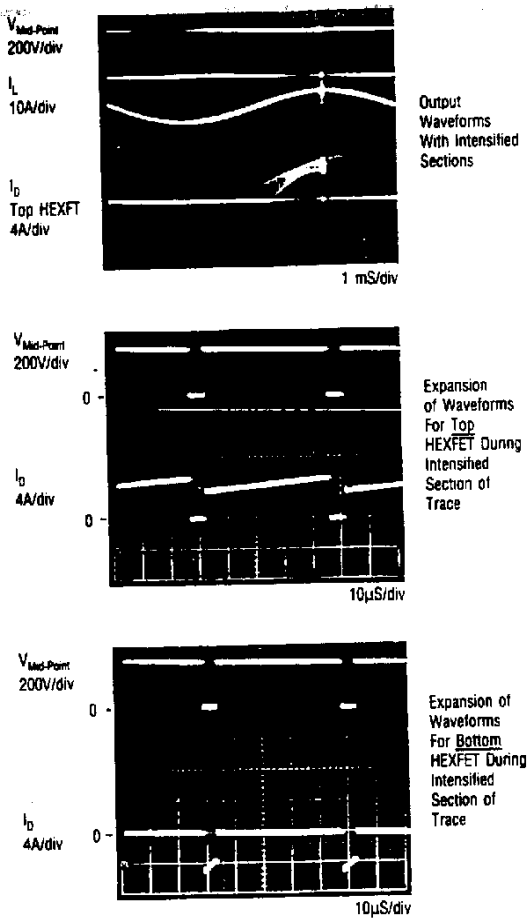


Figure 4a. Current in top and bottom HEXFETS during positive load current

The waveforms shown in Figure 5 were obtained by controlling the gate voltage so that the drain current, composed of the load current plus the diode recovery current, reached the maximum allowable value of drain current I_{DM}, thereby allowing commutation to take place in the shortest possible time. By this means the total commutation losses are minimized. However it is possible to reduce the magnitude of the diode-recovery current to practically any value desired by slowing down the turn-on of the HEXFET. Commutation losses are not reduced until switching is slowed to a point where the delay time and switching time might compromise the quality of the PWM waveform. Although the diode-recovery current pulse appears large in amplitude, it is brief in duration and even with a switching frequency of 20 kHz, the losses produced by the diode-recovery current are acceptable. This is demonstrated later.

The diode recovery current has two main consequences. Firstly, it causes losses in the MOSFETs. More seriously, it tends to initiate conduction of the internal parasitic bipolar transistor contained within the structure of every power MOSFET. The consequence of the parasitic bipolar transistor turning on is that the cell loses its blocking capability, current crowds into that cell and the device is destroyed. It is therefore essential that for inverter applications, power MOSFETs should be used that are immune to this phenomenon.

Diode-Recovery dv/dt

Figure 6 demonstrates the presence of a parasitic bipolar transistor within the double-diffused power MOSFET structure. This parasitic transistor is muted by the shorting of its

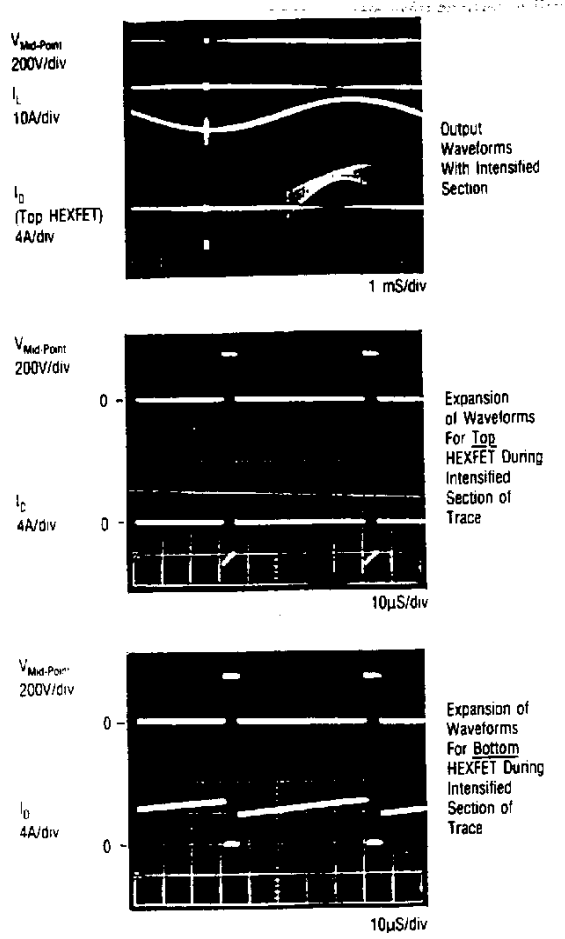


Figure 4b. Current in top and bottom HEXFETs during negative load current

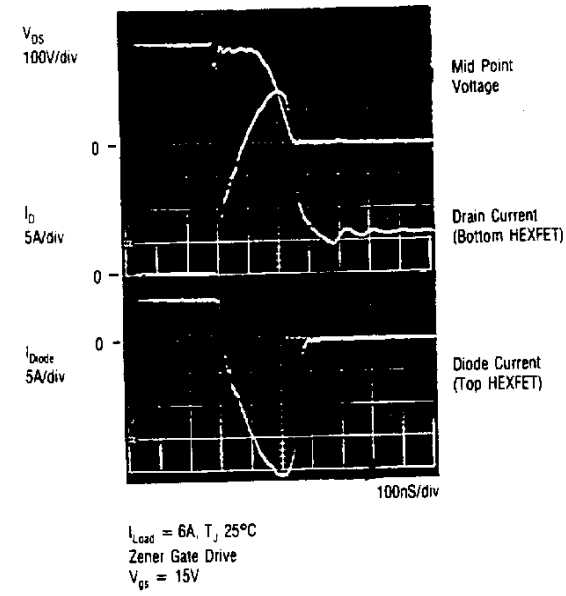


Figure 5. Turn-on current waveforms for inverter consisting of two IRF840 HEXFETS

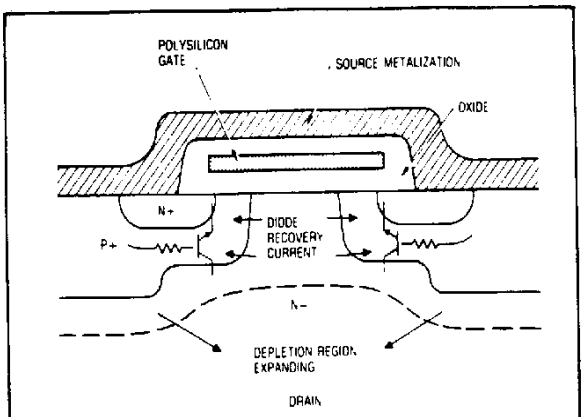


Figure 6. The parasitic bipolar transistor and diode recovery currents in a DMOS power MOSFET

base and emitter regions through the source metalization. However, it is possible for the base emitter junction to become forward biased if a significant amount of current flows laterally through the P-body region. One way of creating this lateral current flow is by avalanche breakdown. The HEXFET III range of devices have been designed to tolerate high levels of avalanche current without activation of the parasitic bipolar transistor [Ref 1].

A second way in which lateral current flow can be generated in the P-body region is by rapid recovery of the body-drain diode after carrying current. Figure 6 illustrates this effect. The drain drift region of the device is saturated with minority carriers as a result of diode conduction. During recovery of the diode a depletion region is formed between the P-body region and the N-type drift region. This sweeps out the remaining carriers as it expands into the drift region. Without proper device design this sweep-out current can be exceptionally large in certain cells of the power MOSFET, thereby causing the parasitic bipolar transistor to conduct with catastrophic consequences.

The critical moment for the device comes as the diode is recovering and the MOSFET (and its internal parasitic bipolar transistor) is called upon to block forward voltage. The more rapid the rise of drain voltage, the more likely is activation of the parasitic bipolar transistor.

The designer of bridge inverters who wishes to make use of the integral diode of a power MOSFET, therefore, needs assurance that the device will not fail under these conditions. The HEXFET III generation of power MOSFETs are rated for dv/dt. The rating is called the diode-recovery dv/dt rating, since it describes the HEXFET's ability to withstand dv/dt during diode recovery. A dv/dt capability of at least 3 V/nS is required in a typical PWM inverter operating from a rectified 220 V ac supply. All HEXFET III devices are rated above this value. A full description of the new ratings can be found in Reference 1.

HEXFET III dv/dt ratings are generally adequate to encompass values of dv/dt found in typical inverter applications. Therefore, when using HEXFET III devices it is unnecessary to slow down switching of the HEXFETs in order to limit dv/dt, although the switching speed may need to be adjusted for other reasons such as maintaining the diode recovery current within the I_{DM} rating and limiting RFI.

Avalanche

As Figure 3 illustrates, the HEXFET symbol employs a zener or avalanche diode symbol to represent the integral body-drain diode. This reflects the enhanced avalanche capabilities of the HEXFET III generation of power MOSFETs, which

are rated for both high-energy non-repetitive avalanche breakdown as well as repetitive avalanching. This avalanche capability adds to the suitability of the HEXFET for inverter applications. As well as being able to tolerate voltage spikes produced by such events as sudden load connection and disconnection and contactor operation, HEXFETs can tolerate overvoltage transients produced during normal operation. For example, if a large amount of parasitic inductance is included in the mid-point of the inverter, as shown in Figure 7, energy will be stored in this inductance during diode recovery. As the waveforms in Figure 8 demonstrate, this energy results in avalanche operation of the HEXFET. The device used in Figure 8 is experiencing first diode-recovery dv/dt (actually well above the rated level) followed immediately by avalanche operation.

An important benefit of the avalanche capability of HEXFET III devices is that since they can tolerate avalanche operation, traditional safety margins which are applied when selecting the voltage rating can be relaxed. This is particularly beneficial in the case of power MOSFETs since their $R_{DS(ON)}$ increases rapidly with voltage rating.

Diode Recovery Losses

At the beginning of every switching cycle the load current is circulating through the body-drain diode of one HEXFET prior to the turn-on of the other HEXFET. Before the diode can sustain a reverse voltage a quantity of charge must be extracted. Further charge is extracted as the voltage of the center point of the bridge swings between power rails with a corresponding rise in the reverse voltage of the diode. The total charge associated with diode recovery flows between the rails of the dc supply without doing useful work. The diode recovery current therefore constitutes a loss of energy which appears as heat in the HEXFETs. (The commutation process is illustrated in Figure 5).

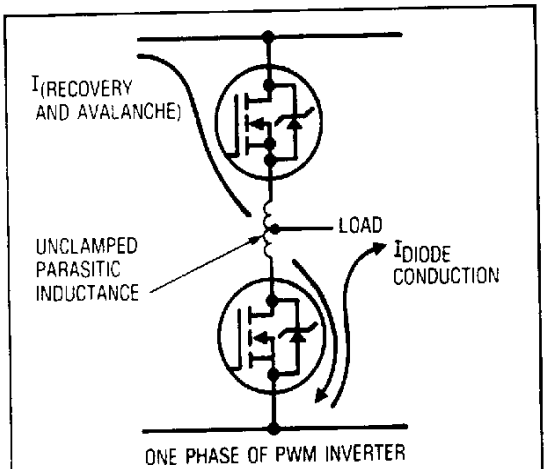


Figure 7. Unclamped parasitic inductance in a bridge circuit

Figure 9 shows the voltage and current waveforms during turn-on of one of the HEXFETs in a bridge composed of a pair of IRF840 HEXFETs, for various values of load current.

Figure 10 illustrates the effect of switching speed on the diode reverse recovery current. The switching speed is determined by the value of the series gate resistor. The diode recovery charge, Q_{RR}, falls as the recovery time is extended due to increased minority carrier recombination.

For very low values of series gate resistance a large dip occurs in the dc supply rail voltage due to the parasitic inductance of the reservoir capacitors and the system wiring. While this may not be too detrimental to waveform quality, it is likely to contribute to the level of RFI generated by the circuit. The gate voltage used in Figure 10 was set by a level which would cause the peak drain current to be limited by transconductance, below the I_{DM} rating of the device.

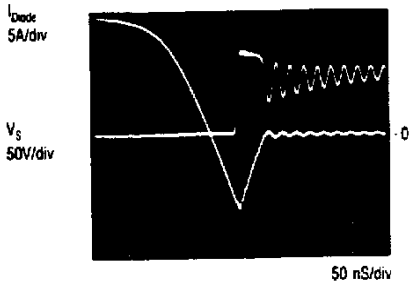
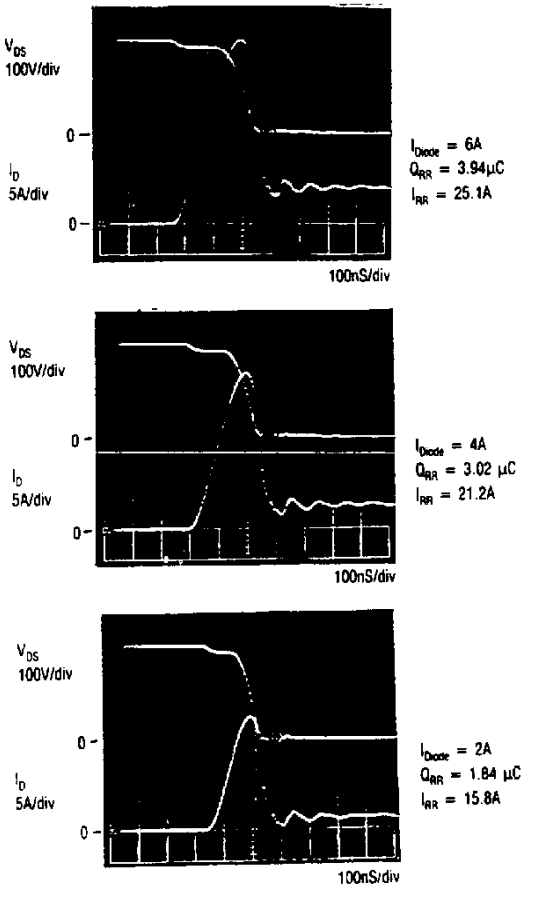


Figure 8. An IRF530 subject to diode recovery dv/dt and avalanche



T_J = 25°C, V_{GS} = 15V, R_G = 220Ω

Figure 9. Variation of recovery current with load current (IRF840)

The diode recovery charge for HEXFETs increases with temperature, but not greatly, as Figure 11 illustrates. This contrasts with other types of power MOSFETs in which minority carrier lifetime killing is employed in order to reduce the recovery time of the diode. As Figure 12 shows, the lifetime killing becomes ineffective as the junction temperature is raised so that at typical maximum junction temperature there is little difference between the speed of the HEXFET and other types of "fast diode" power MOSFETs.

With reference to Figure 13, during turn-on of HEXFET2, the dc rail voltage will be supported by the circuit inductance, the body-drain diode of device 1 and the drain source voltage of device 2. During the period when the body-drain diode of HEXFET 1 is still saturated with carriers and cannot support reverse voltage, the dc rail voltage is approximately distributed across the circuit inductance and the drain-source of HEXFET 2.

The rate of rise of current in HEXFET 2 is controlled by the rate of rise of its gate voltage, since drain current and gate voltage are linked by transconductance. The rate of rise of current determines the voltage drop across the circuit inductance (since $V = L \times di/dt$). The rest of the dc rail voltage appears across HEXFET 2.

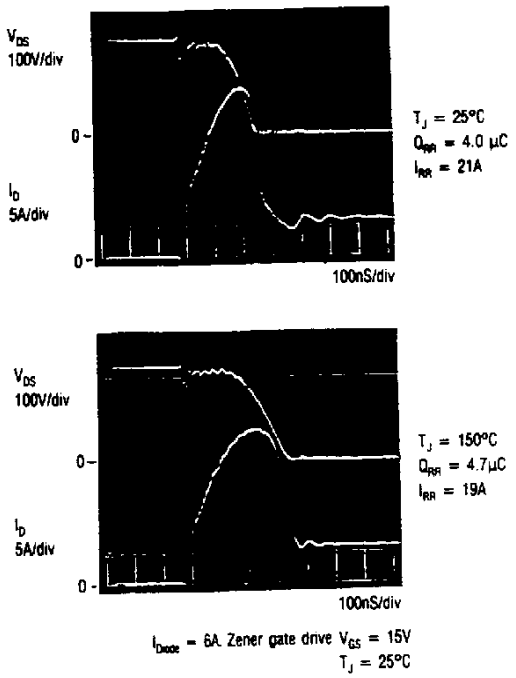


Figure 11. Variation of diode recovery current with junction temperature (IRF840)

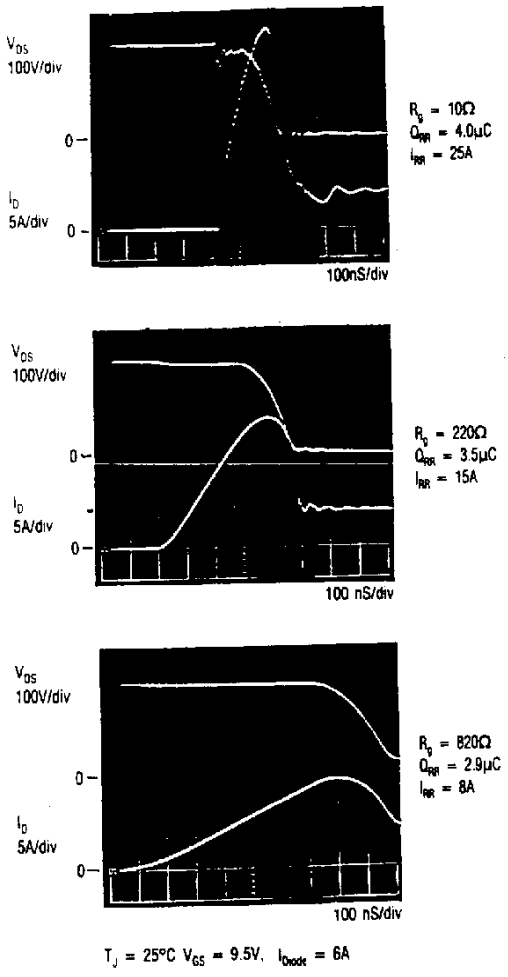


Figure 10. Variation of recovery current with switching speed (IRF840)

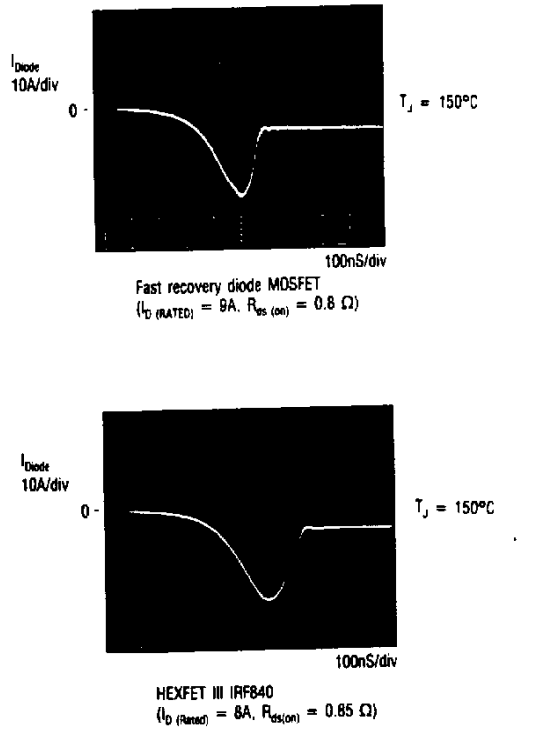


Figure 12. Comparison of recovery time of HEXFET III and MOSFET with minority carrier lifetime killing

The value of parasitic circuit inductance generally will not influence the di/dt during turn-on in an "off line" application. For example, the maximum di/dt in Figure 9 is about 0.15A/nS. This di/dt would develop a voltage of 30V across a typical circuit inductance of 200nH. If the dc bus voltage is 300V, this leaves 270V across HEXFET 2, leaving it still very much in its "linear" region of operation, and fully "in control" of its own di/dt. (The situation can be different for a low voltage high current circuit, or where inductance is purposefully added in the dc bus).

There are a number of ways in which the rate of rise of gate voltage can be controlled, and the reader is referred to IR Application Note AN-937.

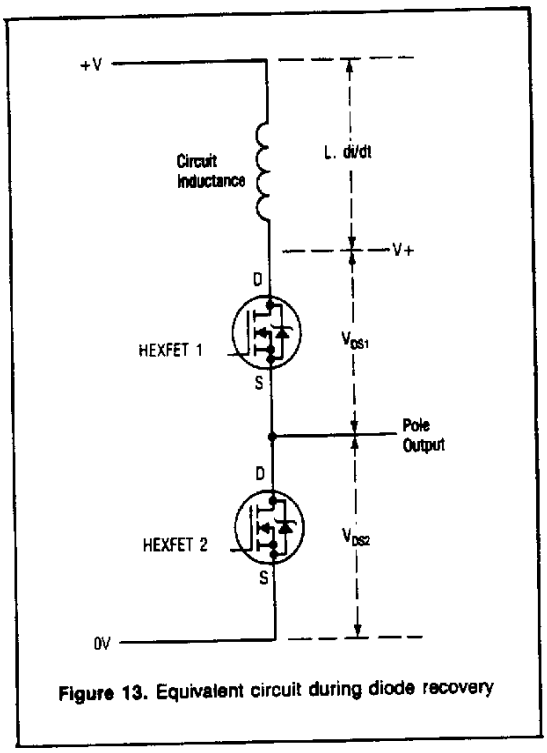


Figure 13. Equivalent circuit during diode recovery

Figure 14 shows an idealized version of the waveforms associated with the turn-on of the lower HEXFET (device 2) in one leg of an inverter. The origin of these waveforms is as follows:

t0 - t1. Delay time. The gate capacitance is charging to the threshold value, which it attains at time t1.

t1 - t2. HEXFET 2 starts to conduct, with a di/dt determined by the rate of rise of the gate voltage. The di/dt causes a voltage drop in the circuit inductance. The rest of the dc rail voltage is supported by the HEXFET. By t2 HEXFET 2 has taken over the load current from the diode of HEXFET 1 and the diode current has fallen to zero.

t2 - t3. Negative diode current in HEXFET 1 (shown as positive drain current) removes charge from the diode of HEXFET 1. At time t3 sufficient charge has been removed to enable HEXFET 1 to block voltage.

t3 - t4. The drain voltage of HEXFET 2 falls as the voltage across HEXFET 1 rises. Miller feedback now influences the switching of HEXFET 2. The diagram shows a constant current during this period. In reality the current is determined both by the Miller feedback and the relationship between rate of change of voltage and diode current during this stage of the recovery.

t4 - t5. The dc rail voltage, aided by the voltage across the circuit inductance produced by the changing current, now appears across HEXFET 1, and the current in its diode decays to zero.

In practice the periods t3 - t4 and t4 - t5 are very short and merge together. The fall in diode current is in fact very rapid at this time and the gate voltage falls to threshold level as the drain current falls to zero. The gate voltage then rises as the gate capacitance is charged through the series gate resistor.

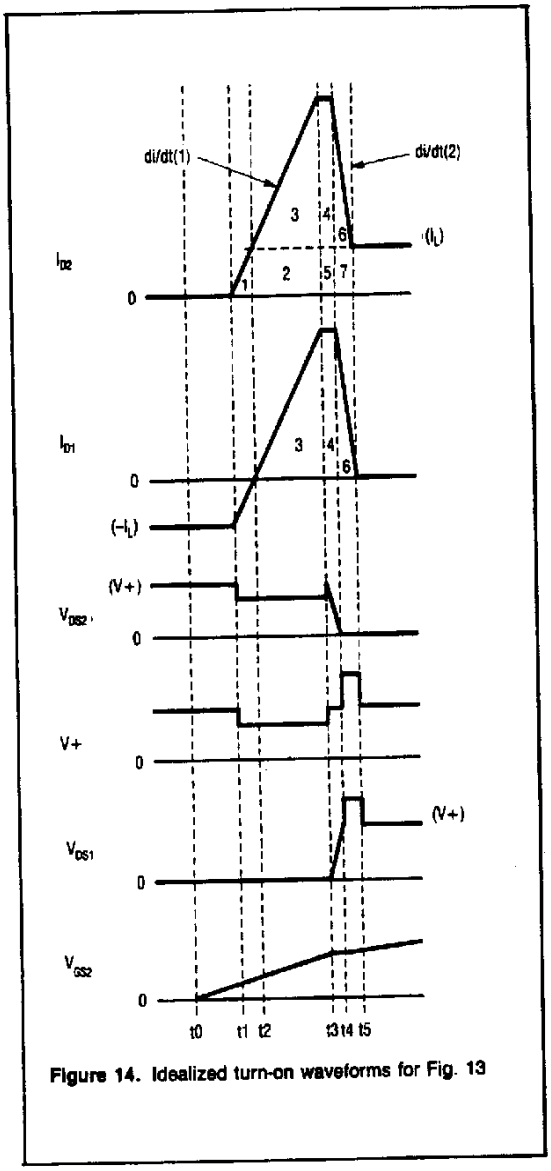


Figure 14. Idealized turn-on waveforms for Fig. 13

Figure 15 shows the waveform photographs corresponding to the theoretical waveforms shown in Figure 14.

Effect of di/dt and Temperature on Q_{RR}

Figure 16 illustrates how Q_{RR} varies with switching speed. The relationship between Q_{RR} and di/dt is shown in Figure 17.

Figure 18 illustrates the effect of increasing temperature on Q_{RR}. The relationship between Q_{RR} and temperature is shown in Figure 19.

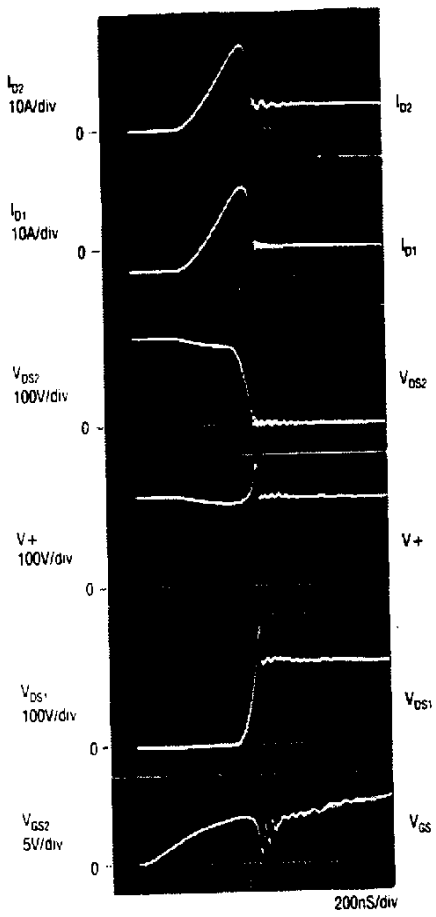


Figure 15. Waveform photographs correspondent to Fig. 14

Calculation of Switching Losses

The losses incurred during commutation may be predicted from Figure 14.

Conduction losses are ignored and only those losses produced when devices are simultaneously carrying current and blocking voltage are considered.

The losses in HEXFET 2 are as follows:

t1 - t2. The drain current builds up to the value of the load current while supporting the available voltage (dc rail voltage minus the drop in the circuit inductance.)

t2 - t3. Both the load current and the rising diode recovery current are carried while blocking the available voltage.

t3 - t4. Some losses incurred during this period but not a significant amount since the drain voltage is falling rapidly.

As the losses in HEXFET 2 decline the losses in HEXFET 1 increase:

t3 - t4. Some losses incurred as the voltage across the diode increases.

t4 - t5. The final phase of the diode recovery current producing losses, since the diode now blocks the available voltage.

The losses in HEXFET 1 and HEXFET 2 have two basic origins: the conduction of the load current by HEXFET 2 during the period t0 - t3 and the passage of diode recovery current through both devices during the period t1 - t5.

Estimation of the total losses is simplified if it is assumed that the effect of the circuit inductance is neutral, in that while it reduces the available voltage during one part of the switching cycle, it increases it during another. (If the breakdown voltage of the HEXFET is exceeded then this energy will be dissipated in avalanche breakdown, which is permitted with HEXFET III devices, provided the repetitive avalanche ratings are respected). Therefore, if it is assumed that all charge transfer takes place between supply rails whose voltage remains constant at the nominal value, the total losses during commutation of the inverter leg may be calculated approximately by multiplying the dc rail voltage by the various transfers of charge that occur. If a series inductor with its own clamping circuit is located in the dc rail, then energy stored in this inductor is not dissipated in the HEXFET but in the clamp circuit.

Thus the losses in HEXFET 2 are given by the rail voltage times the charge represented by areas 1, 2 and 3 in Figure 14. The losses in HEXFET 1 are given by the rail voltage times the charge represented by area 6. Losses associated with areas 4 and 5 are distributed between the two HEXFETs. The total losses are therefore approximately equal to the rail voltage multiplied by the charge represented by areas 1, 2, 3, 4, 5 and 6. Areas 3, 4 and 6 represent the Q_{RR} of the diode. Areas 1, 2 and 5 are a function of the load current and the rate of rise of diode recovery current, di/dt.

Thus the total commutation energy loss may be expressed as:

$$E = V_{dc}\,[(\text{Area 3} + \text{Area 4} + \text{Area 6}) + (\text{Area 2} + \text{Area 5}) + (\text{Area 1})]$$

$$= V_{dc}\left[Q_{RR} + I_L\,(t_4 - t_2) + (t_2 - t_1)^2 \cdot \frac{di/dt}{2}\right]$$

$$= V_{dc}\left(Q_{RR} + I_L\sqrt{\frac{2Q_{RR}}{di/dt}} + \frac{I_L^2}{2di/dt}\right) \qquad (1)$$

Where I_L is the load current at the time of the commutation.

This gives the energy loss for the pulse at one value of drain current. From Figure 20 it can be seen that to a first approximation Q_{RR} is linearly related to drain current and therefore, assuming a sinusoidal load current, can be expressed as:

$$Q_{RR}(t) = K \cdot i(t)$$
$$= K \cdot I_L \sin(\omega t),$$

and:

$$Q_{RR}(\theta) = K \cdot I_L \sin\theta, \text{ where } 0 < \theta < \pi \qquad (2)$$

Substituting into (1) for Q_{RR} gives the energy dissipated when a commutation occurs at a current value of I sin θ.

$$E(\theta) = V_{dc}\left[K \cdot I_L \sin\theta + I_L \sin\theta\sqrt{\frac{2KI_L \sin\theta}{di/dt}} + \frac{I_L^2 \sin^2\theta}{2\,di/dt}\right] \qquad (3)$$

The power loss due to commutation during that switching cycle is given by:

$$P(\theta) = V_{dc} \cdot f_s\left[K \cdot I_L \sin\theta + I_L \sin\theta\sqrt{\frac{2KI_L\sin\theta}{di/dt}} + \frac{I_L^2 \sin^2\theta}{2\,di/dt}\right] \qquad (4)$$

Where f_s is the switching frequency

Since the switching frequency is approximately two orders of magnitude greater than the output frequency, equation (4) can be taken as representing the power loss due to commutation expressed as a continuous function of θ.

The average power loss due to commutation during one half cycle of output current is therefore given by:

$$P_{ave} = \frac{V_{dc} \cdot f_s}{\pi}\left[K \cdot I_L \int_0^{\pi} \sin\theta \, d\theta + I_L \sqrt{\frac{2KI_L}{di/dt}} \int_0^{\pi} \sin^{3/2}\theta \, d\theta + \frac{I_L^2}{2di/dt} \int_0^{\pi} \sin^2\theta \, d\theta\right]$$

$$= \frac{V_{dc} \cdot f_s \cdot I_L}{\pi}\left[2K + 2.47\sqrt{\frac{KI_L}{di/dt}} + 0.785\,\frac{I_L}{di/dt}\right] \quad (5)$$

This represents the sum of the commutation power loss in both HEXFETs in that inverter "leg" (or "pole").

The process for determining the commutation losses is therefore:

(1) Read the typical value for Q_{RR} from the data sheet.

(2) Adjust Q_{RR} for di/dt and temperature, using the graphs shown in Figure 17 and Figure 19.

(3) Using this value of Q_{RR} obtain K from the equation:

$$K = Q_{RR} / I_F$$

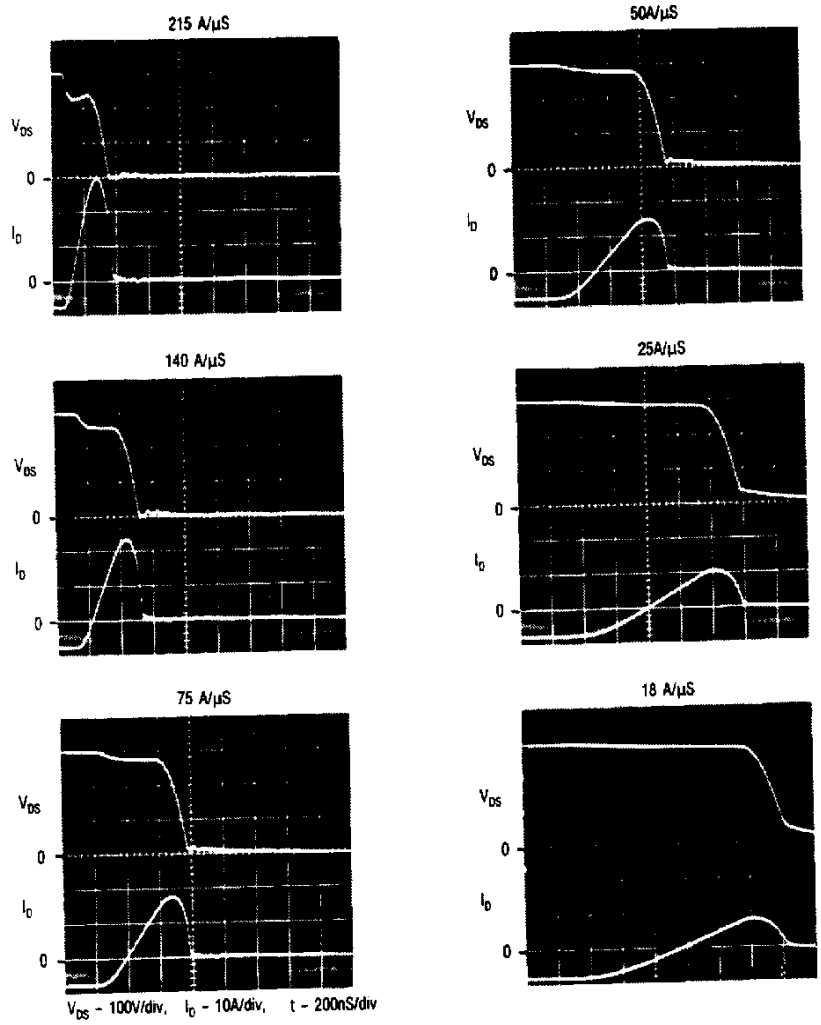


Figure 16. Diode recovery waveforms for a range of di/dt

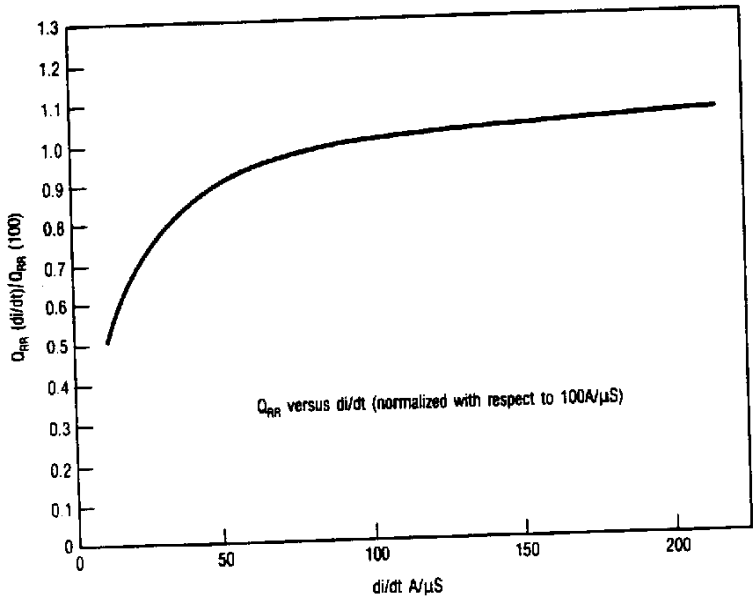


Figure 17. Relationship between Q_{RR} and di/dt

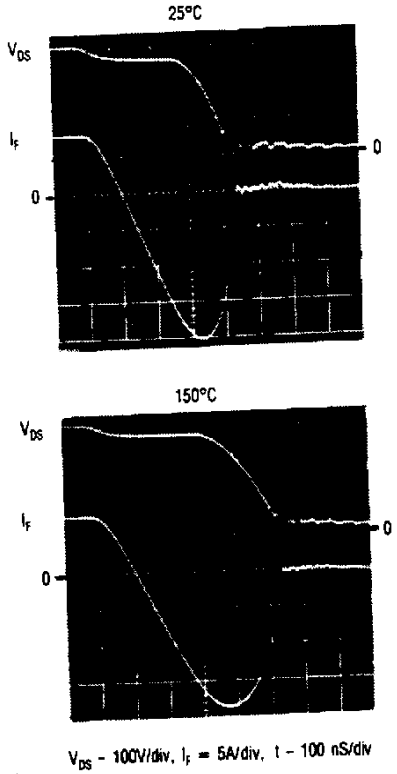


Figure 18. Effect of temperature on Q_{RR}

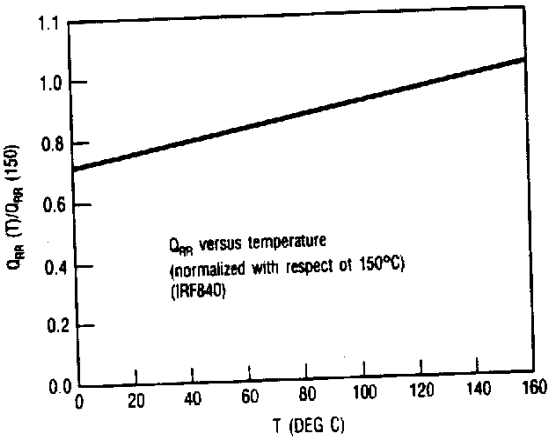


Figure 19. Relationship between Q_{RR} and temperature

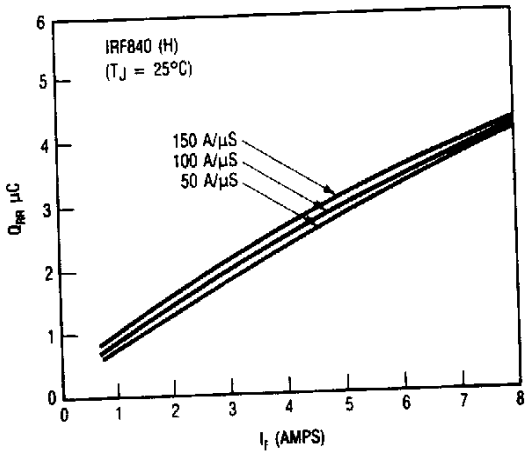


Fig. 20 — Q_{RR} vs. Drain Current

where I_F is the test current specified in the typical Q_{RR} rating in the data sheet.

(4) Substitute K along with di/dt and I_L in equation (5) to obtain the commutation power loss.

Turn-Off Losses

As Figure 21 shows, turn-off losses are small compared with conduction losses and diode recovery losses. Therefore turn-off losses do not significantly affect loss calculations and can be ignored.

Optimum Switching Speed

As long as Q_{RR} remains constant the commutation losses can be minimized by using as high a value of di/dt as possible, as Figure 22 shows. The highest acceptable value of di/dt will be determined by how closely the peak drain current is to be allowed to approach the maximum allowable drain current, I_{DM}.

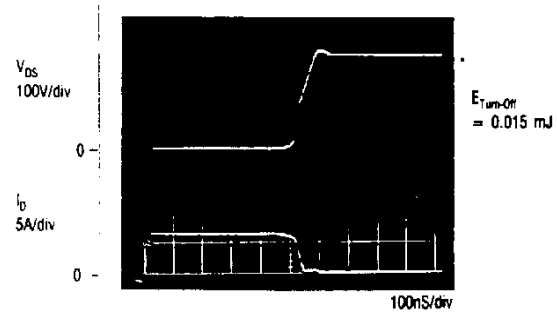


Figure 21. Turn-off (IRF840)

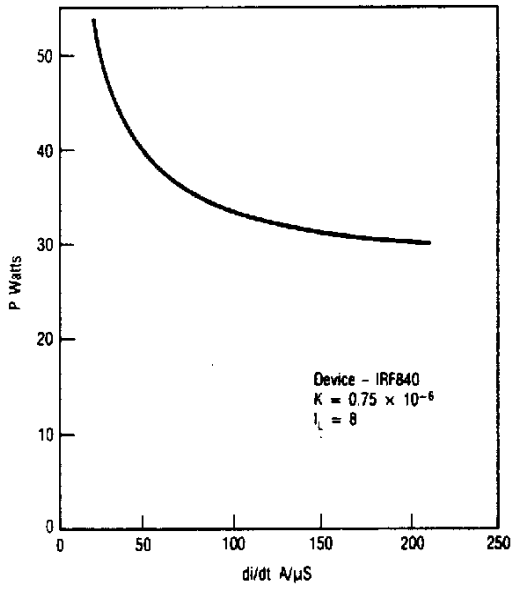


Figure 22. Commutation power loss versus di/dt

Q_{RR} is approximately constant over a wide range of di/dt as Figure 17 shows. Very low values of di/dt do lead to a reduction in Q_{RR}, but this reduction is only achieved by switching at a rate which makes the switching time unacceptably long for most PWM applications.

Conduction Losses

The load current is carried either by the channel of one HEXFET or by the body-drain diode of the other. If carried by the channel of a HEXFET the power dissipation in the HEXFET during that period is given by:

$$P_d = i_d \cdot R_{DS(on)}$$

$R_{DS(on)}$ is a function of the die temperature and, to a lesser extent, of the instantaneous value of the drain current. HEXFET data sheets include graphs of $R_{DS(on)}$ versus temperature and $R_{DS(on)}$ versus drain current.

During the period when the load current is being carried by the body-drain diode of one of the HEXFETs the power dissipation is given by:

$$P_d = i_d \cdot V_{SD}$$

V_{SD}, the forward drop of the body-drain diode, is a function of the load current. HEXFET data sheets incorporate a graph showing V_{SD} versus diode current.

Since the direction of current flow at any time is not predetermined, but rather is determined by load conditions, the upper HEXFET is kept on all the time during positive segments of a switching cycle and the lower HEXFET is kept on during the negative segments of a switching cycle (except for short deadbands when both devices are off to prevent overlapping conduction and shoot-through). When load current is flowing through a body-drain diode, therefore, the channel associated with that diode will be in conducting state. A proportion of the load current will flow through the channel, since current can flow through the channel of a HEXFET in either direction. This lowers the voltage drop across the HEXFET. In high voltage devices with relatively high values of $R_{DS(on)}$ this effect will be negligible but in low voltage inverters conduction losses can be mitigated by this effect. Diode recovery losses, however, are not affected since the channel is turned off prior to commutation, to avoid a shoot-through, and the freewheeling current reverts to flowing in the diode.

As Figure 23 shows, during each switching cycle the proportion of time spent in each mode (channel conduction or diode conduction) depends on the modulation duty cycle, δ, prevailing during that switching cycle. The modulation duty cycle is directly related to the required magnitude of fundamental output voltage at that time. Therefore, for a sinusoidal output waveform, the division of losses between channel conduction and diode conduction varies sinusoidally throughout the output cycle. At the same time the magnitude of the load current varies with a phase relationship to the fundamental voltage output waveform that is determined by the load power factor.

Calculation of Conduction Losses

Heat sinking must be sized for worst-case dissipation, which occurs when the load power factor is unity and the longest MOSFET conduction periods coincide with the peaks of the load current. As will be seen, diode conduction losses are much less than MOSFET forward conduction losses, so that although diode losses increase as the load phase angle moves away from 0°, the total losses are reduced. Similarly total losses are greatest when the modulation depth is unity (assuming sinusoidal modulation).

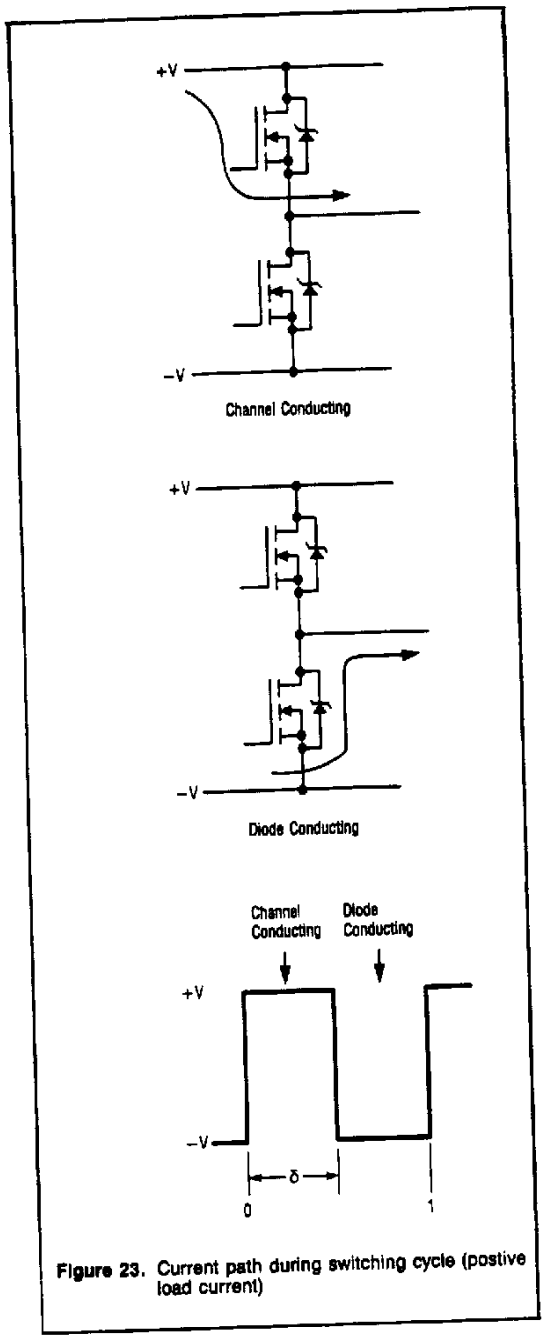


Figure 23. Current path during switching cycle (postive load current)

Under these conditions the MOSFET losses may be calculated as follows. Assume a load current waveform or the form $I_L \cdot \sin\theta$. During a switching cycle occuring approximately at a time corresponding to the angle θ, the MOSFET will conduct in the forward direction for a proportion of the cycle given by:

$$\text{MOSFET pulse width} = 1/2\ (1 + \sin\theta)$$

The proportion of the cycle for which the diode conducts is given by:

$$\text{Diode pulse} = 1/2\ (1 - \sin\theta)$$

Therefore the MOSFET power loss during a pulse occuring at angle θ is:

$$P(\theta) = I_L^2\ R$$
$$= I_L^2 \sin\theta .\ 1/2\ (1 + \sin\theta) \cdot R_{DS(on)}$$
$$= 1/2\ I_L^2\ R_{DS(on)}\ (\sin^2\theta + \sin^3\theta)$$

The average power loss over one half cycle is given by:

$$P_{ave} = \frac{I_L^2\ R_{DS(on)}}{2\pi} \int_0^{\pi} (\sin^2\theta + \sin^3\theta)\, d\theta$$

$$= 0.462\ I_L^2\ R_{DS(on)}$$

Figure 24 shows how losses vary with load power factor.

The diode conduction losses for a switching cycle at angle θ are given by:

$$P(\theta) = I_L \cdot V_{SD}$$
$$= I_L \sin\theta \cdot 1/2\ (1 - \sin\theta) \cdot V_{SD}$$

Where V_{SD} is the forward diode drop. To simplify calculations this is assumed to be constant for all values of current.

The average power loss due to diode conduction over one half cycle is therefore given:

$$P_{ave} = \frac{I_L \cdot V_{SD}}{2\pi} \int_0^{\pi} (\sin\theta - \sin^2\theta)\, d\theta$$

$$= 0.068 \cdot I_L \cdot V_{SD}$$

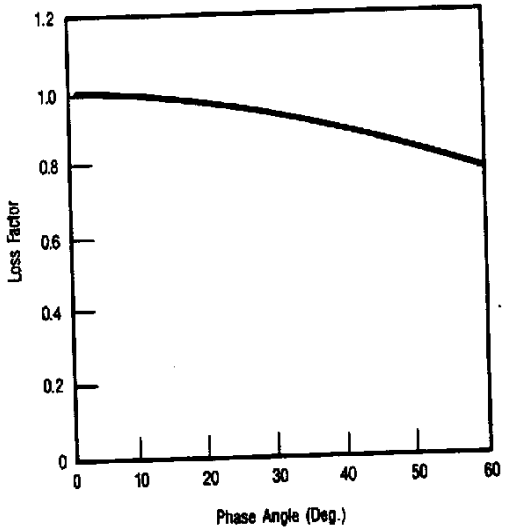


Figure 24. MOSFET conduction losses versus phase angle

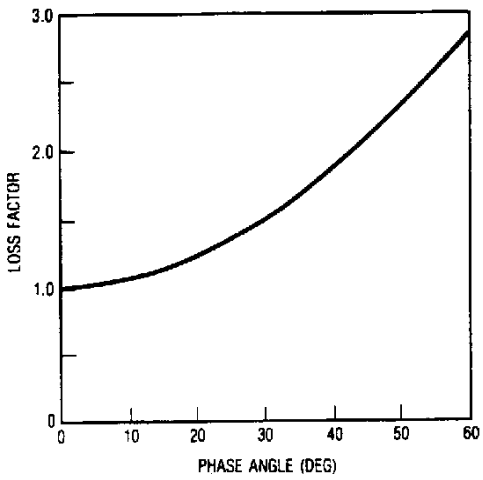


Figure 25. Diode conduction versus phase angle

Figure 25 shows how these losses vary with load power factor.

Example Design - 240V Input 1kVA Inverter

The circuit shown in Figure 26, operating from a dc supply of 305V (rectified 220Vac), using IRF840 HEXFET's, delivered an output power of 1kVA, as detailed by the following test results:

V_{dc} = 305V
Switching Frequency = 20 kHz
Output Frequency = 100 Hz
Modulation Depth = 98%
Power Factor = 0.95
I_{load} = 3.43 amps rms
T_J = 90°C
dc supply input power = 1125 Watts
ac output power = 1005 Watts
Total inverter losses = 1125 − 1005 = 120W
Inverter efficiency = 90%
Inverter rating = 1.05 kVA

The HEXFET losses may be calculated using the following data.

Measured value of I_L = 5.0 Amps (slightly higher than 2 × I_{rms} due to ripple and waveform distortion.)

The data sheet typical value for $R_{DS\ (on)}$ at 25°C is 0.8 Ohms. Using the data sheet graph of $R_{DS\ (on)}$ versus temperature, the typical value of $R_{DS\ (on)}$ at 90°C is 0.8 × 1.6 = 1.28 Ohms.

The diode forward drop is assumed to be 1 Volt for all values of current.

The average power loss per phase due to conduction is therefore given by:

P_{ave} = 0.462 I_L^2 $R_{DS(on)}$ × (phase angle factor from Fig. 24)
+ 0.068 I_L V_{SD} × (phase angle factor from Fig. 25)
= 0.462 × 25 × 1.28 × 0.972) + (0.068 × 5 × 1 × 1.22)
= 14.4 + 0.4
= 14.8 Watts per phase.

Using the data sheet value for Q_{RR} of 6.4 µC (for the conditions I_F = 9 amps at di/dt = 100 A/µs and 150°C) the value of K at 90°C and di/dt = 100 A/µs is given by:

$$K = (6.4 \times 0.9) / 8 = 0.72\ \mu C/Amp$$

$$P_{ave} = \frac{V_{dc} \cdot f_s \cdot I_L}{\pi} \left[2K + 2.47 \sqrt{\frac{KI_L}{di/dt}} + 0.785 \frac{I_L}{di/dt} \right]$$

$$= \frac{305 \times 20 \times 10^3 \times 5}{\pi} \left[2 \times 0.7 + 2.47 \sqrt{\frac{0.72 \times 5}{100}} + \frac{0.785 \times 5}{100} \right]$$

$$= 9.71\ [1.4 + 0.47 + 0.04]$$
$$= 18.5 \text{ watts/phase}$$

The calculated total HEXFET losses are therefore given by:

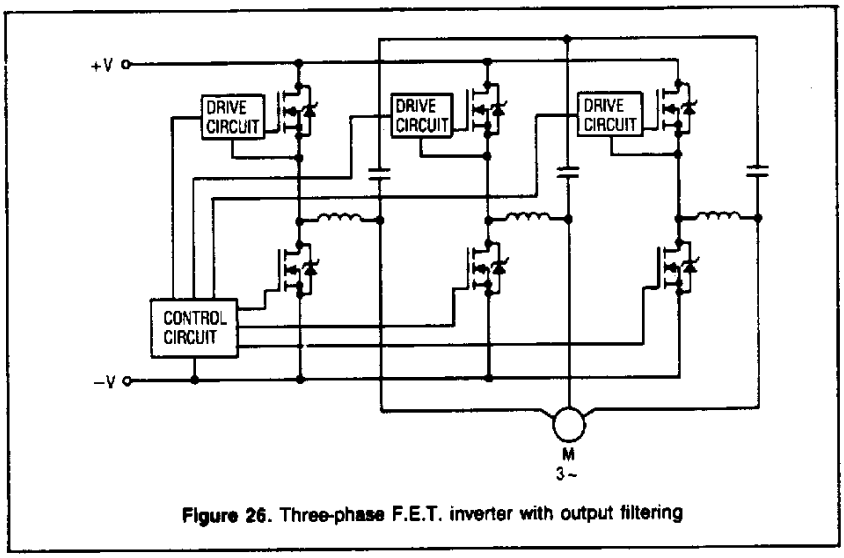


Figure 26. Three-phase F.E.T. inverter with output filtering

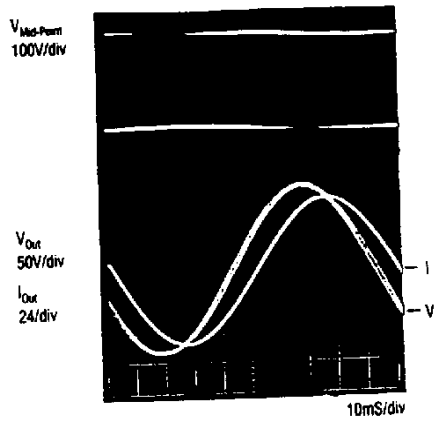


Figure 27. Output waveforms of IKVA inverter using IRF840 HEXFET

$P_{total} = 3 \times (14.8 + 18.5) = 100$ Watts.

The total measured inverter losses were 120W, of which 9W were calculated to be in the filter inductors and wiring. There is thus good agreement between the above calculated HEXFET losses and actual test measurements, with 11W "left over" for capacitor losses and HEXFET turn-off losses (not included in the above because they are relatively small).

Figure 27 shows typical output waveforms of this particular inverter.

Choice of HEXFET for Different Inverter Ratings

The power rating obtainable from a three-phase inverter using a particular HEXFET type depends on two considerations — efficiency and equipment size. The two are linked to some extent. The governing factor for both criteria is the size of the heat sink that the designer considers acceptable. A small heatsink will, for a given power output, give a high junction temperature, high $R_{DS}(on)$ and therefore higher conduction losses. The efficiency will be reduced but the equipment will be small. A larger heatsink, on the other hand, will run cooler with a lower $R_{DS}(on)$ so that although the equipment will be larger the efficiency will be higher.

Conduction losses can be reduced by using HEXFETs with a larger die and a lower $R_{DS}(on)$.

Using the previous example of the IRF840 design, the size of heatsink required can be estimated. The losses for all three phases are 100 Watts (calculated). Allowing a 40°C difference between heatsink and ambient temperatures would require a heatsink with a rating of approximately 0.38°C per Watt for all six devices. Assuming a maximum R_{thJC} of 1°C per Watt and a maximum R_{thCS} of 1° C/W, the junction temperature would be 73° C above ambient temperature. Assuming an ambient temperature of 40°C gives a junction temperature of 113° C. This is an acceptable value given that the maximum allowable junction temperature is 150°C. The calculations were based on a junction temperature of 90°C, so that if a more accurate estimate of maximum junction temperature is required another iteration is required with the new junction temperature.

However, the calculations do show that a heat sink with a thermal resistance of 0.38°C/W is appropriate. The size of such a heatsink would be, for example, 25 cm × 20cm × 4 cm. This size should be acceptable for a general industrial use 1 kVA inverter.

HEXFET Selection Guide

Table 1 is a guide to HEXFET selection for three-phase inverters of various output kVA ratings, for 120V and 240V ac line inputs, for a modulation frequency in the 20kHz range. Higher ratings will be obtainable if forced cooling is used.

Comparison with Bipolar Transistors

Due to the high switching losses associated with bipolar transistors, HEXFETs have clear advantages for dr s switching at 20kHz or higher. However, for PWM driv operating in the 1 - 2 kHz band and for quasi-square-wav drives, HEXFETs must be compared with bipolar transistors on the basis of conduction losses and cost.

The conduction losses in a HEXFET can be reduced to any level desired by using a device with a large enough die (or by parallelling devices.) This means, when using a HEXFET that cost and conduction losses may be exchanged. Therefore, when comparing HEXFETs and bipolar transistors for low switching frequency applications, it is necessary to consider the total cost of each system.

For example, consider an application requiring 400 Volt tran-

Inverter kVA Rating	AC Line Input Voltage	HEXFET Voltage Rating	Die Size	HEXFET GUIDE TO220AB	TO247AC (TO3P)	TO204AA (TO3)	TO240AA (HEXPAK)
0.3	240	500	2	IRF820	—	IRF420	—
0.5	240	500	3	IRF830	—	IRF430	—
1.0	240	500	4	IRF840	IRFP440	IRF440	—
2.0	240	500	5	—	IRFP450	IRF450	—
3.0	240	500	6	—	IRFP460	—	—
3.5	240	500	2 × 5	—	—	—	IRFK2D450
7	240	500	4 × 5	—	—	—	IRFK4H450
0.25	120	250	2	IRF624	—	IRF224	—
0.45	120	250	3	IRF634	—	IRF234	—
0.9	120	250	4	IRF644	IRFP244	IRF244	—
1.8	120	250	5	—	IRFP254	IRF254	—

sistors in which the maximum load current is 5 Amps. The nearest equivalent to a HEXFET, with its high gain and integral freewheeling diode, is a Darlington bipolar transistor with built-in anti-parallel diode. A bipolar transistor rated at 8 Amps would generally have a gain that was just adequate at 5 Amps. Such a device would typically have a guaranteed maximum value of V_{CE} of 2.0 Volts when carrying 5 Amps.

An IRF350 (400V, $R_{DS(on)}$ at 25 C = 0.3 Ohms) has a maximum Rds(on) of 0.5 Ohms at a junction temperature of 100°C. The peak forward drop (at 5 Amps) is therefore 2.5 Volts, so that the average conduction losses would be about the same or slightly lower than for the bipolar transistor; this would be enhanced by the lower switching losses and absence of base drive losses in the HEXFET. Furthermore the bipolar transistor may well require snubbering in order to operate within its SOA during switching. Based on a comparison of device and system losses the correctly chosen HEXFET can have a slight edge.

It has a bigger edge when the base/gate drive requirements, and the ability to withstand arduous operating conditions, are considered. While the bipolar transistor requires both positive and negative current base drives to achieve respectable switching times, the HEXFET may be driven directly from buffered logic. Also, the surge current rating of a HEXFET is approximately four times its average current rating, so that the IRF350 described in the above design could withstand 60 Amps, representing a 1200% overload capability. Furthermore this surge current capability is encompassed within the SOA of the HEXFET.

An important cost factor when a range of drives is planned is that an increase in the power of a HEXFET inverter only requires an increase in the ratings of the HEXFETs, whereas it is necessary to redesign the base drive and snubber circuits when a different type of bipolar transistor is used. Little or no modification is required to the HEXFET gate drive when a HEXFET of different rating is used and no snubber is required with HEXFETs. Expensive design effort is thereby reduced when a product range is designed around HEXFETs.

For operation from a rectified 120V ac supply the 250 Volt range of HEXFETs (for example the IRF244) are suitable. The repetitive avalanche capability of the HEXFET III range ensures that the margin between likely peak values of dc rail voltage and the voltage rating of the HEXFETs is more than adequate. The value of $R_{DS(on)}$ for a die of given size decreases rapidly with decreasing voltage rating. HEXFET conduction losses or HEXFET costs, therefore, reduce rapidly with decreasing voltage.

The following table compares the characteristics and performance of HEXFETs and bipolar transistors:

HEXFET	Bipolar
Integral freewheel diode.	Only some Darlingtons have diode.
No snubber required.	Snubber often required.
Low switching losses.	High switching losses.
Can be driven direct from buffered logic.	Base drive circuits required.
Same design for different power ratings.	New base drive and snubber design required for different power rating.
High overload capability.	Limited overload capability.
Avalanche capability.	Usually no avalanche capability.

References

(1) International Rectifier Application Note An-966. "A New Generation of HEXFETs — HEXFET III."

(2) D.A. Grant, J.A. Houldsworth, K.N. Lower. IEEE IAS Proc. March/April 1983. "A New High-Quality PWM AC Drive."

Appendix 1 PWM Waveform Generation

The traditional method of PWM waveform generation has been to input to a comparator a triangular timing wave and a sinusoidal reference waveform. This method has to a large extent been replaced by digital waveform generation. The digital method has the advantage of freedom from drift, absence of dc components in the output, perfect phase balance, etc. The digital method also facilitates the generation of non-sinusoidal output waveforms where this is advantageous, such as when the output of the inverter is to be increased by the addition of a third harmonic to the phase voltage waveform.

Overmodulation may be used to obtain maximum output from the inverter. While overmodulation increases the amplitude of the fundamental of the output waveform, it also introduces distortion as Figure 28 illustrates. A preferable method of increasing the amplitude of the output is the addition to the reference sine wave a measure of third harmonic as shown in Figure 29 (Ref 2). Since the third harmonic will be eliminated from the line-to-line voltage waveform, by adding a third harmonic of one-sixth amplitude of the fundamental output voltage of the inverter, its kVA rating can be increased by 15% without distortion of the output. □

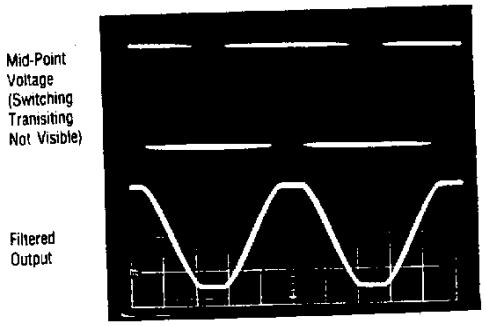


Figure 28. Distortion introduced by overmodulation

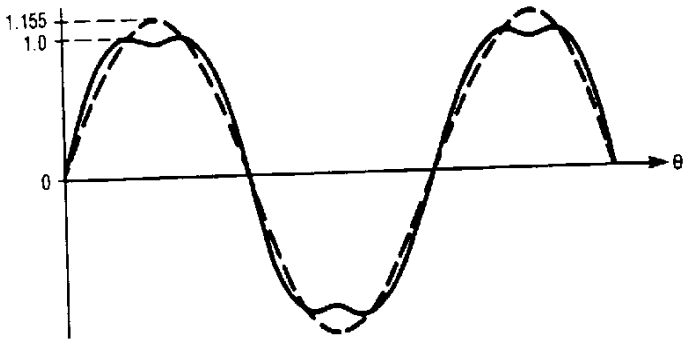


Figure 29. Increasing fundamental output voltage by addition of third harmonic

An Introduction to the HEXSenseTM Current-Sensing Device

(HEXSense and HEXFET are trademarks of International Rectifier)

by S. CLEMENTE, H. ISHII, S.YOUNG

Introduction

This application note will acquaint the designer with International Rectifier's new family of HEXFET power MOSFET devices. Designated the HEXSense "C" Series, they are essentially HEXFETs with an added current-sense capability.

HEXSen.e Characteristics

The HEXSense family extends the present HEXFET matrix. This matrix consist of a number of die sizes, HEX Z to HEX 5, arranged in geometric progression of power handling capability, i.e., each die size has approximately twice the power handling capability of the next smaller die and half that of the next larger one. Each die size is available in a range of voltage ratings. A variety of standard packages and a custom packaging capability complete the matrix.

The Figure 1 table maps out the HEXSense extension to this matrix. The HEXSense device is "downward compatible" with its corresponding HEXFET device. Current-sense capability can be obtained in existing designs without affecting power device performance.

The root IRC in the part number identifies the device as being a HEXSense device. The die size is identified by next to last digit of the part number. Other alphanumeric characters identify voltage grade, package, etc.

Figure 2 shows the first available HEXSense packages and the device I symbol.

HEXSense "C" Series
Current-Sensing Power MOSFETS

	TO-220 Package Style			TO-247 Package Style		
	Die Size			Die Size		
Voltage	HEX-2	HEX-3	HEX-4	HEX-3	HEX-4	HEX-5
50V	IRCZ20	IRCZ30	IRCZ40	IRCP030	IRCP040	—
100V	IRC520	IRC530	IRC540	IRCP130	IRCP140	IRCP150
200V	IRC620	IRC630	IRC640	IRCP230	IRCP240	IRCP250
250V	IRC624	IRC634	IRC644	IRCP234	IRCP244	IRCP254
400V	IRC720	IRC730	IRC740	IRCP330	IRCP340	IRCP350
500V	IRC820	IRC830	IRC840	IRCP430	IRCP440	IRCP450

NOTE: The die size is indicated by the last-but-one digit of the part number. For example:

IRC530 IRC720 IRCP240 IRCP350

HEX-3 HEX-2 HEX-4 HEX-5

Figure 1. HEXSense Product Matrix

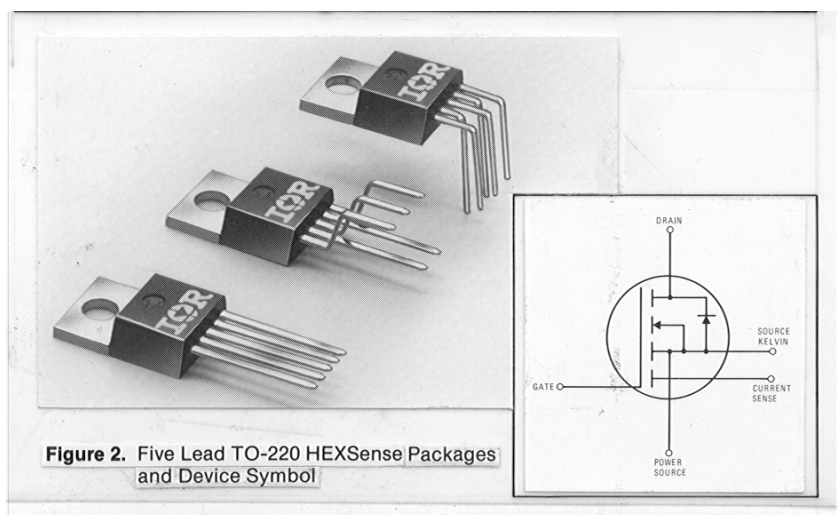


Figure 2. Five Lead TO-220 HEXSense Packages and Device Symbol

HEXSense Fundamentals

A HEXFET die is made of many transistor cells acting in parallel (Figure 3). When the device is on, current flows from drain to source via a narrow channel region around the edge of each cell. Since current is carried by majority carriers in the channel region, the drain current is distributed relatively evenly among cells and varies little from device to device of the same type. Therefore, drain current can be determined by measuring the current passing through a small number of cells and multiplying it by a scaling factor which is known for the particular device type. Little power loss is involved and thus HEXFET drain current can be determined in an almost lossless manner.

The source region of the sensing cells is covered with an isolated metallization which is connected to an external pin via a separate bonding 3 pad and bonding wire and is referred to as the sense terminal or sense pin. The subscript C is used in symbols representing the various electrical quantities associated with the current sense function, e.g., VDc, IDc or Ic, etc.

Two terminal connections are made to the source metallization of the main cells via separate bonding wires. These are the power source pin and the Kelvin source pin. The appropriate use of the Kelvin pin is very important for an accurate measurement of device current, as will beli explained later.

In practice, a HEXSense device consists of two paralleled MOSFETs with isolated sources (Figure 4), commonly referred to as "power device" and "sense device. " The key parameter of this combination is the *current sensing ratio* (r). This is the ratio between the current in the source pin and the current in the sense pin (I_{source}/I_{sense}). This ratio will, of course, be slightly different in terms of drain current, which is the sum of both currents:

$$I_D = (r+1)\, I_C$$

Under the ideal conditions of equal enhancement of all cells and perfect source metallization, the current sensing ratio would be the ratio of the number of cells in the power device to the number of cells in the sense device.

The output capacitance of the sensing cells $(C_{oss})_C$ is higher than would be expected from the area ratio alone because of the relative large capacitance of the bonding pad for the sense pin. Its effects would be felt at the inception of the fully enhanced operation (as an excess of current due to its discharge) and at its end (as a reduction of the same). However, in practice these effects are minor compared to the likely slew rate limitations of the sensing operational amplifier:

Dependence of Current Ratio on Temperature, Gate Voltage and Drain Current

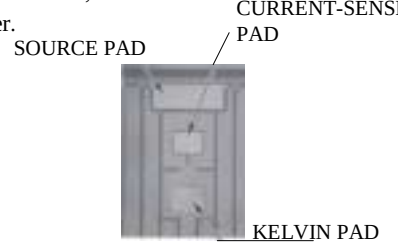
The current ratio, r, varies slightly with temperature, gate voltage and drain current. These variations have a number of causes including variations in the resistivity of the silicon from which the devices are made, temperature gradients across the die and voltage drop in the source metallizations. Typical variations in the current ratio that can be expected with variation of T_j, V_{GS} and I_D are shown for each device in the data sheet. In each case one parameter is varied while the other parameters are held constant.

The effects are cumulative so that if all three parameters vary, each will contribute to a variation in r.

Practical Implementation of the Current Sense Function

Virtual Earth Sensing

The circuit that gives the best performance in terms of speed, accuracy and noise immunity is shown in Figure 5. In a slightly modified version it was chosen for data sheet characterization and is detailed in Appendix I. For fully enhanced operation the accuracy of this circuit may be estimated directly from the data sheets and the tolerance of r. Neither the offset nor the bias current of the operational amplifier should have any significant effect on the overall static performance.



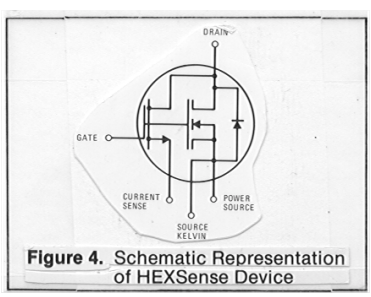


Figure 4. Schematic Representation of HEXSense Device

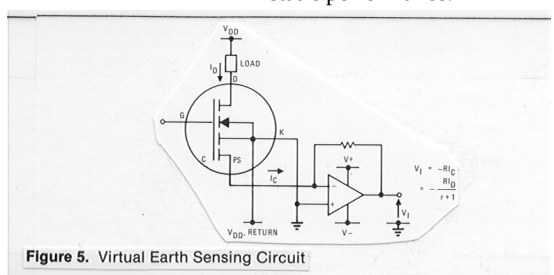


Figure 5. Virtual Earth Sensing Circuit

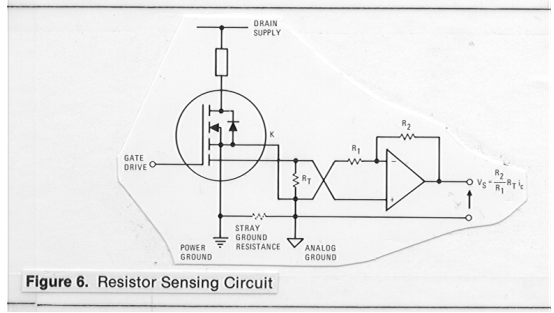


Figure 6. Resistor Sensing Circuit

However, this is not the case when it comes to dynamic performance. Current swings of 10A in 100 nsec are common in switch mode power supplies (SMPS) and similar applications. For a 5 volt output at 10A this translates into a required slew rate of 50 V / IJS which is an order of magnitude above that which commonly available operational amplifiers are capable of. The settling time of high slew-rate operational amplifiers will also affect the dynamic performance of this circuit.

Two disadvantages of this circuit are the dual power supply requirement for the operational amplifier and the negative polarity of the output voltage.

Resistor Sensing

A second circuit, shown in Figure 6, overcomes these disadvantages at a significant penalty in accuracy and performance.

In this circuit the current-to-voltage translation is performed by the sensing resistor RT, while the operational amplifier provides the necessary amplification. Input and output voltages are both positive and no negative supply is required, provided the the common mode input range of the operational amplifier includes ground (CA3130, CA3140, LM324, LM358, TLC271, etc.).

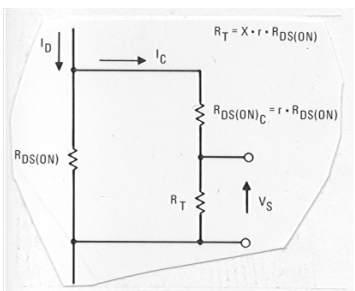


Figure 7. Evaluation of Error Introduced by R_T

The sense ratio of the circuit will vary from the nominal sense ratio due to the introduction of RT. With reference to Figure 7, assuming that RT is a share of (X) of the on-resistance of the sensing cells, which, in turn, is r times the RDS(on) of the main device,

$$I_D / I_C = 1+r (I+X)$$

The voltage across the sensing resistor will be:

$$V_S = (X/ X+) R_{DS(on)} I_D$$

Ideally, it should be:

$$V_S = X * R_{DS(on)} I_D$$

This error, I/(I+X), can be compensated for by increasing the gain of the operational amplifier by the same coefficient. However, it should be remembered that the coefficient X is not a constant because the RDS(on) of the device (and of the sensing cells) is a function of temperature, current, gate voltage and production spread. The value of R_T should be such that the voltage across its terminals at the lowest level of current at which the prescribed measurement accuracy is still required should be significantly higher than the offset of the operational amplifier. Figure 8 shows the minimum values of R_T assuming an offset of 3 mV and a minimum voltage of 20 mV, with a drain current of 10% of rated I_D at 25°C. Furthermore, if it is necessary to amplify the sense signal over a wide voltage range then the output voltage range of the operational amplifier may pose a limitation. An operational amplifier with a low output saturation voltage will be necessary if low level drain currents are to be sensed, or a negative supply may be required.

Changes in MOSFET on-resistance with temperature have an adverse effect on the overall accuracy of the sensing circuit of Figure 6. It can be shown, however, that sensitivity of V s to temperature changes becomes negligible as RT tends to values in the order of 10% of $R_{DS(on)c}$.

With reference to Figure 7,

$$V_S = (R_T/ R_T + R_{DS(on)c})*I_D*R_{DS(on)}$$

$$\sim=(R_T/ R_{DS(on)c})*I_D*R_{DS(on)}$$

$$= R_T * I_D*R_{DS(on)}/ R_{DS(on)c}$$

Since $R_{DS(on)}$ and $R_{DS(on)c}$ should change by the same factor lor a given change in temperature, the ratio $R_{DS(on)}/ R_{DS(on)c}$ should remain constant. Therefore, provided $R_T << R_{DS(on)}$, V S should not be greatly affected by changes in the device temperature.

In final analysis the value of R_T will be the lowest compatible with the offset of the operational amplifier and the noise immunity requirements of the circuit.

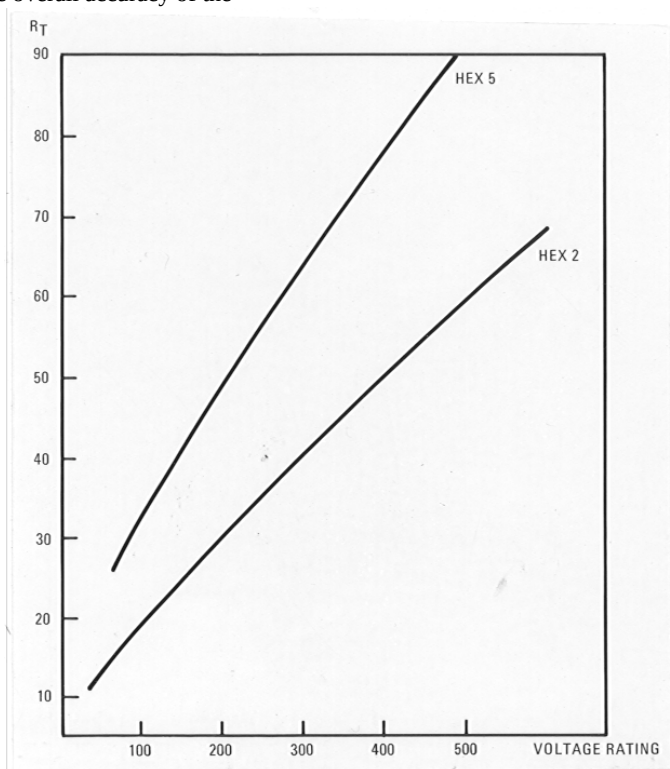
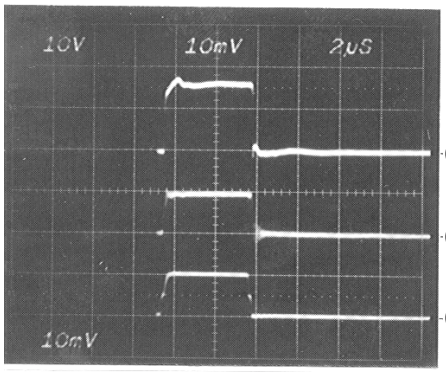


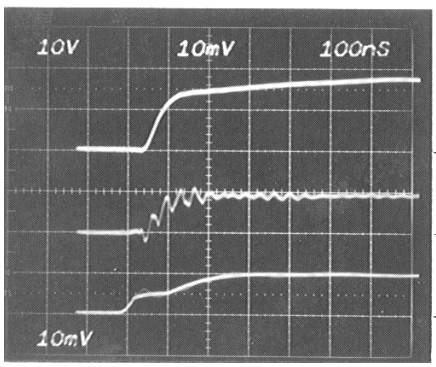
Figure 8. Minimum Value of RT to Achieve 20 mV at a Drain Current of 10% of Rated I_D @ 25°C



I_D UPPER TRACE FROM CP1
0 5A/DIV

IC MIDDLE TRACE FROM CP2
0 5 mA/DIV

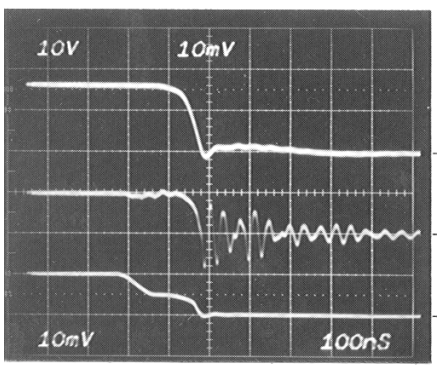
V_{GK} LOWER TRACE
0 10V/DIV



I_D UPPER TRACE FROM CP1
0 5A/DIV

IC MIDDLE TRACE FROM CP2
0 5 mA/DIV

V_{GK} LOWER TRACE
0 10V/DIV



I_D UPPER TRACE FROM CP1
0 5A/DIV

IC MIDDLE TRACE FROM CP2
0 5 mA/DIV

V_{GK} LOWER TRACE
0 10V/DIV

Using the Main Device as the Sense Resistor

If R_T is very large compared with the $R_{DS(on)}$ of the sense cells, the voltage that appears across the sense resistor will be very nearly equal to the voltage developed across the main device. In this case, therefore, the $R_{DS(on)}$ of the main device acts as the current sensing resistor and the sense cells acts as a switch which disconnects the current sense output from the sensing resistor (the main device) during the period when the HEXFET is switched off. During the off-period the current sense output is pulled low by the sense resistor rather than being pulled up to the power rail voltage. Thus, the current signal processing circuit is relieved of the necessity to withstand high voltages during a time when no useful information is available to it. The drawback with this mode of operation, of course, is that $R_{DS(on)}$ varies considerably with temperature and this must be allowed for when interpreting the current sense output.

Switching Performance

The circuit of Figure 5 will also yield a better switching performance than would otherwise be obtained with most schemes (see Figure 9) . Figure 10 shows the t6$t circuit used to obtain these waveforms. It can be seen that the switching performance is in line with the fast switching capabilities of HEXFETs. No significant delays are evident. The sense current follows the drain current during switching with no large peaks noticeable. The ringing on the current waveform is introduced by the measurement probes and is not actually present in the circuit.

Notes on the Use of the Kelvin Pin

The measurement accuracy is somewhat degraded by some parasitic resistance elements that upset the current partitioning between the power device and the sense device. As shown in Figure 11, the metallization, bonding wire and pin contribute additional resistance that is not in the same ratio as the $R_{DS(on)}$ of the sense cells and the $R_{DS(on)}$ of the main cells.

To minimize the effect of the metallization resistance, the Kelvin contact has been placed at the center of the die, close to the current sense pin.

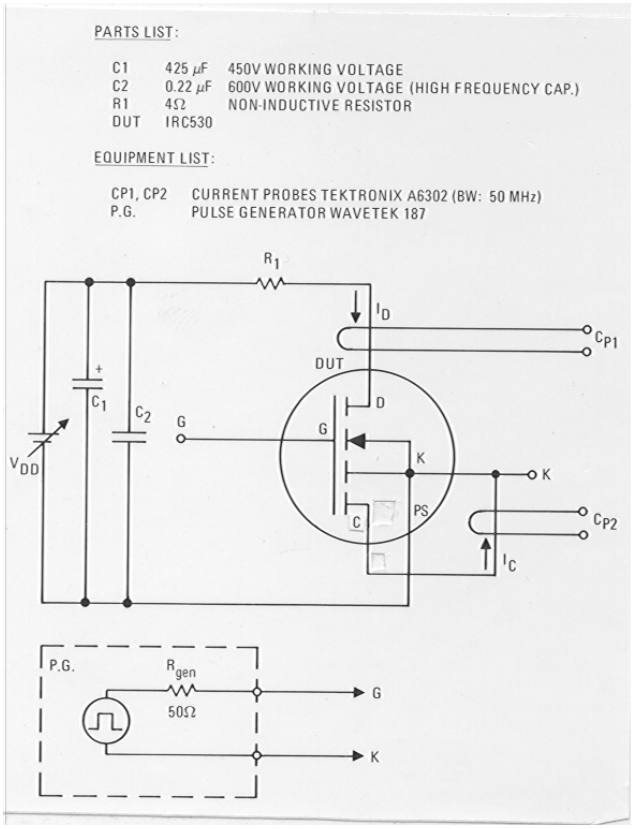


Figure 10. Test Circuit for Switching Performance

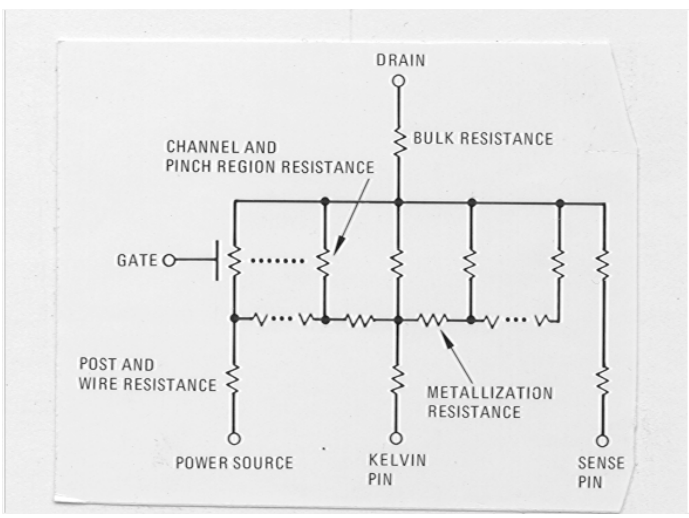


Figure 11. HEXSense Model Showing the Different Components of On-Resistance

In the sensing circuit of Figure 5, this effect can be compensated for by returning the Kelvin to the non-inverting input of the operational amplifier, so that the sense terminal, connected to the inverting input, is raised above ground by a voltage drop that approaches the drop across the parasitic resistances.

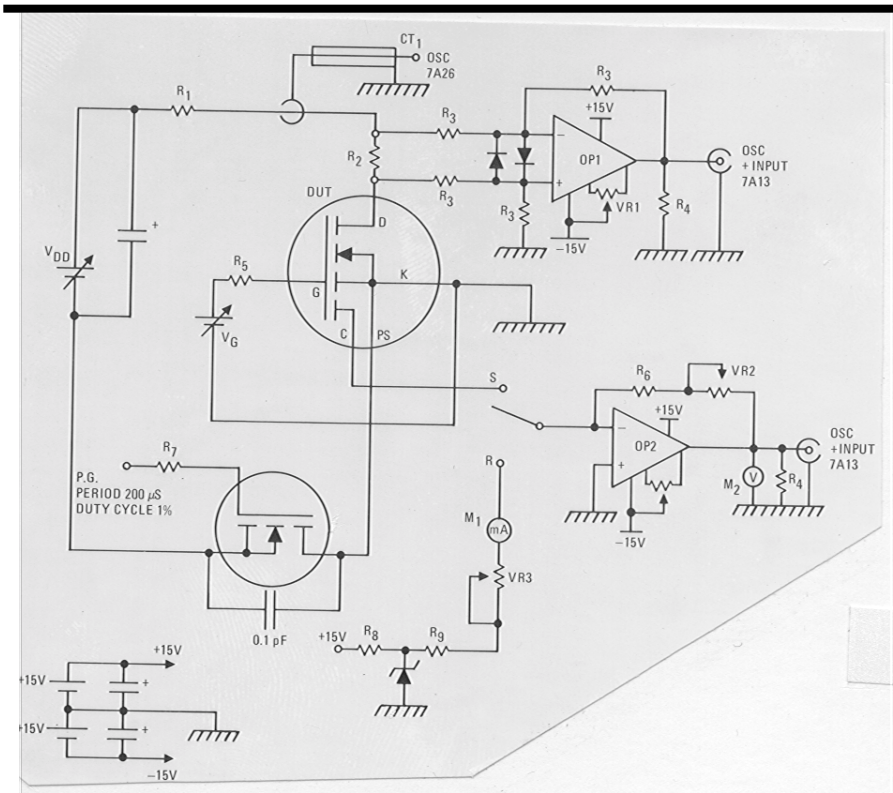
For the same reason, in the Figure 6 circuit, the sensing resistor R_T should be connected between the sense and the Kelvin pins so as to minimize the unbalancing effects of the metallization and the wire and post resistances. In practical circuits ground loops and voltage differentials between the control ground and the power ground make the use of the Kelvin contact essential.

In those power circuits in which very fast switching of the HEXFET is required, the Kelvin contact represents a useful method of bypassing the "common source inductance" which is one of the main limitations in switching speed. Inductance that is common to the drain circuit and to the gate circuit establishes a feedback into the gate drive circuit that is proportional to L_s x di/ dt. This voltage reduces the net available gate voltage and slows down the switching. By applying the gate drive signal between the gate and the Kelvin contact, the source inductance is no longer "corn.: mon" and therefore has no effect on the switching speed of the HEXFEL

APPENDIX I -Sense Ratio Characterization

This Appendix details a test method used for characterization of the nominal sense ratio under static conditions. The test circuit schematic is shown in Figure At.

The Kelvin source pin is connected to signal ground and also acts as a return for the gate-source drive voltage. The sense pin is connected to the virtual signal ground. The power source pin floats with respect to signal ground. Under static conditions and with sufficient gate overdrive the requirements of equal cell enhancement and zero appreciable stray source resistances are met. For characterization purposes the nominal sense ratio (r) is defined as the ratio between drain and sense current as measured with this circuit in the prescribed manner. The ratio r will vary with T_j, I_D and V_{GS} as indicated in the data sheets.



Parts List:

R1	2Ω	3%	5W
R2	0.1Ω	0.1%	2W
R3	10k	0.1%	¼ W
R4	200k	3%	¼ W
R5	1k	3%	¼ W
R6	100Ω	0.1%	¼ W
R7	100Ω	0.1%	¼ W
R8	3k	3%	¼ W
R9	9.1k	3%	¼ W
VR1	20kΩ		
VR2	100Ω		10 turn pot.
VR3	1k		10 turn pot.
OP1, OP2			LM741

Test Equipment:

Oscilloscope -Tektronix 7603
Pulse Generator (P.G.) -
Wavetek 187
Multimeter (MI, M2) -Fluke
80 12 Digital Multimeter
Operational amplifier (OPI, OP2)
outputs to Differential
Comparator- Tektronix 7 AI3
Current transformer (CTI) output to
Dual Trace Amplifier -
-Tektronix 7 A26 I

Test Procedure:

I) Switch in S, Use CTI to monitor I_D.
Adjust V_{DD} to obtain required I_D.
Ensure VG adjusted to provide
gate overdrive-
2) Set 7 Al3 differential Volts/ divto
I0 mV/div.
3) Adjust VR2 until differential voltage is zero.
4) Turn off V_E and V_G.
5) Place switch in R,
Adjust MI current with VR3 to
read 1.000 mA.
Read M2 voltage (200 m V range).
M2 reading = (R6 + VR2) x 1 mA,
Calculate VR2
Nominal sense ratio (r) = R6+ VR2/R2

Using Surface-Mount Devices

(HEXFET is a trademark of International Rectifier)

by W. Parrish

Summary

Surface-mount technology is gaining increasing acceptance over through-hole mounting. International Rectifier offers HEXFET® power MOSFETs, high voltage gate drivers, Schottky diodes, and ultra-fast recovery diodes in packages suitable for surface mounting. This application note gives details of these packages and their thermal characteristics, as well as handling and mounting details.

Introduction

The electronics industry is continually seeking ways to reduce the size and the cost of its products. Surface mounted components represent a major step in this direction. Surface mounting involves soldering parts onto the surface of the printed circuit board rather than inserting the pins through holes in the board and soldering on the underside. Surface-mount component packages are much smaller than those typically used in through-hole mounting, and the leads are short or folded under the package. The result is a much higher packing density — up to four times as many components can be mounted on a board — and more if components are mounted on both sides of the board. Other benefits to be derived from surface mounting include lower parasitic capacitances and inductances, higher reliability, fewer assembly-related faults, reduced production costs, and simplified handling of components.

To date, most progress in the development of surface-mount components has been concentrated on integrated circuits. However, with surface-mount technology gaining rapid acceptance in all sectors of the electronic industry, there is a growing demand for discrete semiconductor devices in surface-mount packages. International Rectifier has responded by producing a range of surface-mount packages for its product line.

Surface-Mount Packages

Table 1 lists International Rectifier's present range of surface-mount packages. More information about specific International Rectifier HEXFET power MOSFET surface-mount devices is available in the HEXFET Designer's Manual, HDM-1, Volume II. For suggested PC board pad sizes, see Figure 2. Several Hi-Rel/Mil devices are also available; for more information, contact IR's Hi-Rel/Mil Department.

Table 1. Surface-Mount Packages

Product	Package Type
HEXFET Power MOSFET	TO-243AA (SOT-89)
HEXFET Power MOSFET	TO-252AA (D-Pak)
HEXFET Power MOSFET	TO-220 with lead form
High Voltage Gate Drivers	LCC
Ultra-Fast Recovery Rectifier	D-64
Ultra-Fast Recovery Rectifier	TO-252AA (D-Pak)
Schottky Rectifier	D-64
Schottky Rectifier	TO-252AA (D-Pak)

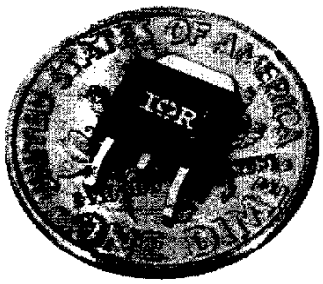


Figure 1. D-Pak Transistor Package

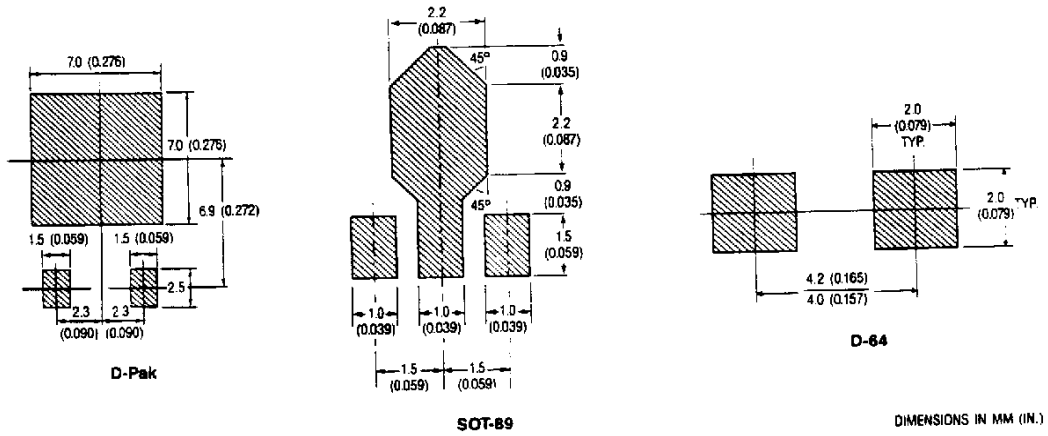


Figure 2. Suggested PC Board Pad Sizes

Thermal Data

As with any power semiconductor device, the current carrying capability is determined by the ability of the package to dissipate heat. The peak junction temperature can be calculated as follows:

$$T_j = T_a + P_t (R_{\theta JC} + R_{\theta CS} + R_{\theta SA})$$
$$= T_a + P_t \cdot R_{\theta JA}$$

where:

T_j = junction temperature
T_a = ambient temperature
P_t = total power dissipation in the device (conduction losses, switching losses, leakage losses, etc.)
$R_{\theta JC}$ = thermal resistance, junction-to-case
$R_{\theta CS}$ = thermal resistance, case-to-sink
$R_{\theta SA}$ = thermal resistance, sink-to-ambient
$R_{\theta JA}$ = thermal resistance, junction-to-ambient

Conversely, fixing the peak junction temperature permits the allowable power dissipation to be calculated.

Table 2 shows the thermal resistance values for the packages listed in Table 1.

In the case of surface mounted devices, the heatsink is usually the printed circuit board or ceramic substrate to which the device is soldered. The sink-to-ambient thermal impedance will depend on the board or substrate material, the pad area available for heat spreading, the proximity of other additional thermal loads on the board, and the velocity of air flow (in the case of forced cooling). Figure 3 shows how the thermal resistance of a three-inch square printed circuit board varies with pad area and air velocity. The data given in this graph should be used with caution, since local air flow can be modified by the shadowing effect of other components. Often, only prototype testing can prove the adequacy of a particular thermal design.

The heat sinking capacity of the board or substrate depends on the thermal conductivity of the board material. Table 3 lists the thermal conductivity of a variety of commonly used materials. The reduction in thermal resistance that can be obtained depends on the material, the thickness of the material, and on the effective area of the board, as well as the air velocity. These factors can interact in a non-linear manner.

Table 2. Thermal Resistance of Surface-Mount Packages

Package	$R_{\theta JC}$ (max)	$R_{\theta CS}$ (typical)	$R_{\theta SA}$	$R_{\theta JA}$ (max)
TO-243AA (SOT-89)	35	5	(Note 1)	110
TO-252AA (D-Pak)	(Note 2)	1.7	(Note 1)	110
TO-220AB with lead form	(Note 3)	1	(Note 1)	80
D-64	—	—	(Note 1)	160

Thermal resistance values are in K/W

Notes:
1. Depends on board material and area of board; see text.
2. 5 for HEX-1 die, 3 for HEX-2 die, 5 to 8 for diodes.
3. Between 1 and 3.5, depending on die size.

Table 3. Thermal Conductivity of Commonly Used Printed Circuit Board Material and Ceramic Substrate

Material	Thermal Conductivity (Watt-in./in.^{2}-°C)	% Increase Over FR-4/G-10
Glass Epoxy: FR-4/G-10	0.0072	—
Alumina Ceramic	0.45	52.5%
Aluminum Nitride	3.3	458%
Beryllia Ceramic*	5.2	722%

***Caution:** The dust from sawing or breaking Beryllia is highly toxic if inhaled.

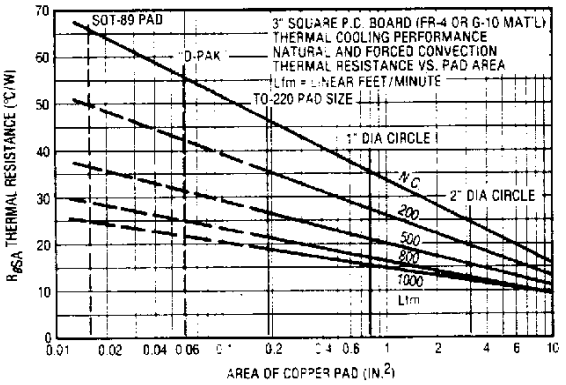


Figure 3. Thermal Resistance of 3-inch Square Printed Circuit Board

Handling

The SOT-89, D-Pak, and D-64 devices are all available for automated assembly using the tape and reel method of packaging. The tapes are available with devices in several different orientations, which affects the quantity on the reel. SOT-89 reels holds 1,000 pieces, independent of the device orientation. D-Pak reels hold either 2,000 or 3,000 pieces, depending on the device orientation. D-64 reels hold 1,800 pieces each.

The devices are held in the pockets in the tape with an adhesive-coated, polyester retainer film. The force required to peel this film from the tape increases with storage time as shown in Figure 4.

More information about tape and reel is available on each data sheet, in HDM-1, Volume II, or from the factory.

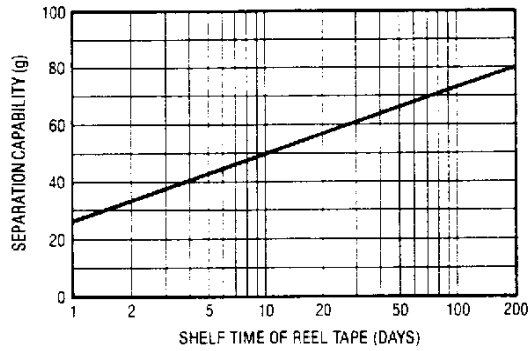


Figure 4. Separation Capability vs. Shelf Time of Reel Tape

Handling HEXFETs

The following measures should be taken to prevent damage to the HEXFETs from electrostatic discharge (ESD):

- Always store and transport HEXFETs in closed conductive containers.
- Remove HEXFETs from containers only after the operator and the container are grounded at a static-controlled work station.
- Personnel who handle HEXFETs should wear a static dissipative outer garment and should be grounded at all times.
- Floors should have a grounded static dissipative covering or be treated with a static dissipative compound.
- Tables should have a grounded static dissipative covering.
- Avoid insulating materials of any kind while handling HEXFETs, since these materials may acquire a static charge, which, if discharged through the HEXFET, could destroy it.
- Always use a grounded soldering iron to install or remove HEXFETs.
- Test HEXFETs only at a static-controlled work station.
- Use all of these protective measures simultaneously and in conjunction with trained personnel.

More detailed information on protection against ESD is available in Application Note AN-955.

Mounting and Soldering

All package types have pre-tinned leads to facilitate soldering. After placement on the board, the device is held in place either by a previously dispensed adhesive or by solder paste. Generally used methods of soldering are listed below.

- Wave soldering
- Vapor phase reflow
- Infra-red reflow
- Pulse-heat soldering tool
- Hand soldering

In all cases, good preparation of the board is essential to obtain the quality of solder joint necessary for good themal contact as well as good electrical contact. Oxide should be removed by a method appropriate to the degree of oxidation that has taken place, such as trichloroethane for light oxidation, an organic acid flux for medium oxidation, or ferric cholride solution for heavy oxidation.

Wave soldering. In its simplest form, wave soldering requires the following steps:

- Accurate dispensing of adhesive where the device is to be mounted.
- Accurate placement of the device on the solder pads and the adhesive (usually accomplished with a "pick-and-place" robot).
- Curing of the adhesive.
- Preheat, foam flux and wave solder.
- Cool and clean flux.

Vapor-phase reflow soldering. This process employs a solder paste to supply the flux and the solder to the solder pad. The paste also acts as an adhesive to hold the device in position while reflowing takes place.

The paste is typically 70% solder and 30% binder. The solder is typically 300 mesh size particles of 60-40 Pb-Sn alloy (occasionally 62-36-2 Pb-Sn-Ag). The binder contains activator (flux), solvent and thickener lubricator mix. The paste is placed on the pads by a silk screening process with a thickness of 8 to 10 mils.

The device is then placed on the prepared pad. Accurate placement is essential, although some alignment of the device with the pad will result when the solder melts due to the surface tension of the solder.

The solder paste is melted by passing the boards through a hot vapor. The solder is melted as the vapor condenses on the board and components. Two methods of vapor-phase reflow are popular. They include (1) the conveyor belt method, in which the boards are carried on a conveyor belt over boiling fluid; and (2) the dual vapor system, in which the boards travel vertically through zones of vapor of different temperatures.

Soldering is carried out in a furnace at a temperature of 230°C to 250°C, preferably in less than 20 seconds. Preheating time should be 120 seconds or longer. Whichever type of heating method is used, the object is to achieve the required time-temperature profile. Figure 5 shows the temperature profile required for belt furnace with tunnel heating. Figure 6 shows the temperature profile required for solder bath soldering with preheating.

Infra-red reflow. The preparatory steps to board heating are the same as those for the vapor-phase reflow method. In the infra-red process, the board is passed under infra-red radiators to achieve reflow of the solder. Care must be exercised not to overheat any large "black bodies" that may be mounted on the board.

Pulse-heat reflow. This method requires a special heat collet which directs the flow of a heated gas around the surface-mounted device and onto the terminals and the printed circuit board pads. The heating, reflowing and cooling cycles should be similar to those shown in Figure 5.

Hand soldering. Manual soldering should be avoided if possible, since the component can easily be dislocated and damaged during manual soldering operations. However, if repairs to a board are necessary, the following guidelines should be observed:

1. The soldering iron tip should not exceed 250°C
2. The reflow should be completed within three seconds. The iron tip should not be more than 1 mm (0.039 inch) in diameter. □

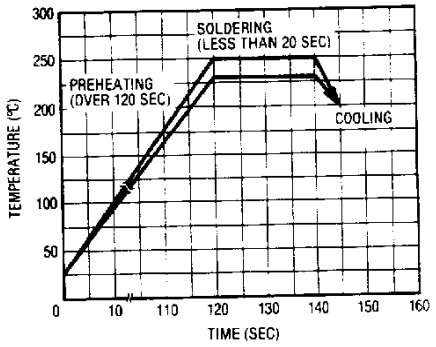


Figure 5. Temperature Time Profile for Two-Zone Reflow Soldering

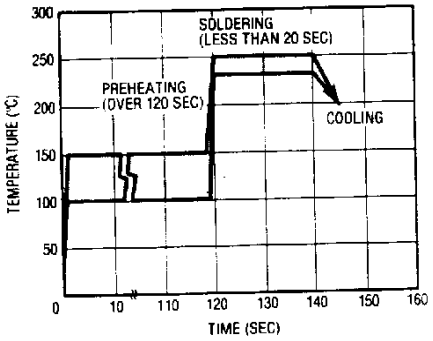


Figure 6. Temperature Time Profile for Solder Bath Soldering with Preheating

IR Application Note AN-955

TITLE:

Protecting IGBTs and MOSFETs from ESD

Notices:
(HEXFET is the trademark for International Rectifier Power MOSFETs)

Summary:



Most power MOSFET users are very familiar with this warning. The problem is that familiarity may breed contempt, especially if one has never destroyed a power MOSFET by improper handling. Statistically, it is unlikely that a particular MOSFET will be destroyed by Electrostatic-Discharge (ESD). However, when thousands of MOSFETs are handled, even a statistically small number of failures may be significant. In view of the fact that IR rejects less than 100 parts per million (ppm) at outgoing Q.A., it is evident that destroying 1 or 2 parts per 1,000 during incoming handling will have a significant impact on the "perceived" quality of the units.

Any effective ESD Control Program is very detailed and specific by nature. But its basic underlying concepts may be summarized by ten simple rules:

1. Always store and transport MOS-FETs in *closed* conductive containers.
2. Remove MOSFETs from containers only after grounding at a Static Control Work Station.
3. Personnel who handle power MOSFETs should wear a static dissipative outer garment and should be grounded at all times.
4. Floors should have a grounded static dissipative covering or treatment.

5. Tables should have a grounded static dissipative covering.
6. Avoid insulating materials of any kind.
7. Use anti-static materials in one-time applications only.
8. Always use a grounded soldering iron to install MOSFETs.
9. Test MOSFETs only at a static controlled work station.
10. Use all of these protective measures simultaneously and in conjunction withtrained personnel.

International Rectifier has an outstanding ESD control program in place in their HEXFETâ manufacturing facility. This Application Note will discuss how HEXFET users can implement and benefit from similar ESD control programs.

What is ESD?

ESD is the discharge of static electricity. Static electricity is an excess or deficiency of electrons on one surface with respect to another surface or to ground. A surface exhibiting an excess of electrons is negatively charged, and an electron deficient surface is positively charged. Static electricity is measured in terms of voltage (volts) and charge (coulombs).

When a static charge is present on an object, the molecules are electrically imbalanced. Electrostatic-Discharge (ESD) takes place when a re-establishment of equilibrium is attempted through the transfer of electrons between one object and another that is at a different voltage potential. When an ESD-sensitive device, such as a power MOSFET, becomes part of the discharge path, or is brought within the bounds of an electrostatic field, it can be permanently damaged.

Generating Static Electricity

The most common way of generating static electricity is triboelectrification. Rubbing two materials together will cause triboelectrification, as will bringing two materials together and then separating them. The magnitude of the charge is highly dependent upon the particular material's propensity toward giving up or taking on electrons.Dissimilar materials are particularly susceptible, especially if they have high surface resistivity.

Another way of placing a static charge on a body is by induction. Induction could be caused, for example, by placing a body in close proximity to a highly charged object or high-energy ESD.

ESD Failure of the Power MOSFET
Failure Mode

One of the biggest operating advantages of the power MOSFET can also be the cause of its demise when it comes to ESD ultra-high input resistance (typically > 4 x 109 ohms). The gate of the power MOSFET may be considered to be a low voltage (+ 20V for HEXFETs) low leakage capacitor. As can be seen in Figure 1, the capacitor plates are formed primarily by the silicon gate and source metallization. The capacitor dielectric is the silicon oxide gate insulation.

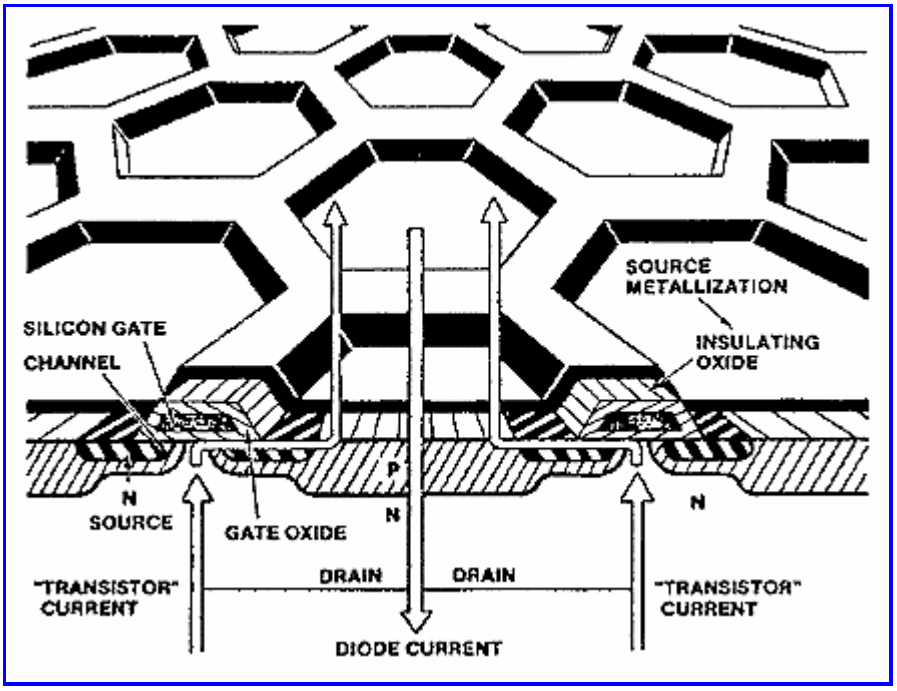


Figure 1. Basic HEXFET Structure

ESD destruction of the MOSFET occurs when the gate-to-source voltage is high enough to arc across the gate dielectric. This burns a microscopic hole in the gate oxide which permanently destroys the device. Like any capacitor, the gate of a power MOSFET must be supplied with a finite charge to reach a particular voltage. Since larger devices have greater capacitance they require more charge per volt and are therefore less susceptible to ESD than are smaller MOSFETs. Also, immediate failure usually will not occur until the gate-to-source voltage exceeds the rated maximum by two to three times.

A typical ESD destruction site can be seen in Figure 2a. This was caused by a human body model charged to 700 volts being discharged into the gate of the device. This photo was taken at a magnification of 5,000 with a scanning electron microscope after stripping the surface of the die down to polysilicon. The photo of Figure 2bshows that no damage was visible on the surface of the die prior to stripping. The actual failure site shown in Figure 2a is only about 8 microns in diameter. The electrical symptom of ESD failure is a low resistance or a zener effect between gate and source with less than ±20 volts applied.

The voltages required to induce ESD damage can be 1,000 volts or higher (depending upon chip size). This is due to the fact that the capacitance of the body carrying the charge tends to be much lower than the Ciss of the MOSFET, so that when the charge is transferred, the resulting voltage will be much lower than the original.

Electrostatic fields can also destroy the power MOSFET. The failure mode is ESD but the effect is caused by placing the unprotected gate of the FET in a Corona Discharge path. Corona Discharge is caused by a positively or negatively charged

surface discharging into small ionic molecules in the air (CO_2^+, H^+, O_2^-, OH^-).

Is ESD Really a Problem?

As previously mentioned, when dealing with small quantities of MOSFETs, ESD may not seem to be a problem. The results in this case may be occasional unexplained failures. When dealing with very large quantities, particularly when quality is of prime consideration, ESD can be a real problem.

The graph in Figure 3 gives a good graphical illustration of the magnitude of the problem and its solution. This graph was derived from data taken at an internal point of International Rectifier's manufacturing facility and does not represent the much lower AOQL levels. Between April 1982 and October 1983, gate-related failure dropped by nearly a factor of 7 at this inspection point as a direct result of the institution of ESD protective measures.

Materials and Methods for ESD Control
Direct Protection Method

In protecting any power MOSFET from ESD or any other excess gate voltage, the primary objective is to keep the gate-to-source voltage from exceeding the maximum specified value (±20 for HEXFETs). This is true both in and out of circuit.

Direct protection of the MOSFET could involve methods such as shorting the gate to the source, or applying zener protection gate-to-source. While effective for in-circuit or small quantity applications, the direct method is usually impractical in the manufacturing

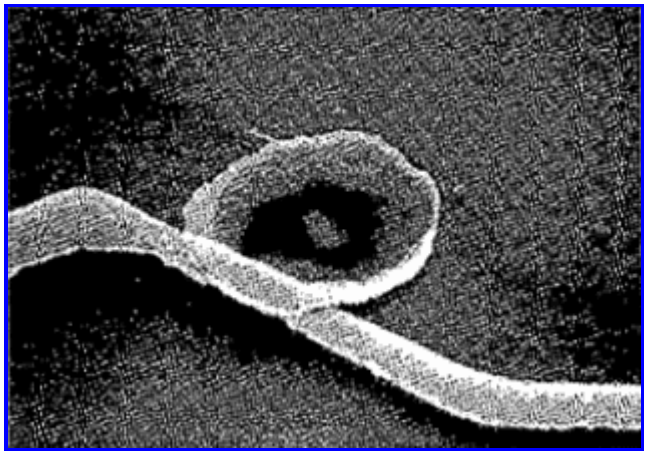


Figure 2a. Typical ESD Failure

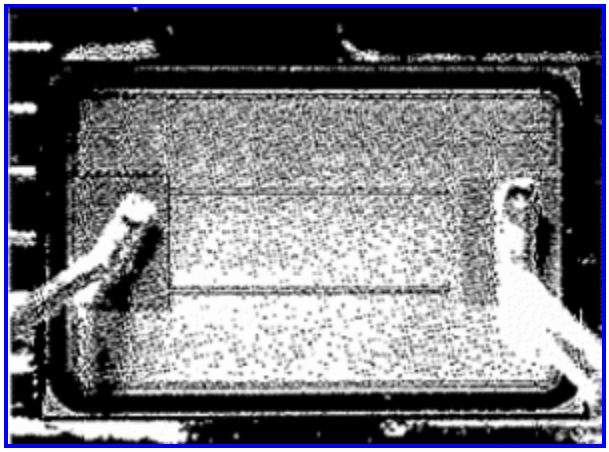


Figure 2b. ESD Damaged Device at Low Magnification before Stripping

environment because of the large volume of power MOSFETs involved. The basic concept of complete-static protection for the power MOSFETs is the prevention of static build-up where possible and the quick, reliable removal of existing charges.

Materials in the environment can either help or hinder static control. These may be placed into four categories of surface resistivity: Insulating (>1014 ohms/Sq.*), Anti-Static (109-1014 ohms/Sq.*), Static-Dissipative (105-109 ohms/Sq.*), and Conductive (Ideally, to protect the HEXFET, one should have only grounded conductive bodies in the facility. Additionally, all personnel involved in the manufacturing process should be hard grounded. Unfortunately the humans involved in the manufacturing process would then become vulnerable to electrocution by faulty electrical equipment. Also, when traveling long distances, it can be difficult to maintain a ground connection. Consequently, protective materials and methods must be chosen based on the situation.

Insulating Material

Because of their propensity for storing static charges and the difficulty with discharging them, it is imperative to keep objects made of insulating materials away from power MOSFETs and out of the environment entirely, if possible. Since electric current cannot flow through an insulator, electrical connections from an insulator to ground are useless in controlling static charges.

Insulating materials include: polyethylene (found in regular plastic bags), polystyrene (found in Styrofoam cups and packing "peanuts"), Mylar, hard rubber, vinyl, rnica ceramics, most other plastic, and some organic materials.

When plastic products must be used in a power MOSFET handling facility, use only items impregnated with a conductive material and/or treated with anti-static compounds.

Anti-Static Material

Anti-static material is resistant to the generation of triboelectric charges, but does

not provide a shield from electric fields. Corona Discharge will pass right through an anti-static enclosure, possibly destroying any MOSFETs which are inside. Because of its high surface resistivity, grounding anti-static material is not very effective for removing a charge.

Some plastic insulators can be treated with anti-static agents which chemically reduce their susceptibility to triboelectrification and lower their surface resistivity. Most anti-static agents require high relative humidity (RH) to be effective. Therefore, the RH of facilities where power MOSFETs are handled should be kept above 40%. Also, anti-static agents tend to wear off or wear out after a period of time, and most of them use reactive ionic chemicals which can be corrosive to metal. Anti-static plastics should be limited to short-term use in one-time only situations, such as Dl P and TO-3 tubes and packing materials for shipping.

** The size of the square does not effect the surface resistivity.*

Mounting Guidelines for the SUPER-220 (AN-951)

by Andrew Sawle and Arthur Woodworth

The impressive gains in power density born from the development of the 'SUPER' type power packages, *i.e. the SUPER-247*, has lead to a similar development of the TO-220 package. The removal of the hole and incorporation of new innovative ideas has lead to the SUPER-220. This new power package can now house areas of silicon that previously would have called for the use of a TO-247. These increases in power density allow designers to realise cost savings through reducing the number of paralleled devices required for a desired current rating and also reducing the areas of costly circuit board needed for their designs. Hence reductions in both the size and cost of designs are possible through the use of the SUPER-220 package.

However, increasing the power density within a design will mean that the designer needs to make careful consideration of the thermal aspects of the design aswell as the electrical. As with the SUPER-247 (see Application Note AN997) the SUPER-220 does not have a screw hole to facilitate bolting to a heatsink and therefore the package will need to be clip mounted. Clip mounting facilitates mass production techniques and good thermal performance but the latter will only be the case if the designer has made careful use of the thermal options available.

This Application Note is intended to outline the thermal options available to designers with regard to interface materials, clip types and the contact forces required to give good thermal contact and the performance that they might expect from each. The following topics will be covered:

- A brief revision of thermal resistance and its effects on system perfomance.
- Clip mounting of SUPER-220 devices to heatsinks, suppliers and interface materials.

Thermal Resistance and its Effects on System Performance

The thermal resistance ($Rth_{(junction\text{-}ambient)}$) of a system (system = package through to heatsink) is made up from a number of component parts as shown in Figure 1.1 below.

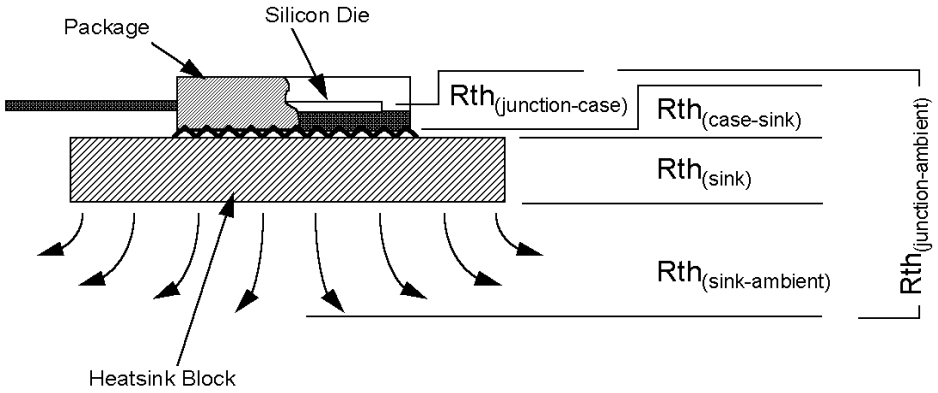


Figure 1.1 - Build-up of Thermal Resistance in a System

The designer of a system has varying amounts of influence over the component parts of the overall thermal resistance of his design:

- **$Rth_{(junction\text{-}case)}$** - this has been determined during the design and manufacture of the product. The system designer has no direct influence.
- **$Rth_{(case\text{-}sink)}$ (or Contact Thermal Resistance)** - determined by the size and quality of the contact areas between the package and the sink, the use of intermediate materials and the contact pressure. Hence, the system designer can have a large influence over this parameter.
- **$Rth_{(sink)}$ and $Rth_{(sink\text{-}ambient)}$** - determined by heatsink design, *i.e. material and shape.* The selection of a heatsink is done by trading off performance and cost requirements.

The thermal resistance of a system will determine the amount of power that can be dissipated by a device without exceeding the maximum junction temperature. Operating at temperatures above $T_{j(max)}$ will reduce the reliability of the device. Therefore by optimising the thermal performance of a system, a greater amount of power can be dissipated by each device thereby minimising the number of devices that need to be used.

Clip Mounting of the SUPER-220 Package

The removal of the hole from the TO-220 package to facilitate the greater area of silicon in the SUPER-220 package means that the new package can **NOT** be bolted to a heatsink. However the package lends itself to clip mounting, a technology that is quickly becoming popular as it holds a number of advantages over the older 'bolting' technology:

- Clips are quick to apply and therefore lend themselves to mass production assembly techniques.
- Clips maintain a constant assembly force even if the intermediate material deteriorates, unlike bolt assembly where the force diminishes.

➲ Clips impart their force on the central part of the package over the silicon, distributing the pressure evenly which creates a good thermal contact with the heatsink. Bolts however, impart the force at one end of the package and the pressure is uneven, see Figure 1.2.

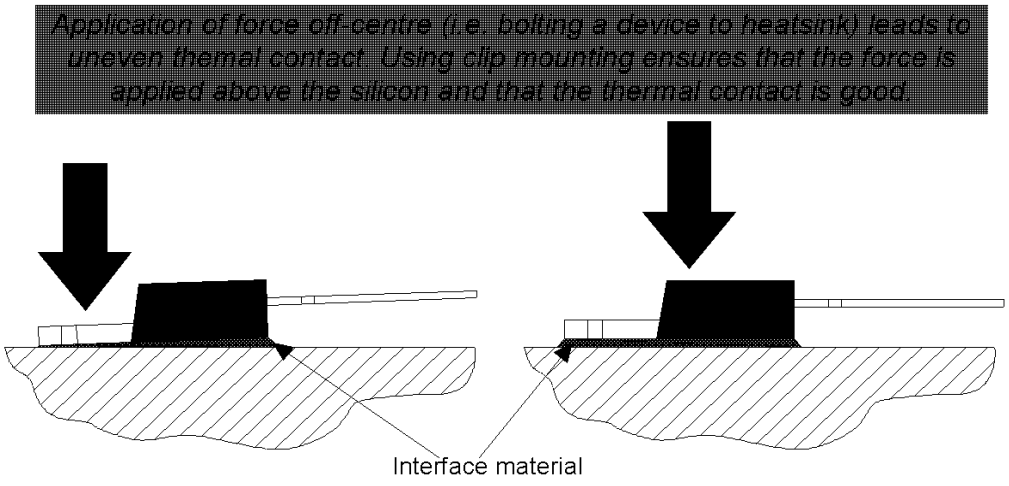


Figure 1.2 - Position of Force Application

The contact force and the way in which it is applied is therefore very important to the thermal performance of a system.

Why and How Does Contact Force Affect Thermal Resistance?

Package cases and heatsink surfaces are never perfectly flat. Hence contact between the two will only occur at several points allowing an air gap between the surfaces (as illustrated in Figure 1.3). Since air is a very good thermal insulator this means that the contact thermal resistance is much greater than it would be if the two surfaces were in perfect contact (no air gap). However, as the contact force (pushing the two surfaces together) increases then so will the number of points at which the two surfaces contact one another and the air-gap will be reduced, in turn reducing the contact thermal resistance.

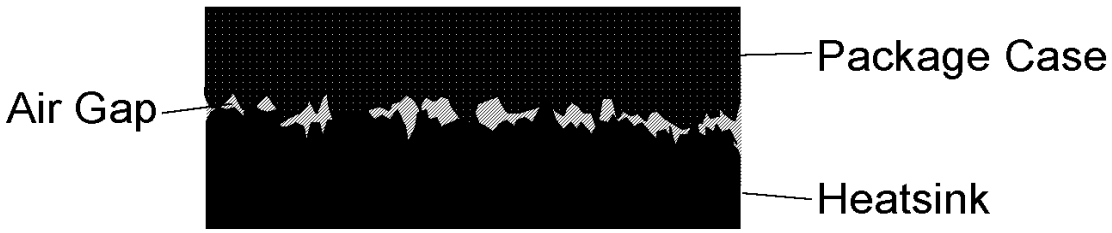


Figure 1.3 - Diagram Showing the Effect (Under High Magnification) When Two Non-perfect Surfaces Meet.

What is the minimum contact force that should be applied to gain good thermal contact

The minimum force required for a good thermal contact will vary from package to package as it will depend on the surface finish, flatness of contact surface and area of contact. Contact thermal resistance reduces with increased contact force but the relationship is non-linear. In essence, diminishing returns in reduced thermal resistance are seen for increases in force. This relationship for the SUPER-220 on a heatsink with NO interface materials, *i.e. 'dry' conditions*, is shown in Figure 1.4. A minimum contact force of 20N is recommended.

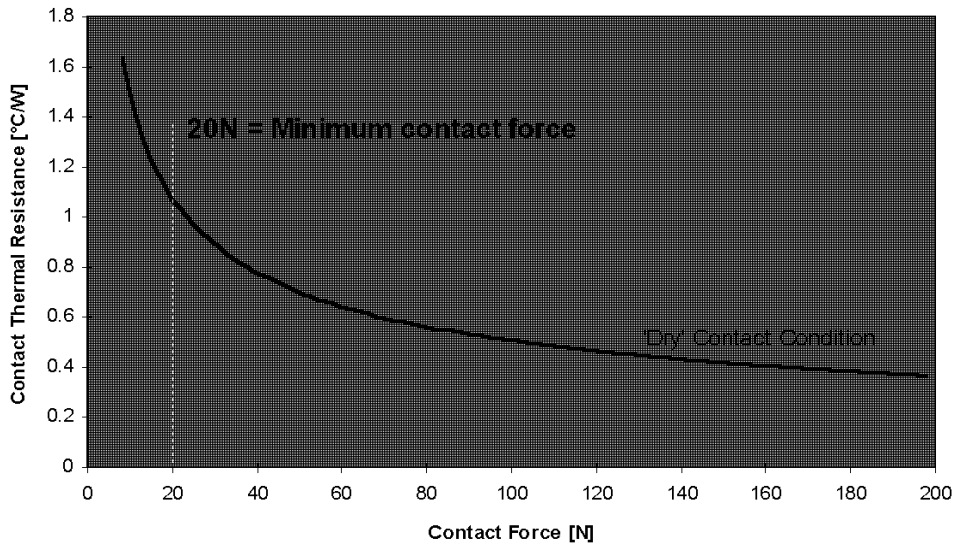


Figure 1.4 - Minimum Contact Force

Maximum Contact Force

The minimum contact force of 20N mentioned above is purely that, the MINIMUM force. Any force applied above that figure will still show gains in reduced contact thermal resistance until the maximum force that the package can withstand before the device characteristics are altered or the package is destroyed. This maximum limit figure has been measured to be 200N TYP. However, these gains are not free, for in general terms a greater contact force means a larger, more expensive clamping system. A contact force should therefore be chosen that optimises both the thermal and the cost requirements of the system.

Contact Conditions

As mentioned previously, the contact conditions between the package and the heatsink will affect the contact thermal resistance. Contact conditions encompass a number of areas including: surface roughness, surface cleanliness, paint finishes and intermediate materials. The surface roughness of the heatsinking material should be no greater than 0.02mm over the area where the device is to be mounted. Surface cleanliness during assembly of package and heatsink is imperative, even if a thermal grease or other material is subsequently added. Unclean surfaces can be held apart by dirt or grease thus increasing the thermal resistance. However, normal paint finishes (up to 50 μm thick) have been shown to have little effect on thermal resistance, this therefore leaves intermediate materials as an area for discussion.

Interface Materials

Figure 1.4 above shows the force vs Rth relationship for 'dry' conditions, however, the use of no interface materials in an assembly is rare and usually one of two conditions is required:

- An interface material to improve the thermal performace of the contact area between device and heatsink.
- An interface material providing electrical isolation between the device and heatsink whilst minimising the adverse effects that it will have on the the thermal performance of the contact area. Isolation is usually required where more than one device is going to share the same heatsink.

Heatsink compound

A number of different companies offer heatsinking compound, these usually consist of silicon grease loaded with some electrically insulating, good thermally conducting material such as alumina. Thinly applied, these compounds are advantageous as they fill the air gaps and do not further increase the distances between the surfaces. Thickly applied they can hold the two surfaces apart and increase the contact thermal resistance. The following graph displayed in Figure 1.5 shows the contact thermal resistance for 'dry' conditions (no compound) and the thermal resistance using compound, both are plotted against contact force.

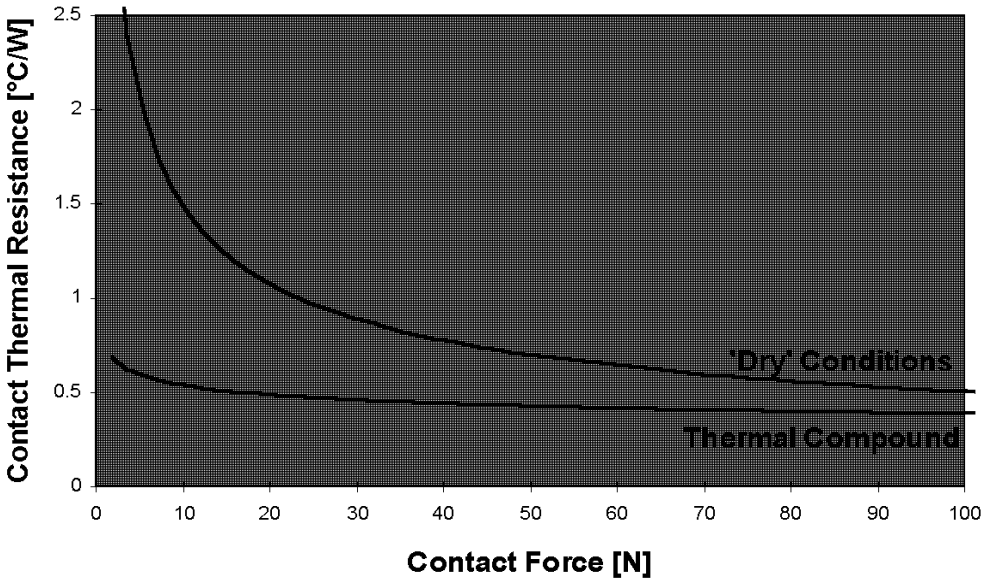


Figure 1.5 - Contact Thermal Resistance for 'Dry' and Compound Conditions, Plotted Against Contact Force

Interface Pads

The metal heatspreader on the back of the SUPER-220 package is non-electrically isolated from the pinouts of the device within, *i.e. the case is the drain contact for a MOSFET.* Hence in cases where devices are not electrically paralleled but share the same heatsink, it is necessary to insert an electrically isolating material between the package and the heatsink block. The isolator usually takes the form of a pad and many companies offer a range of pad material types and sizes dependant on requirements.

The pad obviously has a direct and detremental effect on the contact resistance as insertion adds an extra resistance into the build-up. Again, the contact thermal resistance is dependant on contact pressure. The following graph, shown in Figure 1.6, illustrates the higher thermal resistance when using an isolator pad. The isolator used for the line plot was a typical silicone loaded pad. Therefore, it should be noted that when electrically isolating a device from a heatsink the thermal resistance of the system will increase.

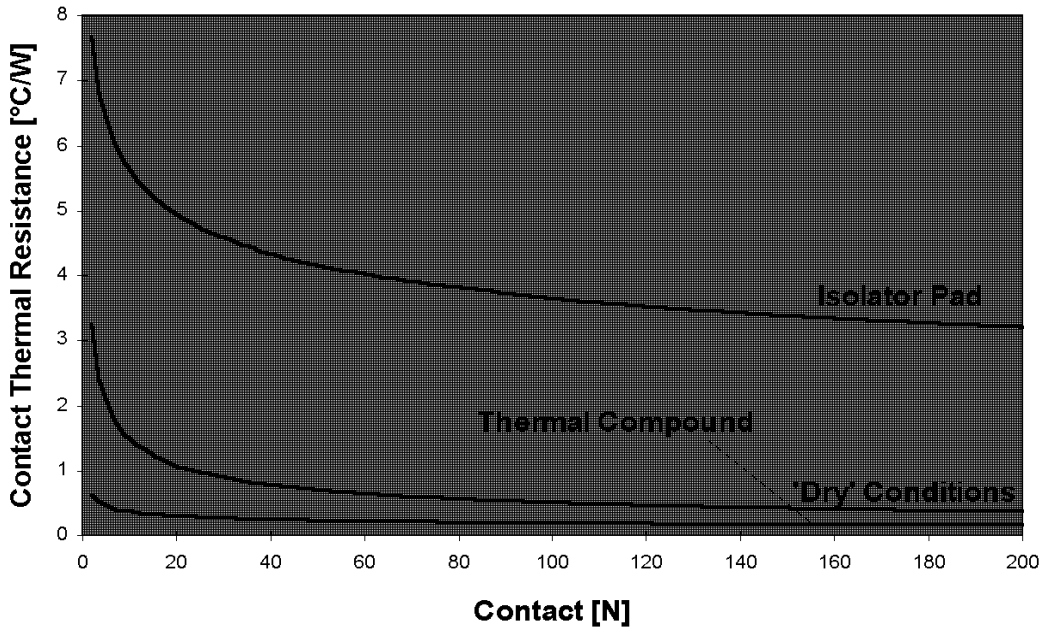


Figure 1.6 - Contact Thermal Resistance Plotted Against Contact Force

Phase Change Materials

One of the problems that interface pads have is that the forces required for good thermal contact are very high. This is because it is difficult to gain the amount of pad deformation necessary to fill the air-gaps in the heatspreader/pad and pad/heatsink interfaces. One of the solutions being offered by a number of suppliers is that of PHASE-CHANGE materials.

Phase change materials are a solid in nature until raised above a certain temperature (~50-65°C) at which point they become a viscous fluid, this change from solid to viscous occurs every time the temperature goes to this level. This fluidity means that with an adequate contact force the air-gaps can easily be filled and good thermal contact can be made. This good contact is maintained once the temperature is reduced as the material solidifies in place, filling the gaps.

The following chart in Figure 1.7 shows the contact thermal resistance using a typical phase-change isolating pad and a non-isolating pad.

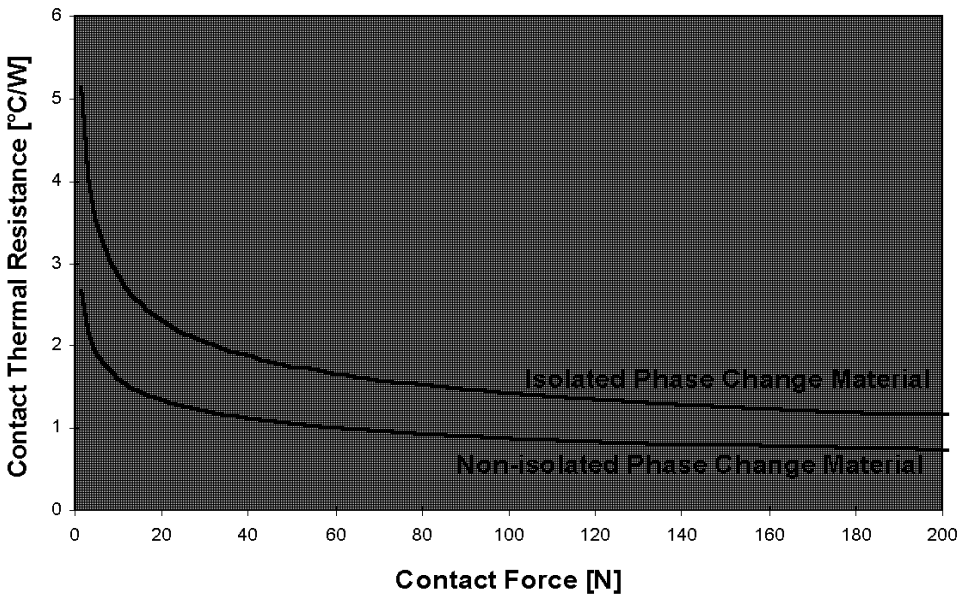


Figure 1.7 - Contact Thermal Resistance for Isolated and Non-isolated Phase Change Materials

It can be seen that phase change materials can offer lower contact thermal resistances when isolation is required over regular isolation pads. Two current manufacturers/suppliers of phase change materials are **Berquist** and **Orcus Inc**.

Heatsinks and Clips

A range of heatsinks and clips have been developed by a number of suppliers for the SUPER-220 package type. A number of these clip types are shown in the following diagrams. However, the clips shown are only a small selection and by no means encompass all available types and solutions.

Saddle Clips

An example of a SUPER-220 mounted to a heatsink using a saddle clip is shown in Figure 1.8.

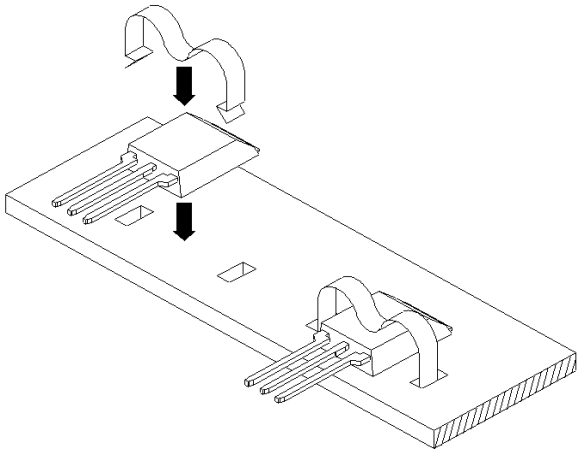


Figure 1.8 - SUPER-220 Mounted to Heatsink Using Saddle Clip

When using saddle clip type solutions, the heatsink materials are thin in cross-section, typically less than 5mm in thickness. The clips push into holes cut into heatsink material and lock against the back face of the heatsink. These clips produce contact forces in the range 15-50N.

'U' Clips

An example of a heatsink assembly utilising a 'U' clip is shown in Figure 1.9.

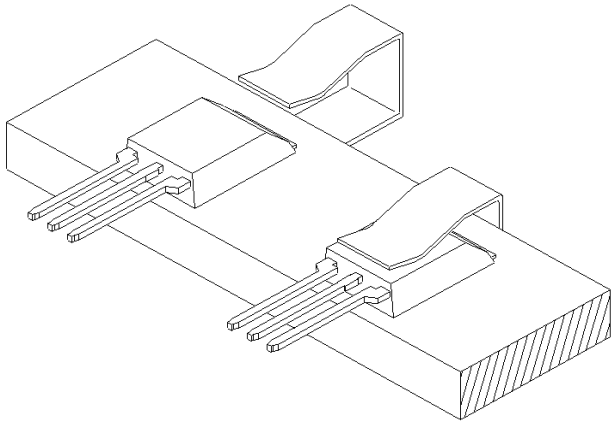


Figure 1.9 - SUPER-220 and a 'U' Clip Assembly

This clip type clamps the device and the heatsink material together. Variations on this clip type allow devices to be clamped to the front and back of the heatsink block using the same clip. 'U' clips can offer contact forces in the range 15-50N.

Extrusion Mounted Clips

There are a number of proprietary clip solutions offered where the clip is anchored in a feature in an extruded heatsink. One such solution is to use rails on extruded sinks for clip anchorage. This method is shown in Figure 1.10.

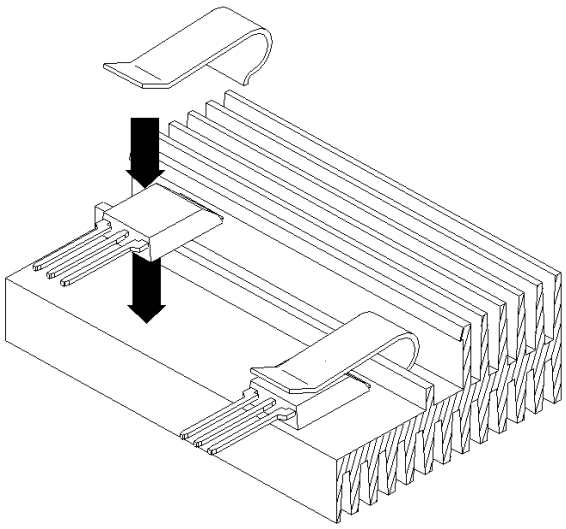


Figure 1.10 - Extrusion Mounted Clip (Rail Anchorage)

Clips on extruded sinks can offer contact forces in the range 25-50N

Typical Clip Solution Suppliers

Redpoint Thermalloy
Cheney Manor,
Swindon,
Wiltshire. SN2 2QN
England

Thermalloy, Inc.
2021 W. Valley View Ln.,
Dallas, TX 75234
USA

Avvid Thermal Technologies
Corporate Headquarters,
One Kool Path,
Laconia,
New Hampshire, USA

Austerlitz Electronic gmbh
Ludwig Feuerbach-Straße 38, 90961
Nüenburg,
Postfach 1048, GERMANY

Current Ratings of Power Semiconductors

Topics Covered:

What is a current rating?
Current ratings for power semiconductors
Continuous current ratings
Current ratings under duty cycle conditions
Transient thermal impedance
Peak Current Ratings of Power Semiconductors
RMS values of common waveforms

1. WHAT IS A CURRENT RATING?

The current rating of an electrical device, be that a circuit breaker or a motor or a transformer, is the current at which the temperature within the electrical device reaches a value that may impair the reliability or functionality of the device itself. The manufacturer knows the temperature limits of the materials used in the device, but he does not know the temperature of the ambient in which the device will be used. So he makes an assumption on this temperature. This has two important consequences:

1. **A current rating is meaningless without the rated temperature**
2. **The temperature at wich the rating applies may, or may not be related to actual operating conditions.** If it is, the current rating can be used as **an indication** of the current capability of that device in a real applications. If the device is rated at a temperature that is not encountered in a typical operating environment, e.g. 25ºC, **it cannot be trusted to provide an indication of actual device capability in an application.** It can only be used to compare the ratings of similar devices rated at the same temperature.

The rating of electrical devices like motors and circuit breakers are dictated by various agreements and regulations. The ratings of many other devices, like transformers, resistors and semiconductors are specified in their data sheets. As a result, the user must do, *at a minimum,* a verification that the device is capable of operating:

a) at the maximum current
b) at the maximum ambient temperature
c) without exceeding its maximum temperature

2. CURRENT RATINGS FOR POWER SEMICONDUCTORS

Like any other electrical device, power semiconductors must be operated within their maximum temperature. Since the vast majority of power semiconductors operate at large power densities, they need to be heatsunk. It is the task of the designer to identify the heatsink, or other cooling method, that fulfills the requirements a, b and c of the previous section. This task is normally referred to as “thermal design”.

Power semiconductors have, however, some additional limitations normally associated with their capability of handling high voltages and high currents at the same time, under static or dynamic conditions. These limitations are peculiar to the specific type of semiconductor, e.g. SOA for transistors, dv/dt, di/dt and t_q for tyristors, t_{rr} for diodes. Information on these limitations are normally contained in publications that are specific to the particular device.

Bipolar transistors have one additional limitation that is not common to other power semiconductors: gain. To operate a bipolar transistor at its headlined “rated” continuous current would require an inconveniently large amount of drive current, and the saturation voltage and switching times would be hard to live with in a practical design.

Other power semiconductors are not limited by gain. IGBT for motor drive applications are, by design, limited in gain to current levels much beyond normal operating conditions to reduce the current under short-circuit conditions.

3. CONTINUOUS CURRENT RATINGS

The continuous rating of a power semiconductor is based is *heat removal when conducting a fixed amount of current.* This is determined by the fundamental equation for temperature rise (see INT-936), with no switching losses present. Rated I_D, for a MOSFET is therefore:

$$I_D = \sqrt{\frac{T_{JMAX} - T_C}{R_{DS(on)}\, R_{th(JC)}}}$$

where $R_{DS(on)}$ is the limiting value of the on-resistance *at rated* $T_{(Jmax)}$ *, at the appropriate value of* I_D. R_{thJC} is the maximum value of internal junction-to-case thermal resistance, and Tc is the case temperature.

Similarly, the continuous current rating of a diode, or a thyristor, or an IGBT is calculated from the basic equation of temperature rise. The power dissipation is calculated from voltage drop and continuous current.

Except for water-cooled sinks, it is very difficult to keep the case temperature of a power semiconductor at less than 90º. Thus, the usable *continuous direct* current of a power device for most practical is whatever is applicable to a case temperature of 90 to 110° C. This allows a sufficient differential between case and ambient temperature for the heat dissipator to handle the heat transfer.

The “headlined” continuous current rating shown on the data sheets of most power transistors is usually larger than the above practically usable level of *continuous* drain current. This is because the case temperature adopted by the industry, to which the “headlined” continuous I_D rating applies, is 25°C.

Figure 1 shows typical heatsinks for TO-3 and TO-220 packaged HEXFET®s that allow them to operate in a 40°C ambient at a *continuous direct* drain current that is 60 to 70% of the rated continuous drain current at Tc = 25°C; the corresponding *steady* case temperature is about 100°C.

The continuous current rating of power transistors is, however, of little direct use to the designer, other than as a benchmark, for the following three reasons:

1. Power transistors are normally operated in switchmode, with duty cycles considerably less than l00%, and what is really of interest is the current-carrying capability of the device under the actual “switched” operating conditions.

2. When operated in switchmode, power transistors have switching losses, that have to be calculated and added to the conduction losses, as indicated in INT-936.

3. The selection of the power device may be dictated by surge requirements that make the continuous current rating irrelevant.

And, if this were not enough, advances in the low-voltage MOSFET technology have reduced conduction losses to the point that the package has become the limiting factor in their continuous current rating. This is explained in INTDT93-4

4. SWITCHING “DUTY CYCLE” RATINGS

The basic thermal equation of INT-936 determines the basic rating of a “thermal system” in a practical application. This equation can be used to determine how much power can be dissipated by a (known) thermal system or the junction temperature for a given set of electrical operating conditions (power dissipation). Since the power entered in that equation is the “average” power, it remains valid as long as the frequency of operation is high with respect to the thermal inertia of the system. When the frequency is very low (tens of Hz), the transient thermal response curve is used, as described below in Section 5.

The power dissipation is normally divided in conduction and switching. Conduction losses in a power MOSFET, being resistive in nature, can be calculated as $(I_{RMS})^2$ x R. The RMS content of waveforms of different shape can be found in the Appendix. Switching losses can be calculated from the switching waveforms, from the gate charge or from analytical methods. Conduction and switching losses for IGBTs are more complex, as explained in INT-990.

5. JUNCTION TEMPERATURE UNDER PULSED CONDITIONS

Under surge conditions the junction temperature rises exponentially, according to its thermal inertia. Rather than using the thermal resistance, that is appropriate for steady state operation, we use the Transient Thermal Impedance (or, more correctly, Thermal Response Curve), as the one shown in Figure 2. For a surge of given duration (x axis), this curve gives a thermal response factor (y axis). The peak junction temperature due to the surge condition can be calculated as indicated in the figure itself. The power dissipation is normally calculated from the voltage and current across the device during the surge.

This curve is also useful for determining the peak junction temperature for power or pulses with a very low repetition rate, when the method described in the previous section is not applicable The reason for this is illustrated by the waveforms in Figures 3(a) and 3(b). Both sets of waveforms are for the same power dissipation and duty cycle, but for different operating frequencies. The cycle-by-cycle fluctuations of junction temperature at 20Hz (Figure 3a) are clearly greater than at 200Hz (Figure 3b). As frequency increases, thermal inertia of the junction "irons out" instantaneous temperature fluctuations, and the junction responds more to average, rather than peak power dissipation. At frequencies above a few kHz and duty cycles above 20% or so, cycle-by-cycle temperature fluctuations become small, and peak junction temperature rise becomes equal to the average power dissipation multiplied by the DC junction-to-case thermal resistance, within one or two percent.

For pulses with low repetition rate the remaining curves in Figure 2 show effective thermal impedance at different duty cycles. These curves are approximately related to the single pulse curve, by the following relationship:

Effective normalized thermal impedance = D + (l - D) x (transient thermal impedance for single pulse of duration t).

The thermal impedance, when multiplied by the power dissipation *during the conduction period t* (i.e., the power *within* the conduction pulse itself, *not* the power averaged over the whole cycle), gives the value of the repetitive peak junction-to-case temperature rise.

To determine the absolute value of the peak junction temperature, it is, of course, necessary to know the case temperature T_C under steady-state operating conditions. Because of thermal inertia, the heatsink responds only to average power dissipation (except at extremely low frequencies which generally will not be of practical interest). T_C is therefore given by:

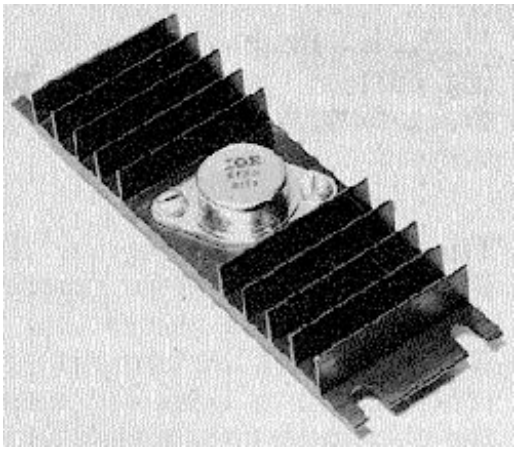
$T_C = T_A + (R_{thC\text{-}S} + R_{thS\text{-}A})\, P_{AV}$

where:

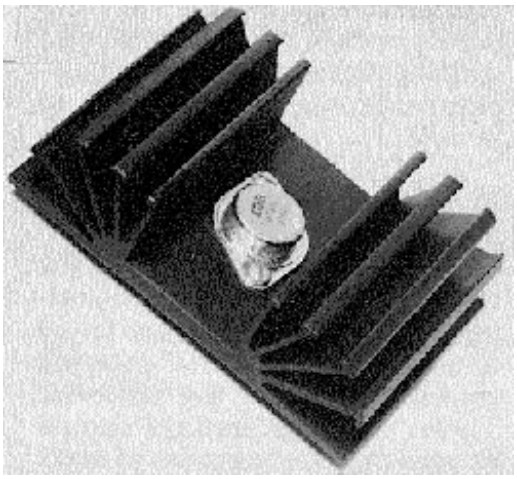
T_A = ambient temperature
$R_{thC\text{-}S}$ = case-to-sink thermal resistance
$R_{thS\text{-}A}$ = sink-to-ambient thermal resistance
P_{AV} = average power dissipation

also,

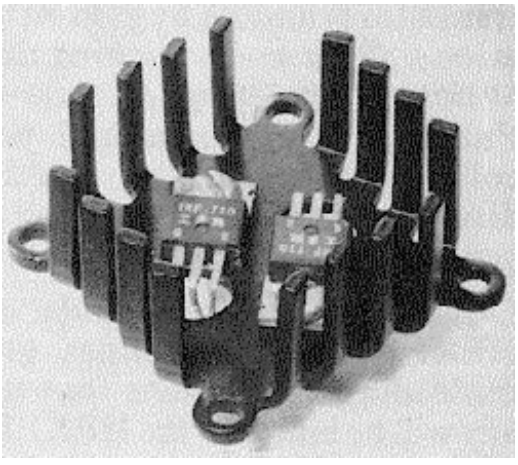
P_{AV} = peak power x duty cycle for rectangular pulses of power



(a) Type 621-A heatsink give 4A continuous rating for IRF331 with 5 CFM airflow in 40^{0}C ambient.



(b) Type 641-A heatsink gives 3.5A continuous rating for IRF331 with natural convection cooling in 40^{0}C ambient.



(c) Type 689-75 e4 heatsink give 1A continuous rating for IRF710 with natural convection cooling in 40^{0}C ambient.

Figure 1. Typical Heatsinks for HEXFETs (Heatsink by Wakefield)

The transient thermal response curve ***assumes constant case temperature***. This is generally valid for pulses shorter than 10ms. For longer surges the case temperature starts to rise and the results are of questionable accuracy. For operation in free air, case temperature starts to rise within few ms and this curve does not provide any useful information. More sophisticated analytical methods that take the entire thermal system into account are normally used to calculate temperature rise under these conditions.

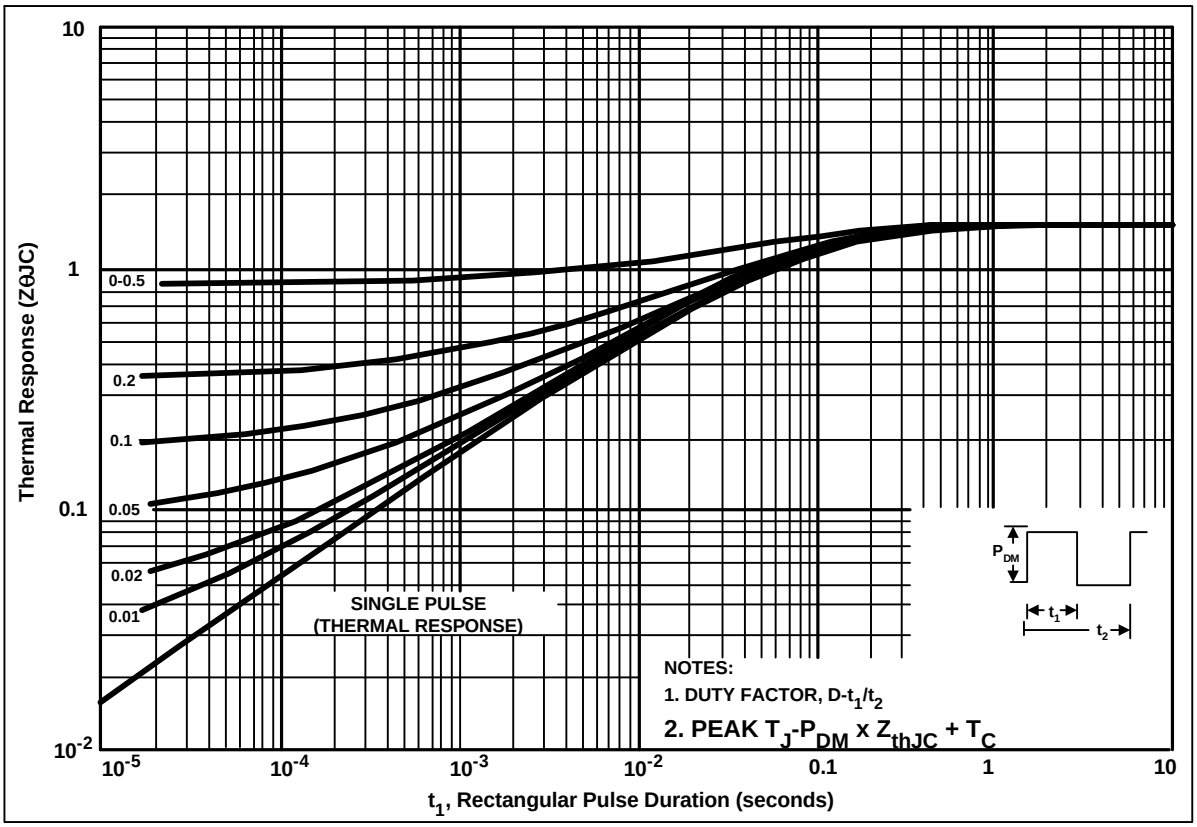


Figure 2. Transient Thermal Impedance Curves for IRF530 HEXFET

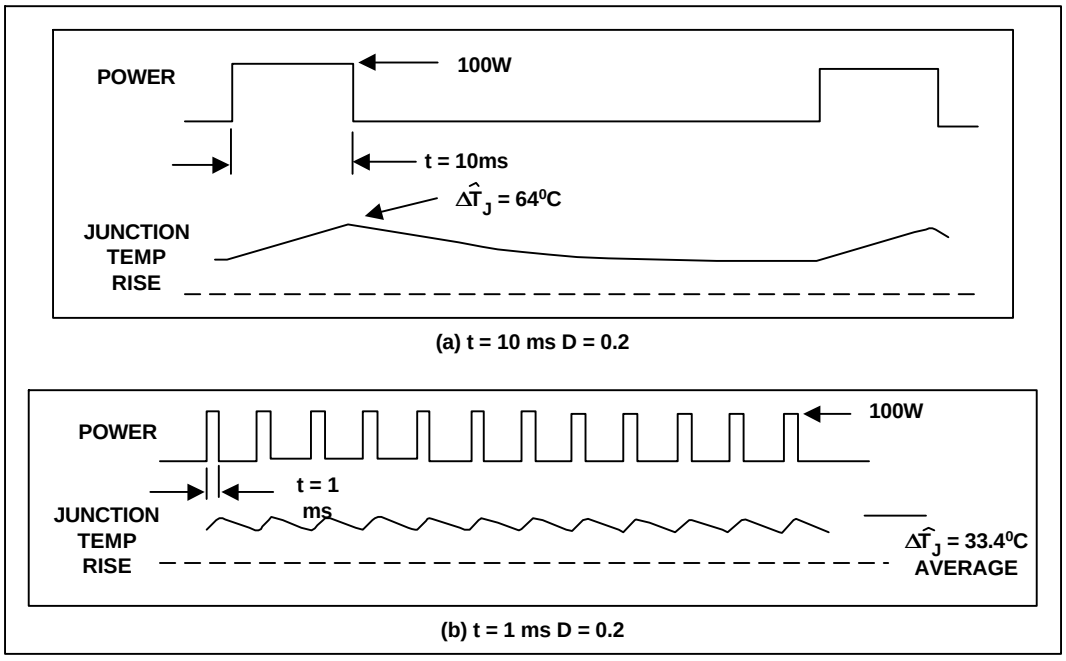


Figure 3. Waveforms of Power and Junction Temperature for Repetitive Operation, showing that Peak Junction Temperature is function of Operating Frequency. IRF330

6. PEAK CURRENT RATINGS

IGBTs and MOSFETs are able to carry peak current well in excess of their continuous current rating, provided that the rated junction temperature is not exceeded. There is, however, an upper limit on the permissible current, defined by the rated peak current. Most devices have a peak rating, that is several times their continuous rating at Tc =25°C.

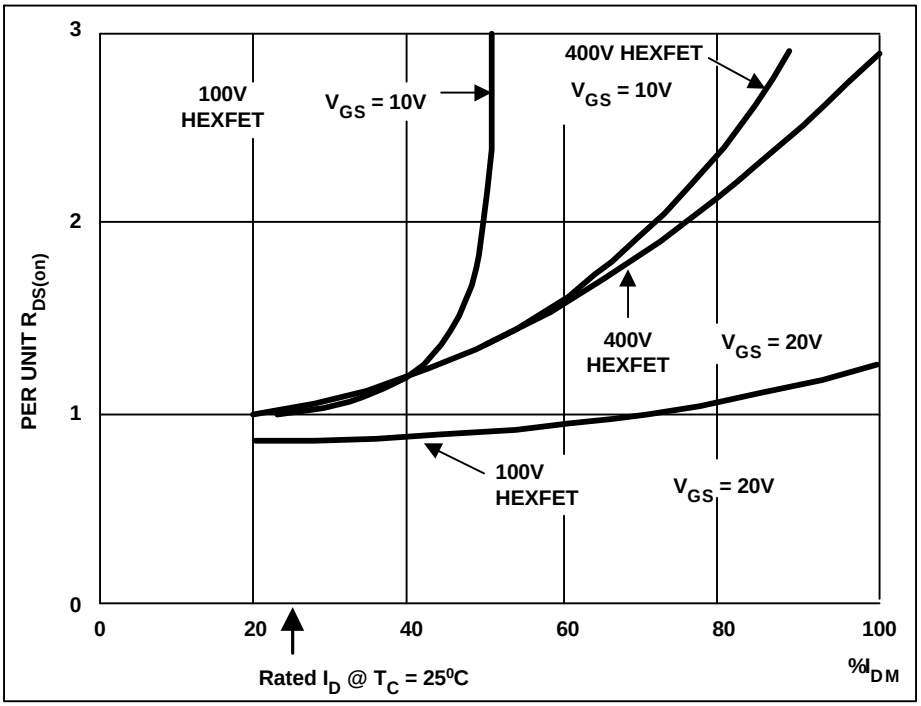


Figure 4. Typical Variation of On-Resistance with Drain Current.

Power transistors are fundamentally "linear" devices, as opposed to "latching" devices. As current increases, the point eventually is reached at which they go into "linear" operation and start to act, in effect, as a current limiter. This point depends upon the drive voltage applied to the gate, the safe limit of which is determined by the thickness of the oxide that insulates the gate from the body of the device. Peak ratings of power devices are normally achievable with an applied gate voltage that is equal to the maximum permissible gate voltage of 20V. They are repetitive ratings, as long as the junction temperature is kept within the rated T_{Jmax}. Peak junction temperature can be calculated from the thermal impedance data for the device, as indicated above.

It should be pointed out that the on-resistance of any MOSFET does increase as current increases. As shown in Figure 4, the on-resistance of a 100V rated HEXFET® at its rated I_{DM} with 20V applied to the gate is typically 1.4 x the value at the rated I_D; the corresponding multiplier for a 400V rated HEXFET® is 2.9. This increase of on-resistance must, of course, be taken into account when making thermal calculations and designing for use of the I_{DM} rating.

APPENDIX

Determining the RMS Value of I_D Waveforms

To accurately determine the conduction losses in a MOSFET, the RMS value for I_D must be known. The current waveforms are rarely simple sinusoids or rectangles, and this can pose some problems in determing the value for I_{RMS}**.** The following equations and procedure can be used to determine I_{RMS} for any waveform that can be broken up into segments for which the RMS value can be calculated individually.

The RMS value of any waveform is defined as $I_{RMS} = \sqrt{\frac{\int_0^t I^2(t)dt}{T}}$ (1)

Figure A-1 shows several simple waveforms and the derivation for I_{RMS} using equation (1).

If the actual waveform can be approximated satisfactorily by combining the waveforms in Figure A-1, then the RMS value of the waveform can be calculated from: $I_{RMS} = \sqrt{I^2_{RMS(1)} + I^2_{RMS(2)} + \cdots + I^2_{RMS(N)}}$ (2)

This is true to the extent that no two waveforms are different from zero at the same time.
In some applications such as switching regulators, it is possible for the designer to control the wave shape with topology or magnetic design. This can be very beneficial in reducing the value for I_{RMS} in the switch for a given value of average current.

EFFECT OF WAVEFORM SHAPE ON RMS VALUE

In a swith mode converter, the current waveforms through the inductors, transformer windings rectifiers and switches will appear as shown in Figure A-1, ranging from a triangle to a rectangle depending on the value of the averaging inductor and load.

The RMS content of the current waveform changes accordingly and this has a bearing on the MOSFET conduction losses that are proportional to I^2_{RMS}.

A measure of the squareness of the waveform can be obtained from the ratio: $K = \frac{I_a}{I_b}$

It can be shown that: $K = \frac{I_a}{I_b} = f(L, L_c)$ where:

L = inductance of the averaging choke.

L_c = l is the critical inductance for a particular input voltage and load power.

As L is increased, K goes from 0 (triangle) to 1 (rectangle).

From the above expression and $I_{avg} = \frac{I_a + I_b}{2}$

we have: $I_a = \frac{2K}{K+1} I_{avg}$,

$I_b = \frac{2}{K+1} I_{avg}$

Substituting into the RMS expression for a trapezoidal waveform, shown in Figure A-1, we have:

$$I_{RMS} = 2\sqrt{D}\, I_{avg} \sqrt{\frac{1+K+K^2}{3(K+1)^2}}$$

For constant $I_{(avg)}$ and D, the normalized (I_{RMS} = 1 for K = 1) I_{RMS} is as shown in Figure A-3. This curve shows that, for trianglar current waveforms, the I^2R losses are 32% higher than for rectangular waveforms. It is also apparent that for $I_a / I_b > 0.6$, the improvement incurred by increasing L is only 2%, so from a practical point of view, L need only be about twice L_c.

Increasing the value of I_a / I_b increases the switch turn-on losses but decreases the turn-off losses. Since the turn-off losses tend to be larger than the turn-on losses, increasing I_a / I_b reduces the total switching loss also.

For the case of discontinuous inductor currcnt (L < L_c), $I_a / I_b = 0$ and is no longer relevant, since the waveforms are now triangles.

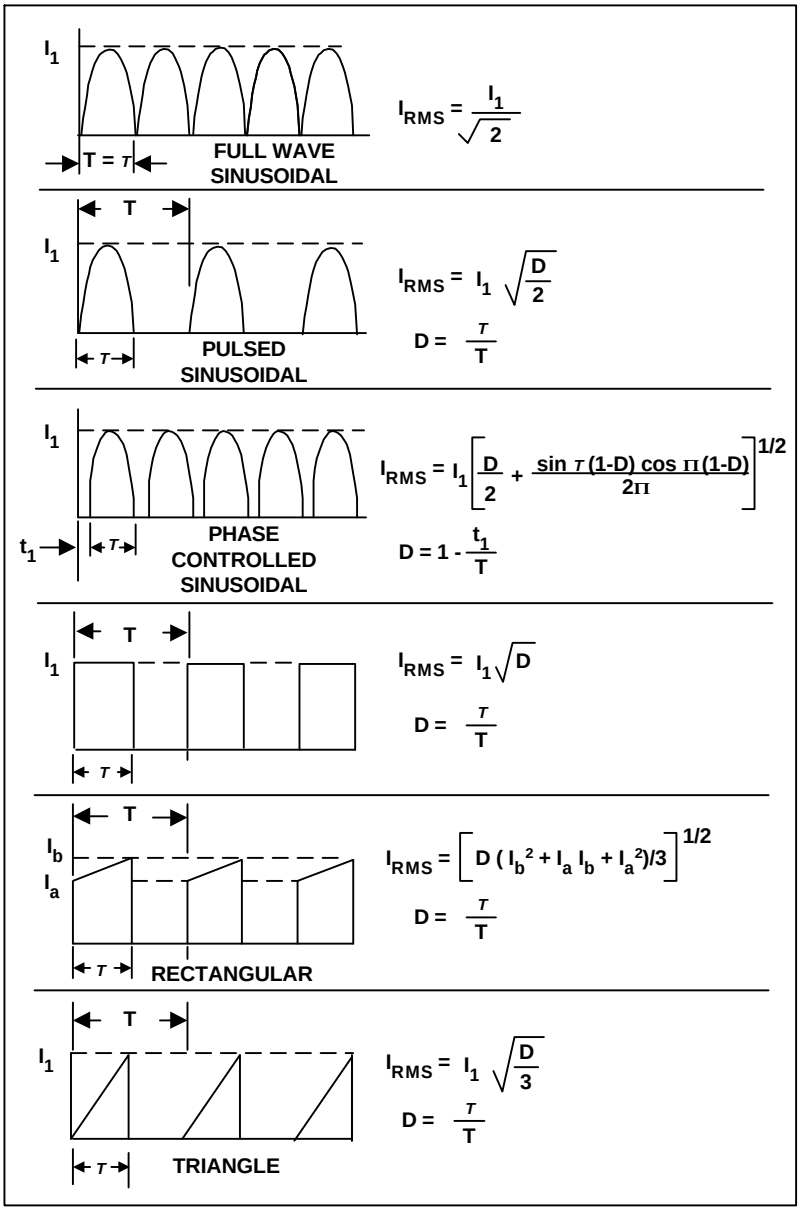


Figure A-1

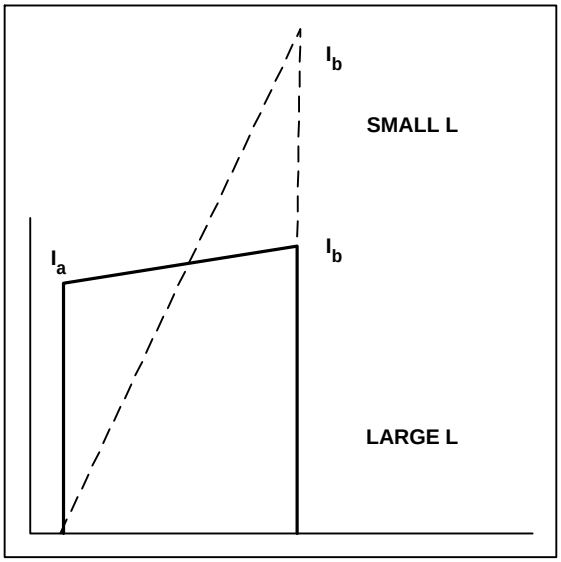


Figure A-2. Current Waveform

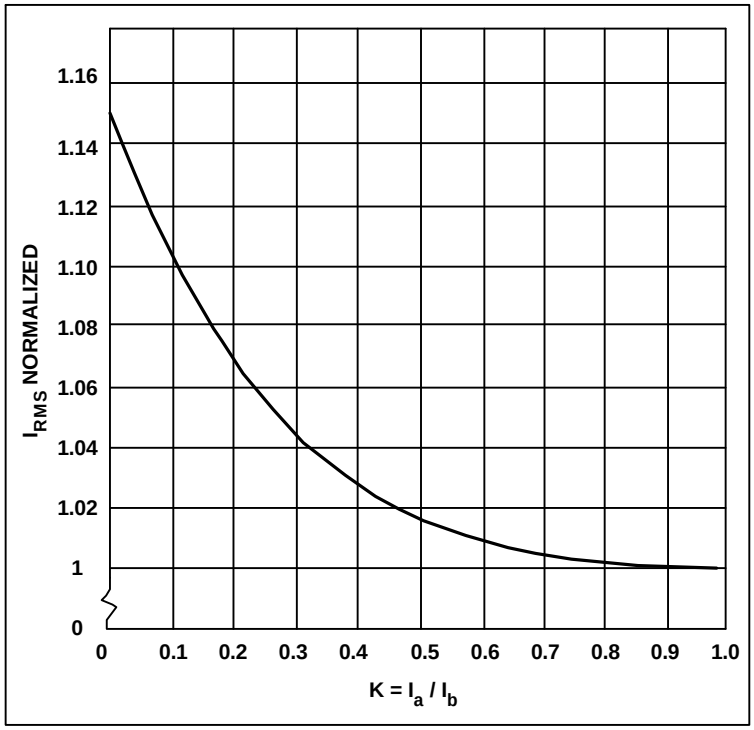


Figure A-3. Variation of IRMS with Squareness Ratio

DETERMINATION OF AVAILABLE FAULT CURRENT FOR SEMICONDUCTOR FUSING

One of the problems facing the design engineer is selecting adequate circuit interrupting devices for his equipment. With the increased emphasis on safety today, it is mandatory that short circuit faults be cleared quickly and without danger to personnel and equipment. Of prime consideration is the determination of the available fault current at the location of the protective device.

The commonly used circuit interrupting devices are circuit breakers and fuses. Circuit breakers are rated for specific maximum current interrupting capacities, and it is common practice to employ various sizes and interrupting capacities in plant distribution systems according to location and service. Some industrial fuses are rated up to a certain stated current interrupting rating, such as 10,000 amperes. Other fuses are tested and certified to be capable of interrupting very large currents. The proper selection of semiconductor protective fuses is dependent upon the available fault current. The sizing of semiconductor devices subject to multiple cycle short circuit currents, such as encountered with a slow-blow fuse or a slow circuit breaker, is also dependent upon the available fault current.

In applying semiconductors and their protective fuses, there are two different sets of conditions to consider. In the first case there is no transformer associated with the semiconductors. One example is a thyristor AC controller working directly off the plant AC supply. Another example is a three-phase bridge also working directly off the plant AC supply.

The second case is where a rectifier transformer is used to supply the power to the semiconductors. An example would be an electroplating rectifier power supply. In this case, the impedance of the associated transformer is high compared to the supply circuit impedance.

The impedance of a transformer is defined as the percentage of rated applied voltage required to cause full rated current to flow through a short circuited secondary winding. Another way of expressing transformer impedance is to say that the impedance of the transformer will limit the short circuit current in the secondary with full rated voltage applied to the primary to a value according to the following relationship:

$$I_{sc} = \frac{I_s}{Z_t}$$

Where:

I_{sc} = Steady state short circuit current

I_s = Rated secondary current

Z_t = Transformer impedance (percent)

Therefore, a transformer with a 5 percent impedance will limit the short circuit current to 20 times the rated current. A transformer with a 4 percent impedance will limit the short circuit current to 25 times the rated current. Transformer impedance values can be obtained from the nameplate or from the manufacturer.

Under the first set of conditions, where the semiconductors are connected directly to the AC supply, the current limitation during short circuit conditions comes from transformer impedances, cable drops, and accumulated impedances reaching back to the source. Normally, the semiconductors are not connected on a primary input supply system with very low impedance and corresponding extremely high available fault current. They are usually installed in an industrial plant where the AC supply has a number of distribution transformers in the line, along with circuit breakers, various sized feeder conductors and cables. Of major interest is the distribution transformer feeding the applicable power line.

The common situation involves a low voltage three-phase system of 60 Hz supplied through transformers. As shown in Fig. 1, the available fault current depends on the following items: available fault current in the primary, transformer size and impedance, secondary voltage, sizes and

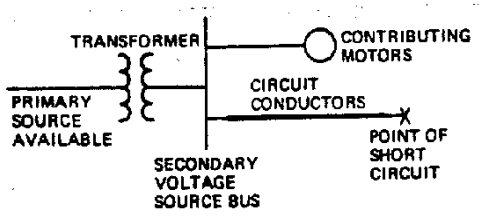


Figure 1 — Circuit Investigated and Results Obtained

effective impedances of motors contributing to the short-circuit current, and the size, length, and cross-section geometry of the feeder conductors connecting the secondary voltage source bus to the point at which the short-circuit duty is being investigated. Electrical motors can contribute substantial amounts of current, when the voltage source is interrupted by acting as generators and converting the kinetic energy into electrical energy.

In Figures 2 through 9, the results of calculations are presented for various transformer sizes. The short circuit current and power factor for each transformer size is defined in terms of distance from the transformer to the point of fault and for various cable sizes. Each figure shows curves for 208, 240, 480 and 600 volt systems.

The magnitude of the AC RMS symmetrical component of the short-circuit current and the power factor of the short-circuit current can be determined from these curves.

Approximate short-circuit current and power factor values for other feeder conductor sizes and arrangements can be obtained by interpolating between the lines on any curve sheet, using impedance values as a rough basis for the interpolation.

The total asymmetrical short-circuit current may be determined from the plotted symmetrical short-circuit current by using a multiplier that is a function of short-circuit power factor, as shown in Fig. 10.

System Conditions Used for Calculations

The equivalent circuit investigated consists of impedances that are considered minimum values. It is assumed that a 500 Megavolt-ampere (MVA) short-circuit capacity is available at the primary of the transformer, and that the source circuit reactance-resistance (X/R) ratio is 25. This ratio corresponds roughly to the standard multiplier of 1.6 used to obtain maximum phase RMS total currents in primary circuits from calculated symmetrical current values. The probability of any set of conditions being more stringent than those selected is very low.

To determine the transformer characteristics, nominal standard transformer impedances of 4-1/2 percent for transformers having ratings up to and including 500 kVA and 5-1/2 percent for transformers having ratings above 500 kVA are assumed. Data supplied by numerous manufacturers were used to determine characteristics.

The impedance of the cables as computed is almost the minimum possible impedance for the conductor sizes considered and is, therefore, conservative. The motors connected to the transformer secondary bus have the characteristics of individual 30-horsepower induction motors and are assumed to have a total kVA equal to that of the transformer.

Using the Curves to Find Short-Circuit Duties

The curves in Figures 2 through 9 are used directly to find the short-circuit current duties and power factor. To find a short-circuit current at the end of the given length of a given size feeder originating at the low voltage bus of a given kVA substation, find a point corresponding to the length of the feeder as read on the horizontal scale of the appropriate graph on the short-circuit current curve marked with the feeder size; then find the short-circuit current corresponding to that point on the vertical current scale. Power factors are found in a similar manner.

Asymmetrical Current Values

To find the asymmetrical current values corresponding to the symmetrical current values determined from the curves, refer to Fig. 10. The average short-circuit asymmetrical current can be found by multiplying the symmetrical current by the multiplier M_A shown in Fig. 10, corresponding to the short-circuit power factor. To find the maximum possible RMS asymmetrical current among the three that are averaged for the value found previously, then use the multiplier M_M found in Fig. 10 corresponding to the power factor.

BIBLIOGRAPHY: AIEE Paper 55-442

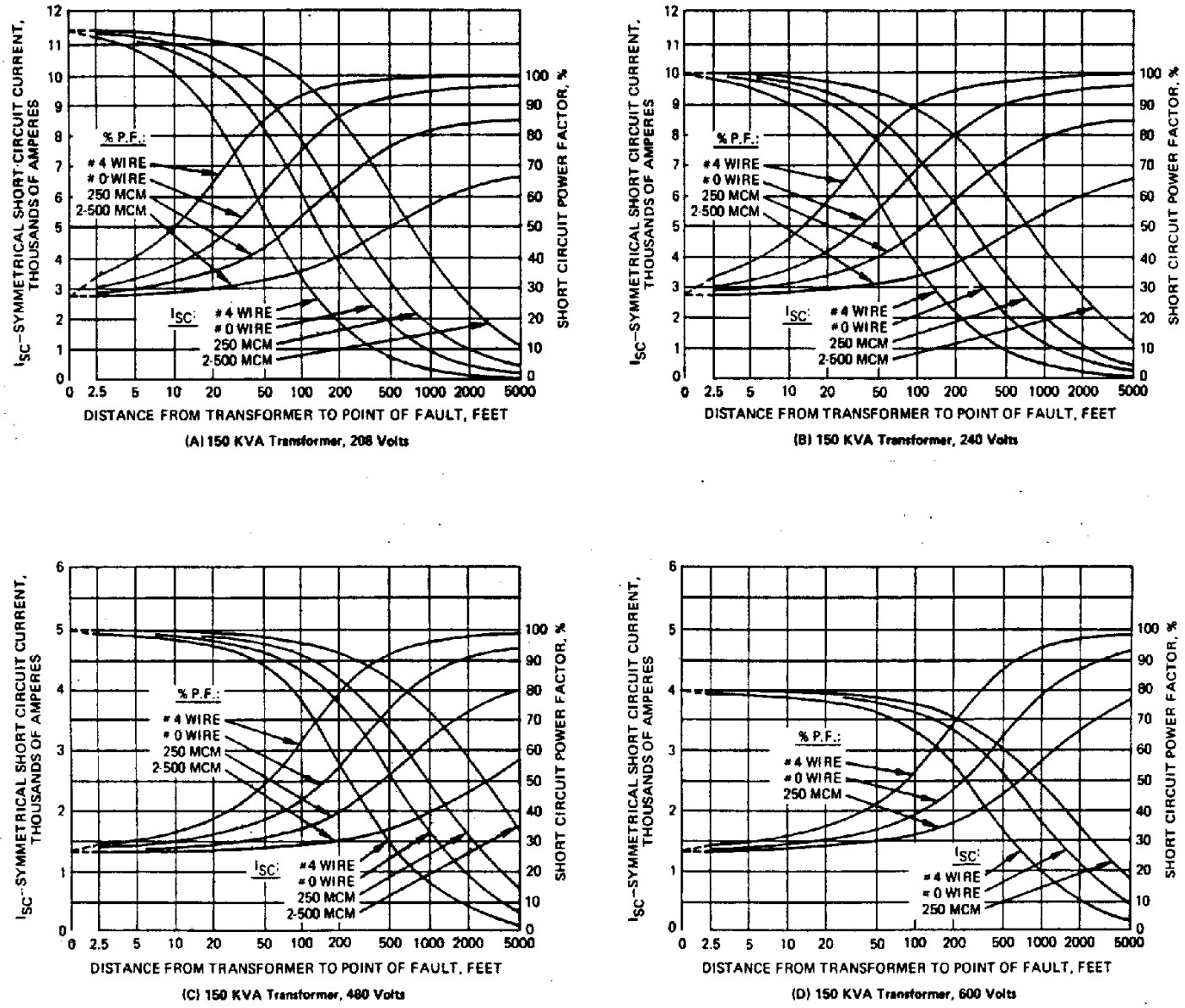


Figure 2 — Symmetrical Short-Circuit Current and Power Factor Versus Distance From a 150-kva Liquid-Filled Power Transformer: X/R = 3.24; R = 1.23 Per Cent; X = 4.0 Per Cent; and Z = 4.19 Per Cent

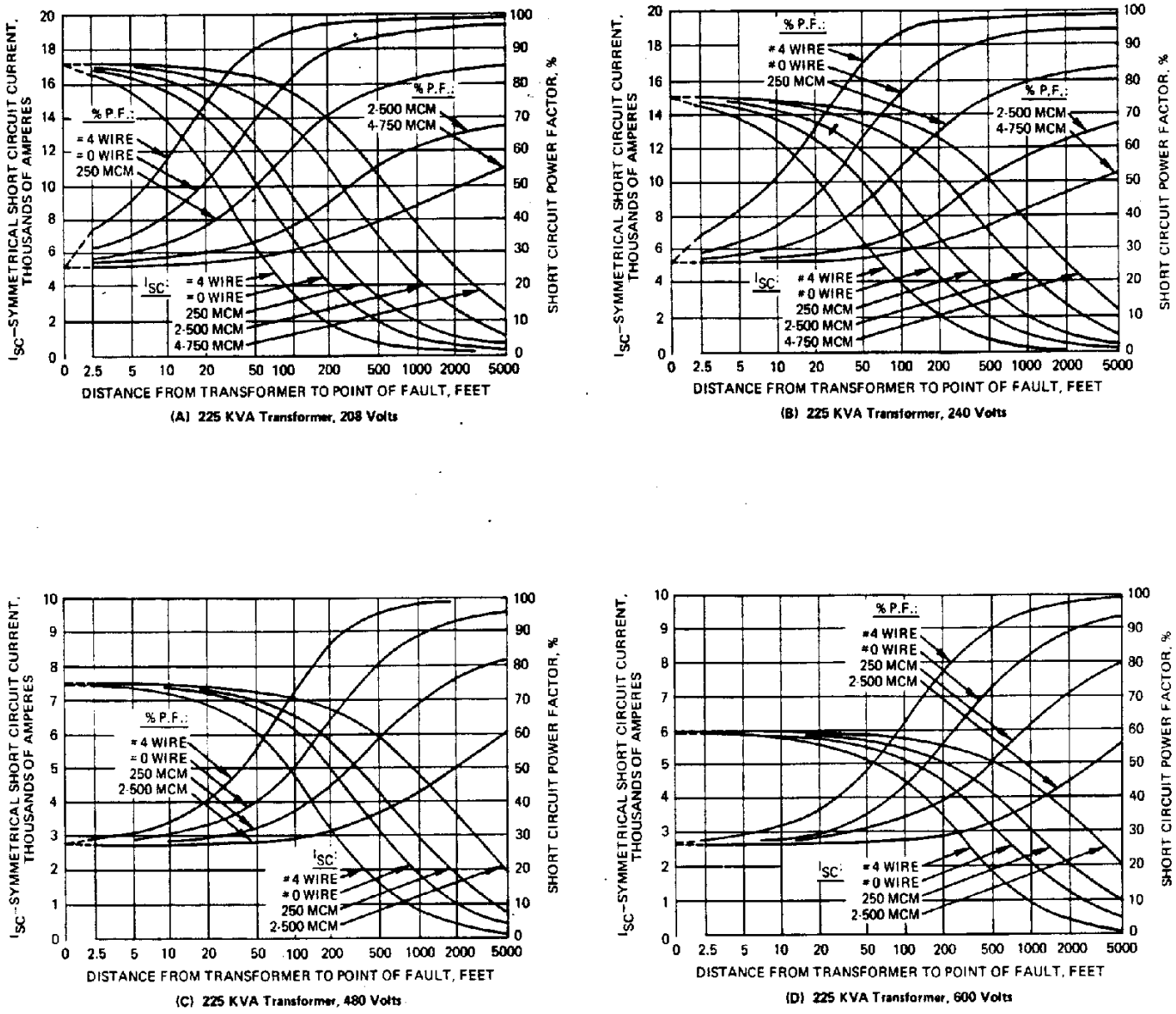


Figure 3 — Symmetrical Short-Circuit Current and Power Factor Versus Distance From a 225-kva Liquid-Filled Power Transformer: X/R = 3.35; R = 1.19 Per Cent; X = 4.0 Per Cent; and Z = 4.17 Per Cent

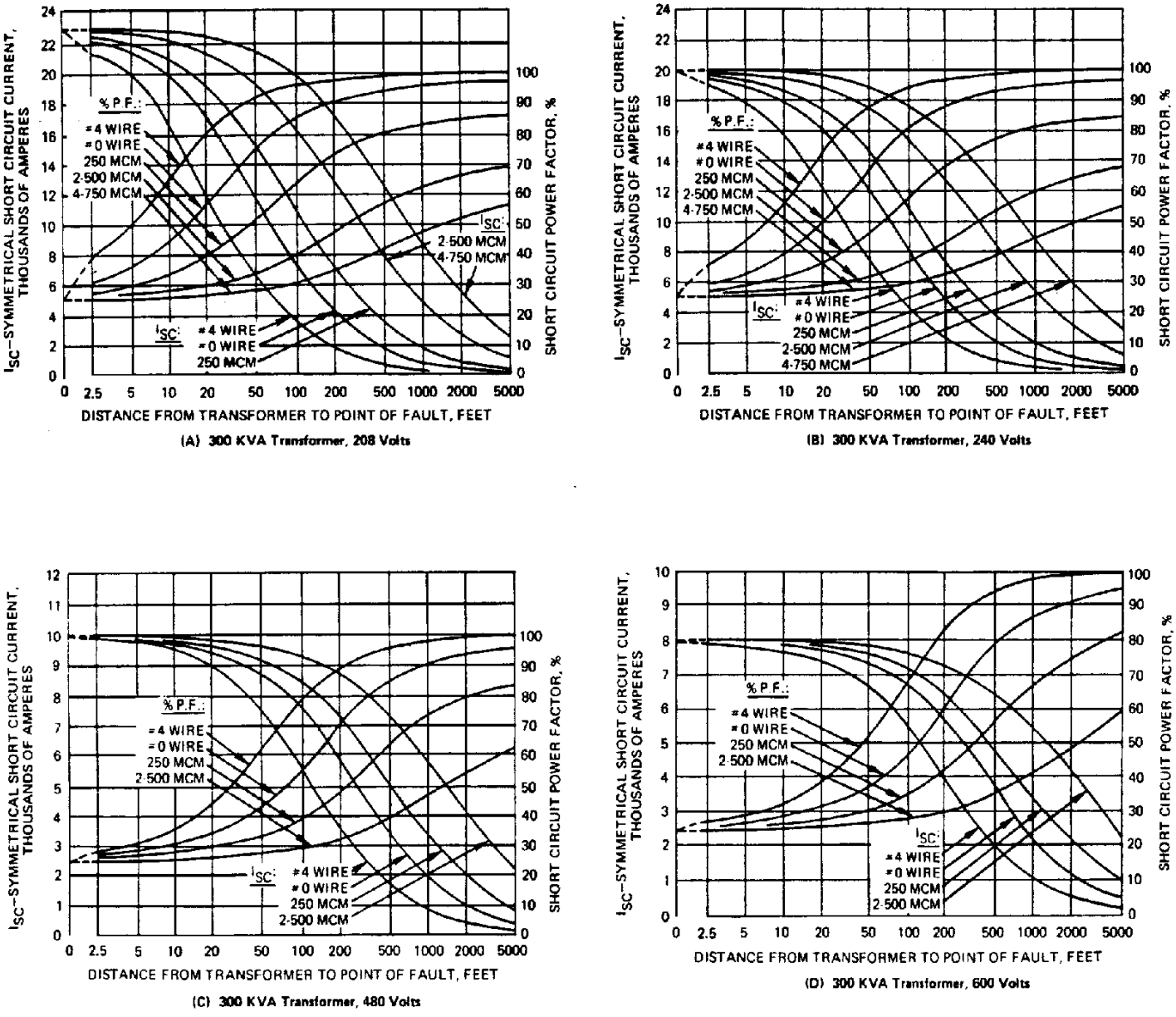


Figure 4 – Symmetrical Short-Circuit Current and Power Factor Versus Distance From a 300-kva Liquid-Filled Power Transformer: X/R = 3.50; R = 1.14 Per Cent; X = 4.0 Per Cent; and Z = 4.16 Per Cent

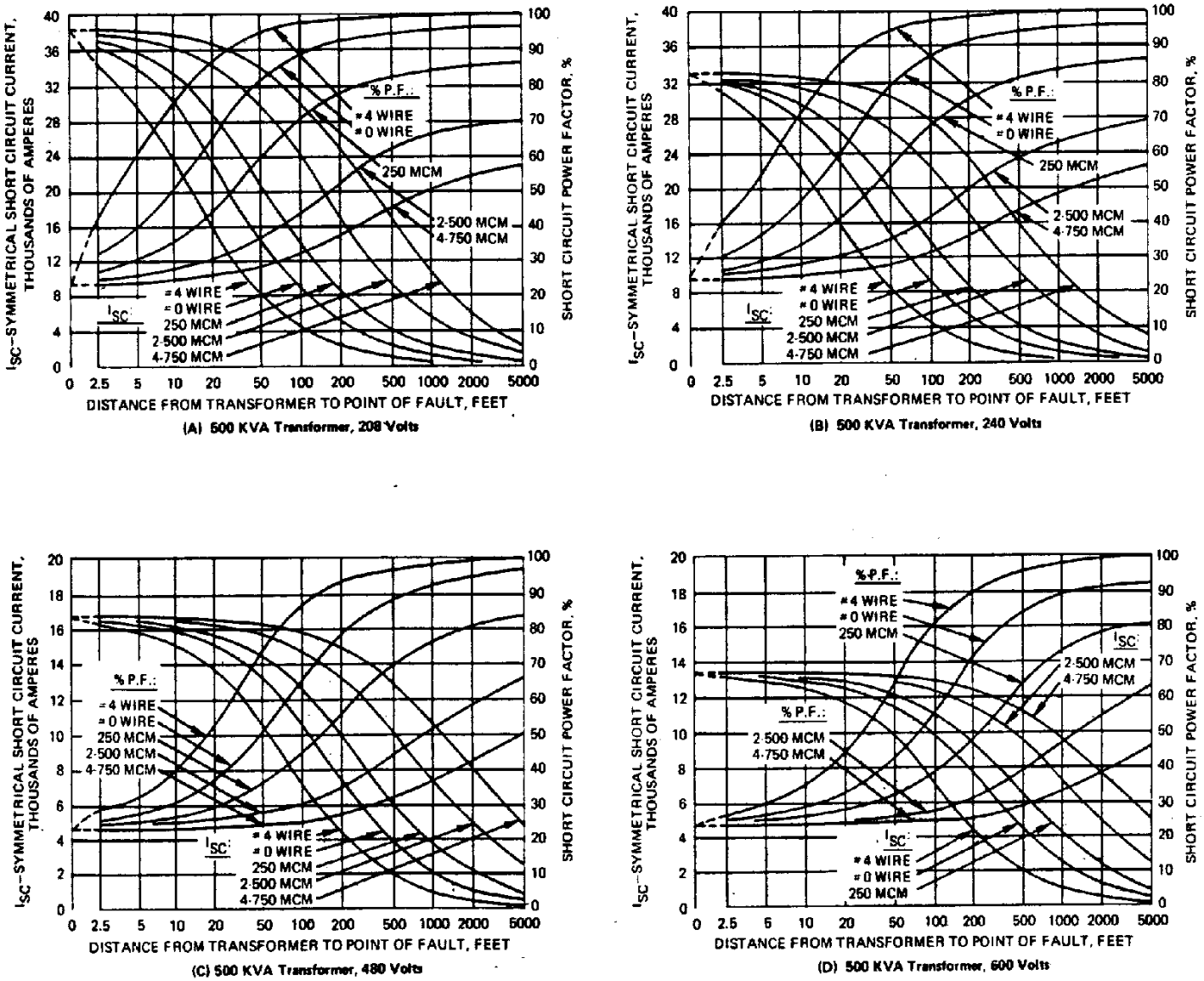


Figure 5 – Symmetrical Short-Circuit Current and Power Factor Versus Distance From a 500-kva Liquid-Filled Power Transformer: X/R = 3.84; R = 1.04 Per Cent; X = 4.0 Per Cent; and Z = 4.12 Per Cent

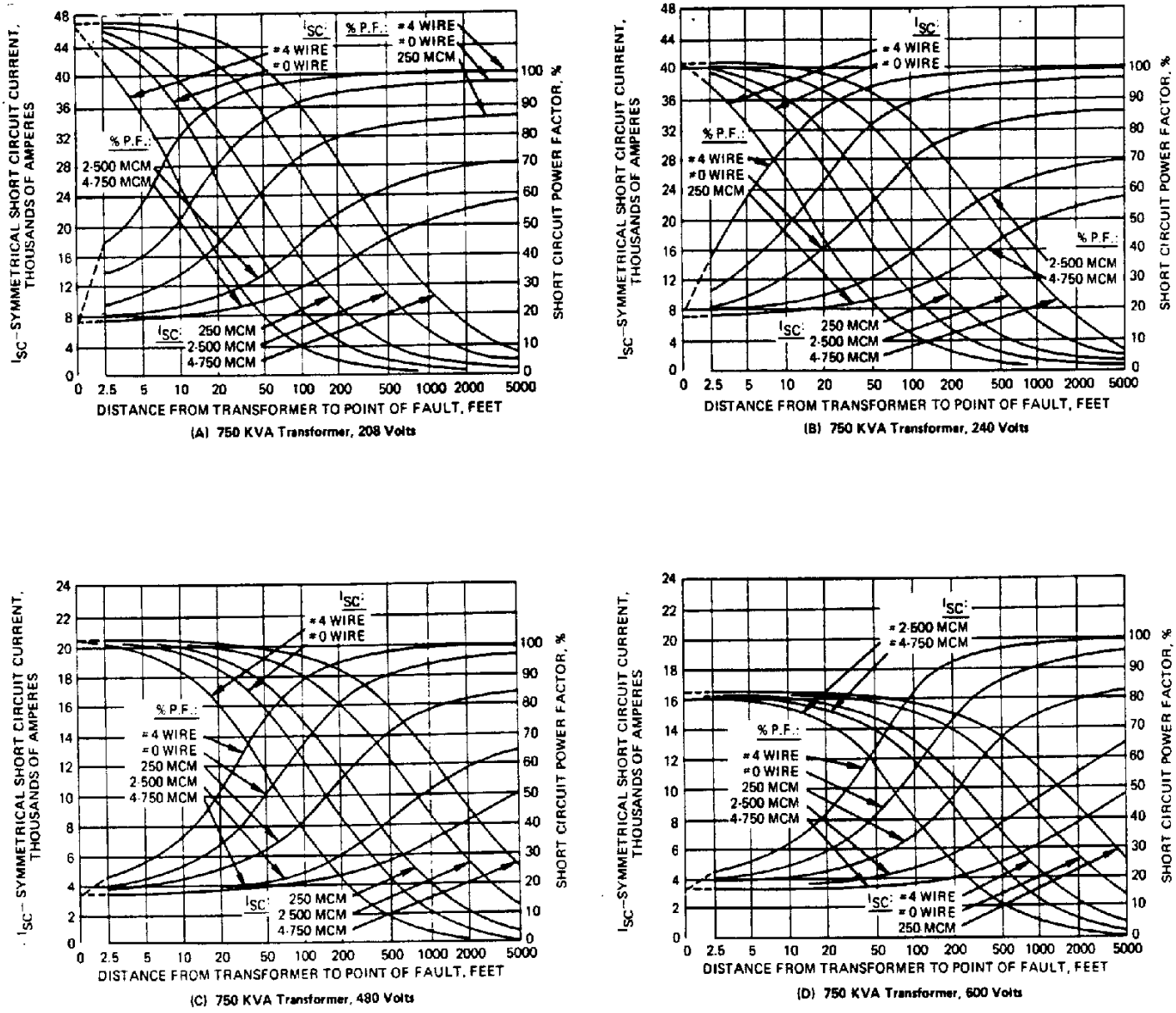


Figure 6 — Symmetrical Short-Circuit Current and Power Factor Versus Distance From a 750-kva Liquid-Filled Power Transformer: X/R = 5.45; R = 0.94 Per Cent; X = 5.1 Per Cent; and Z = 5.19 Per Cent

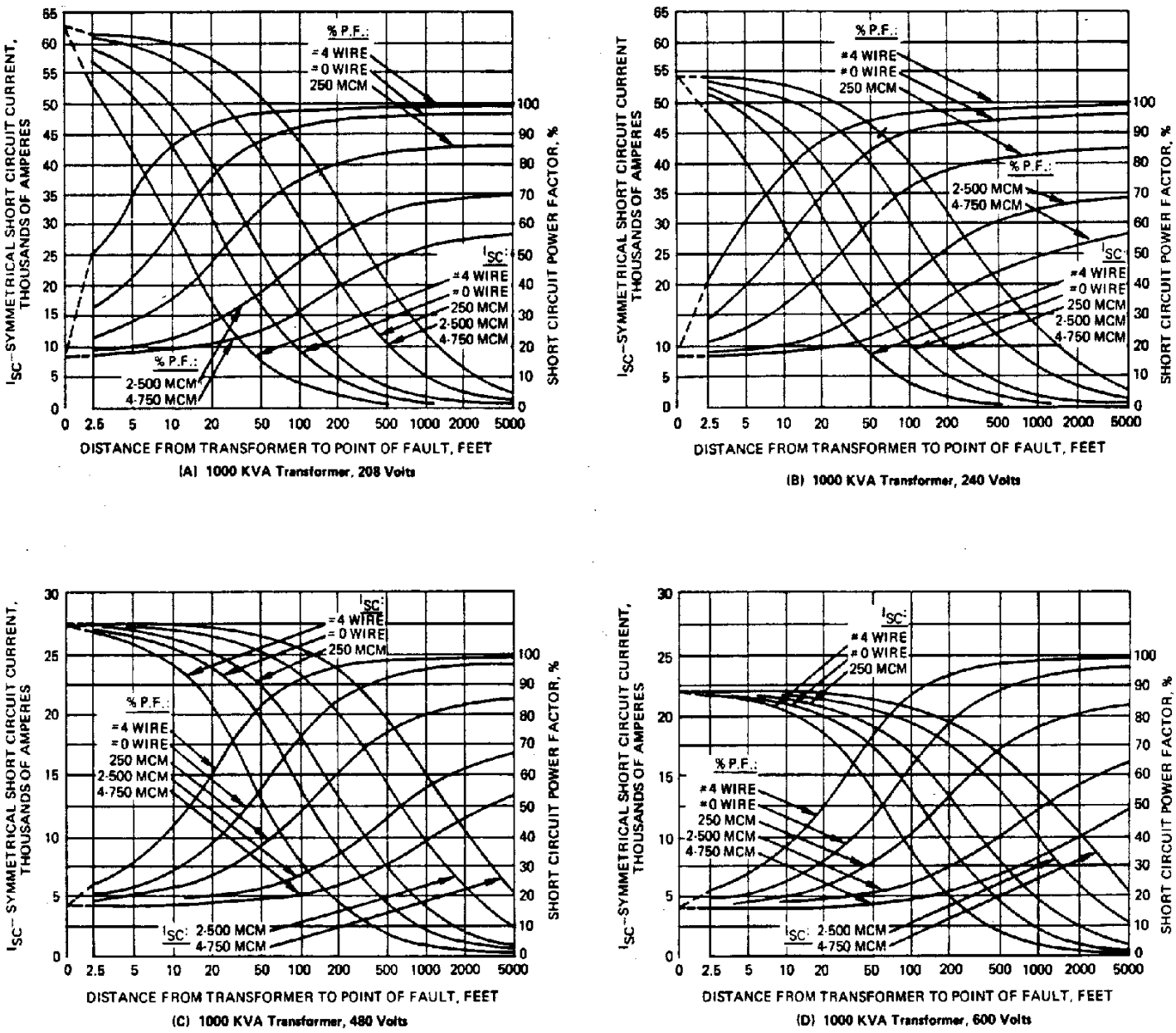


Figure 7 — Symmetrical Short-Circuit Current and Power Factor Versus Distance From a 1,000-kva Liquid-Filled Power Transformer: X/R = 5.70; R = 0.89 Per Cent; X = 5.1 Per Cent; and Z = 5.19 Per Cent

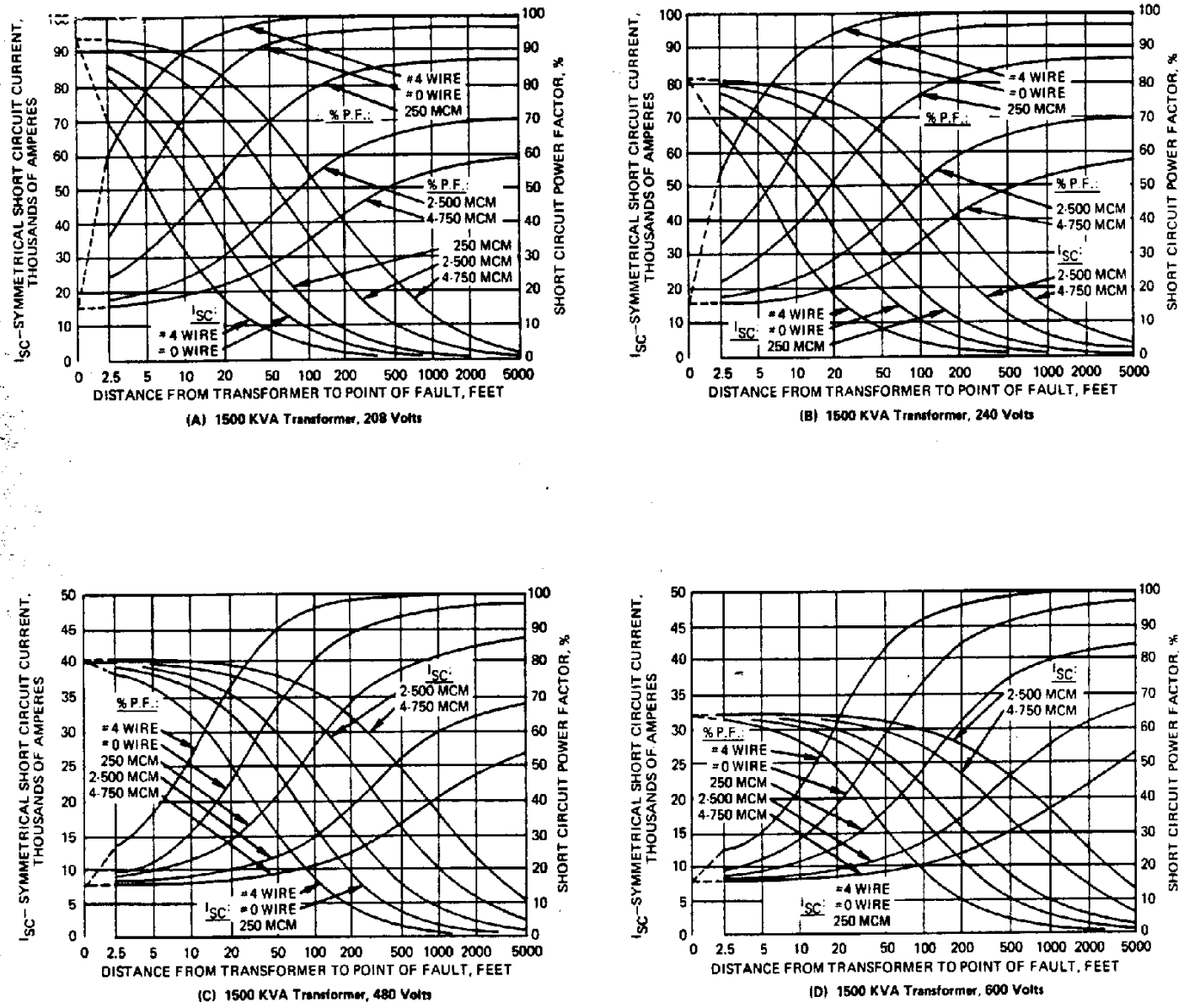


Figure 8 — Symmetrical Short-Circuit Current and Power Factor Versus Distance From a 1,500-kva Liquid-Filled Power Transformer: X/R = 6.15; R = 0.83 Per Cent, X = 5.1 Per Cent; and Z = 5.18 Per Cent

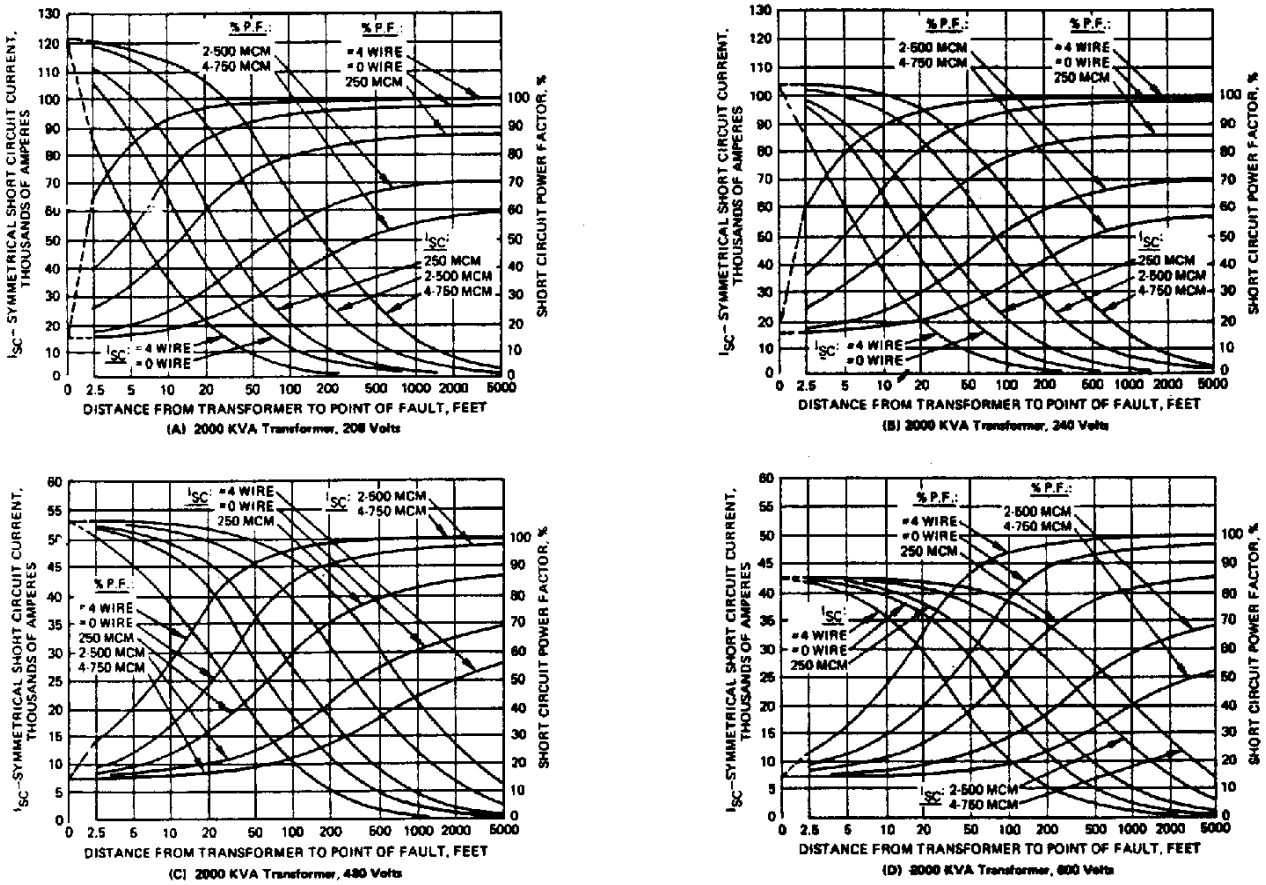


Figure 9 — Symmetrical Short-Circuit Current and Power Factor Versus Distance From a 2,000-kva Liquid-Filled Power Transformer: X/R = 6.63; R = 0.77 Per Cent; X = 5.1 Per Cent; and Z = 5.17 Per Cent

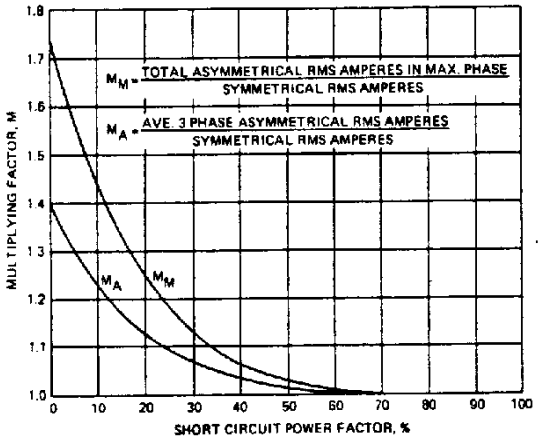


Figure 10 — Multiplying Factors to Obtain Short-Circuit Asymmetrical Current From Symmetrical Values, at a Point in Time 1/2 Cycle (60-Cycle Basis) after Initiation of a Fault

Originally written for this Application Note by Glenn Geissinger, International Rectifier, El Segundo, California.
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Printed in U.S.A. 2/74

APPLICATION NOTE

AN-312

SELECTION OF SCR's FOR SINGLE PHASE DC MOTOR DRIVES

The continuing search for circuit simplicity and low cost in motor speed control has led many designers to SCR controls. Because of their inherent reliability, long life, silent operation, and high efficiency, SCR's are now widely used in motor control circuits.

The circuit in Figure 1 is a full wave bridge feeding the armature of a dc motor through a single controlled rectifier. The speed of the motor is controlled by appropriate firing of the controlled rectifier at various angles with respect to the applied voltage which results in phase control of forward current through the controlled rectifier.

After every half cycle of forward current, the controlled rectifier must recover its forward blocking state. This means that the device must turn off during the time interval between the cessation of forward current and reapplication of forward voltage. A quick analysis of the applied voltage wave shapes would lead one to believe that the time interval between forward current cessation and reapplication of forward voltage is zero. However, in analyzing the circuit, one can see that the time required for the voltage to overcome the threshold voltage of two diodes and the controlled rectifier in series, is the time during which the device can recover to its blocking state. Threshold voltage is that voltage required across the diode or controlled rectifier to cause substantial forward current to flow. Threshold voltage is approximately 0.6 volts.

With an input of 230 volts it would appear that the time interval provided by the threshold voltages should be approximately 23 microseconds, as seen in Figure 2.

Turn-Off Time

Voltages and wave shapes observed in laboratory tests of this circuit, as illustrated in Figure 3, show that in one

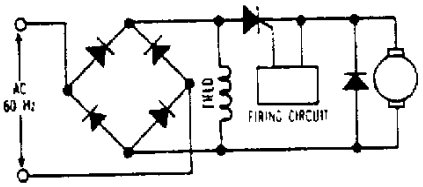


Figure 1 – DC Motor Control

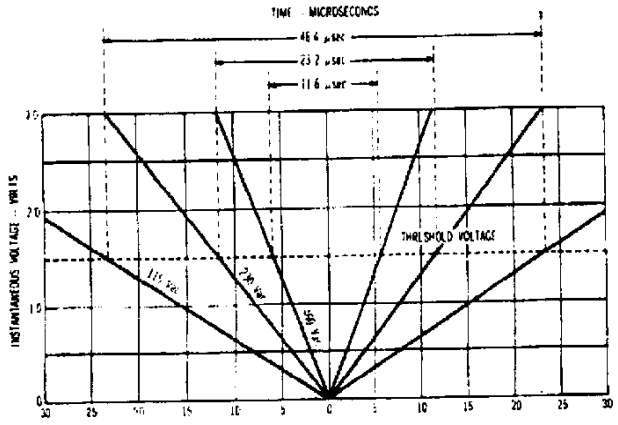


Figure 2 – Interval of Zero Current Flow

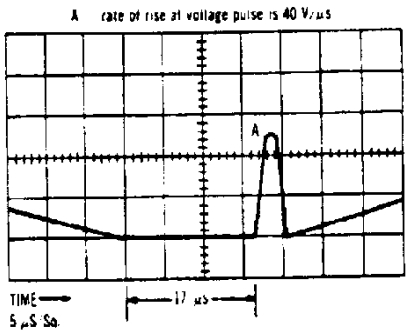


Figure 3(a) – Turn-Off Time

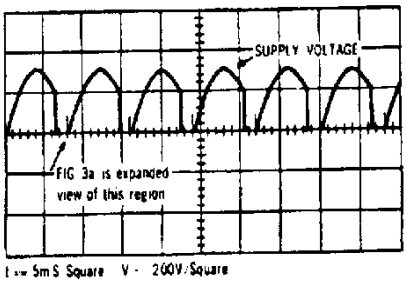


Figure 3(b) – Turn-Off Time

case from the time the forward current dropped to zero (indicated by zero forward voltage drop) to the time of the voltage transient, there is approximately 17 microseconds. This time interval is less than the anticipated 23 microseconds. We can see that with this circuit one critical parameter requiring careful definition is turn-off time. Turn-off time is defined as the time from the end of forward current flow to the reapplication of forward blocking voltage. The industry has standardized on certain test conditions for various size devices. These test conditions are: peak forward current, rate of rise of reverse current, peak reapplied forward blocking voltage, rate of rise of reapplied forward blocking voltage, and junction temperature. An increase in rate of rise of reapplied blocking voltage or reduction in reverse current increases the amount of time required for turn-off.

Getting back to Figure 3, the voltage transient is interesting in that it is 30% of the peak supply voltage, is five microseconds wide, and the rate of rise of the leading edge is 40 volts per microsecond. This particular voltage transient was seen for both resistive and inductive loads.

Thus, we see that instead of 23 microseconds allowed for turn-off, we have only 17, a much more stringent requirement on the controlled rectifier. Also, we can see from Figure 3 that the reverse voltage necessary to help sweep carriers from the forward blocking junction is zero. Therefore, with no reverse voltage to help sweep out carriers, the turn-off time requirements is much more difficult to meet.

We see that in this case the device must recover by itself, i.e., natural recombination of carriers in the junction. Normally, for a controlled rectifier to turn off fast when a diode is connected anti-parallel to it, the turn-off time measured under standard conditions is below 20 microseconds. Experimentally, it has been found that for a device to function in this motor control circuit, the turn-off time requirement will be below 20 microseconds when measured under standard conditions. While it might seem that 20 microseconds far exceeds the 17 we mentioned before, the normal design considerations for the heat sink allow the device to operate below rated junction temperature. This in turn causes the turn-off time of the device to be much shorter than its rated value.

Test Vs. Circuit Conditions

Shown in Figure 4 is a curve of normalized turn-off time (measured under standard conditions) vs. junction temperature. This curve illustrates that by reducing the junction temperature 25 degrees (from 125 to 100 degrees) the turn-off time will be 80% of what is measured at 125 degrees junction temperature. This means that a device measuring 20 microseconds turn-off at 125°C would measure about 16 microseconds at a 100°C.

As noted before, turn-off time is usually measured throughout the industry under certain conditions. While the observed operating conditions are not standard (for turn-off time measurements) a correlation between circuit commutated turn-off time and circuit commutated turn-off time measured with a diode anti-parallel to the controlled rectifier has been observed.

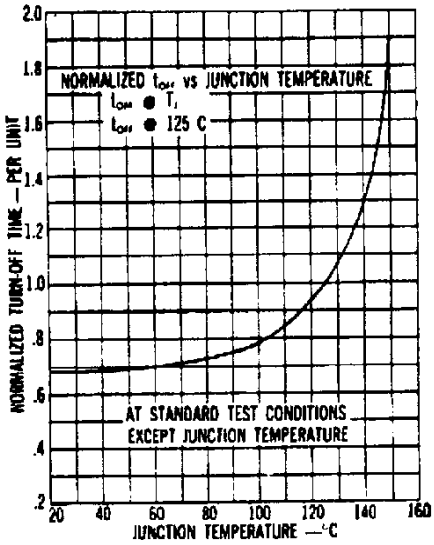


Figure 4 — Normalized Turn-Off Vs. Junction Temperature

Standard turn-off time is known as circuit commutated turn-off time because circuitry causes the reversal of current through the test device which in turn causes the controlled rectifier to turn off.

When a diode is connected in anti-parallel to the controlled rectifier, the reverse voltage (and current) bypasses the controlled rectifier. Turn off time measured under these conditions could be called "starved" circuit commutated turn-off time and more nearly approximated conditions encountered in the circuit under discussion.

During turn-off, the diode in anti-parallel to the controlled rectifier puts a reverse bias of approximately 0.6 volts across the device. The reverse current through the device because of this reverse voltage is negligible and, as expected, the turn-off time measured under these conditions is greater than that measured under standard conditions.

Laboratory tests show that controlled rectifiers measuring less than 20 microseconds turn-off time do not exhibit a large increase (if any) when tested with a diode connected anti-parallel to it. Controlled rectifiers measuring longer than 20 microseconds can double and even triple when tested under these conditions.

Empirically, it has been found that those devices that function properly in 220 V input motor drive circuits, measure less than 20 microseconds circuit commutated turn-off time. However, a turn-off time limit of 22 microseconds under starved circuit commutated test conditions has been shown to give a 95% confidence level of proper circuit operation. This turn-off time is dependent upon the supply voltage as indicated in Figure 2.

Alternative Methods

Fast turn-off devices are not always economical and an alternative is desirable. There are several ways of getting around the turn-off time requirement in this circuit. The obvious solution is to somehow give the device a longer time during which to turn off. One way this can be accomplished is by putting a self-saturating reactance in the ac side of the circuit. This allows more time for the controlled rectifier to turn off by unsaturating at the end of each half cycle, and holding off the appearance of opposite voltage until the reactor saturates again. A method such as this works extremely well and for fractional horsepower dc motors is quite economical.

However, for larger horsepower motors the inductor is quite large, both in inductance required and current capability.

Another method of helping turn-off is to put a capacitor across the load. The capacitor coupled with the distributed inductance of the circuit, will swing the voltage negative at the cessation of forward current and help maintain a counter EMF across the controlled rectifier. This will help sweep out carriers and allow the device to turn off faster. The one drawback to this scheme is that the capacitor during phasing-on periods will draw large amounts of transient current which the controlled rectifier must be able to handle.

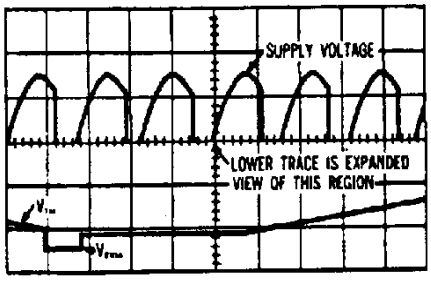


Figure 5 – Voltage Wave Shapes Across the SCR

The voltage wave shapes shown in Figure 5, were taken across the controlled rectifier when a capacitor was connected across the load. We can see that immediately after the forward current conduction the voltage goes negative and helps turn off the device. In addition to this, we see that the transient voltage spike, that is obvious in Figure 3a, has been suppressed. The capacitor across the load does more than just help turn-off by applying a reverse bias; it suppresses the voltage spike which also reduces the severity of the conditions under which the device must turn off.

As a third alternative, the controlled rectifier may be aided in turning off if one or more rectifier diodes are connected in series with it. Doing this will increase the threshold voltage mentioned earlier. In many cases it may be found more economical to do this than to attempt to select extremely fast units, or to use another circuit configuration where turn-off time is not critical. For instance, the turn-off time of the controlled rectifiers in Figure 2 is not critical. However, it is quite possible that it would be more economical to add one or two diodes in series with the controlled rectifier in the circuit of Figure 1 than to use a completely different circuit.

A physical arrangement illustrating how two diodes may be connected in series with the controlled rectifier, at the same time mounting all the rectifying devices on three heat exchangers, is shown in Figure 6.

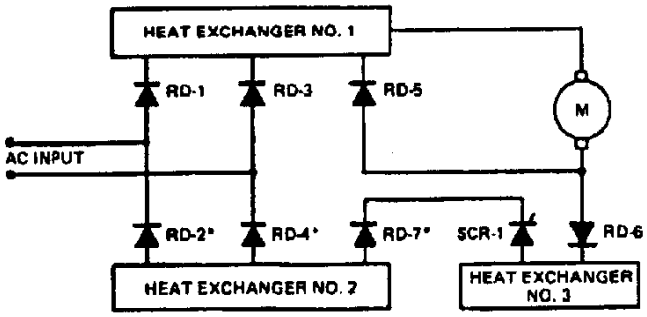


Figure 6 – Rectifying Devices, Including Two Additional Rectifier Diodes, Mounted on Three Heat Exchangers

High Power Systems

This drive is generally not used above 3 hp. There are several reasons. One is that most users prefer to connect larger loads to three phase power supplies as it gives better loading on the power system. Also, as the supply voltage increases, the turn off requirement increases and the larger devices required do not have fast turn off. In addition, large motors don't commutate as well on single phase dc as smaller ones do. They also heat up more due to the high ripple current from a single phase rectifier. Both these drawbacks can be overcome by running the motor at partial load, however this increases motor cost. Generally, the economics of larger motors requires three phase systems.

Originally written by Frank Durnya, International Rectifier, Semiconductor Division, El Segundo, California. Originally published in the Summer 1968 edition of Rectifier News by International Rectifier, El Segundo, California.

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SILICON CONTROLLED RECTIFIERS
AN-309

APPLICATION NOTE

SCRs — Their Parameters, Specifications, Ratings, and Characteristics

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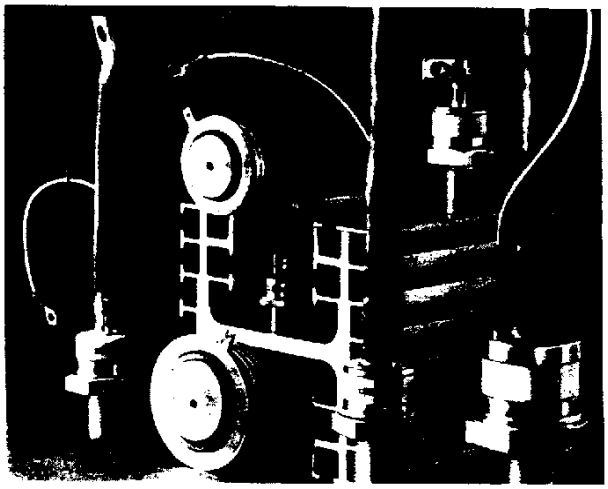
SCR Parameters

- Forward and Reverse Characteristics
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- Di/dt Rating
- Critical Dv/dt
- Turn-off Time
- Parameter Trade-off

Device Data

- Voltage Ratings
- Electrical Specifications
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- Rating Curves

Special Order Devices



The silicon controlled rectifier is a *rectifying* device inasmuch as it has a **forward direction** in which it may have a very low resistance and a **reverse direction** in which it has a very high resistance. It is *controlled* since it can be switched from a high forward resistance **(off-state)** to a low forward resistance condition **(on-state)**. Although the change in resistance is great (high voltages can be blocked, high currents can be conducted), it can be achieved with very small values of gate voltage, current, and power.

International Rectifier offers its SCRs in the most practical and efficient package outlines available. Some of these packages are shown in Photo 1.

IR provides all flex lead outline packages with an auxiliary cathode lead. This lead is designed to be twisted with the gate lead to prevent stray signal pickup and resultant false firing, and to provide a cathode connection to the firing circuit.

The circuit symbol and block diagram of the silicon controlled rectifier are illustrated in Figure 1. Figure 2 shows the cross-section of a typical silicon wafer used in such a device.

As a circuit element, the silicon controlled rectifier can be used to block the normal flow of current for any length of time desired. To initiate conduction, a signal should be

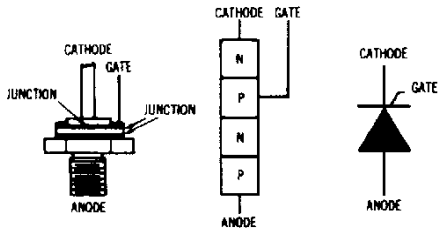


Fig. 1 — Cross Section, Block Diagram, and Electrical Symbol of Silicon Controlled Rectifier

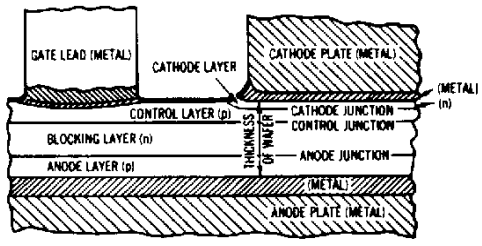


Fig. 2 — Cross Section of Idealized Controlled Rectifier Structure in the Region Close to the Gate

applied to the gate to fire or trigger the device on. When used in an ac circuit, conduction may be initiated at the beginning of any given positive half cycle, thus providing a simple on-off control, or at some later time in the positive half cycle, thus varying the voltage impressed upon the load.

When conduction is initiated only at the beginning of the positive half cycle, it is called zero cross-over firing. It virtually eliminates system electrical noise, radio frequency interference and line voltage disturbance. When conduction is initiated at some time during the positive half cycle it is called phase control and the interval of delaying the initiation of current is the firing angle or angle of phase retard, α (in electrical degrees). The interval of current conduction (in a simple, half-wave resistive circuit) is known as the conduction angle.

In more complicated rectifier circuits having two or more rectifying devices, varying the firing angle α reduces the average output voltage but does not necessarily change the conduction angle, since this is determined primarily by the particular circuit used.

Controlled rectifiers may be used to control ac power by connecting them in an anti-parallel (inverse parallel) manner so that one conducts load current in one direction while the other conducts in the opposite direction (IR's Logic-Triac controls ac as well as dc, depending on gate signal characteristics). The gate firing signal may be used to switch the flow of current on and, by using phase control, the average voltage applied to the load may be varied.

In dc circuits where the voltage across the controlled rectifier does not reverse, the gate may be used to initiate current flow, but some specific means must be provided to turn the flow off. (In operation in ac circuits, current flow ceases when the supply voltage reverses at the end of each positive half cycle.) In a dc circuit, a mechanical switch may be used to interrupt the current, or a more complex circuit can be used in which firing a second controlled rectifier causes a momentary flow of reverse current through the first controlled rectifier, causing it to turn off. This process is known as commutation, and is the basis of operation of the controlled rectifier inverter. Devices having fast turn-off times are used for such applications.

Gate triggering circuits should provide a well defined pulse of current which is several times greater than the maximum required gate current to trigger (I_{GT}) (at the minimum anticipated operating temperature) given for the particular device to be used. Curves are presented in each IR Product Data Sheet which show the range of gate voltage and current within which satisfactory operation can readily be achieved without exceeding the voltage, current, and power dissipation ratings of the gate. For applications where the initial anode current rises very steeply (high di/dt), gate pulses approaching the maximum permitted by the gate characteristic curve are most desirable to minimize device heating while it is first turning on. Triggering by varying a dc bias, commonly used with thyratron tubes, is not recommended for controlled rectifiers since gate sensitivity varies markedly with changes in junction temperature as well as from one device to another.

SCR PARAMETERS

Forward and Reverse Characteristics

The graph of the on-state, off-state, and reverse characteristics of a typical controlled rectifier is shown in Figure 3.

Turn-On Time

Turn-On Time consists of two distinct periods, the Delay Time (t_d) and the Rise Time (t_r). See Figure 4 for a display of the graphs of current and voltage during turn-on.

The Delay Time of a controlled rectifier is dependent on the internal geometry of the device and the bulk properties of the silicon. It takes a finite time for the injected carriers to move in the thin gate layer.

Delay time (t_d) is defined as the time taken from the moment at which the gate pulse reaches 10% of its peak to the time when the anode-to-cathode voltage has fallen to 90% of its initial value.

Rise time (t_r) is defined as the time taken for the anode-to-cathode voltage to drop from 90% to 10% of its initial value. It should be noted that 10% of the initial anode-to-cathode voltage is generally many times the on-state voltage which the controlled rectifier will exhibit at the same current when it is fully turned on.

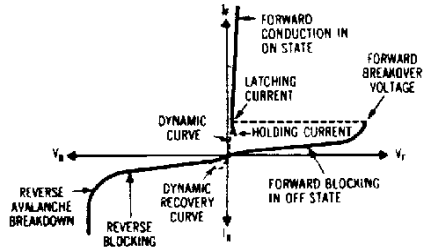


Fig. 3 — Controlled Rectifier Instantaneous Forward and Reverse Characteristics

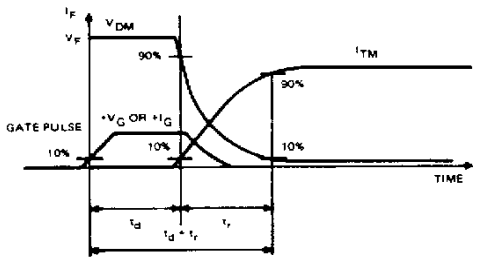


Fig. 4 — Anode Voltage and Current Waveforms During Test for Turn-on Time

Controlled rectifiers turn on first in the region near the gate and then the action spreads until the entire junction is turned on. This action is illustrated in Figure 5. The propagation rate of turn-on is approximately 0.1 mm/μsec, but it may vary during the turn-on interval and is affected by the magnitude of the load current.

SILICON CONTROLLED RECTIFIERS
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IR's ACE SCRs incorporate an advanced internal geometry, thereby, offering improved turn-on characteristics, including greater area turned on initially and a reduction in the time required for device to completely turn on.

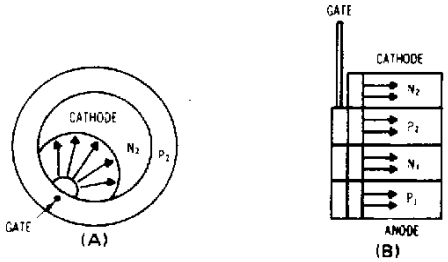


Fig. 5 — Initiation of Gated Turn-on Action

Turn-On Voltage Drop

Turn-on voltage drop (V_{TO}) is measured by applying a short, sinusoidal current pulse and measuring the voltage drop at the peak of this pulse. Two test conditions have been commonly used by controlled rectifier manufacturers:

1. 10 microsecond pulse width, 150 Amperes peak. (Fig. 6A)
2. 4 microsecond pulse width, 300 Amperes peak. (Fig. 6B)

A third method has been devised which permits V_{TO} to be read at both current levels and at almost the same time intervals. (Fig. 6C)

Waveforms under all three test conditions are shown in Figure 6. IR employs conditions (B) and (C).

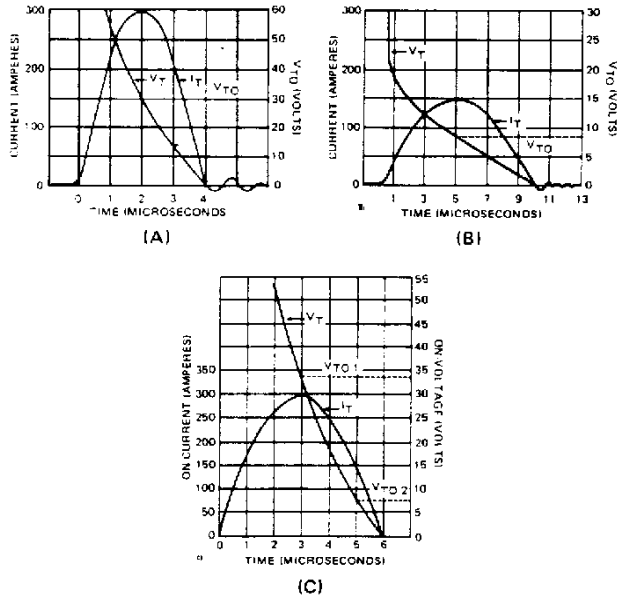


Fig. 6 — Voltage and Current During Test for V_{TO}

Di/dt Rating

The test circuit and on-state current waveform adopted by the industry for testing for di/dt are given in Figure 7. The anode current pulse is such that the 50 per cent point is reached in 1 microsecond or a little longer. The pulse reaches its peak about 2 microseconds later and then drops quickly to zero. Thus, this test is truly a test only of the ability of the device to handle a steeply rising current during initial turn-on.

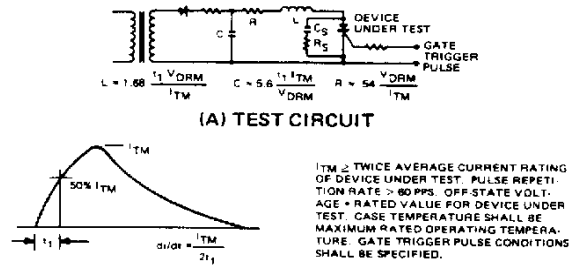


Fig. 7 — Circuit and Waveform for Testing di/dt

Critical Dv/dt

If the forward voltage across a controlled rectifier in the off-state increases at a very high rate, it can cause the device to turn on as if the device has been triggered by a gate pulse. If this takes place under normal operation the controlled rectifier may be damaged. To avoid this, the device should be tested to be sure it has a minimum dv/dt greater than the maximum value it will be subjected to in normal operation. Figure 8 shows the waveform and measurement points during the test.

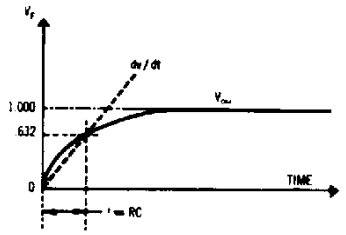


Fig. 8 — Anode Voltage Waveform During Test for Critical dv/dt

Turn-Off Time

Circuit commutated turn-off of a controlled rectifier may be achieved by the application of a reverse voltage to the anode to cathode circuit, causing a substantial reverse current to flow for a short period of time. The Turn-off Time (t_q) of a controlled rectifier is defined as the shortest time interval between the instant at which the anode current reverses from positive to negative and the instant at which the anode-to-cathode voltage becomes positive which can exist with the device being able to sustain the forward voltage without switching to the on-state. The waveforms during turn-off time testing are shown in Figure 9.

SILICON CONTROLLED RECTIFIERS
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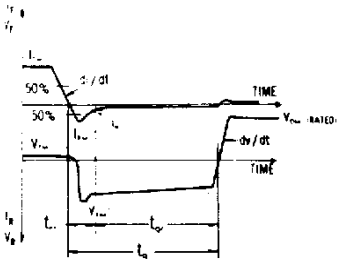


Fig. 9 — Anode Voltage and Current Waveforms During Test for Turn-off Time.

Parameter Trade-Off

The development of devices with standard or special characteristics is a result of compromises among the various parameters a device may exhibit. Table 1 lists the parameters most often discussed for a specific application of a controlled rectifier and the effects various process changes and operating conditions have on them.

These trade-offs may not apply to IR's ACE SCRs. Other IR application notes are devoted to applying and selecting inverter type SCRs.

DEVICE DATA

Data for the individual devices are listed in IR's individual Product Data Sheets under the headings described below.

Voltage Ratings

These values are listed by part number for each device.

This listing includes parameters which are peculiar to specific voltage ratings rather than to specific series as listed under the heading Electrical Specifications. These ratings include specific repetitive and non-repetitive peak reverse or avalanche voltage ratings, and breakover voltage for each individual device.

Electrical Specifications

The values covered in this section give the major characteristics of the devices covered. The values are listed by series rather than by part number.

Mechanical Specifications

Under this heading are outlined the mechanical characteristics needed to enable the user to properly install the device in a given piece of equipment and a physical description of the device.

Rating Curves

Each Product Data Sheet includes curves for rating the device at conditions other than those listed in the specification table.

SPECIAL ORDER DEVICES

IR has a broad background of producing enhanced characteristic devices and a long history of developing SCRs for special applications. IR can help you solve a specific SCR application problem by selecting standard devices which exhibit the characteristics you require; by developing specially produced devices; by evaluating the circuit parameters, operating conditions, and device requirements; or by offering special SCR and SCR-rectifier assemblies, firing circuits, or pressure-assembled devices.

To discuss special requirements or to secure other technical assistance, or to obtain delivery and price quotations, feel free to contact your local IR Distributor, your local IR Field Office, or IR's El Segundo offices.

TABLE 1 – CONTROLLED RECTIFIER PARAMETER TRADE-OFFS

SCR Parameter	Voltage Rating	Current Rating①	I_{GT}	Critical dv/dt	t_q	V_{TO}	di/dt Rating	$
Edge Contouring	↑							↑
Emitter Shorting		↓	↑	↑				↑
Gold Doping②	↓	↓	↑	↑	↓	↑	↓	↑
Thinner n-Base	↓	↑			↓	↓	↑	
Multiple Gates			↑			↓	↑	↑
Better Cooling ④		↑		↑	↓			↑
Reduced Voltage Operation ④				↑				↑

① In each case it is assumed that silicon wafers having identical anode and cathode areas are being compared, with and without the parameter change shown.

② In addition to gold doping, other means of reducing minority carrier lifetime will have the same effect on the listed parameters except voltage rating may not be adversely affected by other methods.

③ This refers to current within the basic device rating which can be carried at a given case temperature. Changes in current rating are brought about by changes in the opposite direction of on-state voltage and power dissipation. Surge current rating will be affected in the same manner as current rating.

④ The user as well as the manufacturer can influence the cooling of the semiconductor junction and also the maximum voltage which will be applied to it.

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CALCULATION OF CURRENT RATING
AN-305

APPLICATION NOTE

CALCULATION OF RECTANGULAR WAVEFORM CURRENT RATING OF THYRISTORS

Most data sheets for reverse blocking, triode, power thyristors (silicon controlled rectifiers) give current ratings only for the case of a single phase (half wave) resistive load. These ratings are usually given in the form of curves showing the maximum allowable current vs. case temperature for various conduction angles such as 180, 120, 90, 60 and 30 degrees. These current waveforms are shown in Figure 1. It should be noted that the highest value of average current shown on the data sheet curves for each current waveform has an RMS value equal to the maximum RMS rating of the thyristor in question.

The designer quickly finds that in a great many applications current flow is nearly rectangular so that the above published ratings do not apply. For a given conduction period and average current value, the heating effect of a rectangular current wave is less than that of a multilated sine wave of equal conduction time, because the peak current is less. This can be seen from Figure 2. Thus, the thyristor current ratings for rectangular waveform current are greater for any given conduction period, and advantage should be taken of this.

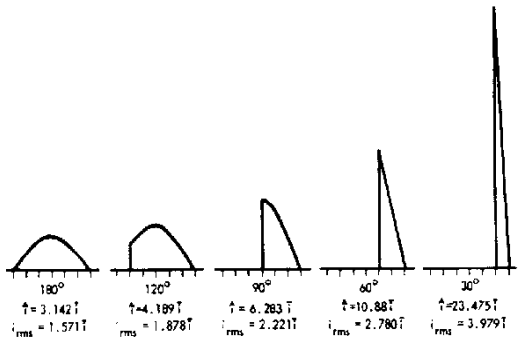


Figure 1 – Sinusoidal Current Waveforms of Equal Average Value but Different Conduction Angles

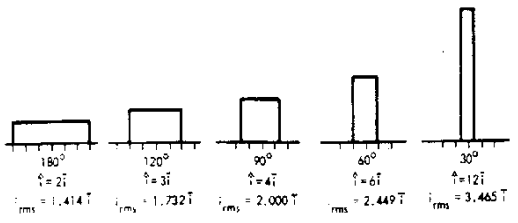


Figure 2 – Rectangular Current Waveforms of Equal Average Value but Different Conduction Periods

WHERE RECTANGULAR CURRENTS ARE ENCOUNTERED

The current waveshapes observed in single phase full wave (bi-phase) and polyphase rectifier units usually are more rectangular than sinusoidal. Load inductance tends to prevent rapid variations in load current, making the current waves flat topped. On the other hand, inductance in the ac supply (including rectifier transformer reactance) prevents instantaneous transfer (commutation) of current from one rectifying element to the next, resulting in overlapping current flow through the circuit elements that are commutating. The resulting current waveforms are illustrated in Figure 3. When phase retard is used in such rectifier equipment to control the average output voltage, the angle of current flow remains essentially fixed; the initiation of the current wave is simply delayed by the angle of phase retard, α, as can be seen from Figure 4. It is interesting to note that as α is increased, for a given value of load current, commutation takes less time so that the current waveform becomes more rectangular.

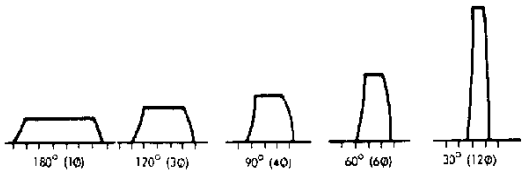


Figure 3 – Anode Current Waveforms of Rectifier Unit Having Inductance in AC Supply and Load

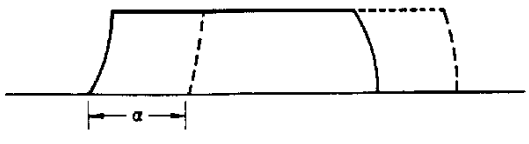


Figure 4 – Effect of Phase Retard, Angle α, on Anode Current Waveform in Rectifier Circuit

The duration of current flow (the conduction period) is determined by the rectifier circuit and not by the angle of phase retard. Conduction periods for common rectifier circuits are given in Table 1.

TABLE 1

Conduction Periods of Common Rectifier Circuits, Inductive and Resistive Loads

Circuit	Conduction Period
Single Phase Center Tap (bi-phase, single-way)	180°
Single Phase Bridge (double-way)	180°
Three Phase Wye (single-way)	120°
Three Phase, Double Wye with IPT (single-way)	120°
Three Phase Bridge (double-way)	120°
Six Phase Star (single-way)	60°
Twelve Phase Quadruple Zig-Zag (single-way)	30°

The current flow through thyristors in many inverter circuits also tends to be rectangular. The current flows through an inductance from a source having a fixed direct voltage and the thyristors serve to switch the current from one transformer winding to another; thus, essentially rectangular current waves result.

CALCULATION PROCEDURE

The calculation of thyristor current rating for rectangular waveform currents is not difficult. Basically, all the device data that are required is the on-state voltage (forward voltage drop) curve at maximum rated junction temperature, the transient thermal impedance curve for times between 1 and 10 milliseconds, and the rated thermal resistance of the device, junction-to-case. If a curve of instantaneous on-state power loss vs. instantaneous anode current is available this will simplify the procedure because it will not be necessary to calculate the instantaneous on-state power loss from the on-state voltage curve.

Junction temperature rise above case temperature can be calculated by the formula:

$$\Delta T_{J(JC)} = \frac{t_p}{\tau} \hat{P}_T R_{\theta JC} + \left(\hat{P}_T - \frac{t_p}{\tau} \hat{P}_T\right) Z_{\theta(t_p)}$$

$$= \hat{P}_T \left[\frac{t_p R_{\theta JC}}{\tau} + \left(1 - \frac{t_p}{\tau}\right) Z_{\theta(t_p)}\right] \qquad (1)$$

Where:

$T_{J(JC)}$ = Junction temperature rise above case temperature.

$\hat{P}_T$ = Peak on-state (triggered) power loss at a given peak anode current.

t_p = Duration of one rectangular wave of current (conduction period).

τ = Time interval between the start of one current pulse and the start of the next (the period, i.e., the reciprocal of the supply frequency).

$R_{\theta JC}$ = Thermal resistance of the thyristor, junction-to-case.

$Z_{\theta(t_p)}$ = Transient thermal impedance of the thyristor for the time duration of one current pulse.

In the above equation, the average junction temperature rise is calculated by the expression $t_p/\tau \cdot P_T \cdot R_{\theta JC}$ (average power dissipated times thermal resistance). To this is added a term which represents the temperature response of the junction in the final pulse of load current. This increment is calculated by multiplying the increment of power dissipated during the pulse which is greater than the average power dissipated, $(1 - t_p/\tau)\ P_T$, by the transient thermal impedance for the time of one current pulse, $Z_{\theta(t_p)}$. More complex expressions have been published for this temperature rise, but the above expression gives a conservative answer that is within a few degrees of the more precise value, and is far easier to calculate.

A further refinement is to allow for the heating effect of the losses during the reverse blocking and forward off-state periods. In power thyristors these losses generally are only a few watts, and so cause only a small additional temperature rise of 1 to 2 degrees Celsius (Centigrade).

Temperature Rise Above Cooling Fluid Temperatures

The equipment designer must know junction temperature rise above cooling fluid temperature (temperature of incoming air, water, oil, etc.), not simply junction temperature rise above device case temperature. The additional rise of the case above the cooling fluid is calculated by multiplying the total average on-state, off-state and reverse blocking losses by the thermal resistance from case to cooling fluid.

There are usually several thermal drops in series in the path of heat flow from case to cooling fluid, such as:

1. Thermal resistance from case to heat exchanger (often referred to as case to heat sink).

2. Thermal resistance from heat exchanger to cooling fluid.

Thermal resistance from case to heat exchanger is a function of the size of the thyristor base and presence or absence of silicone grease on the mating surfaces. Representative values are given in Table 2.

TABLE 2

Thermal Resistance, Case to Heat Exchanger

Size of Thyristor Case			Thermal Resistance to Heat Exchanger	
Hex Base	Threaded Stud	JEDEC No.	Dry	With Silicone Grease DC 100 or Equal
7/16"	10-32	TO-64	0.75°C/W	0.50°C/W
9/16"	1/4-28	TO-48	0.50°C/W	0.35°C/W
11/16"	1/4-28	TO-65	0.35°C/W	0.25°C/W
1-1/16"	1/2-20	TO-49, 83, 94	0.15°C/W	0.10°C/W
1-1/4"	3/4-16	TO-93	0.10°C/W	0.08°C/W
1-11/16"	3/4-16	–	0.05°C/W	0.04°C/W

Thermal resistance from heat exchanger to cooling fluid must be determined from the configuration and size of the heat exchanger used, the velocity of the cooling fluid, the surface finish of the heat exchanger, etc. The thermal resistance, device-mounting-surface-to-coolant, of the heat exchanger can be obtained from the heat exchanger manufacturer or from tests.

An expression for calculating junction temperature rise above cooling fluid temperature can now be written, taking into account the factors just discussed:

$$\Delta T_{J(JA)} = \left(\frac{t_p}{\tau}\hat{P}_T + \bar{P}_B\right)\left(R_{\theta JC} + R_{\theta CH} + R_{\theta HA}\right) + \hat{P}_T\left(1 - \frac{t_p}{\tau}\, Z_{\theta(t_p)}\right) \qquad (2)$$

Where:

$T_{J(JA)}$ = Junction temperature rise above ambient cooling fluid temperature.

$R_{\theta CH}$ = Thermal resistance, case-to-heat exchanger.

$R_{\theta HA}$ = Thermal resistance, heat-exchanger-to ambient.

$\bar{P}_B$ = Average power losses during reverse blocking and forward off-state periods.

(The other terms are the same as those for formula (1).)

The RMS value of the current rating calculated by the above procedures should not exceed the rms current rating of the thyristor being considered.

EXAMPLE

To illustrate the principles discussed above, consider a 70 Ampere (average), 110 Ampere (rms) thyristor operating in a three phase bridge rectifier circuit with inductive load. The on-state voltage and the transient thermal impedance curves for this device are given in Figures 5 and 6 respectively. Maximum thermal resistance, junction to case, is 0.30°C/Watt, and maximum rated junction operating temperature is 125°C. The device is mounted on an air cooled

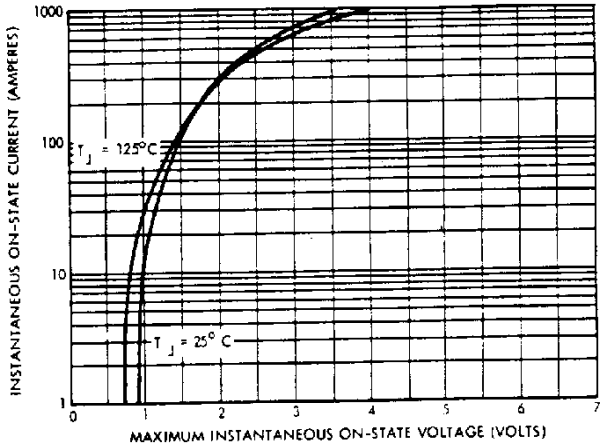


Figure 5 – Maximum Instantaneous On-State Voltage Vs. Instantaneous On-State Current

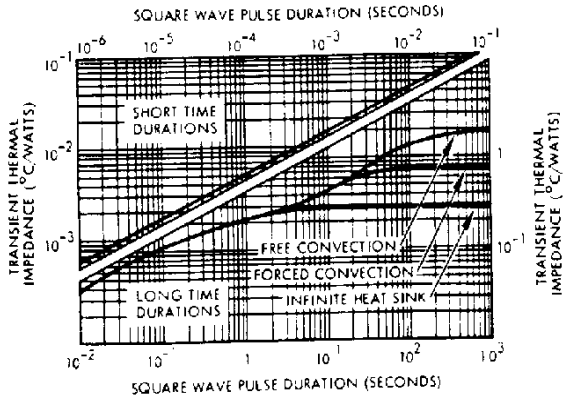


Figure 6 – Maximum Transient Thermal Impedance Vs. Square Wave Pulse Duration. Thyristor Mounted on 7 x 7 x .160" Copper Fin.

CALCULATION OF CURRENT RATING

heat exchanger having a thermal resistance to ambient air of 0.30°C/Watt at a cooling air velocity of 1000 lf/min. The maximum ambient air temperature in which the device is to operate is 45°C. The supply frequency is 60 Hz and therefore the supply period, τ, is 1/60 = 0.0167 seconds. From Table 1 the conduction period is seen to be 120 deg., or 0.0167 x 120/360 = 5.6×10^{-3} seconds, and from Figure 6 the transient thermal impedance for a square wave pulse of this duration is found to be 3.6×10^{-2} °C/Watt.

From Table 2 the thermal resistance from case to heat exchanger is seen to be 0.10°C/Watt (lubricated). The average power loss during the reverse blocking and forward off-state periods can be calculated from the maximum leakage current for the thyristor, which in this case is 5 mA. A value of 3 Watts is a conservative, worst-case estimate.

The above data may be used in equation (2) to solve for the peak power loss required to raise the peak junction temperature to 125°C:

$$\left(\frac{1}{3}\hat{P}_T + 3\right)\ (0.30 + 0.10 + 0.30)$$

$$+ \hat{P}_T\left(1 - \frac{1}{3}\right) 0.036 = 125 - 45$$

$$.257\,\hat{P}_T = 77.9$$

$$\hat{P}_T = 303\ \text{W}$$

From the on-state voltage curve for 125°C junction temperature the peak current producing this amount of power loss can be found (by successive approximations) to be: 303/1.68 = 180 Amperes. The maximum permissible average current is then 180/3 = 60.0 Amperes.

Referring to Figure 2, the RMS value of this current is 180/1.732 = 104A, which is within the 110A RMS rating of the thyristor in this example.

Simplifications

The manufacturer will usually publish a curve of on-state power loss vs. direct current, such as the dc curves shown in Figures 7 and 8. Such curves permit reading the value of permissible peak amperes directly without the need for calculating them from the on-state voltage curve.

If the manufacturer has provided curves of average on-state power loss for square wave operation, such as shown in Figure 8, the average current may be read directly by converting the peak power to average power. In the case of the example, the average power is 101 Watts, which is one third the peak power, since the conduction period is one third of a cycle (120 degrees). From the 120 degree curve in Figure 8 the average current is found to be 59 Amperes.

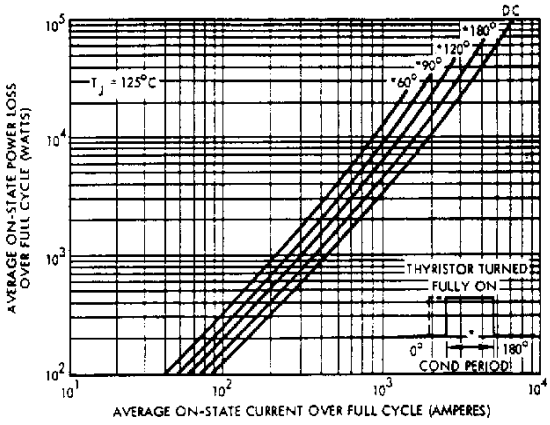


Figure 7 — Average On-State Power Loss Vs. Average On-State Current. Rectangular Waveform Current, High Current Levels.

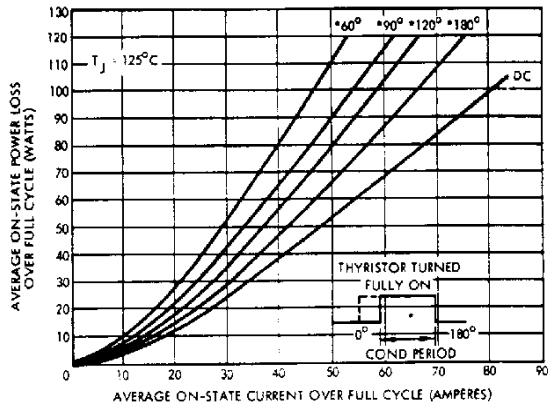


Figure 8 — Average On-State Power Loss Vs. Average On-State Current. Rectangular Waveform Current, Low Current Levels.

Using Rectangular Current Waveform Rating Curve

When the manufacturer provides curves of average on-state current vs. maximum allowable case temperature for rectangular current waves, such as the curves in Figure 9, calculations can be simplified even more. In this case the main step in determining the current rating is to calculate the temperature rise of the case above ambient due to the on-state losses, which is the product of these losses and the thermal resistance from case to ambient. Taking the previous example, this thermal resistance is 0.40°C/Watt. The average off-state and reverse blocking power losses are 3 Watts, and the temperature rise from case to ambient

CALCULATION OF CURRENT RATING

caused by these losses is 1.2 degrees. In effect, this raises the maximum allowable ambient temperature to 46.2°C. A current must now be found for which the maximum allowable thyristor case temperature, as read from Figure 9,

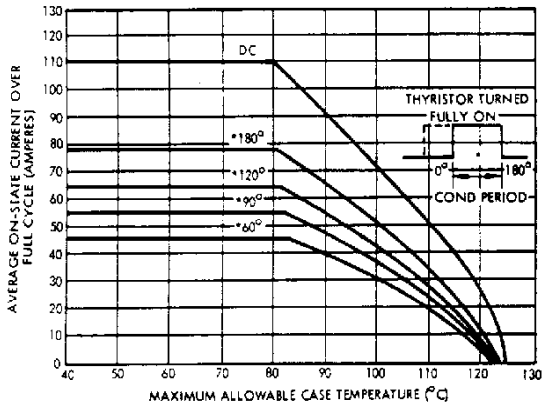


Figure 9 — Average On-State Currents Vs. Maximum Allowable Case Temperature. Rectangular Waveform Current.

will be just high enough to permit the average power generated in the thyristor to be dissipated to the cooling medium by the heat exchanger. This value of on-state current must be found by successive approximations. Since the answer in this case, 59 Amperes, has previously been calculated, the procedure can be illustrated by a single calculation:

Maximum case temperature permitted at 59 Amperes: 86.0°C (from Fig. 9).

Maximum temperature rise permitted between ambient and case at 59 Amperes:

$$86.0 - 45 + (3 \times 0.40) = 86.0 - 46.2 = 39.8^{\circ}C$$

Maximum average on-state power loss permitted:

$$\frac{39.8}{0.40} = 99.5 \text{ Watts}$$

Maximum average on-state current permitted: 58.5 Amperes (from Fig. 8).

This is essentially the same as the 59 Amperes used at the start of the calculation.

OVERLOADS

The manufacturer's data sheet provides a non-recurrent surge current rating, which may be imposed on the thyristor when it is operating at maximum rated current, voltage, and temperature conditions in a half-wave circuit. Following rated non-recurrent overload the thyristor is not expected to exhibit off-state blocking capability until its junction has cooled down to the maximum rated operating temperature. A fault sufficiently severe to cause an overload of this nature is not expected to be a normal operating condition, and a thyristor is not expected to be subjected to more than approximately 100 such faults during its useful life.

On the other hand, more moderate overloads are often encountered very frequently in rectifier equipments. These are known as recurrent overloads, and since they are of indeterminate number, they must not cause the thyristor junction temperature to be raised above the maximum rated operating temperature, if long thyristor life is to be assured. Consequently, a reduction in the continuous loading on the thyristor is required, to provide an additional temperature rise which can take place during the overload.

The required amount of this temperature rise margin depends upon the severity of the overloads and their durations.

Of the many possible overload schedules, one of the most common is that of a short overload following continuous loading. The following simplified formula, which is an extension of equation (2) may be used to calculate the junction temperature rise at the end of the overload:

$$\Delta T_{J(JA)} = \left(\frac{t_p}{\tau}\hat{P}_{T(SS)} + \bar{P}_B\right)(R_{\theta JC} + R_{\theta CH} + R_{\theta HA}) + \hat{P}_{T(SS)}\left(1 - \frac{t_p}{\tau}\right) Z_{\theta(t_p)} + \frac{t_p}{\tau}\left(\hat{P}_{T(OL)} - \hat{P}_{T(SS)}\right) Z_{\theta(OL)} + \left(\hat{P}_{T(OL)} - \hat{P}_{T(SS)}\right)\left(1 - \frac{t_p}{\tau}\right) Z_{\theta(t_p)} \quad (3)$$

Where:

$\hat{P}_{T(SS)}$ = peak steady state on-state power loss (prior to overload).

$\hat{P}_{T(OL)}$ = peak on-state power loss during overload.

$Z_{\theta(OL)}$ = transient thermal impedance of thyristor for overload period.

(The other terms are the same as those given for (1) and (2).)

Care should be taken in determining the transient thermal impedance for the overload period. A transient thermal impedance curve for the thyristor mounted on infinite heat sink may be used only over the range where the transient thermal impedance is no more than ninety percent of the maximum value given on the curve. For longer overloads

a transient thermal impedance curve for the device mounted on the heat exchanger actually being used is required. Two such curves are given in Figure 6 for the thyristor used in the example.

If a temperature rise margin, $\Delta T_{J(OL)}$, is provided for overloads when determining the steady state current loading of the thyristor, the recurrent overload which can be imposed can be found by solving the equation below for $\hat{P}_{T(OL)}$, the peak on-state power loss during the overload period:

$$\Delta T_{J(OL)} = (\hat{P}_{T(OL)} - \hat{P}_{T(SS)}) \left[\frac{t_p}{\tau} Z_{\theta(OL)} + 1 - \frac{t_p}{\tau} Z_{\theta(t_p)} \right] \quad (4)$$

Having found the maximum peak on-state power loss permitted during the overload period, the average current which can be carried during the overload period may be calculated as before.

Originally written by David W. Borst, International Rectifier, Semiconductor Division, El Segundo, California.
Originally published in Summer 1967 edition of Rectifier News by International Rectifier, El Segundo, California.

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Designing with IR2137

by Dorin O. Neacsu, Toshio Takahashi and Hoa Huu Nguyen

TOPICS COVERED

Brief description of the application circuitry
Considerations regarding the bootstrap stage
Establishing if IR2137 can be used directly to control an inverter
Criteria for design of the gate resistors
Conclusions

1. Brief description of the application circuitry

IR2137 is a three-phase gate driver with enhanced protection features such as desaturation for the high-side devices.

The usual application circuitry is presented in Fig.1. It shows the communication link with the microcontroller stages through the *PWM* signal as well as the *Fault* and *Clear_Fault* signals. This stage needs a 5V power supply.

The operation mode of the *Desat* function or over-current protection (*ITRIP*) are not detailed in this design tip as they are presented in a separate technical paper.

This design tip is trying to address the questions regarding the applicability of the IR2137, the particular design of the bootstrap stage when applied within different PWM converters, to the design of the gate resistors as well as to the grounding issues.

2. Considerations regarding the bootstrap stage

IR2137 is delivering the control pulses for three-phase inverters that are working under a PWM algorithm. There are different types of PWM algorithms that are currently used by industry. Any particular PWM algorithm defines different values of the minimum and maximum pulse-widths. Since the bootstrap capacitor only charges when the low-side device is on, the duration of this interval should be high enough to ensure the rise of capacitor voltage to VCC.

Denoting by R the resistor on the charging path of the bootstrap capacitor (diode plus additional current-limiting resistor), the voltage across the capacitor is given by:

$$v_C(t) = [V_{CC} - V_f - V_{LS}] \cdot \left[1 - \exp\left(-\frac{t}{R \cdot C}\right)\right] \quad (1)$$

and the on-time of the lower IGBT (considered as charging time) should be enough for charging-up the capacitor above the minimum allowed voltage for proper operation of the high-side circuitry within the IR2137, that is 11.3V when VCC=15V.

Taking account of the possible discharge of the capacitor during the high-side IGBT conduction, one can restrict the level of the desirable voltage at the end of the charging interval at 90%. It yields:

$$[V_{CC} - V_f - V_{LS}] \cdot 0.90 = [V_{CC} - V_f - V_{LS}] \cdot \left[1 - \exp\left(-\frac{(t_{on}^L)_{\min}}{R \cdot C}\right)\right] \quad (2)$$

OR

$$(t_{on}^L) \geq -R \cdot C \cdot \ln[0.1] = 2.3 \cdot R \cdot C \quad (3)$$

By contrast, the bootstrap capacitor should sustain the gate current during turn-on and during the “on” state of the high-side IGBT. The value of the capacitor should correspond to the duration of this interval. In other words, the charge acquired during the on-state of the low-side IGBT should be enough to compensate for the charge needed by the high-side device. The usual equation for designing C is [1]:

$$C \geq \frac{2 \cdot \left|2 \cdot Q_G + [I_{qbs(\max)} \cdot t^H{}_{on}] + Q_{ls} + [I_{Cbs(leak)} \cdot t^H{}_{on}]\right|}{[V_{CC} - V_f - V_{Ls}] - V_{\min}} \quad (4)$$

where V_{min} should stay above 11.3V. Moreover it is suggested to choose a much larger value for a safer design.

It is recommended to use a resistor in series with the bootstrap diode. This resistor brings benefits in:
- correcting the time constant (both with C);
- limiting the charging current at start-up;
- limiting the current through the bootstrap circuit during possible negative V_s spikes. Both capacitor terminals are trying to follow the V_s negative spikes. Both capacitor terminals are trying to follow the V_s negative spike and this can turn-on the bootstrap diode allowing a current through R.

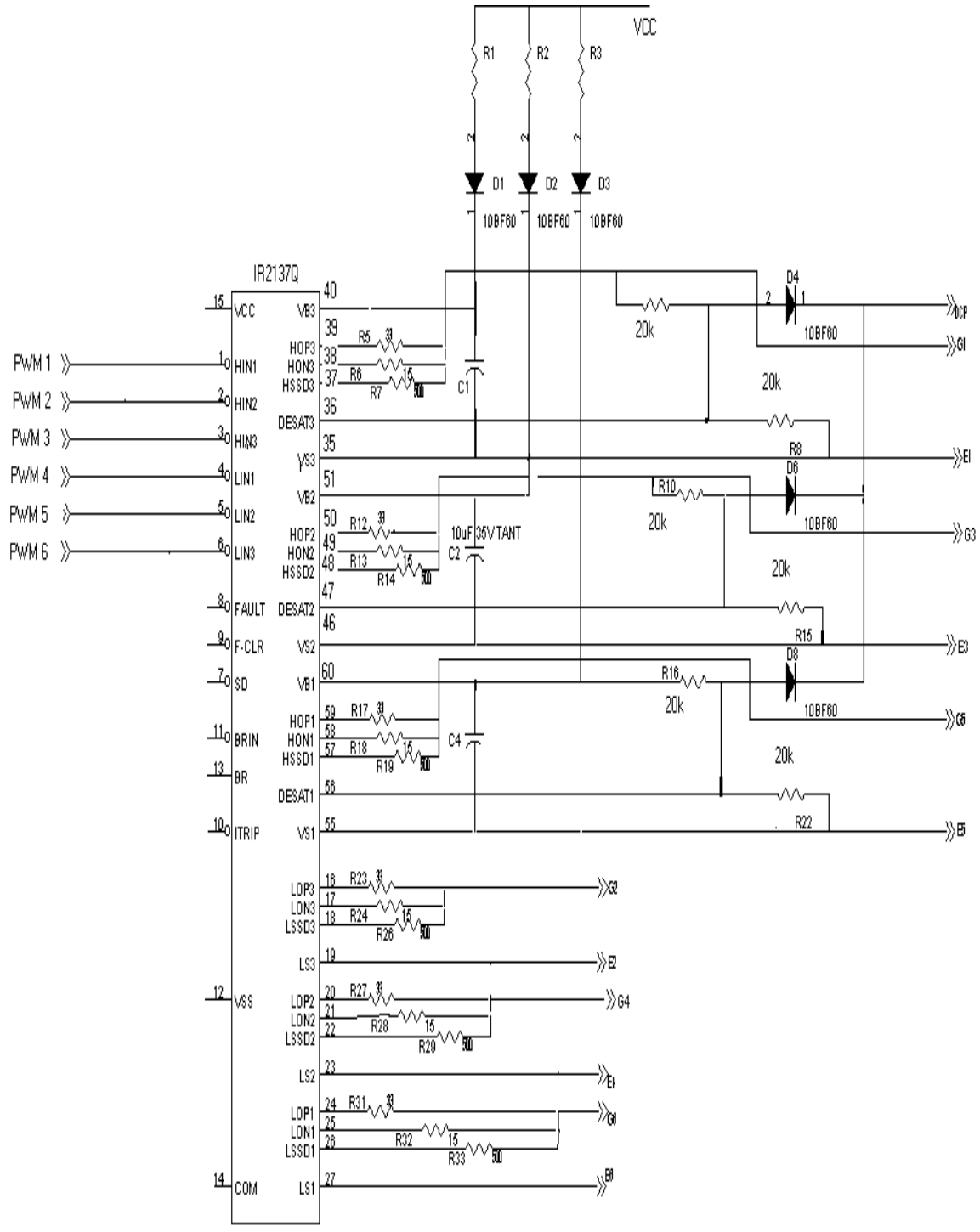


Figure 1: Basic application circuitry of the IR2137

Some measured values of the negative VB-COM spike for different situations are:

	malfunction (still working)	latched (destructive)
Low-side = ON, High side = OFF		
Pulse-Width = 500ns	7V	40V
Pulse-Width = 1us	6V	25V
Low-side = OFF, High side = ON		
Pulse-Width = 500ns	8V	52V
Pulse-Width = 1us	7V	19V

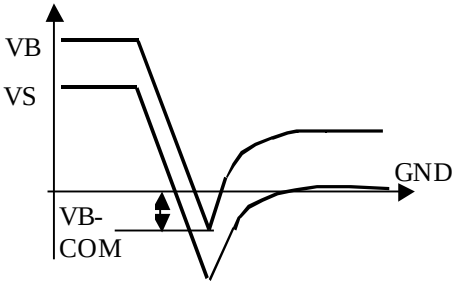


Figure 2: Vs spike definition

Since the three-phase inverters are using PWM algorithms that produce different time variations of the pulse width (t^H_{on} or t^L_{on}), designing a bootstrap capacitor should consider in eq.(3) and (4), the maximum value of the t^H_{on} and the minimum value of the t^L_{on} depending on the PWM method and output fundamental frequency.

Figure 3 presents an example of some possible evolutions of the t_{on} for PWM methods most used by industry.

It can be seen that the bootstrap method can successfully be used within sinusoidal PWM and Space Vector PWM and that there are some problems when used within 2-phase PWM (discontinuous PWM algorithms). Within these methods, the upper or lower IGBT is not switched for long time intervals (120 or 60 degrees) and this makes almost impossible the use of bootstrap capacitor method at low frequencies. Using the traditional inverter switching notations, a possible

Figure 3: Evolution of the pulse-width for different PWM algorithms

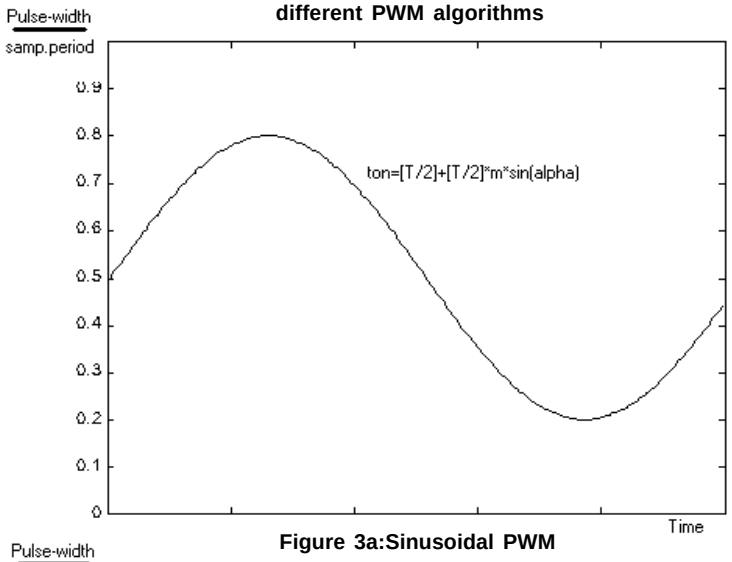


Figure 3a:Sinusoidal PWM

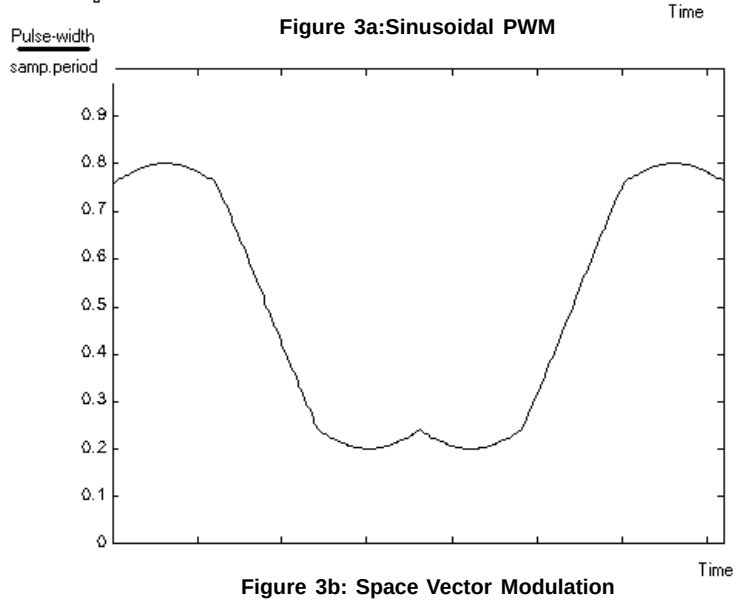


Figure 3b: Space Vector Modulation

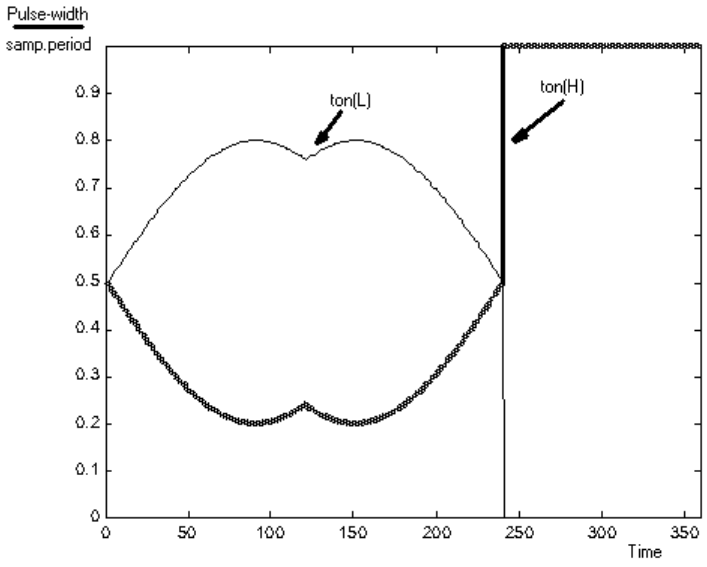


Figure 3c: 2-ph Modulation-A (t^{H}_{on} and t^{L}_{on})

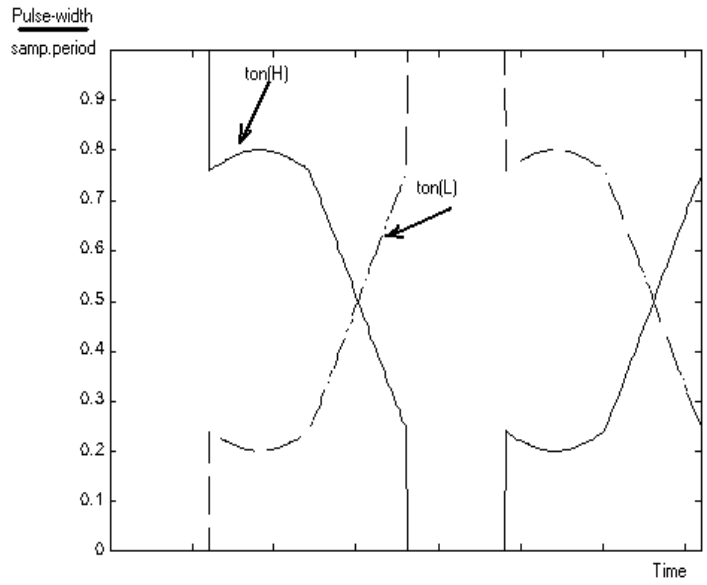


Figure 3d: 2-ph Modulation-B (t^{H}_{on} and t^{L}_{on})

sequence could be: … - 111 - 110 - 010 - 110 – 111 - ... with no switchings of the upper IGBT for 60 or 120 degrees (as shown in Figs.3c and 3d).

However, the discontinuous PWM algorithms demonstrate the advantage of lower inverter losses and many industrial applications take advantage of them. In order to be able to use these methods along with bootstrap capacitor method, the IGBTs should be switched periodically during the no-switching intervals. This means use of 000 state from time to time in low frequency range.

The bootstrap diode is designed based on V_{RRM} and I_F [1]. We recommend choosing diodes with τ_{RR}=50ns.

3. Establishing if IR2137 can be used directly to control an inverter

The first major requirement consists of the gate drive power level. During switching, the IGBT takes power from the gate drive power supply. The amount of the used power is a function of the operating frequency, on and off bias voltages and total gate charge. If we assume that IR2137 is infinitely fast and that its output impedance and inductances are negligible, the average current that must be supplied by the gate drive is:

$$I_G(peak) = \frac{V_{GG}}{R_{G\min}} \qquad (5)$$

The maximum gate currents should be provided under gate output short-circuit conditions and can be 220mA (R_{inIC}=30ohm) at turn-on and 460mA (R_{inIC}=16ohm) at turn-off.

Furthermore, the IR2137 is able to furnish a positive gate voltage only. Performance requirements as (dv/dt) induced shoot-through current, maximum allowable peak current, the desired (dv/dt) of the output phase voltage or power losses within diode and IGBT are considered to designing with IR2137.

The biggest concern when using IR2137 to control IGBT's gate with only positive voltage is related to the shoot-through current that can appear due to (dv/dt) of the turning-on device.

The values of the R_{GON} and R_{GOFF} gate resistors as well as the gate voltage represents degrees of freedom to obtaining desired performance.

Large R_{GON}	decreased EMI by increasing the turn-on time and decreasing the di/dt; decrease I peak and Vpeak during diode recovery
Small R_{GON}	decrease the turn-on losses
Large R_{GOFF}	improve the voltage rise time
Small R_{GOFF}	decrease the dv/dt sensitivity

In order to understand the effects of the Rg resistor, some sample experimental results are next included for an inverter leg equipped with IRG4PH40KD IGBT+D working at 9A (Rgon=Rgoff).

Rg (on/off)	5	30	100	200
dv/dt(off) [V/ns]	6.5	7.2	4.7	3
dv/dt(on) [V/ns]	14	10	6	3.8

4. Criteria for design of the gate resistors

Design of the gate resistors values can be done based on two criteria:

A. efficiency optimization snubberless design

B. low-cost snubberless design with good dynamic performance.

A. Efficiency optimization criteria

Since the gate resistors values are influencing the turn-on, turn-off and conduction losses of IGBT and diode, efficiency optimization can be a design criterium. Equations for power losses are presented in [3]. The main optimal problem consists in choosing between a large value of the gate resistor that would reduce the diode losses and a small value of the gate resistor would reduce the IGBT switching losses. Since there is a difference in the thermal conductivity of the diode and IGBT the optimal problem can be analyzed based on a weighted optimization function:

$$E = \frac{R_{thT} \cdot P_T + R_{thD} \cdot P_D}{P} \qquad (6)$$

B. Good dynamic performance

A low-cost design can be carried out based on simplified constraints as:

- gate driver providing positive voltage only;
- limited available gate peak current;
- minimum ensured (dv/dt)on
- minimum ensured (dv/dt)off
- maximum allowable peak voltage
- avoiding cross—conduction.

The details and equations for each condition can be found on [2].

R_{GON} can be chosen to respect both the design constraints corresponding to the minimum turn-on time (dv/dt) and maximum allowable peak voltage during recovery. However, one can choose within the available surface $R_{GON}(I_L,V_{GE})$, the highest available value of the resistance in order to limit the value of the necessary peak gate current.

R_{GOFF} results from an optimal design involving the condition for avoiding cross-conduction and minimization of turn-off (dv/dt). Once again, a larger value reduces the peak current requirements for the gate driver.

5. Conclusion

This paper presents some design hints for the three-phase gate driver IR2137. This power IC requires bootstrap supplies of the high-side gate drivers and can allow different gate resistors for turn-on and turn-off. Basic design considerations for these functions are detailed herein.

Notations

Q_G - *Gate charge of the high-side IGBT*
$I_{Cbs(leak)}$ - *Bootstrap capacitor leakage current*
Q_{Ls} - *level-shifter(IC) charge required per cycle*
V_{Ls} - *Voltage drop across the low-side IGBT*
t^H_{on} - *Duration of the high-side IGBT on-state*
t^L_{on} - *Duration of the low-side IGBT on-state*
P_T - *Loss power in IGBT*
P_D - *Loss power in diode*
P – *Total output power*
R_{thT} – *Thermal resistance of the IGBT*
R_{thD} – *Thermal resistance of the diode*

REFERENCES

[1] IR IC Designer Manual, DT 98-2
[2] IR IGBT Designer Manual, AN988, AN990
[3] IR IGBT Designer Manual, TPAP-1

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Using IR2171/IR2172 within DSP-controlled AC Drives

By Dorin O. Neacsu

TOPICS COVERED

Description of the control system including the linear current sensing ICs
Using Texas Instruments TMS320C240 DSP
Hardware description
Software description
Open-loop results

1. DESCRIPTION OF THE CONTROL SYSTEM INCLUDING THE LINEAR CURRENT SENSING ICs

Many applications require a three-phase AC drive ranging from hundreds of W to few MW. All of these cases are based on a three-phase inverter controlled by a microcontroller or DSP system. Measurement of at least two phase currents is desired in more advanced systems that are employing Field-Orientation Control of induction or synchronous machines.

There are several methods generally used for measurement of inverter currents:

- shunt resistors on the phase currents followed by linear optocouplers;
- Hall effect current sensors used on the phase currents;
- shunt resistors on the DC link current followed by an OpAmp and extensive reconstruction hardware/software.

IR2171/IR2172 are a promising alternative to these methods and they are based on sensing the phase currents through an external shunt resistor and transfer of the signal to the low side after converting it from analog to digital. The level shift function is realized using IR's high-voltage isolation technology. The output signal is a carrier pulse-width modulated wave with *fc* around 40kHz that can interface to a microcontroller system directly or through a galvanical separation. The duty ratio varies according to the shunt resistor voltage up to ±260mV.

This new approach has inherent advantages over the previous solutions in reduced cost and size as well as the possiblity of using the microcontroller system on the same ground level as the power system (especially in low power applications). Design note introduces the IR2171/IR2172 by explaining their use

as current measurement system within a micro-controlled AC drive. The *Texas Instruments TMS320F(C)240* has been chosen as an example due to its simple interface. Both system interface and software are explained and performance is analyzed based on some results that are finally detailed.

The PWM signal is applied to a counter input and the pulse widths are transformed in digital code by counting at the microcontroller clock frequency. The temperature drift of the output carrier voltage can be cancelled by measuring both intervals corresponding to the low and high level. A software routine is expected to calculate the duty ratio and to transform this data into an equivalent current value.

2. Using TMS320C(F)240 DSP

Texas Instruments TMS320C(F)240DSP is a good performing computing engine with rich peripherals designed for AC motor drive applications. The Field-Orientation control structure based on this DSP contains

- the Event Manager for the generation of the Space Vector PWM signals;
- 2 capture channels for the encoder.

The other two channels of the capture unit are herein used to the phase current measurement.

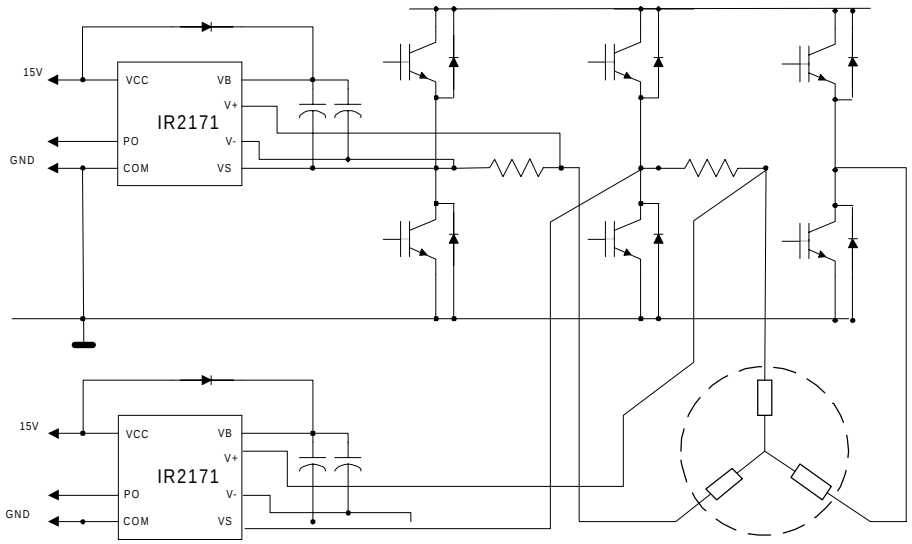


Figure 1 - IR2171 current measurement in a three-phase inverter drive

In this respect, a timer is selected to count at the CPU clock frequency of 20 or 30MHz and the counter content is saved into a stack at transitions on the capture input pins. The latency from a transition happens on an input pin and the moment the counter value is locked is 3.5-4.5 CPU clock cycles.

Since it is likely to measure both active and inactive state intervals, the timer content should be saved at both rising and falling edges. Unfortunately, the DSP system does not allow to separate the capture event from the interrupt generation event. In other words, we cannot capture both transitions

and ask the capture unit to generate an interrupt for reading data at each second transition. When employing interrupts on both edges, there is not enough time to serve those interrupts and to perform the main Field-Orientation control program. There would be 2 interrupts at each *1/fc* for each current measurement, each interrupt service routine lasting for at least 2µs. The DSP utilization factor would therefore be seriously affected.

Another possible problem is related to the minimum pulse width that is basically 2 µs, but can reach its minimum of τmin=1.87µs due to technological dispersion.

The delay between the interrupt request and its service is composed of:

- the synchronization time it takes for the interrupt to be recognized by the peripheral interface and converted into a request to the DSP. It takes:
  - **2 clock cycles** for internal interrupts
  - **4 clock cycles** for external interrupts.
- the CPU response time to recognize and acknowledge the enabled interrupt request. The minimum latency is **4 clock cycles** and longer for multicycle operations (memory access using wait states, repeat loops, pipeline operation, or serving other interrupt before the interrupts are unmasked again).
- the time needed by ISR to branch to get the specific event that produced the interrupt. possible case leads to minimum **4 clock cycles**.
- the time needed by the software routine designed to serve the interrupt to save the status registers, accumulator and sometimes other registers before doing the expected stack readings, savings of data to memory and other calculations. Minimum time expected for this interrupt routine initialization is **6 clock cycles**.

The overall time necessary to save the capture unit data to memory is very close to the value of the minimum pulse width of the input PWM signal.

Noticing these allows us to propose a solution based on having only one interrupt for each period (around 40kHz) at each falling edge of the capture input signal. During the appropriate interrupt servicing routine, the last two values of the capture stack are read and minor calculations are employed to defining the pulse widths. Such interrupt can be requested by a separate input of the DSP and acting as an external interrupt. The interrupt latency is about the same in this approach when compared to the solution of having two interrupts at each sampling interval, interrupts caused by the capture unit itself. However, the DSP utilization factor is improved allowing further development such as Field-Oriented Control or sensorless control.

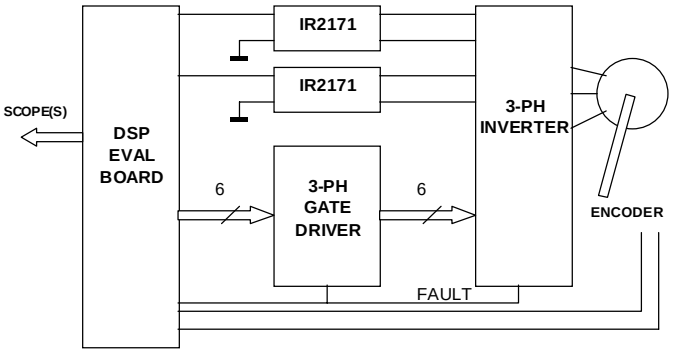


Figure 2 - Block diagram of the control system

3. Hardware description

The interface of the two IR2171 devices with the DSP is shown in Fig.2. The TMS320C24x DSP controllers evaluation module has been used for testing the current acquisition. *Table I* provides some information about the interface with IR2171, but the power supply, clock and usual circuitry is not included.

Name of the signal		DSP TMS320C240 pin	Eval.board connector
PWM outputs to be connected to the inverter gate drivers	PWM1/CMP1	94	P1-pin3
	PWM2/CMP2	95	P1-pin4
	PWM3/CMP3	96	P1-pin5
	PWM4/CMP4	97	P1-pin6
	PWM5/CMP5	98	P1-pin7
	PWM6/CMP6	99	P1-pin8
Fault signal	PDPINT	52	P1-pin26
Encoder signals	CAP1/QEP1	67	P1-pin21
	CAP2/QEP2	68	P1-pin22
2171-ph.A	CAP3/QEP3	69	P1-pin23
2171-ph.B	CAP4/QEP4	70	P1-pin24
2171-ph.A	XINT2	54	P4-pin19
2171-ph.B	XINT3	55	P4-pin20
Scope-ch.1	DACOUT0	-	P2-pin25
Scope-ch.2	DACOUT1	-	P2-pin26
Scope-ch.3	DACOUT2	-	P2-pin27
Scope-ch.4	DACOUT3	-	P2-pin28

Table I

4. Software description

This section describes the software routines that could be included in any control software for a 3-phase motor drive in order to make use of the IR2171 for current measurements.

This solution is not unique and it is presented herein as a test example. Moreover, only those parts of code that refer to the capture unit configuration and current calculations are included herein.

```
;********* initialization of variables ————————————————-
……
;******** Vector address declarations   ********************************
             .sect   ".vectors"
RSVECT        B      START   ; PM 0    Reset Vector          1 ;00
INT1          B      CRT_ISR  ; PM 2    Int level 1           4 ;02
INT2          B      PWM_ISR  ; PM 4    Int level 2           5 ;04
INT3          B      PHANTOM  ; PM 6    Int level 3           6 ;06
…..
       .text
```

```
;********* M A I N   C O D E  - starts here    ************************
START: ……..
;*********   SYSTEM CONFIGURATION         *********************************
…..
              LDP    #04h          ;
              MAR    *,1           ;
              LAR    AR0,#initar   ;
……..
;********* CONFIGURE EVENT MANAGER   ——————————————-
; Configure I/O pins as capture units ——————————————-
              LDP    #0E1h         ;
              SPLK   #0FF00H,OPCRA ;
              SPLK   #00F0H,OPCRB  ;
;********* INITIALIZE EVENT MANAGER   ——————————————-
              ……..
;——— Configure CAPCON and enable capture operation ———————-
              SPLK #1001101000001111b,CAPCON    ;
;——— External digital inputs used for interrupting at current measurement
              LDP    #0E0h                ;
              SPLK #1000000000000001b,XINT2_CNTL;
              SPLK #1000000000000001b,XINT3_CNTL;
……..
;********* Main background loop   ************************************
MAIN          LDP    #04h          ;
              NOP                  ;
              NOP
              B      MAIN          ;
;********* Routine Name: P W M _ I S R   *************************
PWM_ISR:      CLRC   INTM          ;
              SST    #0,stk1               ; save ST0 - Forced Page 0
              SST    #1,stk2               ; save ST1 - Forced Page 0
              LDP    #00h          ;
              SACL   stk3   ; save ACCL
              SACH   stk4   ; save ACCH
              LDP    #0E8h         ;
              SPLK   #0FFFFh,IFRA  ; Clear all Group A interrupt flags
;******** Phase Current calculation - Phase A = IaDelta2/[IaDelta1+IaDelta2]
              LDP    #04h          ;
              LACC   IaDelta2      ;
              ADD    IaDelta1      ;
              SACL   GPR2          ;
              ZALR   IaDelta2      ;
              RPT    #15           ; Place 16-bit pos. divisor in data memo
              SUBC   GPR2          ; Execute SUBC for 16 times
                                   ; L-ACC=quotient and H-ACC=remainder
              SACL   Ia            ; Save ‘Ia’ in D0 format (norm.)
;******** Phase Current calculation - Phase B = IbDelta1/[IbDelta1+IbDelta2]
              LACC   IbDelta2      ;
              ADD    IbDelta1      ;
              SACL   GPR2          ;
              ZALR   IbDelta2      ;
              RPT    #15           ; Place 16-bit pos. divisor in data memo
              SUBC   GPR2          ; Execute SUBC for 16 times
                                   ; L-ACC=quotient and H-ACC=remainder
              SACL   Ib            ; Save ‘Ib’ in D0 format (norm.)
……..
```

```
;******** configure DAC for scope *********************************
              LDP    #04h          ; Set data page pointer to 0000h
              LACC   Ia,12         ;
              SACH   DAC0_VAL      ; Load Ta to channel 1 of DAC
              LACC   Ib,12         ;
              SACH   DAC1_VAL      ; Load Tb to channel 2 of DAC
              LACL   IaTime1       ;
              SACL   DAC2_VAL      ; Load Tc to channel 3 of DAC
              LACL   IaTime2       ;
              SACL   DAC3_VAL      ; Load Tc to channel 3 of DAC
              OUT    DAC0_VAL,0000h       ; Write to the DAC0 register
              OUT    DAC1_VAL,0001h       ; Write to the DAC1 register
              OUT    DAC2_VAL,0002h       ; Write to the DAC2 register
              OUT    DAC3_VAL,0003h       ; Write to the DAC3 register
              OUT    DAC3_VAL,0004h       ; Start DAC conversions by writing DAC
update reg.
;********* Restore regs   ———————————————————
              LDP    #00h          ;
              ZALH   stk4          ; restore ACCH
              ADDS   stk3          ; restore ACCL
              LST    #1, stk2      ; restore ST1
              LST    #0, stk1      ; restore ST0
              RET                  ;
;********* Routine Name: C R T _ I S R   **********************
CRT_ISR       SST    #0,*-         ;
              SST    #1,*-         ;
              LDP    #0E0h         ;
              BIT    SYSIVR,13     ;
              BCND   Ib_ISR,TC     ; If TC=1, run XINT3_S_ISR (Ib)
Ia_ISR        LDP    #0E8h         ; Set data page pointer to 7400h
              LAR    AR6,FIFO3     ; Read the old stack data to AR6
              LAR    AR7,FIFO3     ; Read the newer stack data to AR7
              SACL   *-            ;
              SACH   *-            ;
              CLRC   INTM          ;
              LDP    #04h          ;
              SAR    AR6,IaTime1   ; Save first reading to ‘IaTime1’
              LACC   IaTime1       ;
              SUB    IaTime2       ;
              SACL   IaDelta1      ; Calculate the ‘off’ time.
              SAR    AR7,IaTime2   ; Save second reading to ‘IaTime2’
              LACC   IaTime2       ;
              SUB    IaTime1       ; Calculate the ‘on’ time
              SACL   IaDelta2      ;
              B      SAVEREG       ;
Ib_ISR        LDP    #0E8h         ; Set data page pointer to 7400h
              LAR    AR4,FIFO4     ; Read the old stack data to AR6
              LAR    AR5,FIFO4     ; Read the newer stack data to AR7
              SACL   *-            ;
              SACH   *-            ;
              CLRC   INTM          ;
              LDP    #04h          ;
              SAR    AR4,IbTime1   ; Save first reading to ‘IbTime1’
              LACC   IbTime1       ;
              SUB    IbTime2       ;
              SACL   IbDelta1      ; Calculate the ‘off’ time
              SAR    AR5,IbTime2   ; Save second reading to ‘IbTime2’
              LACC   IbTime2       ;
              SUB    IbTime1       ;
              SACL   IbDelta2      ; Calculate the ‘on’ time
```

```
SAVEREG     SETC   INTM          ;
            MAR    *+,AR0        ;
            LACC   *+,16         ;
            ADDS   *+            ;
            LST    #1,*+         ;
            LST    #0,*          ;
            CLRC   INTM          ;
            RET                  ;
```

5. Results

Several tests have been made in order to validate both hardware and software. In the beginning, open-loop tests have been carried out by applying pure sinusoidal input signals to the IR2171/2172 development board. Most of the waveforms are obtained by reconstruction through 12-bit D/A converters. The data is sent to this converter when currents are calculated by DSP from input data during the interrupt routine for inverter switching PWM generation that occurs at each 4kHz. Effects of sampling could be noticed in most waveforms. However, they are inherent in a digital system and provide information about the real data used by the control loop. The worst case shows a delay of 38µs that corresponds to 13.68º for 1kHz input signal. This delay is measured from the original sinusoidal signal to the left-end point of each S/H level and it contains not only IR2171 phase delay (about 10º phase shift) but also delay due to DSP internal S/H.

5-A Waveforms (Fif. 3)

Trace 3 (up) = input signal
Trace 4 (mid)=2171 to DSP signal (40kHz)
Trace 2 (dwn)= signal reconstructed through the D/A conv.

5-B Phase delays (Fig. 4)

Trace 3 = input signal
Trace A = DSP signal

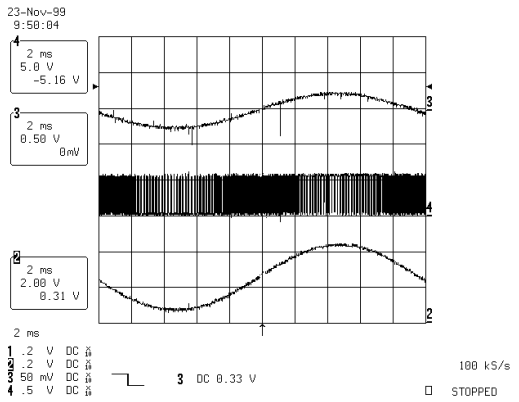


Figure 3a
Input signal: freq.=50Hz, amplitude of 240mV

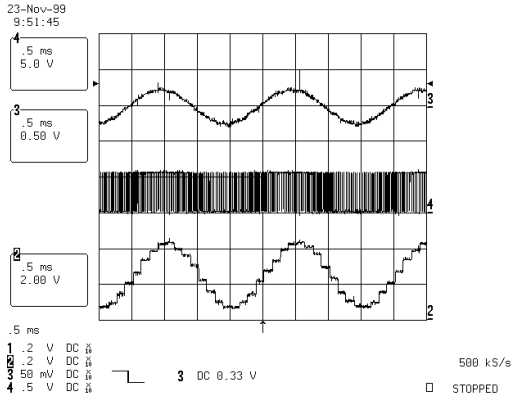


Figure 3b
Input signal: freq.=500Hz, amplitude of 240mV

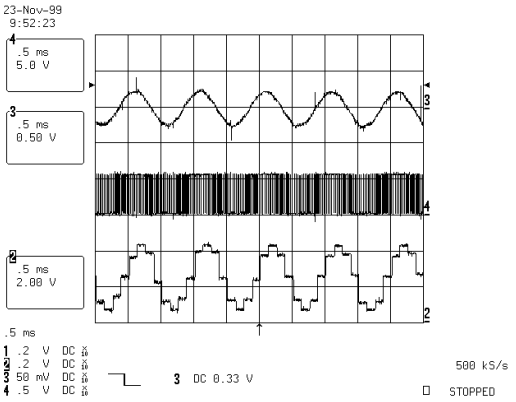


Figure 3c
Input signal: freq.= 1kHz, ampl. of 240mV

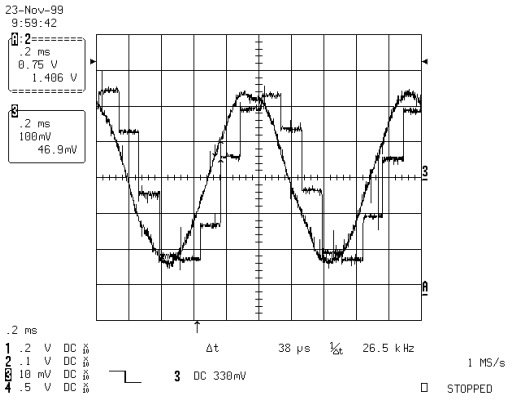


Figure 4
Phase delay measurement for 1kHz signal

5-C Capture operation

A better understanding of the counter operation and capture units can be achieved by looking at the Fig.5. Both low and large duty ratio cases are presented. One has to keep in mind that the internal counter counts up to *0FFFFh* (16 bits) while the D/A converter allows us to see 12 bits only. As a result, the counter content would look truncated on the scope. This, however, does not affect the meaning of these waveforms. Also, the D/A signals are output during the very fast interrupt routine that occurs during current acquisition (at about 40kHz). Figure 5 presents:

Trace 3 (up) = input signal
Trace 4 (mid) = 2171 to DSP signal (40kHz)
Traces 2,1 (down) = counter at reading time

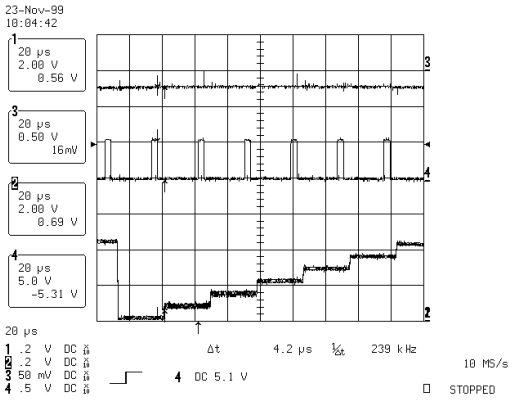


Figure 5a Low duty ratio

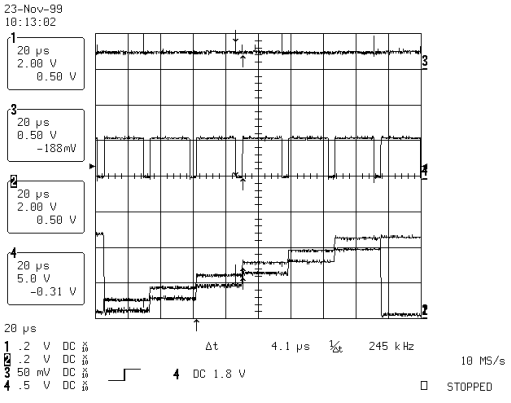


Figure 5b Large duty ratio

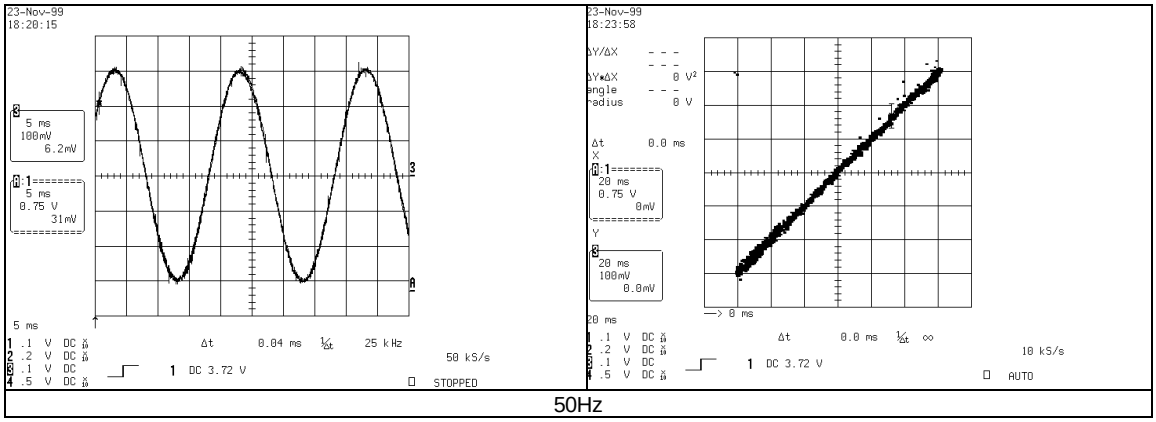
5-D Transfer characteristics

Trace 3 (up) = input signal

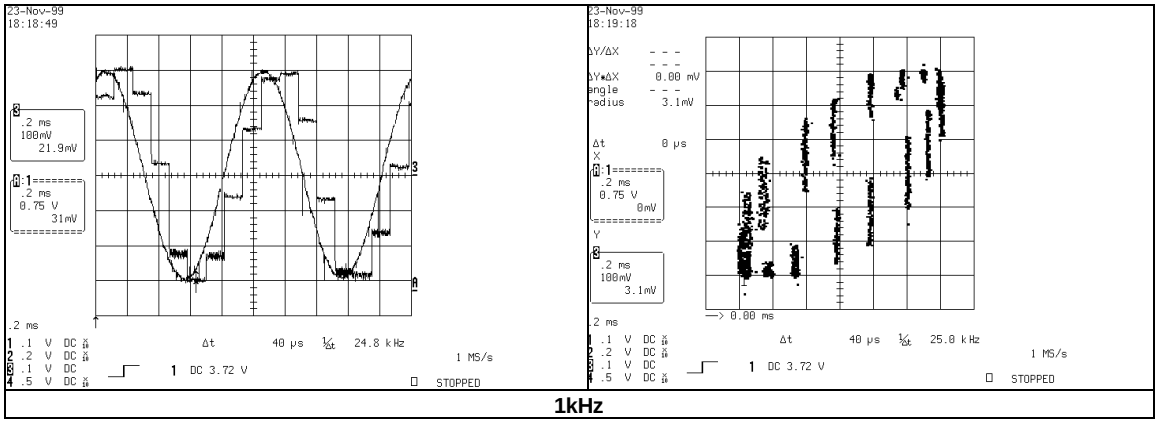
Trace A (down) = signal reconstructed through the D/A converter

The IN/OUT characteristics are presented at two different frequencies (50Hz and 1kHz) and it is possible to see the effect of sampling the current measurement at the PWM frequency.

The same characteristics are plotted as X-Y functions they are allowing us to observe their linearity.



50Hz



1kHz

Figure 6 Transfer characteristics

5-E Operation at overvoltage

When the shunt resistor voltage is higher than the allowed maximum voltage at the IC input, IR2171/2172 automatically limits the pulse width and the resulting reconstructed signal is shown in Fig.7.
Trace 2=input voltage
Trace 3=D/A result

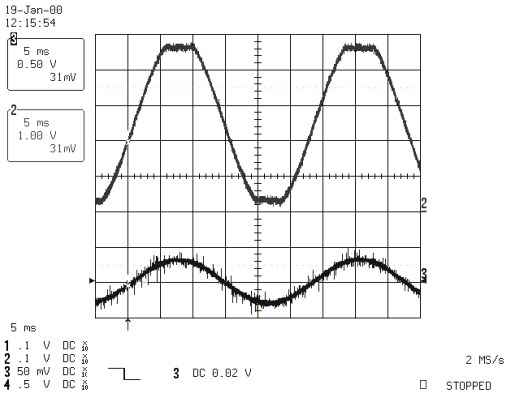


Fig.7 Voltage limitation at IR2172(40kHz). Results for 36Hz and 300mV

6. CONCLUSION

The suitability of IR2171/2172 to the DSP-controlled three-phase AC drives is herein demonstrated and a possible software implementation of the phase current measurement is detailed

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Alleviating High Side Latch on Problem at Power Up

By Toshio Takahashi and Hoa Huu Nguyen

TOPICS COVERED

Introduction
Typical Application Problem
Recommended Solution
Conclusion

I - INTRODUCTION

In a typical IR2xxx high voltage IC application with bootstrap power supply, the bootstrap capacitors are charged before the system becomes operational. In the process of charging up the bootstrap capacitor prior to establishing the high side supply voltage, if the high side output inadvertently turns on and stays on, it may cause a shoot through and may damage the IGBT devices. Even though the data sheet does not specify this power up transient case, the startup behavior is crucial for motor drive applications.
In general, the high side outputs of most of our control IC products rely on the high side Under Voltage Lock out circuit (UVBS) during power up to stay low during the power up. Under a combination of certain overstress and startup conditions, however, the high side output can inadvertently turn on and such an operating condition must be avoided.

II - TYPICAL APPLICATION PROBLEM

The high side output could latch on during a power up sequence in the system if a combination of the following conditions takes place:

1. No load condition (no motor lead connection to each VS nodes): The voltage at Vs node could be anywhere between the positive and the negative DC bus prior to charging the bootstrap capacitor.
2. High dVbs/dt: Fast charging of the bootstrap capacitor.
3. Vbs is biased at a negative voltage prior to power up.

An AC motor drive system which uses a high voltage IC with bootstrap power supply initially goes through a power up sequence in which the bootstrap capacitors are charged up. Figure 1 shows a typical power up sequence. The following description assumes the three conditions listed above:

At start up, the units go through several stages before the drive is ready for normal operation. One of these stages involves charging up the bootstrap capacitor by turning on the low side IGBT devices. When the VS node is pulled down to the ground from high voltage floating node, the bootstrap capacitor charges through the bootstrap diode as shown in Figure 2. At this moment, if the conditions mentioned above are all met, the following events could occur:

- Vbs is charged at a very fast rate when the low side outputs are turned on.
- The whole high side circuit is biased to the negative DC bus at a very fast rate of dVs/dt due to high impedance floating condition (no motor connection).
- If a negative voltage is applied to VBS, when the high side circuit is powered up, the output can be latched on due to unwanted current flow into all of the high side circuit through its internal ESD diode structure.

(d) As a result, the high side output can be latched on while the associated low side output has already been turned on.

This is a mode of potential shoot through during a power up. The key to avoiding the shoot through is to properly initialize the high side circuit during a power up.

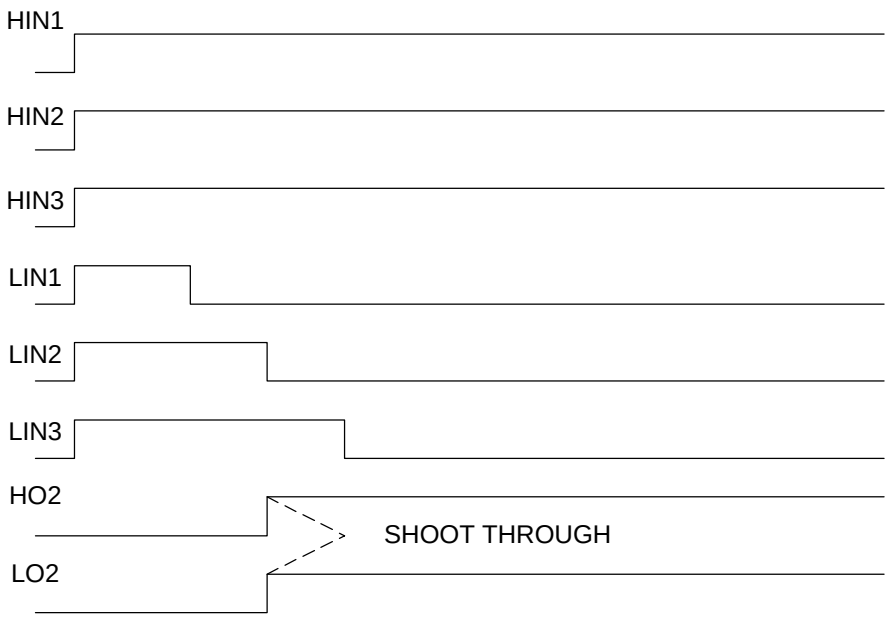


Figure 1: Power up sequence of Bootstrap Capacitor Charging

III - RECOMMENDED SOLUTION

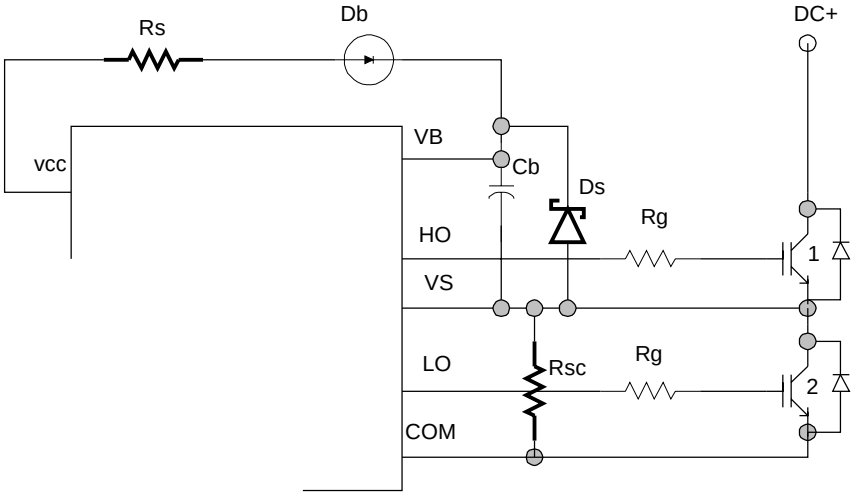


Figure 2: Typical bootstrap scheme with preventative elements

The most effective way of eliminating a potential shoot through is to eliminate the overstress condition of a negative voltage on VBS. Prior to a power up, if Vbs is biased to negative voltage which exceeds more than -0.3V as specified in the Absolute Maximum Rating specification - i.e. the condition #3 mentioned above -, then a forward diode current would flow through the ESD diode for the internal circuit in the high side as well as all P/N junctions in the high side well. One of the cause for such an overstress condition could be that, under a no load condition – i.e. condition #1 mentioned above -, the VS node is floating and the VS voltage could be high anywhere between DC+ and COM prior to charging up the bootstrap capacitor. To avoid both negative bias on VBS and a high dv/dt on the Vs node when the low side turns on, one can connect a bleeding resistor (Rsc) between VS and COM (Figure 2) so that the high side voltage can stay roughly at the negative DC bus potential prior to normal operation mode. Note that the Rsc value should both satisfy normal operation condition and minimize the power dissipation across Rsc – e.g when M1 switches on, the Rsc should be able to dissipate Pd = DC+ x DC+ / Rsc.

If a Schottky diode (Ds) must be connected between VB and VS – see Figure 4 – to avoid a negative bias on VBS, the Schottky diode should have the following specification:

- low forward voltage drop, e.g. Vf =0.2V
- minimum 35V reverse breakdown voltage
- low reverse leakage current
- fast reverse recovery time

One effective method of slowing down the dVbs/dt is to add a resistor in series with the bootstrap diode (figure 2). The value of series resistor relative to the bootstrap capacitor value should be chosen such that the RC time constant is equal or greater than 10usec. Note that if the rising dVbs/dt is slowed down too much, it could result in a few missing pulses temporarily during the start-up phase due to insufficient VBS voltage. This possibility is more likely in a higher frequency application, and detailed guidelines are given in the Appendix. For bootstrap capacitor selection, refer to the design tip DT 98-2.

IV - CONCLUSION

To eliminate the possibility of a latch-on at power up under a no load condition, the IC must be operated as follows:

- dVbs/dt higher than 10usec.
- Do not allow the VS node to float prior to normal operation mode.
- Do not allow VB to go below VS by more than one diode forward voltage drop prior to the power up of the high side circuit.

APPENDIX

In order to choose the optimum value for Rs, the following two conditions must be satisfied:

1. Rs X Cb time constant (figure 4) must be greater than 10usec.
2. The bootstrap capacitor (Cb) would charge through not only the bootstrap diode (Db) but also through the series resistor (Rs) from the Vcc supply. Thus, the minimum charge which the bootstrap capacitor needs to supply would be:

$$Cb \times (Vcc - Vrs - Vf - VBSmin) > 2Qg + (Iqbs/fc) \quad (1)$$

Where:

Vrs: Voltage drop across series resistor.
Vf: Forward voltage drop across the bootstrap diode.
VBSmin: Minimum voltage across the bootstrap capacitor required for full enhancement.
Qg: Gate charge of high side IGBT.
Iqbs: high side channel quiescent current.
fc: switching frequency.

Examples:
The following two examples demonstrate the cycle-by-cycle fluctuation in the bootstrap voltage during the start-up phase over one PWM fundamental frequency.

Condition:
For both Case 1 and Case 2
Vcc= 15v, Vf= 1.5v, VBSmin= 12.5v, Qg= 200nC, Iqbs= 200uA, fc= 2kHz, Cb = 2uF
For Case 1, Rs = 9Ω and for Case 2, Rs = 10Ω

Each parameters in the table are derived by the following equations.

$Tc = 1 / fc$
$m = (\sin 2\pi ft + 1) / 2$ where f= 60Hz (fundamental frequency)
$\Delta Vdis = (2Qg + (Iqbs \times Ton)) / Cb$
$Vbsdis = Vbscharg(prev) - \Delta Vdis$
$\Delta Vch = (Vcc - Vf - Vbsdis) \times (1 - \exp(-t/RC))$ Assume Vf is constant over charging current

$Vbscharg = Vbsdis + \Delta Vch$

$Irs = (Cb \times \Delta Vch) / Toff$
$Vrs = Irs \times Rs$

Where:

Tc: carrier period
m: modulation index [0 - 1]
∆Vdis: voltage difference for discharging period of Cb
Vbsdis: voltage across Cb after discharge
∆Vch: voltage difference for charging period of Cb

Vbscharg: voltage across Cb after charge
Vbscharg(prev): voltage across Cb after charge of previous state

Case 1: Cb = 2uF, Rs = 9 Ohms

seq #	Tc (ms)	m	T(on) (us)	T(off) (us)	∆Vdis (v)	Vbsdis (v)	∆Vch (v)	Vbscharg (v)	Irs (mA)	Vrs (v)	Vbsdis > Vbsmin ?
1	0	.5	250	250	0.225	13.275	0.225	13.5	1.8	0.016	Yes
2	0.5	0.593	297	203	0.23	13.27	0.214	13.484	2.1	0.019	Yes
3	1	0.684	342	158	0.235	13.249	0.232	13.481	2.9	0.026	Yes
4	1.5	0.768	384	116	0.239	13.242	0.232	13.474	4	0.036	Yes
5	2	0.842	421	79	0.242	13.232	0.23	13.462	5.8	0.052	Yes
6	2.5	0.904	452	48	0.245	13.217	0.215	13.432	8.9	0.08	Yes
7	3	0.952	476	24	0.248	13.184	0.175	13.359	14.5	0.131	Yes
8	3.5	0.984	492	8	0.249	13.11	0.093	13.203	23.3	0.21	Yes
9	4	0.999	499.5	0.5	0.25	12.953	0.009	12.962	36.4	0.328	Yes
10	4.5	0.991	498	2	0.25	12.712	0.051	12.763	50.6	0.455	Yes
11	5	0.975	488	12	0.249	12.514	0.26	12.774	43.3	0.39	Yes
12	5.5	0.938	469	31	0.247	12.527	0.478	13.005	30.8	0.278	Yes
13	6	0.885	443	57	0.244	12.761	0.443	13.204	15.5	0.14	Yes
14	6.5	0.819	410	90	0.241	12.963	0.397	13.36	8.8	0.079	Yes
15	7	0.741	370	130	0.237	13.123	0.298	13.421	4.6	0.041	Yes
16	7.5	0.654	327	173	0.233	13.188	0.271	13.459	3.1	0.028	Yes
17	8	0.563	282	218	0.228	13.231	0.241	13.472	2.2	0.02	Yes
18	8.5	0.469	235	265	0.224	13.248	0.232	13.48	1.75	0.016	Yes
19	9	0.376	188	312	0.219	13.261	0.223	13.484	1.4	0.013	Yes
20	9.5	0.287	144	356	0.214	13.27	0.217	13.487	1.2	0.011	Yes
21	10	0.206	103	397	0.21	13.28	0.212	13.492	1.1	0.01	Yes
22	10.5	0.136	68	432	0.207	13.285	0.205	13.49	0.95	0.009	Yes
23	11	0.078	39	461	0.204	13.286	0.205	13.491	0.9	0.008	Yes
24	11.5	0.035	18	482	0.202	13.289	0.203	13.492	0.84	0.0076	Yes
25	12	0.009	5	495	0.201	13.291	0.201	13.492	0.81	0.0073	Yes
26	12.5	0	0.1	499.9	0.2	13.292	0.2	13.492	0.8	0.0072	Yes
27	13	0.009	5	495	0.201	13.291	0.202	13.493	0.81	0.0073	Yes
28	13.5	0.035	18	482	0.202	13.291	0.202	13.493	0.84	0.0075	Yes
29	14	0.077	39	461	0.204	13.289	0.204	13.492	0.9	0.0079	Yes

Case 1: Cb = 2uF, Rs = 9 Ohms

seq #	Tc (ms)	m	T(on) (us)	T(off) (us)	ΔVdis (v)	Vbsdis (v)	ΔVch (v)	Vbschar g (v)	Irs (mA)	Vrs (v)	Vbsdis > Vbsmin ?
30	14.5	0.135	68	432	0.207	13.286	0.206	13.493	0.95	0.0086	Yes
31	15	0.205	103	397	0.21	13.282	0.209	13.491	1	0.009	Yes
32	15.5	0.286	144	356	0.214	13.277	0.214	13.491	1.2	0.011	Yes
33	16	0.375	188	312	0.219	13.272	0.217	13.489	1.4	0.013	Yes
34	16.5	0.468	235	265	0.224	13.265	0.222	13.487	1.7	0.015	Yes

Table 1

Case 2: Cb = 2uF, Rs = 10 Ohms

seq #	Tc (ms)	m	T(on) (us)	T(off) (us)	ΔVdis (v)	Vbsdis (v)	ΔVch (v)	Vbschar g (v)	Irs (mA)	Vrs (v)	Vbsdis > Vbsmin ?
1	0	.5	250	250	0.225	13.275	0.225	13.5	1.8	0.018	Yes
2	0.5	0.593	297	203	0.23	13.27	0.212	13.482	2	0.02	Yes
3	1	0.684	342	158	0.235	13.247	0.233	13.48	2.9	0.029	Yes
4	1.5	0.768	384	116	0.239	13.241	0.23	13.471	3.9	0.039	Yes
5	2	0.842	421	79	0.242	13.229	0.227	13.456	5.8	0.058	Yes
6	2.5	0.904	452	48	0.245	13.211	0.21	13.421	8.8	0.088	Yes
7	3	0.952	476	24	0.248	13.173	0.167	13.34	13.9	0.139	Yes
8	3.5	0.984	492	8	0.249	13.091	0.089	13.18	22.3	0.223	Yes
9	4	0.999	499.5	0.5	0.25	12.93	0.009	12.939	34.7	0.347	Yes
10	4.5	0.991	498	2	0.25	12.689	0.044	12.733	44.1	0.441	Yes
11	5	0.975	488	12	0.249	**12.484**	0.259	12.743	43.1	0.431	**No**
12	5.5	0.938	469	31	0.247	**12.496**	0.453	12.949	29.2	0.292	**No**
13	6	0.885	443	57	0.244	12.705	0.472	13.177	16.6	0.166	Yes
14	6.5	0.819	410	90	0.241	12.936	0.394	13.33	8.8	0.088	Yes
15	7	0.741	370	130	0.237	13.093	0.319	13.412	4.9	0.049	Yes
16	7.5	0.654	327	173	0.233	13.179	0.272	13.451	3.2	0.032	Yes
17	8	0.563	282	218	0.228	13.223	0.245	13.468	2.2	0.022	Yes
18	8.5	0.469	235	265	0.224	13.244	0.234	13.478	1.8	0.018	Yes
19	9	0.376	188	312	0.219	13.259	0.223	13.482	1.4	0.014	Yes
20	9.5	0.287	144	356	0.214	13.268	0.218	13.486	1.2	0.012	Yes
21	10	0.206	103	397	0.21	13.276	0.212	13.488	1.06	0.0106	Yes
22	10.5	0.136	68	432	0.207	13.281	0.208	13.489	0.96	0.0096	Yes
23	11	0.078	39	461	0.204	13.285	0.205	13.49	0.89	0.0089	Yes
24	11.5	0.035	18	482	0.202	13.288	0.203	13.491	0.84	0.0084	Yes
25	12	0.009	5	495	0.201	13.29	0.202	13.492	0.81	0.0081	Yes
26	12.5	0	0.1	499.9	0.2	13.292	0.2	13.492	0.80	0.008	Yes
27	13	0.009	5	495	0.201	13.291	0.202	13.493	0.81	0.0081	Yes

Case 2: Cb = 2uF, Rs = 10 Ohms

seq #	Tc (ms)	m	T(on) (us)	T(off) (us)	ΔVdis (v)	Vbsdis (v)	ΔVch (v)	Vbschar g (v)	Irs (mA)	Vrs (v)	Vbsdis > Vbsmin ?
28	13.5	0.035	18	482	0.202	13.291	0.201	13.492	0.83	0.0083	Yes
29	14	0.077	39	461	0.204	13.288	0.204	13.492	0.88	0.0088	Yes
30	14.5	0.135	68	432	0.207	13.285	0.206	13.491	0.95	0.0095	Yes
31	15	0.205	103	397	0.21	13.281	0.21	13.491	1.1	0.011	Yes
32	15.5	0.286	144	356	0.214	13.277	0.212	13.489	1.2	0.012	Yes
33	16	0.375	188	312	0.219	13.27	0.218	13.488	1.4	0.014	Yes
34	16.5	0.468	235	265	0.224	13.264	0.222	13.486	1.7	0.017	Yes

Table 2

In case #1 with Rs= 9 Ohms, the high side supply voltage at the end of Ton (Vbsdis) is greater than the required minimum voltage (Vbsmin= 12.5v) at all times, while in case #2 with Rs= 10 Ohms, Vbsdis is smaller than Vbsmin in two of the sequences 11 & 12. Therefore, to satisfy the two conditions mentioned the optimum value of the Rs would be:

$$5\ \Omega < Rs < 10\ \Omega$$

DESIGN TIP

International Rectifier 233 Kansas Street El Segundo CA 90245 USA

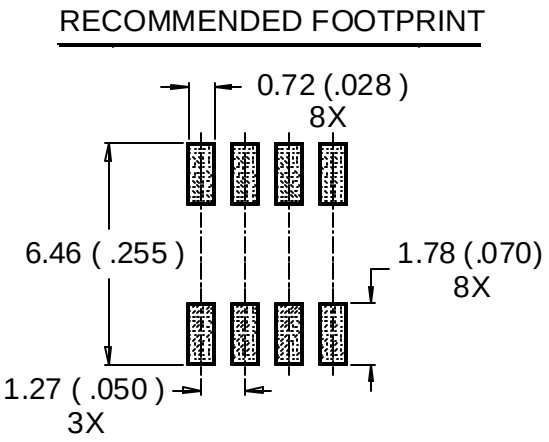
Hand-Soldering SO-8 MOSFETs

by David Jauregui

Hand-soldering SO-8 MOSFETs to a printed circuit board (PCB) may cause damage if not done properly. This application note describes how to properly hand-solder SO-8 devices to PCBs.

The SO-8 Footprint

An SO-8 MOSFET must be mated to a proper PCB footprint in order to minimize the chances of mechanical failure. International Rectifier's minimum recommended footprint is shown below.



Grounding

MOSFETs are sensitive to electrostatic discharge (ESD). Proper grounding prevents device failure caused by ESD. The workbench, workmats and the soldering equipment must be grounded. Personnel must also be grounded via a grounded wrist strap. The PCB power and ground bus lines must also be grounded, when no live voltage is present.

Recommended Equipment

Proper equipment is important for good solder joints. You'll need a temperature controlled soldering iron, such as the Pace ST-20A with a fine point soldering iron tip (Pace 1/16" chisel, single point), and low melting-point solder and flux, Kester Sn60Pb40 "44" Rosin Core, or similar.

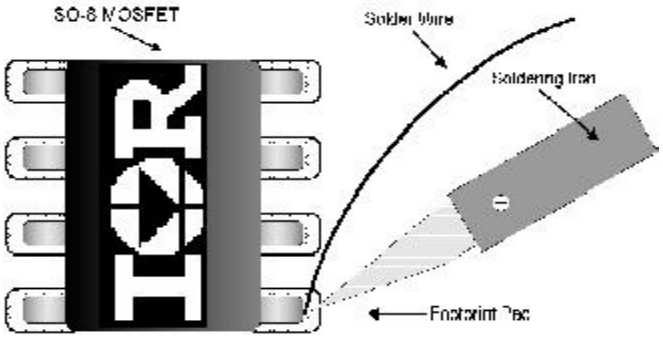
Attaching and Soldering

There are two essential points to ensure reliable results and prevent thermal shock: The soldering iron tip temperature should be about 300ºC, and the tip must not directly touch device lead. The SO-8 device should first be tack-soldered to the board so that it will stay within the boundaries of its footprint. First, tin the gate pad on the PCB. Second, align the device to its footprint. Next, heat the joint just enough to re-flow solder between the pad and the gate lead. The tip should be applied to the pad of the footprint when soldering. Feed the solder at the device lead and pad junction. Soldering time should not exceed what is necessary to flow solder into the joint. Solder one lead at a time, alternating between drain and source leads, leaving the gate lead last. Since the gate lead is tack-soldered to the PCB, you must re-solder the gate to the pad properly for a reliable joint. Finally, remove all flux residue with flux remover.

De-Soldering

If a device must be removed, de-soldering is necessary. A suitable de-soldering tip is the Pace SOIC-8 Surface Mount Removal Tip. However, there is no guarantee that the device will not be destroyed. Reusing the same device is not recommended.

Avoid over-heating the board to prevent de-laminating the PCB foil traces. Maintaining a clean PCB footprint is important to reduce mechanical failure. Once the device is out, remove excess solder and any leftover residue.



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DESIGNTIP

DT 99-1

International Rectifier 233 Kansas Street El Segundo CA 90245 USA

Overshoot Voltage Reduction Using IGBT Modules With Special Drivers.

By David Heath & Peter Wood

TOPICS COVERED

Design Considerations
Turn-off Parasitics
New Method for Voltage Overshoot Reduction
Design Example

1. DESIGN CONSIDERATIONS

A critical problem common to all power switching circuits is inductive energy storage in stray inductances within the circuit. At low power levels of a few Watts a fast turn-off transition results in ringing with an overshoot voltage proportional to the stored energy and the switching speed. At high power levels these overshoots pose a major problem in terms of adequate voltage margins to handle them and the additional cost of such devices. Higher switch voltage ratings also result in higher conduction losses and lower overall efficiency. We are thus faced with a dilemma, how to maintain high efficiency with fast switching speeds without creating huge overshoots with all their attendant problems.

2. TURN-OFF PARASITICS

It is not possible to eliminate all stray inductances so there will always be overshoots at turn-off. Obviously circuit inductance must be reduced to the absolute minimum and there are many ways to do this, but the internal package inductance of the switching device is a measure of how well its manufacturer understands the inductance problem and has designed his switch accordingly.

Circuit inductance can be reduced by decreasing the effective loop size of the circuit and the most effective way to do this is by the use of laminated bus structures. The energy storage is thus greatly reduced and with it the overshoot voltage for a given switch speed. Strategically placed decoupling capacitors further reduce inductance values. Note, low internal ESR-ESL of these capacitors is also critical.(See DT 99-2 for further details)

There are a variety of methods used to combat these overvoltage spikes, all with the tradeoff of increased power dissipation in the switching device or external devices such as snubbers. One method of reducing the overvoltage spike is by limiting di/dt by increasing Rg. This can be done individually for turn-off as well as turn-on, but still has a substantial increase of the switching loss in order to obtain an appreciable reduction in the voltage spike.

Figure 1 shows a typical voltage spike at turn-off across a 600V, 200A Ultra-fast IGBT module operating at a bus voltage of 360V and 200A, where Rg(on) is 4.7Ω and Rg(off) is 0, and the effect of increasing Rg(off) to 30Ω in the indicated increments. Table 1 shows the increase in switching loss.

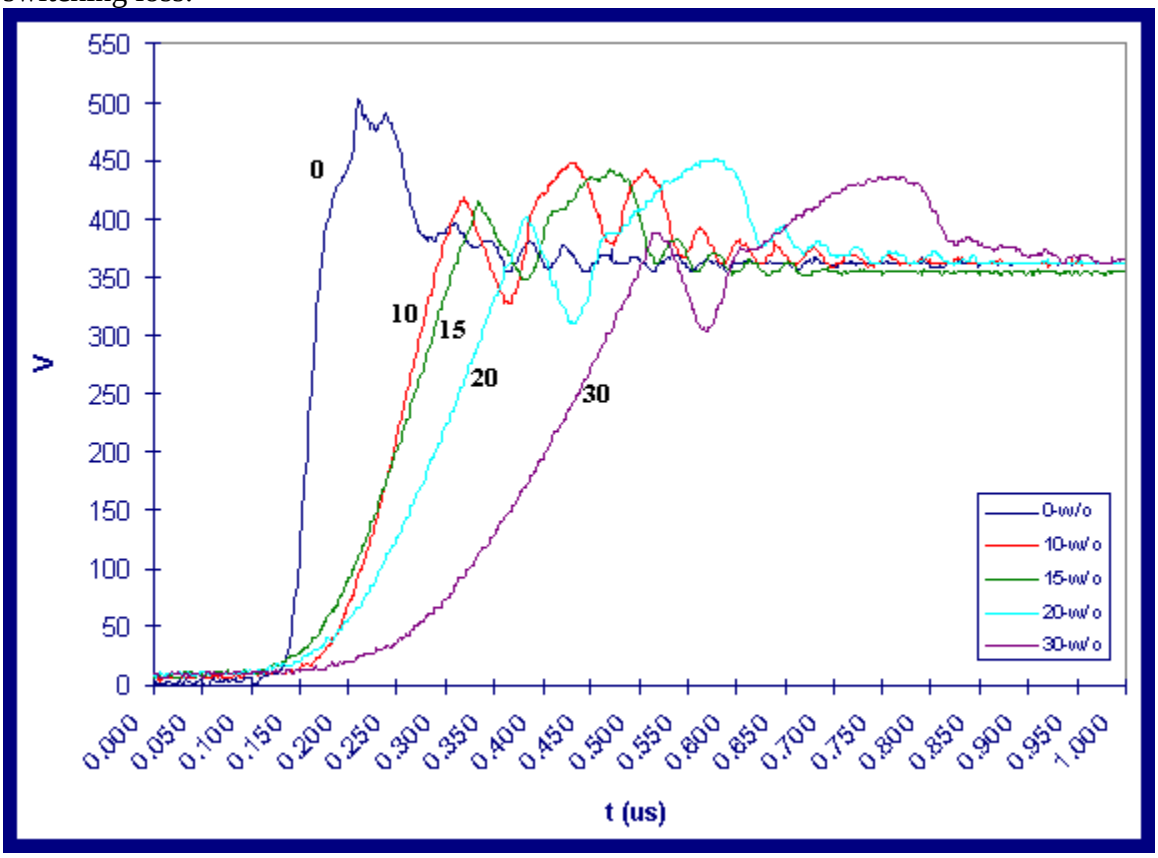


Figure 1

TABLE 1	
Rg(off)	Eoff
0	6.0mJ
10	11.1mJ
15	13.2mJ
20	15.4mJ
30	19.8mJ

As can be seen, increasing Rg to 10 ohms doubles the turn-off switch loss while only reducing the peak voltage by 13%. This would allow the use of a 600V device with a reasonable safety margin, but at the expense of a decrease in overall efficiency.

3. NEW METHOD FOR VOLTAGE OVERSHOOT REDUCTION

The ideal scenario would be to use dv/dt control such that the device turns off as fast as possible (within the dV/dt limits of the commutation diode) until Vce reaches the bus voltage, then decrease dv/dt to reduce the overvoltage spike. This will minimize switch loss while also reducing the overshoot.

The basic approach to this would be to discharge the gate at turn-off through a 0Ω gate resistor, or through a small value if dV/dt is too high, until Vce reaches the bus voltage, then switch the discharge path to a higher value resistance. Figure 2 shows one approach to accomplishing this.

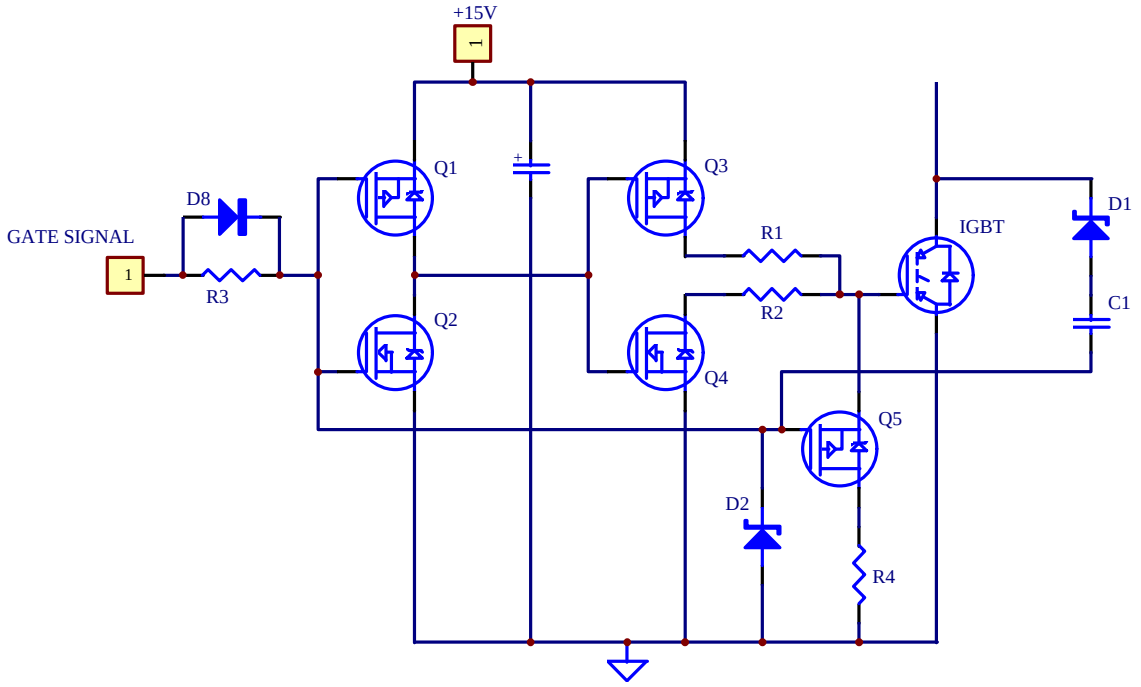


Figure 2: Overvoltage reduction method

With this approach, the input drive signal is fed into D8, bypassing R3, for a fast rise time. This turns Q1 off and Q2 on, bringing the gates of Q3 and Q4 to ground, which turns Q3 on and Q4 off. The drain current of Q3 flows through R1 and charges the gate of the IGBT. The gate of Q5 is connected to the gate signal, which is turned off during the IGBT turn-on. To turn off the IGBT, Q1 turns on and Q2 turns off. The gates of Q3 and Q4 are biased high, which turns Q3 off and Q4 on. At the same time, the gate of Q5 is pulled low, turning it on. This will discharge the gate immediately through R4, which could be a short or set to some value depending on the dV/dt parameters of the IGBT in use. Vce will begin to rise.

When the collector voltage reaches the breakdown voltage of zener D1, it will conduct and current will flow through C1to charge the gate of Q5, turning it off. This pulse will be very short, but long enough to turn Q5 off. With Q5 no longer discharging the gate, the remainder of the gate charge now flows through R2, slowing the rate of turn-off and reducing the overshoot voltage. D2 is a 12-15V zener to protect the IGBT gate from excessive forward voltage.

Figure 2 shows the effect of different resistor values for Rg(off) with this circuit. Table 2 shows the corresponding effect of Eoff.

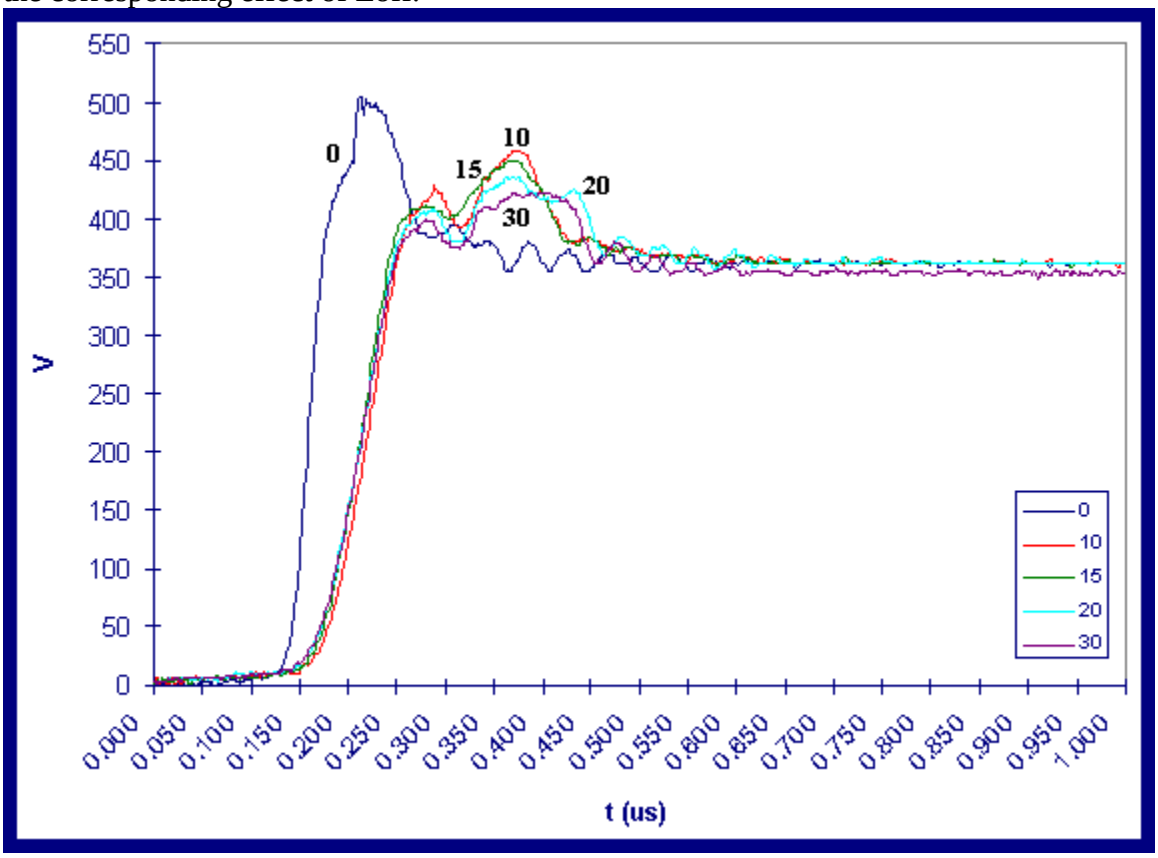


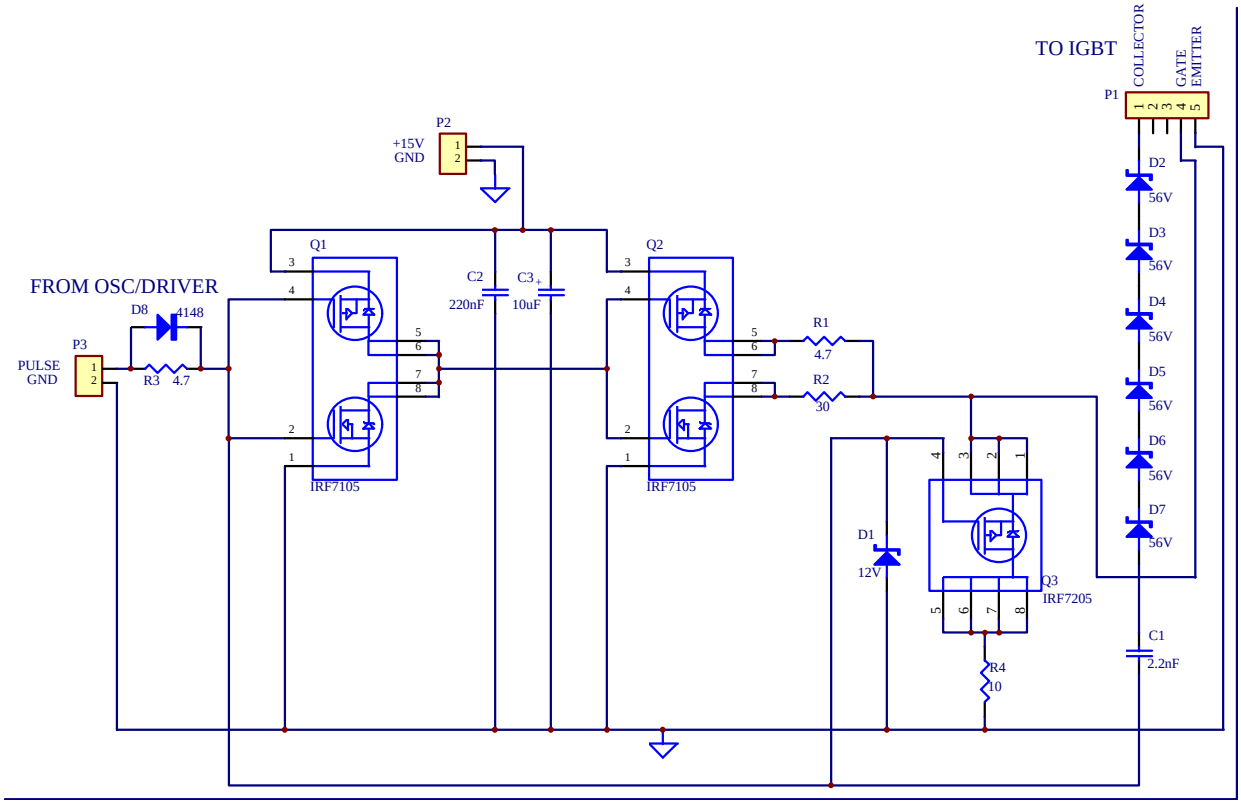
Figure 3

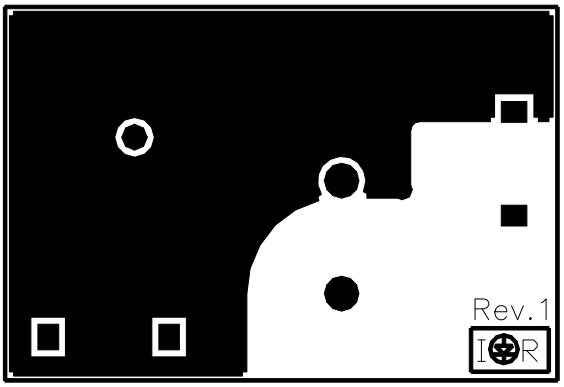
TABLE 2	
Rg(off)	Eoff
0	6.0mJ
10	9.4mJ
15	9.9mJ
20	10.3mJ
30	10.6mJ

So, in conclusion, a lower peak turn-off voltage can be achieved with half the switching loss of an IGBT without dv/dt control.

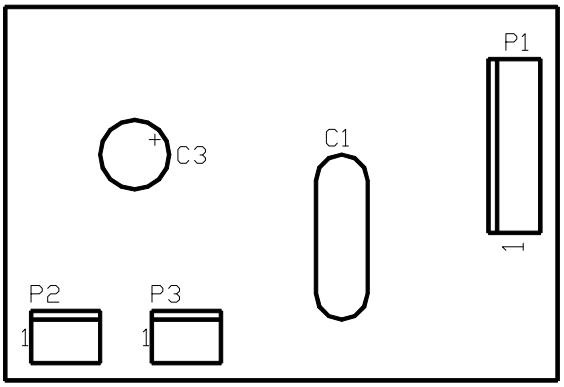
4. DESIGN EXAMPLE

A driver circuit was optimized for circuit inductance/impedance by using SMT components to keep the loop size of the gate discharge path to a minimum.

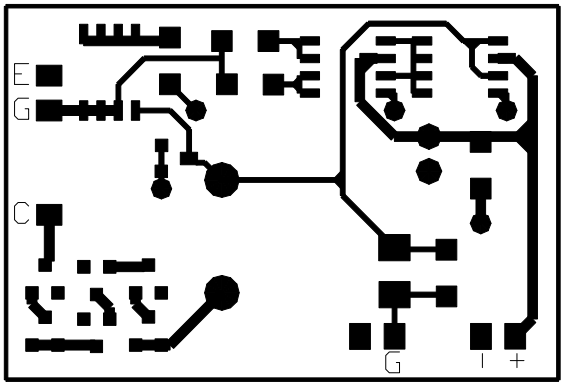




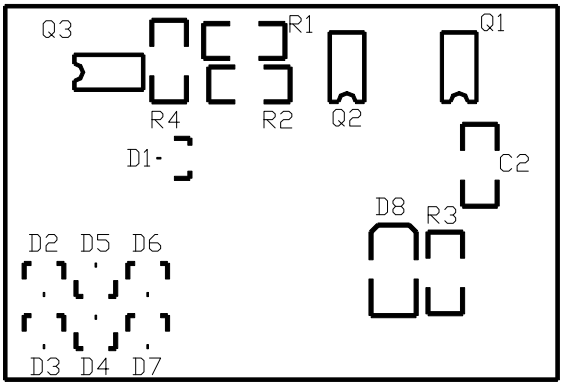
COMPONENT SIDE



TOP SILK



SOLDER SIDE



BOTTOM SILK

INTERNATIONAL RECTIFIER CORPORATION
100 North Sepulveda Boulevard, 8th Floor, El Segundo, California 90245
Phone: 310-726-8622 Fax: 310-252-7167

Design Tip

Using WARP Speed™ IGBTs In Place Of Power MOSFETs at Over 100kHz Converter Applications

By Chesley Chao - Strategic Marketing Manager

Introduction:

International Rectifier's latest development in IGBT technology has offered the power converter industry with optimized power switches - the WARP Speed™ IGBTs. They have switching characteristics that are very close to those of power MOSFETs, without sacrificing the inherently superior conduction characteristics of IGBTs. Thus, in higher-power power supply type applications where power MOSFETs can become prohibitively expensive, the IGBT offers a more cost-effective solution.
Due to the higher usable current density of IGBTs, it can usually handle two to three times more current than a typical MOSFET it replaces. This means that a single IGBT device can replace multiple MOSFETs in parallel operation or any of the super-large single power MOSFETs that are available today. IGBTs have already been replacing MOSFETs and Bipolars at up to 75Khz for several years. Now, with the advent of higher-frequency WARP Speed IGBTs, which improves their Eoff (turn-off switching loss) by more than 50%, the same can apply at frequencies up to 150 kHz.

How to replace MOSFETs with IGBTs

To replace a power MOSFET with an IGBT is easy. The IGBT has the same pinouts, it blocks the same voltage, all you need to do is to factor in a few design criteria indicated below in order to take full advantage of this device.

The Gate Drive Requirement

The gate drive for MOSFETs and IGBTs are essentially the same. In fact, due to a smaller input capacitance the IGBT is, if anything, a little simpler.
As with any technology replacement there are invariably some differences, for instance the gate voltage (Vge) for an IGBT is recommended to be 12V (preferably 15V) for the device to turn on fully, while a FET has a 10V recommendation. This is probably the single most important detail to

watch out for when replacing a FET, if the device is not fully turned on then the Vce(on) will be greater losses and potentially device failure.
You will also find, in the case of existing designs, the change in gate capacitance (lower for the IGBT) may require a change of gate resistor to re-tune the gate circuit. Adjusting the value of the IGBT gate resistor will normally have minimal effect on the switching-loss behavior and is of secondary importance.

EMI Consideration

The slope of the current waveform characteristics during device turn-off is important when considering EMI. Compared with a typical 600V power MOSFET, the WARP Speed IGBT turn-off waveform has made 25% improvement in di/dt which gives the device a slower slope during turn-off (see Figure 1 for details). If anything, this will probably lower the EMI noise level significantly.

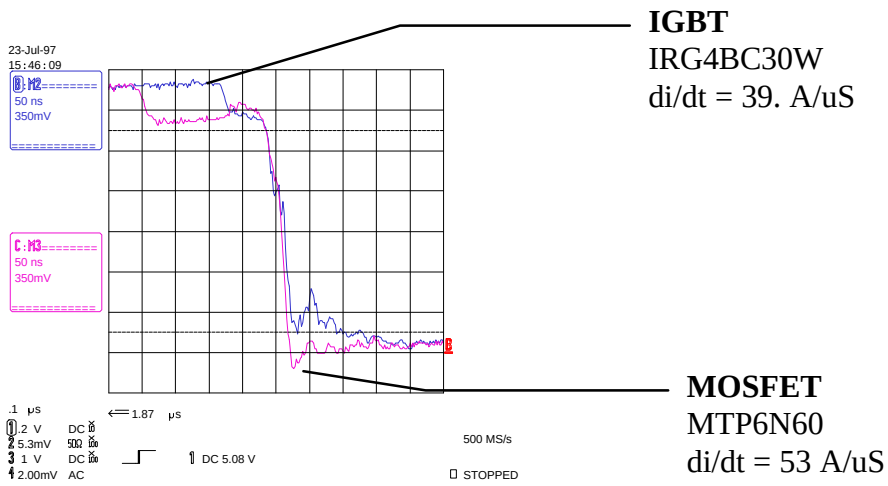


Figure 1. Current Turn-off di/dt Comparison - IGBT vs. MOSFET

Higher Junction Temperature

One should notice that the IGBT will often a slightly higher junction temperature than the equivalent Power MOSFET. As the Vce(on) and switching losses don't change significantly when you add more silicon area, one should select the minimum IGBT device rating to fulfill the application requirement.

Some well known methods of calculating the junction temperature for both MOSFET and IGBT are listed below :

MOSFET	**IGBT**
Conduction Loss :	
$Pcond = I^2_{D(rms)} * Rds(on)_{Hot} * D$	$Pcond = Vce(on) * Ic * D$
(where D - Duty cycle)	
Switching Loss :	
$Psw = Id * Vds * t_{SW} * f_{SW}$	$Psw = Ets_{(Hot)} * f_{SW}$
(where f_{SW} - switching frequency $Ets_{(Hot)}$ - total switching losses (in data sheet) t_{SW} - total switching time (on + off, in data sheet))	
Total Loss Pd :	
$Pd = Pcond + Psw$	$Pd = Pcond + Psw$
$Tj = Pd * Rth\text{-}jc + Tc$	$Tj = Pd * Rth\text{-}jc + Tc$
(where Tc - Case temperature Tj - Junction Temperature Rth-jc Thermal Resistance Junction to Case (in data book))	

Packaging Design

The package style and pinouts of IGBTs and MOSFETs are similar, all the basic primary functions are the same, no fundamental mechanical or layout changes are required.

PCB Layout

All the same criteria that are useful in MOSFET layout apply to the IGBT layout, good design rules such as very low inductance tracks to the device, control and power tracks separate and not running parallel etc.

Conclusion

The WARP Speed IGBT can be used to generate same amount of output power as a much larger Power MOSFET does in a hard-switching applications. In resonant converter applications, the difference is even greater. The component cost saving and board space saving as a result of this can be considerable.

International
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DESIGN TIP

DT 98-4

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Technical Overview of IR215x Products

By John Parry

Introduction

IR215x devices are widely used in high volume off-line, cost sensitive areas such as Electronic Ballasts, Primary and Standby AC/DC and DC/DC Power Supplies and Battery Chargers. All IR215x Control IC's integrate high voltage half-bridge drive with oscillator and all absorb the function of outmoded gate transformer and separate driver.

The most broadly applicable IR215x device is referred to as a Self-Oscillating Control IC. Table 1 lists availability and release order. Since introduction,the IR2155 has set an industry standard which has been advanced by subsequent devices, culminating in third generation products IR2153, IR2154, IR21531 IR53H series SIP hybrid modules and now the IR2157 and IR2159.

Topics covered;

- Technical Comparison of Second and Third Generation Self Oscillating Control IC's
  Application benefits of recently released devices.
- The IR2157 as an Advanced Variable Frequency Control IC
  New controller for HF Electronic Ballasts and other systems using resonant loads
- ESD, Latch Immunity and Hidden Value within IR Control ICs
  Frequently overlooked ruggedness benefits of all International Rectifier HVICs

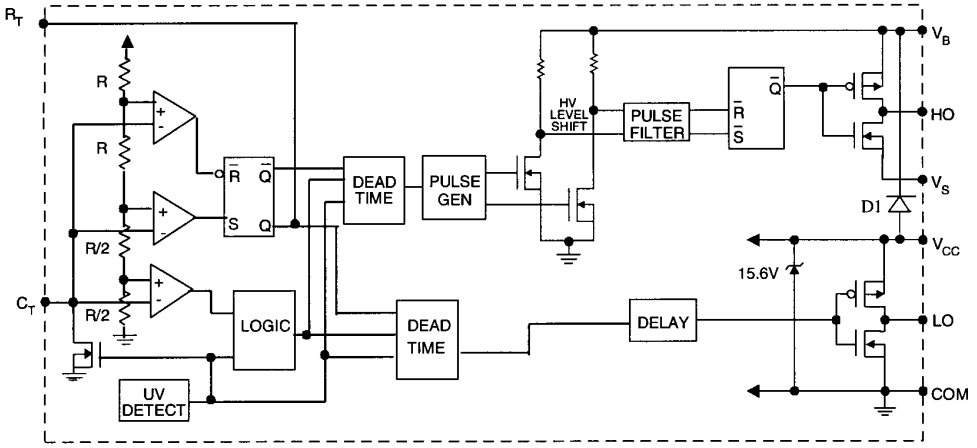
Table 1: **IR215x** Product Family.

Base #	Hybrid	Description	Oct /98; Status
IR2151	IR51H(D)xxx	Gen.2 Self-Oscillating Control IC	Not new designs
IR2152	Possible	Gen.2 Self-Oscillating Control IC	Not new designs
IR2153	IR53H(D)xxx	Gen.3 Self-Oscillating Control IC	Available
IR2153D	Possible	Gen.3 Self-Oscillating Control IC	Available
IR21531	Possible	Gen.3 Self-Oscillating Control IC	Available
IR21531D	Possible	Gen.3 Self-Oscillating Control IC	Available
IR2154	Possible	Gen.3 Self-Oscillating Control IC	Available
IR2155	No	Gen.1 Self-Oscillating Control IC	Not new designs
IR2157	- -	CIC for HF.Ballast /Resonant loads	Sampling now
IR2159	- -	CIC with Phase Mode Control	In Development

1. Technical Comparison of Second and Third Generation Self Oscillating Control IC's

This section shows improvements made to third generation Self-Oscillating Control IC's by direct comparison with the second generation IR2151. Key points are underlined and summarised at the end of the section. Part number IR2153 refers to all third generation ICs and IR2151 for second generation. Due to wide market acceptance, International Rectifier currently plans continued manufacture of all IR215x products. However, for new designs or upgrade to mature designs, third generation Self Oscillating Control ICs are advised on grounds of enhanced electrical performance and functionality

Figure 1: IR2153D Functional Block Diagram



<u>IR2153 has Increased Under Voltage Lockout Hysterisis.</u>

What is under-voltage lockout ?

Under voltage lockout (UVLO) is the name for a protection feature built into IR2151, IR2153 and many other Control IC's from International Rectifier. This block is marked as UV detect on figure 1 and ensures that the gate drive outputs, HO and LO are both low should bias become too marginal for comfortable gate drive to the output transistors. The UVLO circuit also assures a repeatable start-up sequence and controls bias current needed for various elements of the IC. Second and third generation IR215x have one UVLO circuit, which is used to monitor the bias supply, Vcc.

What is under-voltage lockout hysterisis ?

Hysterisis is a technique commonly used to improve noise immunity. Instead of switching on/off at one voltage level, two threshold levels are defined; one sensitive to a rising edge and the other to a falling edge. In product data sheets describing Vcc undervoltage lockout, these two thresholds are listed as VccUV+ and VccUV-. Hysterisis is a measure of the difference between these two thresholds and is separately listed on data sheets as VccUVH. VccUV+ is the threshold at which the chip is first enabled, when Vcc is rising. Once enabled, Vcc is allowed to drop slightly without adverse effects.

How can Vcc noise be minimised ?

Good local decoupling with low ESR capacitors and adequate reservoir capacitance from Vcc to COM should be used in designs based on IR2151, IR2153 and other Control IC's to minimise noise. Circuit layout is also important. Design Tip DT98-2 offers further guidance on this subject.

IR2153 has True Micropower Start-Up.

What is micropower start-up ?

Micropower start-up means that the bias current needed when the IC is in a quiescent state (i.e. not oscillating and Vcc<VccUV) is reduced to a very low level. Figures 2 and 3 clearly show the differences in start-up bias between IR2151 and IR2153.

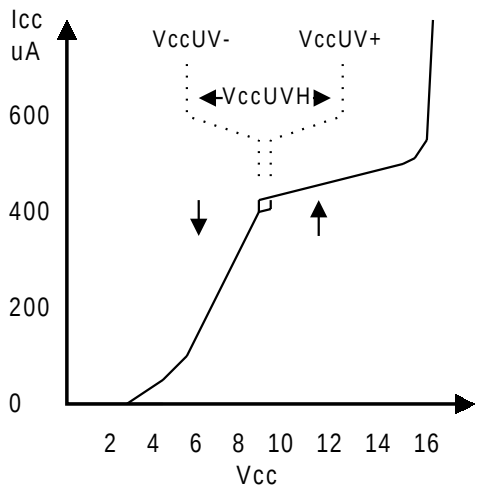
How will micropower start-up benefit my design ?

Off-line applications usually have a single resistor from a high voltage bus for start-up bias to keep component cost and complexity low. In some cases this resistor provides bias for all modes of operation (both start-up and running, where current demand is highest). However, an auxiliary low voltage source is more common for this purpose. 'Bootstrapping' is beneficial because an auxiliary supply can be derived with much higher efficiency than from a simple dropping resistor connected to the line.

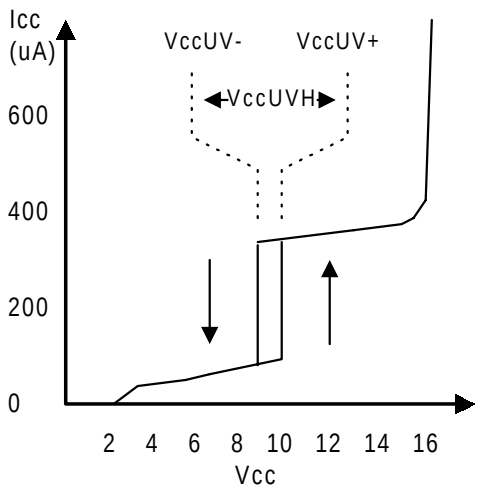
In bootstrap start-up schemes, micropower feature allows the pull-up resistor value to be increased in value compared to schemes in which a single dropping resistor provides all the bias. This is because the resistor needs only to overcome quiescent bias current requirements for the IC and raise Vcc to UV+. When the IC starts oscillating, additional bias requirement is met by an auxiliary supply. The term 'bootstrap' is also used to describe the diode and Vbs capacitor arrangement shown in the typical circuit configuration for IR215x. This part of the circuit, explained by design tip DT98-2 serves a different function to the resistor in a bootstrap 'start-up' scheme.

How is micropower start-up implemented on IR2153 ?

IR2151 typical Vcc bias characteristics



IR2153 typical Vcc bias characteristics



IR2153 and IR2151 behave slightly differently upon power-up. When using IR2151, the Rt output is held high and approximately tracks Vcc until the VccUV+ threshold is reached. The Ct pin is held low at this time and so an additional component of Vcc bias current must flow out through Rt and return to COM through Ct. The component of current flowing through Rt and Ct during start-up is eliminated with IR2153 because Rt is low when Vcc<VccUV. Internal bias current demand of IR2153 is also lower than for IR2151, especially during start-up when Vcc < VccUV+

How can I implement an auxiliary supply and take full advantage of bootstrapping ?

An auxiliary supply can be conveniently derived from a charge pump connected to the half bridge output, or from an isolated secondary winding taken from a donor transformer elsewhere in the system. An example of charge pump implementation may be taken from our compact HF ballast reference design, IRPLCFL1 or from design tip DT94-10B. Making use of an auxiliary supply reduces static power dissipation, temperature rise in the bootstrap resistor and increases circuit efficiency. This difference is significant for low power designs where start-up bias significantly impacts overall efficiency, and is more noticeable if the bus voltage is comparatively high.

<u>IR2153 incorporates a fast Shutdown Mode:</u>

What is fast shutdown and why might I need it ?

Most applications call for protective action against fault conditions that would otherwise destroy output switches. Fusing is the simplest option but is often ineffective at preventing damage to semiconductors and is not self-resetting, unless comparatively more expensive devices are used. If the load is capacitively coupled or resonant in nature, for example as in most Electronic Ballast designs, ample protection may be afforded by only halting the oscillator and preventing further switching cycles. However, adequate protection sometimes calls for both FETs to be rapidly turned off.
How can shutdown be implemented when using IR2151 ?

Vcc must be pulled below VccUV- To turn off both FETs when using IR2151. This requirement may to an extent conflict with the need to provide a healthy charge reservoir and solid decoupling. Any IR2151 shutdown network must be capable of rapidly pulling charge from the Vcc reservoir capacitor (and the decoupling capacitor, if present). Low holding current thyristors can be used to crowbar Vcc and latch the chip off until the supply is recycled in designs based on IR2151. This approach is both simple and inexpensive but does not support automatic power-on reset. If the circuit must reset after fault condition without manual supply interruption, IR2153 is preferable as fewer peripheral components are needed.

How does the IR2153 shutdown mode work ?

The IR2153 offers a convenient shutdown solution by adding a second function to the Ct pin. A third functional threshold is added to Ct and set at Vcc/6. Below this threshold a fast shutdown mode is invoked and both output buffers are set low with minimal delay. This allows a simple open-collector NPN transistor or similar to be used as part of an inexpensive protection scheme.

Can IR2153 be driven directly as a slave device, for example to complete a full bridge ?

The Ct input of IR2151,2152 or 2155 can be directly fed from a square wave source provided Vct high > 2/3 Vcc and Vct low < 1/3 Vcc.The Rt output of any Self Oscillating Control IC can generate a master clock to feed directly into the Ct input of another, effectively bypassing the internal oscillator of the slaved device. This can be a useful way to implement a full bridge using just one type of IC or Hybrid .The shutdown threshold of IR2153 should be noted when it is being used in this way. Square wave drive with zero DC offset will not cause outputs to switch alternately as would be the case with IR2151, because the shutdown condition will invoke when Ct is zero, however IR2153 can still be used as a slave by adding a simple passive circuit to add a small DC offset. A design tip is planned to address master/slave applications using Self-Oscillating Control IC's.

IR2153 has Improved Dead-Time Accuracy with Zero Average Temperature Coefficient.

What is dead-time and why is it important ?

Dead-time is the period during which both HO and LO outputs are intentionally low. This period is fixed inside the IC and serves several essential functions. The primary function of dead-time is to prevent cross conduction or shoot-through in half-bridge designs. If the load is resonant in nature, such as in electronic ballasts and resonant mode power supplies, dead-time also helps maintain zero voltage switching (ZVS). Sometimes called soft switching, this technique significantly reduces switching losses.

How does dead-time prevent cross conduction, or shoot-through ?

Cross-conduction will occur in half bridge circuits if both high and low side transistors are either fully or partially on at the same time.The resulting short across the supply excaserbates EMI, increases dissipation and may destroy power switches, control IC or both if extreme. MOSFET turn on / off times are often inequal and vary in production, so dead-time offers a guard band to account for these differences. IR215x is available with various dead time options, however switching times can be easily modified using small signal diodes across series resistors in the gate drive loop if necessary.
How does dead-time help to support soft switching ?

When the load is inductive or resonant, circuit effeciency is generally highest when zero voltage switching (ZVS or soft switching) occurs. In ZVS, there is just enough time when both FETs are off (approximately equal to the dead-time) to allow load energy to swing the output to the opposite rail, where current will flow in the FET body drain diode. This desirable process is called self-commutation.

Why is soft switching (ZVS) more efficient than hard switching
(Why do MOSFETs become hot when the load is removed ?)

Self-commutation is almost completely lossless because output capacitance of the half bridge rings with the inductive component of the load when both half bridge transistors are off. When the next transistor turns on, the voltage across it is already at or close to zero, so its internal capacitance is already discharged. When its load is not resonant or inductive in nature, the output cannot self-commutate to the opposite rail during off time, so the voltage across the next transistor to turn on is high. It must therefore discharge its own output capacitance in addition to providing load current. This explains why half bridge transistors often get hot when there is no load at all or in ballasts, when the lamp is removed and the oscillator is allowed to continue running.

What is the optimum value of dead-time ?

if ZVS is required but the dead-time is too short, there is insufficient time for the half-bridge output voltage to *completely* self-commutate to the opposite rail. This leaves a fraction of the bus voltage remaining across the output capacitance of both transistors which the next transistor to switch on must disharge. This is partial hard switching (or partial soft switching). Conversely, if the dead-time is too long, the output voltage will self-commutate to the opposite rail, but a short time later, the load current will reverse or ring, producing a voltage transient. Again, the result is partial hard switching and less than optimal switching efficiency. For ZVS, optimal dead time occurs when there is just enough time for self commutation to occur. IR2153 is available with several dead-time options to help meet this requirement. If further adjustments are necessary, small signal diodes can be used in the gate drive loop to independantly change charge/discharge timing.

How does improved dead-time performance of IR2153 benefit my circuit ?

IR2153 has a stringent specification for dead-time and has a zero average coefficient of temperature. This can be important for production repeatability and more easily supports ZVS under variable temperature conditions.

<u>IR2153 output buffers have a reduced di/dt output stage</u>

What is a reduced di/dt output stage ?

This means that the peak rate of change of current (rate of current rise, and fall for turn-on and turn-off) has been deliberately reduced. In effect the 2153 output buffers are turned on and off more slowly than with IR2151.

What are the benefits of reduced di/dt in the gate drive circuit ?

Benefits of reduced di/dt output buffers include lower gate ringing (Vgs overshoot / undershoot) from combination of di/dt and gate circuit parasitics. In some cases gate resistors can be eliminated altogether, however this depends on several factors such as layout and transistor type used. RF interference may also be reduced.

Will reduced di/dt increase switching loss and lower efficiency ?

Provided a suitable series gate resistor is selected, efficiency will not be impaired. Peak output buffer current capability of IR2153 is comparable with IR2151 and so similar size FET’s or IGBT’s may be controlled without detrimental switching characteristics.

Table 2: Parametric Comparison of IR2153 and IR2151

Typical values @ Ta=25 C are listed unless stated otherwise

Parameter	IR2151(D)(S) IR51H(D)xxx	IR2153(D)(S) IR53H(D)xxx	IR21531 IR531H(D)xxx
Quiescent Bias, Iqcc	400uA + Vcc/Rt (Rt=Vcc; Ct=0V during start-up)	150uA (Rt=0; Ct=0V during start-up)	150uA (Rt=0; Ct=0V during start-up)
UVLO Thresholds VccUV+ VccUV- VccUVH	 8.5V 8.1V 0.4V	 9.0V 8.0V 1.0V	 9.0V 8.0V 1.0V
Shudown Method	Vcc < VccUV-	Vcc < VccUV- *OR* Ct < Vcc/6	Vcc < VccUV- *OR* Ct < Vcc/6
Dead-Time, Td Typical Min,Max Temp. Coeffecient	 1.2 uSec 0.5, 2.25 uSec +5000 ppm / C	 1.2 uSec 0.75, 1.65 uSec +/- 1000 ppm / C	 0.6 uSec See Data Sheet +/- 1000 ppm / C
Output Buffer di/dt Typical	0.3A / 20nS	0.3A / 70nS	0.3A / 70nS

Note:

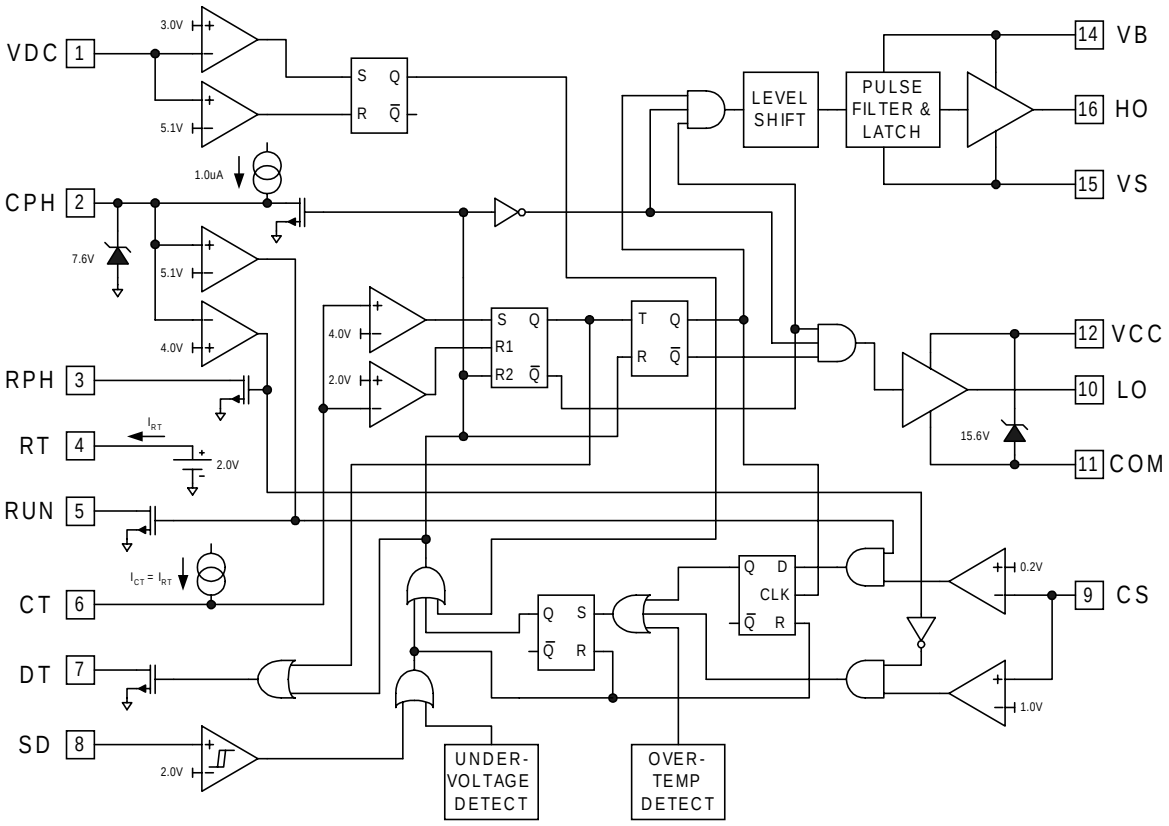
Data shown in this table is subject to change. Please consult latest product data sheets for latest specifications

3. The IR2157 as an Advanced Variable Frequency Control IC

What is the IR2157 ?

The IR2157 Control IC is primarily intended to act as the core of a high frequency Electronic Ballast. The device Integrates a variable frequency oscillator, control functions and half-bridge drive delivering extremely low component count, reliability and reduced manufacturing costs. However many of the features incorporated in the IR2157 will benefit other applications, especially when resonant loads are involved. In this respect, the device can be categorised as an advanced Self-Oscillating Control IC suitable for more general application areas.

Figure 4 : IR2157 Block Diagram



What applications suit the IR2157 ?

Beyond the primary use as an Electronic Ballast control IC, the IR2157 will demonstrate advantages in several applications where a variable frequency half bridge drive is required. For example, resonant mode circuits require frequency modulation and are increasingly found in high performance AC/DC power supplies.

As an advanced Self-Oscillating Control IC, how does IR2157 compare with IR2153 ?

In addition to IR2153 features noted in the prior section, the IR2157 offers the following enhancements for designs using resonant or inductive loads.

- Dynamically programmable dead-time
- Precise 50% duty cycle
- Variable frequency oscillator with sequential state control logic
- Programmable, high frequency start
- Fault shutdown with auto-restart

What is the advantage of dynamically programmable dead-time ?

Self-Oscillating Control IC's such as IR2153 are available with several dead time options, however this parameter is fixed on-chip for all 8-pin ICs. IR2157 dead-time may be programmed with a single resistor and can therefore be tailored to the optimum value for zero-voltage switching or to meet other requirements.The control signal is ground referenced, so dynamic modulation of dead-time is convenient.

Why is the duty cycle precisely set at 50% ?

When driving capacitively coupled resonant loads, such as the series-resonant load circuit of an Electronic Ballast, it is often important to maintain duty cycle at 50%. Departure from this duty ratio can couple a low frequency 'envelope' to the resonant load through the comparatively low impedance DC blocking capacitor.The resulting low-frequency modulation produces unwanted harmonics in the load and may saturate magnetics, if sufficiently extreme.

The IR2157 achieves 50% duty cycle by operating the oscillator at twice the frequency of other Self-Oscillating Control IC's. A T-type toggle flip-flop is used prior to the drive stage to accomplish this. 50% duty cycle can be maintained with IR2153, however precise control becomes difficult in practice with these parts if variable frequency is also required. Design-tip DT98-1 details this topic.

In what ways are the oscillator of IR2153 and IR2157 different ?

The oscillator onboard Control IC's such as IR2153 is similar in some ways to the industry standard '555, except that the timing capacitor of IR2153 is both charged and discharged from the same pin. In applications that require fixed frequency 50% duty cycle the circuit is completed using a timing resistor connected between the oscillator output pin, Rt and the top plate of the timing capacitor. The Rt pin can source and sink current and under normal loading switches between Vcc and COM. A different approach is adopted by IR2157 in which a highly stable on-chip current mirror is used to derive charging current for the timing capacitor.

With IR2157, timing capacitor discharging occurs via a separate path to ground that does not involve the current mirror and this period controls dead-time. The sum of these two periods determines the run frequency. Charging time is controlled only by current flowing to ground (sink current) so frequency may be controlled with a programmable, ground referenced current sink. This can be practically implemented with a simple n-channel MOSFET or small signal bipolar transistor.

In Electronic Ballast application, the IR2157 oscillator is controlled by onboard state control logic. This logic drives integrated open-drain switches to connect resistors or simple R/C networks to ground at the appropriate time. This process can be duplicated using common emitter connected transistors controlled by an external circuit. Closed-loop regulation can also be achieved in this way using an op-amp or a linear programmable shunt such as 3-pin TO-92 packaged TL431.

What is the benefit of programmable, high frequency start ?

The IR2157 state logic provides a programmable duration, high frequency start. This is useful in cases where the resonant load is coupled to the half bridge through a DC blocking capacitor. Initial operation well above the resonant point ensures low current flow in the primarily inductive resonant tank circuit. This helps to eliminate unwanted spikes, saturation of magnetic components and allows time for the DC blocking capacitor to acquire static charge necessary for steady state operation.

3. ESD, Latch Immunity and Hidden Value within IR Control ICs

What is ESD and what can it do ?

Static charge is something we're all familiar with. A form of potential energy generated by friction between moving materials and gases such as air and stored on both objects and people. Electro Static Discharge occurs when this stored charge finds a path through the IC, either by direct contact with pins or indirectly via dielectric breakdown (spark) usually through air. In manufacturing environments, devices are generally at greatest risk from ESD damage during handling or automatic insertion when they are removed from packaging but not yet electrically connected with the remainder of the system. When soldered in place, semiconductors are *usually* reasonably well protected because potential conducting paths through the chip are often bridged. Left Unchecked, ESD can produce effects ranging from slight parameter shifts to complete destruction and all levels of damage between these two extremes.

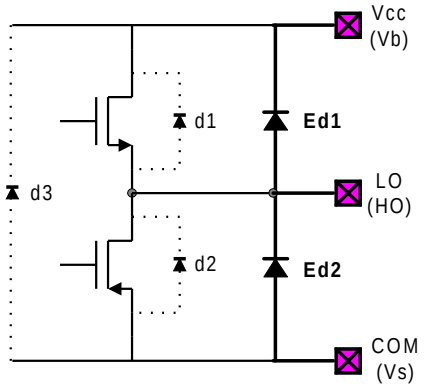
What can be done to reduce the risk of damage from ESD ?

Anti-Static precautions and working regime should always form the primary barrier against ESD because these actions tackle the issue at source. However, all semiconductor manufacturers can influence ESD immunity of their product, though there is usually an additional cost associated with higher levels of protection. International Rectifier applies extremely conservative design margins and special circuit design techniques to maximise ESD immunity. Though ESD is given separate consideration, design philosophies adopted to increase latch-up immunity further benefit ESD reselience.

What is CMOS latch-up ?

As in circuit design, building blocks used to create any IC inherently contain parasitic elements that occur consequentially rather than by choice. For example, MOSFETs always contain a parasitic diode between drain and source. Parasitic elements can be useful, irrelevant or disadvantageous, depending on where and what they are used for in circuit. Common to the basic building blocks of all CMOS IC's is an undesirable parasitic structure that can latch in the conducting state in a similar way to an SCR (thyristor) under some abnormal circumstances. Latch-up is a failure mode that is said to occur if the SCR shown in figure 1 is triggered. It can be avoided by careful design of both the IC itself and peripheral circuitry.

Figure 5 : Simplified Parasitic Structure of CMOS IC Output Buffer



What can happen as a result of CMOS latch-up ?

During latch-up in any CMOS IC uncontrolled currents can flow within the IC through the parasitic SCR structure. This can cause permanent damage to the chip, loss of functionality or undefined behavior. If latch-up occurs when bias is derived from a weak supply which would easily collapse under abnormal loading, the IC may recover when the bias supply is recycled, however cummulative damage or undefined operation are still possible under these circumstances. Also possible is a situation in which the IC is destroyed as a second order effect. For example: Undefined operation ->MOSFET damage -> IC damage.

How does International Rectifier add value in CMOS latch-up prevention ?

As with ESD immunity measures, all semiconductor manufacturers can influence latch immunity of their product, though there is usually an additional cost associated with higher levels of protection. International Rectifier applies extremely conservative design margins and special circuit techniques to maximise latch immunity. Though latch immunity is given separate consideration, design philosophies adopted to increase ESD immunity further benefit latch-up reselience. Output buffers used in International Rectifier Control ICs provide latch immunity to +/- 500mA. This is considered to be an excellent level of protection.

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DESIGN TIP

DT 98-2a

International Rectifier • 233 Kansas Street, El Segundo, CA 90245 USA

Bootstrap Component Selection For Control IC's

By Jonathan Adams

TOPICS COVERED

Operation Of The Bootstrap Circuit
Factors Affecting The Bootstrap Supply
Calculating The Bootstrap Capacitor Value
Selecting The Bootstrap Diode
Layout Considerations

1. OPERATION OF THE BOOTSTRAP CIRCUIT

The V_{bs} voltage (the voltage difference between the V_b and V_s pins on the control IC) provides the supply to the high side driver circuitry of the control IC's. This supply needs to be in the range of 10-20V to ensure that the Control IC can fully enhance the MOS Gated Transistor (MGT) being driven, some of International Rectifier's Control IC's include undervoltage detection circuits for V_{bs}, to ensure that the IC does not drive the MGT if the Vbs voltage drops below a certain voltage (V_{bsuv} in the datasheet). This prevents the MGT from operating in a high dissipation mode.

This V_{bs} supply voltage is a floating supply that sits on top of the Vs voltage (which in most cases will be a high frequency square wave). There are a number of ways in which the V_{bs} floating supply can be generated, one of these being the bootstrap method described here in this design tip. This method has the advantage of being simple and inexpensive but has some limitations, duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor (long on-times and high duty cycles require a charge pump circuit - see Application Note AN978). The bootstrap supply is formed by a diode and capacitor combination as shown in fig 1).

The operation of the circuit is as follows. When V_s is pulled down to ground (either through the low side FET or the load, depending on the circuit configuration), the bootstrap capacitor (C_{bs}) charges through the bootstrap diode (Dbs) from the 15V Vcc supply. Thus providing a supply to V_{bs}.

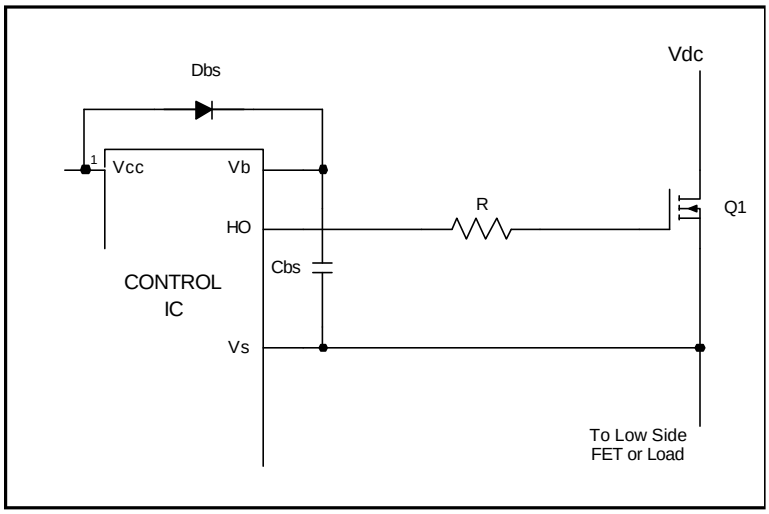


Fig 1) Bootstrap Diode/ Capacitor circuit used with IR Control IC's

2. FACTORS AFFECTING THE BOOTSTRAP SUPPLY

There are five influencing factors which contribute to the supply requirement from the V_{bs} capacitor. These are:

1. Gate Charge required to enhance MGT
2. I_{qbs} - quiescent current for the high side driver circuitry
3. Currents within the level shifter of the control IC
4. MGT gate-source forward leakage current
5. Bootstrap capacitor leakage current

Factor 5 is only relevant if the bootstrap capacitor is an electrolytic capacitor, and can be ignored if other types of capacitor are used. Therefore it is always better to use a non-electrolytic capacitor if possible.

3. CALCULATING THE BOOTSTRAP CAPACITOR VALUE

The following equation details the minimum charge which needs to be supplied by the bootstrap capacitor:

$$Q_{bs} = 2Q_g + \frac{I_{qbs(\max)}}{f} + Q_{ls} + \frac{I_{Cbs(leak)}}{f} \qquad \text{EQ(1)}$$

where:

Q_g=Gate charge of high side FET f=frequency of operation
$I_{cbs(leak)}$=Bootstrap capacitor leakage current
Q_{ls} = level shift charge required per cycle = 5nC (500V/600V IC's) or 20nC (1200V IC's)

The bootstrap capacitor must be able to supply this charge, and retain its full voltage, otherwise there will be a significant amount of ripple on the V_{bs} voltage, which could fall below the V_{bsuv} undervoltage lockout, and cause the HO output to stop functioning. Therefore the charge in the C_{bs} capacitor must be a minimum of twice the above value. The minimum capacitor value can be calculated from the equation below.

$$C \geq \frac{2\left[2Q_g + \frac{I_{qbs(\max)}}{f} + Q_{ls} + \frac{I_{Cbs(leak)}}{f}\right]}{V_{cc} - V_f - V_{LS} - V_{Min}} \qquad \text{EQ(2)}$$

Where:

V_f = Forward voltage drop across the bootstrap diode V_{LS} = Voltage drop across the low side FET (or load for a high side driver)

V_{Min} = Minimum voltage between V_B and V_S

IMPORTANT NOTE: The C_{bs} Capacitor value obtained from the above equation EQ(2) is the absolute minimum required, however due to the nature of the bootstrap circuit operation, a low value capacitor can lead to overcharging, which could in turn damage the IC. Therefore to minimize the risk of overcharging and further reduce ripple on the V_{bs} voltage the C_{bs} value obtained from the above equation should be should be multiplied by a factor of 15 (rule of thumb).

The C_{bs} capacitor only charges when the high side device is off, and the Vs voltage is pulled down to ground. Therefore the on time of the low side switch (or the off time of the high side switch for a high side driver) must be sufficient to ensure that the charge drawn from the C_{bs} capacitor by the high side driver, can be fully replenished. Hence there is inherently a minimum on time of the low side switch (or off time of the high side switch in a high side driver). Also in a high side switch configuration where the load is part of the charge path, the impedance of the load can have a significant effect on the charging of the C_{bs} bootstrap capacitor - if the impedance is too high the capacitor will not be able to charge properly, and a charge pump circuit may be required (see Application Note AN978).

4. SELECTING THE BOOTSTRAP DIODE

The bootstrap diode (D_{bs}) needs to be able to block the full power rail voltage, which is seen when the

high side device is switched on. It must be a fast recovery device to minimize the amount of charge fed back from the bootstrap capacitor into the Vcc supply, and similarly the high temperature reverse leakage current would be important if the capacitor has to store charge for long periods of time. The current rating of the diode is the product of the charge calculated from equation EQ(1) and the switching frequency.

Therefore:

Diode Characteristics

V_{RRM} = Power rail voltage
max t_{rr} = 100ns
I_F = Q_{bs} x f

5. LAYOUT CONSIDERATIONS

The Bootstrap capacitor should always be placed as close to the pins of the IC as possible (as shown in Fig 2 on the left).

At least one low ESR capacitor should be used to provide good local de-coupling, e.g. a separate ceramic capacitor close to the IC would be essential if an aluminum electrolytic capacitor is used for the bootstrap capacitor. If the bootstrap capacitor is either a ceramic or tantalum type, this should be sufficient in itself as the local decoupling.

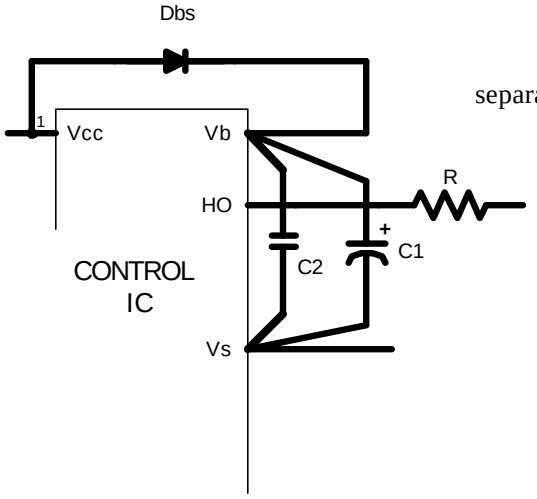


Fig 2) Recommended layout of the Bootstrap Components

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Design Tip for *QUIETIR*™

QUIETIR™ Series Used in DC Motor Chopper Applications

By Ugo Robino and Alberto Guerra

Topics covered:

The Problem
Customer Solution
The Efficiency Improvement
Other Benefits

1. THE PROBLEM

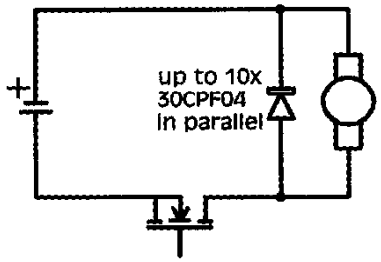
The application of the fast recovery rectifier as freewheeling diode to re-circulate the current, and then to prevent the overvoltage across a switch (i.e., IGBT, HEXFET) may be frequently a pain when, due to unexpected snappy recovery characteristic, a large amount of voltage spikes (then noise) are produced, resulting in the requirement of snubber elements properly mounted to attain noise reduction.

Moreover, when the diode is also required to conduct a large amount of forward current, the unbalanced trade-off "speed Vs forward voltage drop" usually adds power dissipation problems. This is the typical case for applications for speed control of DC motor.

The new Quiet*IR* series 30CPF.. has been proven to be the right solution versus traditional Ultra Fast devices in choppers operating below 20kHz up to 400A.

2. CUSTOMER SOLUTION

Traditionally, the DC Motor Control uses the "Chopper" topology with PWM control to properly "chop" the DC voltage and then regulate the motor speed. The following schematic shows the basic configuration.



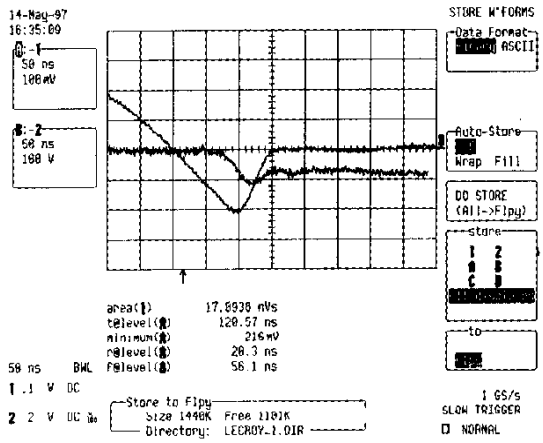
The design implemented in the customer system solution adopts the same well-known topology and uses for the diode cell 1, 2, 4, 6, 8 and even 10 (for the highest power level) diodes 30CPF04 in parallel.

The systems operate with a duty cycle up to 95% at 16kHz with a maximum output current in the ranges from 50 to 400Apk.

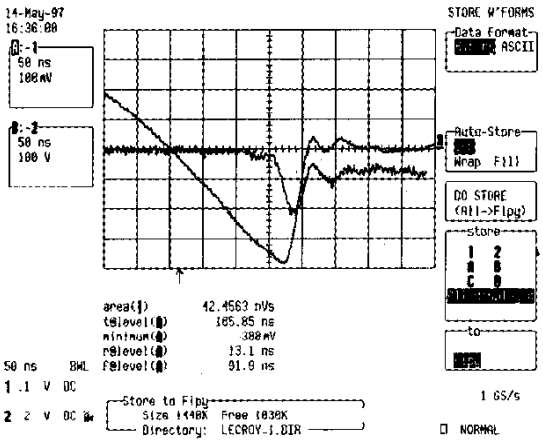
3. THE EFFICIENCY IMPROVEMENT

Under the customer conditions, previous diode devices showed snappier characteristics, while the 30CPF04 is a very smooth one. The following figures (on page 2) show the clear comparison with the *QUIETIR* recovery waveform under the same switching conditions.

30CPF.. series



Brand "A" series



The substantial improvement of the snap factor (tb/ta) from 0.34 to 0.66 is a major contributor in the reduction of the snubber circuit (RC networks) needed to clamp the voltage spikes and then the noise.

4. OTHER BENEFITS

Due to the specific diffused Moat Structure and the die bonding technique, all *QUIETIR* diodes show an unprecedented stability of performances with time and stresses, moreover, the 30CPF series with the specific T0-247 3-pin ouline allows a drop-in replacement for common cathode diodes (used in parallel to achieve higher current density) offering a lower V_f.

The customer also has the opportunity to reduce design time and effort for all new and old systems that use traditional control configurations without the need to change layout for the power stage.

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Design Tip for *SAFEIR*™

QUIETIR™ Series Used in High Frequency Welding Applications

By Ugo Robino and Alberto Guerra

Topics covered:

The Problem
Customer Solution
The Efficiency Improvement
Benefits

1. THE PROBLEM

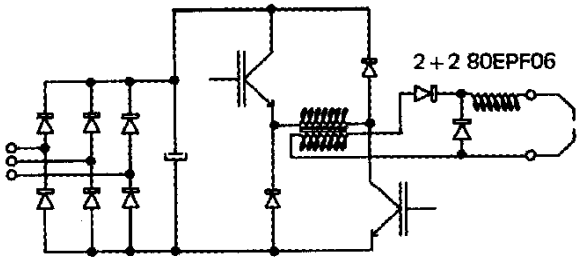
The HF welding equipment manufacturers are quickly converting the current product designs into more efficient, lighter, better controlled, and less noisy systems. The switching frequency range now adopted is rapidly reaching 30-40-50kHz and, where possible, even higher. The output rectifier stage is a major contributor of the overall system efficiency.

The total welding current is "rectified" by the center tap cell in the output stage, and then the conduction and switching losses of the diodes are the key elements in the selection of the "best" component solution. The softness of the output diodes is also a fundamental element to minimize the voltage spikes induced by the stray inductance. The new *QUIETIR* series 80EPF.. has been proven to be the right solution versus traditional Ultra Fast devices in low-medium power welders below 50kHz.

2. CUSTOMER SOLUTION

Traditionally, the HF welders for low-medium power range (below 300A) use a typical "Dual forward" topology for the switching stage.

The following schematic shows the basic configuration.



The Actual design, adopting the same well know topology, uses for the output stage 2+2 80EPF06 (2 in parallel per leg), and operates with a duty cycle of 40% at 30kHz with a maximum output current of 140A.

3. THE EFFICIENCY IMPROVEMENT

Under the customer conditions, the power losses at the maximum duty cycle operation can be compared with an equivalent 80A 600V Ultra fast diode used by the customer as an alternative during the design phase.

The IR 80EPF06 series in the application conditions, dissipate a total of (P_{off} is calculated with a V_R of 80V and f = 30kHz),
$P_{on} + P_{off} = 42 + 9$,
then for all 4 units an average power loss of **204W**.

The "equivalent" Ultra fast (80A, 600V) device dissipates a total of
$P_{on} + P_{off} = 55W + 3W$,
then for all 4 units an average power loss of **232W.**

Thus a total saving of 14% in power losses and lower operating T_{case}, due to the better thermal resistance 0.3 °C/W vs. 0.4°C/W.

4. BENEFITS

It is clear how the better efficiency automatically means more output current with the same number or components (or lower temperature operation) and is considered an important benefit, however, several others benefits are connected to this application, including lower cost.

Due to the specific diffused Moat Structure and the die bonding technique, the *QUIETIR* diodes show an unprecedented stability of performances with time and stresses. In particular, the V_f (forward voltage drop) remains within a few millivolts drift from the initial value after long severe power cycling.

Another is the large current rating of welders required to parallel several output diodes, which are needed to maintain their initial V_f matching to prevent unbalanced current sharing during the life of the equipment. This is ideally ensured by the 80EPF which guarantees no change in the original V_f matching established at the time of the assembling.

Real test performed at 60A on several units (100 pcs.) under the extreme severe condition, $\Delta T_j > 100°$, t_{on} = 4 min., t_{off} = 6 min., showed a ***maximum mutual drift of 6mV (pair of diodes) and a total of 25mV deviation among all units after 2000 Hrs. of "stress"!***

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Design Tip for *QUIETIR*™

EMI Reduction Using *QUIETIR*™

By Ugo Robino and Alberto Guerra

Topics covered:

The Problem
Traditional Solution
A Different Approach
Benefits

1. THE PROBLEM

At present, international standards on Electro-Magnetic Interference (EMI), such as IEC 1000, and EN 50081 series, limit drastically the disturbances conducted on the public network by any electrical equipment.

The range of frequencies of interest is 150kHz to 30MHz. In rectifying circuits, there are different sources of noise in this range of frequencies.

A source of noise is usually the input diode bridge. The specific cause of noise is the recovery process of the diode at the end of the conduction period

2. TRADITIONAL SOLUTION

One typical solution used to reduce the emission of noise into the public network is the insertion of EMI filters at the input of the bridge.

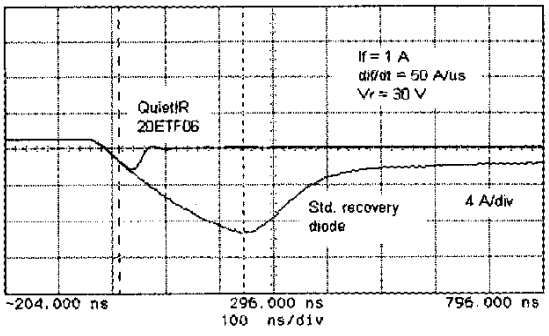
Another approach is the insertion of capacitors in parallel with the diodes of the bridge. A capacitance in parallel on each diode is provided to smooth the recovery current and voltage transients across the diode itself. For this application, standard recovery diodes are the common choice.

3. A DIFFERENT APPROACH

The problem of reduction of EMI conducted noise has been faced by IR introducing the *QUIETIR* family of diodes.

QUIETIR are fast and soft recovery diodes that are used for rectification purposes. Using fast diodes in input bridges is a new approach that gives the following advantages:

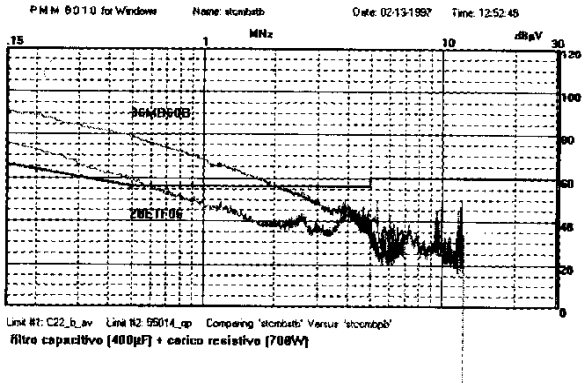
Reduction of the noise emission at recovery, consequent to the reduction of the reverse peak current and the reverse recovery time (see figure below).



This is particularly important whenever stray inductances are present in the circuit.

Elimination of the capacitor in parallel with the diodes, whenever the specific application requires this solution in the presence of standard recovery diodes.

An example of noise reduction using a 20ETF06 diode is given in the figure to the right, where the frequency plots of emitted noise for two comparing diodes are reported.



The plots have been obtained for a rectifying circuit with a bridge, a filter capacitor of 400µF, and a resistive load of 700W. It can be easily recognized that the 20ETF06 diode provides a reduction of approximately 25dB in the most interesting frequency range of 150kHz to 2MHz.

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Design Tip for *SAFEIR*™

Line Surges in Input Rectifiers

By Ugo Robino and Alberto Guerra

Topics covered:

The Problem
Traditional Solution
A Different Approach
Benefits

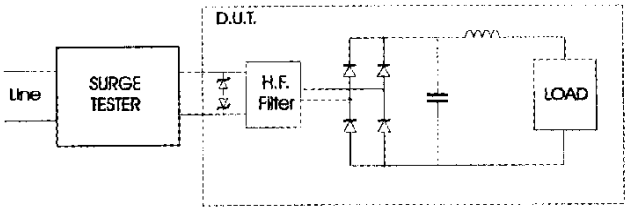
1. THE PROBLEM

Supply networks are subjected to current and voltage transients, caused by lightning and turning-off of highly inductive loads. These disturbances can cause severe damages to electronic equipment.

For the purpose of constructing equipment that can safely withstand the traansients present in actual networks, international standards have been prepared to define laboratory reference test conditions. These standards are becoming, in Europe, more and more mandatory for any kind of electrical and electronic equipment. The basic standard IEC 1000-4-5 (adopted in Europe by CENELEC as EN 61000-4-5) requires that the equipment will sustain pulses from 1000 to 4000V, according to the specific application with duration of 50μs, on an impedance of 2Ω. This voltage pulse, applied to low impedance circuits, becomes a current pulse from 500 to 2000A with 20μs duration.

2. TRADITIONAL SOLUTION

When the input bridge of a rectifying circuit is subjected to a surge pulse, as described, it behaves differently depending on the configuration of the circuit connected to the bridge. A typical circuit, including voltage suppressors, EMI filter, bridge, output filter, and load is shown in the figure below.



When an inductor is present, the bridge is stressed by a voltage spike superimposed to the peak value of the line voltage (e.g., 220x1.41+1000V ≈ 1300V). When a capacitor (> 50μF) is present, this behaves as a voltage clamp, and the input bridge is consequently subjected to a current surge (e.g., for a 1000V pulse, a current pulse of 500A with 20μs duration will result.

In order to withstand these stresses, in traditional circuits, some kind of voltage suppressor is inserted in front of the input bridge, to clamp the voltage spikes. In any case the diodes in the bridge must be able to withstand the current pulse. As diodes are not characterized for short (20μs) pulses of high peak current (> 500A), circuit designers are forced to keep large margins on diode current capability, and arrange a lot of laboratory tests to ensure an appropriate reliability of the circuit.

3. A DIFFERENT APPROACH

As the problem to respond to international EMC standards is becoming more and more important, IR pursues the objective to supply components fully characterized as able to sustain voltage and current pulses according to IEC regulations. In particular, using diodes of the *SAFEIR* family, there is no more need to characterize the circuit, as they are fully characterized for short current pulses (20μs) and voltage spikes (50μs).

For example, the 10ETS16 standard recovery diode guarantees to sustain 1000V pulses with any rectifier topology and 4000V pulses in the case of the capacitor topology, with no use of any voltage suppressor. In this conditions, the current pulse sustained is in excess of 2000A over 20μs. Using these devices, the circuit designer can completely avoid the characterization of his or her input bridge circuit for compliance to the IEC 1000-4-5 standards.

4. BENEFITS

1) **Cost reduction:** An overall cost reduction of the system derives from the elimination of the voltage suppressor and no more need of overdimensioning the input diodes with respect to their current rating.

2) **Smaller dimensions and lighter weight:** The overall size of the circuit can be reduced for the same reasons of point 2.

3) **System more rugged and reliable:** By definition, the system is more rugged and reliable, as IR guarantees that all the diodes will sustain the voltage and current pulses.

4) **Reduction of design time and development effort:** The characterization of the IR diodes according to IEC standards reduces substantially the time required to the circuit designer for test and characterization, and removes the need to make EMC tests at specialized laboratories.

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DESIGN TIP

DT 97-3

International Rectifier • 233 Kansas Street, El Segundo, CA 90245 USA

Managing Transients in Control IC Driven Power Stages

By Chris Chey and John Parry

Topics covered:

Control IC Product Range
Parasitic Elements of the Bridge Circuit
V_S Undershoot: Cause
V_S Undershoot: Effects on the Control IC
Avoiding Latch-Up
Monitor and Verify
General Recommendations
Boosting V_S Undershoot Immunity
Appendix 1. IR2110 Parasitic Diode Structure

1. CONTROL IC PRODUCT RANGE

International Rectifier offers a broad range of control ICs from single channel to complete three-phase bridge drivers. All types employ high-integrity level shifting techniques to simplify control of power transistors from logic circuits. Our latest products further enhance this capability to drive power switches relatively displaced by up to 1200V.

As leading edge performance demands switching more current at ever higher speeds, the unwanted effects of parasitics are magnified and warrant heightened attention. The aim here is to locate their source, quantify the immunity of the IC against a potentially troublesome effect and finally, show how to maximize the margin between the two.

2. PARASITIC ELEMENTS OF THE BRIDGE CIRCUIT

The circuit shown in figure 1 depicts a typical application in which two power MOSFETs are driven by a control IC in a half bridge configuration. Unwanted inductance in the power circuit from die bonding in the transistors, pinning and PCB tracks are lumped together and arbitrarily labeled LS1,2 and LD1,2.

Further parasitics will exist in the gate drive circuit and these should also be considered during circuit layout but for now, we will focus on the bridge itself as the highest currents and di/dt will occur here. During switching, rapidly changing bridge current induces voltage transients across all parasitics shown. Left unchecked, these transients may couple into other circuits causing noise problems, increased switch dissipation or even IC damage in extreme cases.

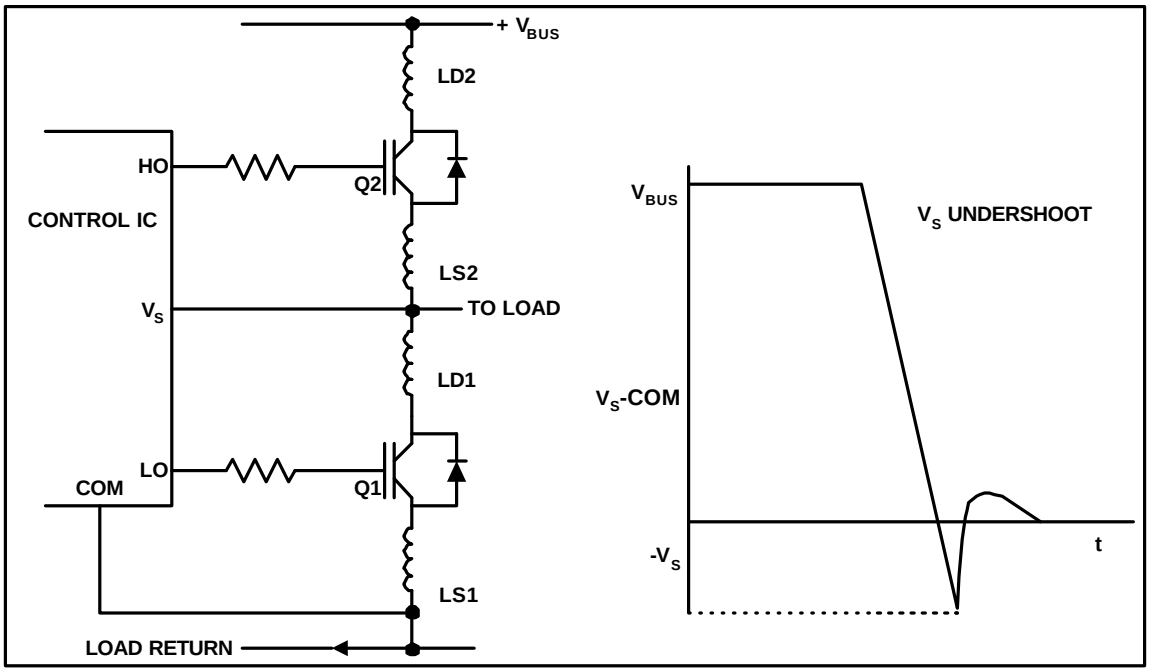


Figure 1. Parasitic Elements of the Half Bridge

3. V_S UNDERSHOOT: CAUSE

Of the problems caused by parasitics, one of the main issues for control ICs is a tendency for the V_S node to undershoot ground following switching events. Conversely, overshoot does not generally cause a problem due to the high differential voltage capability of International Rectifier's proven HVIC process.

With inductive loading of the bridge, high side transistor turn-off causes load current to suddenly flow in the low side free-wheeling diode. On top of the 'slack' from diode turn-on delay and forward voltage drop, stray inductance LS1+LD1 contribute to undershoot of the Vs node beyond ground, as shown in the graph of figure 1. If the load circuit does not totally self-commutate in the dead-time (both transistors off) V_S undershoot or ringing may occur when the low side device is hard switched.

4. V_S UNDERSHOOT: EFFECTS ON THE CONTROL IC

International Rectifier control ICs are guaranteed completely immune to V_S undershoot of at least 5V, measured with respect to COM. If undershoot exceeds this level, the high side output will temporarily latch in its current state. Provided V_S remains within absolute maximum limits the IC will not suffer damage, however the high-side output buffer will not respond to input transitions while undershoot

persists beyond 5V. This mode should be noted but proves trivial in most applications, as the high-side is not usually required to change state immediately following a switching event.

5. AVOIDING LATCH-UP

The parasitic diode structure for a typical control IC is shown in appendix 1. - As with any CMOS device, driving any of these diodes into forward conduction or reverse breakdown may cause parasitic SCR latch-up. The ultimate outcome of latch-up often defies prediction and can range from temporary erratic operation to total device failure.

The control IC may also be damaged indirectly by a chain of events following initial overstress. By way of example, latch-up could conceivably result in both output drivers assuming a high state, causing cross-conduction followed by switch failure and finally catastrophic damage to the IC. This failure mode should be considered a possible root cause if power transistors and/or control IC are destroyed in the application.

The following theoretical extremes can be used to help explain the relationship between excessive V_S undershoot and the resulting latch-up mechanism.

In the first case an 'ideal bootstrap' circuit is used in which V_{CC} is driven from a zero-ohm supply with an ideal diode feeding V_B. Undershoot now sums with Vcc causing the bootstrap capacitor to overcharge as shown in figure 2. By way of example, if V_{CC} =15V then V_S undershoot in excess of 10V forces the floating supply above 25V, risking breakdown in diode D1 and subsequent latch-up. Suppose now that the bootstrap supply is replaced with the ideal floating supply of figure 3 such that V_{BS} is fixed under all circumstances. Note that using a low impedance auxiliary supply in place of a bootstrap circuit can approach this situation.

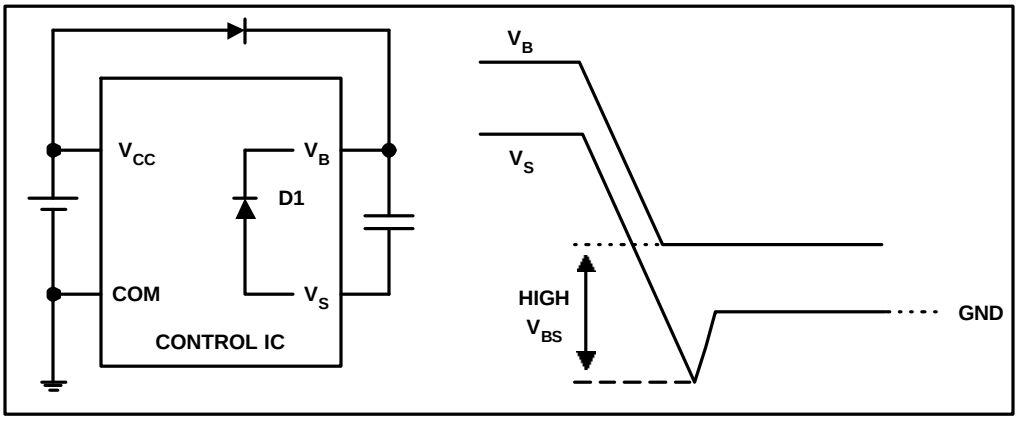


Figure 2. Case 1: Ideal Bootstrap Circuit

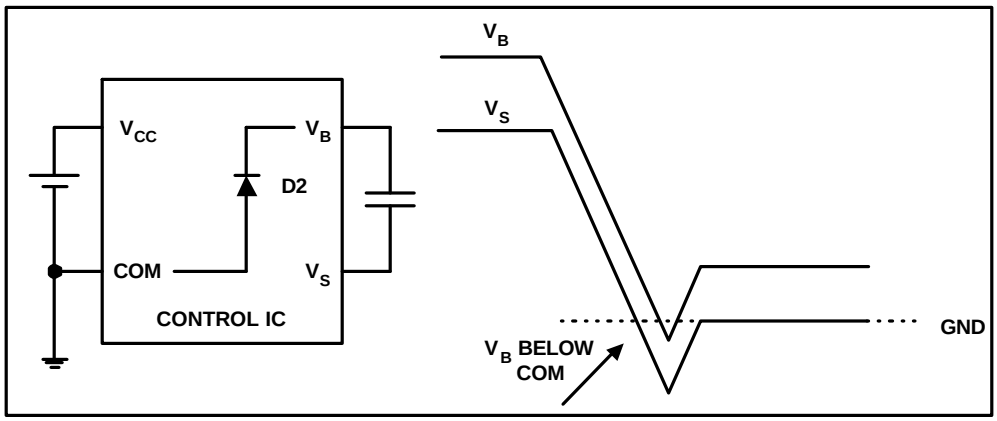


Figure 3. Case 2: Ideal Floating Supply

This time, latch-up risk appears if V_S undershoot exceeds V_{BS}, since parasitic diode D2 will ultimately enter conduction.

A practical circuit is likely to fall somewhere between these two extremes, resulting in both a small increase of V_{BS} and some V_B droop below V_{CC} as depicted by Figure 4.

Exactly which of the two extremes is prevalent can be checked as follows.

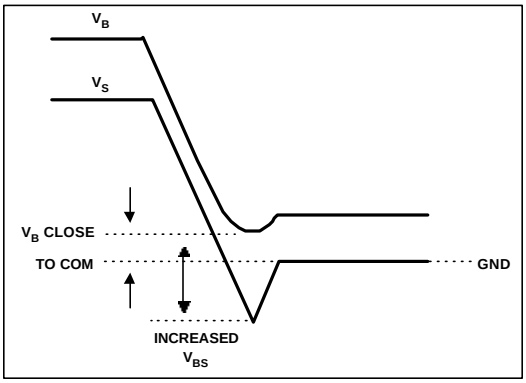


Figure 4. Typical Response

6. MONITOR AND VERIFY

The signals listed below should be observed both in normal operation and during high-stress events such as short circuit or over current shutdown, when di/dt is highest. Readings should always be taken directly across IC pins as shown in figure 5, so that contributions from parasitics in the drive coupling are included in the measurement.

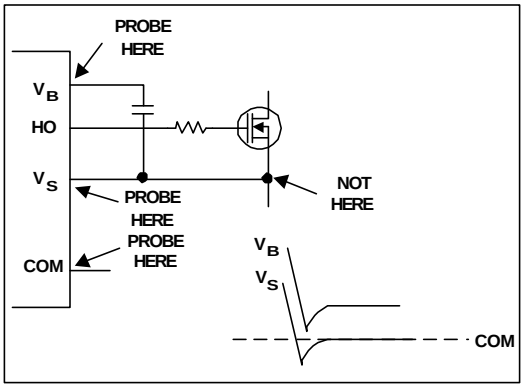


Figure 5. Measurement Points

Measurements to verify undershoot severity

(1) High side offset with respect to common; V_S-COM
(2) The floating supply; V_B - V_S

Most bridge circuits employ a bus of several hundred volts which means selecting an insensitive Y-axis scale to prevent distortion from saturation of the input amplifier. This can make the comparatively small Vs undershoot difficult to quantify.
For best resolution, check your oscilloscope manual and then select the highest useable sensitivity level.

For the second measurement, the signal of interest is permanently superimposed on the changing bridge voltage. The oscilloscope may be floated with a transformer, but this method is discouraged because capacitive loading can alter circuit performance and sometimes mask underlying problems by inadvertently reducing dv/dt.

A high-bandwidth differential voltage probe (or an isolated differential-input oscilloscope) can give good results here, allowing other ground referenced signals to be viewed at the same time. However, be aware of propagation delay mismatch between differential and conventional probes when comparing relative event times.

Always measure the noise floor prior to making measurements. Common-mode noise on high side referenced signals (Vb,HO) can be observed by joining probe tip and ground lead directly to the Vs node.

Do not assume that 'low-side' referenced signals are free from common-mode noise. Measure the noise floor by joining probe tip and ground lead together at the COM node.

7. GENERAL RECOMMENDATIONS

The following guidelines represent good practice in control IC circuits and warrant attention regardless of the observed latch-up safety margin. Design tip DT94-15 'Design Check List for IR21xx MGDs' may be consulted for pictorial representation of the suggestions listed below.

Minimize the parasitics of figure 1

1a. Use thick, direct tracks between switches with no loops or deviation.
1b. Avoid interconnect links. These can add significant inductance.
1c. Reduce the effect of lead-inductance by lowering package height above the PCB.
1d. Consider co-locating both power switches to reduce track lengths.

Reduce control IC exposure.

2a. Connect V_S and COM as shown in figure 6.
2b. Minimize parasitics in the gate drive circuit by using short, direct tracks.
2c. Locate the control IC as close as possible to the power switches.

Improve local decoupling.

3a. Increase the bootstrap capacitor (Cb) value using at least one low-ESR capacitor. This will reduce overcharging from severe Vs undershoot. See Design Tip DT98-2 for more information

3b. Use a second low-ESR capacitor from Vcc to COM. As this capacitor supports both the low-side output buffer and bootstrap recharge, we recommend a value at least ten times higher than Cb.

3c. Connect decoupling capacitors directly across appropriate pins as shown in figure 7.

3d. If a resistor is needed in series with the bootstrap diode, verify that V_B does not fall below COM, especially during start-up and extremes of frequency and duty cycle.

Granted proper application of the above guidelines, the effects of V_S undershoot will be minimized at source. If the level of undershoot is still considered too high, then some reduction of dv/dt may be necessary.

External snubbing and/or increasing gate drive resistance may be used to trade efficiency for lower switching rate. If the system will not tolerate this, then fast anti-parallel clamping diodes may be considered appropriate. HEXFRED diodes are ideal for this purpose.

8. BOOSTING V_S UNDERSHOOT IMMUNITY.

If the key signals measured fall within specified limits under worst case conditions, then no further action should be necessary. However, in very noisy environments, where Vs undershoot remains excessive despite the measures above, then further steps may be taken to increase control IC tolerance. We recommend two different methods for improving undershoot immunity.

Method A:

A resistor between the V_S pin and the bridge center may be used to limit the current flow into the Vs pin during undershoot. This method is viable for resistor values of around 5 Ohms or less.

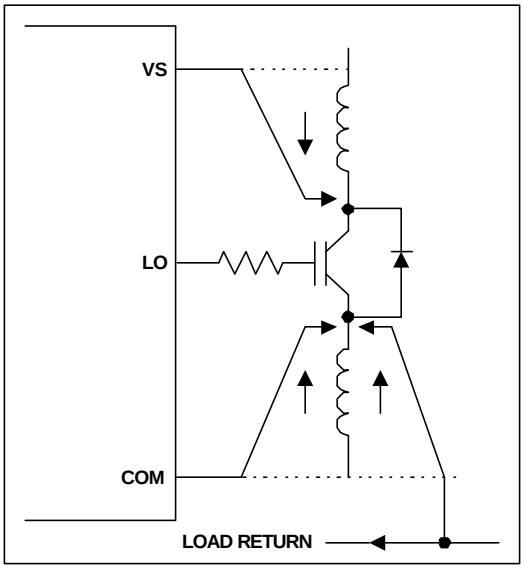


Figure 6. Bypass Parasitics

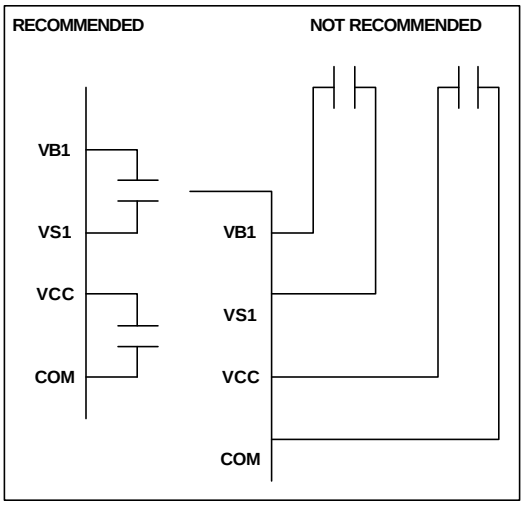


Figure 7. Decoupling Capacitor Location

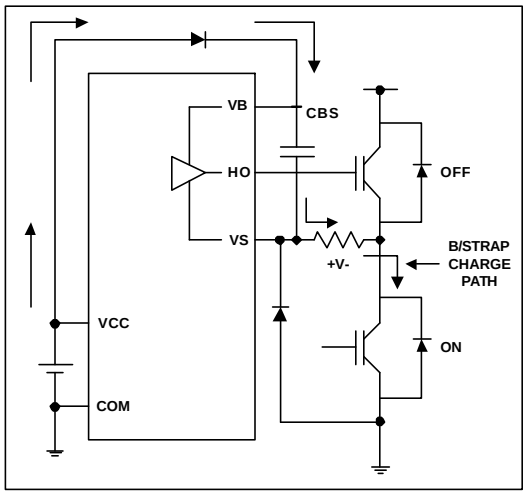


Figure 8. Boosting Immunity Method A

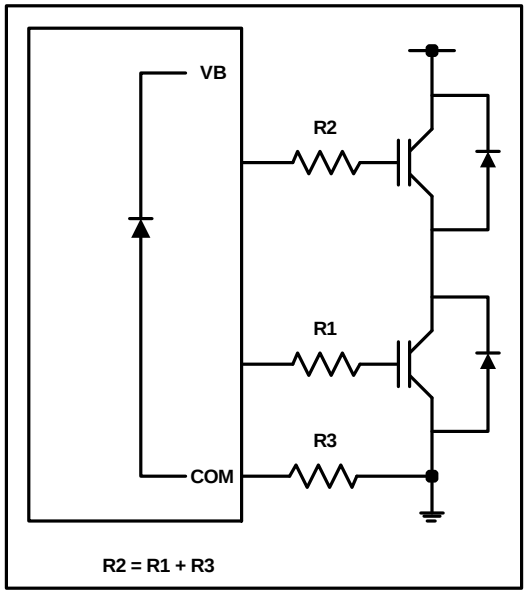


Figure 9. Boosting Immunity Method B

Since the bootstrap capacitor charges through this resistor, as shown in figure 8, inadvertent shoot-through may occur at start-up if the value is too high. If there is a series gate resistor, this should be reduced in value so the nett gate resistance of both high and low side transistors remains equal.

Method B:

By way of an alternative approach, we also recommend the insertion of a single resistor between COM and the low side source or emitter as depicted by figure 9. Since the bootstrap capacitor is not charged through the resistor, this method grants flexibility to choose a higher resistance and afford greater protection to the control IC.

A resistor in this location has the effect of limiting peak current flow in the 600V diode D2 shown in figure 3. Again, drive symmetry requires that the total resistance in both gate drive circuits be equal, so the low-side gate resistor should be slightly reduced to accomplish this.

Note:

When using control ICs which do not have a separate logic ground, i.e. those which share COM for both input and output ground references, either of the two methods discussed may be applied. However, care should be taken to ensure that logic inputs fall within the permitted levels.

9. APPENDIX 1.

IR2110 PARASITIC DIODE STRUCTURE

The parasitic diode structure of the IR2110 control IC is shown in Figure 10. This is, in essence, a pictorial representation of our Absolute Maximum Ratings table.

The IR2110 has separate logic and output supply rails, however, these rails are combined in some control IC types due to pinning restrictions.

Further details on the parasitic diode structure and latch-up mechanism may be found in design tip DT94-9A, 'Maximizing Latch Immunity of the IR2151 and IR2152 In Ballast Applications'

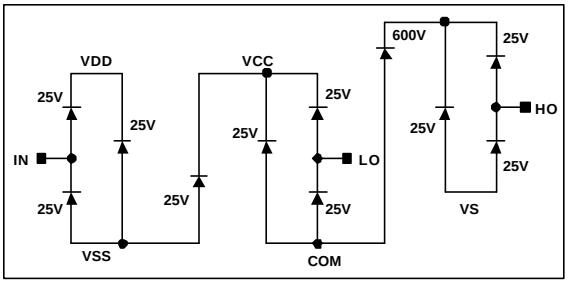


Figure 10. IR2110 Parasitic Diode Structure

International IOR Rectifier DESIGN TIP DT 94-17

INTERNATIONAL RECTIFIER CORP. APPLICATIONS ENG. 233 KANSAS ST., EL SEGUNDO, CA. 90245 TEL (310)322-3331 FAX (310)322-3332

THERMAL RESISTANCE CHARACTERIZATION FOR NEW SURFACE MOUNT DEVICES

by Tyler Fure

Many new surface mounted power devices have no connection for a heat sink, so they rely on the drain's exposed metal leads and thermal connection to the traces to dissipate heat. Since the characterization for heat sink mountable devices assumes an infinite sink, a new method of thermal characterization is necessary that will accurately reflect the operation of these new devices. This Design Tip describes how International Rectifier characterizes thermal resistance for HEXFET® power MOSFETs in the new SO-8, Micro8, and Micro3 packages. General information on thermal design is available in AN-949B.

1. Thermal Resistance Characterization

Total thermal resistance ($R_{\theta JA}$) for semiconductor devices consists of the sum of all thermal resistances between the junction and the ambient environment. Thermal resistance ratings are continuous by definition and require the device to be in thermal equillibrium. Transient thermal impedence ($Z_{\theta JC}$), based on pulsed current, provides a method to calculate junction temperature rise due to current with any duty cycle (AN-949B). Measurement of junction to ambient thermal resistance requires a method to measure the ambient and junction temperatures (T_A and T_J respectively) as well as the power dissipation (P_D). The formula for junction to ambient thermal resistance follows:

$$R_{\theta JA} = \frac{(T_J - T_A)}{P_D}$$

Measurement of the junction temperature requires a temperature sensitive electrical parameter (TSEP). We use $R_{DS(ON)}$ as the TSEP because the test circuit is simple and requires no switching. This parameter changes approximately 1% / °C, providing adequate change for an accurate temperature measurement. The test circuit, shown in Figure 1, applies a constant voltage to the gate and allows an adjustable amount of current through the device, thereby heating the junction. Using $R_{DS(ON)}$ as the TSEP provides for a true steady-state measurement because it is monitored continuously.

In order to measure $R_{\theta JA}$ for these new devices, the following four main steps are performed: 1) Calibrate $R_{DS(ON)}$ at maximum junction temperature, 2) Mount the device on a PC board, 3) Apply power and stabilize the junction temperature at its calibrated value, 4) Measure P_D and T_A to calculate $R_{\theta JA}$.

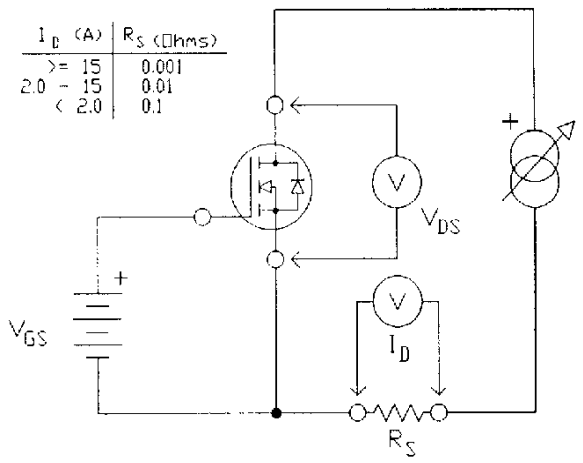


Figure 1
Test circuit for thermal characterization.

The first step is to calibrate $R_{DS(ON)}$ at the maximum rated junction temperature (T_{JMAX}) for each device. A thermostatic bath heats the devices to T_{JMAX} and ensures that the junction temperature is constant during calibration. When the devices are in thermal equillibrium, $R_{DS(ON)}$ is measured at five pulsed current levels, as shown in Figure 2. Known values of $R_{DS(ON)}$ are necessary for a range of current levels because it is not known beforehand the level of current that will heat the junction to T_{JMAX}.

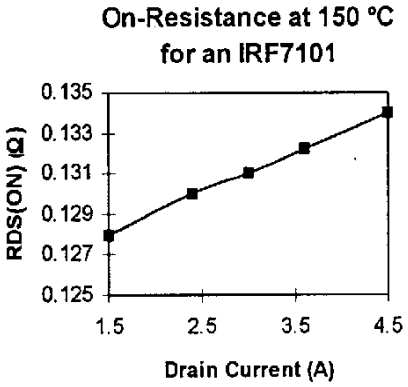


Figure 2
Calibration curve provides on-resistance values for 150 °C junction temperature.

The second step is to mount the individually calibrated devices for testing. SO-8 devices are mounted on a one inch square copper plated PCB (FR-4, 2 oz. copper), as shown in Figure 3.

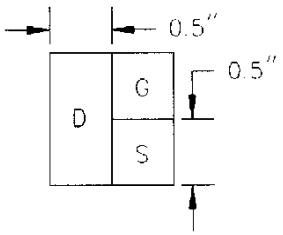


Figure 3
Test board for SO-8 thermal characterization (2 oz. copper on FR-4).

This is the industry standard test board. As packages continue to shrink though, the $R_{\theta JA}$ values produced with a board of this size become unrealistic. International Rectifier is now improving the standard by using test boards that more closely simulate real applications. The new Micro8 and Micro3 devices are tested on a PCB (GIN, 1 oz. copper) using the recommended footprint, shown in Figure 4. Therefore, designers can be confident that calculations based on the published values will accurately reflect the circuit in operation.

The third step is to apply power and heat the junction to T_{JMAX}. The drain current is slowly increased with the standard gate voltage applied (i.e. the V_{GS} at which I_D is rated). Power dissipation and $R_{DS(ON)}$ is calculated from drain voltage and current. The drain current continues to increase until $R_{DS(ON)}$ reaches a calibrated value, and the device is in thermal equilibrium (i.e. the junction remains at 150 °C for several minutes). At this point, a continuous power dissipation maintains the junction temperature at 150 °C as measured by the curve in Figure 2.

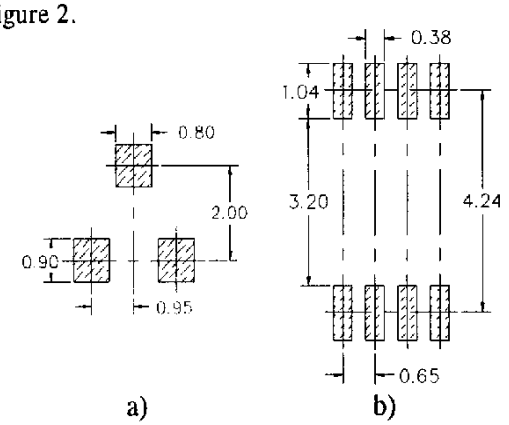


Figure 4
The recommended footprint for a) Micro3 and b) Micro8 closely approximates true applications (in mm).

The fourth step is to calculate $R_{\theta JA}$. Once the device reaches thermal equilibrium, the ambient temperature and power dissipation is measured. The junction is at its calibrated 150 °C value, so thermal resistance can be computed from the above equation.

2. Conclusion

Thermal resistance characterization must be done under steady-state conditions. It is a continuous, stable measurement with the devices in thermal equilibrium. Pulsed current characterization provides useful information as the transient thermal impedence, but should not be confused with $R_{\theta JA}$. The actual thermal resistance of a surface mounted device in a customer application depends heavily on the size of the drain pad. The values published by International Rectifier will accurately reflect actual operation because the recommended footprint is used for characterization.

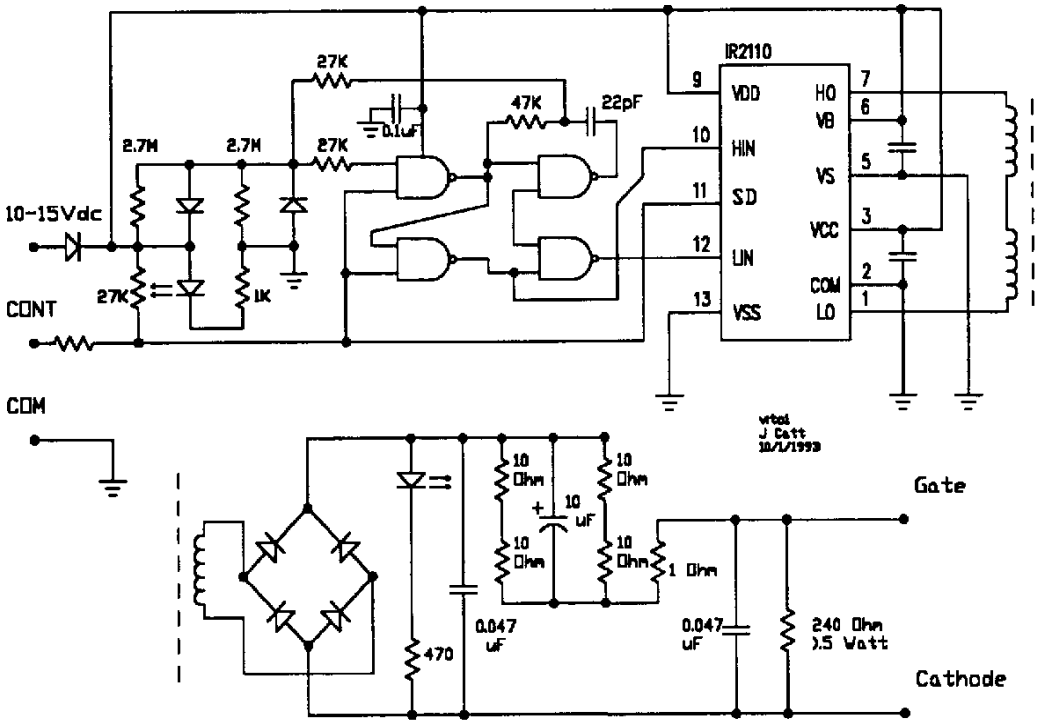
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Isolated SCR Gate Drive Circuit

by Vito Rinaldi



Features:

Simple Components, Galvanic Isolation, Strong Drive Signal.

Benefits:

Inexpensive, Compact Layout, Status Indication.

Further Details: International Rectifier Applications Engineering (El Segundo, California, USA).

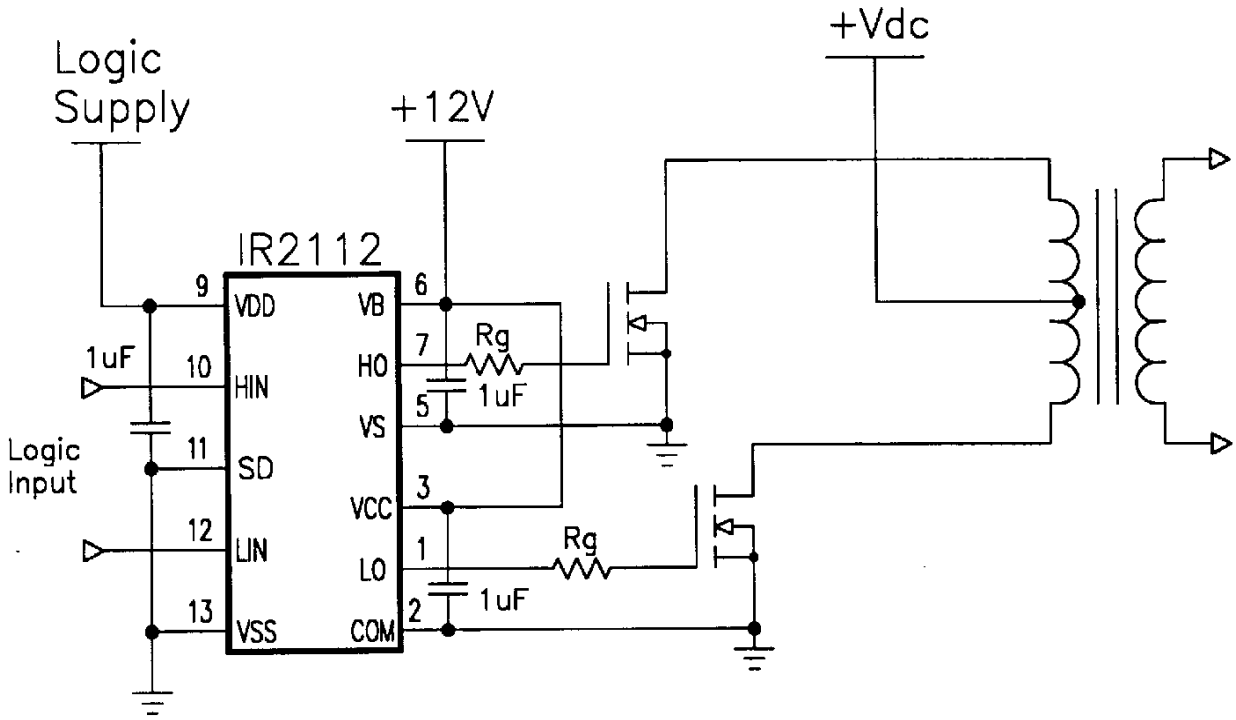
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Push Pull Drive Circuit

by Jamie Catt



Features:

Single Chip Solution, Interface to Any Logic, Low Cost.

Benefits:

Simplifies Circuit Layout.

Further Details: International Rectifier Applications Engineering Group (El Segundo, California, USA).

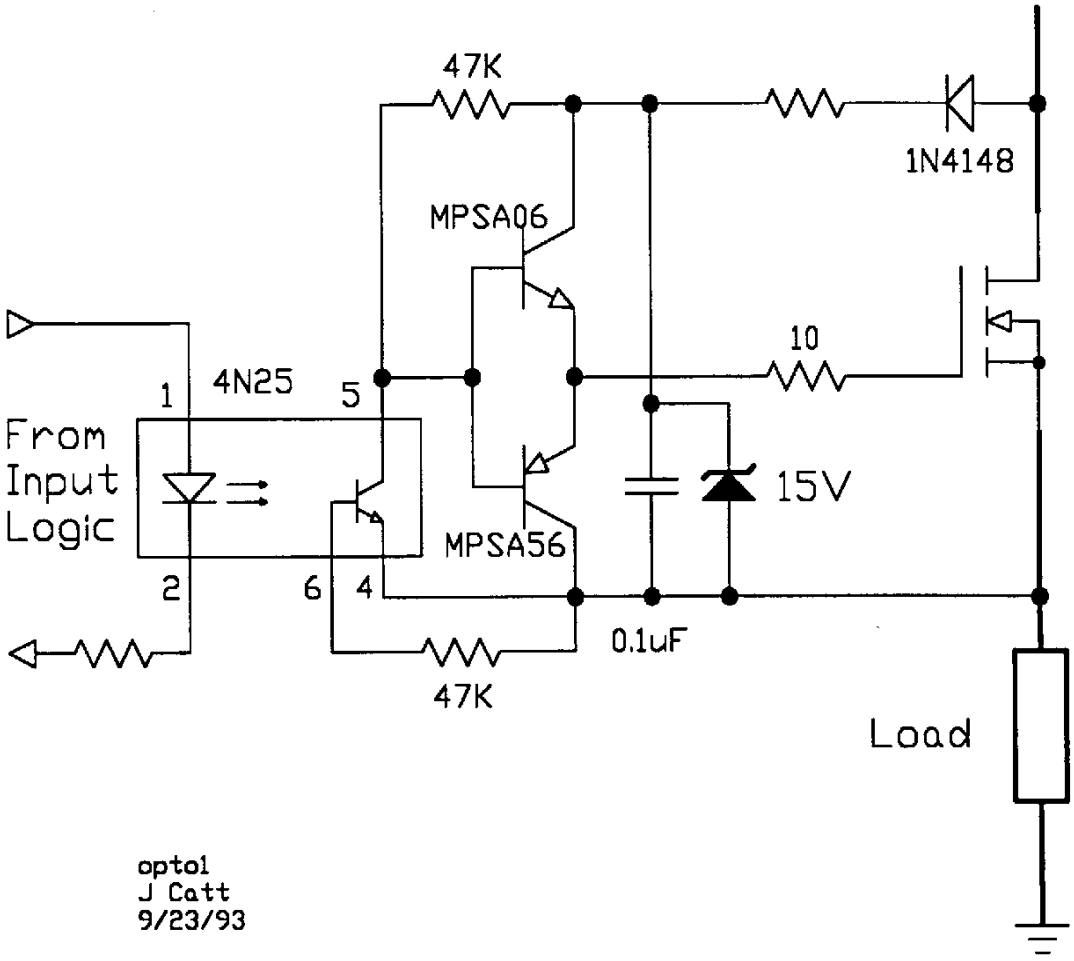
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Optically Isolated Gate Drive Circuit

by Jamie Catt



Features:

High Side Drive, Supply Derived from Drain of MOSFET, Galvanic Isolation, Low Cost.

Benefits:

Drives N-Channel FET on High Side of Load, No Floating Power Supply Required.

Further Details: International Rectifier Application Note AN-937A:
"Gate Drive Characteristics and Requirements for HEXFET® Power MOSFETs".

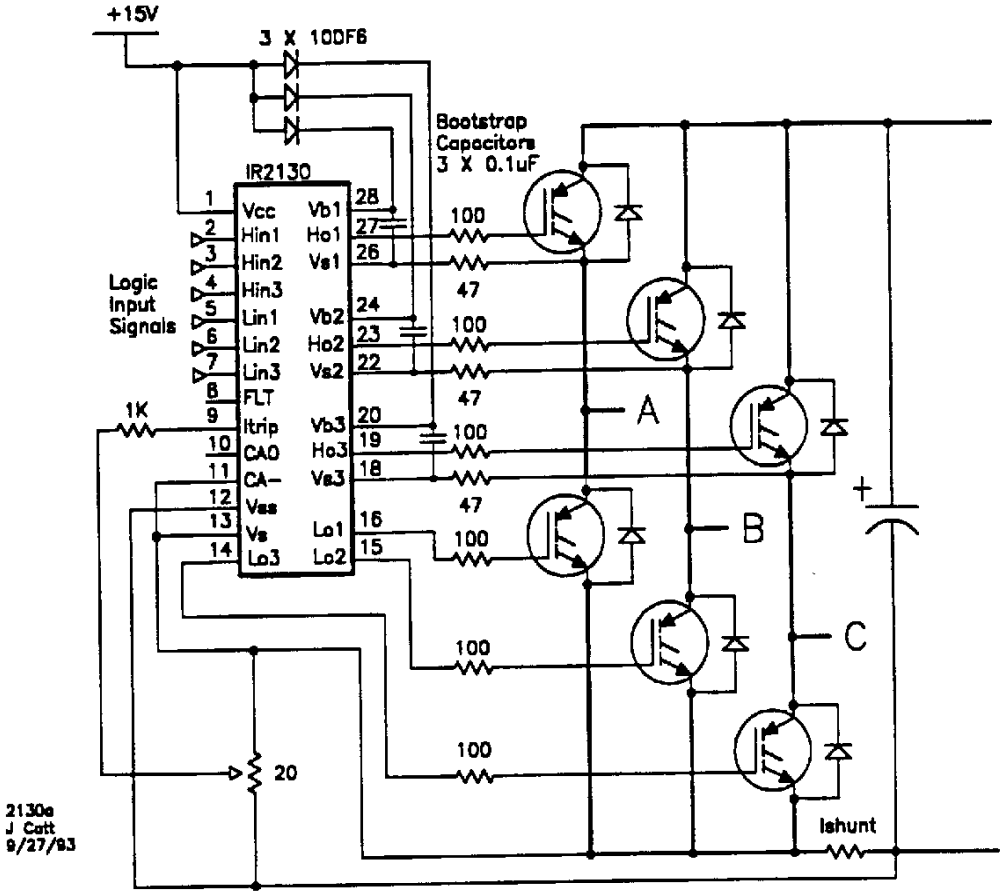
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3-Phase Bridge Drive With Overcurrent Protection

by Jamie Catt



Features:

Single Chip Solution, Interfaces Directly to All Input Signal Levels, Built in Deadtime, Overcurrent Protection, 600 Volt Rating.

Benefits:

Simple Circuit Layout, Low Cost, Eliminates Cross-Conduction.

Further Details: International Rectifier Application Note AN-985: "The IR2130: A Six Output, High Voltage MOS Gate Driver".

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TRADE-OFF CONSIDERATIONS BETWEEN EFFICIENCY AND SHORT CIRCUIT CAPABILITY IN IGBTS

By Rahul Chokhawala

The switching devices are selected by system designers to reliably handle circuit currents under normal as well as estimated overload conditions. Under fault conditions however, a device is subjected to very high surge currents - with magnitude limited mainly by its own gain. Only timely control and removal of the fault current by some external means would save the switching device from failure. In applications where system fault is a possibility, external protection circuits are used to sense the fault and turn-off the transistors by shutting down the base/gate drive in a time duration shorter than the short circuit withstand time - a measure of how long a device would survive under specified fault conditions.

There is a fundamental device trade-off between short circuit withstand time. t_{sc}, and transistor current-gain. The higher the gain of the transistor, higher will be the fault current magnitude and the shorter will be the t_{sc}[1]. The on-state voltage drop directly depends on the current-gain. High gain IGBTs have lower $V_{CE(sat)}$ but shorter tsc. The lower gain IGBTs on the other hand boast of longer t_{sc} but only at the expense of the operating frequency. The generalized plot in Figure 1 clearly illustrates this trade-off.

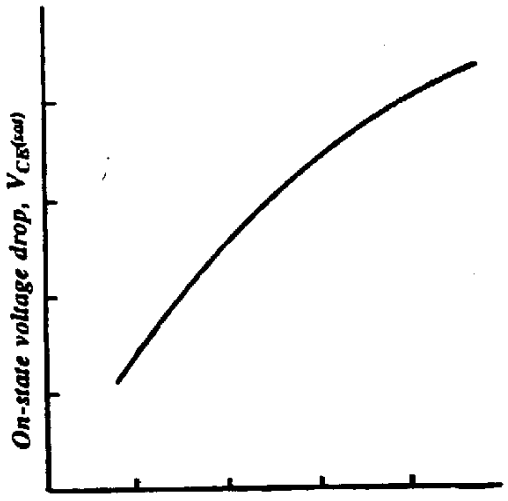


Figure 1 - Short Circuit time, t_{sc}

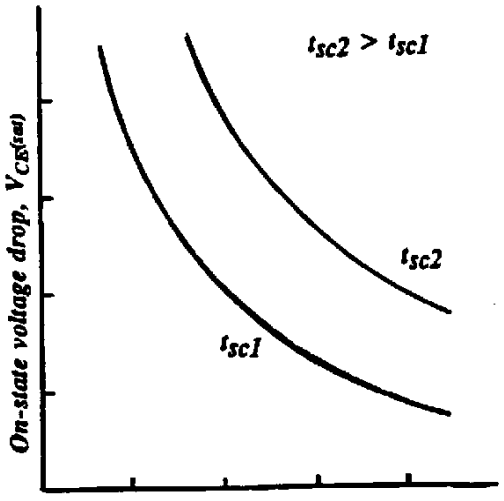


Figure 2 - Turn-Off Losses, E_{off} *(a measure of stored charge)*

[1] "A Discussion on IGBT Short Circuit Behavior and Fault Protection Schemes."

There also exists a device trade-off between the current-gain and the minority carrier life-time. The latter influences the amount of trapped charge in the IGBT; the shorter the carrier life-time the faster the free-charge recombination process. The consequence is shorter turn-off current tail and therefore lower turn-off losses, E_{off}. The curves in Figure 2 show generalized relationship between $V_{CE(sat)}$ and E_{off} for two different values of tsc. As seen from this figure, the trade-off between $V_{CE(sat)}$ and E_{off} is improved as the short circuit withstand time requirement is relaxed.

The above trade-offs result in IGBTs with more relaxed t_{sc} constraint be able to handle higher load currents. Figure 3 shows generalized trends in allowable load current against switching frequency for IGBTs with "low" and "high" short circuit times. The shape of the curves strictly depend on the $V_{CE(sat)}$ versus E_{off} trade-off.

In applications like uninterruptible power supplies, where the fault current is limited by the circuit components, the principal criteria for selection is the efficiency of the switching device. For such applications, devices not rated for long short circuit time but designed to be more efficient should be selected.

It should be noted that fast reacting protection circuits are now available[2] to protect most efficient IGBTs, despite their shorted short circuit endurance times. Usage of such circuits in association with high efficiency IGBTs would enhance circuit efficiency without sacrificing system reliability.

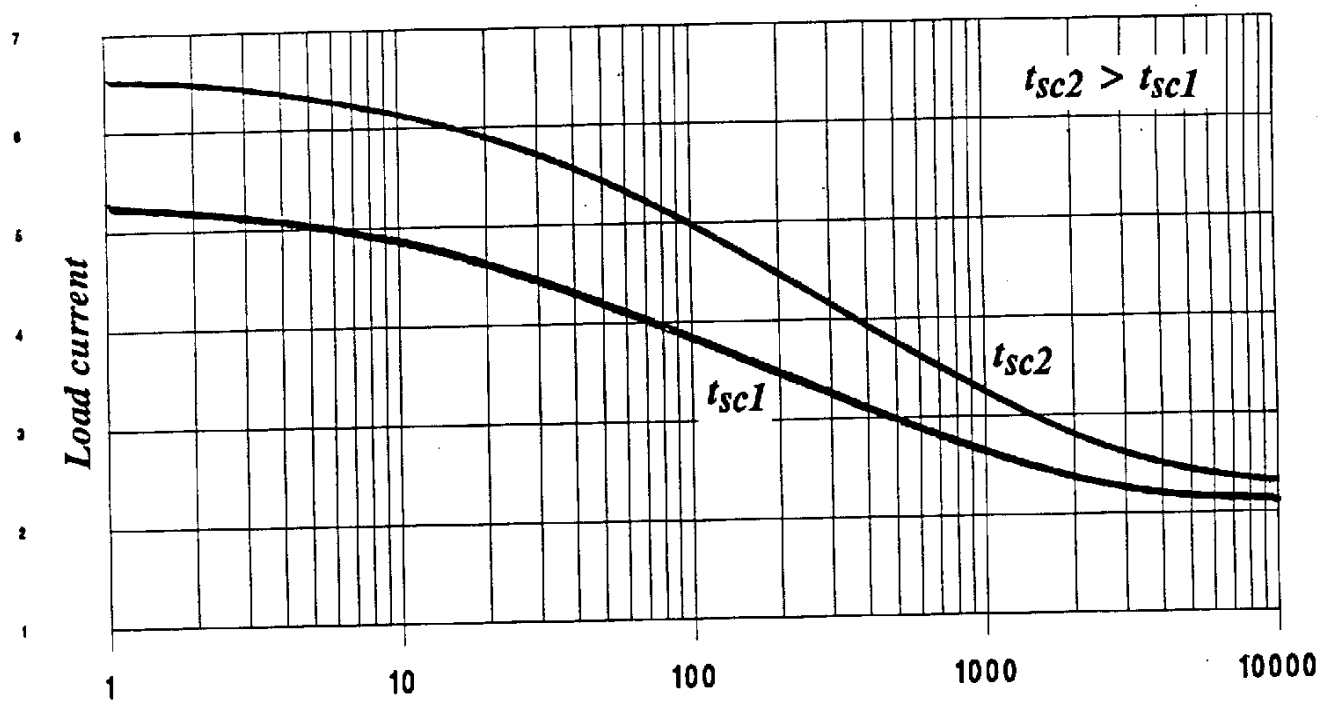


Figure 3 - Switching Frequency

[2] "IGBT Fault Current Limiting Current."

CHOOSING BETWEEN MULTIPLE DISCRETES AND HIGH CURRENT MODULES

By Brian R. Pelly

Introduction

Many circuits using HEXFETs or IGBTs operate at current in the range of tens to hundreds of amps. IR's packages that cover this range are shown in Figure. 1.

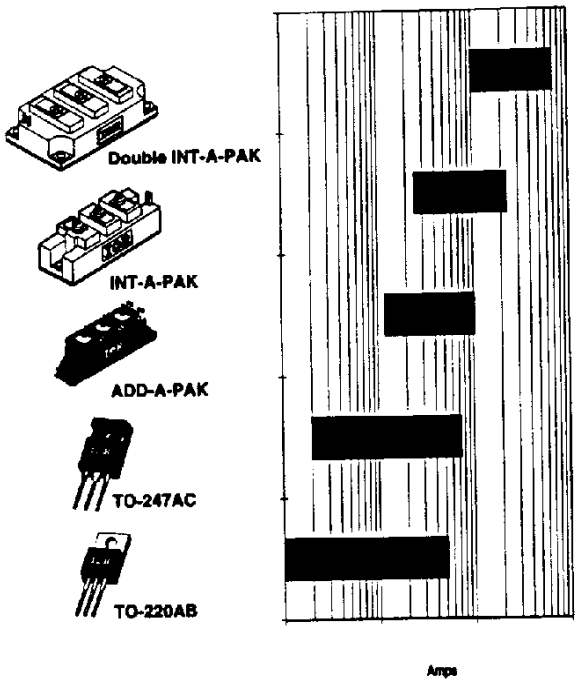


Figure 1. Current Ratings of Discrete TO-220AB, TO-247AC, and High Current Module Packages

The discrete TO-220 and TO-247 packages contain a single MOSFET, a single IGBT, or an IGBT with antiparallel HEXFRED fast recovery diode (Co-Pack). The TO-247 has a rated maximum current of 70A; full-load continuous operating design current of this package is typically in the range of 10 to 20A. Both the TO-220 and TO-247 discrete packages are manufactured in volume and offer low cost-per-ampere.

The isolated high current modules generally contain half-bridge, "chopper," or single switch configurations. Current ratings range from 25A, for a 1200V half-bridge Int-a-pak, to 600A, for a single-switch 600V Double Int-a-pak.

Attractive features of high current modules are that they are electrically isolated, easy to mount to heatsinks, and easy to interconnect with other modules to form the overall circuit. They also avoid the need for paralleling for currents up to several hundred amperes. Cost-per-ampere of high current modules is higher than for discretes, in terms of the basic semiconductor *component* cost — though not necessarily in terms of final *system* cost.

Figure 1 shows a range of overlap of current ratings covered by both discretes and high current modules. Within this range, the discrete often will offer the most cost-effective system design because of its lower cost-per-ampere.

TO-220 and TO-247 Co-Packs add to the attraction of the discrete packages for inverter circuits because they reduce the required number of components by 50%, compared to using discrete IGBTs with separate diodes.

The range of overlap where discretes can offer an alternative to high current modules can be extended by using multiple discretes in parallel.

Multiple discretes offer the potential for system cost savings versus high current modules because of the lower cost per ampere of the semiconductor *components*. Whether overall cost savings will be achieved will depend upon the design requirements for the specific application, and how these requirements will affect the total *system* cost.

This Design Tip presents a brief discussion and general guidelines that will assist the user in choosing between multiple discretes or high current modules for specific design situations.

Considerations for paralleling discretes are discussed sufficiently for a general qualitative understanding of the issues. The reader should refer to other, more specific, IR application literature for greater detail on paralleling.

Cost of Module as Function of Its Rated Current

As shown in Figure 1, a given module package covers a range of current ratings. A given module package, at its highest rating, contains the largest area of silicon die that it can accommodate; it is said to be "fully loaded." The same module with lower current ratings contains less than the full complement of silicon, and is "partially loaded."

Figure 2 illustrates that a fully loaded 200A, 600V Int-a-pak half-bridge has the same silicon die area as eight TO-247 Co-Packs. A partially loaded 50A, 600V Int-a-pak half-bridge, by contrast, contains the equivalent silicon of just two TO-247 packages.

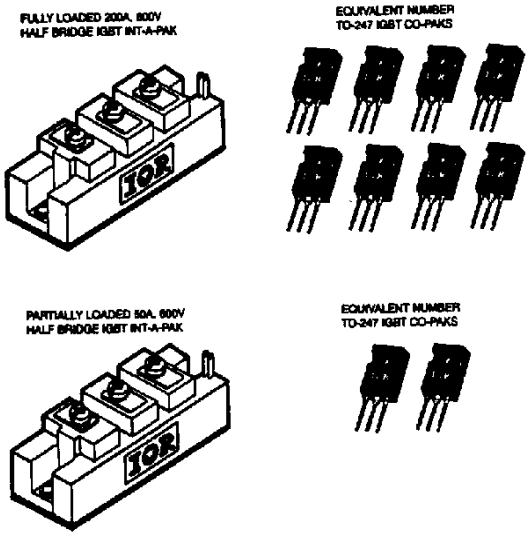


Figure 2. Equivalence Between IGBT INT-A-Paks of Different Current Ratings and TO-247 IGBT Co-Packs

Since module package cost is essentially fixed, independent of how much silicon goes inside it, a fully loaded module will inevitably have lower cost-per-amp than a partially loaded one.

Cost of Module versus Discretes

The simple construction of the discrete package, coupled to its high manufacturing volumes, ensures that the discrete's cost-per-ampere will always be less than that of a high current module. Cost-per-ampere of a fully loaded module may be 150% or more of the cost of the equivalent number of discrete *components*.

Against the *component* cost advantage of the discrete, the user must weigh additional assembly costs, derating needed for paralleling, and technical practicality of using multiple discretes. These factors depend upon the specific design requirements.

Electrical Connections

A basic difference between the discrete and the high current module is the method of making electrical connections to the package.

A discrete TO-220 or TO-247 is designed for soldering to a Printed Circuit Board (PCB). The maximum continuous operating current that can be handled by a PCB is typically less than 100A. This tends to set a natural limit on the number of discretes that can conveniently be connected in parallel.

High current modules, by contrast, have screw terminals; they are designed primarily for cable-lug or busbar connections, as illustrated in Figure 3(a). The high current module can also be connected directly via through-holes to a PCB, as illustrated in Figure 3(b). This type of connection is best suited to operating currents below 100A.

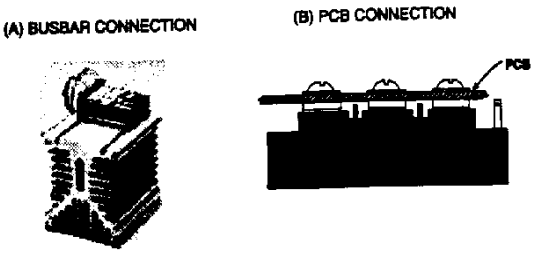


Figure 3. Methods of Making Connection to INT-A-Pak Module

Equalizing Junction Temperatures of Multiple Discretes

Paralleling of multiple discretes requires that power losses and — more importantly — junction temperatures of each device should be equalized as much as possible.

Some unbalance of losses is inevitable, because of differences in electrical characteristics between different devices. The variation of characteristics between individual devices will require a certain amount of current derating, typically around 20%. Even with this derating, good thermal coupling is necessary to force individual junction temperatures to "equalize."

The need for tight thermal coupling between the junctions of individual discretes weighs against an electrical isolation barrier, such as a "Silpad," being placed directly at the cooling surface of a TO-220 or TO-247. This places a thermal barrier between individual discretes and tends to decouple individual junction temperatures. For this reason, electrically isolated "Fullpak" TO-220 and TO-247 packages are not ideal for paralleling.

Parallel discretes should be mounted on a common heatsink. If electrical isolation is required, the discretes can be mounted on a common heatspreader to thermally couple the junctions. The heatspreader also serves the purpose of a mechanical carrier for the discretes during assembly. The isolation barrier is placed between the busbar and the main heatsink structure, as illustrated in Figure 4.

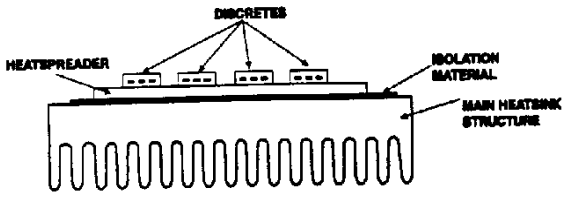


Figure 4. Use of Heatspreader to Provide Thermal Coupling Between Discretes

Unbalance due to Circuit Layout

External circuit unbalance due to non-symmetrical layout can cause significant differences in losses between parallel discretes. The most serious effects of non-symmetrical layout will be current unbalance during switching intervals and unbalanced switching losses. The most sensitive stray circuit elements to be balanced are the individual common emitter inductances. This is illustrated in Figure 5.

If switching losses are relatively small in relation to the conduction losses, a certain amount of circuit-induced unbalance of switching losses can be tolerated, and symmetrical layout will not be super-critical. This will depend on the design requirements of the application.

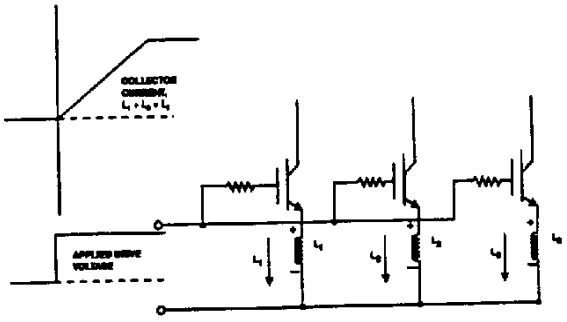


Figure 5. Common emitter circuit inductances L1, L2, L3 develop Ldi/dt voltages during switching, modifying the gate-emitter voltage applied to the IGBTs. Unbalanced inductances cause unbalanced drive voltages and unbalanced currents.

Switching losses will be low where switching frequency and/or switching voltage is relatively low. The simple in-line arrangement of discretes, shown in Figure 6(a), though not electrically symmetrical, can be satisfactory in these circumstances.

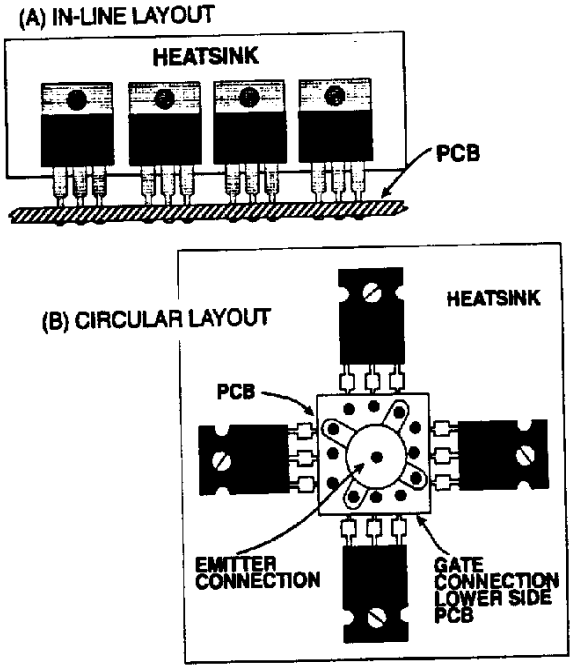


Figure 6. Different Layouts of Discretes

Where switching losses are significant, careful attention to layout is important. The symmetrical layout illustrated in Figure 6(b) is ideal, in terms of balancing individual common emitter inductances and equalizing switching losses.

Figures 7 and 8, for HEXFETs and IGBTs respectively, show typical boundaries of switching voltage and average device switching frequency that correspond to switching losses of 15% and 30% of the total device losses in hard switching applications[1]. Layout will generally not be super-critical where switching losses are less than 15%; it becomes increasingly more so as switching losses increase above this level.

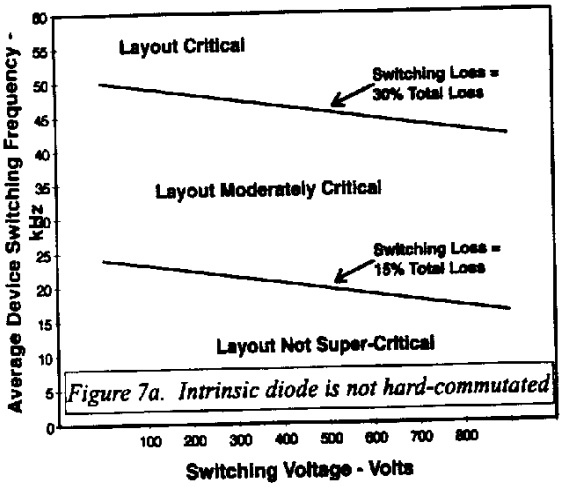


Figure 7a. Intrinsic diode is not hard-commutated

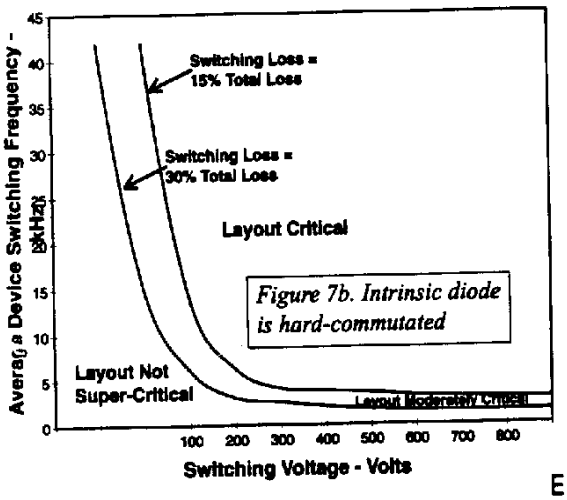


Figure 7b. Intrinsic diode is hard-commutated

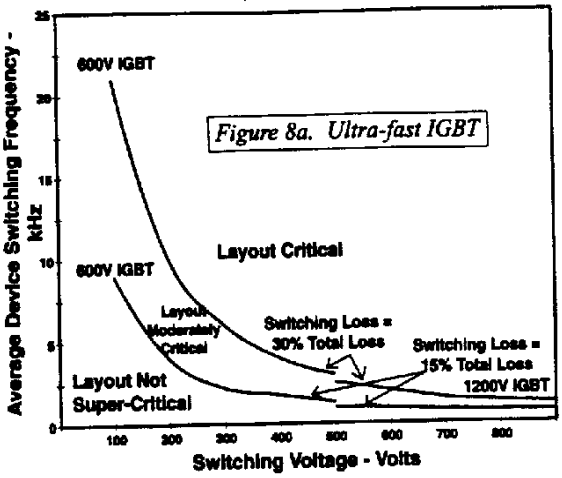


Figure 8a. Ultra-fast IGBT

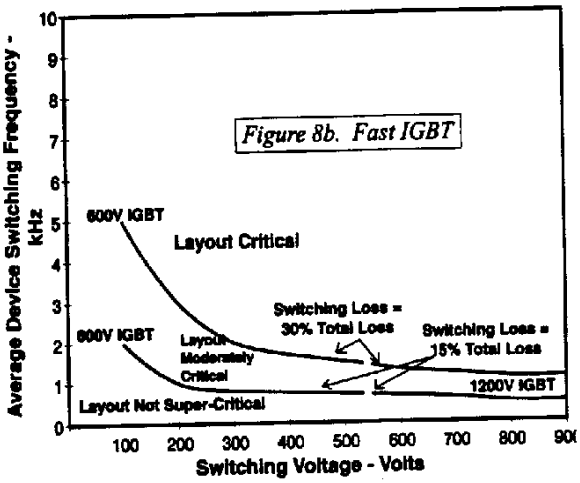


Figure 8b. Fast IGBT

Figure 7(b) shows that if the HEXFET's internal diode is hard commutated — as is the case in sinusoidal PWM inverters — the area of operation for non-critical layout is generally restricted to low voltage operation because the switching losses caused by recovery of the HEXFET's intrinsic diode increase significantly as voltage increases.

[1] Note that the average device switching frequency in a sinusoidally modulated PWM inverter is *half* the output PWM frequency. Thus for this type of circuit, average device switching frequency should be multiplied by 2 to obtain the output PWM frequency.

Figures 7 and 8 are intended only as a general indication of the operating areas that are "easy" or "less easy" for parallel discretes, based on layout considerations.
Tables 1 and 2 relate this basic information to typical circuits.

Table 1
Design Situations for Multiple Discretes For Which Layout is not Super-critical

Design Conditions	*Typical Circuits*
Operating frequency of HEXFET or IGBT is low	Line frequency inverter Line frequency ACswitch
Operating voltage of HEXFET or IGBT at switching instant is low	Inverters operating from battery voltage below 100 V Zero-voltage-switching resonant inverters
Operating current of HEXFET or IGBT at switching instant is low	Zero-current-switching resonant inverters
HEXFET internal diode is not hard-communtated	Forward, flyback, bridge inverters

Table 2
Design Situations for Multiple Discretes For Which Layout is Critical

Design Conditions	*Typical Circuits*
Operating frequency and voltage of HEXFET are high, internal diode is hard-commutated	PWM inverter
Operating frequency and voltage of IGBT are high	PWM Inverter Buck Converter Boost Converter

Heatsink Mounting Area

The symmetrical layout of discretes shown in Figure 6(b), (two similar sections for a half-bridge) with the same silicon area as a fully loaded Int-a-pak, would require three to four times more heatsink mounting area.

The simpler, non-symmetrical, in-line arrangement of TO-247 Co-paks shown in Figure 6(a), on the other hand, with the same silicon area as a fully loaded Int-a-pak, would require slightly less heatsink area. The savings in heatsink area become more significant when in-line Co-Packs are compared against a partially loaded Int-a-pak.

Summary

Table 3 shows a summary of the factors that will influence the choice between multiple discretes and high current modules, and typical applications that are potentially suited to each design approach.

Table 3
Summary

Factors that favor multiple discretes	*Factors that favor high current module*
A few discretes in parallel are needed	Beyond the capability of a few discretes in parallel
Current is below rating of fully loaded module	Fully loaded module is needed
High volume manufacturing geared to handling discretes	Low-to-medium volume manufacturing
Design time not critical	Important to minimize design time
Electrical isolation not required	Electrical isolation is required
Design will use printed circuit board	High-current cable-lug or busbar connections needed
HEXFET internal diode is not hard-communtated	Forward, flyback, bridge inverters
Typical Applications	
Line frequency inverters Low-voltage PWM inverters for UPS Line-frequency AC switches/breakers Electric vehicle controllers Resonant power supplies Resonant HF welders HEXFET switching power supplies	PWM AC motor drives Line voltage PWM inverters for UPS High current power factor correction

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DESIGN TIP

DT 93-6

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Miniaturization of the Power Electronics for Motor Drives

Gerry Limjuco and Dana Wilhelm

Introduction:

The power electronics for a fractional HP AC or BL-DC motor drive can be built in a volume not much larger than a pack of cigarettes. MOS Gate Drivers and co-packaged IGBTs in surface mounted TO-220 (IRGBC30KD2-S)are the key to achieve this level of power density (see Figure 1).

Figure 2 shows the schematic of the power stage. The input is the logic signal from the modulator (standard TTL/CMOS) and the outputs are the three phases to the motor.

If isolation is required between the modulator and the power stage, it can be provided with inexpensive (low dv/dt) opto-isolators at the input of the IR2130 (see Figure 3).

In addition to the logic inputs, the power stage requires a single 12-15V, 20mA supply. It can operate to bus voltages up to 600V.

The power stage is split into two boards, one with the power devices (see Figures 4 & 4A), the other with the gate driver and overcurrent protection and shutdown. Figures 5 and 5A show the control board layout using IR2130S (SOIC), whereas Figures 6 and 6A show the control board layout using IR2130J (PLCC). Either of these control boards can be interconnected with the power board using standard 0.100" center headers into mating receptacles.

Figure 7 shows how much current can be delivered to an AC motor operated with pulse-width modulation. Larger currents can be obtained from a board with better thermal characteristics than a standard FR4, 4 oz. copper. The thermal resistance between junction and air for this specific designs was measured at 40°C/W per device. The attached sheet shows a breakdown of the different components of losses.

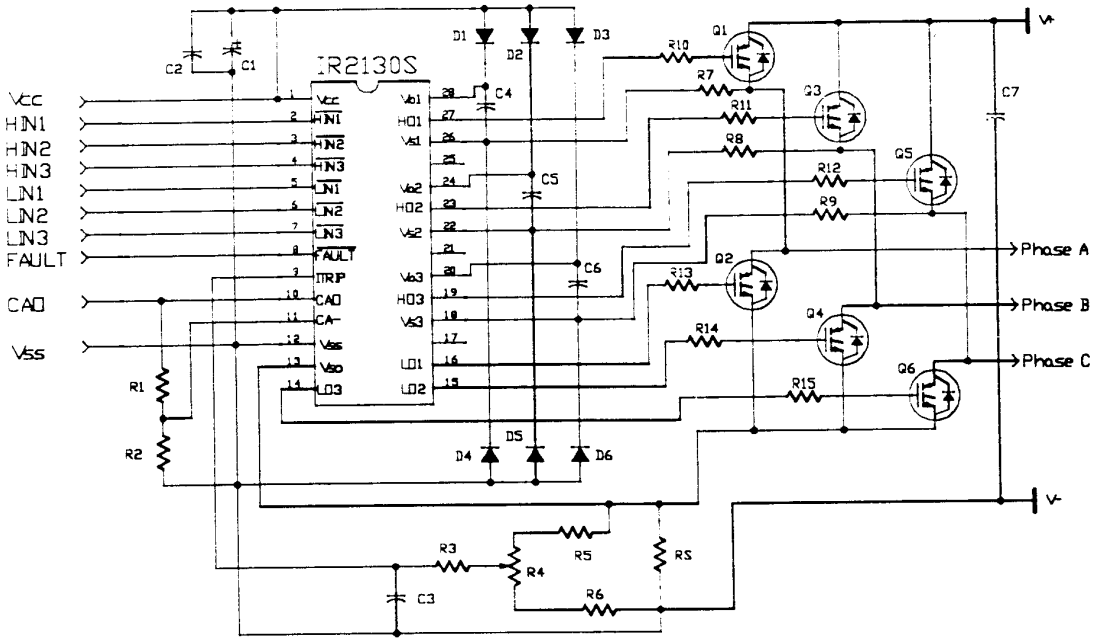


Figure 2. **3-Phase SMD Power Stage (Schematic Diagram - IR2130S)**

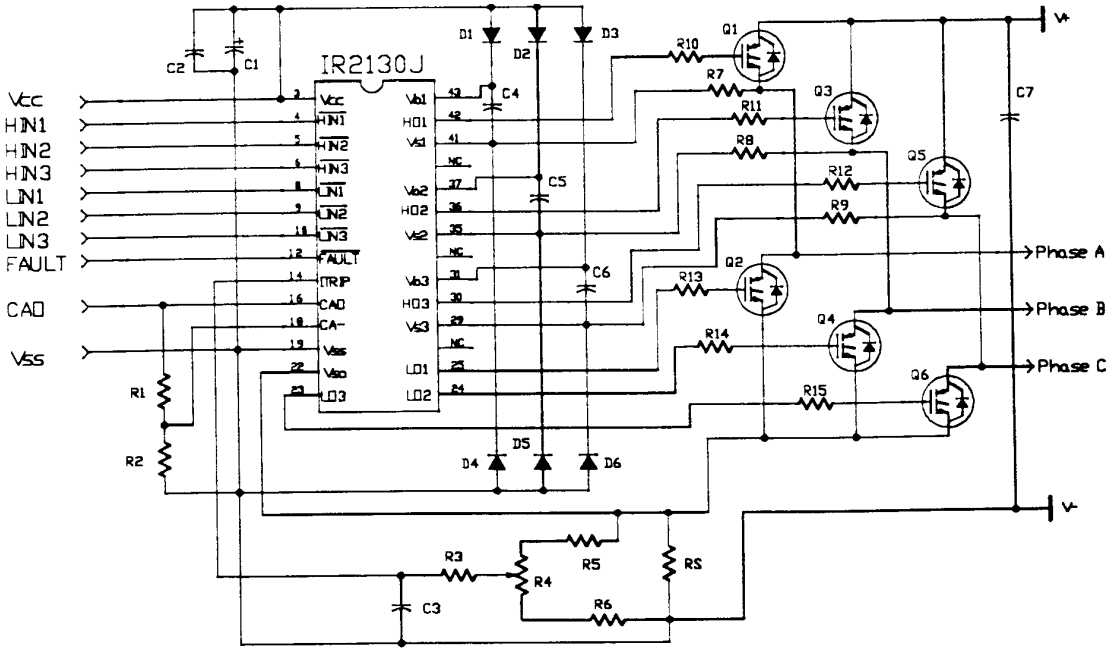


Figure 2A. **3-Phase SMD Power Stage (Schematic Diagram - IR2130J)**

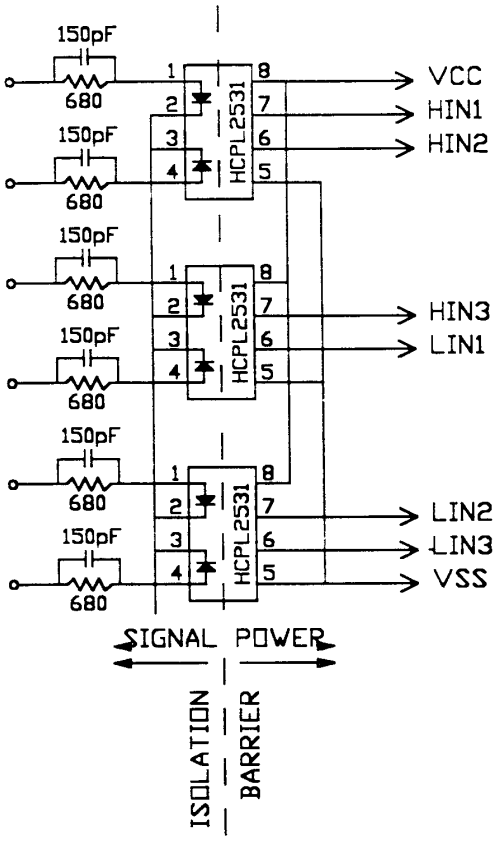


Figure 3. **Input Isolation Stage**

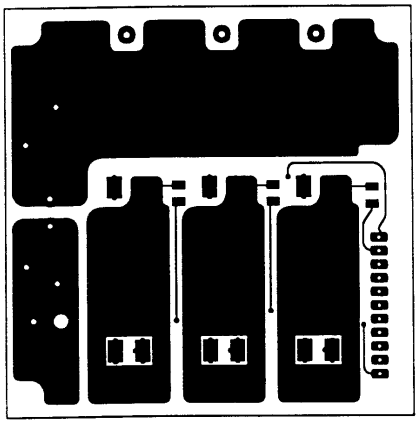


Figure 4. **Power Circuit** (top view)

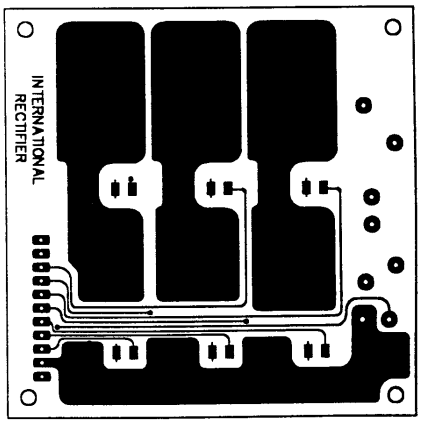


Figure 4A. **Power Circuit** (bottom view)

IR2130S Control Circuit

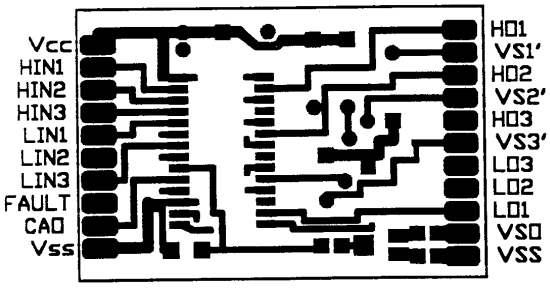


Figure 5. **IR2130S Control Circuit** (top view)

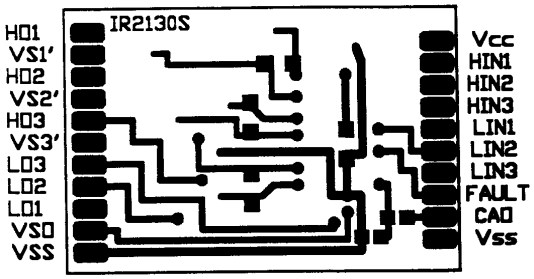


Figure 5A. **IR2130S Control Circuit** (bottom view)

IR2130J Control Circuit

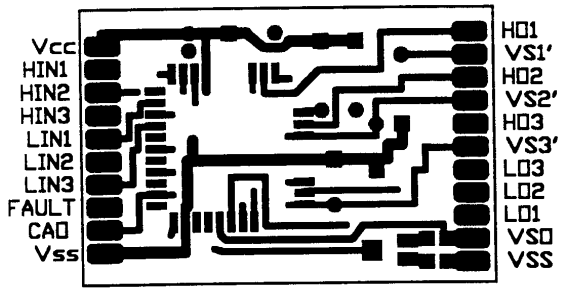


Figure 6. **IR2130J Control Circuit** (top view)

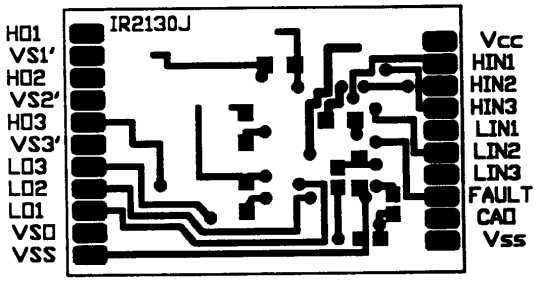


Figure 6A. **IR2130J Control Circuit** (bottom view)

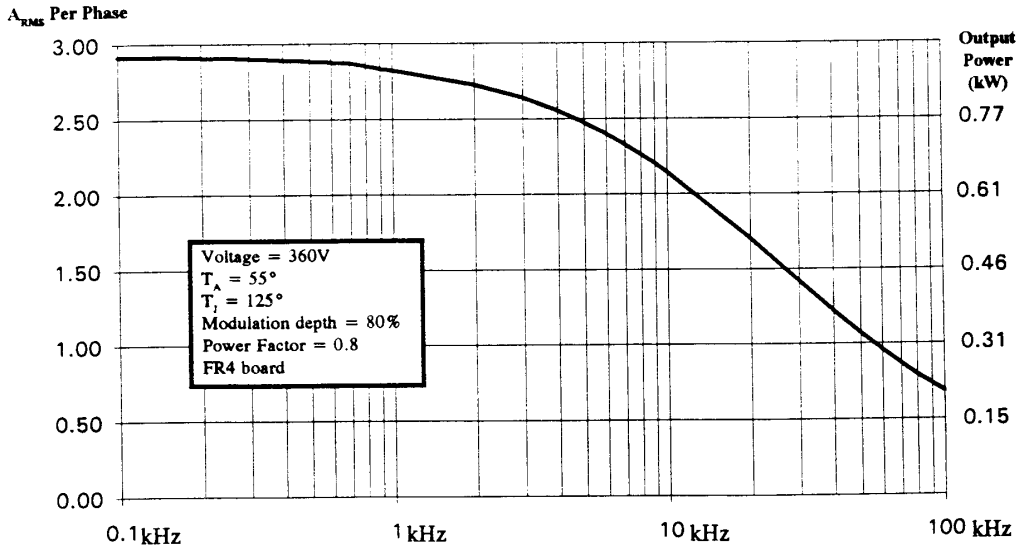
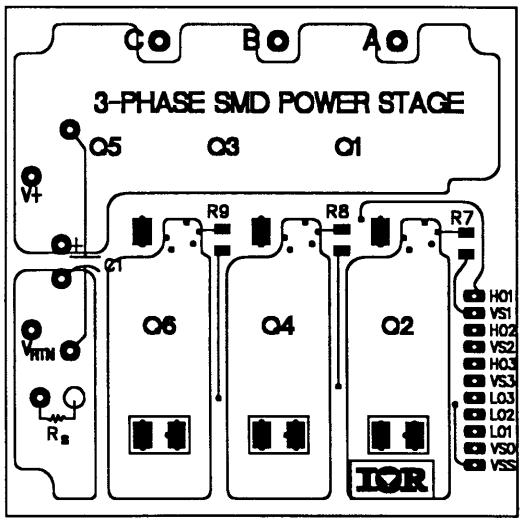


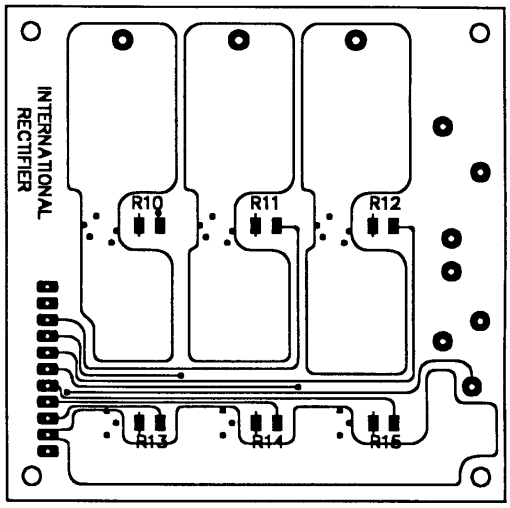
Figure 7. **Typical Output vs Frequency of a 3-Phase Bridge with IRGBC30UD2S**

Components Placement Diagrams

Power Circuit



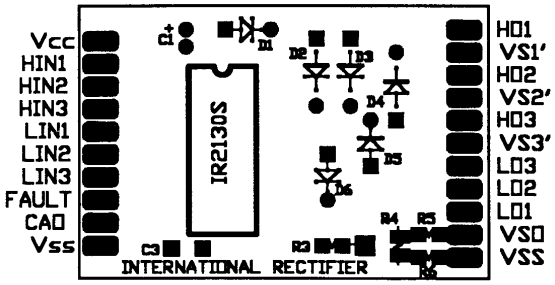
Top View



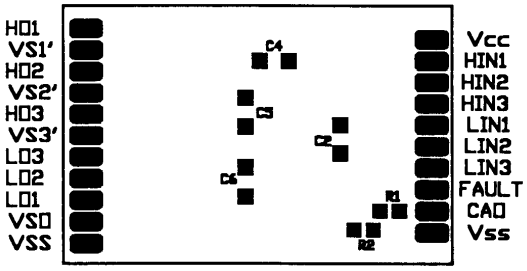
Bottom View

Control Circuit

IR2130S (SOIC)

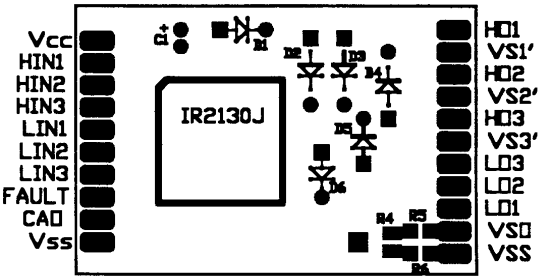


Top View

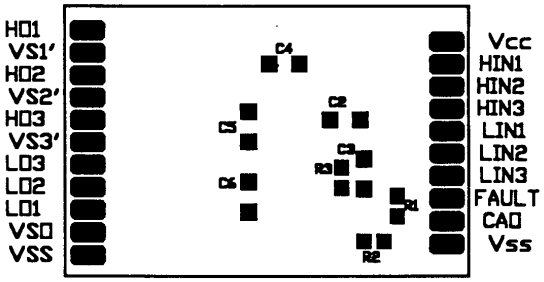


Bottom View

IR2130J (PLCC)



Top View



Bottom View

3-Phase SMD Power Stage Components List

IC	IR2130S or IR2130J MOS Gate Driver
Q1 - Q6	See Table I
R1	9.1k0, thick film resistor, type 0805
R2, R3	l.OkW, thickfilm resistor, type 0805
R4	50Ω, Bourns trimmer type 3314G
RS, R6	IOW, thick film resistor, type 0805
R10, R11, R12, R13, R14, R15	100Ω, thickfilm resistor, type 1206
R7, R8, R9	47Ω, thick film resistor, type 1206
RS	.100Ω, 16Ω, (Caddock typeMP816)
Do -D6	10DF6 Ultra-fast recovery diode
C2	l 0 µF, 25V tantalum capacitor
C3	I nF, 50V Ceramic capacitor, type 1206
C1, C4, CS, C6	0. l µF, 50V Ceramic capacitor, type 1206
C7	I 0 µF, 450V Aluminum electrolytic capacitor
C8	(external - use appropriate value for intended application)
Header & Receptacle	0.100" center, square pins

Frequency	Short Circuit Rating Required
1 to 6 kHz	IRGBC30MD2-S or IRGBC20MD2-S
6 to 25kHz	IRGBC30KD2-S or IRGBC20KD2-S

For more information, please refer to:

AN-983A IGBT Characterstics and Applications.
AN-98S The IR2130: A Six-Output, High Voltage MOS Gate Driver.
AN-978A High Speed, High Voltage IC Drive for HEXFET or IGBT Bridge Circuits.
AN-990 Application Characterization of IGBTs.

"An Algorithm for the Selection of the Optimum Power Device" (Section 3) Clemente and Pelly.
"Accurate Junction Temperature Calculations" by Clemente and Dapkus.

APPLICATION PARAMETERS

Switching voltage	V	360
Displacement angle	rad	0.64
Modulation depth		0.8

Power factor 0.8

THERMAL OPERATING CONDITIONS

Ambient temperature	oC	55
Thermal resistance j-c	K/W	40.00

IGBT MODEL AND PARAMETERS: IRGBC30KD2 (typ)

Temperature of ref. parameters	oC	125.00
Vt	V	0.636
a	Ohm	0.390
b		0.674
Gamma function, (b+2)/2	1.337	0.892
Gamma function, (b+3)/2	1.837	0.941
h	mJ/A	2.15E-2
k		1.352
Gamma function, (k+1)/2	1.176	0.924
Gamma function, (k+2)/2	1.676	0.904
m	mJ/A	5.27E-2
n		1.102
Gamma function, (n+1)/2	1.051	0.973
Gamma function, (n+2)/2	1.551	0.889
Reference voltage	V	480

DIODE MODEL	HFRD-2, 600 V			Tj =	125 oC		Gamma
Conduction model:	Vt =	0.60	a =	0.120	b =	1.000	0.88623
Switching model:	Pk Irr/If=	1.30	ta (us)=	0.025	tb (us)=	0.015	1

ELECTRICAL OPERATING CONDITIONS

Operating frequency	kHz	0.10	0.20	0.50	1.00	2.00	5.00	10.00	20.00	50.00
Peak current	A	4.03	4.02	3.97	3.90	3.77	3.41	2.94	2.04	1.06
RMS fund. voltage, line to neutral	V	129.60	129.60	129.60	129.60	129.60	129.60	129.60	129.60	129.60
RMS Current, fundamental	A	2.85	2.84	2.81	2.76	2.66	2.41	2.08	1.45	0.75
Output power, fundamental	kW	0.89	0.88	0.87	0.86	0.83	0.75	0.65	0.45	0.23
Voltage drop at peak current	V	1.63	1.63	1.62	1.61	1.59	1.53	1.44	1.27	1.04
Conduction losses	W	1.44	1.43	1.41	1.37	1.31	1.14	0.93	0.58	0.25
Turn-on losses, ideal diode	W	0.00	0.01	0.02	0.03	0.06	0.12	0.20	0.24	0.25
Correction factor for gate drive	23 Ohms	1.00	1.00	1.00	1.00	1.00	1.00	1.00	2.00	3.00
Corrected turn-on losses	W	0.00	0.01	0.02	0.03	0.06	0.12	0.20	0.49	0.76
Turn-off losses	W	0.01	0.01	0.03	0.05	0.11	0.24	0.40	0.54	0.65
Total IGBT losses	W	1.45	1.45	1.45	1.46	1.47	1.50	1.53	1.60	1.66
Diode conduction losses	W	0.30	0.30	0.30	0.29	0.28	0.24	0.20	0.13	0.06
Diode, switching losses	W	0.00	0.00	0.00	0.00	0.00	0.01	0.02	0.02	0.03
Total diode losses	W	0.30	0.30	0.30	0.29	0.28	0.25	0.22	0.15	0.09
Total losses in co-pak	W	1.75	1.75	1.75	1.75	1.75	1.75	1.75	1.75	1.75
Junction temperature	oC	125.00	125.00	125.00	125.00	125.00	125.00	125.00	125.00	125.00
Semiconductor Efficiency	%	98.82	98.81	98.80	98.78	98.73	98.60	98.38	97.67	95.51

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CURRENT CAPABILITY OF TO-220 PACKAGE

by Steve Clemente and Shahin Maloyans

1. Background

From the early days, the two reference points for power transistor ratings have been:

- 25°C case temperature
- continuous current waveform.

This was a break from established tradition since, at the time power transistors were first introduced, diodes and thyristors were rated at higher temperatures and complex waveforms, more representative of actual operating conditions.

Today the 25°C rating of power transistors is well established, in spite of the problems and confusion it causes to design engineers and to the semiconductor manufacturers.

The source of these problems is the fact that electronic equipment is invariably designed to operate at ambient temperatures that are higher than 25°C. As a result, the 25°C current rating specifies a capability that, on the one hand must be met by the manufacturer, on the other hand is much beyond what any designer can reasonably use.

Embedding a current rating in the part number gives additional emphasis to a rating that cannot be utilized in practical applications. For this reason some manufacturers are using a current rating in the part number for operation at a higher temperature than 25°C. However, the temperature associated to this rating is not indicated in the part number and this compounds the confusion even further.

In an effort to provide useful information to the designers, International Rectifier publishes ***two*** current ratings for its power MOSFETs (one at 25 and one at 100°C) and ***a curve*** of current rating at any temperature between 25 and 150 °C or 175°C. IR does not use a current rating in the part number.

2. The Current Rating of Low Voltage HEXFET Power MOSFETs

In an ideal world the limitations of the die and those of the package would converge to the same operating point. This means that, as the current increases to the device limits, the die temperature and the package temperature would be at their respective limits, less safety margins.

In the real world, for the large majority of devices, die limitations occur well before package limitations, with the exception of the new, very low on-resistance MOSFETs. Their voltage drops are so low that their current handling capabilities exceed that of most

popular packages. This has stimulated new package designs, as well as improvements in the leadframe material and in the epoxy compounds.

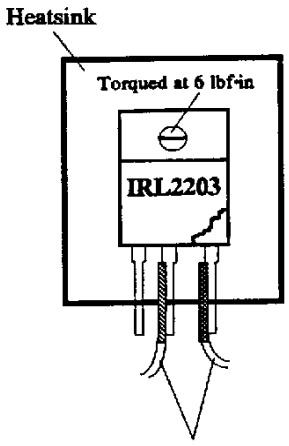


Figure 1 - The Set-Up Used for High Current Tests

3. *Package Limitations*

The limits to the current handling capability of a TO-220 package are much more difficult to establish than those of the die. The following experiment provides a better understanding of these limitations.

We have prepared IRL2203 (10mΩ, 30V) by partially removing the epoxy to expose the area where the wires are ultrasonically bonded to the source pin. This device has two 0.38 mm (15mils) source bonding wires. We have mounted this device on a large heatsink with thermal grease, torqueing the 6-32 screw to 0.6 N•m (6 lbf•in), as shown in Figure 1. Two 4.1 mm (6-gauge) cables were soldered to the leads 4 mm (0.15") from the package. The size of these wires is such that they do not contribute any power dissipation and the distance from the package is typical of TO-220 mounting techniques.

With a current of 75 A in the device, after reaching thermal equilibrium, the following temperatures were measured with a thermal imager:

- bonding wires: 220°C
- source pin: 180°C
- heatsink: 35°C

Knowing the resistance of the bonding wires (0.3mΩ) and the power dissipation (1.73W), the thermal resistance can be calculated to be 113°C/W. With this information and given that the glass transition point of this epoxy is over 190°C, the graph of Figure 2 can be generated.

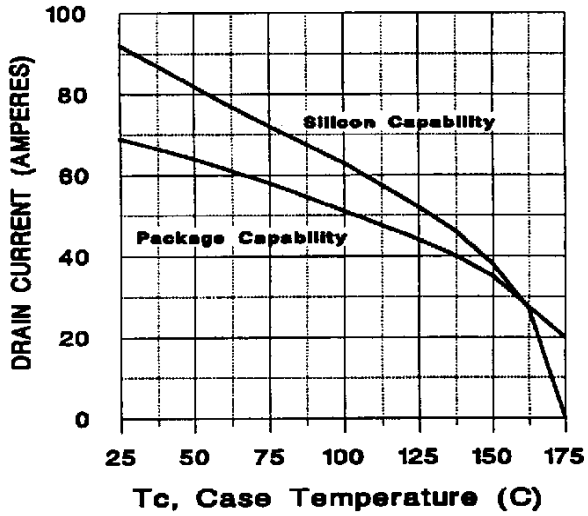


Figure 2 - Current Handling Capability of the TO-220 with a low voltage HEXFET (IRL2203)

Under these conditions the on-resistance of the IRL2203 is 17mΩ, the voltage drop is 1.28V and power dissipation is less than 100W. Hence, in the test described above, the temperature of the die itself is approximately 150°C.

This confirms what is shown in Figure 2, i.e. that over most of the temperature range the package limits the current capability of the device to a lower value what the die itself can handle. While it may appear that we are unduly limiting the device with the bond wires, this is not true for typical applications. The next section discusses this in more detail.

4. *Current Capability in a Typical Application*

The vast majority of low voltage MOSFETs are designed-in for their low on-resistance and low voltage drop, not for their current carrying capability. In spite of this, current rating is still used by many designers to compare devices from different manufacturers, hence the incentive to put as high a number as possible.

In order to achieve the rated current, cooling techniques are required that are not practical in reality. Thus, the wirebonds do not limit the maximum current capability, but rather the thermal design is the limiting factor.

Until all manufacturers agree to use a common rating technique, this confused state of affairs will continue. Meanwhile, the following paragraphs should provide helpful design guidelines.

1. ***International Rectifier has chosen to use the silicon capability as the limiting factor in establishing the current rating of its low voltage HEXFETs, while providing designers with information on package limitations.***

2. ***If the device must handle a significant amount of current for one second or more, its RMS value must be within the capability of the silicon and of the package, whichever is lower.***

   The package limitation is shown in Figure 2, the current limitation is normally shown in Figure 9 of the data sheet. The package limitation will be incorporated in the future revisions of the data sheet.

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TESTING HIGH-POWER SCRs AND DIODES

by Donald A. Dapkus II
Application Engineer

This Design Tip is intended to help field service and repair personnel test high power SCRs and diodes using simple, portable test set-ups. International Rectifier's SCRs and diodes are rated for very high power levels. Testing the characteristics of these devices presents some problems unless the proper equipment is available.

Test Equipment

One of the best methods of testing these devices is to use a curve tracer to simultaneously display the current and voltage. Using a curve tracer, it is possible to determine if a power device is damaged or not by measuring breakdown voltages, leakage currents, forward voltages, etc. However, curve tracers such as the Tektronix 576 are expensive pieces of equipment whose use is nearly limited to power devices. Thus, many companies can not devote the resources necessary to obtain this piece of sophisticated equipment.

We are now presented with a dilemma - how to test these devices without the use of a curve tracer. Is it possible to use an ohmmeter or megger? For extremely limited testing, yes, for dwelving deeper into the device's operation, no. Basically, if the device is so totally damaged that it is completely shorted, then this test will work. However, if the device is not completely shorted, the results obtained may be misleading due to the small test currents and/or voltages. This may lead to confusion or a faulty conclusion as good devices may measure resistances that vary by three or four times, or even appear as an open circuit. Often times, a good device is discarded because of these faulty testing methods. Bad devices may block up to approximately 100V, and then break down before their rated voltage.

As an alternative to using an ohmmeter or megger, simple test circuits can be constructed that allow limited testing of power devices for proper operation. This Design Tip presents three sample circuits for testing these devices. These test circuits go from extremely simple to slightly more complex.

Testing

When testing SCRs, there are two parameters that are crucial to the device's operation: I_{GT} - the DC gate current required to trigger the SCR, and I_H - the holding current necessary to keep the SCR conducting once it has been successfully fired. At room temperature for most of International Rectifier's SCRs, I_{GT} is less than 150 mA, and I_H is less than 500 mA. (If in doubt, please check the SCR's data sheet to ensure that the test circuit is providing the necessary drive and load currents.)

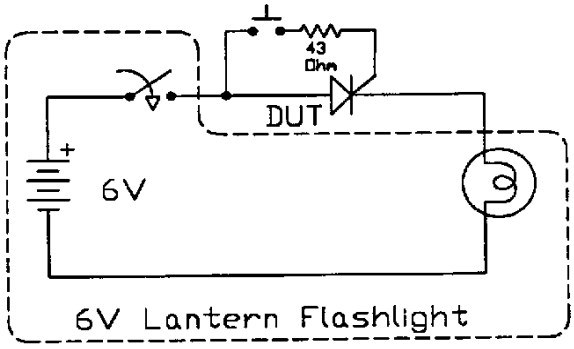


Figure 1 - SCR I_{GT} & I_H Tester

This first test circuit, shown in Figure 1, is simply a 6V latern-type flashlight modified to test the holding function of SCRs. This is an extremely handy test circuit to use in the field. Basically, the SCR is connected in series with the lamp and battery, with a momentary switch providing the gate pulse required to fire the SCR.

The test circuit in Figure 2 is used to test diodes. Two

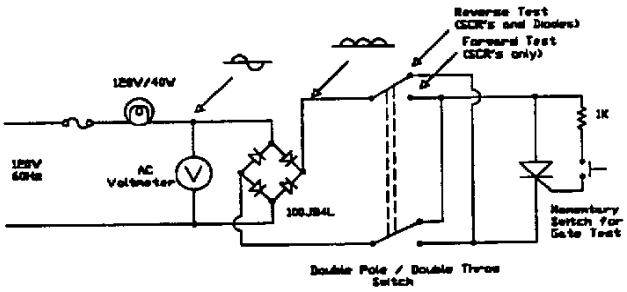


Figure 3 - SCR Blocking/Gating and Diode Blocking Tester

incandescent bulbs double as both loads, as well as indicators. If the diode is damaged, and no longer has reverse blocking capability, both lamps will illuminate, indicating a bad diode. Otherwise, the left lamp should light indicating the diode is functioning properly. Nearly any 12V lamp will work, and D1, and D2 can be nearly any diode. This circuit is limited by the small test currents and voltages available.

Finally, Figure 3 depicts the most complete test setup. Rectified line voltage is applied to the DUT (Device Under Test, i.e., the SCR or diode), to ensure the device blocks under high voltage conditions. The DPDT switch selects the test between forward and reverse. The reverse test confirms that both SCRs and

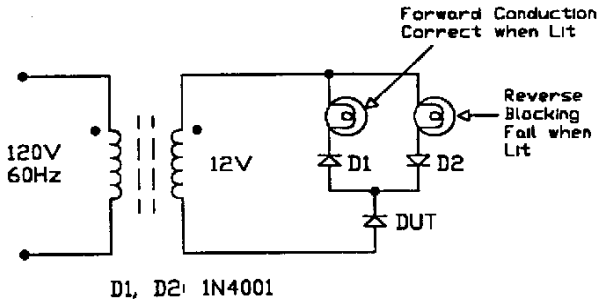


Figure 2 - Diode Tester

diodes block under application of reverse voltage. If the lamp lights during this test, then the DUT is not blocking reverse voltage, and is damaged. This circuit is much more complex than the previous two, but provides the best results because it uses relatively high voltage to test the blocking characteristics.

The forward test is used for SCRs only. This tests the gate of the SCR. The lamp should remain off until the momentary switch is depressed, at which time the lamp should light. The lamp will go out as soon as the switch is released.

Hockey Puk

For the highest power levels, International Rectifier offers the hockey puk package. This is a very reliable, low thermal resistance package in which the contact to the silicon is established by applying external pressure with a clamp. Attempting to measure the characteristics of a hockey puk without having it correctly mounted in a clamp will result in erroneous measurements (likely an open circuit) as proper contact will not be made internally.

Conclusion

Through the use of the simple circuit ideas presented here, high power devices can be debugged for proper operation. The use of an ohmmeter or megger is not recommended. While the above testers provide more reliable information on the functionality of the devices; only curve tracers can accomplish this task thoroughly. The flashlight circuit (Figure 1) is ideal for field use due to its simplicity. The circuit in Figure 3 is ideal for the lab of a technician who often tests SCRs and diodes, but does not have access to a curve tracer.

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CURRENT SENSING WITH THE IR2130

Jamie Catt

Introduction

The IR2130 High voltage MOS gate Driver IC provides a convenient and cost effective gate drive solution for applications requiring a three phase bridge configuration. It comprises three high side and three low side referenced drive channels and has been has been targeted at applications that include:

- WM AC Motor Drives,
- Six Step AC Motor Drives,
- UPS.

The IR2130 has features added to enhance its performance in these applications. These features include:

- Fault indicator output,
- Over current trip input,
- Current signal amplifier.

It is the use of this third feature, the current signal amplifier, that is the subject of this paper.

Amplifier Uses:

The current signal amplifier has been included so that the current in the return leg of the DC supply of the three phase bridge may be monitored. A typical circuit configuration is provided in the IR2130 data sheet.

This signal is amplified by the ratio of the feedback resistors and output on the VCaO pin of the IR2130.

The details of the amplifier connection are shown in Figure 3 of International Rectifier Application Note AN-985.

The shape of the current seen in the DC link will depend on the switching topology used for the three phase bridge. Two such topologies are the “Six Step Inverter” and the “Pulse Width Modulated Inverter”. Suffice to say that for reasonable load levels at moderate to high power factors the DC link current will always be a positive value. Any negative current passed back through the free wheeling diodes in the bridge due to the lagging current will be absorbed in the bridge and not appear in the DC link.

At light or low power factor loads the negative current levels will begin to exceed the positive demands in the bridge and a net negative current will flow in the DC link. The same will occur if the load is caused to regenerate back into the system.

Amplifier Limitations:
The recommendations for the operating limits of the internal current amplifier as specified in the data sheet are as follows:

V_S	(Low Side Drive Return)	-5 to +5 V
V_{CA}	(Amplifier Inverting Input)	0 to 5 V
V_{CAO}	(Amplifier Output Voltage)	0 to 5 V
I_{SRC}	(Amplifier Output Source Current)	2A
I_{SINK}	(Amplifier Output Sink Current)	0.5 mA

From these figures it is obvious that the output of the amplifier will not provide a negative voltage. This means that any negative current excursions in the DC link through the current sensing resistor will not appear at the output of the amplifier. This loss of information is further compounded by a characteristic of the amplifier that is not obvious from the data sheet. A recovery delay exists in the current sense amplifier operation as the input signal changes from a negative to a positive value.

The loss of negative input signals and the recovery delay of the amplifier is illustrated in Figure 1 where a triangular input was used as an example. The length of the delay is related to the dv/dt at the zero crossover of the input signal. As described earlier, negative inputs to the current sense amplifier are possible at light and low power factor loads. These negative excursions of current will be lost by the current amplifier.

Solution:
The recovery delay of the amplifier is due to the Vs input pin to the amplifier saturating when a negative voltage is applied . The charge accumulated requires time to be removed or dissipated before the amplifier will begin to function correctly. The only method to stop this recovery delay time is to inhibit the Vs input voltage from going negative.

The input voltage will generally be of a small magnitude (less than 1 volt) since it is desirable to minimize the losses across the current sensing resistor and not introduce excessive voltages that will upset the drive circuitry. Such a small voltage signal is unsuitable for diode clipping.

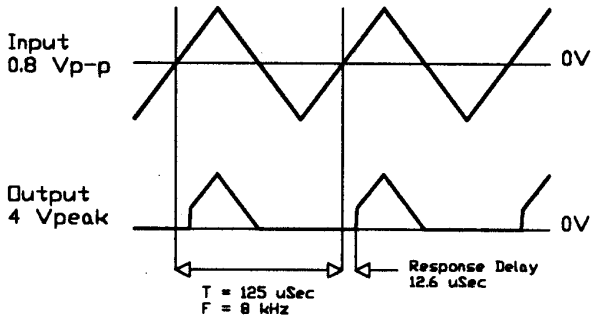


Figure 1. **Current Amplifier Operation with Triangular Waveform Input**

Method 1:
The signal to the non-inverting input to the amplifier must be inhibited from having a negative value. If a differential amplifier is used with a voltage reference to shift the effective zero current reference input signal, the output will appear as an amplified version of the input signal, offset by some positive voltage The circuit for this solution is shown in Figure 2.

The relevant calculations for the selection of components for the given circuit are given in the Appendix. It can be seen that the choice of components is limited by the total amount of resistance allowed in the gate loop, and the maximum current that can be sourced by the internal amplifier.

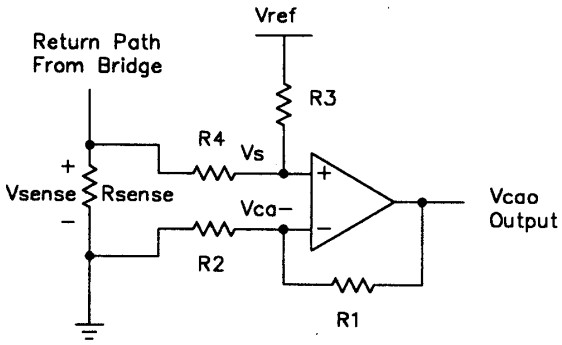


Figure 2. **Differential Amplifier with Voltage Offset**

Method 2.
As stated in Method 1, the signal to the non-inverting input of the amplifier must be inhibited from having a negative value. This can be achieved by only allowing the positive components of current to pass through the sense resistor.

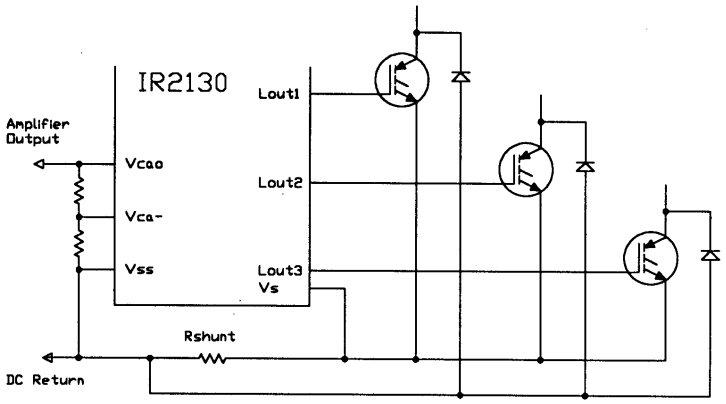


Figure 3. **Measurement of Positive Current Components in the DC Link**

Since the positive components of current in the three phase bridge pass through the switching devices, and the negative components pass through the free wheeling diodes, it is a relatively simple operation to separate them. The circuit in Figure 3 shows an implementation of this technique in a bridge that utilizes IGBTs. When MOSFETS are used as the switching devices an additional diode is required in series with each MOSFET to negate the internal body-drain diode. This is illustrated in Figure 4.

Method 3:
A variation on Method 2 that may have advantages in respect to component count and cost in a MOSFET bridge is shown in Figure 5. The positive components of DC link current are passed through the shunt resistor by a diode. Negative current components are blocked by the shunt resistor diode and forced through a second rated parallel diode. These diodes do not have to be high voltage rated, but will have to carry the Full DC link current.

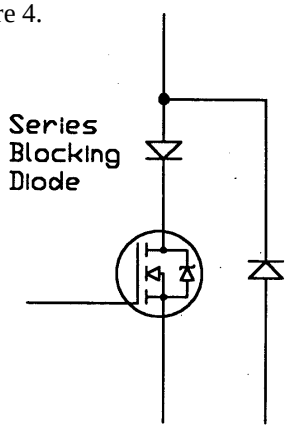


Figure 4. **MOSFET Connection for Separation of Positive and Negative Current Components**

Conclusion:

The IR2130 has an internal current signal amplifier designed to monitor the current flowing in the DC link. The amplifier provided has limitations in regard to the range of input signals it will operate with and poor response delay from a negative input signal. Improving the performance of the amplifier is awkward since the input pin on the IC for the non-inverting input to the amplifier is also the gate return connection for the drives to the low side devices.

Three solutions have been presented that alleviate the performance limitations of the amplifier and will improve the functionality of the IR2130 in applications where accurate current sensing of the DC link is required.
Method 1 enables the use of the total link current, including negative current components. Methods 2 and 3 allow only the positive components of DC link current to be passed through to the IR2130 internal current amplifier.

Appendix 1 Component Selection

When selecting components to use with the internal current amplifier the following design guidelines should be followed.

- The maximum value of resistor that can be inserted in the gate return path is 47 Ohms. Larger values than this may affect the switching performance of the device.
- The maximum output current of the amplifier is 2mA under worst case conditions.

Consider the circuit configuration shown in Figure 2. The gain of the non inverting amplifier stage is:

$$\frac{VCaO}{Vs} = 1 + \frac{R1}{R2} \qquad \textbf{(1)}$$

The signal at the VSO pin may be defined by the equation:

$$VS = Vsense + (Vref - VSenSe) \times \frac{R4}{R3+R4} \qquad \textbf{(2)}$$

Combining equations (1) and (2) gives:

$$VCao = Vsense \times \left(1+\frac{R1}{R2}\right) + \left[(Vref \sim Vsens) \times \frac{R4}{R3+R4}\right] \times \left(1+\frac{R1}{R2}\right)$$

If the conditions R1 = R3 and R2 = R4 are true, then the last equation collapses to:

$$VCao = Vref + \frac{R1}{R2}$$

Using the design guidelines sets the range of resistor values that may be chosen. The 2mA current limit sets a minimum a minimum for the resistance sum R1 + R2. -This limit is defined by:

$$Ilimit = \frac{VcaO(max)}{R1+R2}$$

Ilimit = 2mA, Vcao(max) = 5V

This means that R1 + R2 > 2.5 kΩ. R2 is limited to 47 Ohms and R1 > 2.45 kΩ. This gives a gain in the circuit of R1/R2 = 52. If the output of the amplifier is in the range [0;+5V], then the offset could be 2.5 V, giving an allowable output voltage variation of +/-2.5V. The maximum variation of the input voltage is thus +/-50mV. This small signal level is possible with commercially available shunts that are low inductance to reduce noise from power device switching. It does mean however that the internal current trip function of the IR2130 cannot be used, as it has an internal 0.5V trip point. Care should be taken when using small input signal levels as the data sheet specification for the amplifier offset voltage is 10mV. An offset adjustment may need to be included in the circuit.

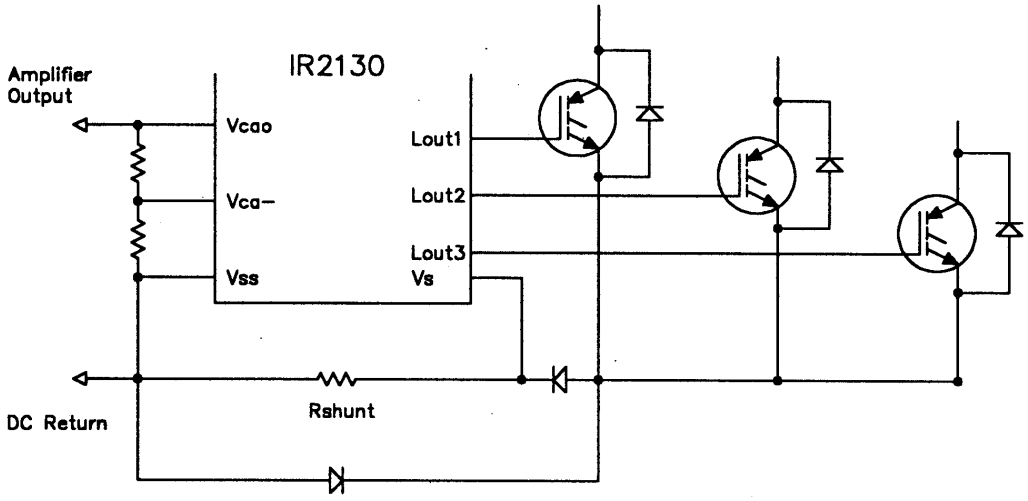


Figure 5. **Current Sense Blocking Diode**

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SIMPLE HIGH SIDE DRIVE PROVIDES FAST SWITCHING AND CONTINUOUS ON-TIME

By Laszlo Kiraly

INTRODUCTION

P-channel power MOSFETs are typically used as high-side switches in low power applications because of simplier gate drive circuitry. As power levels, either voltage or current, increase, the advantages of P-channel devices are quickly offset by their increased on-resistance, limited voltage range, increased cost, and increased complexity of the gate drive circuitry. By switching to an N-channel device, it is possible to improve on the P-channel's disadvantages, at the expense of increased gate drive complexity. For high power levels, the IGBT is extremely well suited for use as a high-side switch, yet all currently available IGBTs are N-channel devices. Presented is a circuit that, with the use of an extra IC and a few passive components, solves the N-channel gate drive circuit issue.

DEDICATED HIGH SIDE DRIVERS MAKE LIFE EASIER

The Control IC drivers from International Rectifier provide ground referenced, logic level inputs, and high energy, low impedance gate drive for MOSFET or IGBT power transistors up to 500V DC operating voltage when used in switchmode applications. These Control ICs use the bootstrap technique to create gate voltage for the MOS-gated device and to power the floating section of the high-side driver. The advantages of the bootstrap circuit are its simplicity and the fast switching times, but to keep the bootstrap capacitor charged the MOS-gated device has to periodically be turned off. With the addition of a simple charge pump, both the fast switching of the bootstrap circuit and unlimited on-time of the charge pump circuit can be achieved.

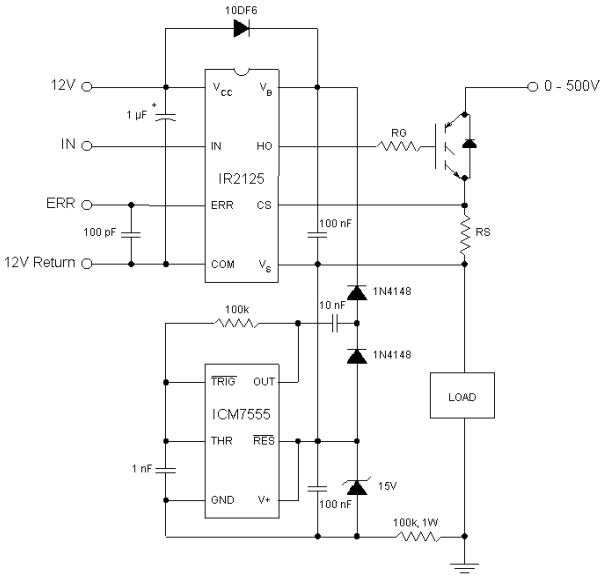


Figure 1
High side drive provides fast switching, continuous on-time and protection for the switching device

CIRCUIT AND TEST RESULTS

The schematic diagram of the circuit is shown in Figure 1. The IR2125 Control IC was selected to demonstrate the cooperation of the charge pump and the bootstrap circuits. The IR2125 also has an over-current shut down capability, providing protection for the MOS-gated device. To provide the low operating current requirement of the IR2125, the charge pump employs a 555 CMOS timer.

When the IGBT is off, the bootstrap capacitor is charged through the 10DF6 diode and the load resistor. When the IGBT is on, the 100 kΩ resistor connected to ground charges the 100 nF capacitor connected between leads 1 and 8 of the 555 timer generating -15V referenced to lead 5 of the IR2125. The charge pump circuit formed by the two 1N4148 diodes and the 10 nF capacitor which converts the 7.5 kHz square wave at lead 3 of the 555 timer to +15V referenced to V_S and charges the bootstrap capacitor.

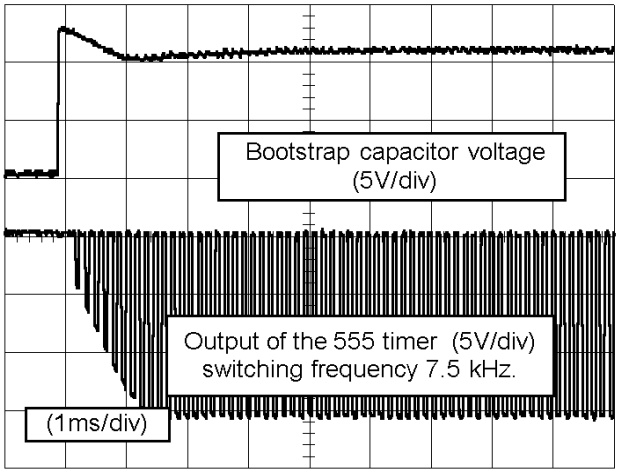


Figure 2
Wafeforms at start-up

Figure 2 shows the circuit waveforms at start-up. As the IGBT turns on, the bootstrap diode disconnects lead 8 of the IR2125 from the +12V power supply, and the voltage across the bootstrap capacitor starts dropping. At the same time the 100k resistor located between lead 1 of the 555 timer and ground starts charging the 100 nF capacitor connected to it and generates supply voltage for the CMOS (MAXIM ICL71555IPA) timer. The output voltage of the charge pump increases with increasing supply voltage. The charge pump maintains the voltage in the bootstrap capacitor, keeping the voltage above the undervoltage threshold level of the IR2125.

DESIGN CONSIDERATIONS

- The absolute maximum voltage supply voltage for the 555 is 18V, consider this when selecting the zener diode and its tolerance.
- The supply current at the V_B pin (I_{QBS}) of the IR2125 increases with increasing temperature.
- The 100k 1kW resistor should be sized according the maximum supply current at the high side of the IR2125, the minimum operating power supply voltage and the timing requirements.

CONCLUSION

This simple, inexpensive charge pump circuit overcomes the maximum on-time limitation of the bootstrap circuit. The circuit presented above utilizes the advantages of the bootstrap and charge pump technique providing excellent switching speed and steady state operation allowing the use of an N-channel MOS-gated power device as a high-side switch. This improves system efficiency, expands voltage range, and reduces the cost of the power device required.

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USING STANDARD CONTROL IC'S TO GENERATE NEGATIVE GATE BIAS FOR MOSFETS AND IGBTS

By Laszlo Kiraly

INTRODUCTION

Inherently neither the MOSFET nor the IGBT requires negative bias on the gate. Setting the gate voltage to zero at turn-off insures proper operation and virtually provides negative bias relative to the threshold voltage of the device. Negative gate bias does not significantly affect switching speed as opposed to the bipolar transistor. However, there are circumstances when a negative gate drive is necessary:

- The semiconductor manufacturer specifies negative gate bias for the device
- When the gate voltage can not be held safely below the threshold voltage due to noise generated in the circuit.

Although reference will be made to IGBTs, the information contained is equally applicable to power MOSFETs.

DC GATE CHARACTERISTICS

The minimum threshold voltage for most IGBTs is 3V at room temperature. The temperature coefficient of the threshold voltage is always negative; increasing junction temperature results in decreasing threshold voltage. If the junction temperature rises from 25°C to 150°C, and the temperature coefficient is -11 mV/°C, then the threshold voltage decreases by 1.4V. Thus, a threshold voltage of 1.6V can be expected at high temperature and worst case conditions.

DYNAMIC OPERATION

The problem arises when the voltage increases rapidly between the collector-emitter terminals of the IGBT. During the transient, the gate-collector (Miller) capacitance delivers charge to the gate, increasing the gate voltage. The height and width of the voltage 'blip' at the gate is determined by the ratio of the gate-collector and gate-emitter capacitances, the impedance of the drive circuit connected to the gate, and the applied dV/dt between the collector-emitter terminals.

The internal capacitances are given on the data sheet. Notice the Miller capacitance of the IGBT is smaller than a similarly rated MOSFET, due to the smaller die size.

The impedance to the gate can be minimized by selecting a low impedance Control IC and by minimizing the stray inductance in the drive loop.

The dV/dt can be set to an optimum value (noise versus losses) by selecting the proper value of series gate resistor. The series gate

resistor affects only the turn-on speed of the IGBT, the turn-off speed is largely determined by the IGBT itself. A parallel diode, with the anode towards the gate, across the gate resistor is also recommended. The diode is reverse biased at turn-on but holds the gate down at turn-off, and during the off state.

The Control IC has to have an electrically separated reference pin for the gate drive output. This pin should be connected directly to the emitter terminal of the IGBT, or the Kelvin terminal of the IGBT module. The gate and the emitter voltages are then floating on top of the noise generated by high current ground wiring, but the difference of the two voltages (the effective drive voltage) is free from the noise.

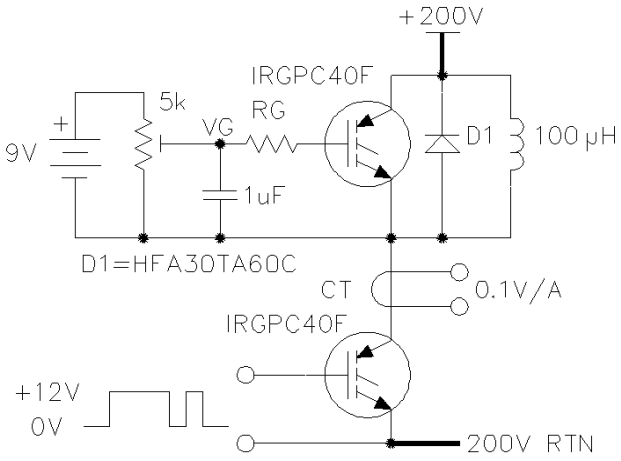


Figure 1
Test Circuit

INTERNATIONAL RECTIFIER's IGBTs DO NOT REQUIRE NEGATIVE BIAS

The IGBTs made by International Rectifier do not require negative bias. The switching times and energy loss values that are published on the data sheets for both discretes and modules were measured at zero gate voltage turn-off. With shorted gate-emitter terminals, the IGBT will withstand the highest dV/dt another similar IGBT can produce in the circuit, without latching or partial turn-on. A common misconception is identifying the current 'blip' due to charging the output capacitance (C_{oes}) of the IGBT as conduction current. The amplitude of the current 'blip' is approximately 5A for a IRGPC50F IGBT at a dV/dt of 20V/ns. The amplitude of the 'blip' does not change with the applied negative bias.

The following test was conducted to determine the threshold voltage and the effect of the series gate resistance in high dV/dt applications. The test circuit is shown in Figure 1. The positive bias to the upper IGBT was increased until the switching losses in the bottom IGBT indicated excessive shoot-through current. The turn-on loss was measured at 15A inductor current and 6V/ns switching speed. The results are shown in Figure 2. The threshold voltage levels increasing the turn-on losses are 4V, 5V and 5.6V with 47Ω, 10Ω, and 0Ω series gate resistance, respectively. A parallel diode across the series gate resistor (anode toward the gate) helps clamp the gate low, so the series gate resistor can be sized according to the turn-on requirements.

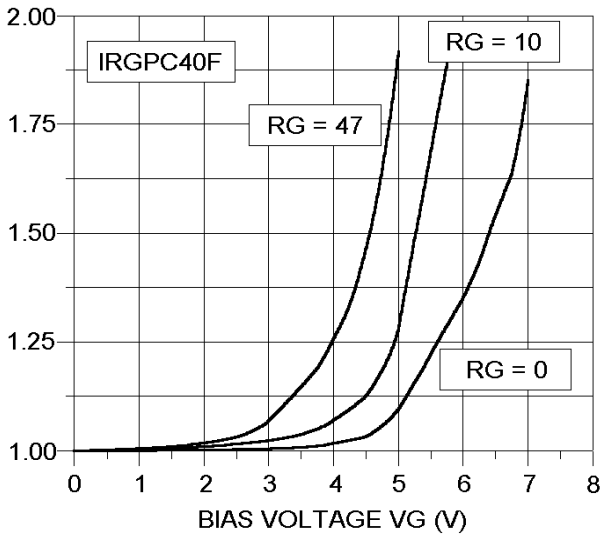


Figure 2
Normalized Turn-On Losses vs. V_G

BUFFER AND NEGATIVE CHARGE PUMP

The basic buffer circuit and the negative charge pump are shown in Figure 3. The buffer circuit employs two P-channel and two N-channel MOSFETs. Resistor R1 between the gates of Q3 and Q4 slows down the turn-on of the output transistor and limits the shoot-through current in the drivers. D1 reduces the voltage to the gate of Q3 and Q4. D2, C2 and R2 form a level shifter for Q2. C3, C4, D3 and D4 convert the incoming signal to negative DC voltage. After turn-on, the negative voltage settles in a few cycles even at extremely low or high duty cycles (1 - 99%). The settling time and the stiffness of the negative voltage are affected by the output impedance of the signal source.

DRIVING LARGE FLOATING LOADS

The circuit is shown in Figure 4 utilizes the high voltage level shifting capability of the IR2110 and the drive capability of the MOS buffer shown in Figure 3. It also generates negative voltage for turn-off. The circuit was tested with an IGBT module part number IRGSI270F06 capable of 270A connected to each output. The gate total charge for the module is 600 nC. The waveforms are shown in Figure 5. The turn-on delay of the circuit is 1 µs, the turn-off delay is 0.2 µs. The settling time of the negative bias voltage is about 10 ms at 5 kHz switching frequency at 50% duty cycle. At start-up, the circuit delivers some negative gate voltage even after the first cycle. During power down, the gate voltage remains negative until the reservoir capacitor discharges.

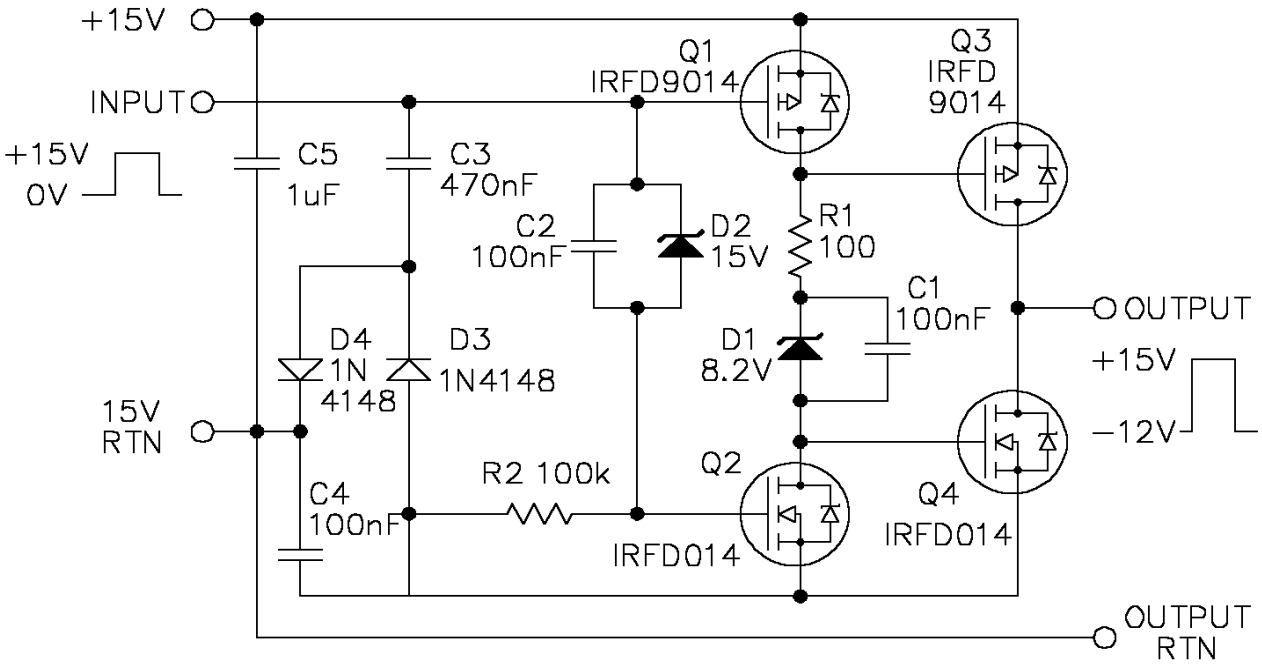


Figure 3
Buffer With Negative Charge Pump

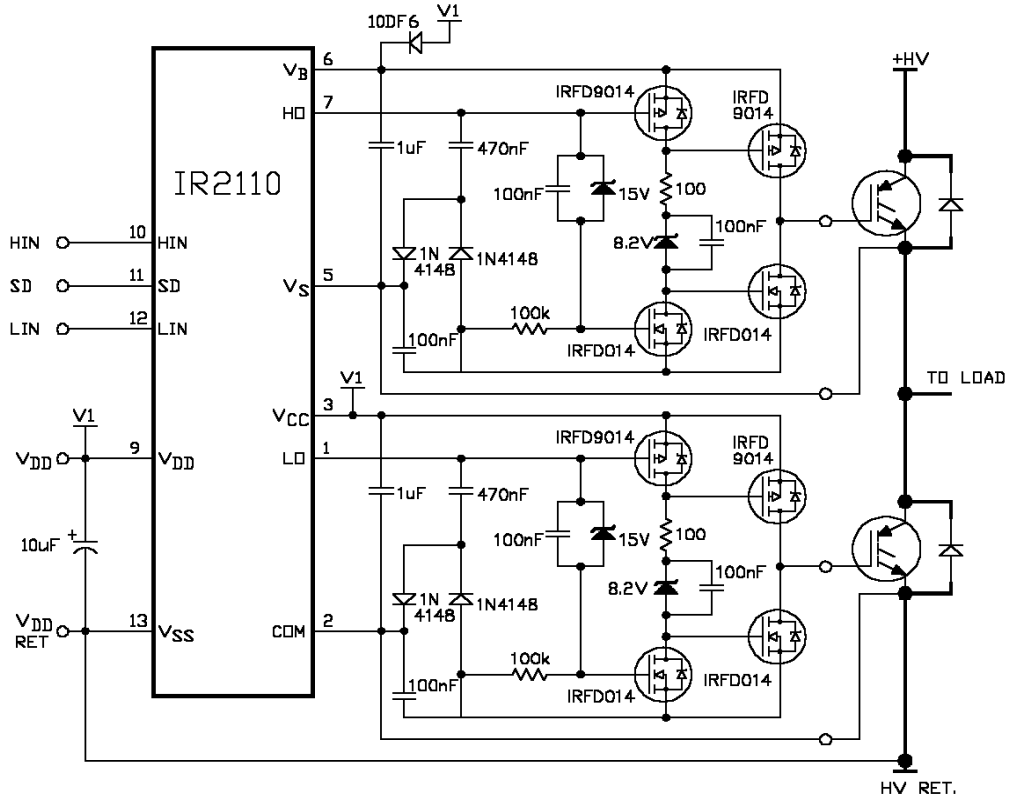


Figure 4
Half-Bridge Drive That Generates Negative Bias

A Simple Control IC with Negative Bias

Though the circuit evolution process usually results in more complication and less reliability, our circuit evolved in a different manner. The buffer and negative charge pump were removed, and the circuit became very simple as shown in Figure 6. Input and output waveforms are shown in Figure 7. The negative voltage is provided by an external power supply, while the negative bias voltage for the high-side is generated by a 100k resistor and a zener diode. The negative gate voltages are limited to the maximum applicable offset voltage between the V_{SS} - COM and V_{SS} - V_S leads. The total power supply voltage to the IR2110 cannot exceed 20V. The 100k resistor is sufficient for HV = 160V, 50% duty cycle operation. Different operating conditions may require different resistor values. The average current through the resistor should be at least 1 mA. The power handling capability and maximum operating voltage of the resistor also have to be considered. Since the operating current of the zener diode is small, the special low current ones are preferable in this application.

CONCLUSION

Both discrete and IGBT modules made by International Rectifier do not require negative bias for proper operation. The Control ICs can be used with minimal amount of external components. However, there are IGBT manufacturers specifying negative bias on their products, and the noise margin can also be improved by applying negative bias to the gate during the off state. The circuit in Figure 4 was intended for high power IGBT module drive applications. The circuit shown in Figure 6 is an economical solution for medium power IGBT applications.

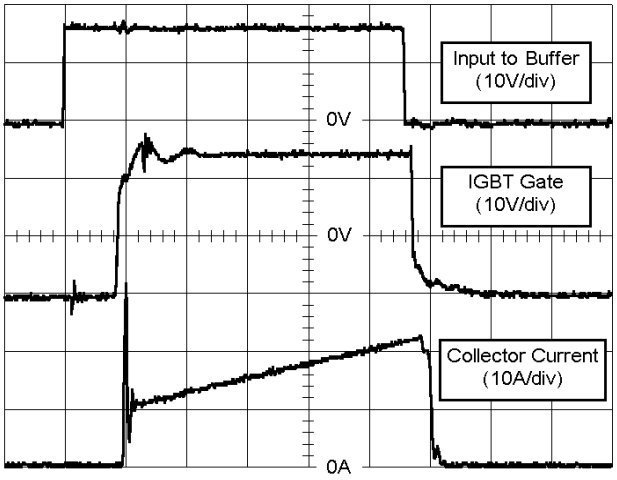


Figure 5
Waveforms From Negative Bias Half-Bridge Driver
(1 µs/div)

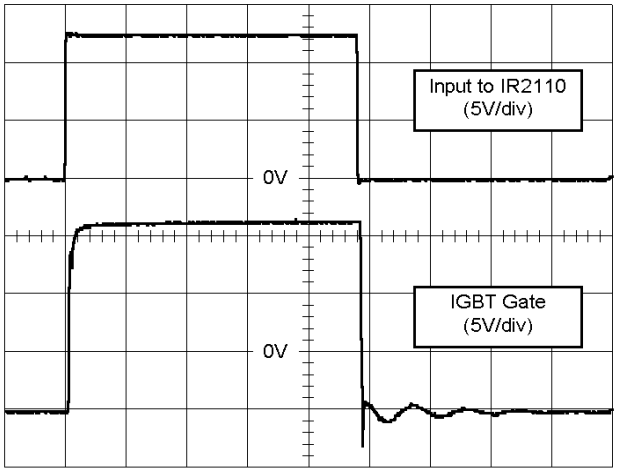


Figure 7
Waveforms From Circuit in Figure 6
(2 µs/div)

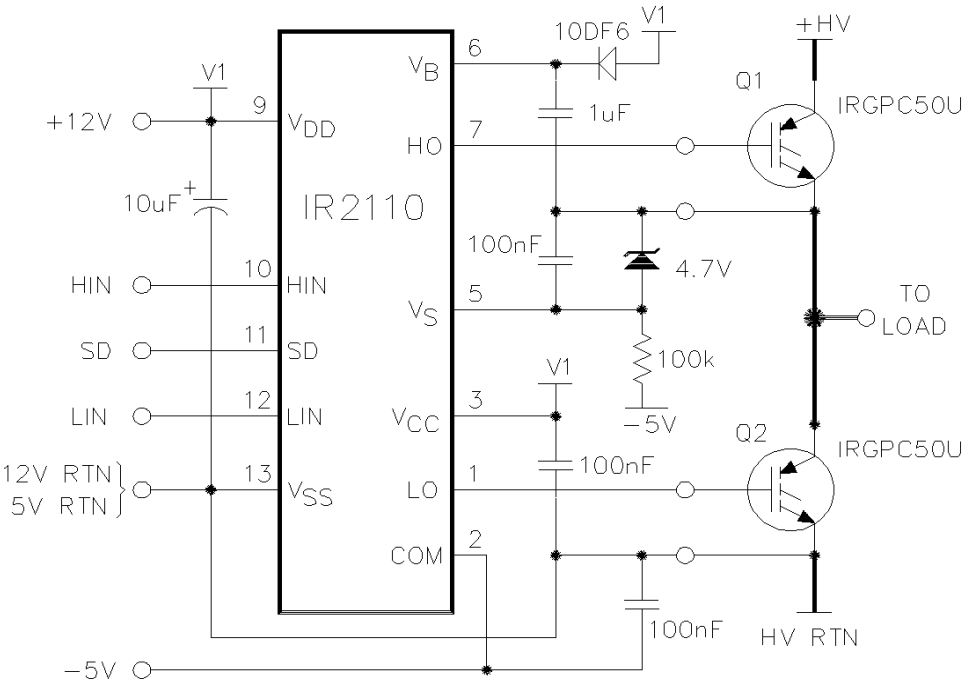


Figure 6
Half-Bridge Driver With External Negative Bias

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HIGH CURRENT BUFFER FOR CONTROL IC'S

By Laszlo Kiraly

INTRODUCTION

Modules and other paralleled MOS-gated power transistors can present difficulties to gate drive circuits. International Rectifier's family of Control IC drivers can provide large peak output currents acceptable for most applications. However, when driving the extremely large loads of many paralleled devices, excess power dissipation in the MOS-gate drive section of the Control IC may become an issue when switching above the few tens of kilohertz range. The subject of this Design Tip is a current-buffer to alleviate this problem.

The high input impedance power buffer shown in Figure 1 delivers 8A peak output current yet draws negligible quiescent current.

Q1 and Q2 are low current drivers for Q3 and Q4 which can be sized to suit the peak output current requirement.

OPERATION

When the input signal changes state, R1 limits the current through Q1 and Q2 for the few nanoseconds that both transistors are on.

When the input settles to its new state, the driver transistor quickly discharges the gate capacitance of the conducting output transistor forcing it into off-state. Meanwhile the gate of the other output transistor will be charged through R1; the turn-on will be delayed by the RC time constant formed by R1 and the input capacitance of the output transistor.

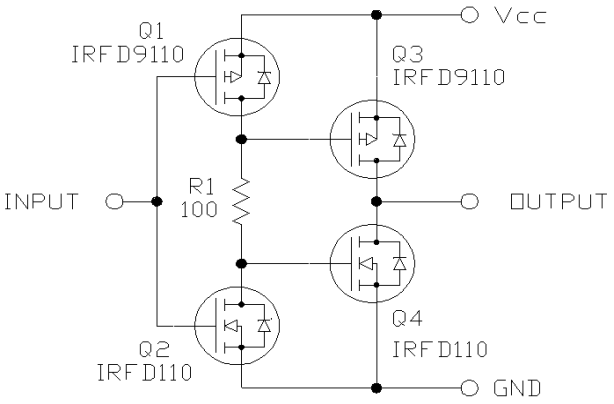


Figure 1

TEST RESULTS

The test circuit is shown in Figure 2. The buffer receives its drive signal from the IR2110, and drives an IGBT module which has a total gate charge (Q_G) of 600 nC. The IGBT module switches an inductive load current of 60A. The typical switching performance is shown in Figure 3. Turn-on and turn-off delays are 50 nS. Rise and fall times are less than 40 nS.

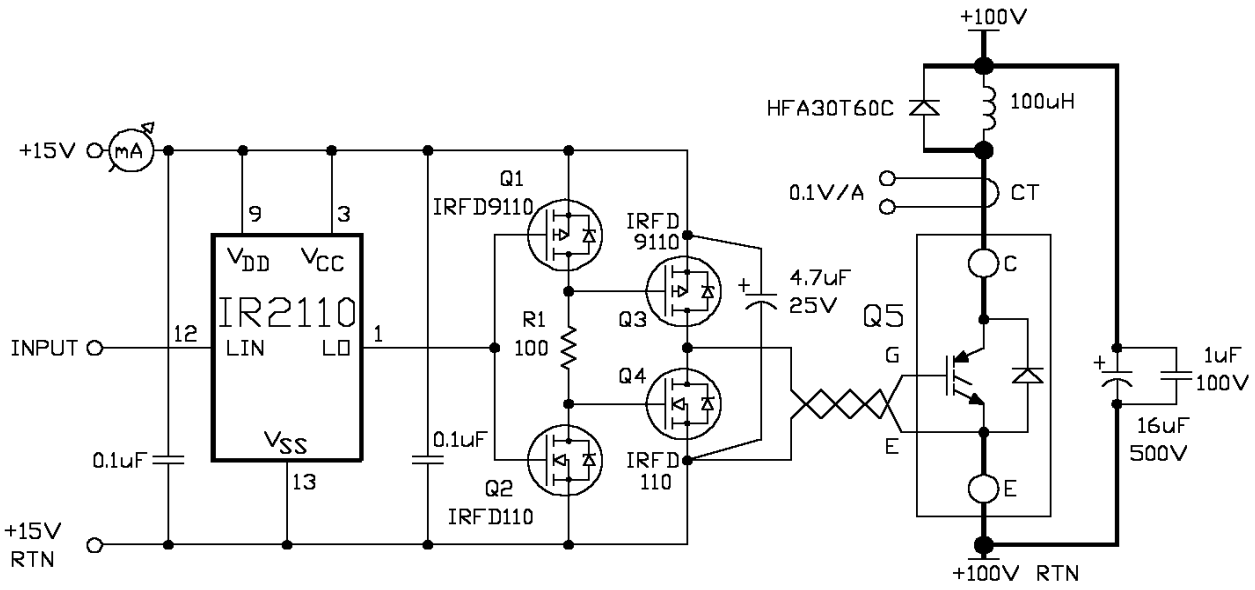


Figure 2
Test Circuit

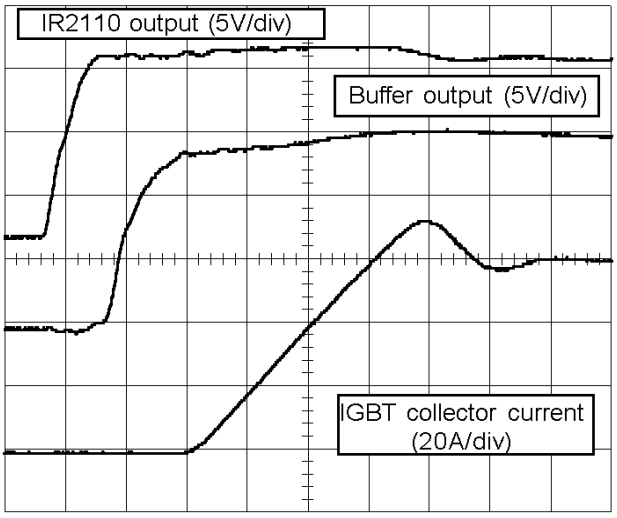


Figure 3a
Waveforms, turn-on. IGBT module switching inductive load of 60A.
(50 ns/div)

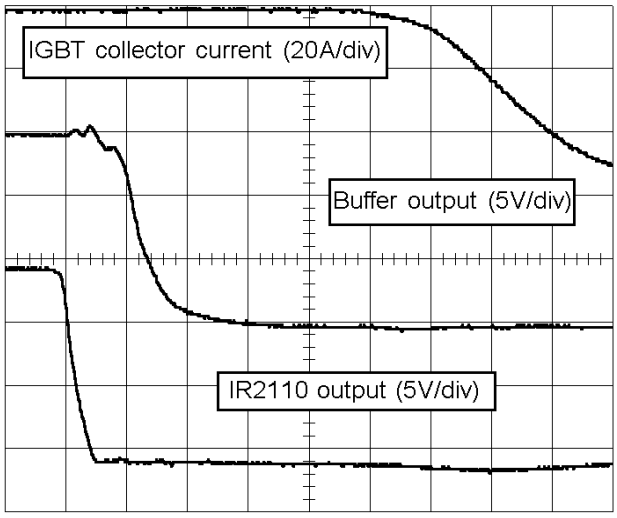


Figure 3b
Turn-off. Propagation delay is 50 ns, fall time is less than 40 nS when driving 600 nC gate charge of the module.
(50 ns/div)

The buffer was tested with a 0.1 µF capacitive load. The waveforms are shown in Figure 4. The ringing was due to the resonant circuit at the output, formed by the capacitive load and the stray inductances.

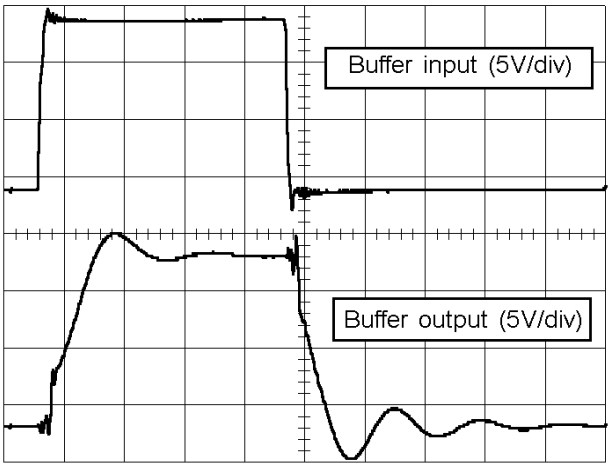


Figure 4
Waveforms driving 0.1 µF capacitor (250 ns/div)

The current consumption vs. frequency plot is shown in Figure 5.

APPLICATION SUGGESTIONS

A high current half-bridge circuit is shown in Figure 6.

It is possible to use lower voltage HEXFETs (i.e. 60V), but it was found that the large reduction in $R_{DS(on)}$ gave rise to large peak currents which caused a great deal of noise and ringing in the circuit.

LAYOUT SUGGESTIONS

- Use good quality 10 µF tantalum or 10 µF electrolytic and 0.1 µF ceramic capacitors at the output of the buffer. These decoupling capacitors should be mounted physically close to the output HEXFETs to nullify the effects of stray inductance. They reduce the ringing at the gate during turn-on.

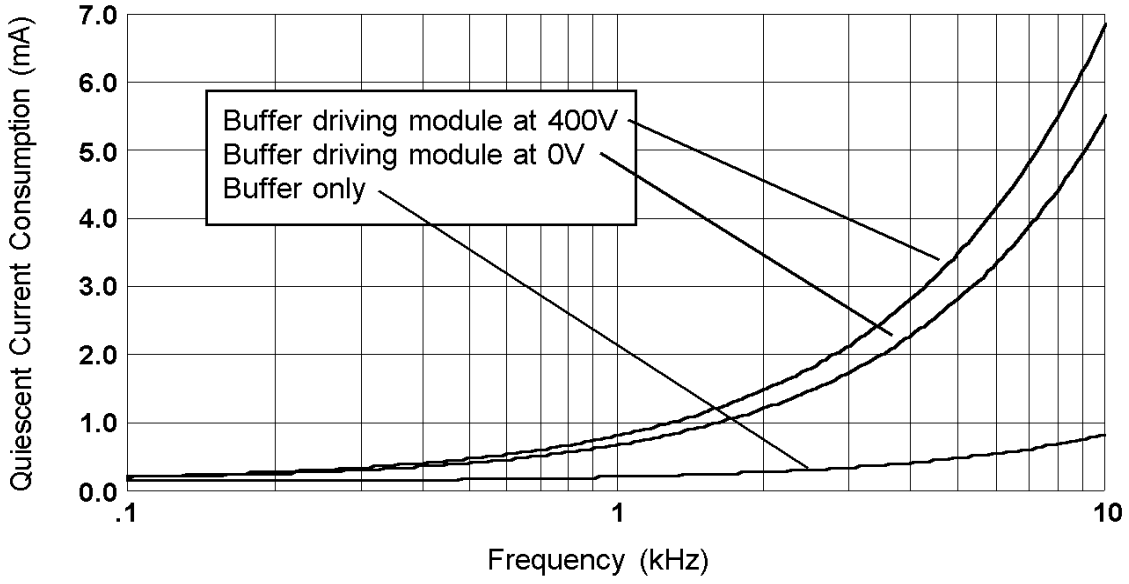


Figure 5
Current consumption vs. frequency

- Use short, tightly twisted wires between the output of the buffers and the modules.
- Use a single point ground at the emitter of the bottom IGBT module. In a bridge configuration, connect the emitters of the bottom IGBT modules to a common point with short heavy wires. Use this point as a common ground.
- Use a low ESR decoupling capacitor (Cf) at the power stage. The value of the capacitor depends on the quality of the layout and switched current. The typical value is between 10 µF and 1000 µF.

(HEXFET is the trademark for International Rectifier Power MOSFETs)

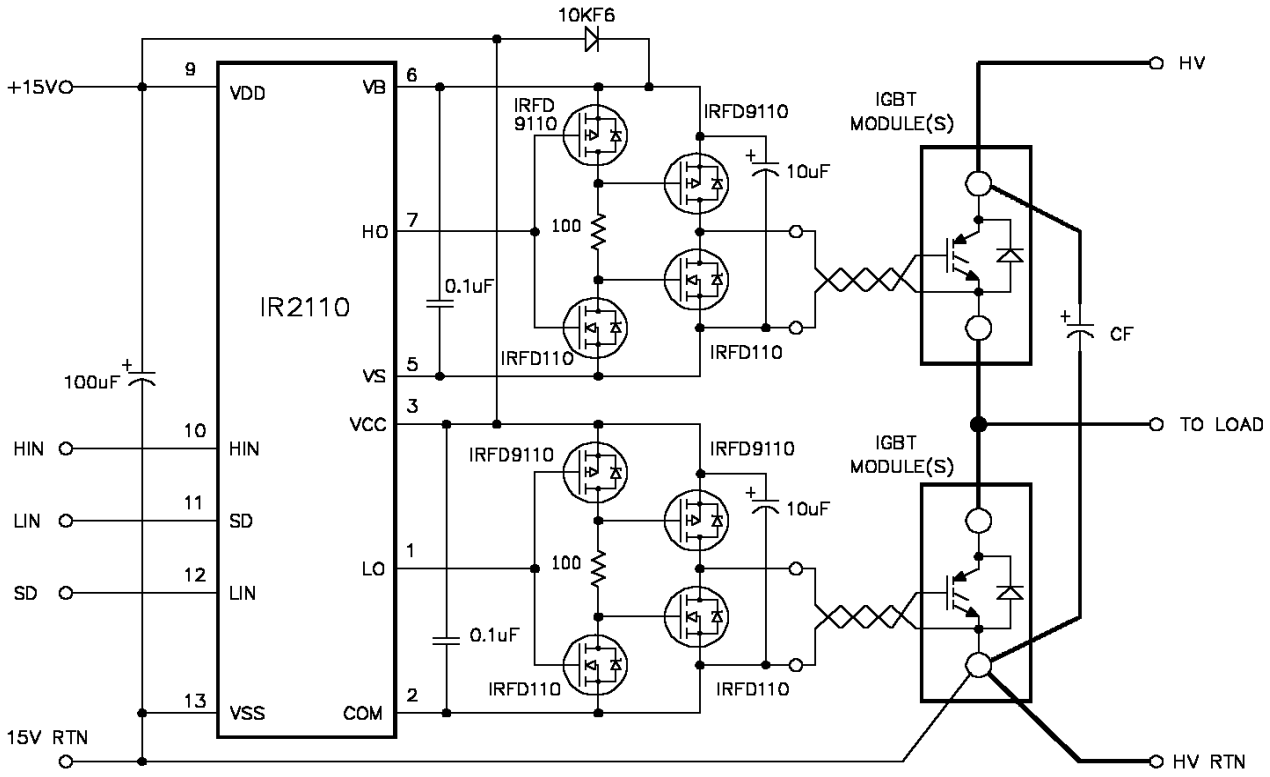


Figure 6
Application circuit schematic

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IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 3L1, Tel: (905) 475 1897 **IR GERMANY:** Saalburgstrasse 157, 61350 Bad Homburg Tel: 617 237066 **IR ITALY:** Via Liguria 49, 10071 Borgaro, Torino Tel: (39) 1145 10111 **IR FAR EAST:** K&H Bldg., 2F, 3-30-4 Nishi-Ikeburo 3-Chome, Toshima-Ki, Tokyo 171 Tel: (03)39830641 **IR SOUTHEAST ASIA:** 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371
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IRMDAC2

IR2133 Reference Design Kit: 3-Phase 230VAC 3HP Motor Drive

Product Description

The IRMDAC2 Reference Design is a kit of parts that work together as an evaluation platform for IR2133 three phase motor control IC and IRPT2056A power module. User connects three phase AC, drive signals, motor and hall sensors to complete the system. Power hook-up is via terminal blocks and control signals are made using a single in line header.

How the IR2133 Control IC Adds Value

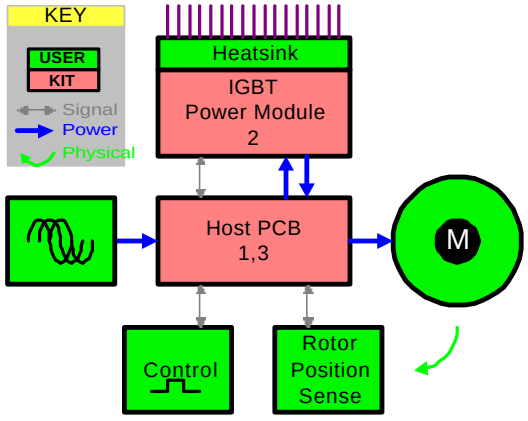
- Monolithic HVIC Integrates Control and Drive Yields Compact, Robust, Economical Designs
- Allows Elegant, Convenient System Partition
- Compatible with Short Circuit, Ground Fault and Over-Temperature Protection Schemes

How the Power Module Adds Value

Integration of All Inverter Power Components;

- Low Parasitic Coupling = High Performance
- Current Sensing Shunts in DC Feed and Return
- Onboard Temperature Sensor
- Easily Mounted Package
- Short Circuit Rated, Ultrafast IGBT Gen #4
- Wide Operating Temperature Range
- Metal Base gives Excellent Thermal Transfer and Isolation to 2500V RMS

System Block Diagram *Fig 2*



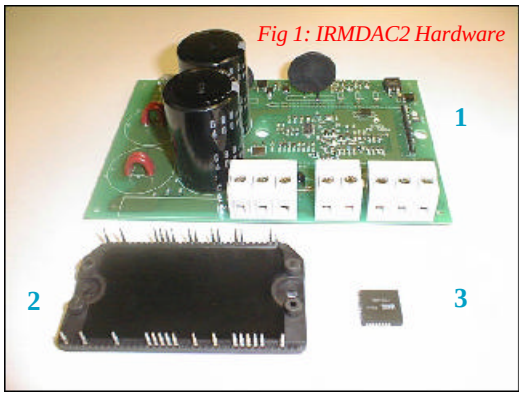


Fig 1: IRMDAC2 Hardware

Kit Content

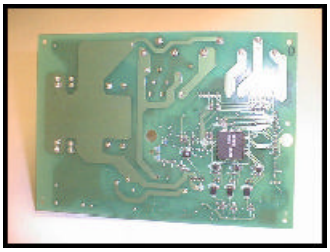
1 Host PCB for Input Processing and Control
2 IRPT2056A Integrated Power Module
3 IR2133J Three Phase Motor Control IC
Technical Contact and License Detail
Schematic and PCB Layout Data
Bill of Materials and Supplier Information

System Features

- 230V Three Phase AC Inlet, 50/60Hz
- Convenient Signal and Power Terminations
- Inrush Current Limit and Surge Suppression
- Integral +15V and +5V Bias Supplies
- DC Bus Voltage and Current Feedback
- 150% Overload Capability (1 Minute)
- Optimized Drive for Power Module

Fig 3

IRMDAC2
Host PCB
Bottom Layer



IRMDAC2 Kit Overview and System Benefits

- When furnished with user-provided logic level control signals, the IRMDAC2 forms a complete reference design for a 3HP AC motor. Unlike outdated circuits based upon transformer drive or opto-couplers, the system uses International Rectifier proprietary level-shifting gate drive circuits integrated within the IR2133 Control IC. Separation of gate drive / control and low-voltage circuits from the power module included in the kit results in a compact, effecient system. The user benfits from immediate hands-on experience and may customize at will using shematics and circuit ideas as the basis for production designs.

- Gate drive, control and protection circuits are designed to closely match the operating characteristics of the power semiconductors. This allows power losses to be minimized and power rating to be enhanced to a greater extent than is possible by designing with individual components.

- Includes **Brake Switch** and Drive

1. Host PCB Description

The host PCB receives power input from a 3-phase line and control signals provided by the user. In conjuntion with the power module the result is a flexible power conversion system, primarily designed for interface with a 3HP Motor, however other 3-phase loads may also be applied. The host PCB supports soft-start function which reduces inrush current by using an NTC thermistor. Surge suppression is implemented using MOV's as a further degree of protection. Also on-board is a regulated low voltage power supply to provide bias for the IR2133 and other low voltage components. When connected to the power module, the unit is fully protected against overcurrent and ground faults through DC bus voltage and current feedback. Over-temperature is guarded against through feedback from a thermistor embedded within the power module. A 16-pin single in line header connector is provided to interface control signals and two terminal blocks connect 3-phase AC inlet and output to the load. The user provides 5V CMOS / TTL level signals which are then processed by the IR2133 Control IC and delivered to the power module.

Signals Available to User

In addition to availability of bias supplies derived for the host PCB, signals from the power module circuits and those derived and processed on the host PCB such as fault status are available to the user. Current feedback signal from the low side shunt is available on the IFB pin at 0.025V/A. If filtering of this signal is required to remove noise, a high impedance buffer stage should be inserted between signal and filter. DC bus voltage feedback is provided on the VFB pin. This reference is been scaled down by a factor of 100 and should be protected with a high impedance buffer stage.

Fault Behavior.

The system is designed to tolerate overload conditions for one minute. The user should prevent such conditions persisting beyond this period. In the event of shutdown initiated by ground-fault, overcurrent or over-temperature, the inverter outputs are terminated and an LED will light to signal this condition. For more information on fault

response for IR2133, please consult the data sheet.
Brake Function

In order to use the integrated brake switch, an external power resistor should be connected between pins BR and P of terminal block J5. This resistor should be dimensioned for desired braking performance. Carefully choose the value of this component to ensure the brake IGBT integrated within the power module remains below its maximum current capability.

2. Power Module Description

The power module integrates all rectifiers, ultra-fast short circuit rated IGBTs, fast recovery commutation diodes , brake IGBT and other processing components needed for a 3HP Motor Drive or other loads requiring a 3-phase variable frequency and/or PWM drive. Semiconductor dice are mounted on a thermally effecient substrate and housed within a convenient, potted module. When connected to the host PCB, the power components become configured as a 3-phase input bridge rectifier, and IGBT inverter with current sensing shunt resistors. An NTC thermistor is bonded to the substrate to furnish the host PCB with accurate temperature reading. A galvanically isolated metal backplate provides excellent thermal coupling to an external heatsink, which is necessary for full-load operation.

Circuit Layout within the module is carefully designed to minimize inductance in the power path, reduce noise during inverter operation and to improve inverter efficiency. The IR2133 host board should be soldered to the power module pins to complete the assembly. For detailed electrical specifications, please refer to the power module datasheet.

Power Module Mounting and Hook-up Instructions

1. Remove all particles and grit from the heatsink and power substrate
2. Spread a thin layer of silicone grease on the heatsink, covering the entire area that the power substrate will occupy
3. Place the power substrate onto the heatsink with the mounting holes aligned and press firmly into the grease
4. Place the 2XM4 mounting screws and tighten to 1NM torque

External Connections

All input and output control connections are made via a 16-terminal single in line connector J6. Three phase input connections are made to terminals R,S and T of J1. Inverter output terminal connections are made to terminals U,V and W of J7. Positive DC Bus and brake IGBT collector connections are available on terminals P and BR respectively of J5. An external power resistor may be connected between P and BR to dissipate braking energy.

Power-Up Procedure

Upon application of 3-phase input power, PWM inputs must be held high until the protection latch circuitry is reset. To reset this latch before inverter start-up, RESET pin on J6 connector must be pulled down low for at least 2usec. This will

Figure 4 Signal Connector

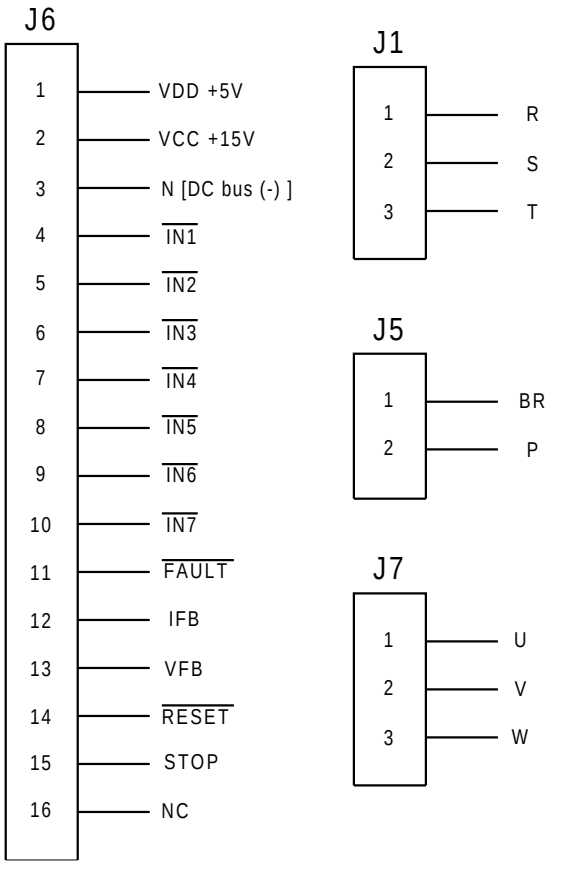
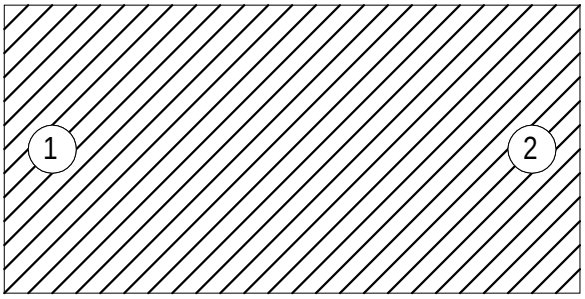


Figure 5 Power Terminal Blocks

Figure 6 Power Module Mounting Screw Sequence



set the Fault feedback signal on J6 high. PWM input signals may then be actively driven.

Mechanical Details

Figure 7

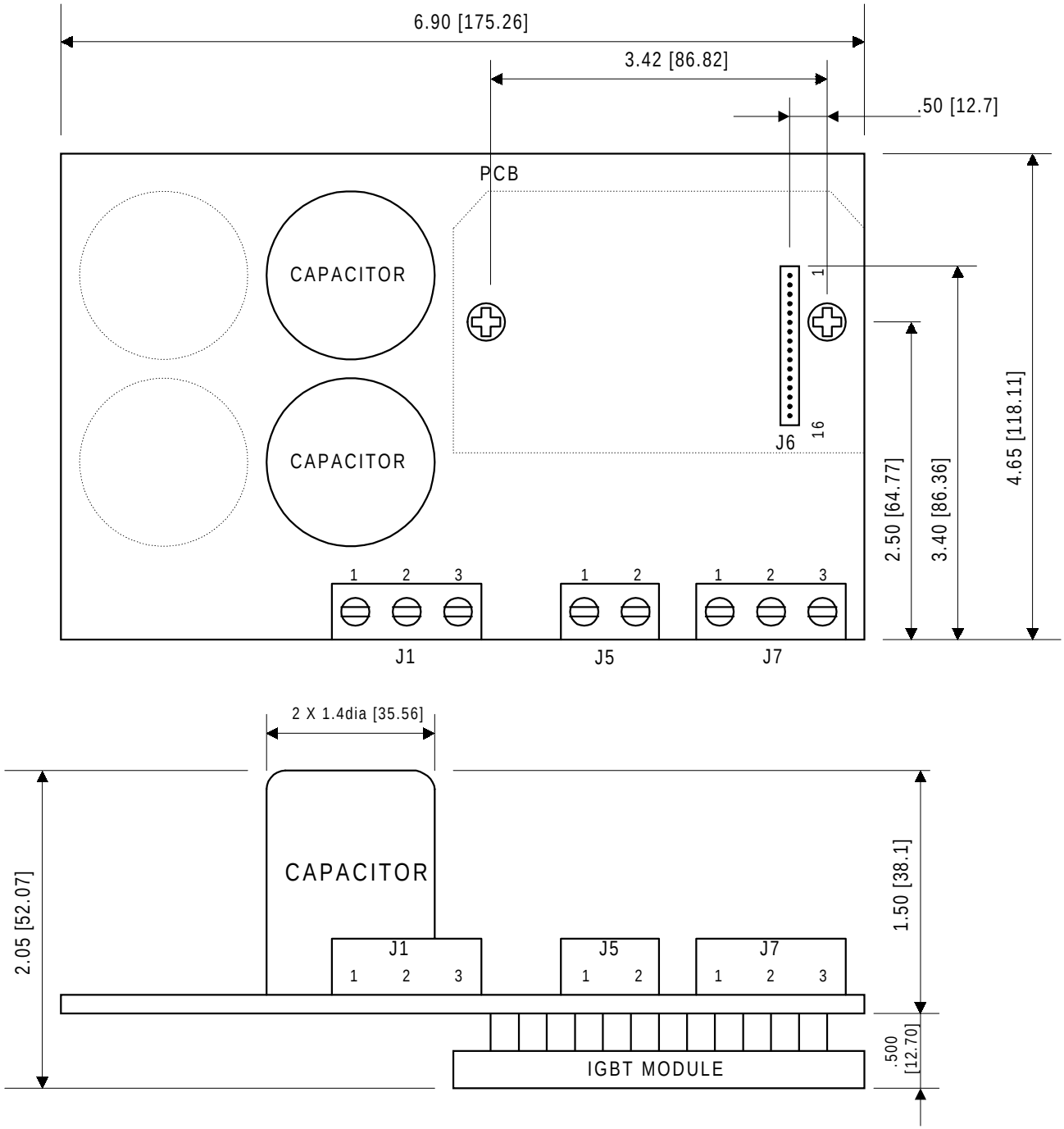


Figure 8: Effeciency Maximization Charts Extract From Module Data Sheet

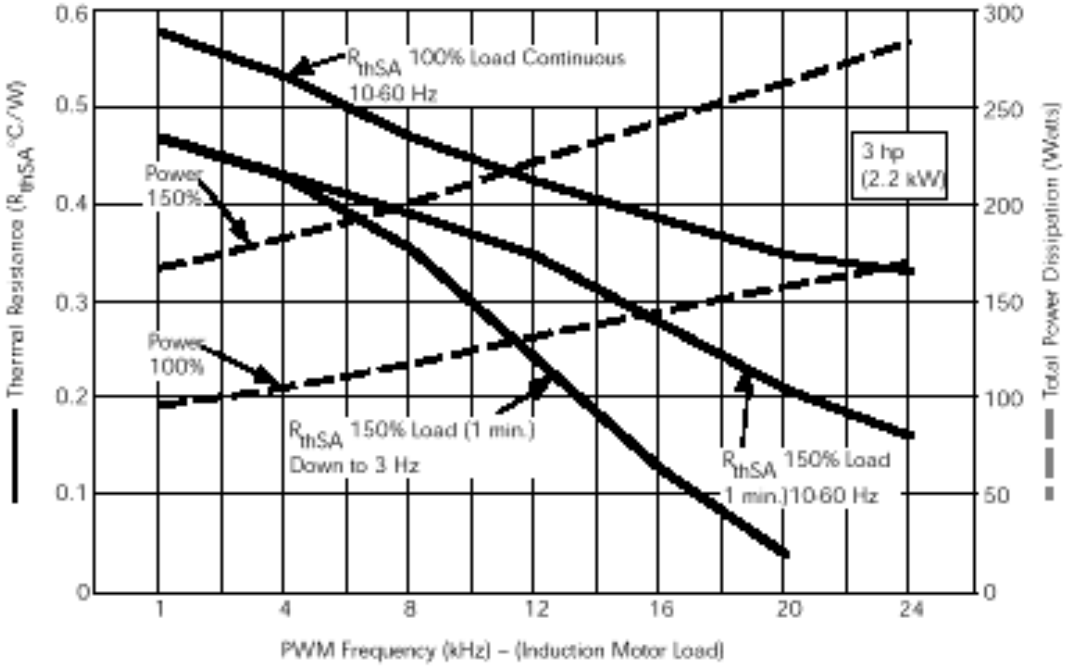


Figure 4a. 3hp/11A output Heat Sink Thermal Resistance and Power Dissipation vs. PWM Frequency

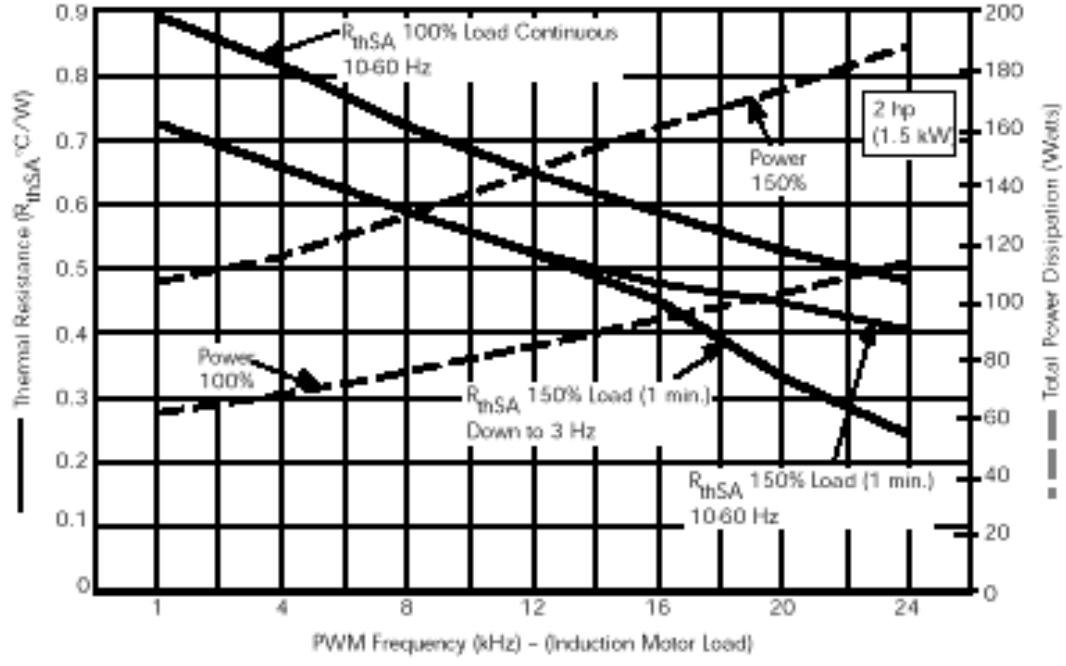


Figure 4b. 2hp/8A output Heat Sink Thermal Resistance and Power Dissipation vs. PWM Frequency

NOTE: For Figures 4a and 4b: Operating Conditions: V_{ll} = 230V_{rms}, MI = 1.15, PF = 0.8, TA = 40°C, Tj < 145°C, Ts < 95°C, Z_{thSA} limits ΔT_j during 1 minute overload to 10°C

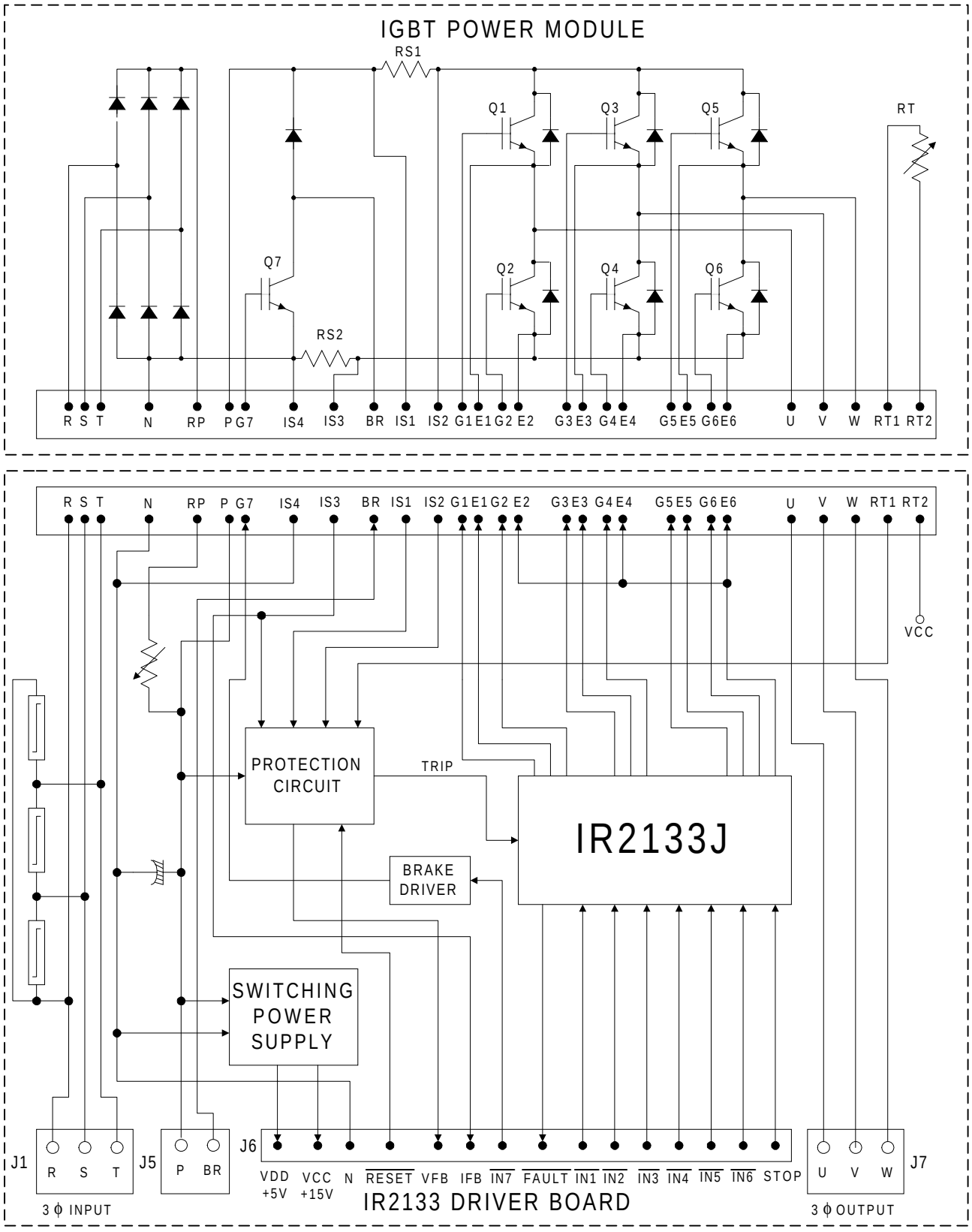

IGBT POWER MODULE
RS1
Q1
Q3
Q5
RT
Q7
Q2
Q4
Q6
RS2
R S T N RP P G7 IS4 IS3 BR IS1 IS2 G1 E1 G2 E2 G3 E3 G4 E4 G5 E5 G6 E6 U V W RT1 RT2
VCC
PROTECTION CIRCUIT
TRIP
IR2133J
BRAKE DRIVER
SWITCHING POWER SUPPLY
J1
R S T
3 ϕ INPUT
J5
P BR
J6
VDD +5V
VCC +15V
N
RESET VFB IFB IN7 FAULT IN1 IN2 IN3 IN4 IN5 IN6 STOP
IR2133 DRIVER BOARD
J7
U V W
3 ϕ OUTPUT

Figure 9: Technical Specifications @ Tc=25C Unless Stated Otherwise

Parameter	Value	Condition
POWER INPUTS		
Voltage	230Vrms - 20% + 10%	
Frequency	50 / 60 Hz	
Current	15.4Arms @ Nominal Full Load Surge Max: 150A Peak	Ta=40C, RthSA= 0.42C / Watt
Line Impedance	4% to 8% Recommended	Line Reactor Required for Source Input Impedance <4%
POWER OUTPUTS		
Voltage	0-230Vrms	
Power	3HP (2.2KW) Nominal Power 150% Overload for 1 Minute	Vin=230VAC, Fpwm=4KHz, Fo=60Hz, Ta=40C, RthSA=0.42C / Watt ZthSA Limits Temp Rise During Overload
Current	11Arms Nominal, 16.5Arms Overload	
Brake Output BR to P (J5)	20A	Max Current
CONTROL INPUTS		
/In1../In7,/Reset	5V Maximum (Active Low)	CMOS, LSTTL or Open Collector Compatible
Stop	5V Maximum (Active High)	CMOS, LSTTL
Deadtime	0.2uSec Minimum	See IR2133 Data
Minimum Input Pulse Width	1.0 uSec	Limited only by Bootstrap Capacitor. See Design Tip 98-2
PROTECTION		
Output Current Trip Level	50A Peak +/- 10%	
Ground Fault Trip Level	66A Peak +/- 10%	
Over-Temperature Trip	100C +/- 5%	Case Temperature
Over-Voltage Trip	425V +/- 10%	Maximum Persistance 30Sec
Maximum DC Link Voltage	400V	Maximium Persistance 30Sec
Minimum DC Link Voltage	150V	To Maintain Auxilliary Supply
Short Circuit Response Time	2.5Usec	Line to Line or Line to Bus
FEEDBACK		
Current (Ifb)	0.025V/Abus Typical	
Bus Voltage (Vfb)	0.014V/Vbus Typical	
Fault Feedback (/Fault)	5V Maximum (Active Low)	CMOS or LSTTL Compatible
AUXILLIARY SUPPLY		
Vcc	15V +/- 10%	
Vdd	5V +/- 5%	
Icc+Idd	60mA	Available to User
POWER MODULE		
Isolation Voltage	2500VAC 60Hz for 1 Minute	Pin to Baseplate Isolation
Operating Case Temp	-20C to +95C	95% RH Max (Non Condensing)
Mounting Torque	1 Newton Metre	M4 Screw
SYSTEM ENVIRONMENT		
Ambient Operating Temp	0 to 40C Recommended With Heatsink	95% RH Max (Non Condensing)

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Reference Design Data Sheet (October 1998)

IRMDAC2

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IR2233 Reference Design Kit: 3-Phase 460VAC 3HP Motor Drive

Product Description

The IRMDAC3 Reference Design is a kit of parts that work together as an evaluation platform for IR2233 three phase motor control IC and IRPT2062A power module. User connects three phase AC, drive signals, motor and hall sensors to complete the system. Power hook-up is via terminal blocks and control signals are made using a single in line header.

How the IR2233 Control IC Adds Value

- Monolithic HVIC Integrates Control and Drive Yields Compact, Robust, Economical Designs
- Allows Elegant, Convenient System Partition
- Compatible with Short Circuit, Ground Fault and Over-Temperature Protection Schemes

How the Power Module Adds Value

Integration of All Inverter Power Components;

- Low Parasitic Coupling = High Performance
- Current Sensing Shunts in DC Feed and Return
- Onboard Temperature Sensor
- Easily Mounted Package
- Short Circuit Rated, Ultrafast IGBT Gen #4
- Wide Operating Temperature Range
- Metal Base gives Excellent Thermal Transfer and Isolation to 2500V RMS

System Block Diagram *Fig 2*

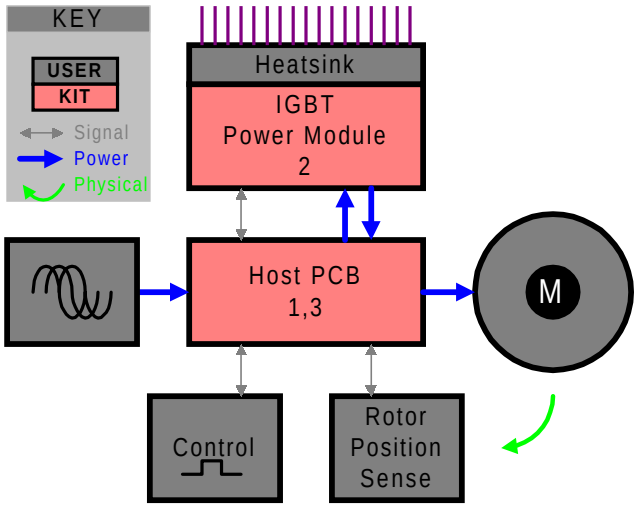
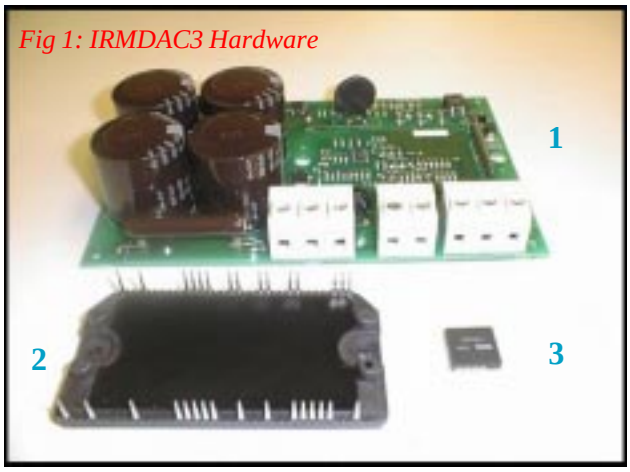


Fig 1: IRMDAC3 Hardware



Kit Content

1 Host PCB for Input Processing and Control
2 IRPT2062A Integrated Power Module
3 IR2233 Three Phase Motor Control IC
Technical Contact and License Detail
Schematic and PCB Layout Data
Bill of Materials and Supplier Information

System Features

- 460V Three Phase AC Inlet, 50/60Hz
- Convenient Signal and Power Terminations
- Inrush Current Limit and Surge Suppression
- Integral +15V and +5V Bias Supplies
- DC Bus Voltage and Current Feedback
- 150% Overload Capability (1 Minute)
- Optimized Drive for Power Module
- Includes **Brake Switch** and Drive

Fig 3

IRMDAC3 Host PCB Bottom Layer



IRMDAC3 Kit Overview and System Benefits

- When furnished with user-provided logic level control signals, the IRMDAC3 forms a complete reference design for a 3HP AC motor. Unlike outdated circuits based upon transformer drive or opto-couplers, the system uses International Rectifier proprietary level-shifting gate drive circuits integrated within the IR2233J Control IC. Separation of gate drive / control and low-voltage circuits from the power module included in the kit results in a compact, effecient system. The user benfits from immediate hands-on experience and may customize at will using shematics and circuit ideas as the basis for production designs.

- Gate drive, control and protection circuits are designed to closely match the operating characteristics of the power semiconductors. This allows power losses to be minimized and power rating to be enhanced to a greater extent than is possible by designing with individual components.

1. Host PCB Description

The host PCB receives power input from a 3-phase line and control signals provided by the user. In conjuntion with the power module the result is a flexible power conversion system, primarily designed for interface with a 3HP Motor, however other 3-phase loads may also be applied. The host PCB supports soft-start function which reduces inrush current by using an NTC thermistor. Surge suppression is implemented using MOV's as a further degree of protection. Also on-board is a regulated low voltage power supply to provide bias for the IR2233J and other low voltage components. When connected to the power module, the unit is fully protected against overcurrent and ground faults through DC bus voltage and current feedback. Over-temperature is guarded against through feedback from a thermistor embedded within the power module. A 16-pin single in line header connector is provided to interface control signals and two terminal blocks connect 3-phase AC inlet and output to the load. The user provides 5V CMOS / TTL level signals which are then processed by the IR2233J Control IC and delivered to the power module.

Signals Available to User

In addition to availability of bias supplies derived for the host PCB, signals from the power module circuits and those derived and processed on the host PCB such as fault status are available to the user. Current feedback signal from the low side shunt is available on the IFB pin at 0.025V/A. If filtering of this signal is required to remove noise, a high impedance buffer stage should be inserted between signal and filter. DC bus voltage feedback is provided on the VFB pin. This reference is been scaled down by a factor of 100 and should be protected with a high impedance buffer stage.

Fault Behavior.

The system is designed to tolerate overload conditions for one minute. The user should prevent such conditions persisting beyond this period. In the event of shutdown initiated by ground-fault, overcurrent or over-temperature, the inverter outputs are terminated and an LED will light to signal this condition. For more information on fault response for IR2233J, please consult the data sheet.

Brake Function

In order to use the integrated brake switch, an external power resistor should be connected between pins BR and P of terminal block J5. This resistor should be dimensioned for desired braking performance. Carefully choose the value of this component to ensure the brake IGBT integrated within the power module remains below its maximum current capability.

2. Power Module Description

The power module integrates all rectifiers, ultra-fast short circuit rated IGBTs, fast recovery commutation diodes , brake IGBT and other processing components needed for a 3HP Motor Drive or other loads requiring a 3-phase variable frequency and/or PWM drive. Semiconductor dice are mounted on a thermally effecient substrate and housed within a convenient, potted module. When connected to the host PCB, the power components become configured as a 3-phase input bridge rectifier, and IGBT inverter with current sensing shunt resistors. An NTC thermistor is bonded to the substrate to furnish the host PCB with accurate temperature reading. A galvanically isolated metal backplate provides excellent thermal coupling to an external heatsink, which is necessary for full-load operation.

Circuit Layout within the module is carefully designed to minimize inductance in the power path, reduce noise during inverter operation and to improve inverter efficiency. The IR2233 host board should be soldered to the power module pins to complete the assembly. For detailed electrical specifications, please refer to the power module datasheet.

Power Module Mounting and Hook-up Instructions

1. Remove all particles and grit from the heatsink and power substrate
2. Spread a thin layer of silicone grease on the heatsink, covering the entire area that the power substrate will occupy
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Upon application of 3-phase input power, PWM inputs must be held high until the protection latch circuitry is reset. To reset this latch before inverter start-up, RESET pin on J6 connector must be pulled down low for at least 2usec. This will set the Fault feedback signal on J6 high. PWM input signals may then be actively driven.

Figure 4 Signal Connector

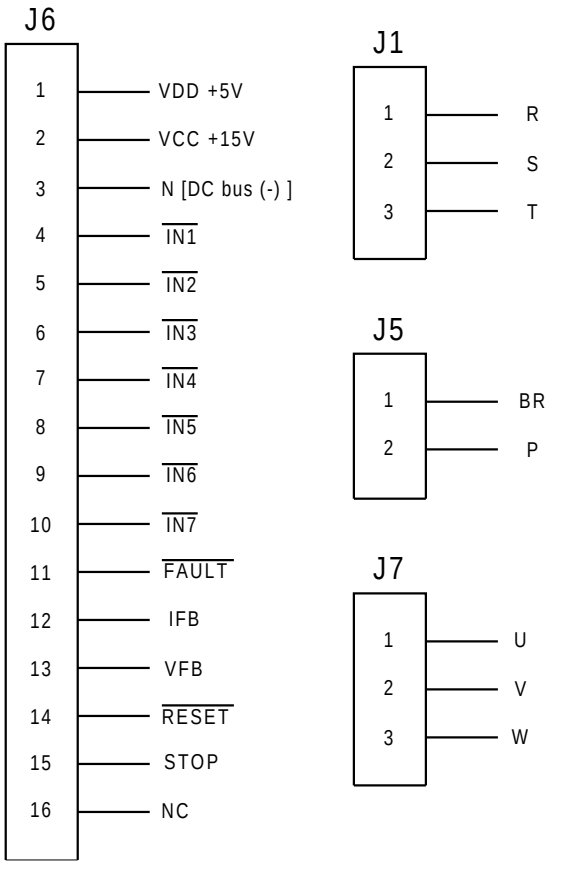
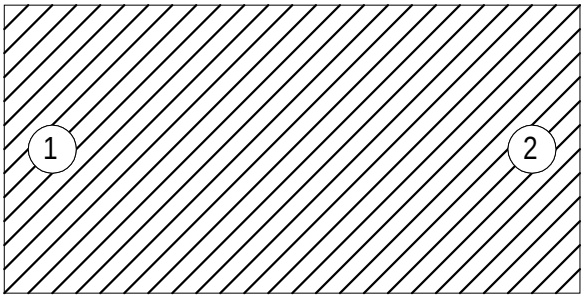


Figure 5 Power Terminal Blocks

Figure 6 Power Module Mounting Screw Sequence



Mechanical Details

Figure 7

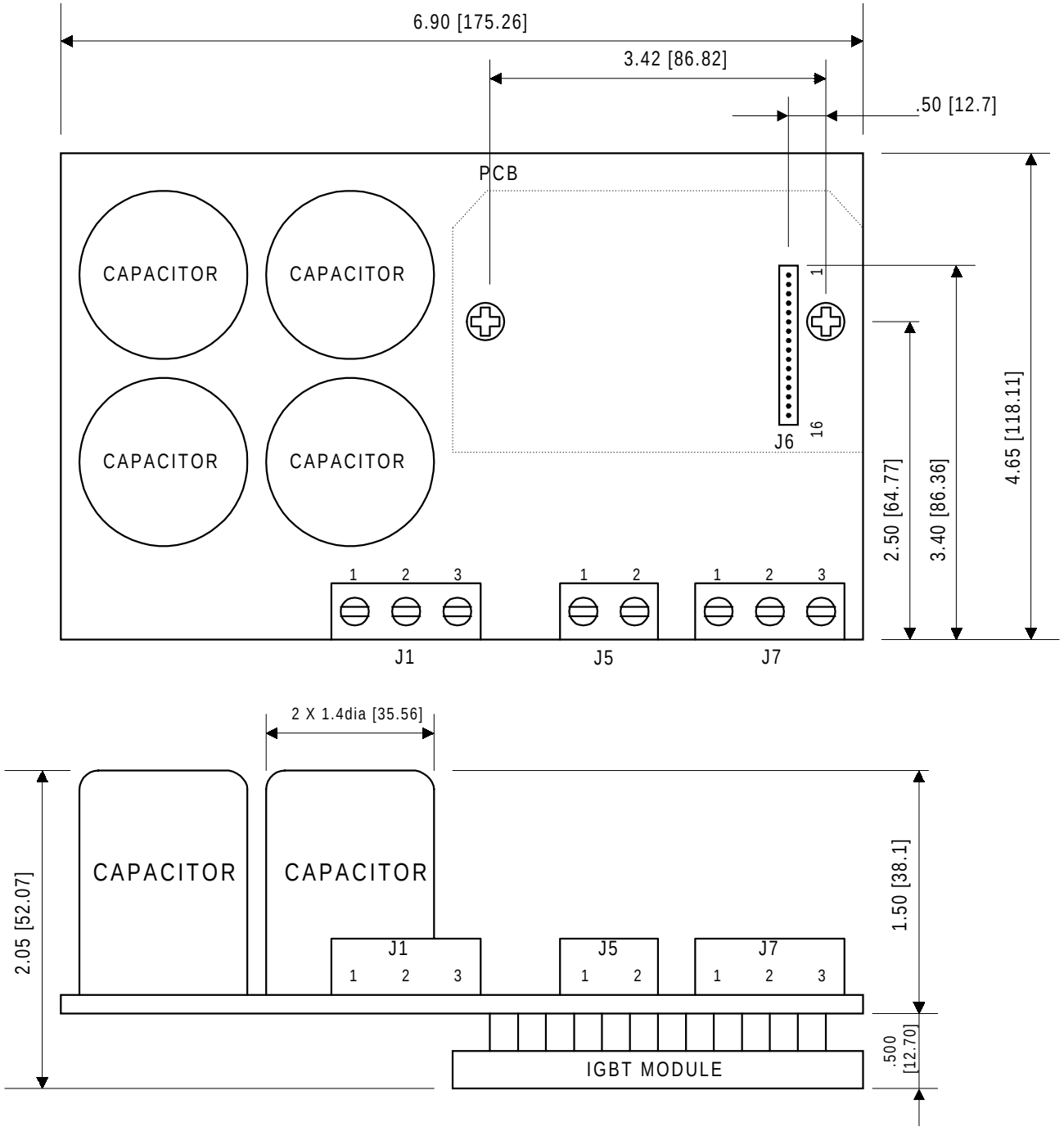


Figure 8: Effeciency Maximization Charts Extract From Module Data Sheet

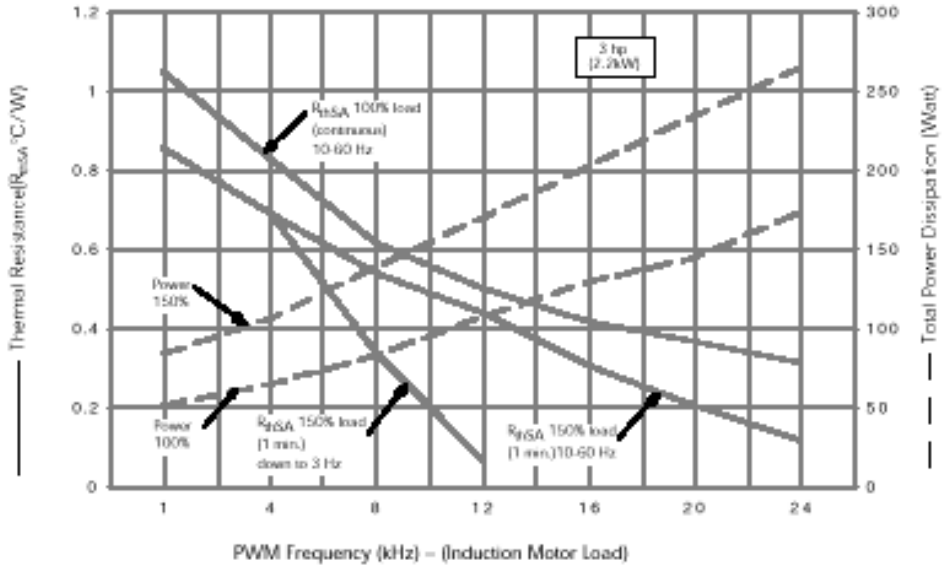


Figure 4a. 3 hp/5.9A Output Heat Sink Thermal Resistance and Power Dissipation vs. PWM Frequency

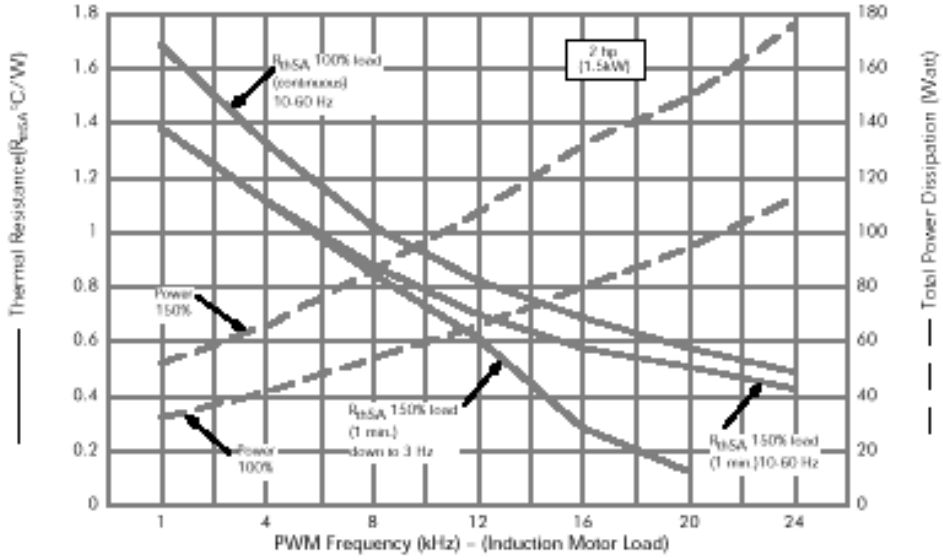


Figure 4b. 2 hp/4.2A Output Heat Sink Thermal Resistance and Power Dissipation vs. PWM Frequency

NOTE: For figures 4a and 4b: Operating Conditions: V_{ac} = 460V_{rms}, MI = 1.15, PF = 0.8, T_A = 40°C, T_j < 145°C, T_S < 95°C, Z_{thSA} limits ΔT_c during 1 minute overload to 10°C

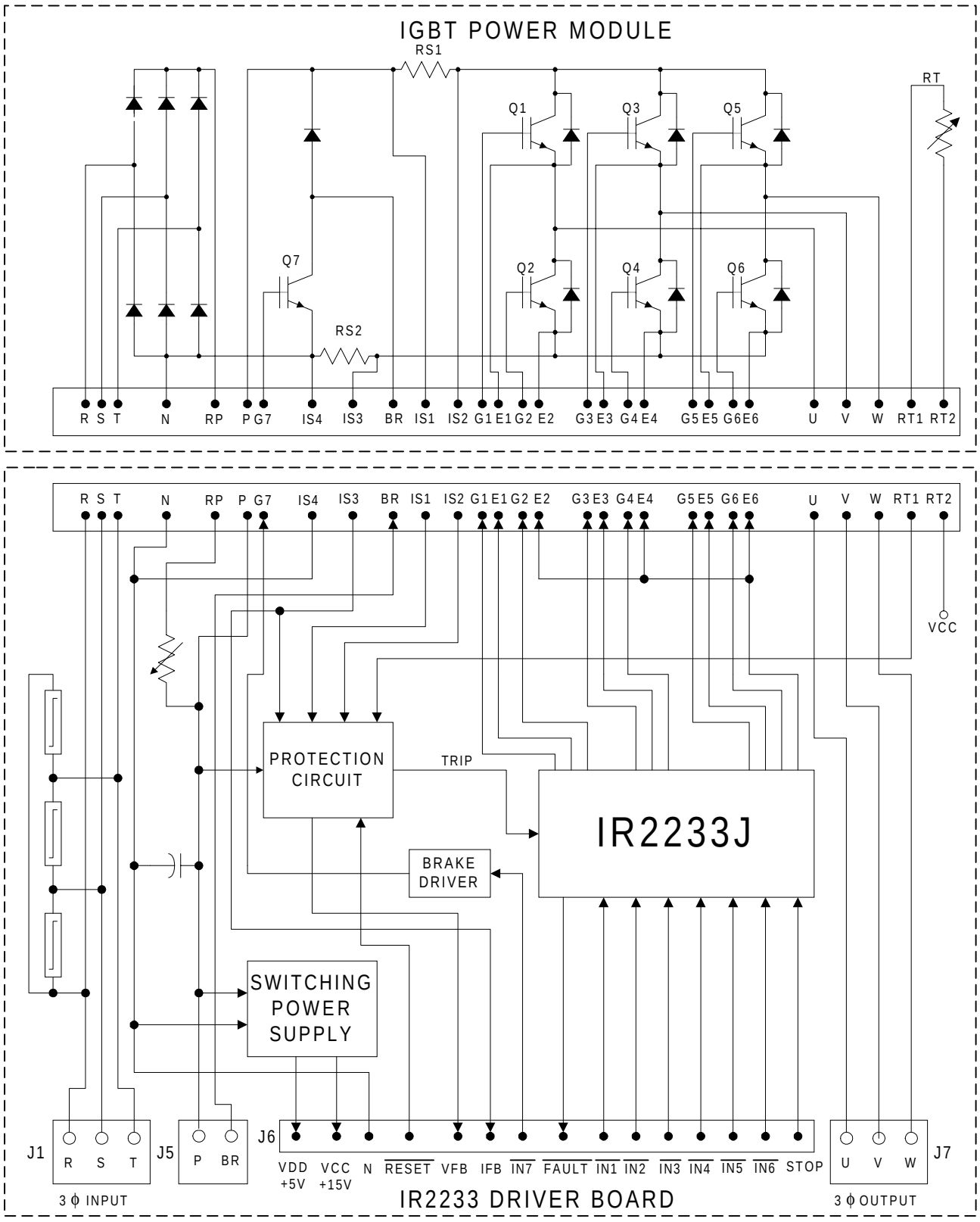

IGBT POWER MODULE
RS1
RT
Q1
Q3
Q5
Q7
Q2
Q4
Q6
RS2
R S T N RP P G7 IS4 IS3 BR IS1 IS2 G1 E1 G2 E2 G3 E3 G4 E4 G5 E5 G6 E6 U V W RT1 RT2
VCC
PROTECTION CIRCUIT
TRIP
IR2233J
BRAKE DRIVER
SWITCHING POWER SUPPLY
J1
R S T
3 ϕ INPUT
J5
P BR
J6
VDD +5V
VCC +15V
N
RESET
VFB
IFB
IN7
FAULT
IN1
IN2
IN3
IN4
IN5
IN6
STOP
IR2233 DRIVER BOARD
J7
U V W
3 ϕ OUTPUT

Figure 9: Technical Specifications @ Tc=25C Unless Stated Otherwise

Parameter	Value	Condition
POWER INPUTS		
Voltage	460Vrms- 20% + 10%	
Frequency	50 / 60 Hz	
Current	8.26A RMS @ Nominal Full Load Surge Max: 150A Peak	Ta=40C, RthSA= 0.42C / Watt
Line Impedance	4% to 8% Recommended	Line Reactor Required for Source Input Impedance <4%
POWER OUTPUTS		
Voltage	0-460Vrms	
Power	3HP (2.2KW) Nominal Power 150% Overload for 1 Minute	Vin=460VAC, Fpwm=4KHz, Fo=60Hz, Ta=40C, RthSA=0.42C / Watt ZthSA Limits Temp Rise During Overload
Current	5.9Arms Nominal, 8.85Arms Overload	
Brake	10.5A	Maximum Current
CONTROL INPUTS		
/In1../In7,/Reset	5V Maximum (Active Low)	CMOS, LSTTL or Open Collector Compatible
Stop	5V Maximum (Active High)	CMOS, LSTTL
Deadtime	0.2uSec Minimum	See IR2233 Data
Minimum Input Pulse Width	1.0 uSec	Limited only by Bootstrap Capacitor. See Design Tip 98-2
PROTECTION		
Output Current Trip Level	28A Peak +/- 10%	
Ground Fault Trip Level	50A Peak +/- 10%	
Over-Temperature Trip	100C +/- 5%	Case Temperature
Over-Voltage Trip Level	850V +/- 10%	Maximium Persistance 30Sec
Maximum DC Link Voltage	800V	Maximium Persistance 30Sec
Minimum DC Link Voltage	150V	To Maintain Auxilliary Supply
Short Circuit Response Time	2.5Usec	Line to Line or Line to Bus
FEEDBACK		
Current (Ifb)	0.025V/Abus Typical	
Bus Voltage (Vfb)	0.010V/Vbus Typical	
Fault Feedback (/Fault)	5V Maximum (Active Low)	CMOS or LSTTL Compatible
AUXILLIARY SUPPLY		
Vcc	15V +/- 10%	
Vdd	5V +/- 5%	
Icc+Idd	60mA	Available to User
POWER MODULE		
Isolation Voltage	2500VAC 60Hz for 1 Minute	Pin to Baseplate Isolation
Operating Case Temp	-20C to +95C	95% RH Max (Non Condensing)
Mounting Torque	1 Newton Metre	M4 Screw
SYSTEM ENVIRONMENT		
Ambient Operating Temp	0 to 40C Recommended With Heatsink	95% RH Max (Non Condensing)

International
IOR Rectifier

Reference Design Data Sheet (October 1998)

IRMDAC3

International
IOR Rectifier

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IR2137/IR2171 Reference Design Kit
For 3-phase/230V 3HP AC Motor Drives

IR2137/IR2171 Power Board

- 230V AC input / 2.2kW output
- IR2137Q monolithic 3-phase HVIC driver.
- IR2171S monolithic linear current sensing IC
- DC bus capacitor with NTC inrush current limiter.
- On-board +15V and 2 X +5V power supply.
- Linear Motor Phase Current Feedback.
- DC bus voltage and current feedback.
- Full protection for short circuit, earth/ground fault and over-temperature.
- Optically isolated PWM gate/Fault signals.
- Terminal blocks for 3-phase input/output connec tions.

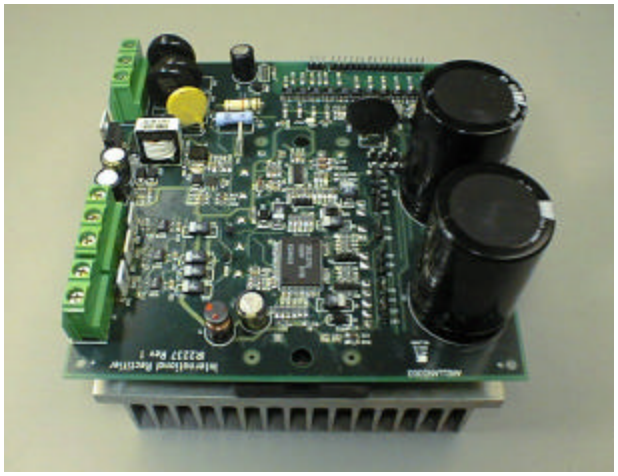


Figure 1 IRMDAC4 IR2137/IR2171 Reference Design Kit (Shown with Optional Heatsink and IGBT Power Module)

Power Module

- Standard EconoPIM2 IGBT module.
- 600V/30A short circuit rated IGBT.
- 600V/20A short circuit rated BRAKE IGBT.
- 800V/30A 3-phase rectifier bridge.
- Built-in Temperature sensor.
- Pin-to-base plate isolation 2500VAC rms.
- Easy-to-mount two screw package.

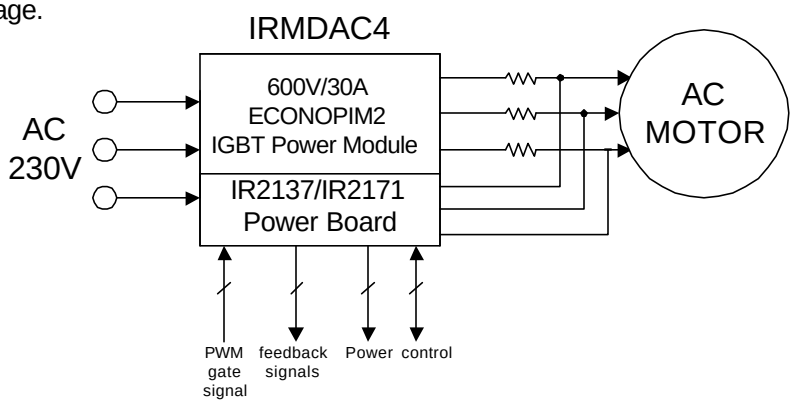


Figure 2 Typical Connection Diagram

System Description

The IRMDAC4 is the AC motor reference design kit for the IR2137Q 3-phase gate driver IC and the IR2171 current Sensing IC. It is the power conversion unit for a 3-phase/230V 3HP (2.2kW) AC PWM (Pulse Width Modulated) drives. This design kit consists of the IR2137/IR2171 power board based on 4-layer PCB. The ECONOPIM2 power module and the heat sink are supplied separately. User must provide soldering connection between the power board and the power module, and the appropriate heat sink to complete the power conversion function.

Figure 1 shows the complete assembly of the IRMDAC4 Reference Design Kit. Figure 2 illustrates the typical connection block diagram of the IRMDAC4.

The IR2137/IR2171 power board contains an IR2137Q gate driver High Voltage IC, DC link capacitors, soft start function using NTC thermistor, AC input MOVs for surge suppression, switching power supply, brake IGBT buffering circuit, over-current/ground fault/over-temperature protection circuit, DC bus voltage and current feedback signals. On-board 16-pin single row header connector (J9) is provided to interface the control signals, and two terminal blocks are provided to facilitate connection to 3-phase AC input (J7) and output (J6).

The power module contains a 3-phase input bridge rectifier, 3-phase IGBT inverter; brake IGBT/diode, and the temperature thermistor on the substrate base. It is designed for easy mounting to a heat sink.

Output power is PWM 3-phase, variable frequency and voltage controlled by a user provided 5V PWM signal input. The limited amount of the power is available for two 5VDC (one ground isolated and one non-isolated), and 15VDC non-isolated to facilitate the PWM interface. The non-isolated powers are referenced to the negative DC bus that the IR2137Q gate driver IC is also referenced to.

The IRMDAC4 offers several benefits to the users listed below:

- It gives a complete working reference of the 3HP AC drive power conversion based on the state-of-art 3-phase gate driver and IGBT power module. User can gain immediate hands-on experience based on the system. The design detail can be further utilized in the area of: PCB layout, gate drive optimization, protection circuit, and on-board switching power supply.
- Gate drive and protection circuits are designed to closely match the operating characteristics of the power semiconductors. This allows power losses to be minimized and power rating to be maximized to a greater extent than is possible by designing with individual components.
- It reduces the effort of calculating and evaluating power semiconductor losses and junction temperature.

IR2137 Driver Board

The IR2137/IR2171 power board also contains the feedback signal circuit, brake driver, soft start circuit, and the local switching power supply. The driver also interfaces to the AC input line. It houses the DC link capacitors, current sensing shunt resistor, NTC in-rush limiting thermistor, and surge suppression MOVs.

The inverter **gate drive circuits**, implemented with an IR2137Q monolithic 3-phase HVIC driver, delivers gate drive to the IGBTs corresponding to PWM control signals $\overline{\text{HIN1}}$ through $\overline{\text{HIN3}}$, and $\overline{\text{LIN1}}$ through $\overline{\text{LIN3}}$ into J9 connector. It introduces a 0.2µsec deadtime between upper and lower gate signals for each phase. Any additional deadtime necessary to expand must be included in the PWM signals. Gate drives must be enabled with an active low pulse applied to the $\overline{\text{RESET}}$ pin into J9 pin 14 while PWM inputs $\overline{\text{HIN1}}$ through $\overline{\text{HIN3}}$, and $\overline{\text{LIN1}}$ through $\overline{\text{LIN3}}$ are held high (off condition).

After power up, the $\overline{\text{RESET}}$ pin must be pulled low before any input signals are activated.

The **protection circuitry** of the system is incorporated by two means: One is by the function of the high side de-saturation protection input (DESAT) in the IR2137Q IC, and the other is by the comparator circuit and current sensing shunt resistor (R44) for the low side gate driver that enables the ITRIP input of the IR2137Q device. The internal fault logic of the IR2137Q will enable the $\overline{\text{FAULT}}$ output in an event of a short circuit, earth/ground fault, over-temperature, or over-voltage/ over-current conditions with Soft Shutdown, as specified. Over-current signals are sensed through shunt resistors located in the negative DC bus rail. Earth/ ground faults are sensed using the high side shunt resistor and the signal is level shifted through the opto-isolator to the protection circuitry. Over-temperature protection is obtained using a thermistor inside the

power module. A $\overline{\text{FAULT}}$ condition occurs when the temperature of the power module substrate exceeds 110°C. After a fault condition all inverter gate drivers are disabled and latched, which illuminates the on-board red LED. The resulting $\overline{\text{FAULT}}$ signal can be monitored at pin 1 of J9.

Like all logic inputs for high/low side gate driver outputs (J9 pins 1 through 6), the $\overline{\text{SD}}$ input is fed through an opto-isolator and into the IR2137Q device and must be an active high input signal at the input of the opto-isolator. When $\overline{\text{SD}}$ is active low, all output drivers will simultaneously shut down without being latched (real time). Furthermore, in a soft shutdown scheme, simultaneous shutdown of all 6 IGBTs is required to prevent a potential false turn-on while the IGBTs are in the soft shutdown mode. The system is designed for 150% overload for one minute while operating with the specified heatsink. The controller should shut off the PWM signals if the overload condition persists over one minute.

Current sensing is implemented via 0.01Ω current sensing shunt resistors in series with each of the 3ϕ output lines at J6, and decoupled with 1000PF capacitors in parallel with each shunt resistor. Each pair of the shunt resistors is tied into the inputs of the linear current sensing IC, IR2171. The output of each IR2171 device is fed into an opto-isolator. The output of each opto-isolator is routed to pins 11, 12 and 13 of connector J9, current sensing outputs. When over-current occurs, the PWM output (PO) of IR2171 goes low and initiates the opto-isolator that flags a signal at the current sense output at J9. In addition, the dedicated over-current trip (OC) output of the IR2171 initiates a signal into the opto-isolator, which in turn, flags a signal at J9 pin 3 (Ocrt/s). Output $\overline{\text{OC}}$ is a negative logic output signal that facilitates IGBT short circuit protection.

The **brake function** is implemented by connecting a power resistor between the terminals on the Brake terminal block. The external power resistor will determine the maximum braking capability in conjunction with the drives regenerative power. The value of resistor should be carefully chosen not to exceed the maximum current handled by the brake IGBT. The input signal on the $\overline{\text{BRAKE}}$ pin of J9 pin 14 is active low and CMOS or LSTTL compatible. The $\overline{\text{BRAKE}}$ input is permanently pulled high to +5V V_{DD} via a 10KΩ resistor to ensure CMOS or LSTTL compatibility.

The **switching power supply** employs a UC2844AD8 current mode PWM controller and self-oscillating driver chip to deliver a nominal 5V and 15V DC through a line isolation transformer with respect to the negative DC bus. The power supply feeds the gate drive and protection circuits. At an input voltage of 230VAC the PWM Carrier Frequency is 8kHz and the output Frequency is 60Hz. The minimum and maximum required DC Bus Voltage are 90V and 400V, respectively. The 15V (V_{CC}) and 5V (V_{DD}) outputs are available on the interface pins for the external control logic circuit.

As part of the switching power supply, a +5V isolated (floating) power supply is available for powering most opto-isolators and isolating all opto-isolator's ground from the COM pin of the IR2137Q IC. The isolated +5V supply can be monitored at J9 pin 2 (VC_ISO) with reference to the isolated supply ground, J9 pin 16 (GNDISO).

The ECONOPIM2 Power Module

The ECONOPIM2 Power Module is an IGBT power Module based on Direct Bonded Copper substrate (DBC). It houses input rectifiers, output inverter, brake IGBT/diode, and a thermistor. The 3-phaseinput bridge rectifiers are rated 600V/30A. The inverter section employs 600V, short circuit rated, ultrafast IGBTs and ultrafast freewheeling diodes. The internal thermistor provides temperature-sensing capability.

The power circuit and layout within the module are carefully designed to minimize inductance in the power path, to reduce noise during inverter operation and to improve the inverter efficiency. The IR2137/IR2171 driver board required to run the inverter can be soldered to the power module pins, this minimizing assembly and alignment. The power module is designed to mount on a heatsink with two screw mount positions, in order to insure good thermal contact between the module substrate and the heatsink.

For detailed electrical specifications, please refer to each power module data sheet.

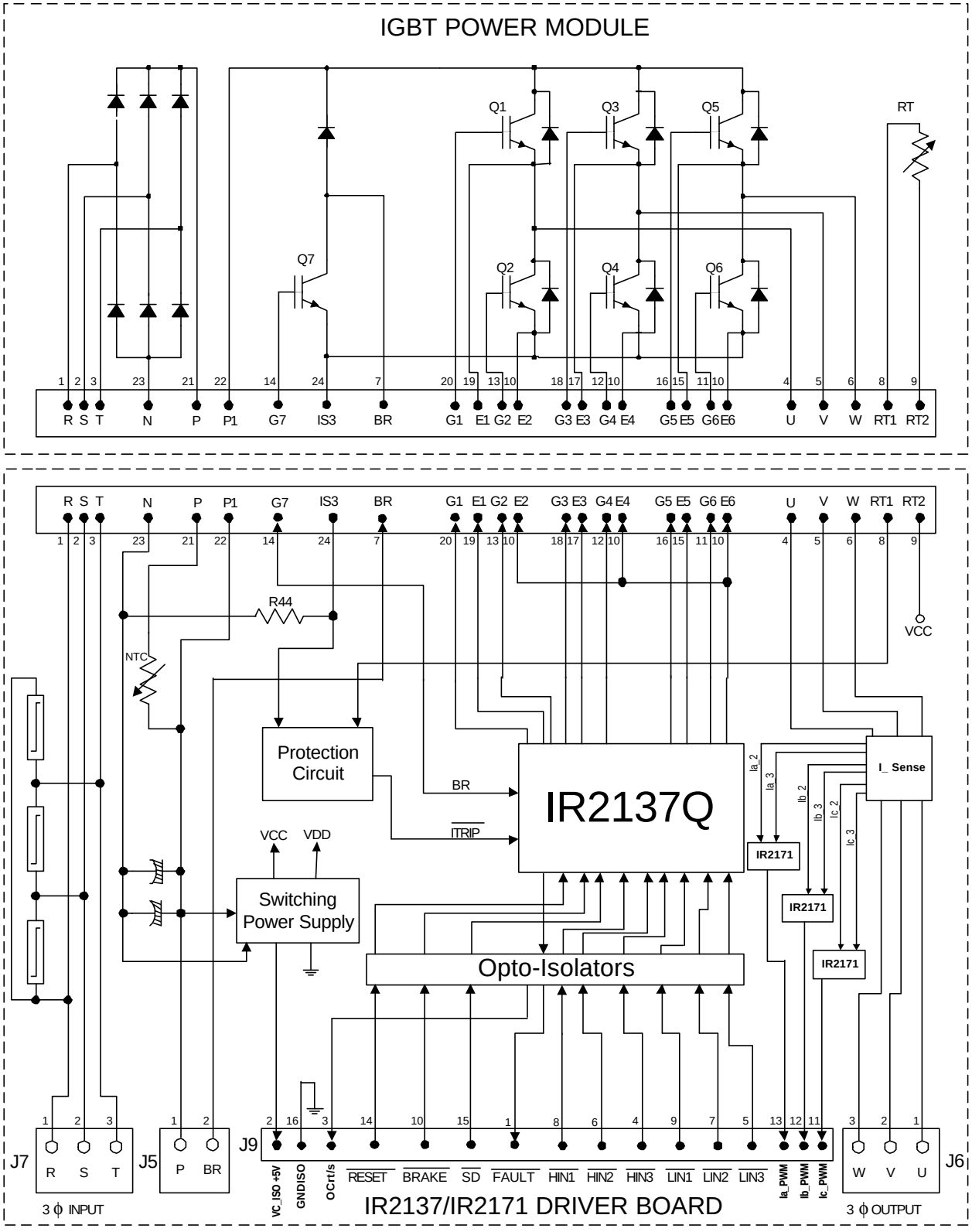


Figure 3 IRMDAC4 Block Diagram

Specifications Tc = 25°C unless otherwise specified

Parameters	Values	Conditions
Input Power		
Voltage	115 - 230V, -20%, +10%	Output Power Rating is half at 115VAC Input
Frequency	50/60Hz	
Input current	15.4A rms (Continuous) 150A (Peak Inrush Current)	Ambient Temperature, TA=40°C Heat Sink RthSA=0.35°C/W
Input line impedance	4%~8% recommended	
Output Power		
Voltage	0-230V rms	
HP	3HP (2.2kW) nominal power 150% overload for 1 minute	Input Voltage=230V AC, PWM Carrier Frequency=8kHz, Output Frequency=60Hz, Ambient Temperature=40°C, Heatsink Rth=0.35°C/W
Current	11Arms Continuous, 16.5Arms Overload	
Control Inputs		
$\overline{IN1}$, $\overline{IN2}$, $\overline{IN3}$, $\overline{LN1}$, $\overline{LN2}$, $\overline{LN3}$	10mA Source Current	Primary PWM input of Opto-coupler
$\overline{RESET}$, $\overline{SD}$, $\overline{BR}$	10mA Sink Current	Primary PWM input of Opto-coupler
$\overline{FAULT}$, IA, IB, IC, $\overline{OC}$	Open Drain Output	Output of out-coupler (1.2kΩ pull-up)
IA, IB, IC (Current Feedback)	40kHz Digital PWM Output	Motor Current
Deadtime	Minimum 700nsec required	Internal 0.2µsec provided by IR2137
Protection		
Line-to Line short	87A peak, ±30%, Response time = 2.5µsec (typical)	IR2137 Internal Function
Ground fault	100A peak, ±30%	IR2137 Internal Function
Over Temperature	110°C, ±10%	IGBT Module Substrate Temperature
DC Bus Voltage		
Maximum	400V	
Minimum	90V	
Power Supply		
V_{CC1}	15V, ±10%, 130mA	
V_{DD2}	5V, ±5%, 100mA	For Isolate Primary Circuit of OptoCoupler
V_{DD1}	5V, ±5%, 120mA	
Minimum Operating Voltage	90V	AC Input Voltage Greater than 70V
Brake IGBT		
Current	20A Peak	
HeatSink		
Thermal Resistance	Less than 0.35°C/W	3HP Continuous Output, fc = 8kHz
Ambient Temperature		
Heatsink Temperature	Maximum 80°C	
Humidity	Maximum 95%	No Condensing

Mounting, Hookup and Application Instructions

1. Remove all particles and grit from the heatsink and power substrate
2. Spread a .004" to .005" layer of silicone grease on the heatsink, covering the entire area that the power substrate will occupy Recommended heatsink flatness is .001inch/inch and Total Indicator Readout (TIR) of .003 inch below substrate
3. Place the power substrate onto the heatsink with the mounting holes aligned and press it firmly into the silicone grease
4. Place the 2XM4 mounting screws through the PCB and power module and into the heatsink and tighten the screws to 1NM torque

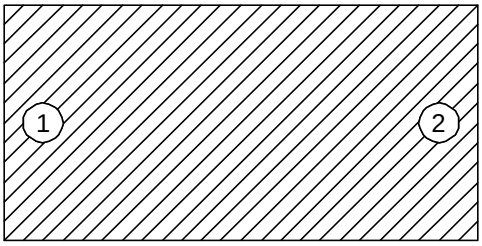


Figure 4 Power Module Mounting Screw Sequence

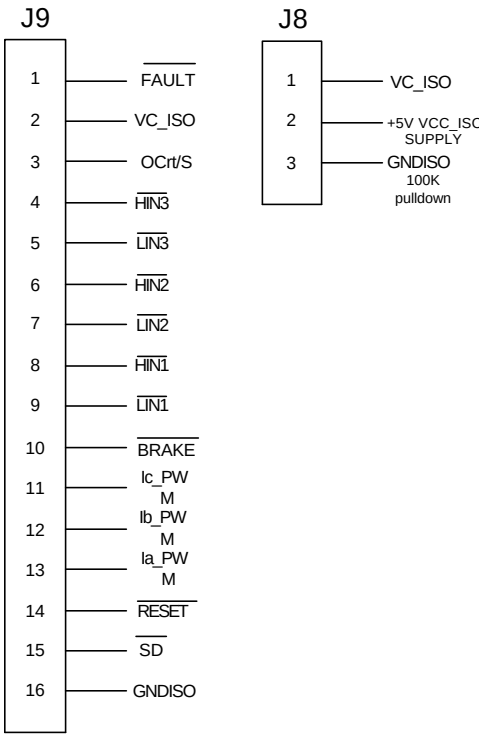


Figure 5 Control Signal Connector

All input and output control connections are made via a 16-pin terminal female connector to J9. J8 shown in Figure 5 is the output connector for the +5V Isolation power supply (VCC_ISO). This power supply is mainly used to power all on-board Opto-Isolators where its ground is isolated from the COM pin of the IR2137Q IC. Note that pin 1 of J8 and J9 is physically located adjacent to the connector reference designator.

Power Connections

3-phase input connections are made to terminals R, S and T (J7). Inverter output terminal connections are made t o terminals U, V and W (J6). Positive DC bus and Brake IGBT collector connections are brought out to terminals P (positive) and BR (brake) of J5 connector. An external resistor for braking can be connected across these terminals.

Power-Up Procedure

When 3-phase input power is first switched on, PWM inputs to IRMDAC4 must be inhibited (held high) until the protection latch circuitry is reset. To reset this latch before inverter start-up, RESET pin on J9 connector must be pulled down low for at least 2usec. This will set the Fault feedback signal on J9 high. Now, the PWM input signals can be applied for inverter start-up.

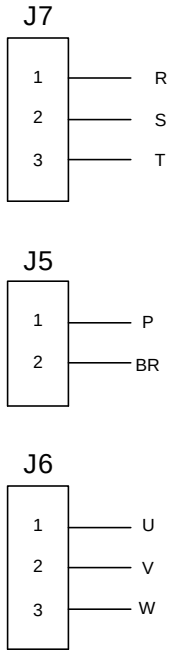


Figure 6 Input and Output Terminal Blocks

IRMDAC4 Mechanical Dimensions

inches [millimeters]

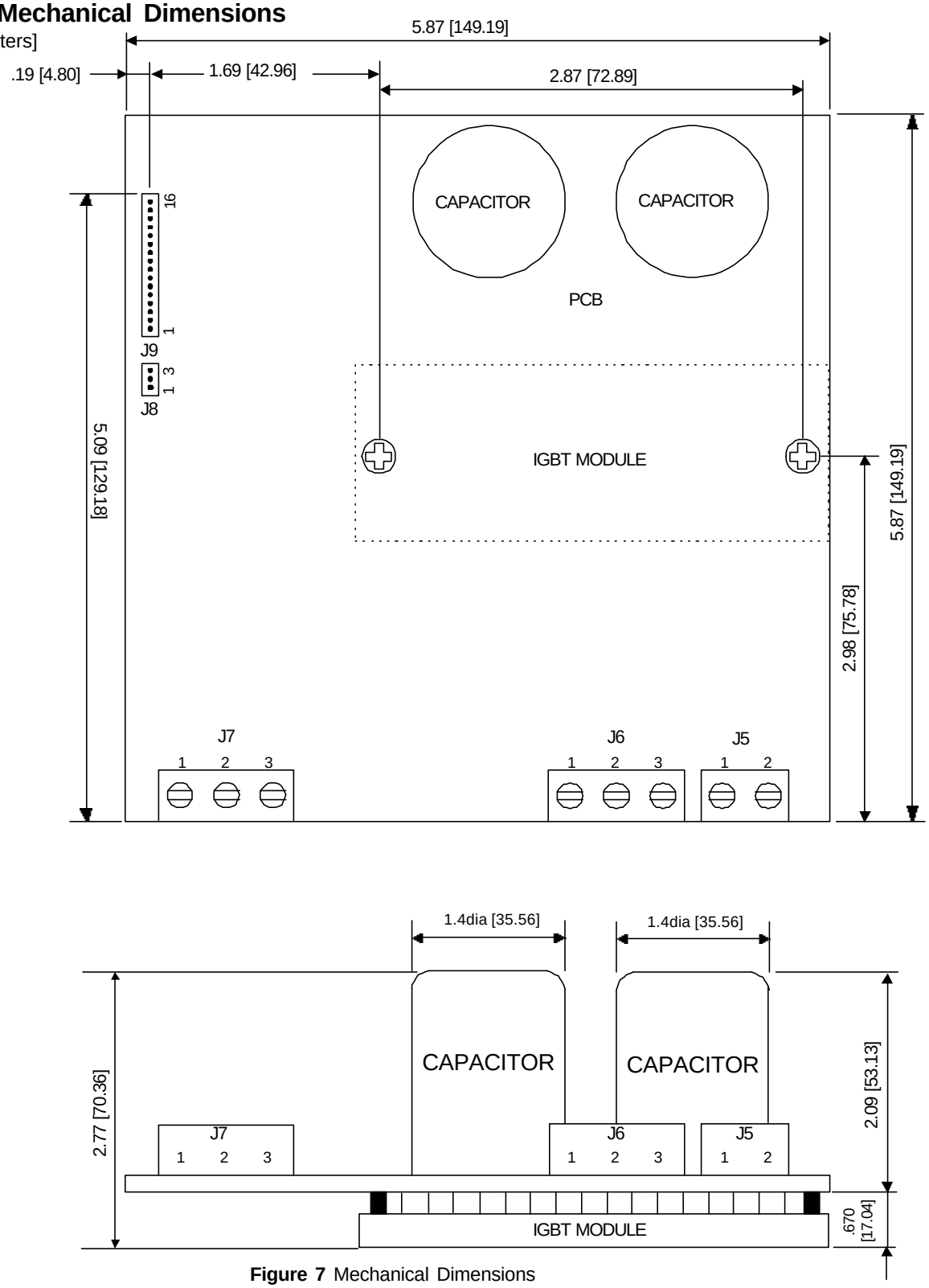


Figure 7 Mechanical Dimensions

POWER CONVERSION PROCESSOR ™ ARCHITECTURE AND HVIC PRODUCTS FOR MOTOR DRIVE

IR's Motor Drive IC family supports the emerging Power Conversion Processor ™ Architecture and delivers new level of ruggedness, compact size and lower EMI. Monolithic integration of high voltage circuits for gate driving with protection, soft start charging of DC bus and linear current sensing of motor phase current enable best in class power conversion platforms. Each new generation of products drives down the price points for high performance control techniques and evolves cost effective motor drive designs from V/Hz to sensor-less vector or servo control.

INTRODUCTION

International Rectifier (IR) has recently expanded their family of 600V and 1200V ICs specifically designed to be used in 115Vac, 230Vac and 460Vac motor drives for industrial and appliance applications. The common theme at the heart of the new products is the Power Conversion Processor ™ Architecture that IR is setting the standard and paving the way for implementation by the industrial and appliance drive companies.

New products in the Industrial Motor Drive IC family include the latest generation of the industry standard three phase gate drivers, the 600V IR2137 and 1200V IR2237, that add integrated protection and soft shutdown for the IGBT inverter stage. Expanding the family, new product category is created for current sensing ICs, 600V IR2171 and 1200V IR2271, that sense motor phase current and convert to digital format to be used in the algorithm for closed loop current control. Another new product category, the soft start converter controller IC, IR1110, is designed to soft charge the DC bus capacitor and provide a bulletproof input converter stage.

New products in the Home Appliance and Light Industrial Drive IC family include the 600V half-bridge gate drivers IR2106/07/08/09, IR21064/74/84/94 and the three-phase gate driver IR2136 and IR21362. These series of new products are simple and low cost. They are especially designed to be used in refrigerator compressor, air-conditioner compressor and direct drive washing machine.

DRIVE FUNCTIONS AND ARCHITECTURES

The power conversion sub-system in AC or BLDC motor drive is commonly partitioned into different functions (Figure 1). Each function serves its unique requirements but also has to couple with each other in order for the complete system to work as a whole. For example the IGBT gate drive and protection functions have to be synchronized and the feedback sensing and the regulator control and PWM have to be matched.

Older types of drive use an architecture that can be called two levels power conversion processing (Figure 2). All the motion profile and power conversion signal processing functions are implemented within an isolated low voltage supply level that is remote from the power level. The power conversion actuation devices, diodes and IGBTs, are contained within the high voltage supply level directly connected to the AC main. Then different types of technologies are used to connect the two levels. Gate drives are supplied through opto-couplers, feedback functions are implemented through combination of linear opto-couplers and hall-effect sensors, and soft start function is implemented through relay. A bulky multiple winding transformer is also needed to supply the various isolated supplies for the different functions.

In more modern drives a new type of architecture is becoming popular that uses single level power conversion processing (Figure 3). Here all the gate drive, protection, feedback sensing and control functions are implemented within the same level of the high voltage supply rail and all the functions are coupled with each other in the same electrically connected level. Now higher performance control loop is implemented easier, protection is localized and more effective, the board layout is more compact contributing to lower EMI and the total system cost is lower. This type of architecture is most effective for "dedicated purpose" drive such as for home appliance and the new class of small industrial drive less than 5hp or 3.75kW, called Micro-Inverter or Micro-Drive.

A more advanced type of architecture is emerging that uses mixed mode power conversion processing (Figure 4). Primarily the power conversion processing is done at the high voltage supply level. A second level of signal processing is added for motion profiling and communication. This second level helps facilitate network and option cards connection for "general purpose" drives. Also it simplifies the encoder connection for position sensing in servo drives. The two levels of processing are connected through isolated serial bus such as the SPI interface. The bus speed and performance are not very demanding because the information bandwidth is not so severe at this connection layer with all the high speed signal processing already done locally at the power conversion processing level. A comparison between the different power conversion architectures is shown in Table 1.

HIGH VOLTAGE INTEGRATED CIRCUIT TECHNOLOGY

One of the key features of the single level and mixed mode Power Conversion Processing Architecture is the integration of the gate drive, protection and sensing functions. The integration is implemented in a high voltage integrated circuit (HVIC) technology (Figure 5). This structure supports a versatile set of devices and circuits plus the unique capability of integrating high voltage level shifting and floating CMOS in a single piece of silicon.

The 600V or 1200V N-channel and P-channel LDMOS are used for level shifting functions from low voltage to high voltage and vice versa. The CMOS circuits can be referenced to a high voltage floating supply level (VB-VS) for high-side gate drive and

signal processing circuits. This floating capability allows differential mode signal processing on top of 600V or 1200V common mode voltage. Other uses for the high voltage devices include start-up bias supply and synchronous bootstrapping supply.

Gate drive circuits are implemented in enhanced voltage CMOS with supply rail up to 25V and provides necessary gate drive voltage to the IGBT. Analog and digital circuit blocks are implemented in BiCMOS. Circuit library includes Pulse Width Modulator (PWM), Voltage Control Oscillator (VCO), Precision Sense Amplifier, Fast Fault Comparator and other power conversion control functions.

GATE DRIVER AND PROTECTION FUNCTIONS

The gate drive and protection functions are divided into three types of circuits. The first one is the output buffer that is needed to provide sufficient gate charge to the IGBT. The second is the level shifters that are needed to interface between the control signals to the high side and low side output buffers. The third is the sensing of overload conditions in the IGBT and the appropriate countermeasure taken in the output buffer as well as fault status feedback.

IR pioneered the first single phase and three phases gate driver ICs and is now leading the evolution of the products. These devices set the standard for appliance drives and industrial micro-drives. Each new generation of devices are evolved to obtain higher performance and more features at lower cost. Table 2 shows the available types, ratings and main features for three generations of products.

First generation devices were the first of their types and spurred the development of the Single Level Power Conversion Processing Architecture. They provide simple high and low side gate drive functions. The monolithic integration delivers compact size and the tight layout lowers EMI. Separate series were offered to match the price/performance requirements for appliance and for industrial drives.

Second generation devices were introduced to improve the transient immunity capability as well as the introduction of 1200V rating. Higher level of immunity to –Vs voltage spike allows simpler layout and handles safely larger excessive voltage swing at the IGBT stage during transient over-load conditions. The series for industrial drives feature 1200V rating for 460Vac input while the 600V devices are used for 230Vac applications. The series for appliance drives feature 110/220Vac operation, improved noise immunity, more functions and lower cost.

Table 2: Three Generations of HVIC Products

Types	Topology & Ratings	Features	Applications
First Generation			
IR2101 IR2102 IR2103 IR2104	1-Phase Gate Drive 600V, 0.5A	Simple HS and LS Drivers 8-pin Package	110-220Vac Appliance 0.1-0.5kW
IR2110 IR2113	1-Phase Gate Drive 600V, 2A	High Current HS/LS Drivers 14-pin Package	230Vac Industrial 3-10kW
IR2125 IR2127 IR2128	High Side Gate Drive 600V, 1A	HS Shutdown HS Fault Status	230Vac Industrial 3-10kW
IR2130 IR2132	3-Phases Gate Drive 600V, 0.5A	Control all 3-phases LS Current Comp and Amp	230Vac Industrial 0.3-3kW
Second Generation			
IR2106 IR2107 IR2108 IR2109	1-Phase Gate Drive 600V, 0.3A	High Side UVLO Soft Gate Drive 8-pin package	110-220Vac Appliance 0.1-0.5kW
IR21064 IR21074 IR21084 IR21094	1-Phase Gate Drive 600V, 0.3A	Logic + Power Ground Dead time adjust 14-pin package	110-220Vac Appliance 230Vac Industrial 0.1-3kW
IR2181 IR2182 IR2183 IR2184	1-Phase Gate Drive 600V, 1A	High Current HS/LS Drivers High –Vs Immunity 8-pin package	230Vac Industrial 3-10kW
IR21814 IR21824 IR21834 IR21844	1-Phase Gate Drive 600V, 1A	High Current HS/LS Drivers Logic + Power Ground High –Vs Immunity 14-pin package	230Vac Industrial 3-10kW
IR2213	1-Phase Gate Drive 1200V, 2A	High Current HS/LS Drivers High –Vs Immunity	460Vac Industrial 3-10kW
IR2136 IR21362	3-Phases Gate Drive 600V, 0.3A	Low Cost 3-Phase LS Current Trip Comparator	110-220Vac Appliance 230Vac Industrial 0.1-3kW
IR2133 IR2135	3-Phases Gate Drive 600V, 0.5A	High –Vs Immunity LS Current Trip Comparator	230Vac Industrial 0.3-5kW
IR2233 IR2235	3-Phases Gate Drive 1200V, 0.5A	High –Vs Immunity LS Current Trip Comparator	460Vac Industrial 0.3-5kW
Third Generation			
IR2137	3-Phases Gate Drive 600V, 0.5A	HS De-Saturation Detection Synchronous Soft Shutdown	230Vac Industrial 0.3-5kW
IR2237	3-Phases Gate Drive 1200V, 0.5A	HS De-Saturation Detection Synchronous Soft Shutdown	460Vac Industrial 0.3-5kW
IR2171	High Side Current Sense 600V	Differential +/-300mVin PWM output, +/-0.5%	230Vac Industrial 0.3-5kW
IR2271	High Side Current Sense 1200V	Differential +/-300mVin PWM output, +/-0.5%	460Vac Industrial 0.3-5kW
IR1110	3-Phases SCR Drive 230/460Vac	Soft Charge Control DC Bus Regulation Power Dip Ride-Through	460Vac Industrial >10kW

Third generations devices are now being introduced to address robust protection of the IGBT inverter stage. Over-current conditions are fatal faults to the drives. Three types of over-current faults -- line to line short, ground fault or shoot-through -- are commonly encountered as shown in Table 3 and Figure 6. Protection circuit implementation and type of over-current sensing device vary depending on which mode of the over-current condition to be protected due to different path and flow of the current in each mode. And protection schemes also depend on the drive architecture.

Over-current mode	Potential causes
line-to-line short	Miss-wiring, motor leads short, motor phase-to-phase insulation breakdown
Ground fault	Motor insulation breakdown to ground
Shoot through	False IGBT turn-on

Table 3: Over-current modes and causes

Main feature of the new third generation gate driver products, 600V IR2137 and 1200V IR2237, is the integration of IGBT protection functions with high side de-saturation detection and synchronous soft shutdown for all six IGBTs. The high side output buffer schematic is shown in Figure 7. Here the pull-up and pull-down output drivers are separated to allow simpler optimization of IGBT turn-on and turn-off characteristics. In the event of an over-current condition that triggers the de-saturation threshold, a soft shutdown sequence is initiated. The soft shutdown scheme prevents large voltage over-shoot at the IGBT due to too fast current turn-off transient. The synchronization allows all six IGBTs to be turned off together to avoid potential false IGBT turn-on.

The integrated protection scheme in the IR2137/2237 offers many advantages. Table 4 shows a comparison against the traditional protection method in the Two Levels Power Conversion Processing Architecture.

	Two Levels Architecture	Single Level Architecture IR2137/2237
Gate Drive	Six Fast Optical Isolators	Single chip
IGBT Protection	Two Hall Effect sensors and two comparators	Integrated high side de-saturation protection
	Snubber circuit or discrete soft shutdown circuits	Integrated soft shutdown function
Additional Circuits	Brake IGBT drive circuit with a optical isolator	Integrated brake IGBT driver circuit
	Four floating power supplies	Use bootstrap power

Table 4: Protection methods - single and two levels power conversion architectures

Figure 8 shows the oscillogram of the current and voltage turn-off waveforms of the IGBT in short circuit condition using the IR2137 solution. No snubber circuit was used for this test. Thanks to soft shutdown feature, there is virtually no overshoot voltage across the collector and the emitter when it turns softly off.

CURRENT SENSING FUNCTION

Perhaps the most difficult function in the drive design is sensing the inverter stage and motor phase currents. The current signals are used for current mode control, which requires high precision and linearity, as well as for over-current protection, which requires fast response. Different circuit techniques have to be used to process the current signals depending on which parts of the inverter stage that the current signals are sampled. Precision, low ohmic value, sensing resistors are typically used in the current path to generate a sensing voltage signal with maximum range of +/-300mV to minimize power dissipation. Alternatively hall-effect sensors are used. They are generally bulkier and more expensive than sense resistors but they have the advantages of loss-less sensing.

Practically the current signals can be sampled in series with +DC bus, -DC bus, individual IGBT phase leg or motor phase lead (Figure 9). Current signals sampled in the + DC or – DC bus are the vector sum of all the IGBT phase leg currents. Also the signal content is the pulse width modulated envelop, at fixed carrier frequency, of the fundamental variable frequency motor current. Therefore rather complicated sample and hold plus digital signal processing circuits have to be used to extract useful current information with good linearity and accuracy. Individual IGBT phase leg current is somewhat easier to process but cannot escape from dealing with carrier frequency sampling. By far the simplest current signal available is from the motor phase lead. The signal content is only the fundamental variable frequency motor current. However the one significant complication is that the small differential signal in the mV range is floating on top of 600V to 1200V common mode voltage. In addition the common mode voltage is swinging from –DC to +DC at a dv/dt rate of up to 10V/ns.

IR now offers a new type of monolithic HVIC product that solves the difficult problem of sampling motor phase current. The IR2171 is a 600V product and the IR2271 is the 1200V counterpart. Figure 10 shows the block diagram of the HVIC. Basically the current signal as sampled across (Vin+, Vin-) is processed by a precision differential amplifier. After the amplified signal is converted to digital format by an analog to digital converter, the signal is translated from the floating high voltage channel (VB-VS) to the ground referenced supply rail (VCC-COM) through high voltage level shifters. Then the signal is re-constructed and sent to the VO pin as 35kHz digital PWM output. Note that the VBS floating channel has common mode voltage range up to 600V for IR2171 and 1200V for IR2271 plus immunity to dv/dt transient up to 50V/ns. Another advantage is the low current drawn from the VBS circuit such that a bootstrap power supply can be used instead of complicated isolated supply.

The typical performance data of the 600V IR2171 are shown in Table 5. Note that the extremely low temperature drift that enables the device to operate linearly in wide industrial temperature range. And the high power supply ripple rejection ratio counteracts the effects of noises on the bootstrap supply.

Linearity	0.4%
Linearity temperature drift	0.0003%
Total offset	1.5mV
Total offset temperature drift	30uV/°C
Gain error	1%
Gain error temperature drift	37ppm/°C
Power Supply Ripple Rejection	.06%@6kHz, 1Vpp

Table 5: Performance Data of the IR2171

Actual system performance data using the IR2171 in an industry leading closed loop Servo Drive is shown in Figure 11. The Servo Drive has a 1.3kHz current loop bandwidth on top of 8kHz PWM frequency. The top trace is velocity monitor signal that indicates a fast acceleration and deceleration from 0 to 5000rpm in 40msec. The motor has two times the inertia load such that it requires substantial current amplitude up to 12.5A. The bottom trace is a superimposed composite of the IR2171 output re-constructed as analog signal on top of a hall-effect sensor output of the same motor phase current output. The two signals are practically indistinguishable.

Figure 12 shows an application circuit of using the IR2171 together with the IR2137 to provide linear current feedback as well as IGBT protection. IR2171 shares the bootstrap power supply in its high side secondary circuit with IR2137. Output of IR2171 is a 35kHz digital PWM signal and is able to interface directly to the micro-controller's capture compare/timer unit. IR2137 provides the fast de-sat protection as well as synchronous soft shutdown. Together these two chips provide another step toward the IR Power Conversion Processor ™ Architecture.

SOFT START FUNCTION

The DC bus capacitor is charged by the AC line through the input diode bridge. Common practice is to use a series resistor that limits the charging current when the AC line is switched on. Since the series resistor is dissipative, some sort of bypass is required after the bus is charged up. Conventional methods use temperature sensitive (NTC) resistor, electromechanical contactor bypass, or auxiliary SCR bridge (Figure 13). All of these methods suffer from bulkiness, slow charge up time due to the exponential tail in the charging profile, long recovery time after AC line disturbance, too slow protection against DC bus short circuit and little or no control of the DC bus voltage.

A new IC, IR1110, from the IR Power Conversion Processor ™ product family, solves these problems and offers additional value added features. This new IC is designed to phase control a SCR bridge as shown in Figure 14. The phase angle of the SCR firing pulses is advanced step by step, increasing the bus voltage in controlled series of steps, as illustrated in Figure 15. Total ramp-time is programmable and typically set at 150 to 350ms with linear charging profile.

IR1110 is unique in its ability to minimize the effect of line interruption. The power dip ride through capability of motor drive is defined as the time it takes to re-establish load power after input line dips or outages. Figure 16 shows the fundamental difference between series resistor charging versus IR1110 SCR phase control method. Load power can be re-established even during the ramp-back time in the phase control method whereas the resistor method dictates a long waiting period until the bus capacitor is fully charged and the series resistor is bypassed.

Other value-added benefits of the IR1110 include increase of inverter output current at low speed using bus regulation as well as protection against bus over-voltage, bus short circuit and phase loss (Table 6).

IR1110 Features	**System Benefits**
Phase control DC bus voltage linear ramp-up	Controlled and faster system start up time
Phase control re-charging after line interruption or outage	Fast power dip ride-through reduces system down-time
Dynamic control of DC bus voltage	Enable higher inverter output current at low speed by decreasing IGBT losses
Phase angle retardation due to DC bus short circuit	Protect against input bridge failures from high fault current
Phase loss detection and feedback	Protect against high capacitor ripple current from single phase

Table 6: Value-Add Features and Benefits of the IR1110 Soft Start Solution

ARCHITECTURAL EVOLUTION AND ROAD MAP

The IR Power Conversion Processor ™ Architecture, for the first time in the industry, provides an integration of product and system designs for the power conversion processing functions of AC or BLDC motor drive. Designers no longer have to wrestle with incompatible components that are designed with little or no system knowledge on how they are supposed to work together. Now the system problems are addressed with a set of integrated product solution (Figure 17). Furthermore the architecture is modular and expandable while evolving with advancement in the technologies of power and control elements.

Evolution in IGBT/FRED and associated HVIC gate drive technologies will allow high carrier frequencies with lower losses and lower EMI. That in turns will reduce the heat sink and noise filtering requirements such that the overall size of the drive will also be decreased in lockstep. Monolithic integration of the gate drive, protection and linear current sensing functions in a single piece of silicon using HVIC technology will be the next step. Going still further out and taking advantages of the compatibility of integration with the single level power conversion processing architecture, more functions will be either monolithic or multi-chip integrated in the IR Power Conversion Processor (Figure 18). Potentially the sensing function will integrate phase current, phase voltage and IGBT junction temperature feedback signals that can be used to enable algorithms for sensor-less vector control. Additionally the IGBT devices will be integrated with on-chip current and temperature sensors that are compatible with the sensing IC. And since integration of these control elements together with the micro-controller or DSP controller are small enough to be easily mounted on PCB alongside the IMS or DBC Substrate containing the shunt resistors and power elements, new type of Power Conversion Processor Module can be defined.

In the system design side, the open loop V/Hz control with current limit function had completely been integrated within the Single Level Power Conversion Processor ™ Architecture and it is now the standard for the Micro-Drive. Adding the linear current sensing function expands the architecture to sensor-less vector control. And in the future multi-functions sensing chips integrating current and voltage feedback with both amplitude and phase information will simplify the designs of sensor-less field oriented vector control. For designs that require an encoder feedback such as the permanent magnet servo control and sensor based field oriented vector control, a Mixed Mode Power Conversion Processor Architecture can be used. The high bandwidth current regulator will be completely configured in the power conversion processing level while the speed and flux regulations are handled separately in another motion profile processor operating at an isolated supply level. In all cases, the complete power conversion functions for the AC or BLDC motor drive will be integrated in modular fashion with appropriately defined serial communication protocol. The net effect is that the price points for advanced control are reduced and economic implementation of high performance drives are brought into the realm of high volume industrial and appliance applications. Figure 19 illustrates the nominal price points for drives with different control methods reducing with the IR Power Conversion Processor ™ road map.

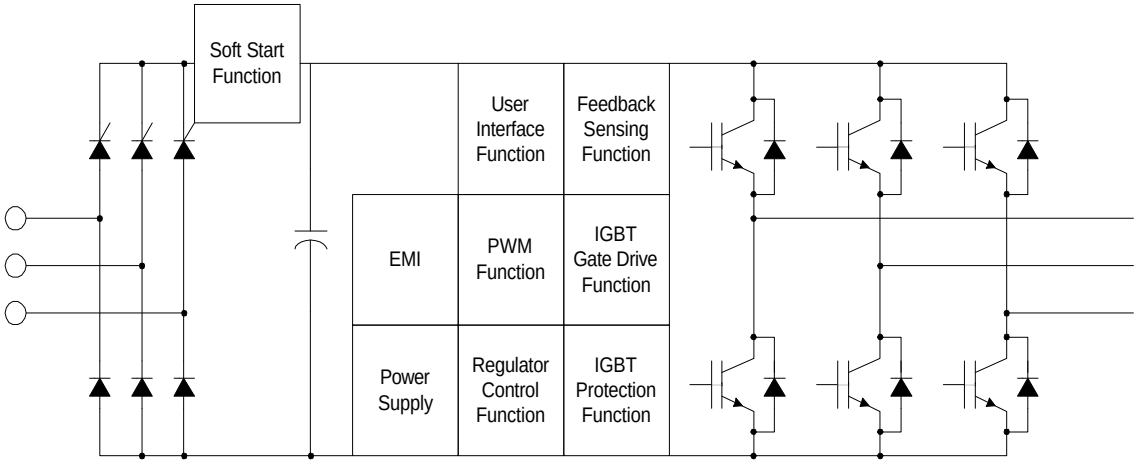


Figure 1: AC or BLDC Motor Drive Power Conversion Processing Functions

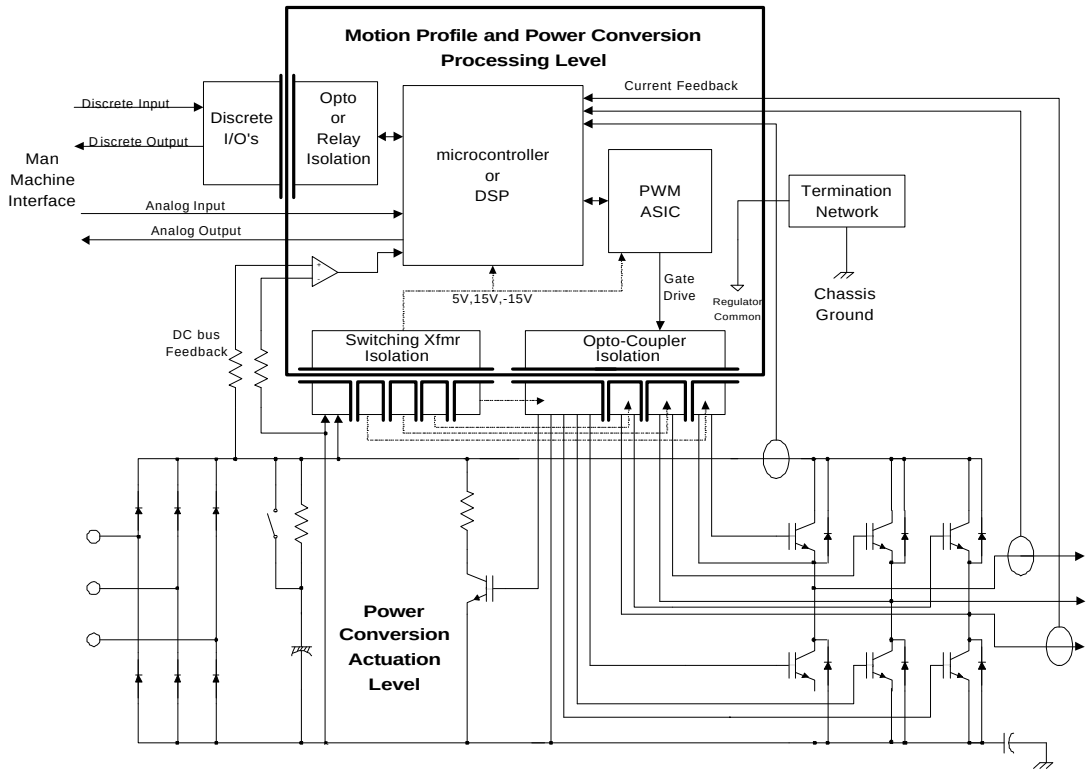


Figure 2: Two Levels Power Conversion Processing Architecture

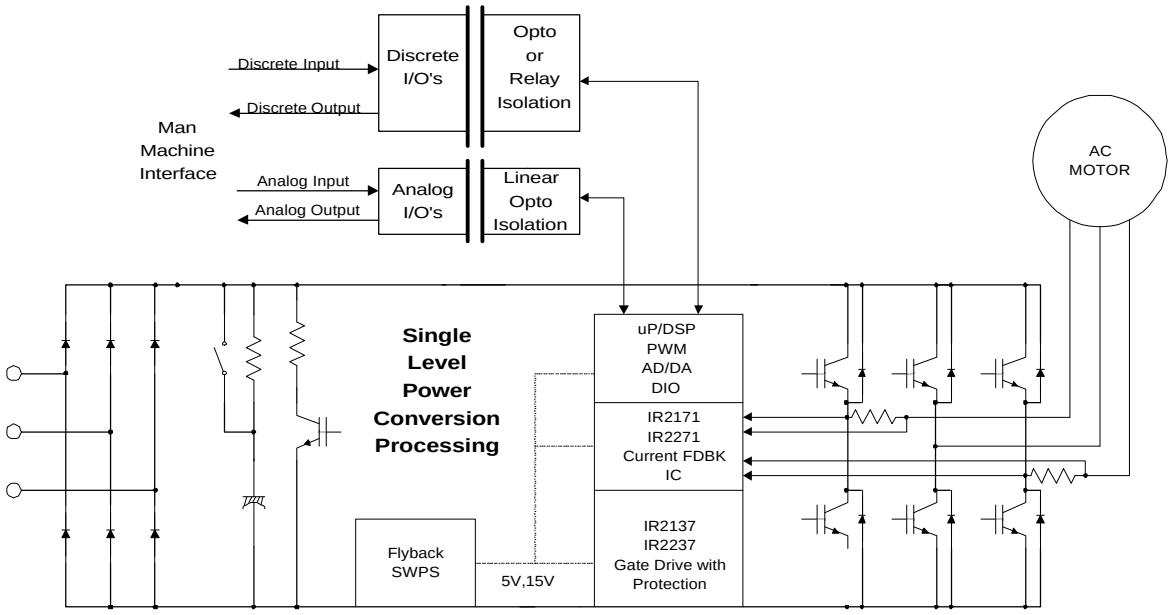


Figure 3: Single Level Power Conversion Processing Architecture

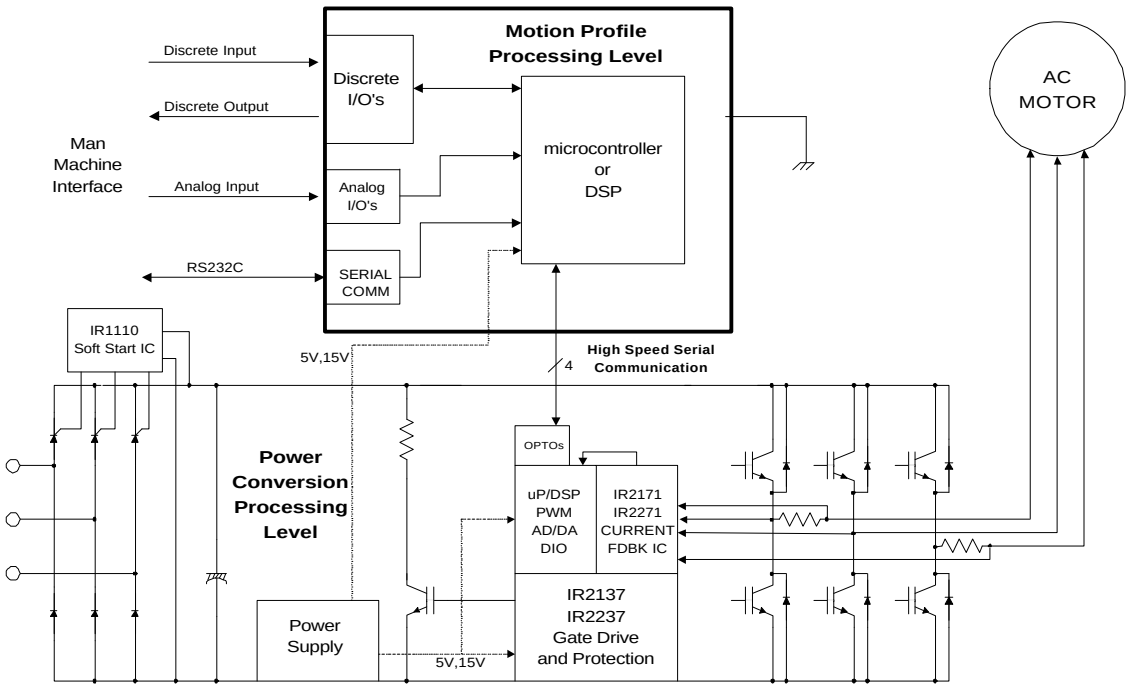


Figure 4: Mixed Mode Power Conversion Processing Architecture

Two Levels Architecture	**Single Level Architecture**
Motion and Power Conversion Processed Together	Motion and Power Conversion Processed Separately
Isolation at Opto Drivers (sensitive high speed signals)	Isolation at Digital Interface (high noise-margin signals)
Large Deadtime	Small Deadtime
Complex Switching Supply	Simple Flyback Supply
Large Hall Current Sensors	Small HVIC Current Sensors
Protection at Signal Level	Protection at Power Level
Larger Size and More EMI	Smaller Size and Less EMI

Table 1: Comparing Two Levels vs. Single Level Power Conversion Architecture

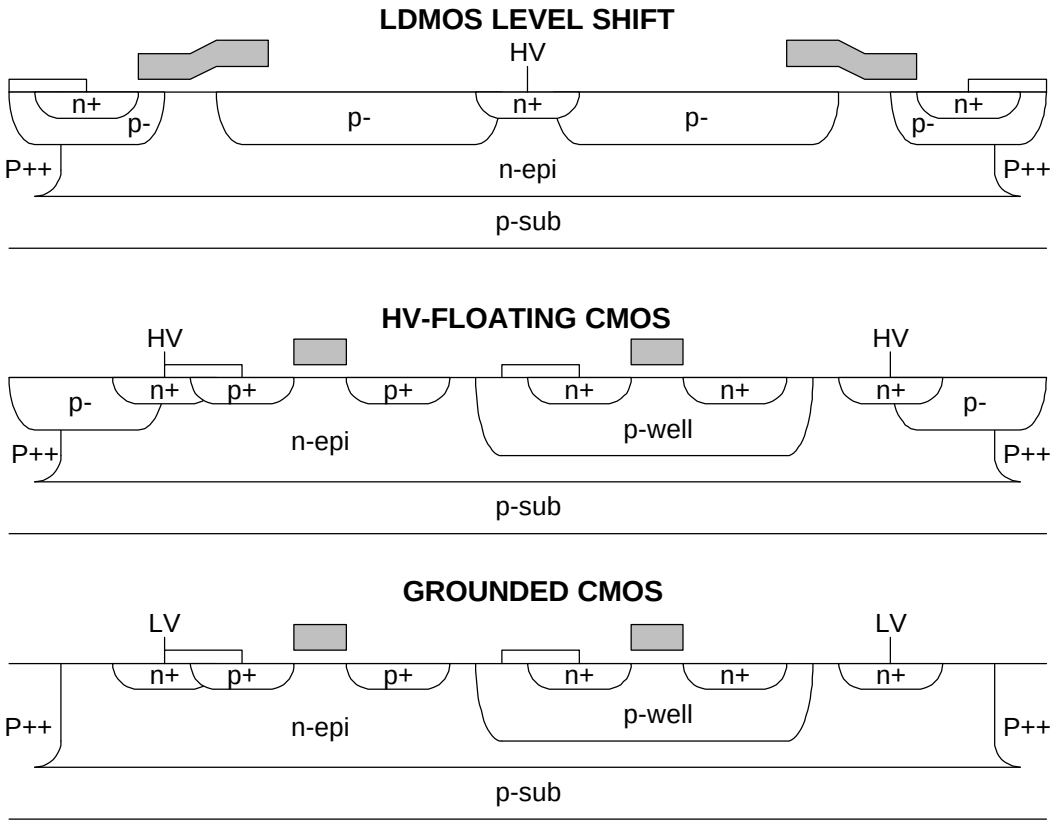


Figure 5a: Device Cross Section of HVIC

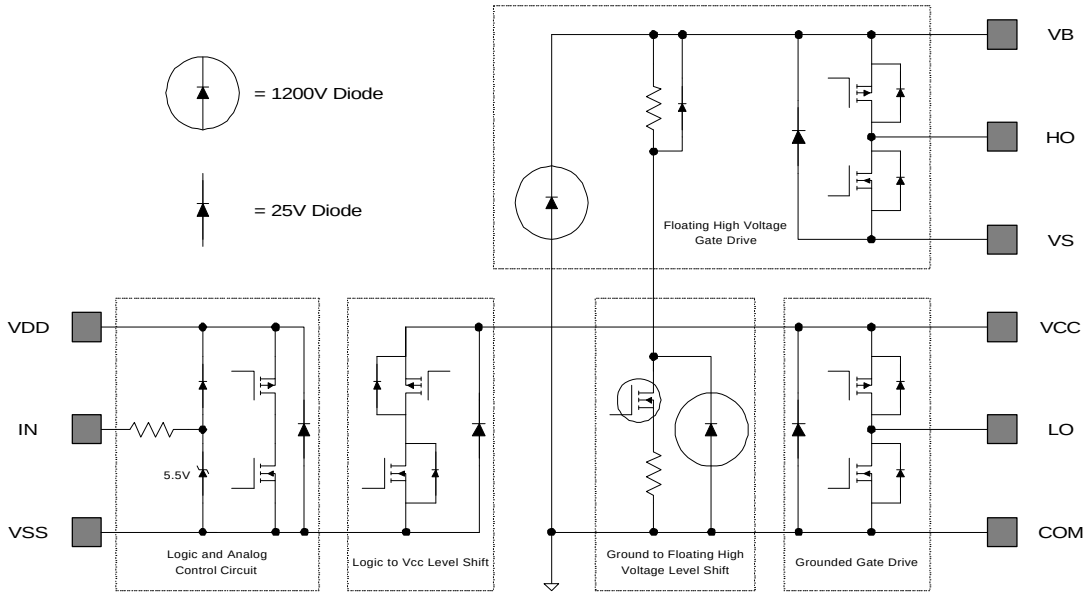


Figure 5b: Common Circuit Blocks of HVIC

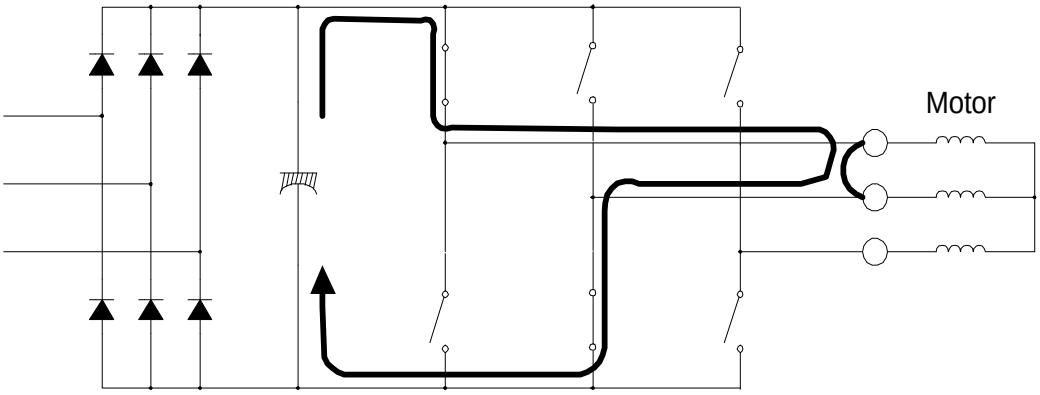


Figure 6a: Line to Line Short

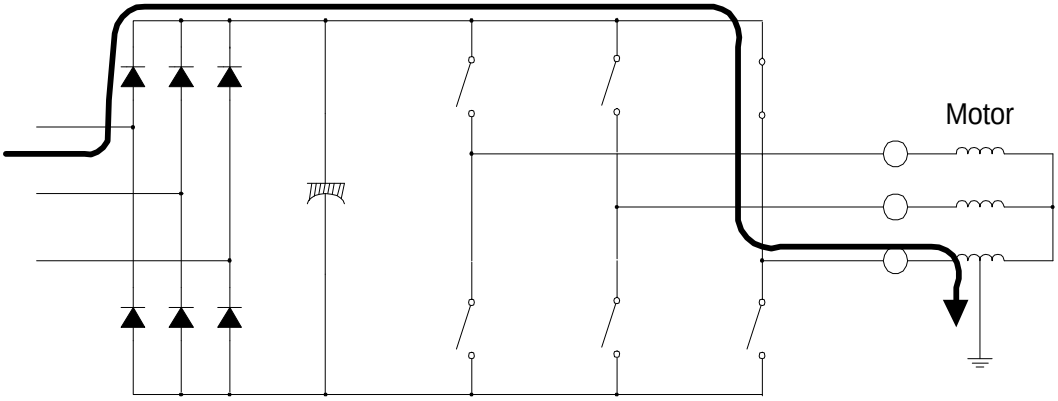


Figure 6b: Ground Fault

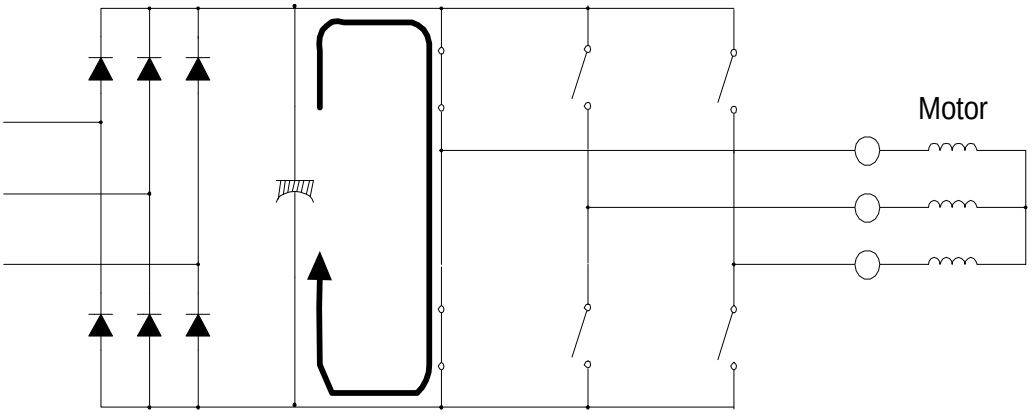


Figure 6c: Shoot-through

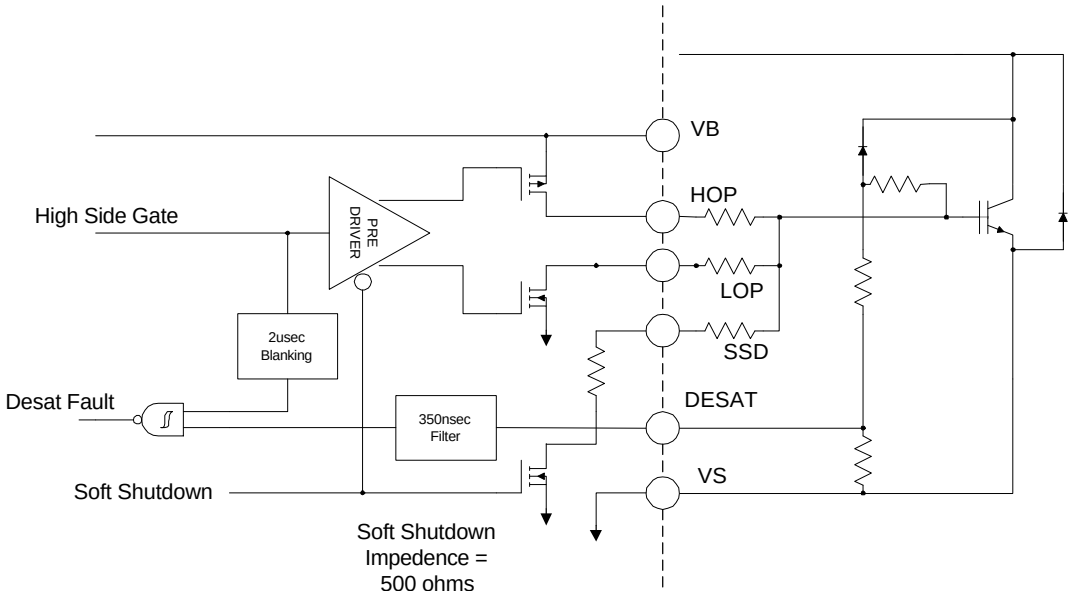


Figure 7: High side Output Buffer Circuit Schematic for IR2137/2237

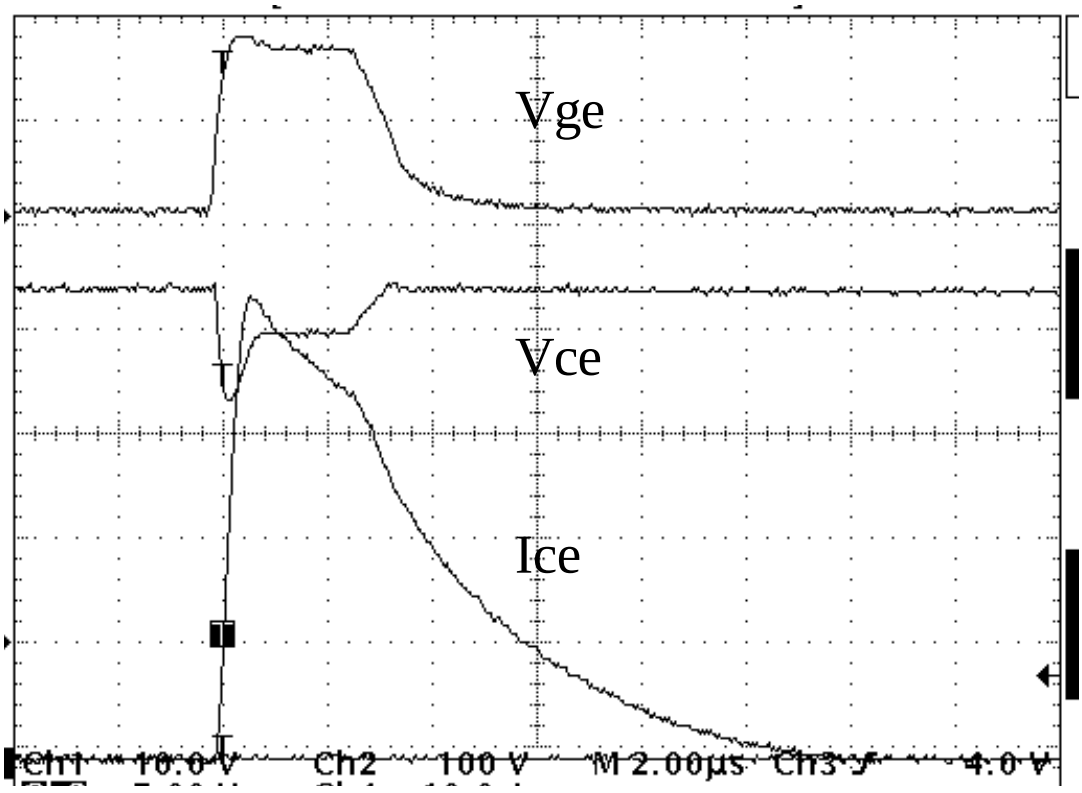


Figure 8: IGBT Soft Shutdown using IR2137

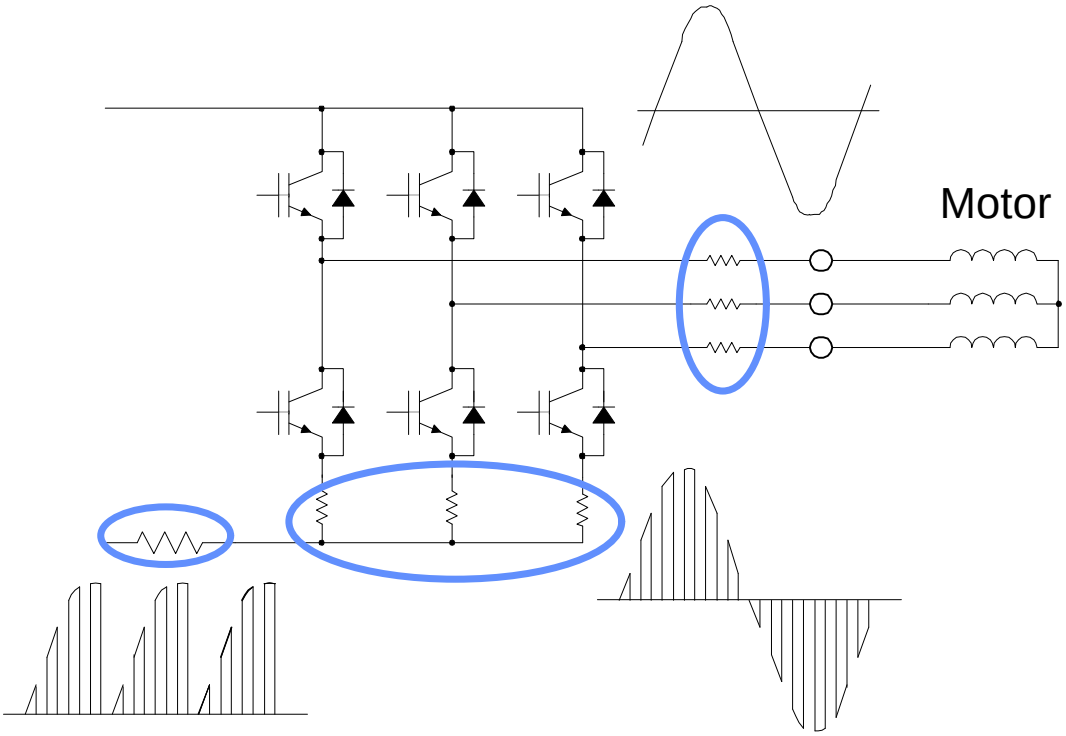


Figure 9: Current Signal from DC Bus, IGBT Phase Leg or Motor Phase Output

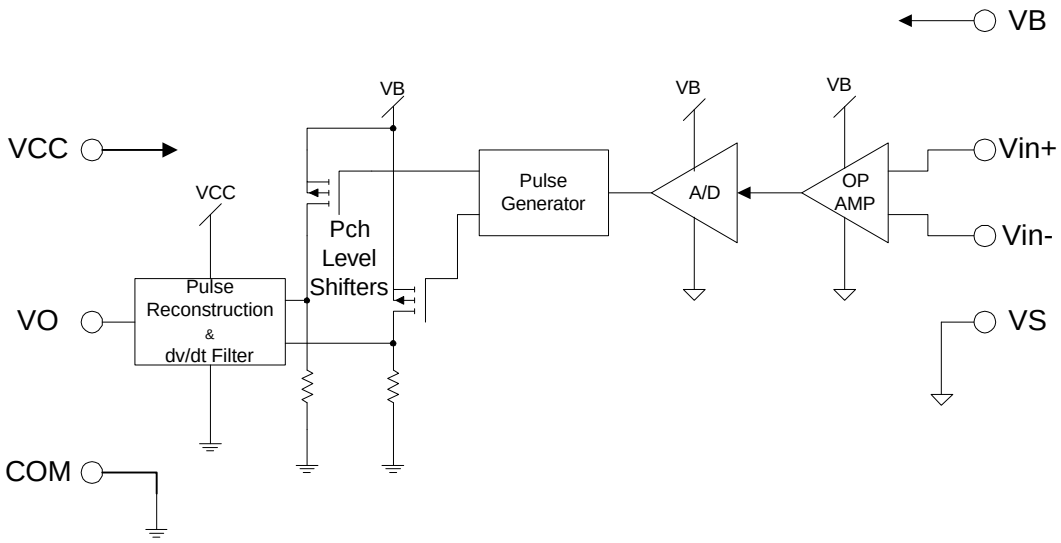


Figure 10: Current Sensing IC Block Diagram

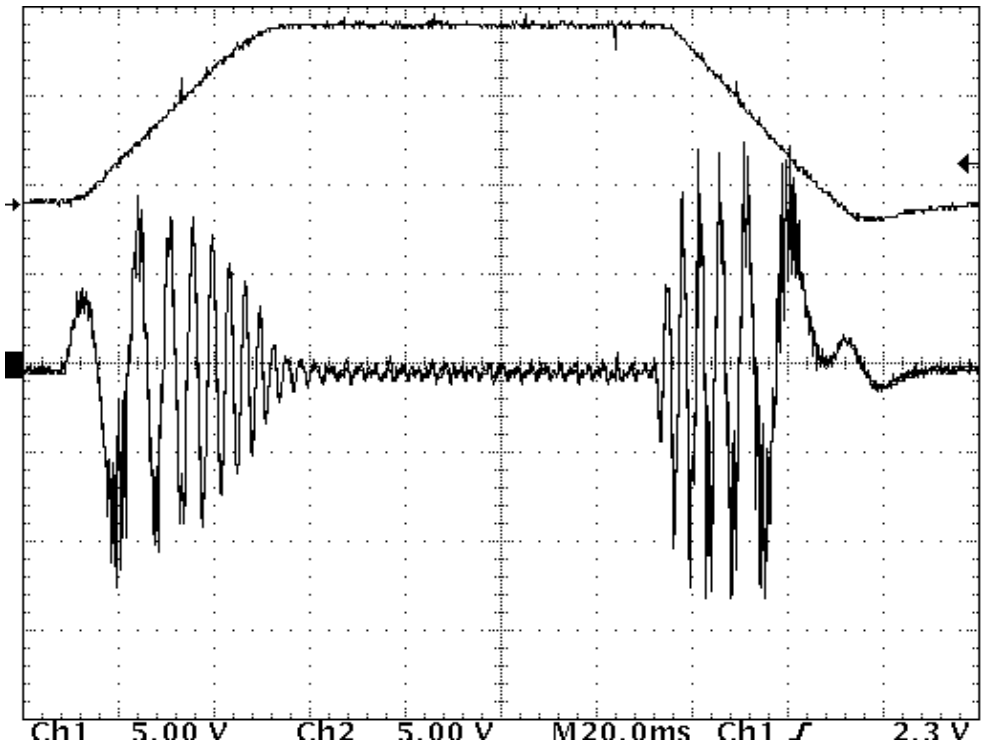


Figure 11: Current Waveforms Using the IR2171 in a Closed Loop Servo System during Fast Acceleration and Deceleration

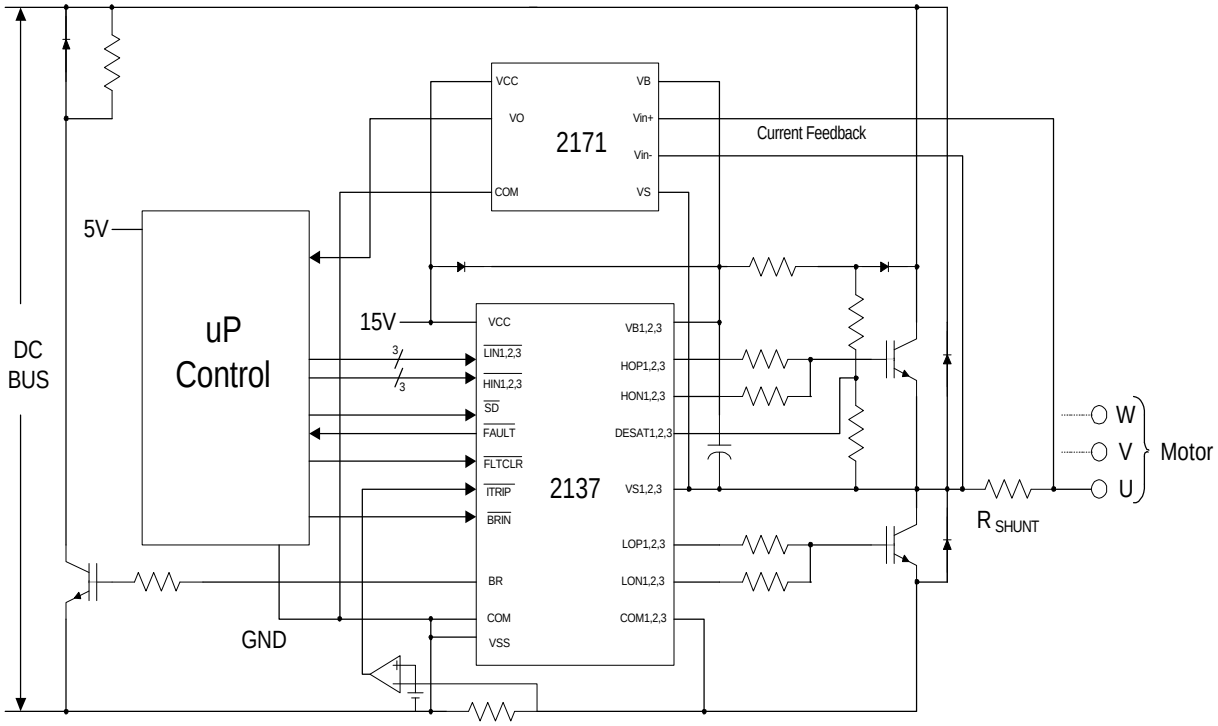


Figure 12: IR2171 & IR2137 in the IR Power Conversion Processor ™ Architecture

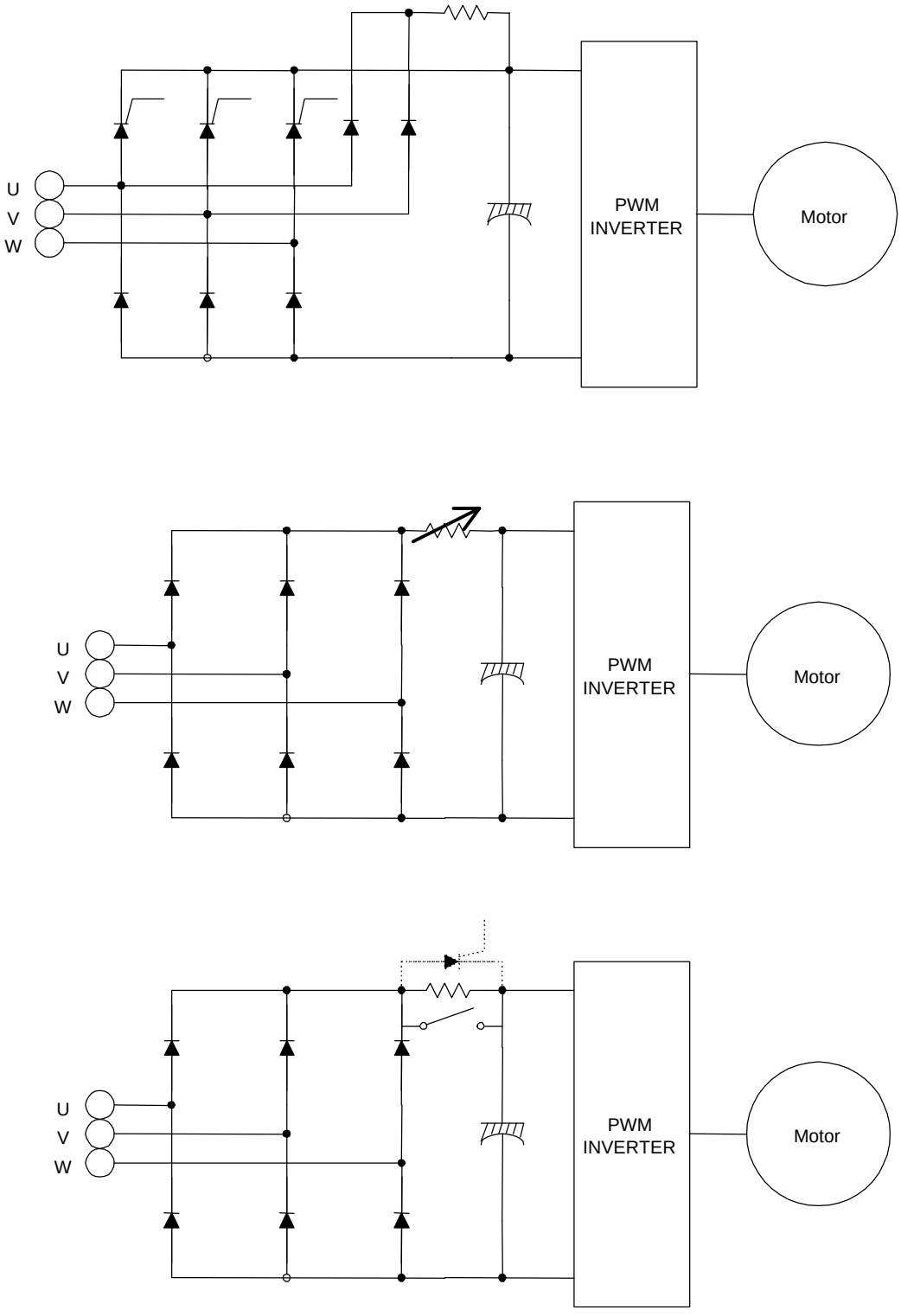


Figure 13: Series Resistor Connected Soft Charging Circuits

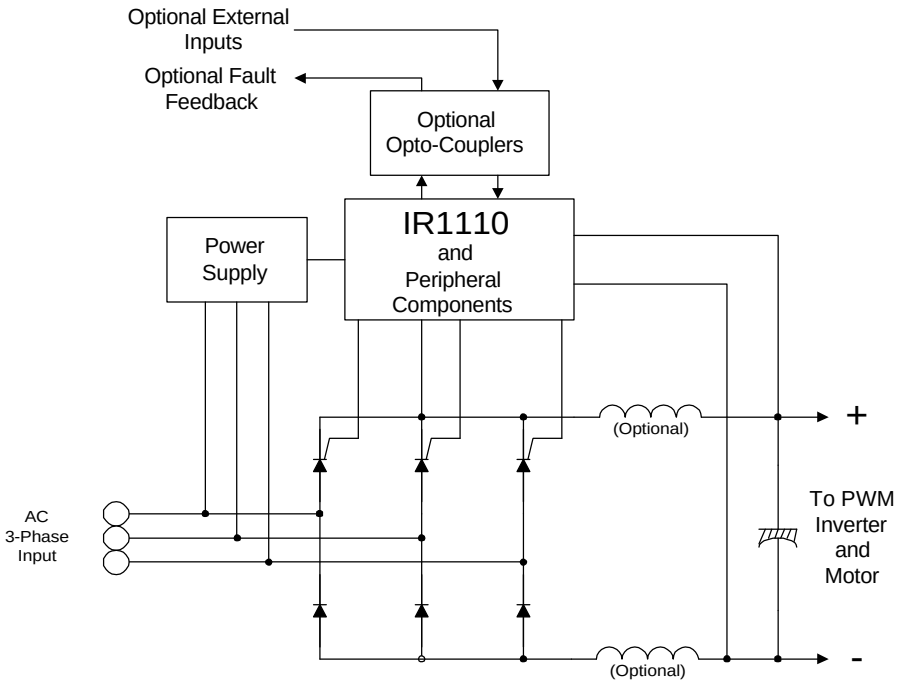


Figure 14: IR1110 Phase Control SCR Soft Charging Method

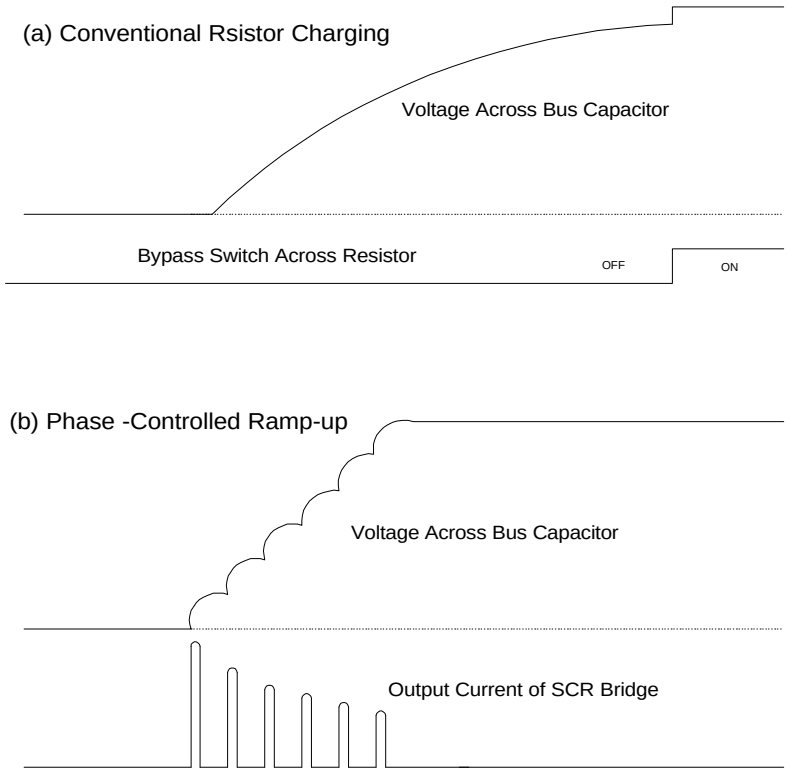


Figure 15: Series Resistor vs. Phase Control DC Bus Voltage Ramp-Up Waveforms

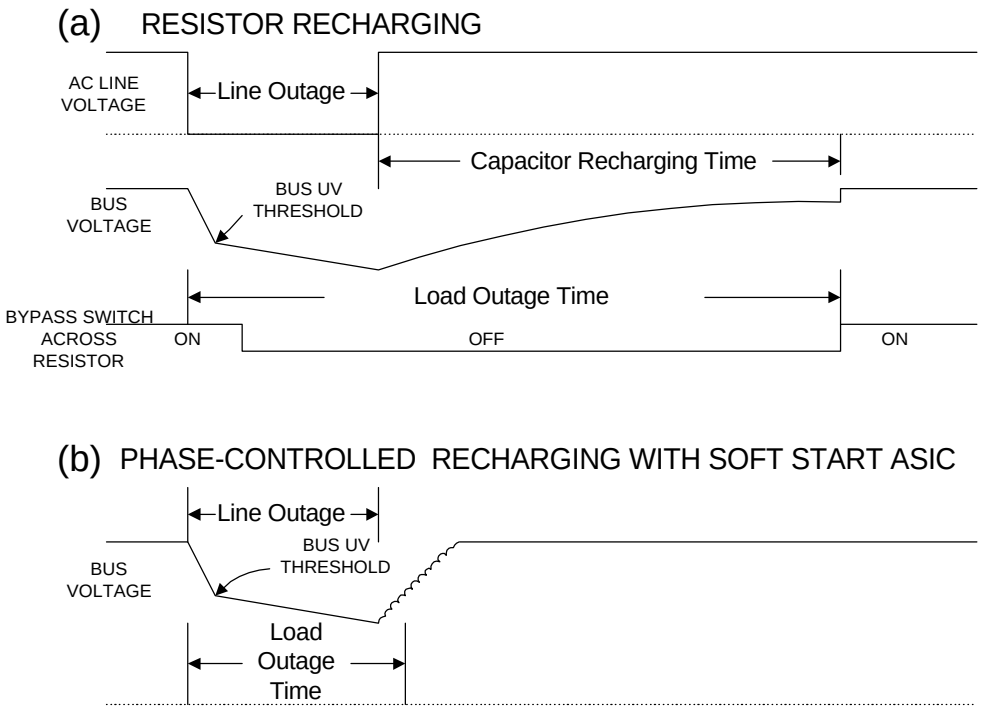


Figure 16: Power Dip Ride Through

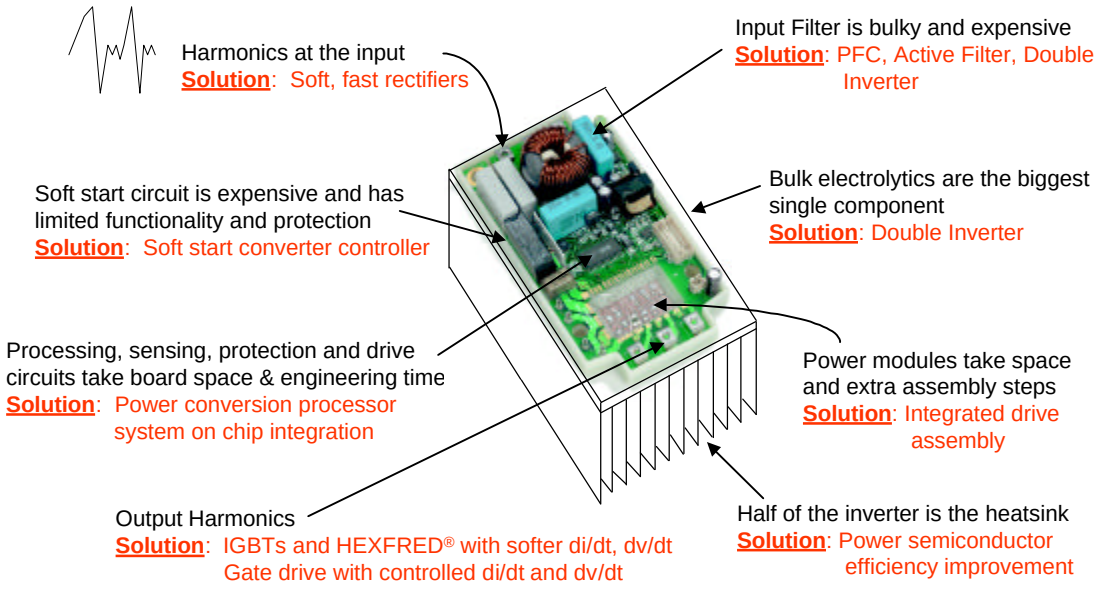


Figure 17: Drive System Problems and Integrated Product Solutions

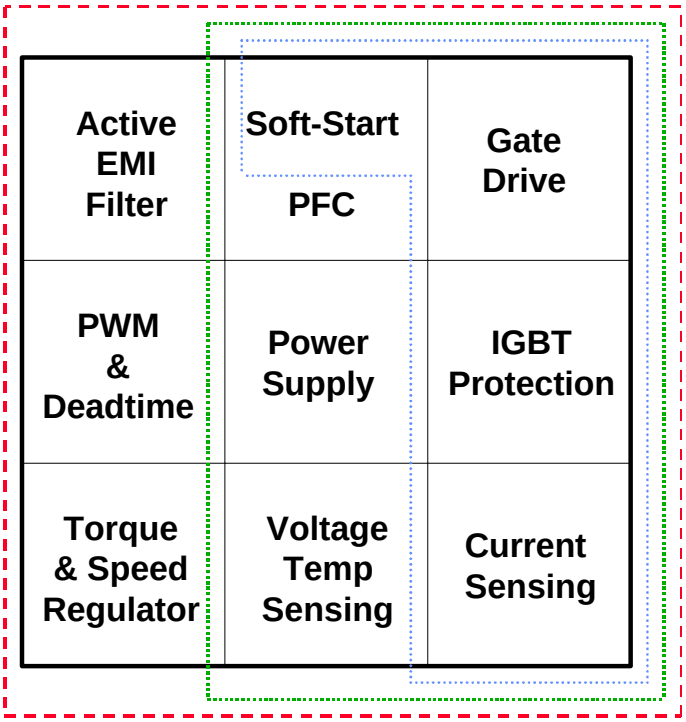


Figure 18: Product Function Evolution in IR Power Conversion Processor

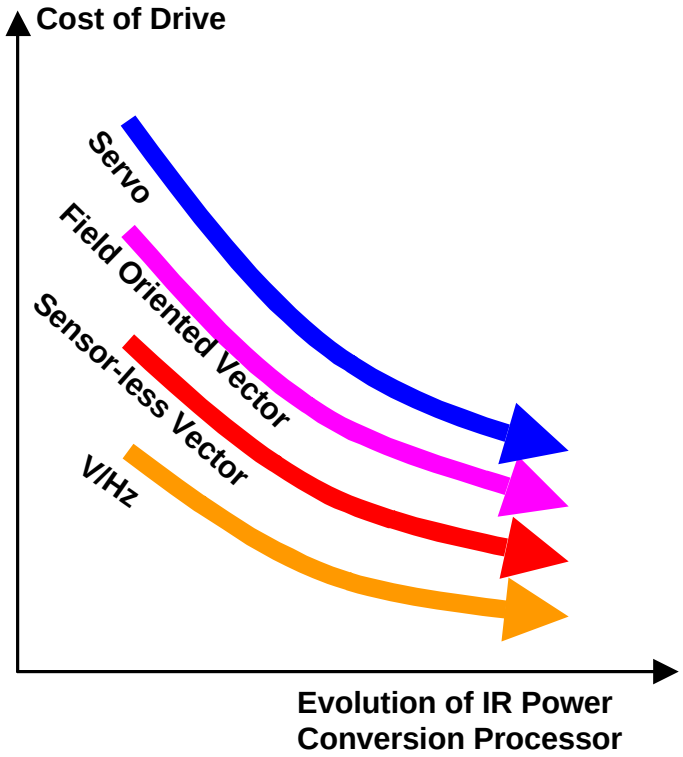


Figure 19: Nominal Cost of Drive vs. Evolution of IR Power Conversion Processor

`SOLVING IGBT PROTECTION IN AC OR BLDC MOTOR DRIVE

The new IR2137 IGBT Gate Driver IC integrates Ground Fault and Over-Current Protection with Soft Shutdown.

1. INTRODUCTION

In the last decade, industrial AC drives have become more advanced in performance and more compact in size. This is largely due to the rapid development of power silicon technology, including the enhancement of IGBTs and of High Voltage Integrated Circuits. Additionally, this technological growth has been particularly accelerated for low horsepower (< 5 Hp) AC Drives. Yet, the ground fault protection, a feature sought increasingly in motor drives of all power levels, is available widely only in the high-end models due to the sensors and other circuitry involved. The market, however, continues to demand a fully protected, yet inexpensive, system. To meet this demand, International Rectifier has introduced the IR2137: a new generation 3-phase IGBT gate driver, featuring full IGBT protection and advanced soft shutdown features.

2. TRADITIONAL METHODS OF IGBT PROTECTION

This section outlines the traditional methods of protection, thereby allowing us to better appreciate the need for the IR2137.

2-1 Background Theory for Protecting Against Failure

One of the most common, and fatal, AC drive faults for IGBTs is the Over-Current condition. Table 1 outlines the causes for the 3 common Over-Current modes.

Over-Current Mode	**Potential Causes**
Line-to-Line Short	Mis-wiring, Motor leads shorting, Motor phase-to-phase insulation breaking down.
Ground Fault	Motor phase-to-phase insulation breaking down.
Shoot Through	False IGBT turn-on.

Table 1: Potential Causes of Over-Current

In order to protect IGBT devices effectively under an Over-Current condition, we need to focus on two factors.

First, one needs to detect the Over-Current mode and shut the system down. In both Line-to-Line and Shoot Through mode, the short-circuit current flows from and to the DC bus capacitors (Figures 1 and 3). Therefore, a shunt resistor in the ground path can detect these Over-Current conditions. However in the Ground Fault mode, the current flows from the AC line input, through the positive DC bus and high side IGBT, to the earth ground (Figure 2). Thus such an Over-Current condition must be detected either with a shunt resistor on the positive bus line or by detecting the current in the output lines.

Second, one needs to look at the AC drive architecture, and its influence on the method. For instance, Figure 4 shows a typical Floating Ground Reference Architecture, in which the micro-controller (μC) is on the Floating Ground reference, and therefore any Over-Current detection circuit needs to be isolated. Alternate architecture may require reduced or no isolation.

2-2 Traditional Methods of Over-Current Detection

Method 1

One can detect the Line-to-Line Short and Shoot Through currents by inserting a Hall Effect sensor or a linear opto isolator across the shunt resistor. The device should be in series with the negative DC bus line. For Ground Fault protection, an additional Hall Effect leakage current sensor could be placed either on the AC line input or on the DC bus. The protection circuit is then implemented by using fast comparators. The output of these comparators is 'OR'd with the micro-controller or PWM generator to initiate the shutdown of the gate signals.

Method 2

If located in the motor phase output, each Hall Effect sensor uses 2 comparators. This is done because both positive and negative current polarities flow during a Line-to-Line Short condition. Another important consideration is the total propagation delay for shutdown. The delay time associated with the optical isolators in the gate drive and the Hall Effect sensor is typically more than 2 microseconds. Therefore, regardless of protection circuitry implementation, this delay should be added to the circuit delay, before matching it with the IGBT short circuit duration time. As shown in Figure 4, the configuration requires 2 Hall Effect sensors and/or opto isolators in addition to the protection circuit. The protection circuitry comprises of comparators (2), voltage references, capacitors, and resistors.

Method 3

Another protection method is to use an IGBT de-saturation circuit. This discrete circuit can be constructed in the secondary side of the opto gate driver. (Opto isolated devices with built-in de-saturation circuits can also be found in the market). This circuit detects voltage build-up across the collector and emitter while the device is fully on. If the voltage exceeds a specified limit, the associated gate signal is shut off. A discrete circuit would require a comparator with voltage reference, a high voltage diode, and various resistors and capacitors.

2-3 Traditional Methods of Over-Current Shutdown

For shutting down an IGBT when an Over-Current condition is detected, a soft turn-off is preferred because it reduces a high voltage spike across the collector and emitter of the IGBT device at fault. Thus it provides a wider margin for the RBSOA limit during a short-circuit condition and the snubber circuit can be significantly minimized or even eliminated. When implemented in the discrete circuit based on the floating ground

reference architecture, a soft turn-off circuit can get very complex. Each IGBT gate drive circuit requires an additional fast opto isolator and soft turn-off circuit with the dedicated totem pole buffer transistors. Given circuit costs and complexities, a snubber circuit is preferred to the discrete soft shutdown circuit. For low Hp devices, the snubber circuit can be implemented with a high frequency type capacitor across the DC bus, near the IGBTs.

2-4 Problems with the Traditional Method

A. Circuit Control Problems

In a soft shutdown scheme, simultaneous shutdown of all 6 IGBTs is required to prevent a potential false turn-on while the IGBTs are in the soft shutdown mode. If a high side IGBT is turned off softly while the other IGBTs are in the middle of a switching transition within a PWM period, that IGBT can unintentionally be turned back on. It is extremely difficult to synchronize simultaneous shutdown using traditional architecture.

B. Part Count, Size, and Cost Problems

If the system requires full IGBT protection, including Ground Fault protection, and if it is based on the floating ground reference architecture, then the gate drive and protection circuit require the following major components even without the soft shutdown feature:

- 6 fast opto isolators
- 2 fast Hall Effect sensors or fast linear opto isolators
- 2 comparators
- 4 floating 15V power supplies

Hall Effect sensors and opto isolators are relatively large and bulky, thus requiring a lot more space than a monolithic IC. In addition, if the system requires a soft shutdown function, 6 additional opto isolators and 6 buffer circuits (with a provision for soft turn off capability) are required. Thus, whereas low Hp AC drive systems are today moving toward smaller sizes, the above solutions provide neither the simplicity nor the integration of the gate drive and protection circuitry that is needed.

The total cost, including assembly of the inverter system, is large due to the large number and bulkiness of components. Furthermore, components such as the Hall Effect sensors are still subject to manual assembly.

To circumvent these issues, a small, integrated IC device that is capable of performing all the above functions is a necessity.

IR2137: 3-PHASE GATE DRIVER WITH INTEGRATED IGBT PROTECTION

International Rectifier has now introduced the IR2137 into the AC drives market. This latest High Voltage Integrated Circuit provides a monolithic solution to driving all six IGBT gate drivers, while simultaneously providing full IGBT protection and soft shutdown. In contrast to the Floating Ground Reference architecture discussed in the

previous section, the IR2137 circuit enables a simple structure. The differences between the two architectures are summarized in Table 2.

	Floating Ground System	**IR2137 solution**
Gate Drive	Six Fast Optical Isolators	IR2137
IGBT Protection	Two Hall Effect sensors and Two comparators	IR2137 integrated function with a shunt resistor and a comparator
Additional Circuits	Four floating power supplies	Eliminated (boot strap power)
	Snubber circuit or discrete soft shutdown circuits	Eliminated by integrated soft shutdown function
	Brake IGBT drive circuit with a optical isolator	Eliminated by integrated brake IGBT driver circuit

Table 2: Solution Comparison of Gate Drive and IGBT Protection

For the IR2137 circuit, as shown in Figure 5, the IR2137 and a micro-controller (µC) share the same ground potential – the negative DC bus potential. (This architecture is already the industry standard in the micro AC inverter drive segment). Unlike its traditional counterpart, the IR2137 circuit requires a single shunt resistor and associated comparator. With this, it can perform all modes of IGBT short circuit protection.

Additionally, the IR2137 contains IGBT de-saturation logic in the circuit of each high-side gate drive. In the event of a Ground Fault condition, the DESAT pin is activated, and the fault signal is transferred to the low side fault logic circuit. The low side fault logic then initiates the simultaneous soft shutdown of all 6 IGBTs. When the soft shutdown signal is transferred back to the high side, the active PMOS/NMOS transistor buffer goes into a high impedance mode and another weak NMOS transistor becomes active to slowly drive the gate pin low. The shutdown softness can be programmed by adding an external resistor to the SSD pin – thus allowing the user to optimize softness for the specific gate charge of the IGBT. To eliminate the dv/dt induced false triggering of the DESAT pin, there is a blanking filter delay of 2 microseconds at each high-side gate turn-on transition.

Figure 8 shows the oscillogram of the ground fault protection feature in the IR2137. In this measurement, a size 4 IGBT, IRG4BC40KD, was used in conjunction with a turn-on resistor, Rg = 33Ω, turn-off resistor, Rg = 16Ω, and softness resistor, R_{SSD} = 500Ω. The top trace in Figure 8 is the IGBT gate signal (10V/div), while the middle trace is the V_{CE} voltage (100V/div), and the bottom trace is the IGBT short circuit current (40A/div). No snubber circuit was used for this test. One can see that the de-saturation protection activates quickly and the soft shutdown feature virtually eliminates the overshoot voltage across the collector and the emitter.

For comparison, the oscillogram of a 'hard' shutdown is shown in Figure 9. The same IGBT, IRG4BC40KD, and the same PCB pattern were used as in the example shown in Figure 8. The top trace is the IGBT short circuit current and the bottom trace is the IGBT V_{CE} voltage (100V/div). As can be seen in Figure 9, the overshoot voltage reaches approximately 100V above the normal V_{CE} voltage during the turn-off transition.

In summary, the IR2137, a monolithic IC, provides excellent protection and soft shutdown features in an extremely compact and cost-effective package.

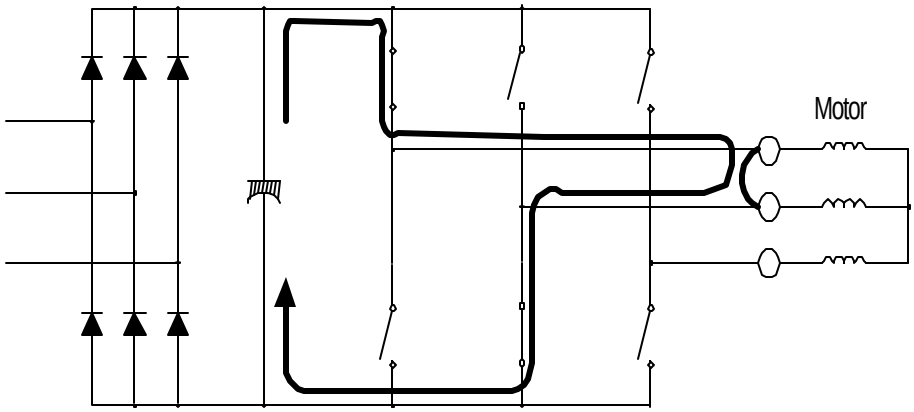


Figure 1: Current Flow during Line-to-Line Short

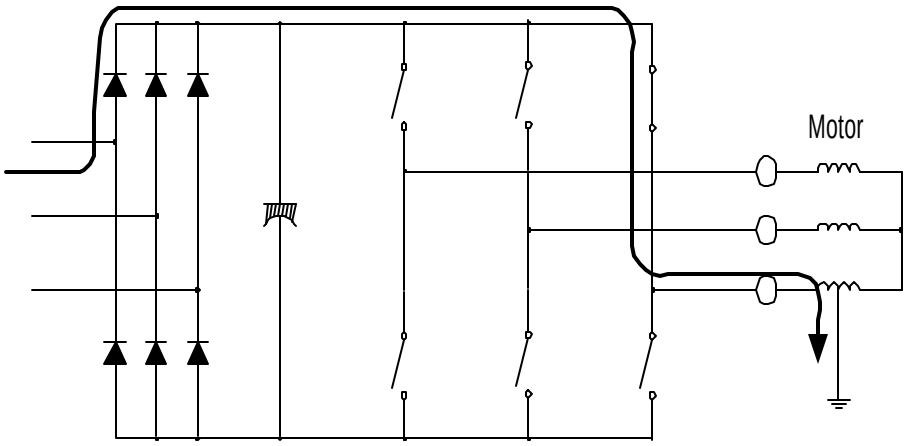


Figure 2: Current Flow during Ground Fault

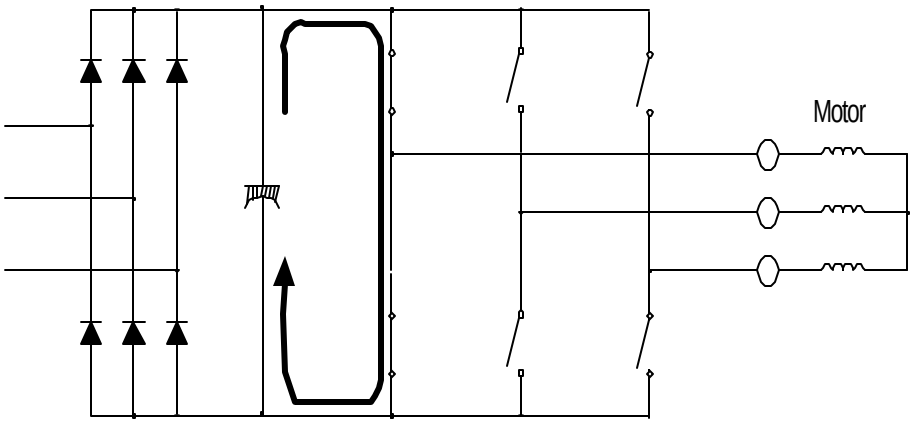


Figure 3: Current Flow during Shoot Through Mode

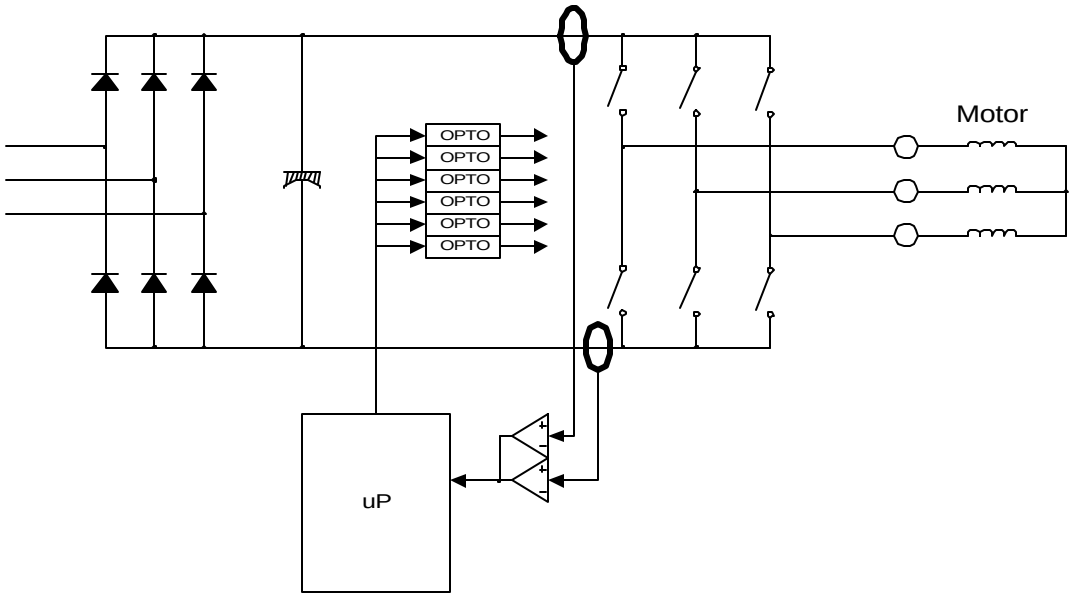


Figure 4: Overcurrent Protection in Floating Ground Reference System

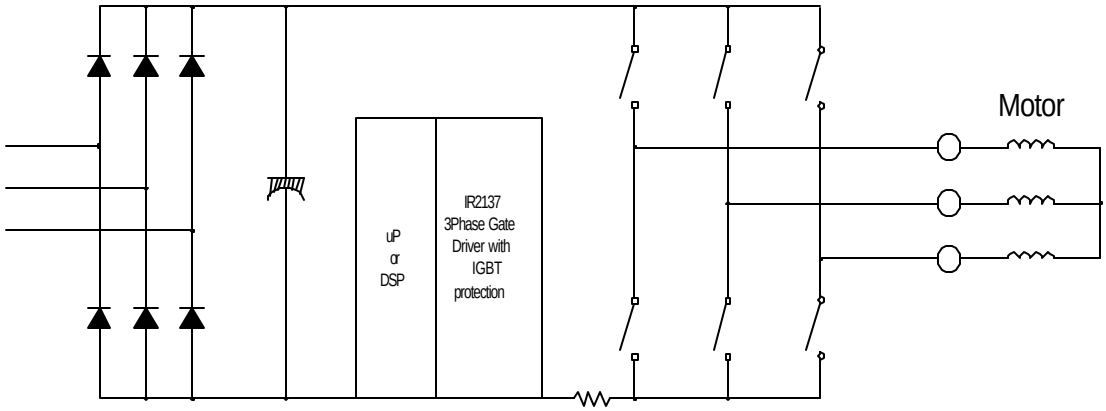


Figure 5: IR2137 Gate Driver with IGBT Overcurrent Protection

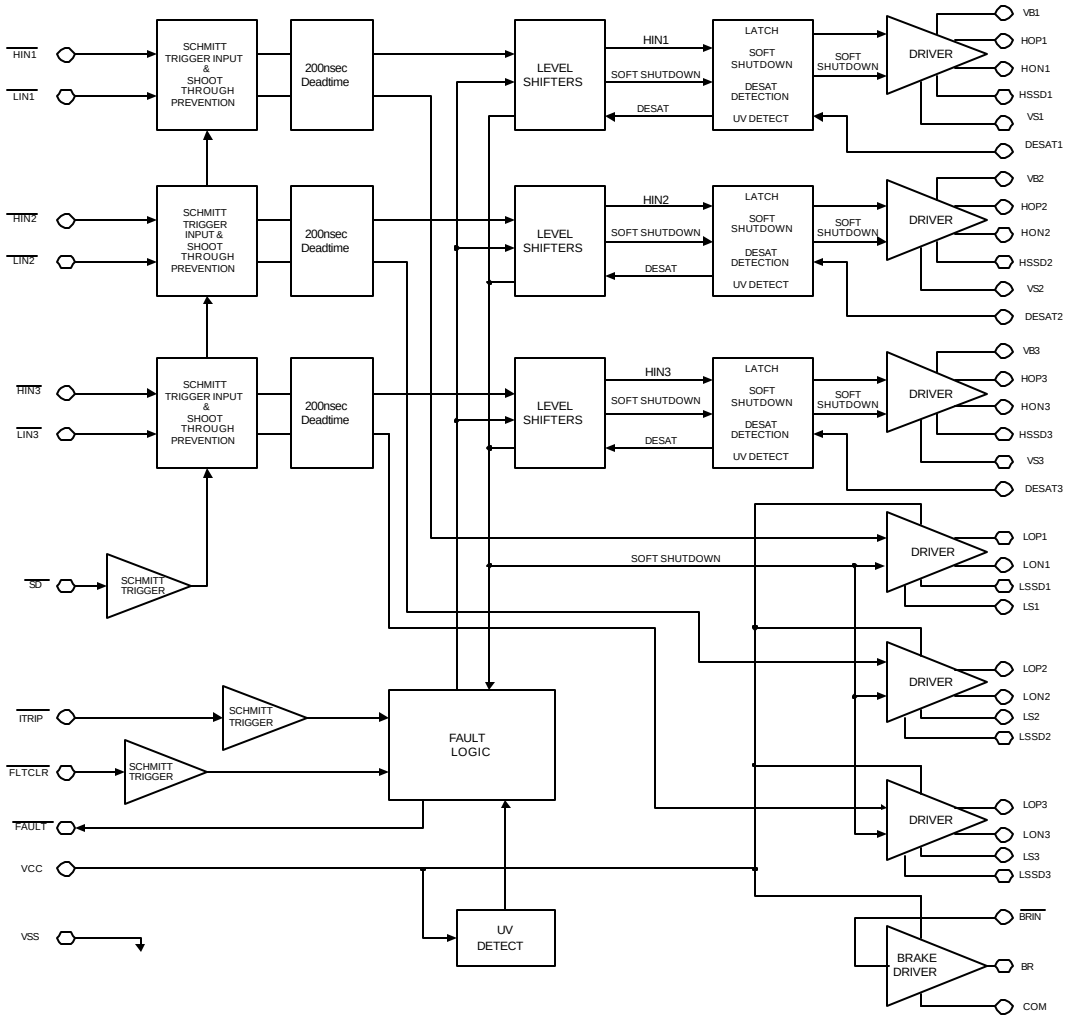


Figure 6: IR2137 Block Diagram

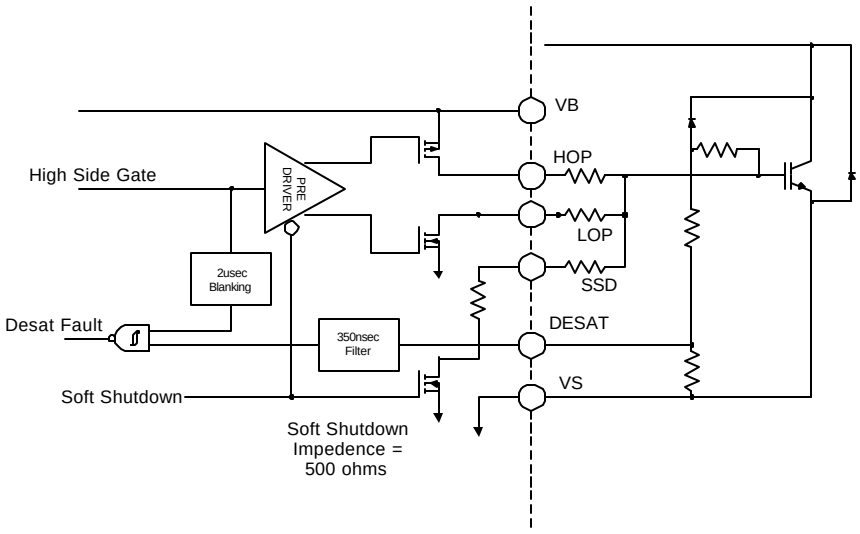


Figure 7: IR2137 High Side Circuit

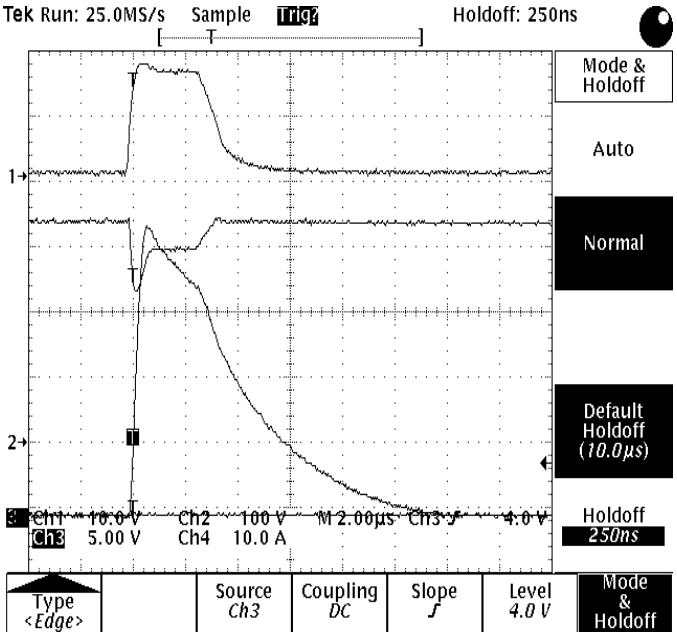


Figure 8: IR2137 Soft Shutdown

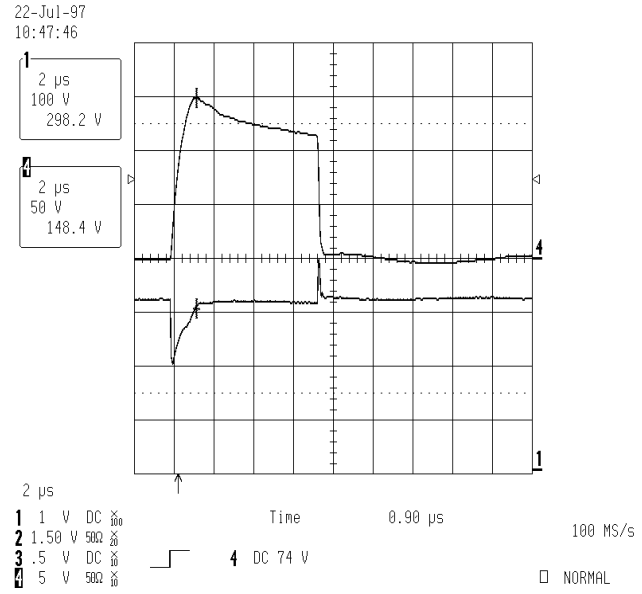


Figure 9: Hard Shutdown

NEW MONOLITHIC HIGH VOLTAGE CURRENT SENSING IC SIMPLIFIES AC DRIVE INTEGRATION

As power electronic technology evolves, the AC PWM inverter drive becomes more efficient, more compact, more advanced in performance, and less expensive. This tendency has been further accelerated in the small horsepower AC drives, particularly in the area of less than five horsepower range application. High Voltage Integrated Circuit (HVIC) technology has been one of the major contributing factor to achieve these objectives.

The motor current sensing device is an important element in the AC motor drive, which provides IGBT protection information as well as linear current feedback information for control purposes. Traditionally, the Hall Effect current sensing device has been widely used in the past. In some applications, shunt resistors with the optically isolated linear current sensing device have been used as well. However, these devices have often been limiting further size reduction and simplification of the AC inverter drives due to the mechanically large construction and the number of additional peripheral components.

International Rectifier has recently introduced the 600V monolithic motor current sensing IC based on the proprietary high voltage technology, which is the first in the industry. This will enable further integration and simplification of the AC drive and accelerate functional advancement of the Intelligent Power Module.

INTRODUCTION

Today's AC PWM inverters, the so-called "micro AC inverters", are typically equipped with the high voltage gate drive IC (HVIC) to accomplish significant space and cost reduction by a simplified ground isolation scheme. Due to the non-galvanic isolated direct control of the IGBTs, all control functions, except user interface I/Os, have the ground potential fixed to the negative DC bus voltage potential.

As the drive performance advances towards the sensor-less vector drive operation, the following features have been requested in the linear current sensing device to achieve a certain performance goal:

- Low secondary power to share the bootstrap power supply with HVIC gate drive IC
- Low PSRR (power supply variation rejection ratio) with a wide range of power supply voltage
- High accuracy, low temperature drift, reasonable bandwidth
- High dv/dt common noise immunity by PWM motor drive
- Simple and easily manufacturable construction

- Monolithic and low cost

Traditional devices - either Hall Effect or the optically coupled current sensing device - lack some of the above criteria. In order to meet the criteria above, the IR2171 has been newly developed. This paper discusses the key implementation issue of IC (i.e. high voltage IC technology), the latest test results, applications, and future direction of the high voltage linear current sensor technology.

MONOLITHIC CURRENT SENSING IC

The IR2171 is a linear current sensing device, which is based on the monolithic integrated circuit, fabricated with a high voltage junction isolation. Figure 1 shows the functional block diagram of the IR2171.

The internal circuit is mainly divided into two segments: the high side circuit and the low side circuit. High voltage level shifters isolate these circuits and allow two independent reference ground potentials within the monolithic integrated circuit. The high side circuit, floats up and down from 0 to 600V with respect to the low side ground potential (COM). This high side circuit contains most of the important functions such as the high precision operational amplifier, the analog-to-digital conversion unit, and the pulse generator. There are two P-channel level shifters, which transfer the digital PWM information in the high side circuit to the low side circuit by trailing edge pulses. The low side circuit contains simple circuits such as the PWM pulse reconstruction circuit, dv/dt filter and the output buffer.

The key innovation and achievement resides in the high side circuit. Today, although the 600V as well as the 1200V high voltage junction isolation technologies are available, it requires several key technological hurdle and innovation in order to accomplish precision measurement of small analog signal under harsh environment. Monolithic integration, low power consumption on the secondary floating power supply, wide range of the secondary voltage supply, and low temperature drift are the key design issues of this high precision linear current sensing device.

Figure 2 shows cross sectional view of three main devices, which form the monolithic integration. The P-channel level shifter transfers information across the high voltage barrier between the low side grounded CMOS circuit and the high side floating CMOS circuit. This device, located in the high side well, is designed to be able to send data from the high side well to the low side circuit under any voltage differential (600Vmax) including high dv/dt transient condition up to 50V/nsec. CMOS devices both in the low and the high side have well structures based on the P-type substrate and designed to sustain up to 25V breakdown voltage providing enough margin over 15V power supply for the motor drive environment.

High side CMOS floating circuit contains key technical innovation for high precision analog circuit. One is the low temperature drift P-channel MOS differential input stage which is designed to cancel out the temperature coefficient difference. The other is the stable current source to provide reference to the analog circuit, which can operate without degradation of accuracy under wide range of power supply ranging from 7V to 20V.

MOTOR CURRENT SENSING APPLICATIONS

Motor phase current feedback is quite often required in the motor drive application. In order to sense the Motor phase current, the location of sensing devices is ideally in series with the motor phase lead output as shown in Figure 3, since it provides the current waveform of the motor fundamental frequency. (If the current sensing devices are located in the other places within the PWM inverter power structure, then they need to reconstruct the measuring waveform to the fundamental waveform).

Application of the motor phase current is mainly divided into two purposes - the control purpose and the monitoring purpose. For the control purpose, it becomes a vital part when used for the closed loop current control in the vector control environment in terms of linearity, accuracy, offset temperature drift, and bandwidth. When used for the monitoring purpose, requirement becomes less stringent.

Historically Hall Effect current sensing device or more recently an optically isolated linear current sensing device has been used to meet the requirement. High voltage isolation is done by galvanic isolation in these devices. Although these devices have been widely used, it sometimes becomes a bottleneck for more advanced integration and simplicity in the AC PWM inverter drive application. Construction of Hall Effect sensor is mechanically large and does not compatible with any conventional integrated circuit packages due to electro-magnetic device structure. This in turns creates unwanted manual assembly process for the inverter drive manufacturing. It is also inherently expensive. Linear optical device is also a hybrid device consisting of three pieces of silicon devices; high side amplifier circuit, light emitting diode, and receiving circuit. Drawback of this device is large current requirement in the high side circuit (typically 7mA or more) and limited range of the high side voltage supply. Therefore it typically requires dedicated power supplied by individual transformer winding and its associated circuit.

IR2171 solves these cumbersome and open the door to more advanced PWM AC inverter integration. In particular, if the AC drive is based on Power Processing Architecture where the regulator hardware common is referenced to the negative DC bus potential, design of motor current feedback becomes very simple and a part of plug-in building block. Figure 3 shows typical block diagram of this type of AC inverter drive where all hardware pieces of the regulator function – uP, high voltage gate drive IC, high voltage linear current sensing IC- are directly coupled together and sit on the DC bus. In this architecture, whole regulator functions only require 5V and 15V with one common. The power supply is greatly simplified.

Figure 4 shows more detailed application circuit. IR2171 shares the bootstrap power supply in its high side secondary circuit with IR2137, which is the high voltage 3-phase gate driver IC with IGBT protection. Linear current sensing combined with the gate drive and IGBT protection function can be realized only by three pieces of silicon chips with simple 15V supply.

Output of IR2171 is a 35kHz digital PWM signal and is able to interface directly to the micro-controller's capture compare/timer unit. If other form of digital circuit is used such as a digital ASIC/gate array, then a simple timer to measure the PWM duty period can be easily implemented. Since it is an open drain output with 20mA driving capability, it can easily interface to the optically isolated device to achieve a galvanic isolation if needed.
In order to eliminate temperature drift more thoroughly, additional carrier frequency period measurement is recommended. If two measurement of duty and carrier period is concurrently performed, then temperature drift of gain and linearity can be wisely canceled. This due to the fact that temperature drift between two measurements tracks each other. For example, if a duty divided by a carrier period is performed, then resulting value can be used for temperature drift free variable inside of the AC drive function.

Since the input front-end circuit measures the small voltage across a shunt resistor in the IGBT driven PWM inverter circuit, it should be operational under any condition including short circuit condition. In particular, the input pin, VIN-, is designed to sustain up to negative 5V with respect to VS common pin. When input exceeds beyond +/-300mV, internal circuit naturally limits the final PWM waveform output to either 5% or 95% duty depending on the polarity of the input signal. Therefore, when used in the closed loop current control, it does not create abrupt discontinuity in the regulation.

TEST RESULTS

The first fabricated silicon device was tested and key parameters are obtained. Table 1 summarizes the key parameter performance data.

Linearity	0.4%
Linearity temperature drift	0.0003%
Total offset	1.5mV
Total offset temperature drift	30uV/°C
Gain error	1%
Gain error temperature drift	37ppm/°C
Power Supply Ripple Rejection	.06%@6kHz,1Vpp

Table 1: Key Parameters Performance Data

All temperature drift was derived over the range of [0 - 150°C]. Total offset was measured by shorting inputs and measuring PWM output duty at 25°C. Power supply ripple rejection was also measured by shorting inputs and measuring PWM output duty

fluctuation while a 1Vpp triangular ripple voltage (6kHz) was applied onto the 15V VB power supply. In realistic situation, the bootstrap power supply can be easily designed less than 1Vpp voltage fluctuation.

Further system test was conducted to verify more practical performance data by using the leading manufacturer's AC servo motor drive product. Comparison was made against the Hall Effect sensor, which is used to sense the 750W permanent magnet motor phase current for the closed loop vector control. This AC drive has a 1.3kHz current loop bandwidth with an 8kHz IGBT PWM carrier frequency. The current rating is 5A normal condition and 15A for overload condition.

For comparison purpose, the simple analog output circuit was constructed to convert IR2171 PWM output signal to analog voltage with a galvanic isolation by an opto-coupler device. Figure 5 shows the circuit basic schematic. Two bootstrap capacitor values are 4700PF.

Actual test waveforms are shown in Figure 6 and Figure 7. Although the original servo drive uses the Hall Effect sensor inside, it was removed and used as monitoring and comparison purpose. Instead, IR2171 was used for the closed loop control. The motor has more than two times of inertia load on its rotational shaft so that it creates substantial amount of current amplitude during acceleration and deceleration. Top traces are velocity waveform, which shows 40 msec acceleration and deceleration from 0 to 5000rpm. In Figure 7, the bottom trace actually contains two traces on top of each other. In Figure 8, two traces are separated and shown in different amplitude range.

FUTURE DIRECTION

Design and application of the new HVIC current sensing device have been discussed. Practical test result shows that it has a wide range of application for the motor drive covering from the standard AC drive to the servo drive application. 1200V version of same current sensing IC is also under development to serve the 460V AC drive application.

Further monolithic integration is also possible. Since the technology basis is essentially compatible with one that used in the HVIC gate driver, it is logical to integrate this current sensing function into the existing HVIC and combine these functions. Eventually it will be not so long that one chip intelligent IC to perform gate drive, IGBT protection, and linear current sensing altogether.

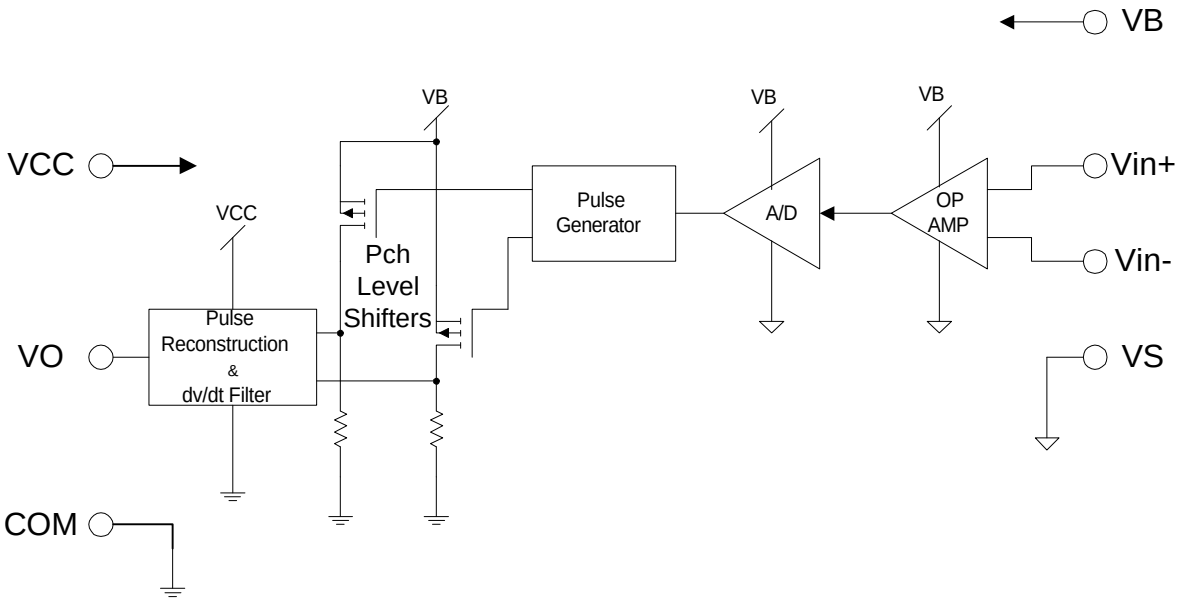


Figure 1: IR2171 Functional Block Diagram

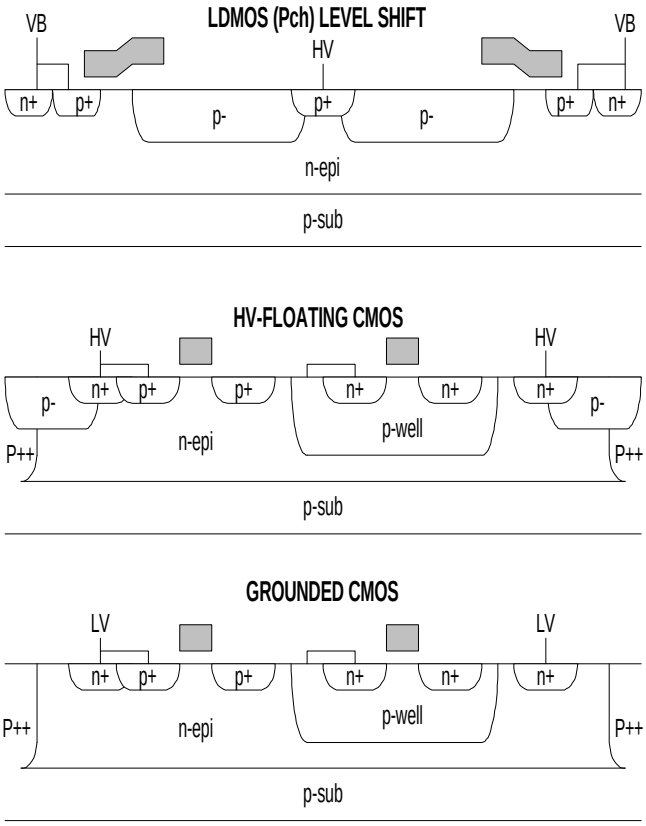


Figure 2: IR2171 Device Cross Sections

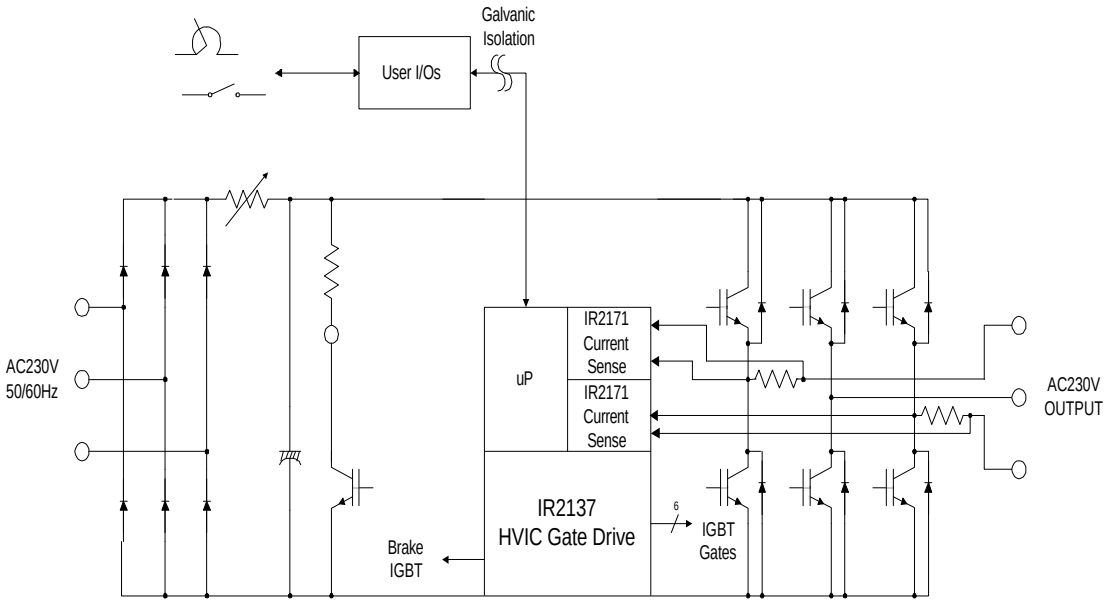


Figure 3: IR Power Conversion Processor ™ Architecture

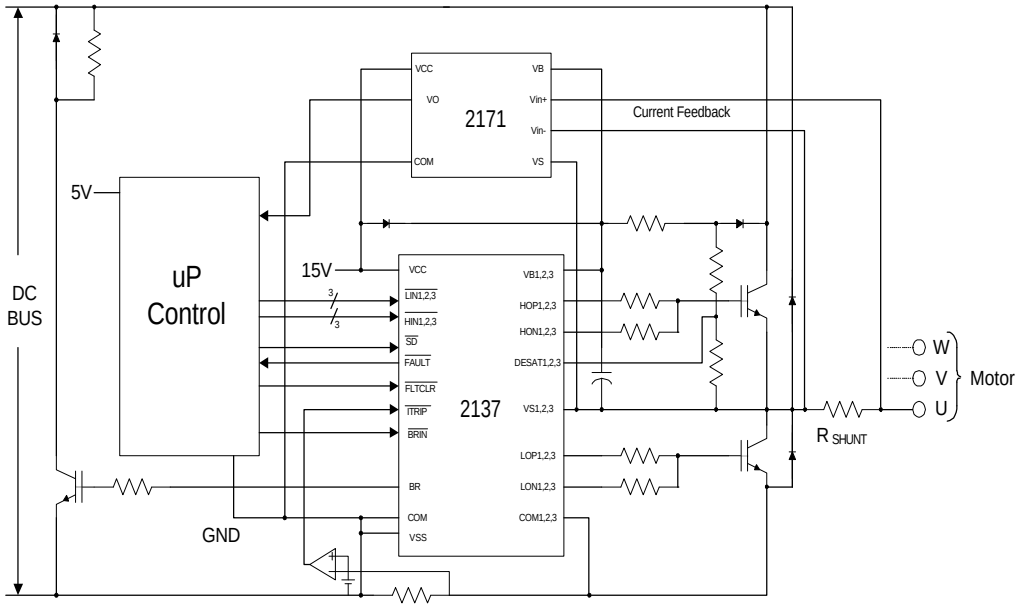


Figure 4: Companion Interface to HVIC Gate Drive

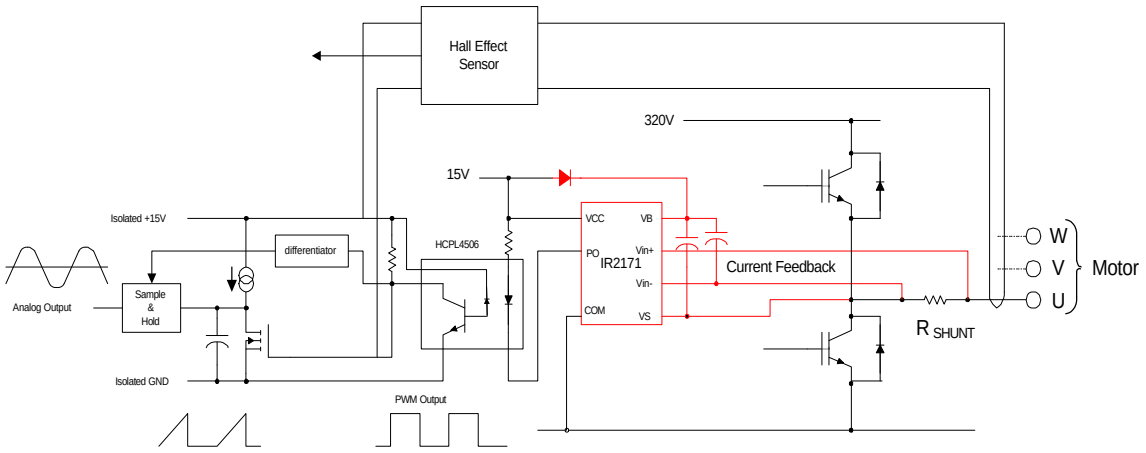


Figure 5: Servo Drive Closed Loop Current Control Test Circuit

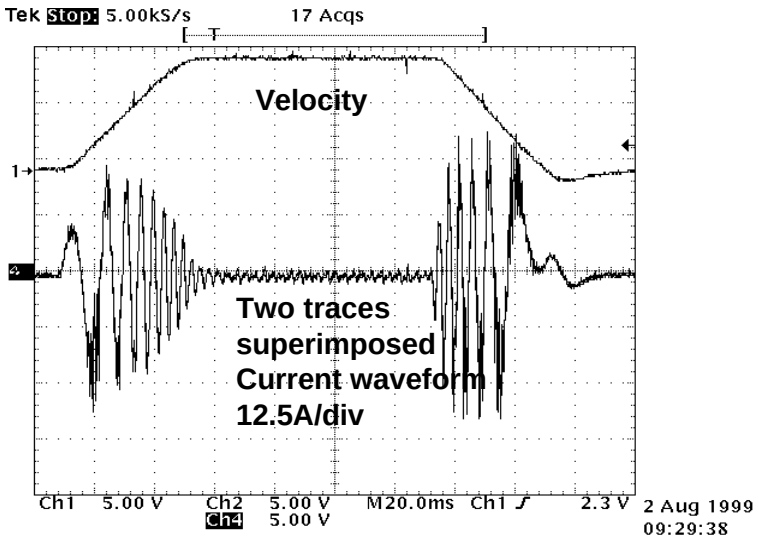


Figure 6: Fast Acceleration/Deceleration Current Waveform (superimposed)

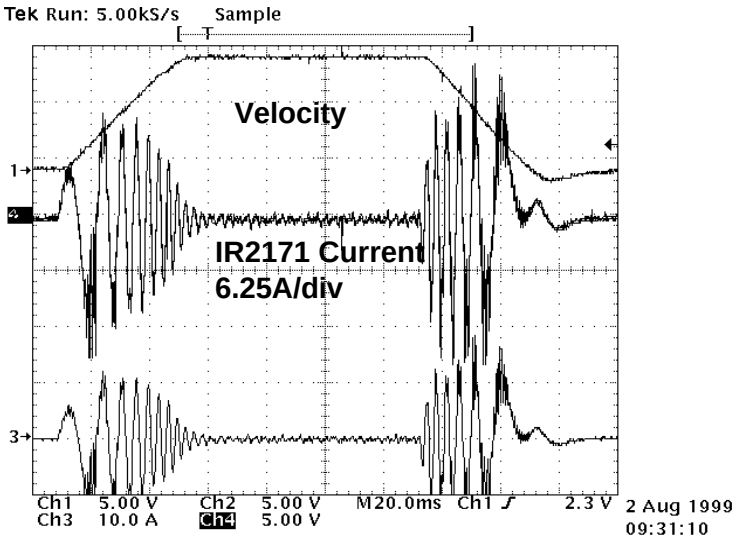


Figure 7: Fast Acceleration/Deceleration Current Waveform (separated)

Motor Drive and Inverter Designer's Manual





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CONTACT INFORMATION

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