HARRIS
S E M I C O N D U C T O R

DG201A, DG202

August 1997

Quad SPST, CMOS Analog Switches

Features

- **Input Signal Range** . . . . $\pm$**15V**
- **Low $r_{DS(ON)}$** . . . . $\leq$**175Ω**
- **TTL, CMOS Compatible**
- **Latch Proof**
- **True Second Source**
- **Maximum Supply Ratings** **44V**
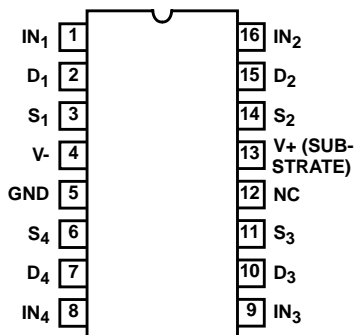- **Logic Inputs Accept Negative Voltages**

Description

The DG201A (normally open) and DG202 (normally closed) quad SPST analog switches are designed using Harris' 44V CMOS process. These bidirectional switches are latch-proof and feature break-before-make switching. Designed to block signals up to 30V_{P-P} in the OFF state, the DG201A and DG202 offer the advantages of low ON resistance ($\leq$175Ω), wide input signal range ($\pm$15V) and provide both TTL and CMOS compatibility.
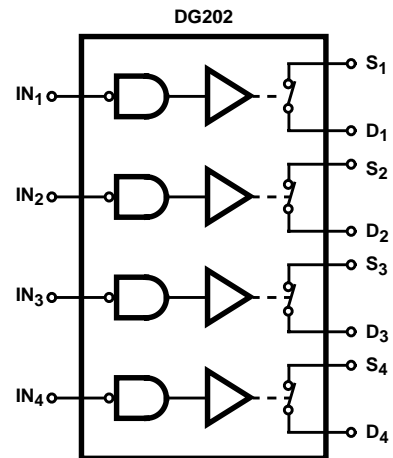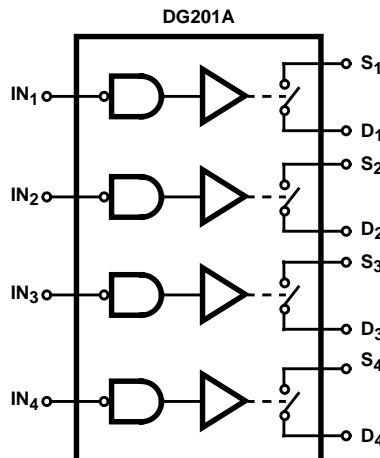
The DG201A and DG202 are specification and pinout compatible with the industry standard devices.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
DG201AAK	-55 to 125	16 Ld CERDIP	F16.3
DG201ABK	-25 to 85	16 Ld CERDIP	F16.3
DG201AAK/883B	-55 to 125	16 Ld CERDIP	F16.3
DG201ACK	0 to 70	16 Ld CERDIP	F16.3
DG201ACJ	0 to 70	16 Ld PDIP	E16.3
DG201ACY	0 to 70	16 Ld SOIC	M16.3
DG202AK	-55 to 125	16 Ld CERDIP	F16.3
DG202AK/883B	-55 to 125	16 Ld CERDIP	F16.3
DG202BK	-25 to 85	16 Ld CERDIP	F16.3
DG202CJ	0 to 70	16 Ld PDIP	E16.3

Pinout

**DG201A, DG202
(CERDIP, PDIP, SOIC)**
TOP VIEW

IN$_1$	1	16	IN$_2$
D$_1$	2	15	D$_2$
S$_1$	3	14	S$_2$
V-	4	13	V+ (SUB-STRATE)
GND	5	12	NC
S$_4$	6	11	S$_3$
D$_4$	7	10	D$_3$
IN$_4$	8	9	IN$_3$

Functional Block Diagrams

DG201A

DG202

NOTES:
1. Four SPST switches per package.
2. Switches shown for logic "1" input.

TRUTH TABLE

LOGIC	DG201A	DG202
0	ON	OFF
1	OFF	ON

Logic "0" $\leq$0.8V, Logic "1" $\geq$ 2.4V

File Number **3117.1**

Absolute Maximum Ratings

V+ to V- 44V
V- to Ground . . . .-25V
V_{IN} to Ground (Note 1). (V- -2V), (V+ +2V)
V_S or V_D to V+ (Note 1) . . . . +2, (V- -2V)
V_S or V_D to V- (Note 1) . . . .-2, (V+ +2V)
Current, any Terminal Except S or D .30mA
Continuous Current, S or D 20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max). . . .70mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
CERDIP Package	75	20
PDIP Package	100	N/A
SOIC Package	100	N/A

Maximum Junction Temperature
CERDIP Package . . . . 175°C
PDIP Package . . . . 150°C
Maximum Storage Temperature Range
C Suffix . . . .-65°C to 125°C
A and B Suffix . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on V_S, V_D, or V_{IN} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications   V+ = 15V, V- = -15V, GND = 0V, T_A = 25°C

PARAMETER	TEST CONDITIONS		DG201AA/DG202A			DG201AB, C/DG202B, C			UNITS
		MIN	(NOTE 3) TYP	MAX	MIN	(NOTE 3) TYP	MAX		
DYNAMIC CHARACTERISTICS									
Turn-On Time, t_{ON}	See Figure 1	-	480	600	-	480	-		ns
Turn-Off Time, t_{OFF}	See Figure 1	-	370	450	-	370	-		ns
Charge Injection, Q	C_L = 1000pF, R_S = 0, V_S = 0V	-	20	-	-	20	-		pC
Source OFF Capacitance, $C_{S(OFF)}$	f = 140kHz, V_{IN} = 5V, V_S = 0V	-	5.0	-	-	5.0	-		pF
Drain OFF Capacitance, $C_{D(OFF)}$	f = 140kHz, V_{IN} = 5V, V_D = 0V	-	5.0	-	-	5.0	-		pF
Channel ON Capacitance, $C_{D(ON)}$ + $C_{S(ON)}$	f = 140kHz, V_{IN} = 5V, V_S = V_D = 0V	-	16	-	-	16	-		pF
OFF Isolation, OIRR	V_{IN} = 5V, Z_L = 75Ω, V_S = 2.0V, f = 100kHz	-	70	-	-	70	-		dB
Crosstalk (Channel to Channel), CCRR		-	90	-	-	90	-		dB
INPUT									
Input Current with Voltage High, I_{INH}	V_{IN} = 2.4V	-1.0	-0.0004	-	-1.0	-0.0004	-		μA
	V_{IN} = 15V	-	0.003	1.0	-	0.003	1.0		μA
Input Current with Voltage Low, I_{INL}	V_{IN} = 0V	-1.0	-0.0004	-	-1.0	-0.0004	-		μA
SWITCH									
Analog Signal Range, V_{ANALOG}		-15	-	15	-15	-	15		V
Drain Source On Resistance, $r_{DS(ON)}$	V_D = ±10V, V_{IN} = 0.8V (DG201A) I_S = 1mA, V_{IN} = 2.4V (DG202)	-	115	175	-	115	200		Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{IN} = 2.4V (DG201A) V_{IN} = 0.8V (DG202) — V_S = 14V, V_D = -14V	-	0.01	1.0	-	0.01	5.0		nA
	V_S = -14V, V_D = 14V	-1.0	-0.02	-	-5.0	-0.02	-		nA
Drain OFF Leakage Current, $I_{D(OFF)}$	V_S = -14V, V_D = 14V	-	0.01	1.0	-	0.01	5.0		nA
	V_S = 14V, V_D = -14V	-1.0	-0.02	-	-5.0	-0.02	-		nA

Electrical Specifications   V+ = 15V, V- = -15V, GND = 0V, T_A = 25°C   **(Continued)**

PARAMETER	TEST CONDITIONS		DG201AA/DG202A			DG201AB, C/DG202B, C			UNITS
			MIN	(NOTE 3) TYP	MAX	MIN	(NOTE 3) TYP	MAX	
Drain ON Leakage Current, $I_{D(ON)}$ (Note 5)	V_{IN} = 0.8V (DG201A) V_{IN} = 2.4V (DG202)	$V_D = V_S$ = 14V	-	0.1	1.0	-	0.1	5.0	μA
		$V_D = V_S$ = -14V	-1.0	-0.15	-	-5.0	-0.15	-	μA
POWER SUPPLY CHARACTERISTICS									
Positive Supply Current, I+	All Channels ON or OFF		-	0.9	2	-	0.9	2	mA
Negative Supply Current, I-			-1	-0.3	-	-1	-0.3	-	mA

Electrical Specifications   V+ = 15V, V- = -15V, GND = 0V, T_A Over Operating Temperature Range

PARAMETER	TEST CONDITIONS		DG201AA/DG202A			DG201AB, C/DG202B, C			UNITS
			MIN	(NOTE 3) TYP	MAX	MIN	(NOTE 3) TYP	MAX	
INPUT									
Input Current with Voltage High, I_{INH}	V_{IN} = 2.4V		-10	-	-	-	-	-	μA
	V_{IN} = 15V		-	-	10	-	-	-	μA
Input Current with Voltage Low, I_{INL}	V_{IN} = 0V		-10	-	-	-	-	-	μA
SWITCH									
Analog Signal Range, V_{ANALOG}			-15	-	15	-	-	-	V
Drain Source On Resistance, $r_{DS(ON)}$	$V_D = \pm10V$, V_{IN} = 0.8V (DG201A) I_S = 1mA, V_{IN} = 2.4V (DG202)		-	-	250	-	-	-	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{IN} = 2.4V (DG201A) V_{IN} = 0.8V (DG202)	V_S = 14V, V_D = -14V	-	-	100	-	-	-	nA
		V_S = -14V, V_D = 14V	-100	-	-	-	-	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		V_S = -14V, V_D = 14V	-	-	100	-	-	-	nA
		V_S = 14V, V_D = -14V	-100	-	-	-	-	-	nA
Drain ON Leakage Current, $I_{D(ON)}$ (Note 5)	V_{IN} = 0.8V (DG201A) V_{IN} = 2.4V (DG202)	$V_D = V_S$ = 14V	-	-	200	-	-	-	μA
		$V_D = V_S$ = -14V	-200	-	-	-	-	-	μA

NOTES:

3. Typical values are for design aid only, not guaranteed and not subject to production testing.

4. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.

5. $I_{D(ON)}$ is leakage from driver into ON switch.
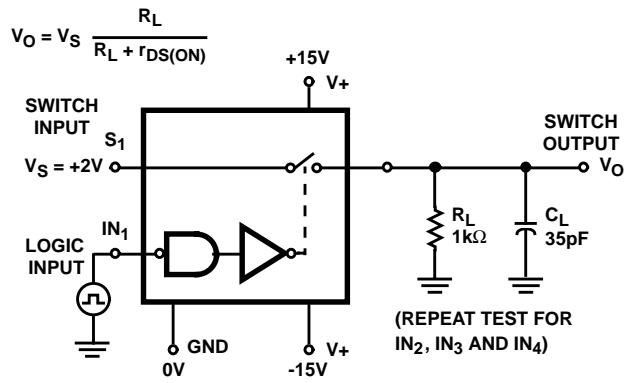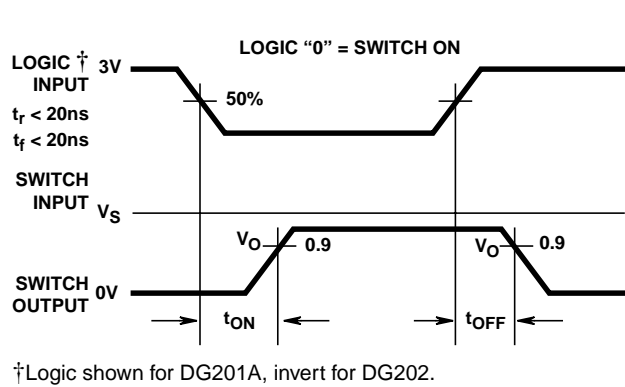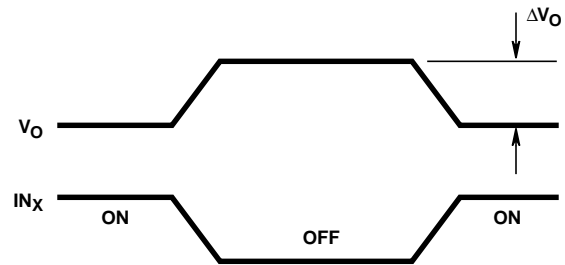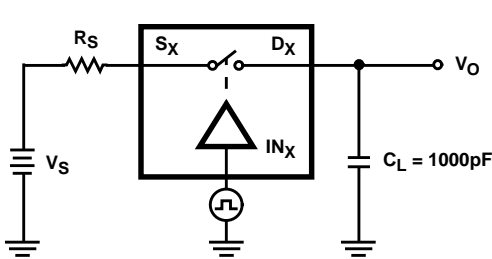
Test Circuits and Waveforms

†Logic shown for DG201A, invert for DG202.

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 1. t_{ON} AND t_{OFF} SWITCHING TEST CIRCUIT AND WAVEFORM

NOTES:

6. ΔV_O = Measured voltage error due to charge injection.

7. The error voltage in coulombs is $\Delta Q = C_L \times \Delta V_O$.

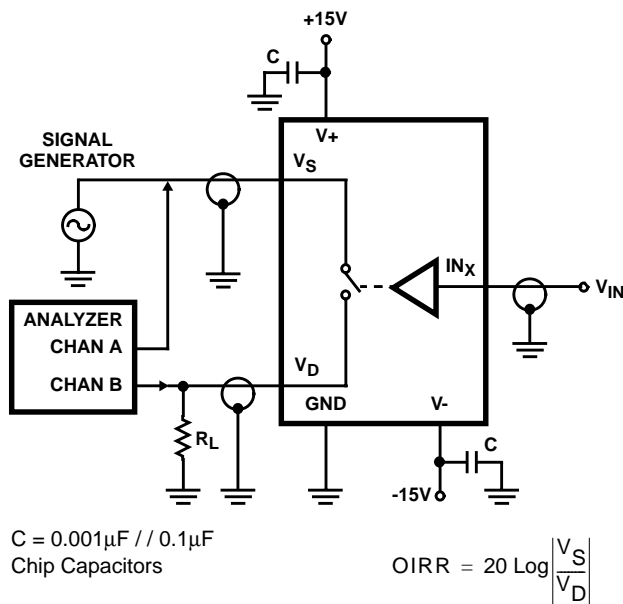**FIGURE 2. CHARGE INJECTION TEST CIRCUIT AND WAVEFORM**

C = 0.001μF // 0.1μF
Chip Capacitors

$$OIRR = 20 \, Log \left| \frac{V_S}{V_D} \right|$$

FIGURE 3. OFF ISOLATION TEST CIRCUIT

C = 0.001μF // 0.1μF
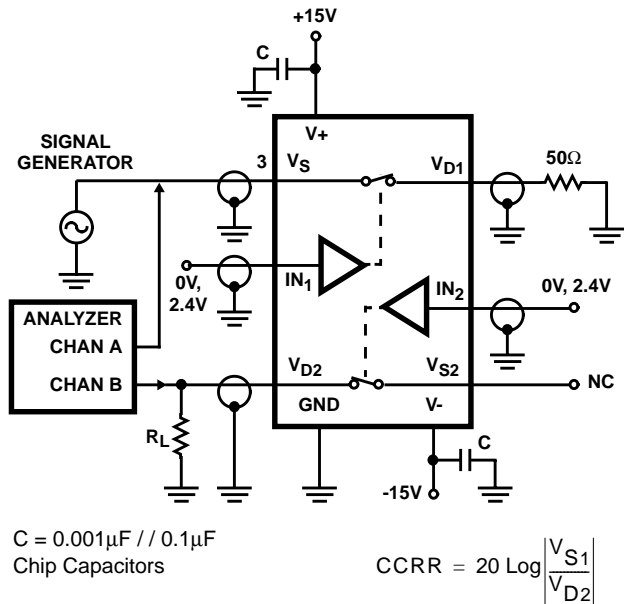Chip Capacitors

$$CCRR = 20 \, Log \left| \frac{V_{S1}}{V_{D2}} \right|$$

FIGURE 4. CHANNEL TO CHANNEL CROSSTALK TEST CIRCUIT