FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-28215-2E

ASSP For Video Applications

CMOS

8-bit 140 MSPS A/D Converter

MB40C318

■ DESCRIPTION

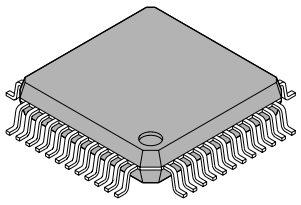
MB40C318 is a high-speed A/D converter using a fast CMOS technology.

■ FEATURES

- Resolution : 8 bit
- Linearity error : ±0.40% (standard)
- Maximum conversion rate : 140 MSPS (minimum)
- Power supply voltage : 3.3 V/5 V (standard: PECL clock input)
  3.3 V (standard: PECL other than clock input)
- Clock input voltage range : PECL level (140 MHz max differential input CLKEP, CLKEN)
  CMOS level (70 MHz max two-phase input CLKA, CLKB)
- Digital input voltage range CMOS level
- Digital output voltage range : CMOS level compatible
- Analog input voltage range : 0 to 3.0 V (2 Vp-p)
- Analog input capacitance : 22 pF (standard)
- Power dissipation : 300 mW (standard)
- Additional features : Reference voltage generator circuit: V_{REFT} = 3.0 V, V_{REFB} = 1.0 V
  High impedance output, power down function
  1:2 demultiplex output enable (RESET action enable)
  1/2 deviding clock output
  Cross sampling at 70 MHz (two-phase CLK) enable (CLKA, CLKB)
- Package : LQFP48 (7 mm × 7 mm, lead pitch 0.5 mm)

■ PACKAGE

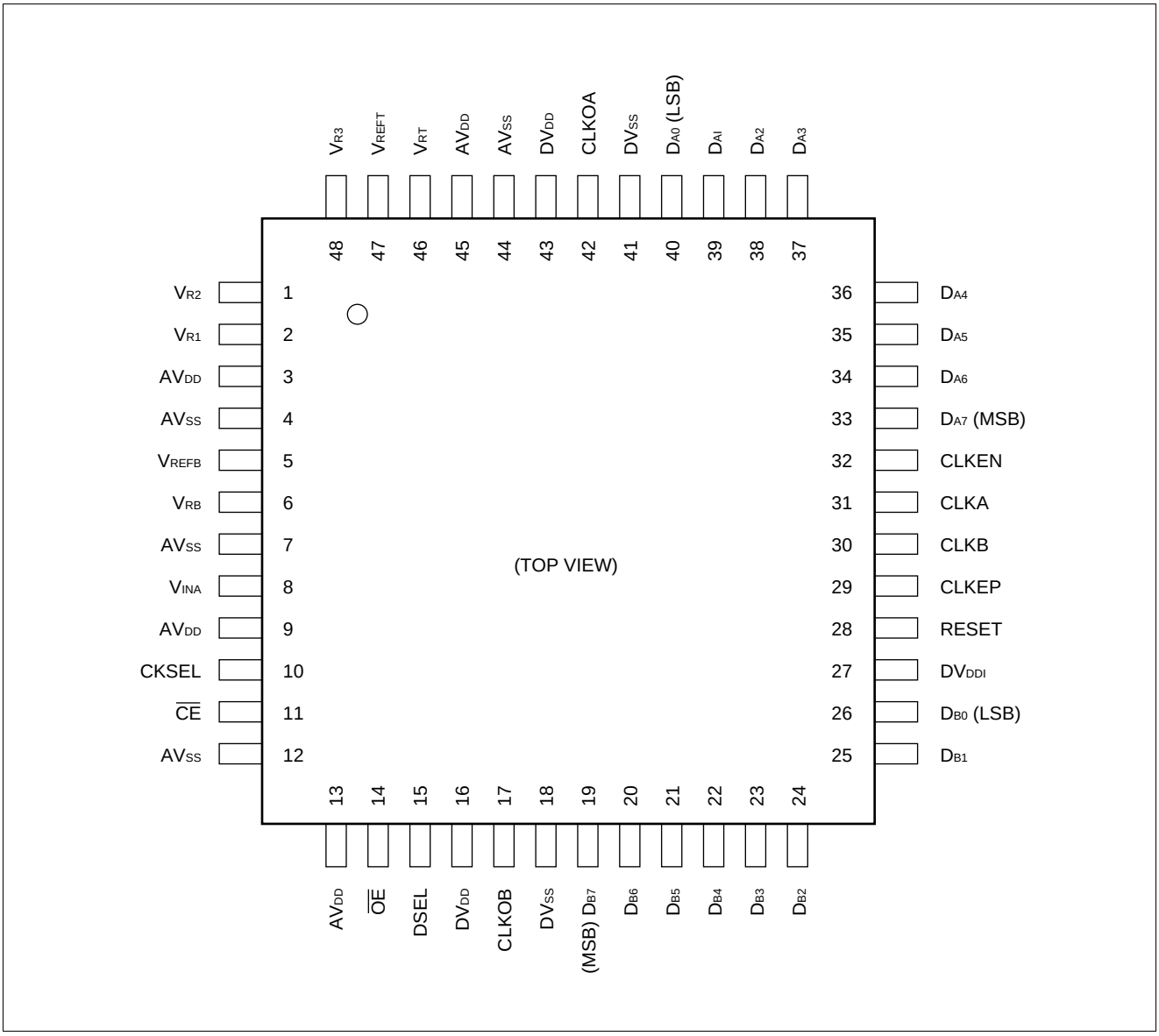
48-pin plastic LQFP



(FPT-48P-M05)

MB40C318

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin No.	Symbol	Description	
3, 9, 13, 45	AV_{DD}	Analog power supply (+3.3 V)	
16, 43	DV_{DD}	Digital power supply (+3.3 V)	
27	DV_{DDI}	Digital power supply for CLKEP/CLKEN (+5.0 V or +3.3 V)	
4, 7, 12, 44	AV_{SS}	Analog power supply ground pin (0 V)	
18, 41	DV_{SS}	Digital power supply ground pin (0 V)	
33 to 40	D_{A7} to D_{A0}	Digital output pin (Port A) D_{A7}: MSB, D_{A0}: LSB	
19 to 26	D_{B7} to D_{B0}	Digital output pin (Port B) D_{B7}: MSB, D_{B0}: LSB	
11	$\overline{CE}$	Power down at $\overline{CE}$ input “H” (internal pull-up resistor)	
14	$\overline{OE}$	Digital output (Both Port A, B) and clock output (CLKOA, CLKOB) are high impedance at $\overline{OE}$ input “H”.	
10	CKSEL	Mode of operation setting input pin (Refer to ■ MODE SETTING)	
15	DSEL		
28	RESET	Dividing circuit reset input pin (See ■ TIMING CHART 2, 3)	
29	CLKEP	Differential clock (positive-phase) input pin (max 140 MHz)	PECL level
32	CLKEN	Differential clock (negative-phase) input pin (max 140 MHz)	
31	CLKA	Two-phase clock (A ch) input pin (max 70 MHz)	CMOS level
30	CLKB	Two-phase clock (B ch) input pin (max 70 MHz)	
42	CLKOA	Clock output pin (See ■ TIMING CHART 1 to 4)	
17	CLKOB	Clock output pin (See ■ TIMING CHART 1 to 4)	
8	V_{INA}	Analog input pin Input range is V_{RT} to V_{RB} (0 V to 3.0 V: 2 Vp-p)	
2 1 48	V_{R1} V_{R2} V_{R3}	Reference 1/4 voltage output pin (Add 0.1 µF for AV_{SS}) Reference 1/2 voltage output pin (Add 0.1 µF for AV_{SS}) Reference 3/4 voltage output pin (Add 0.1 µF for AV_{SS})	
46	V_{RT}	Reference voltage input pin on top side	
47	V_{REFT}	Reference voltage output pin By connecting to V_{RT}, $0.9 \times AV_{DD}$ ($\fallingdotseq$ 3 V) is generated.	
6	V_{RB}	Reference voltage input pin on bottom side	
5	V_{REFB}	Reference voltage output pin By connecting to V_{RB}, $0.3 \times AV_{DD}$ ($\fallingdotseq$ 1 V) is generated.	

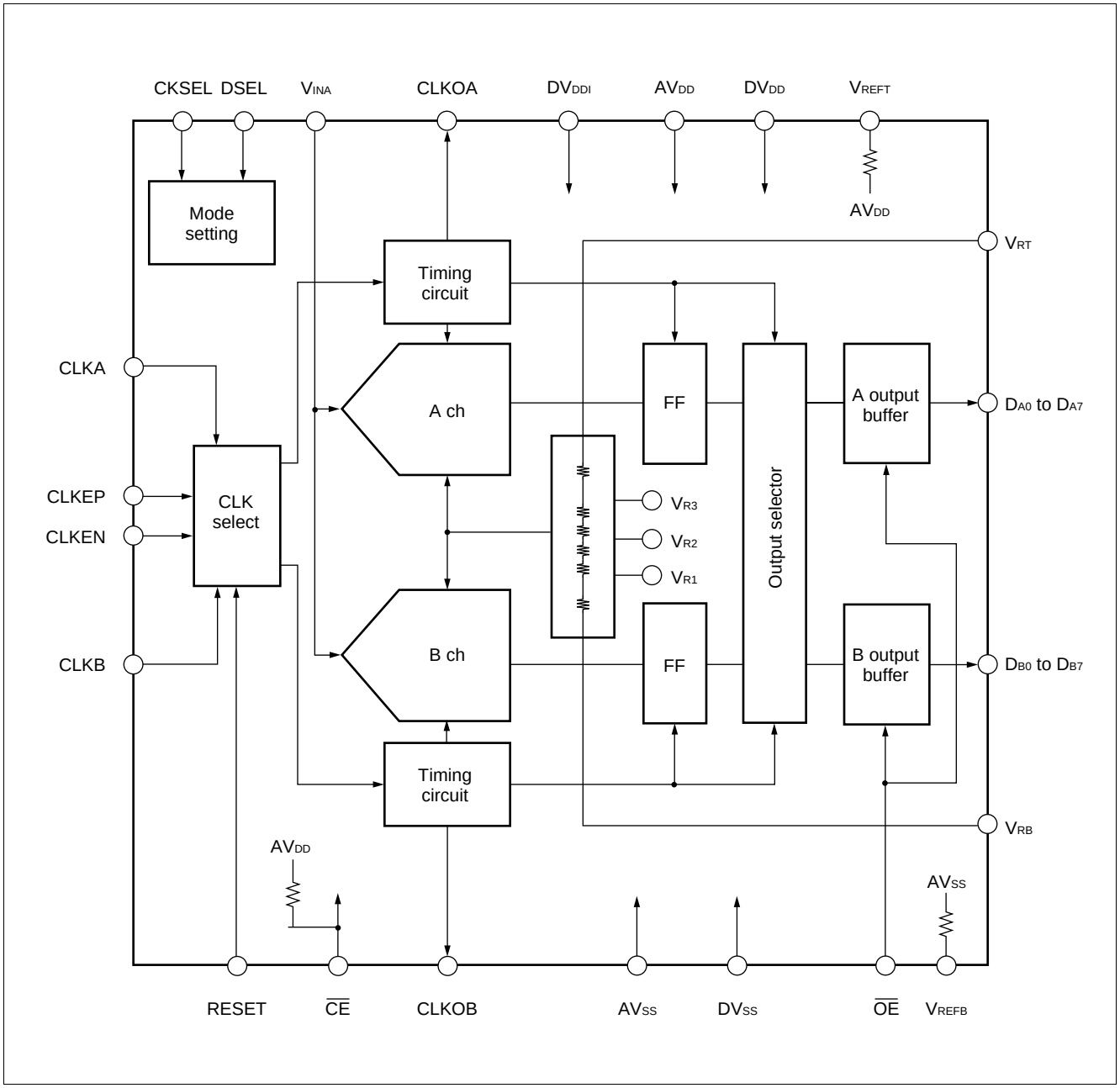
The values in parentheses are standard.

■ PRECAUTIONS ON USE

- Be sure to ground the pins of AV_{DD}, DV_{DD}, DV_{DDI}, V_{RT}, V_{RB}, V_{R1}, V_{R2}, and V_{R3} via high-frequency capacitor. Place the high-frequency capacitor as close as possible to the pin.
- To avoid generation of undesired current owing to indetermination of internal logic, set $\overline{CE}$ to “H” at powering on and input more than five clock pulses just after operation ($\overline{CE}$: “H” $\rightarrow$ “L”).

MB40C318

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	AV_{DD}, DV_{DD}	–0.3	+4.0	V
	DV_{DDI}	–0.3	+7.0	V
Input/output voltage	V_{INA}, V_{RT}, V_{RB}, V_{REFT}, V_{REFB}, V_{R1}, V_{R2}, V_{R3}, $\overline{CE}$, CKSEL	–0.3	AV_{DD}+0.3*1	V
	D_{A0} to D_{A7}, D_{B0} to D_{B7}, CLKOA, CLKOB, CLKA, $\overline{CLKB}$, DSEL, $\overline{OE}$, RESET	–0.3	DV_{DD}+0.3*1	V
	CLKEP, CLKEN	–0.3	DV_{DDI}+0.3*2	V
Storage temperature	T_{STG}	–55	+125	°C

*1: Do not exceed +4.0 V.
*2: Do not exceed +7.0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage		AV_{DD}, DV_{DD}	3.00	3.30	3.60	V
		DV_{DDI} (5 V)	4.75	5.00	5.25	V
		DV_{DDI} (3 V)	3.00	3.30	3.60	V
Analog input voltage		V_{INA}	V_{RB}	—	V_{RT}	V
Analog reference voltage: T		V_{RT}	—	—	3.00	V
Analog reference voltage: B		V_{RB}	0.00	—	—	V
Analog reference voltage range		$V_{RT} – V_{RB}$	1.90	2.00	2.10	V
Digital “H” level input voltage	CKSEL, $\overline{CE}$	V_{IHD}	$AV_{DD} – 0.5$	—	—	V
	$\overline{OE}$, DSEL, RESET, CLKA, CLKB		$DV_{DD} – 0.5$	—	—	V
	CLKEP, CLKEN (DV_{DDI} = 5 V)		$DV_{DDI} – 1.1$	—	$DV_{DDI} – 0.6$	V
	CLKEP, CLKEN (DV_{DDI} = 3.3 V)		$DV_{DDI} – 0.5$	—	DV_{DDI}	V
Digital “L” level input voltage	CKSEL, $\overline{CE}$	V_{ILD}	—	—	0.5	V
	$\overline{OE}$, DSEL, RESET, CLKA, CLKB		—	—	0.5	V
	CLKEP, CLKEN (DV_{DDI} = 5 V)		$DV_{DDI} – 2.0$	—	$DV_{DDI} – 1.45$	V
	CLKEP, CLKEN (DV_{DDI} = 3.3 V)		2.3	—	$DV_{DDI} – 0.5$	V
Digital input voltage range	CLKEP, CLKEN (DV_{DDI} = 5 V)	$V_{IHD} – V_{ILD}$	0.4	0.8	—	V
	CLKEP, CLKEN (DV_{DDI} = 3.3 V)		0.4	0.6	—	V
Digital input current		I_{ID}	–20	—	5	µA
Differential clock frequency		f_{CLKEP}, f_{CLKEN}	0.1	—	140	MHz
Two-phase clock frequency		f_{CLKA}, f_{CLKB}	0.1	—	70	MHz
Minimum clock pulse width (differential)		t_{WS}^+, t_{WS}^-	3.0	3.5	—	ns
Minimum clock pulse width (two-phase)		t_{WD}^+, t_{WD}^-	6.0	7.0	—	ns
Clock pulse rising/falling time		t_r, t_f	—	2.0	—	ns
RESET signal setup time		t_s	1.5	—	—	ns
RESET signal hold time		t_h	1.5	—	—	ns
Operating temperature range		Ta	–20	—	70	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics in Analog Section

(AV_{DD} = DV_{DD} = 3.00 V to 3.60 V, DV_{DDI} = 4.75 V to 5.25 V, Ta = –20°C to +70°C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Resolution	—	—	8	—	bit
Linearity error	LE	—	±0.40	±0.6	%
Differential linearity error	DLE	—	±0.20	±0.36	%
Analog input capacity	C_{INA}	—	22	—	pF
Reference voltage: T	V_{REFT}	0.88 × AV_{DD}	0.91 × AV_{DD}	0.94 × AV_{DD}	V
Reference voltage: B	V_{REFB}	0.27 × AV_{DD}	0.3 × AV_{DD}	0.33 × AV_{DD}	V
Reference current	I_{RB}	–15	–10	—	mA
Analog supply current	AI_{DD}	—	60.0	100	mA
Digital supply current	DI_{DD}	—	30.0	45	mA
	DI_{DDI}	—	1	3	mA
Standby current	I_{SB}	—	1	—	mA

• DC Characteristics in Digital Section

(AV_{DD} = DV_{DD} = 3.00 V to 3.60 V, DV_{DDI} = 4.75 V to 5.25 V, Ta = –20°C to +70°C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Digital “H” level output voltage	V_{OHD}	DV_{DD} – 0.4	—	DV_{DD}	V
Digital “L” level output voltage	V_{OLD}	—	—	0.4	V
Digital “H” level output current	I_{OHD}	–400	—	—	µA
Digital “L” level output current	I_{OLD}	—	—	1.6	mA

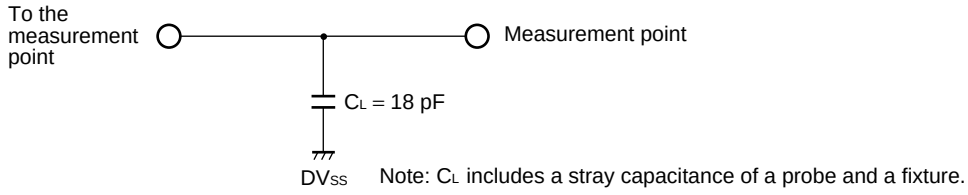
MB40C318

• Switching Characteristics

(AV_{DD} = DV_{DD} = 3.00 V to 3.60 V, DV_{DDI} = 4.75 V to 5.25 V, Ta = –20°C to +70°C)

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Maximum conversion rate		f_S	140	—	—	MSPS
Aperture time	Timing chart 1 to 3	t_{AD}	—	3.5	—	ns
	Timing chart 4		—	2.0	—	ns
Digital output delay time	Timing chart 1	t_{pdS}	4	8	11.5	ns
		t_{pdSO}	t_{WS}^+ + 4	t_{WS}^+ + 8	t_{WS}^+ + 11	ns
	Timing chart 2	t_{pdM1}	4	7	11.5	ns
		t_{pdM1O}	T + 4	T + 7	T + 11	ns
	Timing chart 3	t_{pdM2}	4	7	11.5	ns
		t_{pdM2O}	T + 4	T + 7	T + 11	ns
	Timing chart 4	t_{pdD}	3	6	10.5	ns
		t_{pdDO}	t_{WD}^+ + 2	t_{WD}^+ + 6	t_{WD}^+ + 10	ns

■ DIGITAL OUTPUT BUFFER LOAD CIRCUIT



Note: C_L includes a stray capacitance of a probe and a fixture.

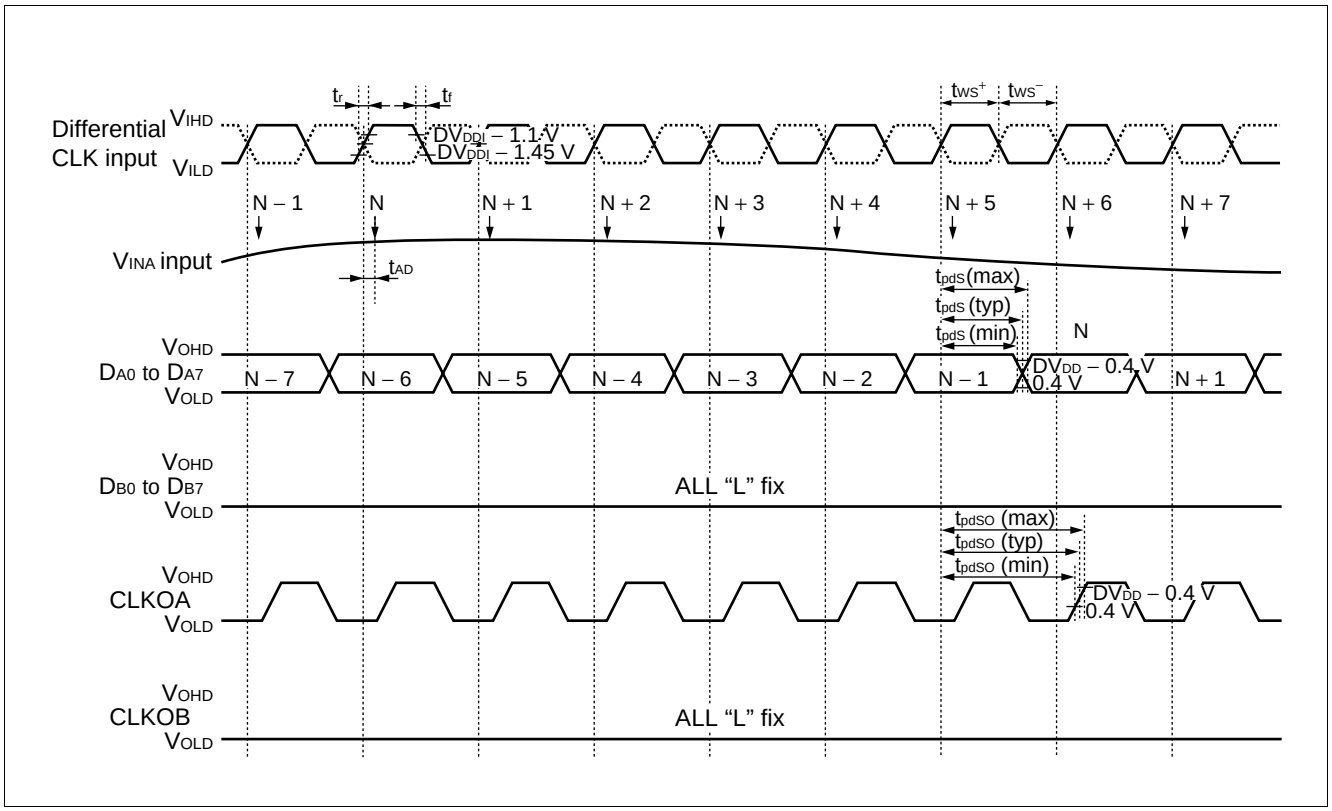
■ MODE SETTING

CKCEL	DCEL	Mode	Timing Chart
H	H	Differential CLK input-straight output mode	Timing chart 1
H	L	Differential CLK input-demultiplex output (in-phase) mode	Timing chart 2
L	H	Differential CLK input-demultiplex output (two-phase) mode	Timing chart 3
L	L	Two-phase CLK input mode (CLKA, CLKB)	Timing chart 4

■ TIMING CHART 1

Differential CLK input-straight output mode

- CLKEP = CLKEN = 140 MHz (max)
- CLKA = CLKB = “L” (DV_{SS})
- CKSEL = “H” (AV_{DD})
- DSEL = “H” (DV_{DD})
- RESET = “H” (DV_{DD})
- $\overline{CE}$ = “L” (AV_{SS})
- $\overline{OE}$ = “L” (DV_{SS})



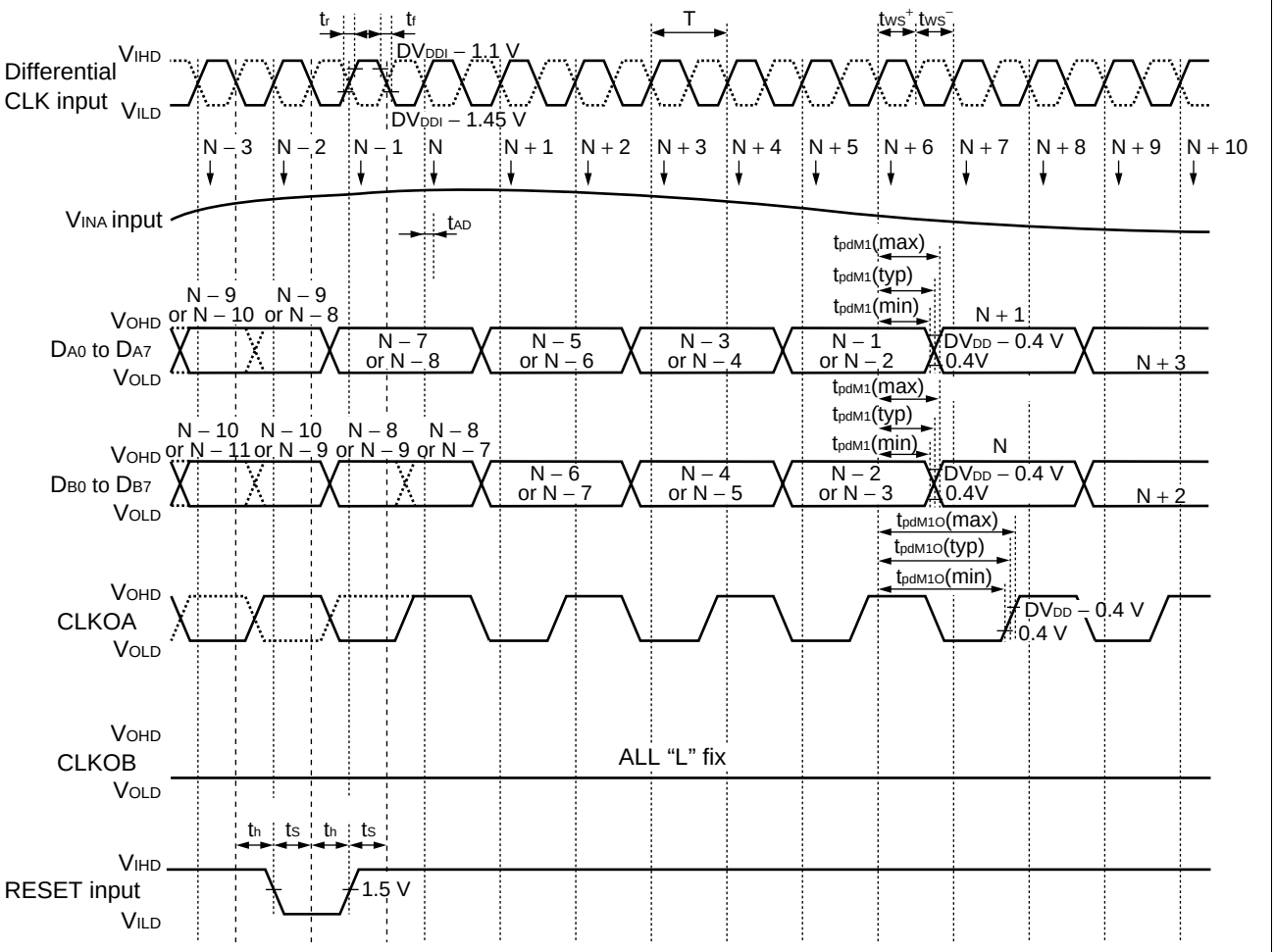
- Differential CLK input — Solid line: CLKEP, Dotted line: CLKEN
- V_{INA} input — Sampling at CLKEP rising (CLKEN falling)
- D_{A0} to D_{A7} — Output (after 5 CLK + t_{pdS} from Sampling) at CLKEP rising (CLKEN falling)

MB40C318

■ TIMING CHART 2

Differential CLK input-demultiplex output (in-phase) mode

- CLKEP = CLKEN = 140 MHz (max)
- CLKA = CLKB = “L” (DV_{SS})
- CKSEL = “H” (AV_{DD})
- DSEL = “L” (DV_{SS})
- $\overline{CE}$ = “L” (AV_{SS})
- $\overline{OE}$ = “L” (DV_{SS})

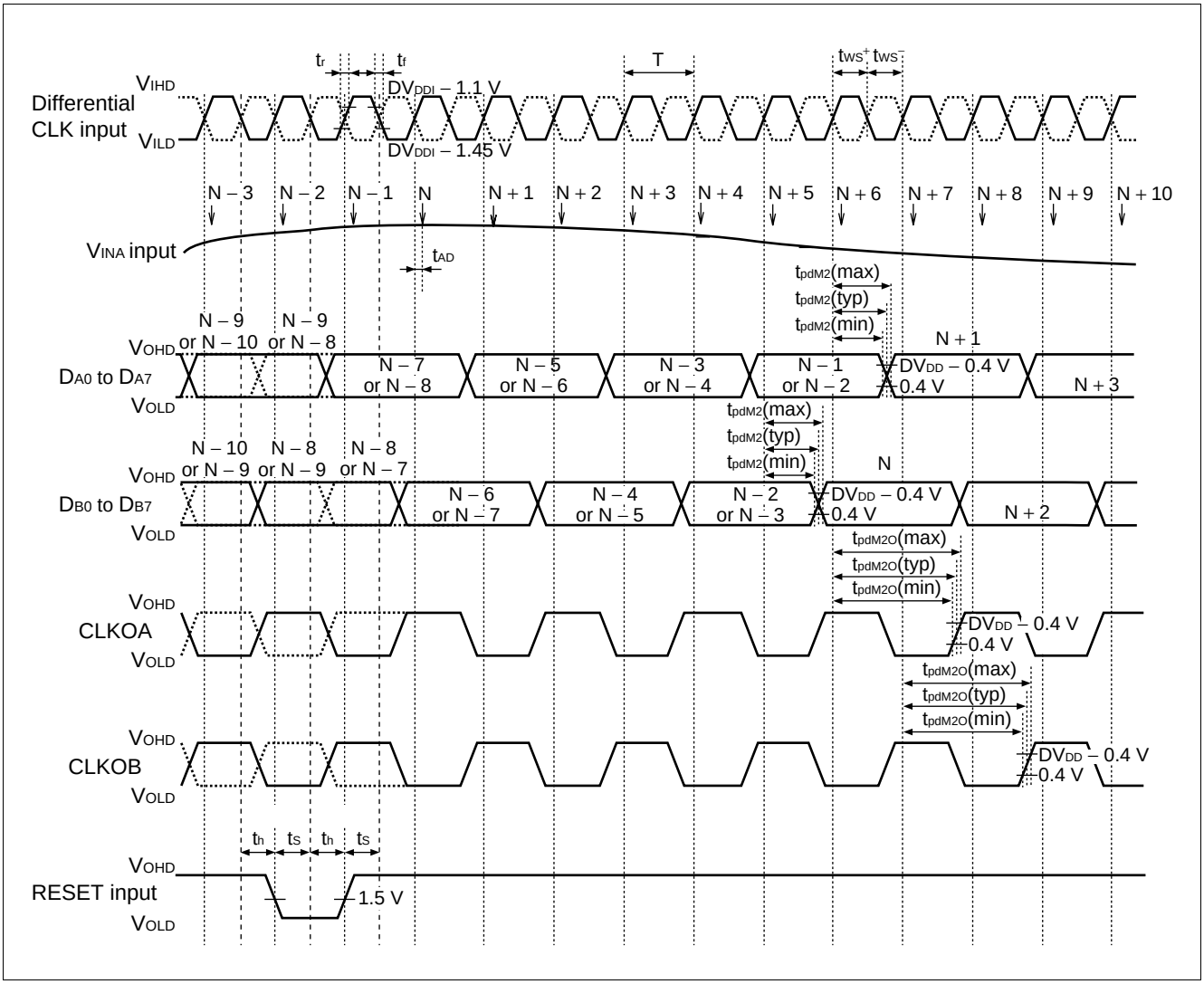


- Differential CLK input — Solid line: CLKEP, Dotted line: CLKEN
- V_{INA} input — Sampling at CLKEP rising (CLKEN falling)
- D_{A0} to D_{A7} — Output (after 5 CLK + t_{pdM1} from Sampling) at CLKEP rising (CLKEN falling)
- D_{B0} to D_{B7} — Output (after 6 CLK + t_{pdM1} from Sampling) at CLKEP rising (CLKEN falling)

■ TIMING CHART 3

Differential CLK input-demultiplex output (two-phase) mode

- CLKEP = CLKEN = 140 MHz (max)
- CLKA = CLKB = “L” (DV_{SS})
- CKSEL = “L” (AV_{SS})
- DSEL = “H” (DV_{DD})
- $\overline{CE}$ = “L” (AV_{SS})
- $\overline{OE}$ = “L” (DV_{SS})

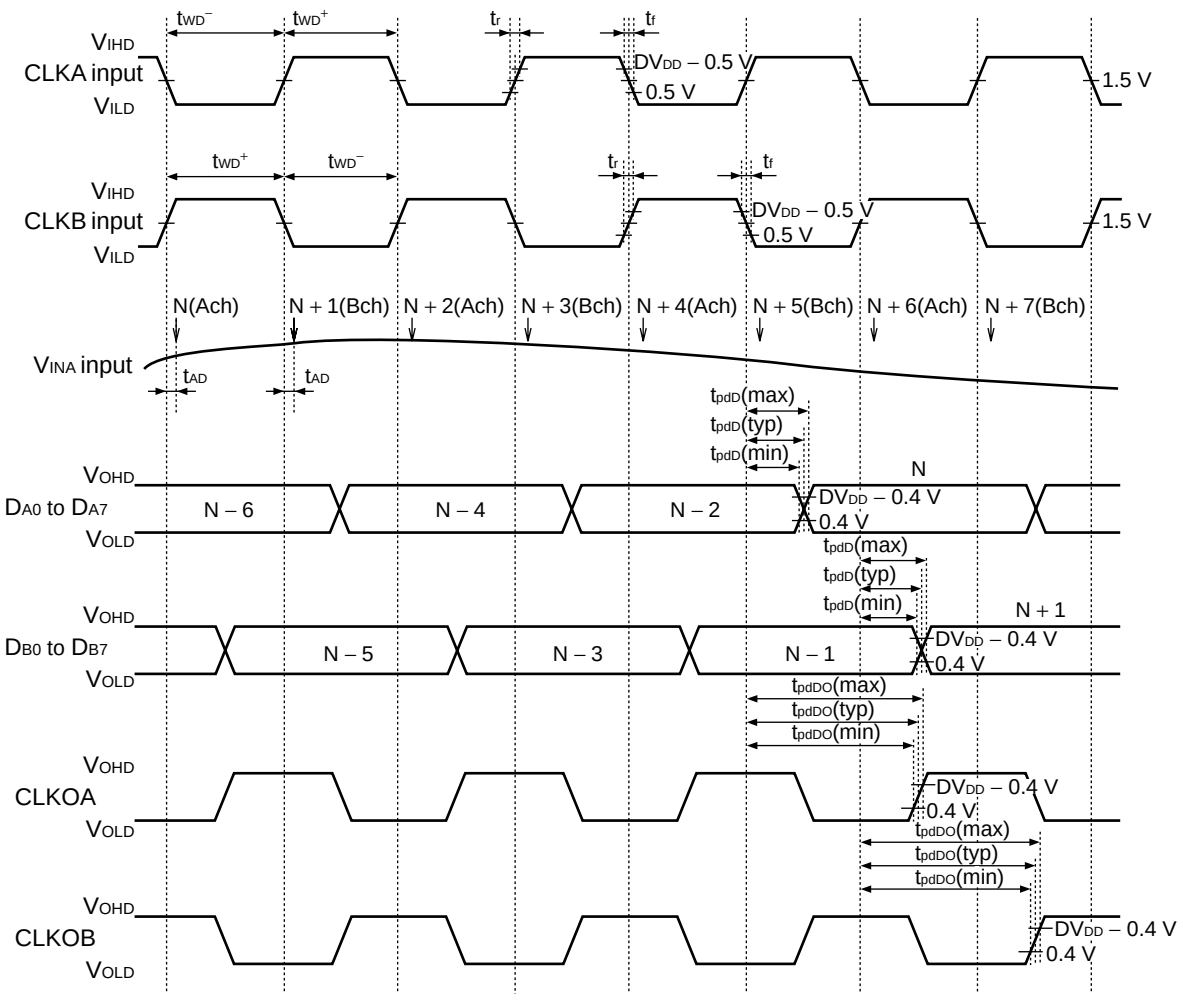


- Differential CLK input — Solid line: CLKEP, Dotted line: CLKEN
- V_{INA} input — Sampling at CLKEP rising (CLKEN falling)
- D_{A0} to D_{A7} — Output (after 5 CLK + t_{pdM2} from Sampling) at CLKEP rising (CLKEN falling)
- D_{B0} to D_{B7} — Output (after 5 CLK + t_{pdM2} from Sampling) at CLKEP rising (CLKEN falling)

■ TIMING CHART 4

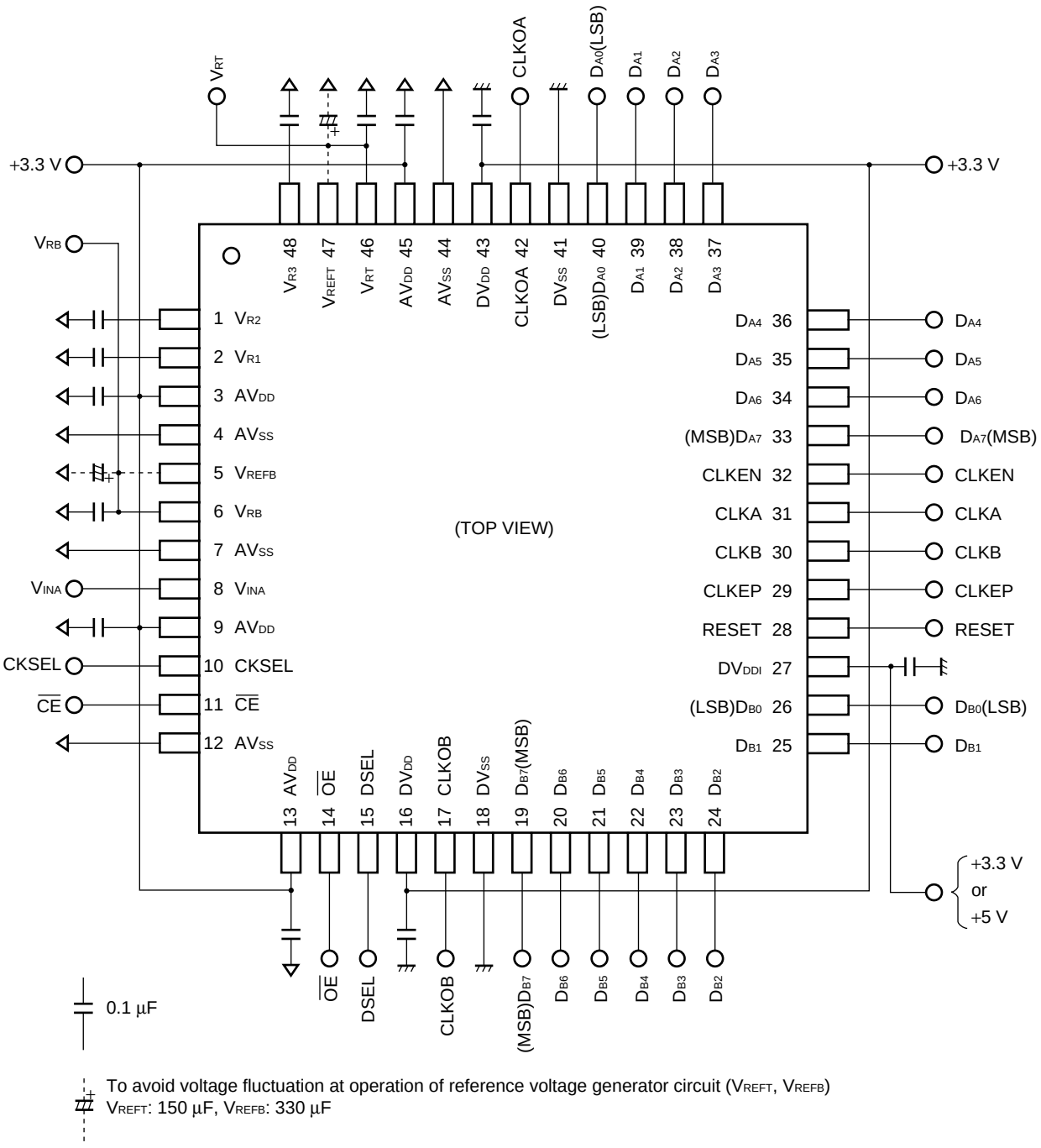
Two-phase CLK input mode (CLKA, CLKB)

- $DV_{DDI} = DV_{DD}$
- CLKEP = “L” (DV_{SS}), CLKEN = “H” (DV_{DD}) or CLKEP = “H” (DV_{DD}), CLKEN = “L” (DV_{SS})
- CLKA = CLKB = 70 MHz (max)
- CKSEL = “L” (AV_{SS})
- DSEL = “L (DV_{SS})
- RESET = “H” (DV_{DD}) or RESET = “L” (DV_{SS})
- $\overline{CE}$ = “L” (AV_{SS})
- $\overline{OE}$ = “L” (DV_{SS})



- V_{INA} input — Sampling (A ch) at CLKA falling
  Sampling (B ch) at CLKB falling
- D_{A0} to D_{A7} — Output (after 2.5 CLK + t_{pdD} from Sampling) at CLKA rising
- D_{B0} to D_{B7} — Output (after 2.5 CLK + t_{pdD} from Sampling) at CLKB rising

■ TYPICAL CONNECTION EXAMPLE



■ ORDERING INFORMATION

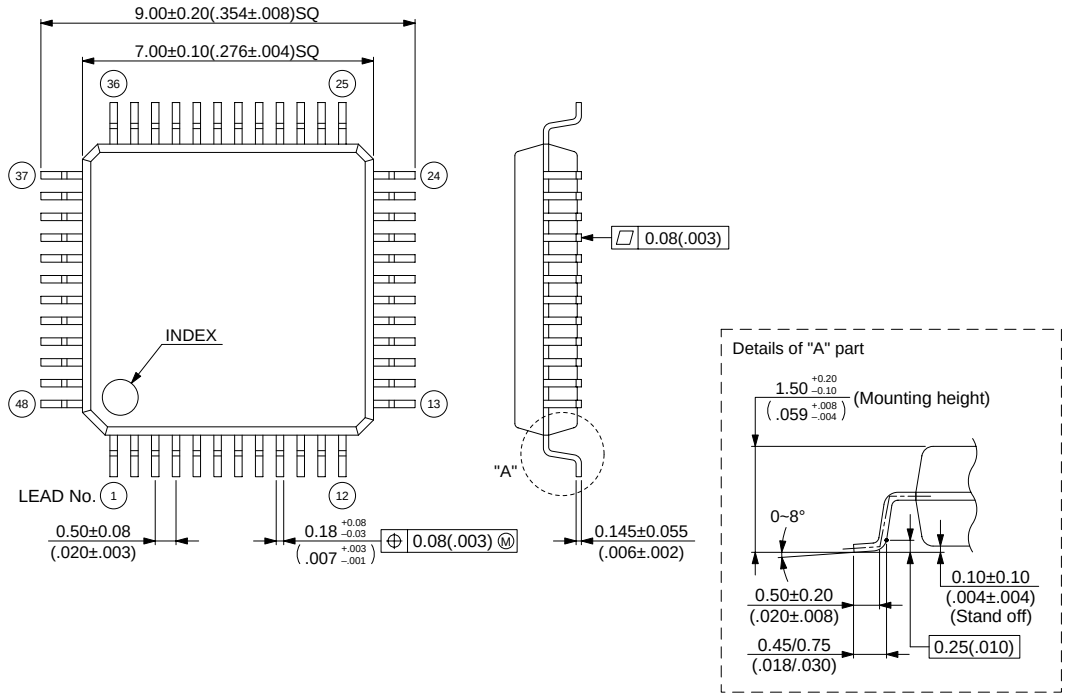
Part number	Package	Remark
MB40C318PFV	48-pin Plastic LQFP (FPT-48P-M05)	

MB40C318

■ PACKAGE DIMENSION

48-pin Plastic LQFP
(FPT-48P-M05)

Note) Pins width and pins thickness include plating thickness.



Dimensions in mm (inches).

MB40C318

FUJITSU LIMITED

For further information please contact:

Japan
FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka,
Nakahara-ku, Kawasaki-shi,
Kanagawa 211-8588, Japan
Tel: +81-44-754-3763
Fax: +81-44-754-3329

http://www.fujitsu.co.jp/

North and South America
FUJITSU MICROELECTRONICS, INC.
3545 North First Street,
San Jose, CA 95134-1804, USA
Tel: +1-408-922-9000
Fax: +1-408-922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: +1-800-866-8608
Fax: +1-408-922-9179

http://www.fujitsumicro.com/

Europe
FUJITSU MICROELECTRONICS EUROPE GmbH
Am Siebenstein 6-10,
D-63303 Dreieich-Buchschlag,
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

http://www.fujitsu-fme.com/

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE LTD
#05-08, 151 Lorong Chuan,
New Tech Park,
Singapore 556741
Tel: +65-281-0770
Fax: +65-281-0220

http://www.fmap.com.sg/

F0001

The contents of this document are subject to change without notice.
Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The contents of this document may not be reproduced or copied without the permission of FUJITSU LIMITED.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipments, industrial, communications, and measurement equipments, personal or household devices, etc.).
CAUTION:
Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.