FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27226-1E

ASSP For Power Management Applications

2-channel DC/DC Converter IC
with Synchronous Rectifier

MB3882

■ DESCRIPTION

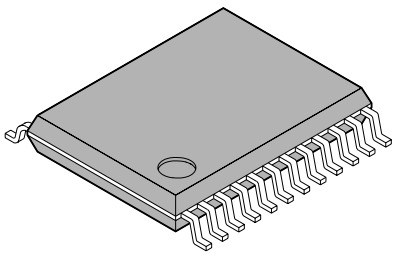
The MB3882 is a 2-channel DC/DC converter IC using pulse width modulation (PWM) and synchronous rectification, designed for down conversion applications.
This device is a power supply with high output drive capacity. Synchronous rectification also provides for high efficiency.
In addition, a 5 V regulator is built in to reduce the number of system components. The result is an ideal built-in power supply for driving products with high speed CPU's such as home TV game devices and notebook PC's.

■ FEATURES

- Synchronous rectification for high efficiency
- Supply voltage range : 5.5 V to 18 V
- High-precision reference voltage : 2.5 V ± 1%
- Error Amp. threshold voltage : 1.25 V ± 1% (0 °C to 85 °C)
- Oscillator frequency range : 10 kHz to 500 kHz
- Built-in soft start circuit with error Amp. input control
- Totem pole type output for N-ch MOSFET

■ PACKAGE

24-pin Plastic SSOP

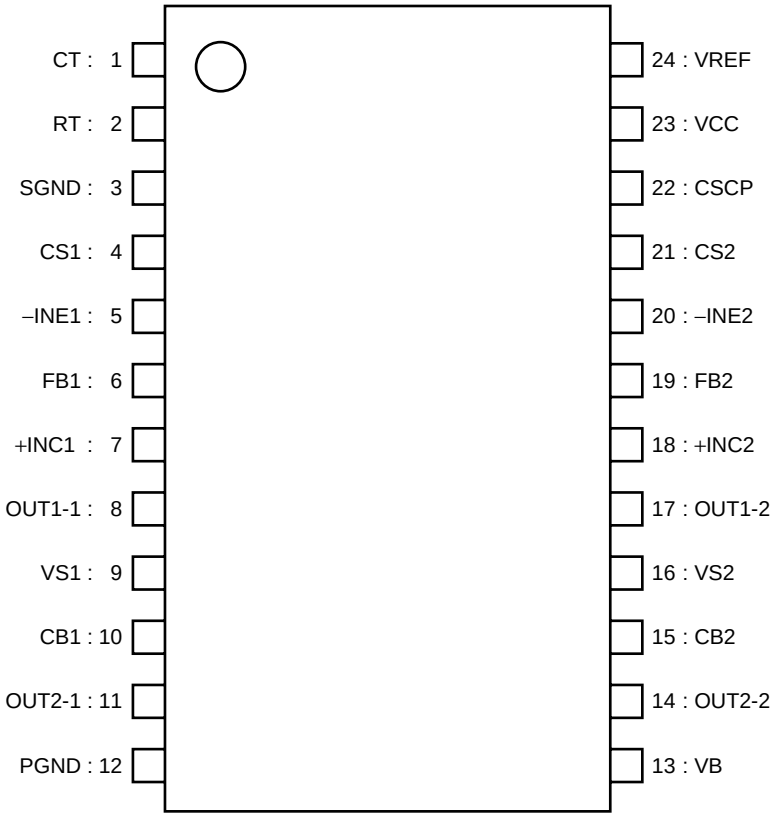


(FPT-24P-M03)

MB3882

■ PIN ASSIGNMENTS

(TOP VIEW)



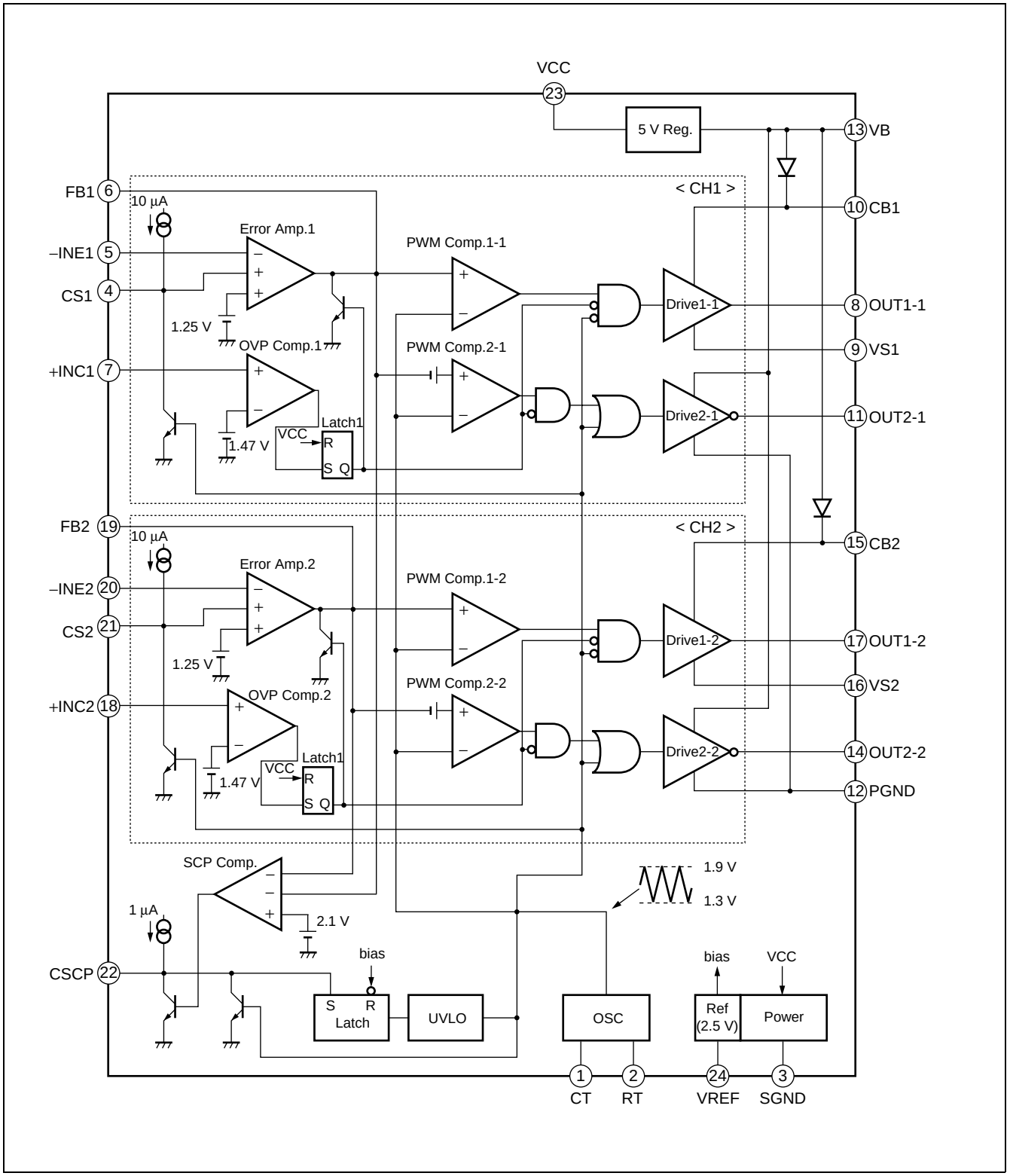
(FPT-24P-M03)

■ PIN DESCRIPTIONS

Pin No.	Symbol	I/O	Description
1	CT	—	Triangular wave oscillator frequency setting capacitor connection terminal
2	RT	—	Triangular wave oscillator frequency setting resistor connection terminal
3	SGND	—	Ground terminal
4	CS1	—	CH1 soft start capacitor connection terminal. (Also used as channel control)
5	–INE1	I	CH1 error Amp. inverted input terminal
6	FB1	O	CH1 error Amp. output terminal
7	+INC1	I	CH1 overvoltage comparator non-inverted input terminal
8	OUT1-1	O	CH1 totem pole output terminal. (External main side FET gate drive)
9	VS1	—	CH1 external main side FET source connection terminal
10	CB1	—	CH1 boot capacitor connection terminal. Connect capacitor between the CB1 terminal and VS1 terminal.
11	OUT2-1	O	CH1 totem pole output terminal. (External synchronous rectifier side FET gate drive)
12	PGND	—	Ground terminal
13	VB	O	Output circuit bias output terminal
14	OUT2-2	O	CH2 totem pole output terminal. (External synchronous rectifier side FET gate drive)
15	CB2	—	CH2 boot capacitor connection terminal. Connect capacitor between the CB2 terminal and VS2 terminal.
16	VS2	—	CH2 external main side FET source connection terminal.
17	OUT1-2	O	CH2 totem pole output terminal. (External main side FET gate drive)
18	+INC2	I	CH2 overvoltage comparator non-inverted input terminal
19	FB2	O	CH2 error Amp. output terminal
20	–INE2	I	CH2 error Amp. inverted input terminal
21	CS2	—	CH2 soft start capacitor connection terminal. (Also used as channel control)
22	CSCP	—	Timer latch short protection capacitor connection terminal
23	VCC	—	Reference voltage, control circuit power supply terminal
24	VREF	O	Reference voltage output terminal

MB3882

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min.	Max.	
Supply voltage	V_{CC}	—	—	20	V
Boot voltage	V_{CB}	CB terminal	—	25	V
Output current	I_O	—	—	120	mA
Peak output current	I_{OP}	Duty ≤ 5% (t = 1 / f_{OSC} × Duty)	—	800	mA
Power dissipation	P_D	Ta ≤ +25 °C	—	740*	mW
Storage temperature	Tstg	—	–55	+125	°C

* : The packages are mounted on the dual-sided epoxy board (10cm × 10cm).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

MB3882

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Supply voltage	V_{CC}	—	5.5	12	18	V
Boot voltage	V_{CB}	CB terminal	—	—	23	V
Reference voltage output current	I_{OR}	VREF terminal	–1	—	0	mA
Bias output current	I_{OB}	VB terminal	–1	—	0	mA
Input voltage	V_{IN}	–INE terminal	0	—	V_{CC} – 1.8	V
	V_{INC}	+INC terminal	0	—	V_{CC}	V
Output current	I_O	—	–100	—	100	mA
Peak output current	I_{OP}	Duty ≤ 5% (t = 1 / fosc × Duty)	–700	—	700	mA
Oscillator frequency	f_{OSC}	—	10	200	500	kHz
Timing resistor	R_T	—	6.8	10	12	kΩ
Timing capacitor	C_T	—	150	470	15000	pF
Boot capacitor	C_B	—	—	0.1	1.0	µF
Reference voltage output capacitor	C_{REF}	VREF terminal	—	0.1	1.0	µF
Bias output capacitor	C_{VB}	VB terminal	1.0	4.7	10	µF
Soft start capacitor	C_S	—	—	0.1	1	µF
Short detection capacitor	C_{SCP}	—	—	0.01	0.1	µF
Operating ambient temperature	Ta	—	–30	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(VCC = 12 V, VB = 0 mA, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
1. Reference Voltage Block [Ref]	Output voltage	V_{REF}	24	Ta = +25 °C	2.475	2.500	2.525	V
		$\Delta V_{REF}/V_{REF}$	24	Ta = 0 °C to +85 °C	—	0.5*	—	%
	Input stability	Line	24	VCC = 5.5 V to 18 V	—	1	10	mV
	Load stability	Load	24	VREF = 0 mA to –1 mA	—	3	10	mV
	Short output current	Ios	24	VREF = 2 V	–28	–14	–7	mA
2. Bias Voltage Block [VB]	Output voltage	VB	13	—	4.95	5.05	5.15	V
3. Undervoltage Lockout Circuit Block [UVLO]	Threshold voltage	V_{TH}	23	VCC = ↗	2.6	2.9	3.2	V
	Hysteresis width	V_H	23	—	—	0.2*	—	V
	Reset voltage	V_{RST}	23	—	1.7	2.1	2.5	V
4. Soft Start Block [CS]	Charge current	I_{CS}	4, 21	—	–14	–10	–6	µA
5. Short Detection Comparator Block [SCP]	Threshold voltage	V_{TH}	22	—	0.63	0.68	0.73	V
	Input source current	I_{CSCP}	22	—	–1.4	–1.0	–0.6	µA
	Short detection time	t_{SCP}	22	CSCP = 0.01 µF	4.5	6.8	12.2	ms
6. Triangular Wave Oscillator Block [OSC]	Oscillator frequency	f_{OSC}	1	RT = 10 kΩ, CT = 470 pF	170	190	210	kHz
	Frequency temperature variation rate	$\Delta f_{OSC}/f_{OSC}$	1	Ta = 0 °C to +85 °C	—	1*	—	%
7. Error Amp Block [Error Amp.]	Threshold voltage	V_{TH1}	5, 20	FB = 1.6 V, Ta = +25 °C	1.241	1.2500	1.259	V
		V_{TH2}	5, 20	FB = 1.6 V, Ta = 0 °C to +85 °C	1.2375	1.2500	1.2625	V
	Input bias current	I_B	5, 20	–INE = 0 V	–200	–20	—	nA
	Voltage gain	A_V	6, 19	DC	60	100	—	dB

* : Typical setting value

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MB3882

(VCC = 12 V, VB = 0 mA, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
7. Error Amp Block [Error Amp.]	Frequency band width	BW	6, 19	AV = 0 dB	—	800*	—	kHz
	Output voltage	V_{FBH}	6, 19	—	2.2	2.5	—	V
		V_{FBL}	6, 19	—	—	0.8	1.0	V
	Output source current	I_{SOURCE}	6, 19	FB = 1.6 V	—	–100	–45	µA
	Output sink current	I_{SINK}	6, 19	FB = 1.6 V	1.5	9.0	—	mA
8. PWM Comparator Block [PWM Comp.]	Threshold voltage	V_{TL}	6, 19	Duty cycle = 0%	1.2	1.3	—	V
		V_{TH}	6, 19	Duty cycle = Dtr	—	1.81	2.0	V
9. Dead time Adjustment Block [DTC]	Maximum duty cycle	Dtr	8, 17	RT = 10 kΩ, CT = 470 pF	85	90	95	%
10. Output Block [Drive]	Output current (main side)	$I_{SOURCE1}$	8, 17	Duty ≤ 5% (t = 1 / fosc × Duty)	—	–700*	—	mA
		I_{SINK1}	8, 17	Duty ≤ 5% (t = 1 / fosc × Duty)	—	900*	—	mA
	Output voltage (main side)	V_{OH1}	8, 17	OUT1 = –100 mA, CB = 17 V, VS = 12 V	CB – 2.5	CB – 0.9	—	V
		V_{OL1}	8, 17	OUT1 = 100 mA, CB = 17 V, VS = 12 V	—	VS + 0.9	VS + 1.4	V
	Output current (synchronous rectifier side)	$I_{SOURCE2}$	11, 14	Duty ≤ 5% (t = 1 / fosc × Duty)	—	–750*	—	mA
		I_{SINK2}	11, 14	Duty ≤ 5% (t = 1 / fosc × Duty)	—	900*	—	mA
	Output voltage (synchronous rectifier side)	V_{OH2}	11, 14	OUT2 = –100 mA	2.5	4.1	—	V
		V_{OL2}	11, 14	OUT2 = 100 mA	—	1.0	1.4	V
	Diode voltage	V_D	10, 15	VB = 10 mA	—	0.9	1.1	V

* : Typical setting value

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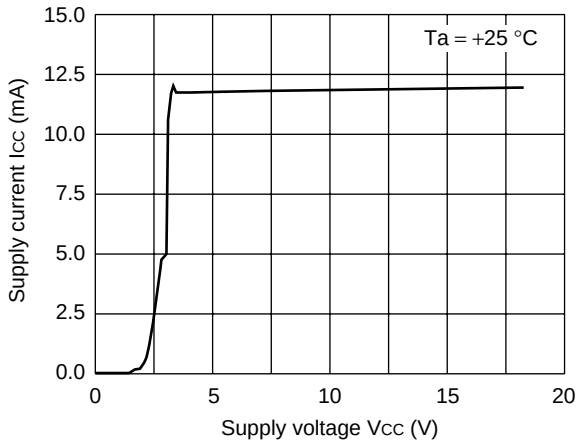
(VCC = 12 V, VB = 0 mA, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
10. Output Block [Drive]	Dead time	t_{D1}	8, 11, 17, 14	RT = 10 kΩ, CT = 470 pF OUT1 = OUT2 = OPEN, VS = 0 V OUT2 : ↓ – OUT1 : ↑	100	200	—	ns
		t_{D2}		RT = 10 kΩ, CT = 470 pF OUT1 = OUT2 = OPEN, VS = 0 V OUT1 : ↓ – OUT2 : ↑	100	250	—	ns
11. Overvoltage Detection Comparator Block [OVP]	Threshold voltage	V_{TH}	7, 18	+INC = ↑	1.44	1.47	1.50	V
	Input bias current	I_B	7, 18	+INC = 0 V	–200	–30	—	nA
12. General	Power supply current	I_{CC}	23	—	—	11	16.5	mA

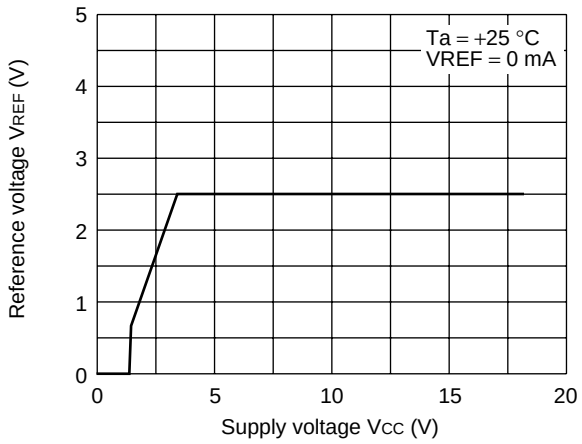
MB3882

■ TYPICAL CHARACTERISTICS

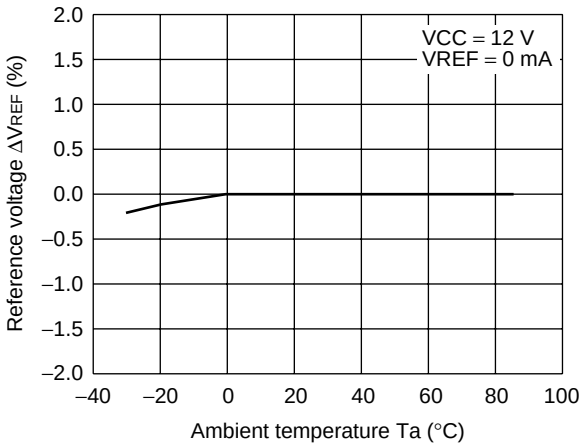
Supply Current vs. Supply Voltage



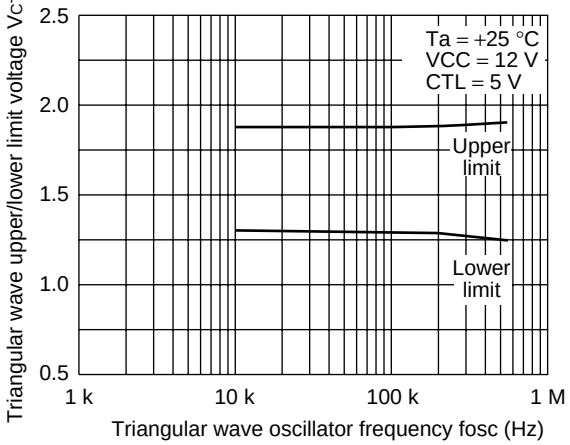
Reference Voltage vs. Supply Voltage



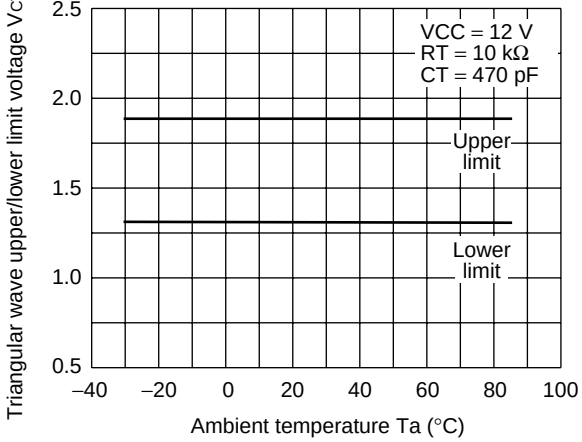
Reference Voltage vs. Ambient Temperature



Triangular Wave Upper/Lower Limit Voltage vs. Triangular Wave Oscillator Frequency



Triangular Wave Upper/Lower Limit Voltage vs. Ambient Temperature



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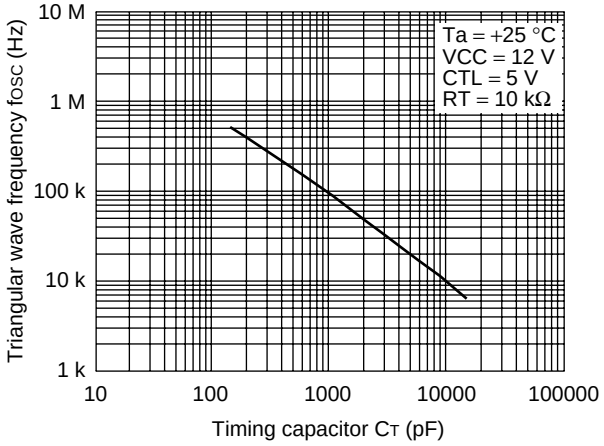
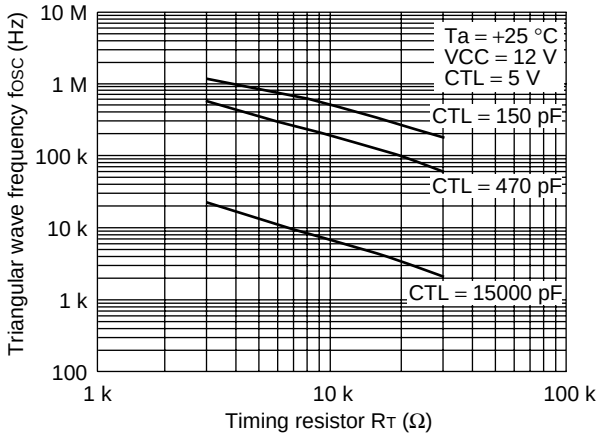
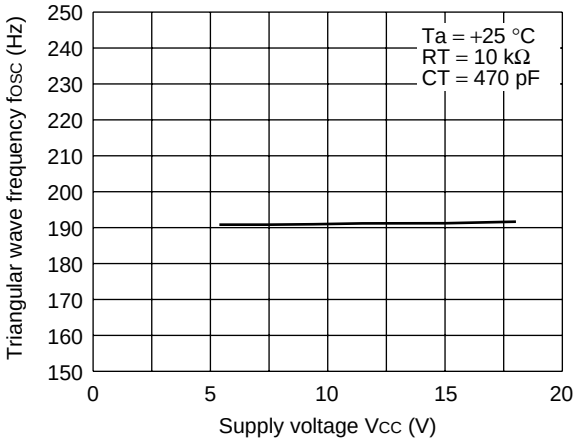
Triangular Wave Oscillator Frequency vs. Timing Capacitor



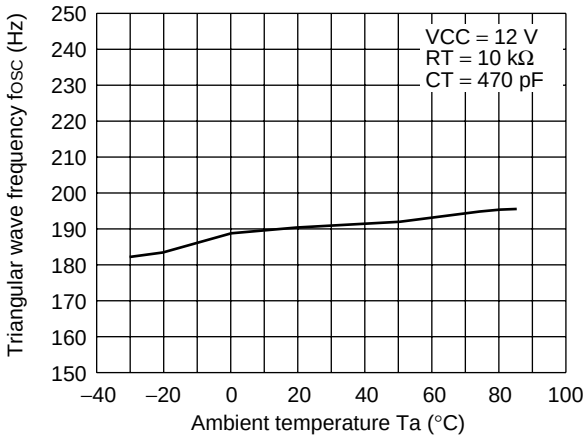
Triangular Wave Oscillator Frequency vs. Timing Resistor



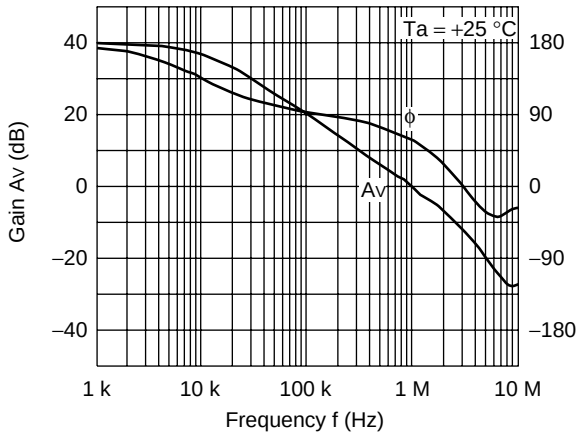
Triangular Wave Oscillator Frequency vs. Supply Voltage

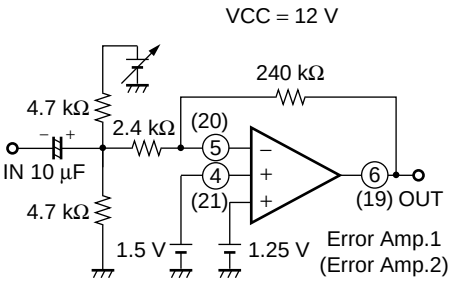


Triangular Wave Oscillator Frequency vs. Ambient Temperature



Error Amp Gain, Phase vs. Frequency





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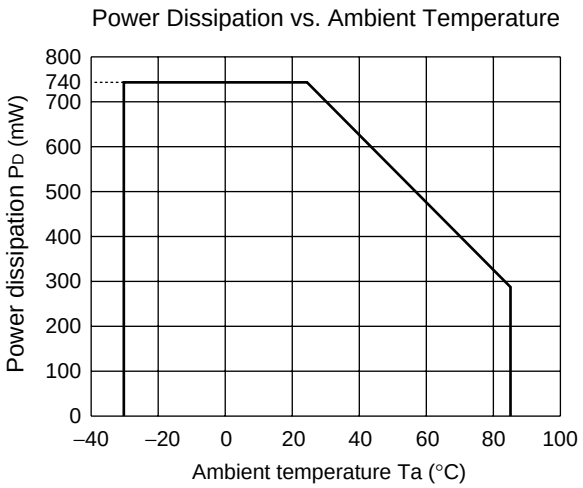


■ FUNCTION DESCRIPTION

1. DC/DC Converter Function

(1) Reference Voltage Block

The reference voltage circuit takes the voltage feed from the power supply terminal (pin 23) and generates a temperature compensated reference voltage (2.5 V typ.) , for use as the reference voltage for the power supply control unit.
Also, an external load current can be obtained from the power supply at the VREF terminal (pin 24) , up to a maximum of 1 mA.

(2) Triangular Wave Oscillator Block

A triangular waveform with amplitude 1.3 V to 1.9 V can be generated by connecting a timing capacitor and resistor to the CT terminal (pin 1) and RT terminal (pin 2) , respectively.
The triangular oscillator waveform can be input to the IC's internal PWM comparator, as well as supplied externally from the CT terminal.

(3) Error Amp Block (Error Amp.)

The error Amp. is an amplifier that detects the output voltage from the DC/DC converter and outputs a PWM control signal. The error Amp. has a broad in-phase input voltage range of 0 to Vcc−1.8 V that can be easily set by the external power supply.
In addition, an arbitrary loop gain can be set up by connecting a feedback resistor and capacitor between the error Amp. output terminal and inverter input terminal, providing stable phase compensation to the system.
Also, power-on rush current can be prevented by connecting a soft start capacitor between the error Amp. non-inverted input terminals CS1 terminal (pin 4) and CS2 terminal (pin 21) . The soft start function operates with a stable soft start time that is not dependent on the output load of the DC/DC converter.

(4) PWM Comparator Block (PWM Comp.)

This is a voltage - pulse width modulator that controls the output duty according to the input voltage.

Main side :	Turns the output transistor on in the intervals in which the error Amp. output voltage is higher than the triangular wave voltage.
Synchronous rectifier side :	Turns the output transistor on in the intervals in which the triangular wave voltage the is lower than error Amp. voltage.

(5) Output Block

The output block has totem pole configuration on both the main side and synchronous rectifier side, and can drive an external N-ch MOSFET.
Also, the high output drive capability (700 mA max : duty ≤ 5%) provides high gate-source capacitor, enabling the use of low on-resistor FET devices.

2. Channel Control Functions

Channel ON/OFF control is provided by using the CS1 terminal (pin 4) and CS2 terminal (pin 21) setting functions.

Channel On/Off Setting Functions

CS terminal voltage level		Channel output state	
CS1	**CS2**	**CH1**	**CH2**
GND	GND	OFF	OFF
GND	Hi-Z	OFF	ON
Hi-Z	GND	ON	OFF
Hi-Z	Hi-Z	ON	ON

3. Protective Functions

(1) Timer Latch Short Circuit Protection (SCP)

The short circuit protection comparators read the output voltage levels. If the output voltage on either channel falls below the short detection voltage, the timer circuit is activated to start charging the external capacitor Cscp connected to the CSCP terminal (pin 22) .
When capacitor voltage reaches approximately 0.68 V the output FET turns off, setting the idle interval to 100%. Once the protection circuit is activated, it can be reset by turning the power supply off and on again. (See “Setting the Timer Latch Short Circuit Protector Time Constant.”)

(2) Undervoltage Lockout Circuit Block (UVLO)

Transient status during normal power-on or momentary drops in supply voltage can cause abnormal operation in an control IC, leading to damage or degradation of system components. The undervoltage lockout circuit prevents such abnormal operations by reading the internal reference voltage level and switching the output transistor off, setting the idle interval to 100% and holding the CSCP terminal (pin 22) to “L” level.
System operation is restored when the supply voltage rises back about the undervoltage lockout circuit threshold voltage.

(3) Overvoltage Protection Block (OVP)

The overvoltage protection circuit uses an overvoltage comparator (OVP Comp.) on each channel to read the output voltage levels from the DC/DC converter. If the output voltage exceeds the threshold voltage a latch is set, turning off the main side FET on the corresponding channel.

■ SETTING THE TIMER LATCH SHORT CIRCUIT PROTECTOR TIME CONSTANT

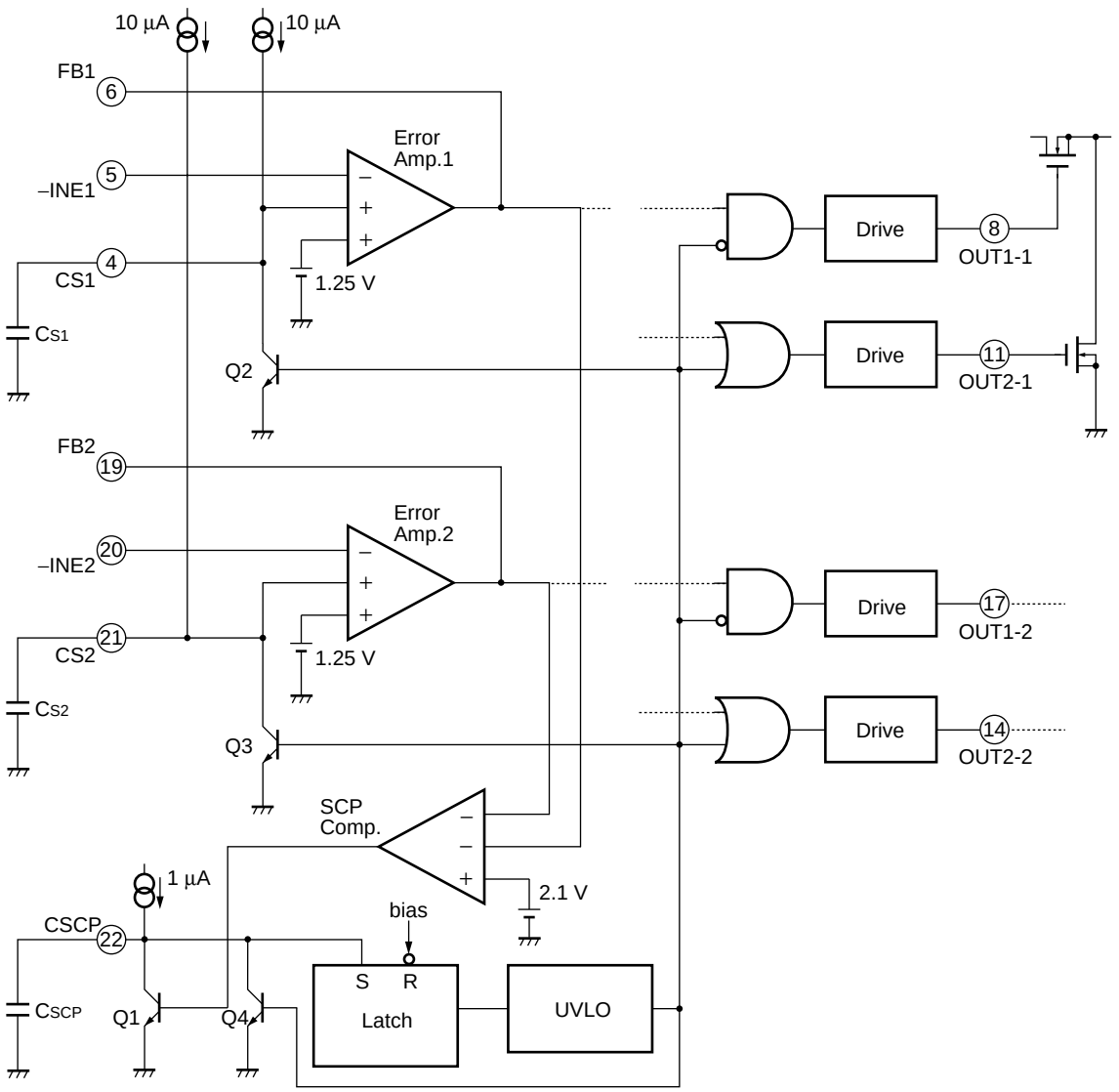
Each channel has a short circuit protection comparator (SCP Comp.) which constantly compares the error Amp. output level to the reference voltage.
When the DC/DC comparator load conditions are stable on all channels, the short circuit protection comparator output is at “H” level, transistor Q1 is on, and the CSCP terminal (pin 22) is held at input standby voltage (V_{STB} : = 50 mV) .
If load conditions change rapidly, such as during a load short, causing output voltage to drop, the short circuit protection comparator output goes to “L” level. This causes the transistor Q1 to shut off, charging the short circuit protection capacitor Cscp (connected to the CSCP terminal) at 1 μA.

Short detection time

$tscp\ (s) \fallingdotseq 0.68 \times Cscp\ (\mu F)$

When the capacitor Cscp is charted to the threshold voltage (V_{TH} : = 0.68 V) a latch is set, turning the external FET off (setting the idle interval to 100%) . At this time the latch input is closed and the CSCP terminal is held at the input latch voltage (V_I : = 50 mV) . (When a short circuit is detected on either of the two channels, both channels are shut off.)

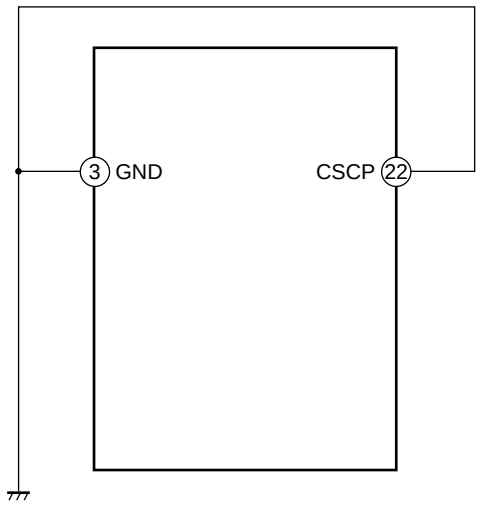
MB3882



< Timer Latch Short Circuit Protection Circuit >

■ PROCESSING WITHOUT USING THE CSCP TERMINAL

When the timer latch short circuit protection circuit is not used, the CSCP terminal (pin 22) should be shorted to GND using the shortest possible connection.



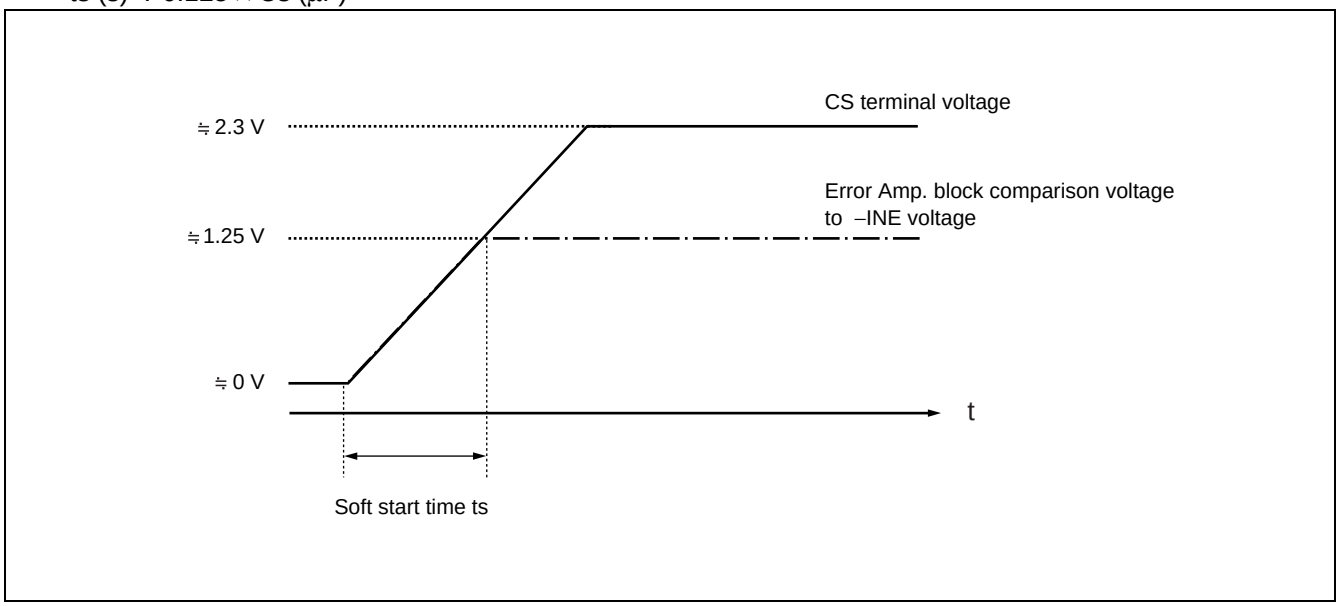
< Operation Without Using the CSCP Terminal >

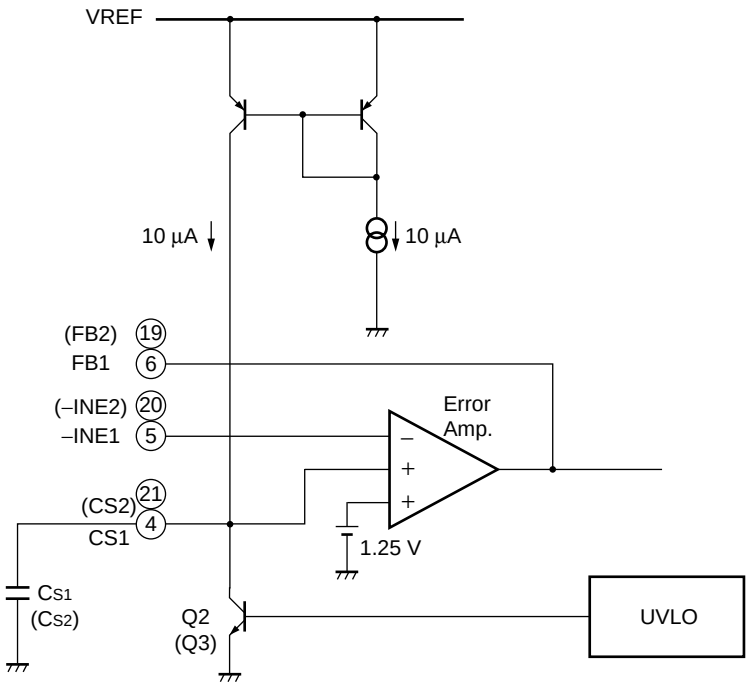
■ SOFT START TIME SETTING

The soft start function prevents rush current events when the IC power is turned on, by connecting soft start capacitors (Cs_1, Cs_2) to the CS1 terminal (pin 4) for channel 1, and the CS2 terminal (pin 21) for channel 2.
When the IC is activated (Vcc ≥ UVLO threshold voltage) , Q2 and Q3 are off and the CS1 and CS2 terminals begin charging the externally connected soft start capacitors (Cs_1, Cs_2) at 10 μA.
Because the error Amp. output (FB1, FB2) is determined by the ratio of the lower of the two non-inverted input terminals (1.25 V, CS terminal voltage) to the inverted input terminal voltage (–INE) , the soft start interval (when CS terminal voltage < 1.25 V) FB is determined by the ratio of the –INE terminal voltage and CS terminal voltage. Thus the DC/DC converter output voltage rises in proportion to the rise in the CS terminal voltage as the soft start capacitor connected to the CS terminal charges. The soft start time is determined by the following formula.

Soft start time (time to output 100%)

ts (s) ≒ 0.125 × Cs (μF)





< Soft Start Block >

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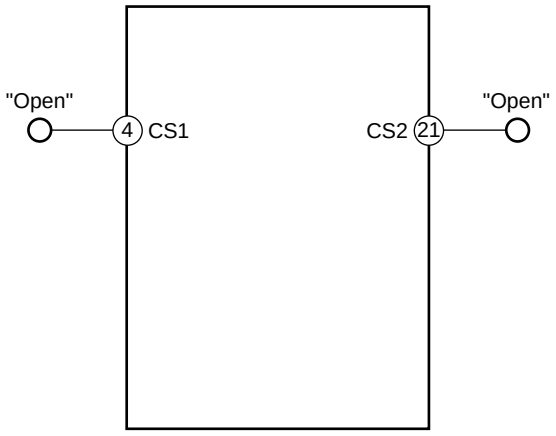
■ PROCESSING WITHOUT USING THE CS TERIMNALS

When the soft start function is not used, the CS1 terminal (pin 4) and CS2 terminal (pin 22) should be left open.



< Operation Without Soft Start Setting >

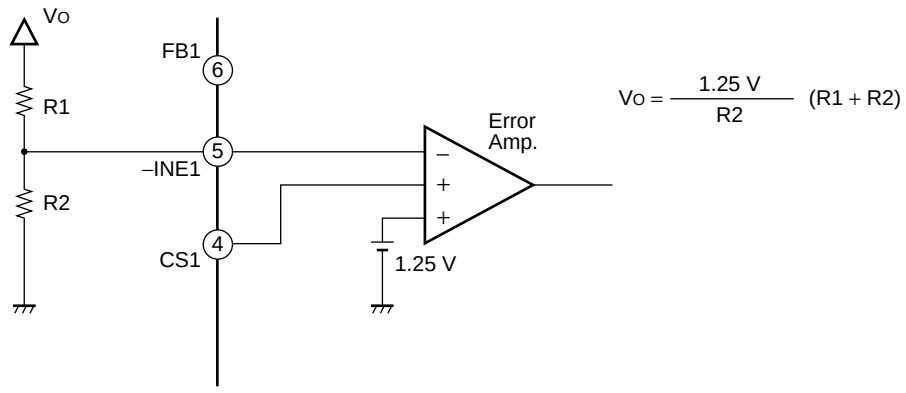
■ OSCILLATOR FREQUENCY SETTING

The oscillator frequency can be set by connecting a timing capacitor (C_T) to the CT terminal (pin 1) and a timing resistor (R_T) to the RT terminal (pin 2) .

Oscillator frequency

$$fosc\ (kHz) \fallingdotseq \frac{893000}{C_T\ (pF) \bullet R_T\ (k\Omega)}$$

■ OUTPUT VOLTAGE SETTING



< CH1, 2 >

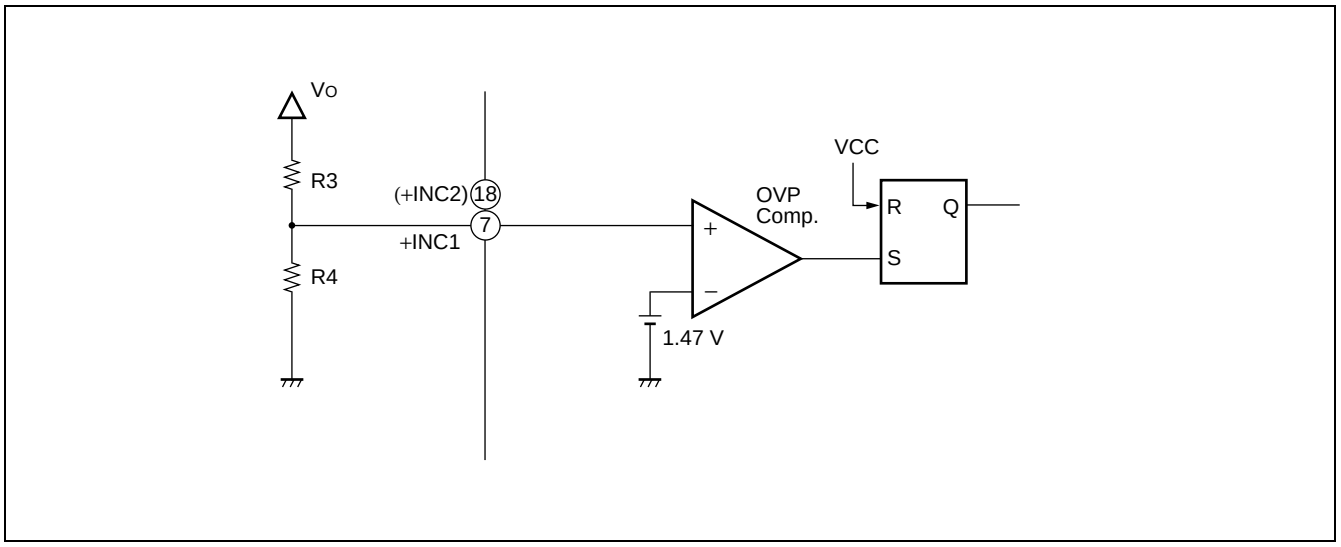
■ OVERVOLTAGE PROTECTION CIRCUIT VOTAGE SETTING

Overvoltage conditions in the DC/DC converter output voltage can be detected by connecting external resistance from the DC/DC converter output voltage to the +INC1 terminal (pin 7) and +INC2 terminal (pin 18) on the respective overvoltage protection comparator circuits (OVP comp. 1, 2) .
When the output voltage of the DC/DC converter rises above the detection voltage, the overvoltage protection comparator (OVP Comp. 1, 2) output goes to “H” level, setting a latch and shutting off the corresponding channel. Each of the overvoltage protection circuit latches operates independently.

Detection voltage

V_{OVP} (V) ≒ 1.47 × (R3 + R4) /R4

Once the protection circuit has been activated, it can be reset by lowering the VCC voltage below the reset voltage (1.7 V min.) .



■ PRECAUTIONS RELATED TO INTERNAL IC POWER CONSUMPTION

The internal power dissipation in the IC is greatly affected by the oscillator frequency and the FET total gate charge. When using the MB 3882 in an application, caution must be taken in relation to internal IC power consumption.
As shown below, I_B (average current) can be determined from the total gate charge Qg_1, Qg_2, charged from the gate capacitance (C_{iss1}, C_{iss2}, C_{rss1}, C_{rss2}) of the external FET Q1, Q2, by the following formula.

Per individual channel :

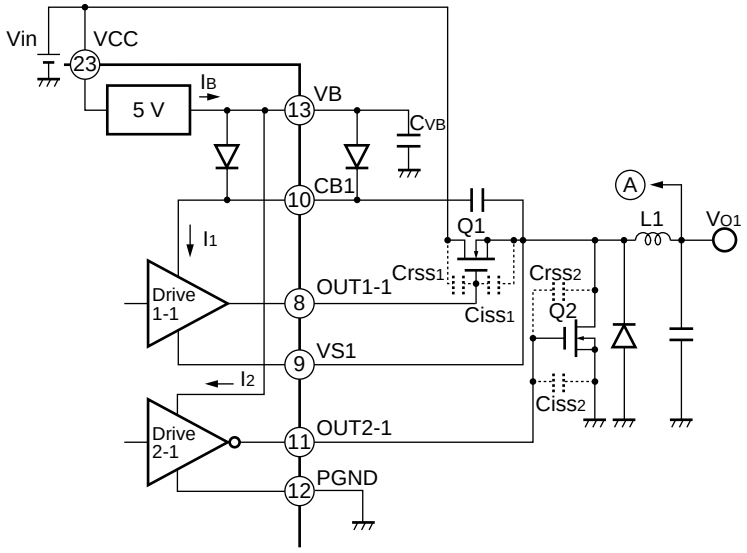
$$I_B\ (A) = I_1 + I_2$$

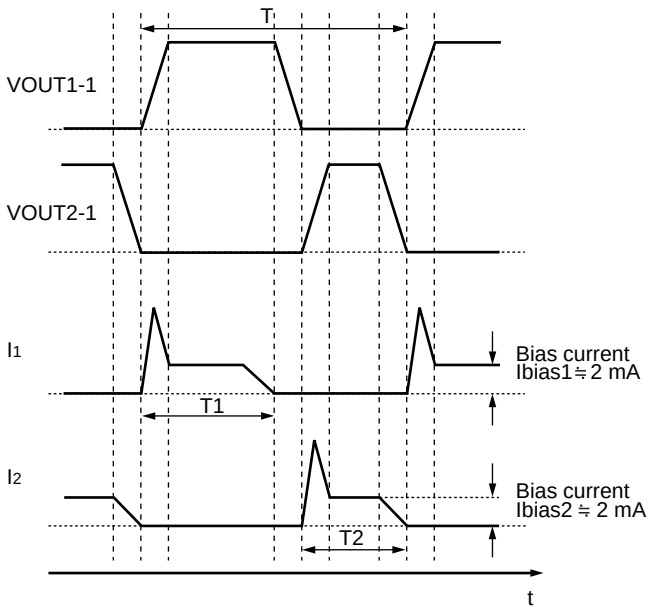
$$\fallingdotseq Ibias_1 \times \frac{T1}{T} + \frac{Qg_1}{T} + Ibias_2 \times \frac{T2}{T} + \frac{Qg_2}{T} \qquad (Ibias_1 = Ibias_2 \fallingdotseq 2\ mA)$$

Because IC current consumption other than I_B is 11 mA, power consumption can be determined from the following formula.

Power consumption : Pc

$$Pc\ (W) = 0.011 \times V_{CC} + 2 \times V_{CC} \times I_B - V_B \times I_B$$

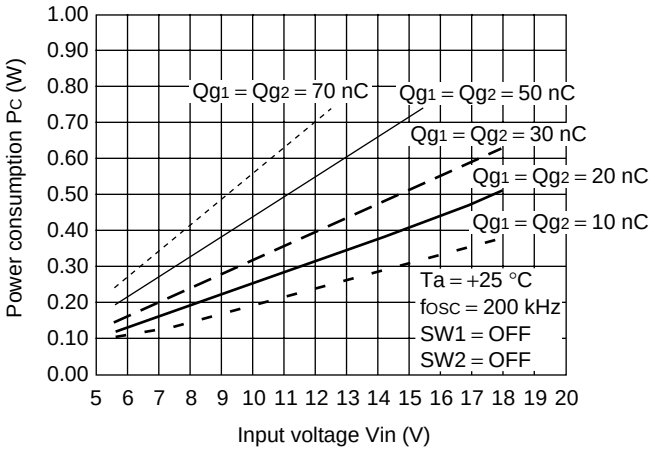




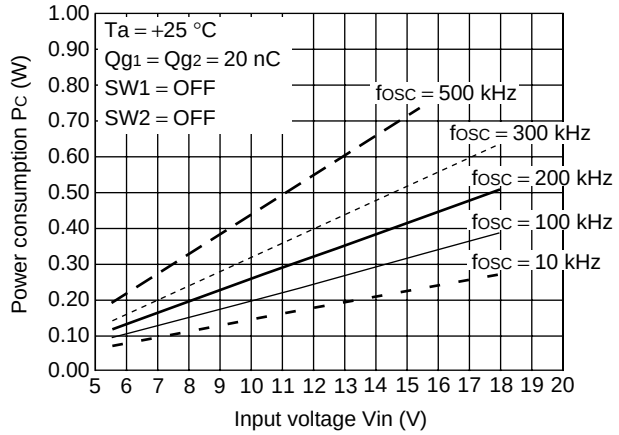
Using the above formulas to determine power consumption, settings should be made with reference to the “Power Consumption vs. Input Voltage” on the following page, as well as the “Power dissipation vs. Ambient Temperature.”

MB3882

Power Consumption vs. Input Voltage (Qg Parameters)

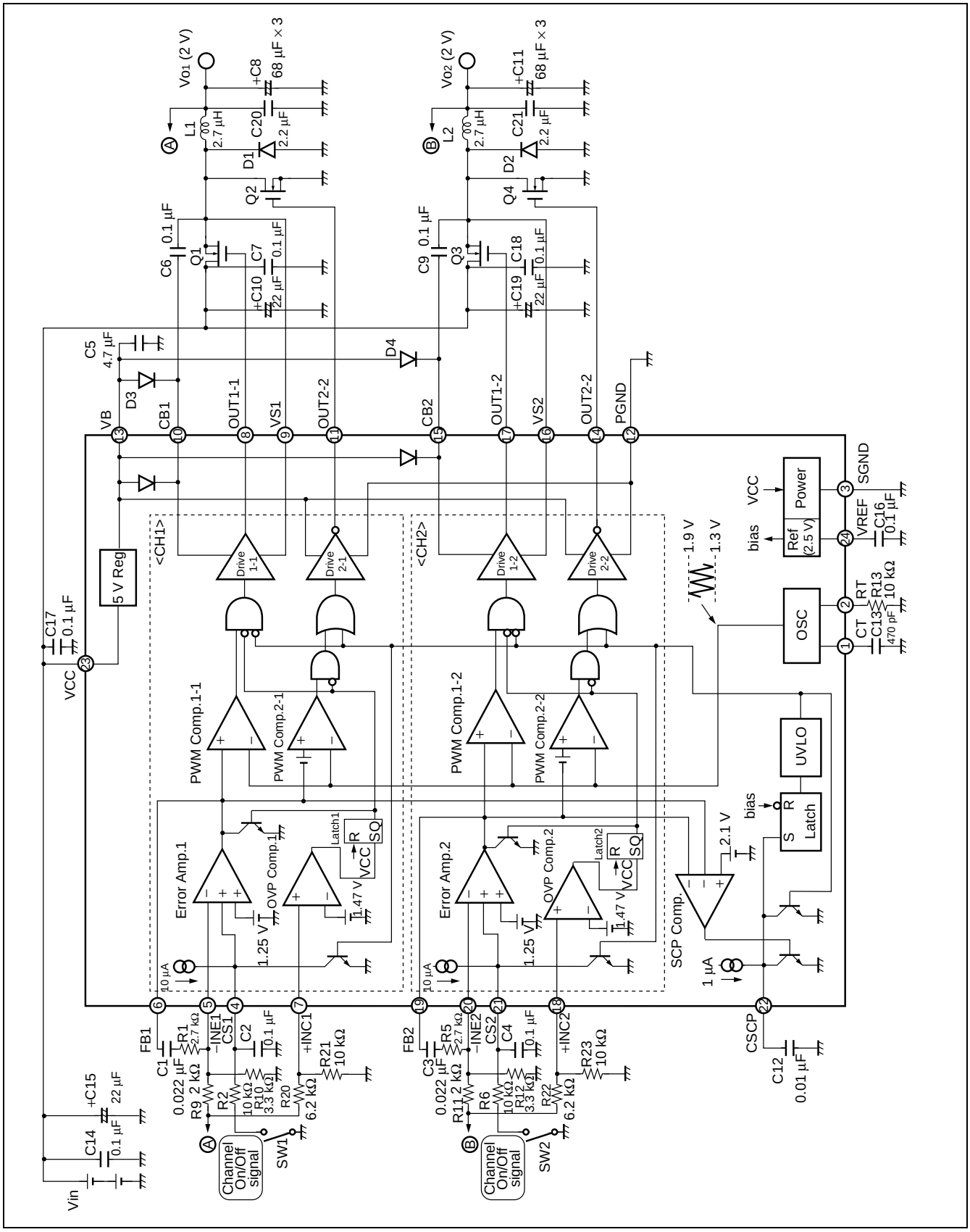


Power Consumption vs. Input Voltage (fosc Parameters)



MB3882

■ APPLICATION CIRCUIT



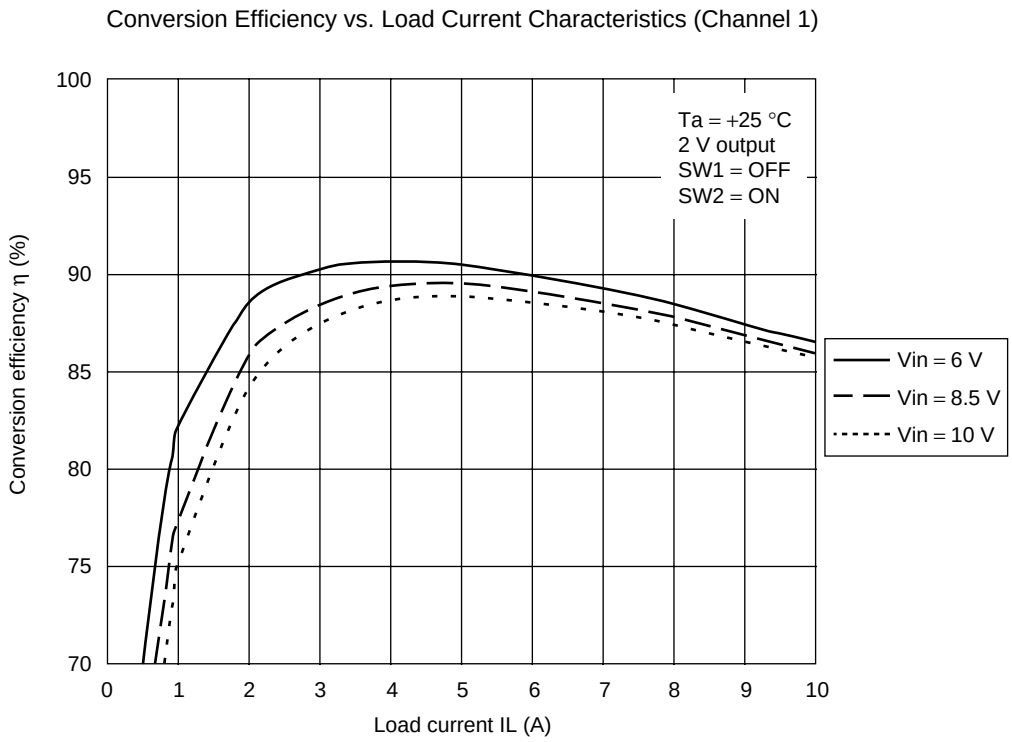
MB3882

■ COMPONENT LIST

COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS No.
Q1 to Q4	FET	VDS = 30 V		IR	IRF7811
D1, D2 D3, D4	Diode Diode	VF=0.35V(Max.),at IF=1A VF=0.30V(Max.),at IF=10mA		ROHM ROHM	RB051L-40 RB495D
L1, L2	Coil	2.7 µH	12 A, 4.5 mΩ	TDK	RLF12545T -2R7N8R7
C1 C2 C3 C4 C5 C6, C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 to C18 C19 C20, C21	Ceramics Condenser Ceramics Condenser Ceramics Condenser Ceramics Condenser Ceramics Condenser Ceramics Condenser Electrolytic Condenser Ceramics Condenser OS Condenser Electrolytic Condenser Ceramics Condenser Ceramics Condenser Ceramics Condenser OS Condenser Ceramics Condenser OS Condenser Ceramics Condenser	0.022 µF 0.1 µF 0.022 µF 0.1 µF 4.7 µF 0.1 µF 68 µF 0.1 µF 22 µF 68 µF 0.01 µF 470 pF 0.1 µF 22 µF 0.1 µF 22 µF 2.2 µF	 6.3 V 25 V 6.3 V 25 V 25 V 	—	—
R1 R2 R5 R6 R9 R10 R11 R12 R13 R20 R21 R22 R23	Resistor Resistor Resistor Resistor Resistor Resistor Resistor Resistor Resistor Resistor Resistor Resistor Resistor	2.7 kΩ 10 kΩ 2.7 kΩ 10 kΩ 2 kΩ 3.3 kΩ 2 kΩ 3.3 kΩ 10 kΩ 6.2 kΩ 10 kΩ 6.2 kΩ 10 kΩ	1/4 W 1/4 W 1/4 W 1/4 W 1/4 W 1/4 W 1/4 W 1/4 W 1/4 W 1/4 W 1/4 W 1/4 W 1/4 W	—	—

Notes : IR : International Rectifier Corp.
ROHM : Rohm, Ltd.
TDK : TDK, Ltd.

■ REFERENCE DATA



MB3882

■ PRECAUTIONARY INFORMATION

- **Printed circuit board ground lines should be designed with consideration for common impedance.**

- **Take sufficient countermeasures should be taken to protect against static electricity.**
- Always place semiconductors in containers that have anti-static provisions, or are conductive.
- After mounting, PC boards should be placed in conductive bags or containers for storage and handling.
- Working surfaces, tools, and measurement equipment should be grounded.
- Persons handling semiconductors should be grounded directly with resistance of 250 kΩ to 1 MΩ.

- **Do not apply negative voltages.**
- Application of negative voltage of –0.3 V or greater can create parasitic transistor effects on an LSI device, leading to abnormal operation.

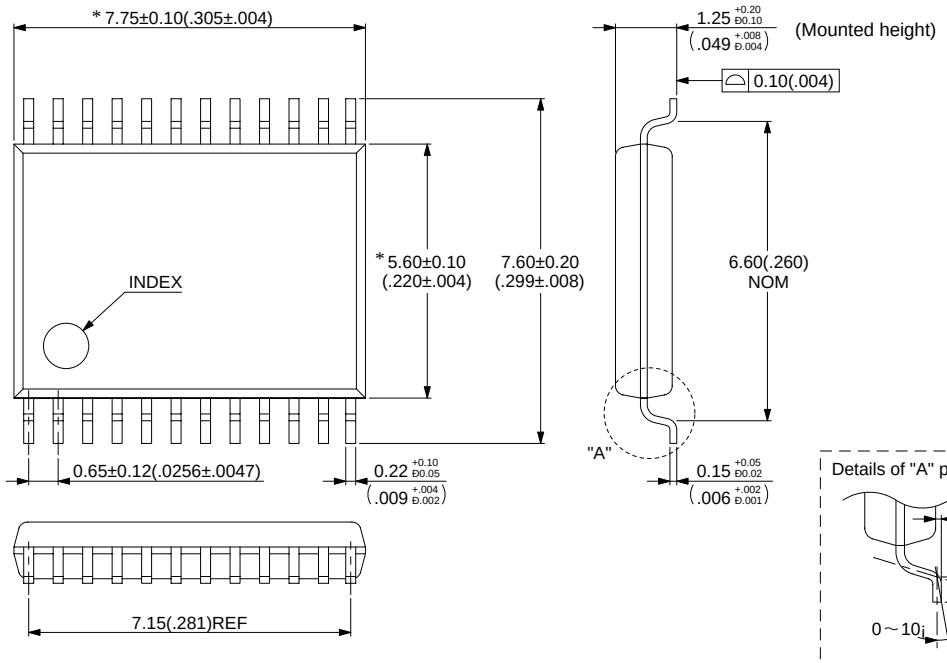
■ ORDERING INFORMATION

Part Number	Package	Remarks
MB3882PFV	Plastic SSOP 24-pin (FPT-24P-M03)	

■ PACKAGE DIMENSION

24-pin, Plastic SSOP
(FPT-24P-M03)

* Dimensions include resin remainder.



Dimensions in mm (inches) .

MB3882

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka,
Nakahara-ku, Kawasaki-shi,
Kanagawa 211-8588, Japan
Tel: +81-44-754-3763
Fax: +81-44-754-3329

http://www.fujitsu.co.jp/

North and South America

FUJITSU MICROELECTRONICS, INC.
3545 North First Street,
San Jose, CA 95134-1804, U.S.A.
Tel: +1-408-922-9000
Fax: +1-408-922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: +1-800-866-8608
Fax: +1-408-922-9179

http://www.fujitsumicro.com/

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Am Siebenstein 6-10,
D-63303 Dreieich-Buchschlag,
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

http://www.fujitsu-fme.com/

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LTD.
#05-08, 151 Lorong Chuan,
New Tech Park,
Singapore 556741
Tel: +65-281-0770
Fax: +65-281-0220

http://www.fmap.com.sg/

Korea

FUJITSU MICROELECTRONICS KOREA LTD.
1702 KOSMO TOWER, 1002 Daechi-Dong,
Kangnam-Gu,Seoul 135-280
Korea
Tel: +82-2-3484-7100
Fax: +82-2-3484-7111

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