FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27223-1E

ASSP For Power Supply Applications

Multi-Resonance AC/DC Converter IC

MB3873

■ DESCRIPTION

The MB3873 is a pulse frequency modulation (PFM) type multi-resonance AC/DC converter IC providing soft switching functions in a more compact, higher-efficiency, low-noise package.

Since this product allows reduced number of the components and reduced size of the transformer, it is also compatible with the miniaturization of AC adaptor.

The product retains the multi-resonance for the non-load, over-load and load short-circuit over the wide range of input voltage, making it the appropriate IC for the small-sized AC adaptor.

■ FEATURES

- Operating power supply voltage : 10V to 28V
- Operating current : 2.5mA typ.
- Low standby current : 400µA typ.
- Control frequency range : 10kHz to 800kHz
- Operating temperature range : –30°C to +105°C
- Soft start circuit on-chip
- Overvoltage detection circuit on-chip

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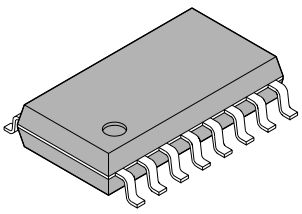
■ PACKAGE

16-pin plastic SOP



(FPT-16P-M06)

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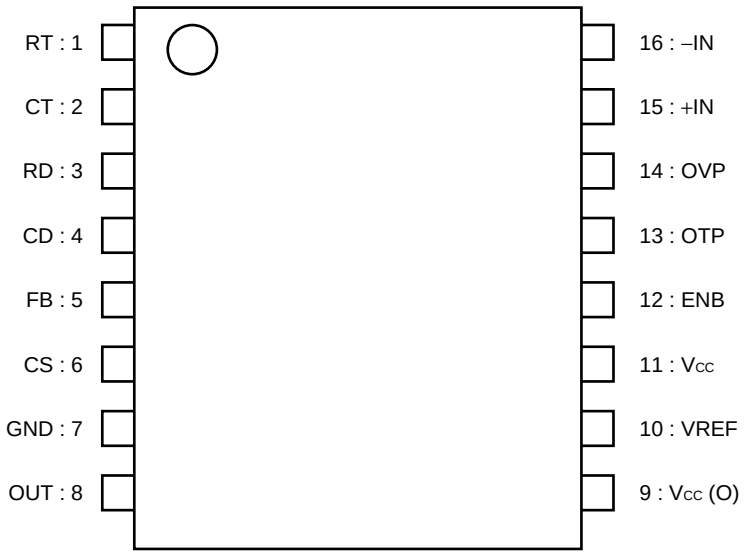
- Overload detection circuit on-chip
- Over temperature detection circuit on-chip
- Under voltage lockout protection circuit on-chip

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-16P-M06)

■ PIN DESCRIPTION

Pin No.	Symbol	I/O	Descriptions
1	RT	—	Triangular wave oscillator frequency setting resistor connection pin
2	CT	—	Triangular wave oscillator frequency setting capacitor connection pin
3	RD	—	Dead time setting resistor connection pin
4	CD	—	Delay interval setting capacitor connection pin
5	FB	I	Control frequency control pin
6	CS	—	Soft start capacitor connection pin
7	GND	—	Ground pin
8	OUT	O	Totem pole type output pin
9	V_{CC} (O)	—	Output circuit power supply pin
10	VREF	O	Reference voltage output pin
11	V_{CC}	—	Reference power and control circuit power supply pin
12	ENB	—	UVLO voltage setting resistor connection pin
13	OTP	I	Overtemperature detection comparator input pin
14	OVP	I	Overvoltage detection comparator 1 input pin
15	+IN	I	Overvoltage detection comparator 2 non-inverted input pin
16	–IN	I	Overvoltage detection comparator 2 inverted input pin

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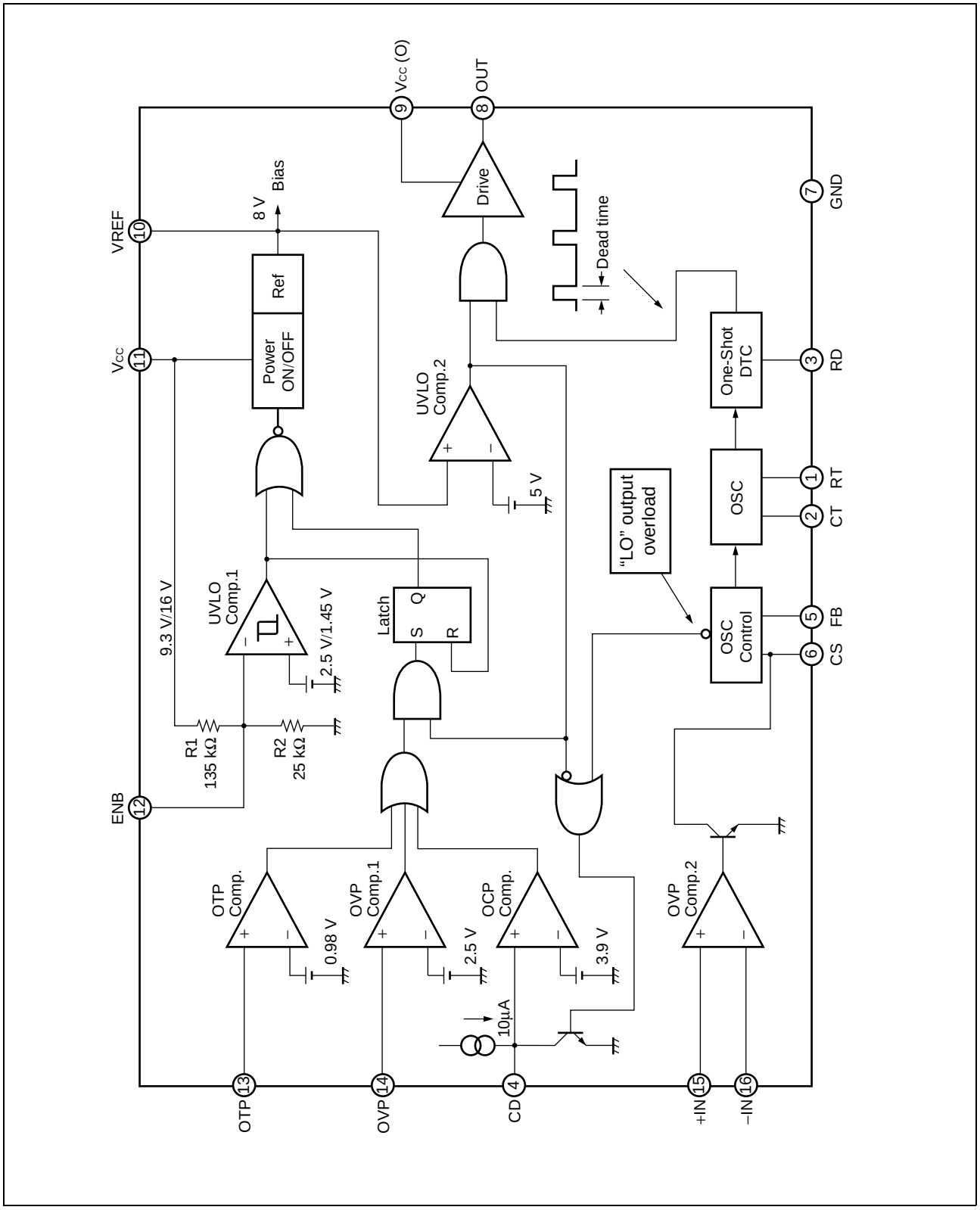
■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RAGINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min.	Max.	
Power supply voltage	V_{CC}	V_{CC}, V_{CC} (O) pin	—	30	V
Output current	I_O	OUT pin	—	20	mA
Peak output current	I_O	OUT pin, Duty ≤ 5 %	—	300	mA
Power dissipation	P_D	Ta ≤ +25°C	—	540*	mW
Storage temperature	Tstg	—	–55	+125	°C

* : The packages are mounted on the dual-sided epoxy board (10 cm × 10 cm).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage	V_{CC}	—	10	18	28	V
	V_{CC} (O)	—	5	VREF	28	V
Reference voltage output current	I_{OR}	V_{CC} (O) = VREF	–10	—	0	mA
Input voltage	V_{IN}	OTP, OVP pin	0	—	V_{CC}	V
		+IN, –IN pin	0	—	VREF	V
Output current	I_O	OUT pin	–15	—	15	mA
Triangular wave oscillator frequency	f_{OSC}	FB = VREF, CS = OPEN	10	105	300	kHz
Timing capacitor	C_T	—	100	220	4700	pF
Timing resistor	R_T	—	15	33	47	kΩ
Control frequency	f_{OSC}	FB controlled	10	105	800	kHz
OSC control current	I_{FB}	FB pin	–1	—	—	mA
Soft start capacitor	C_S	—	—	0.1	1.0	µF
Delay time capacitor	C_D	—	—	0.1	1.0	µF
Dead time resistor	R_D	—	36	120	250	kΩ
Operating ambient temperature	Ta	—	–30	25	105	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

($Ta = +25°C$, $V_{CC} = 18$ V, V_{CC} (O) $= V_{REF}$)

Parameter		Symbol	Pin no	Conditions	Value			Unit
					Min.	Typ.	Max.	
Reference voltage block [Ref]	Output voltage	V_{REF}	10	Ta = 25°C	7.6	8.0	8.4	V
				Ta = –30 to +85°C	7.44	8.0	8.56	V
	Input stability	Line	10	V_{CC} = 10 V to 28 V	–30	—	30	mV
	Load stability	Load	10	VREF = 0 mA to –10 mA	—	25	50	mV
	Short circuit output current	I_{OS}	10	VREF = 4 V	–35	–25	–15	mA
Under voltage lockout circuit block [UVLO]	Threshold voltage	V_{TLH}	10	V_{CC} = ↑	15	16	17	V
		V_{THL}	10	V_{CC} = ↓	8.8	9.3	9.8	V
	Hysteresis width	V_H	10	$V_H = V_{TLH} - V_{THL}$	—	6.7	—	V
Triangular wave oscillator block [OSC]	Oscillator frequency	f_{OSC1}	8	C_T = 220 pF, R_T = 33 kΩ, FB = VREF, CS = OPEN	95	105	115	kHz
		f_{OSC2}	8	C_T = 220 pF, R_T = 33 kΩ, FB = –1 mA, CS = OPEN	535	630	725	kHz
	Frequency temperature stability	Δf/fdt	8	Ta = –30 to +85°C	—	1.0*	—	%
Soft start block [CS]	Charge current	I_{CS1}	6	CS = 0 V	–35	–25	–15	µA
		I_{CS2}	6	CS = 2 V	–3.5	–2.5	–1.5	µA
	Soft start frequency	f_{CS1}	8	C_T = 220 pF, R_T = 33 kΩ, FB = VREF, CS = 0 V	380	450	520	kHz
		f_{CS2}	8	C_T = 220 pF, R_T = 33 kΩ, FB = VREF, CS = OPEN	95	105	115	kHz
Dead time control block [DTC]	Dead time	t_{DEAD}	8	R_D = 120 kΩ	400	500	600	ns
Overload detection block [OCP]	Threshold current	I_{TH}	5	—	–60	–40	–20	µA
	Threshold voltage	V_{TH}	4	—	3.7	3.9	4.1	V
	Charge current	I_{CD}	4	—	–14	–10	–6	µA
Overvoltage detection comparator block1 [OVP1]	Threshold voltage	V_{TH}	14	—	2.37	2.50	2.63	V
	Input bias current	I_B	14	OVP = 0 V	–400	–50	—	nA

*: Standard design value.

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(Ta = +25°C, V_{CC} = 18 V, V_{CC} (O) = V_{REF})

Parameter		Symbol	Pin no	Conditions	Value			Unit
					Min.	Typ.	Max.	
Overvoltage detection comparator block2 [OVP2]	Input offset voltage	V_{IO}	15, 16	CS = 1.5 V	—	—	10	mV
	Common mode input voltage range	V_{CM}	15, 16	—	0	—	V_{REF} – 1.8	V
	Input current	I_{B1}	15	+IN = 0 V, –IN = 3 V	–200	–25	—	nA
		I_{B2}	16	+IN = 3 V, –IN = 0 V	–200	–25	—	nA
Over tempera-ture detection comparator block [OTP]	Threshold voltage	V_{TH}	13	—	0.93	0.98	1.03	V
	Input bias current	I_B	13	OTP = 0 V	–400	–50	—	nA
Output block [Drive]	Output source current	I_{SOURCE}	8	Duty ≤ 5 %, OUT = 5 V	—	–60	—	mA
	Output sink current	I_{SINK}	8	Duty ≤ 5 %, OUT = 3 V	—	100	—	mA
	Output voltage	V_{OH}	8	OUT = –15 mA	6.6	7.1	—	V
		V_{OL}	8	OUT = 15 mA	—	0.9	1.4	V
	Rise time	t_r	8	C_L = 100 pF	—	25	—	ns
	Fall time	t_f	8	C_L = 100 pF	—	20	—	ns
General	Standby current	I_{CCS}	11	V_{CC} = 14 V	—	400	600	µA
	Operating power supply current	I_{CC}	11	V_{CC} = 18 V	—	2.5	3.8	mA
	Cut off power supply current	I_{CCL}	11	V_{CC} = 18 V, OTP = 2 V	—	450	680	µA

*: Standard design value.

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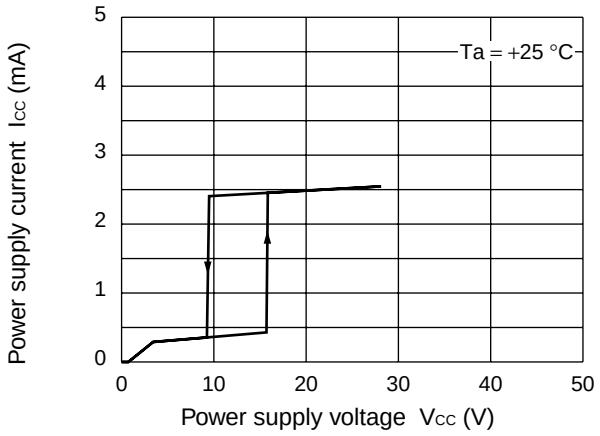
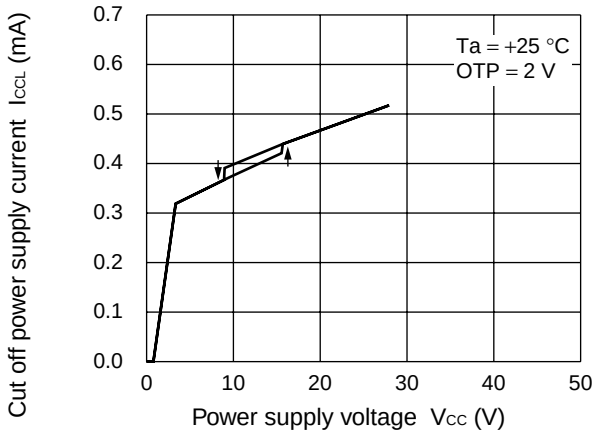
■ TYPICAL CHARACTERISTICS

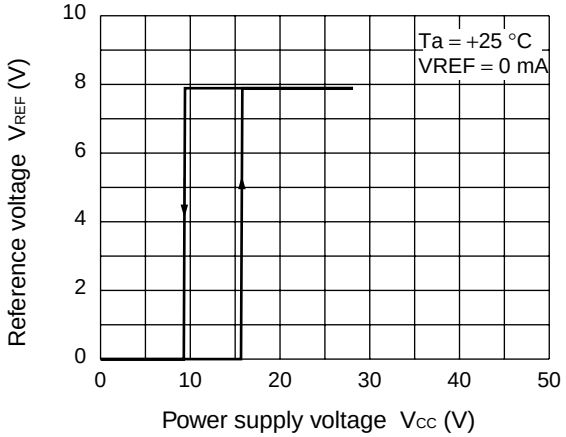
Power supply current vs. power supply voltage



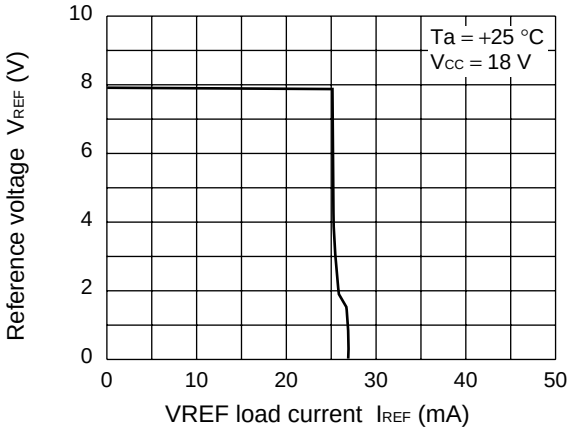
Cut off power supply current vs. power supply voltage



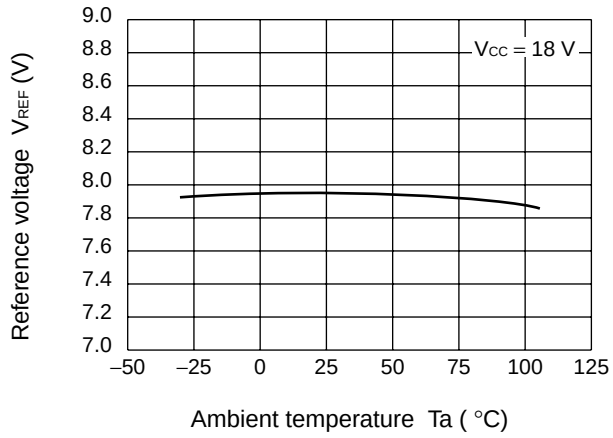
Reference voltage vs. power supply voltage



Reference voltage vs. VREF load current



Reference voltage vs. ambient temperature



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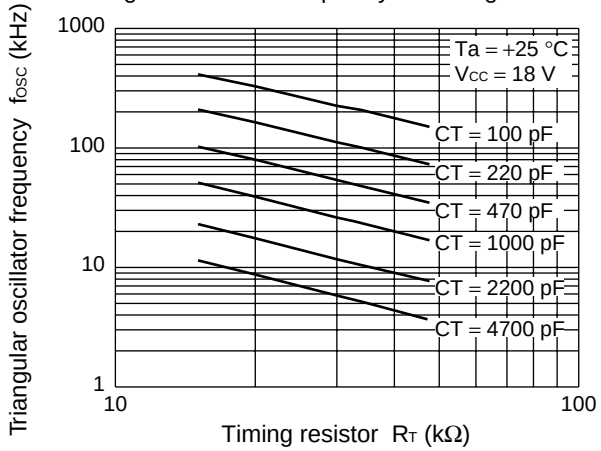
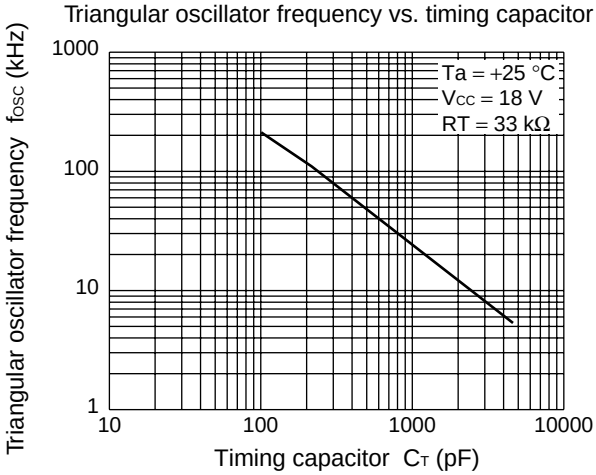
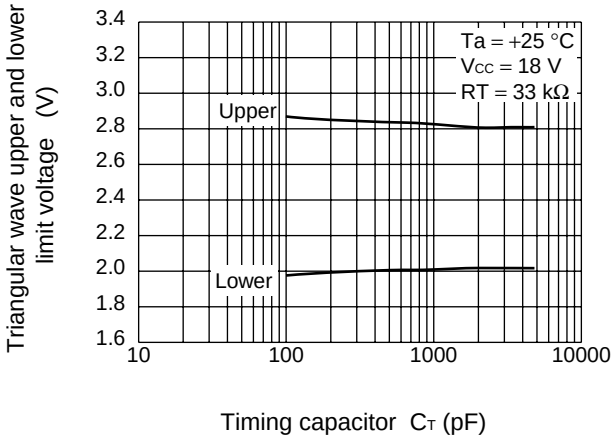
Triangular oscillator frequency vs. timing resistor



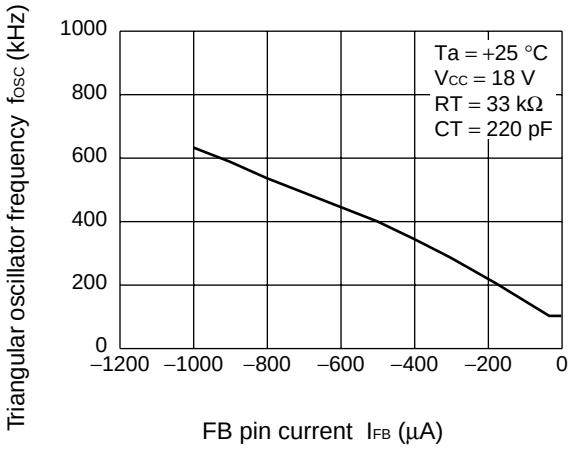
Triangular oscillator frequency vs. timing capacitor



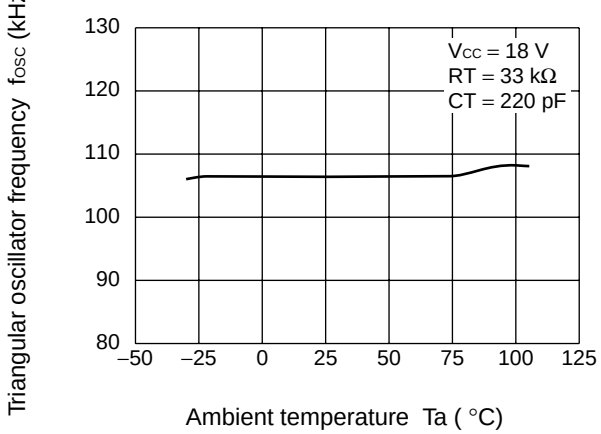
Triangular wave upper and lower limit voltage vs. timing capacitor



Triangular oscillator frequency vs. FB pin current



Triangular oscillator frequency vs. ambient temperature



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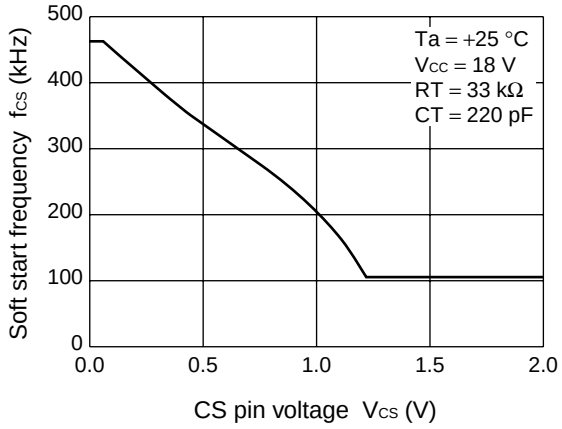
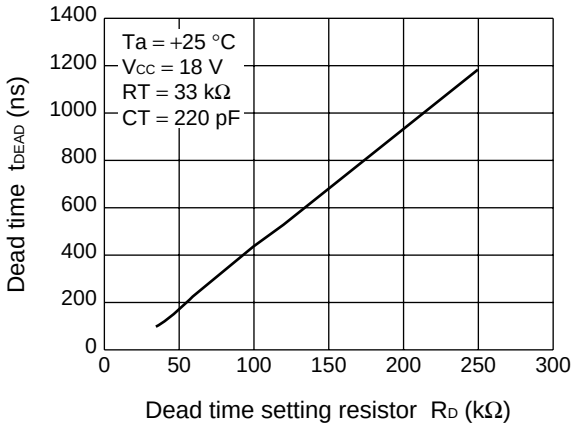
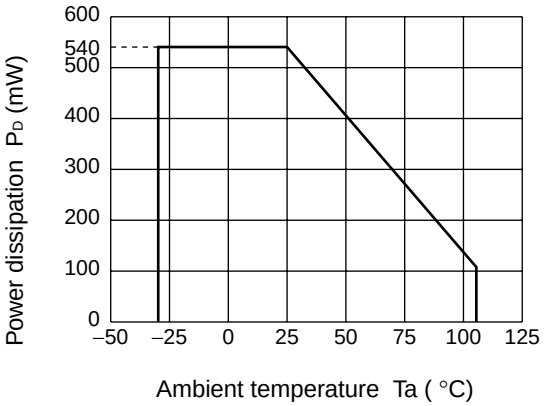
Soft start frequency vs. CS pin voltage



Dead time vs. dead time setting resistor



Power dissipation vs. ambient temperature



■ FUNCTIONAL DESCRIPTION

1. Switching Regulator Function

(1) Reference voltage circuit (Ref)

The reference voltage circuit takes the voltage from the Vcc terminal (pin 11) and generates a temperature-compensated reference voltage (≒ 8V), which is used as the reference voltage supply for the IC internal circuit bias and detection comparator.

A reference voltage can be output from the VREF terminal (pin 10) at levels up to 10mA.

(2) Triangular-wave oscillator circuit (OSC)

This circuit is used to generate a triangular oscillator waveform, by connecting timing capacitor and resistor to the CT terminal (pin 2) and RT terminal (pin 1) respectively. The triangular waveform frequency fosc1 is set according to the timing capacitor and resistor.

The triangular oscillator waveform is input to the IC's internal dead time timing circuit (One-Shot-DTC), and can be output from the CT terminal.

(3) Oscillator frequency control circuit (OSC Control)

The oscillator control circuit detects the AC/DC converter output voltage and outputs the PFM control signal to the triangular wave oscillator. The FB terminal (pin 5) carries the AC/DC converter output voltage at the V/I converted OSC control current. When an overload occurs, the detection signal to the overload detection circuit (OCP Comp.) is also output here.

(4) Dead time timing circuit (One-Shot-DTC)

The dead time timing circuit converts the triangular waveform generated by the triangular wave oscillator to a rectangular wave having a pulse width (= dead time t_{DEAD}) set by the dead time setup resistor that is connected to the RD terminal (pin 3).

(5) Output circuit (Drive)

The output circuit has totem pole configuration, and outputs the PFM signal from the OUT terminal (pin 8). The output circuit power is supplied from the Vcc (O) terminal (pin 9).

2. Protective Function

(1) Undervoltage lockout circuit (UVLO)

Power-on surges and momentary drops in power supply voltage can cause errors in control IC operation, which can destroy or damage systems. To prevent the error operation, the UVLO Comp.1 circuit detects low voltage conditions in the supply voltage (Vcc), and sets the VREF terminal (pin 10) to "L" level. The UVLO Comp.2 circuit detects low voltage conditions in the reference voltage, and sets the OUT pin (pin 8) to "L" level.

Overvoltage/overload/over temperature conditions cause the error detection latch (Latch) to be set. If the VREF terminal (pin 10) is set to "L" level, and the supply voltage falls below the UVLO circuit threshold voltage (VTHL), the UVLO Comp.1 resets the error detection latch. Operation is restored when the power supply voltage returns above the threshold voltage (VTHL) of the UVLO circuit.

The threshold voltage can be set to any desired level by connecting resistor between the ENB terminal (pin 12) and GND terminal (pin 7), or between the ENB terminal (pin 12) and Vcc terminal (pin 11) (for internal resistance constants see "BLOCK DIAGRAM").

(2) Overvoltage detection comparator 1 (OVP Comp. 1)

When the input voltage at the OVP terminal (pin 14) is greater than the threshold voltage (≒ 2.5V), the overvoltage comparator 1 sets the error detection latch, and sets the VREF terminal (pin 10) and OUT terminal (pin 8) to "L" level.

Note that if OVP Comp.1 is not used, the OVP terminal (pin 14) should be shorted to GND by the shortest path (see "PROCESSING WHEN OVP PIN IS NOT USED").

(3) Overvoltage detection comparator 2 (OVP Comp.2)

When the input voltage at the +IN terminal (pin 15) is greater than the input voltage at the -IN terminal (pin 16), the CS terminal is set to “L” level causing the frequency to increase. When the +IN input voltage falls below the -IN input voltage, soft start processing is performed to restart operation. Overvoltage detection comparator 2 does not provide the same latch operation as OVP Comp.1.

Note that if OVP Comp.2 is not used, the +IN terminal (pin 15) should be shorted to GND, and the -IN terminal (pin 16) should be connected to the VREF terminal (pin 10) by the shortest path (see “PROCESSING WHEN OVERVOLTAGE DETECTION COMPARATOR 2 IS NOT USED”).

(4) Overload detection comparator circuit (OCP Comp.)

When an overload occurs, the OCP Comp. circuit detects the overload signal output by the oscillator frequency control circuit, and after a given interval sets the error detection latch and sets the VREF terminal (pin 10) and OUT terminal (pin 8) to “L” level. The time interval from overload detection to setting of the error latch is determined by the delay interval setting capacitor connected to the CD terminal (pin 4).

Note that if the overload detection function is not used, the CD terminal (pin 4) should be shorted to GND by the shortest path (see “PROCESSING WHEN THE CD PIN IS NOT USED”).

(5) Overtemperature detection comparator (OTP Comp.)

The over temperature detection comparator detects the input voltage at the OTP terminal (pin 13) and if greater than the threshold voltage (≒ 0.98V) sets the error detection latch, and sets the VREF terminal (pin 10) and OUT terminal (pin 8) to “L” level.

Note that if the overtemperature detection function is not used, the OTP terminal (pin 13) should be shorted to GND by the shortest path (see “PROCESSING WHEN OTP PIN IS NOT USED”).

3. Soft Start Function

Soft Start Circuit (CS)

The MB3873 oscillator frequency control circuit includes an on-chip soft start circuit. Soft starting can be provided by connecting a capacitor to the CS terminal (pin 6). At start up, this causes the PFM control signal to be input to the triangular wave oscillator, thereby controlling the control frequency and preventing current rush.

Note that if the soft start function is not used, the CS terminal (pin 6) should be left open. (See “PROCESSING WHEN CS PIN IS NOT USED.”)

■ SETTING THE OSCILLATOR FREQUENCY

The oscillator frequency is set by the timing capacitor C_T and timing resistor R_T connected to the CT pin and RT pin respectively.

Oscillator frequency f_{OSC} (when frequency control is not exerted by the FB, CS pins)

$$f_{OSC}\,[\mathrm{kHz}] \fallingdotseq \frac{7.6 \times 10^5}{C_T\,[\mathrm{pF}] \times R_T\,[\mathrm{k\Omega}]}$$

■ SETTING THE DEAD TIME

The dead time is set by the dead time resistor R_D connected to the RD pin.

Dead time (output pin square wave pulse width)

$$t_{DEAD}\,[\mathrm{ns}] \fallingdotseq 4.8 \times R_D\,[\mathrm{k\Omega}] - 44$$

■ SETTING THE SOFT START TIME

When the MB3873 is started, the soft start capacitor (Cs) connected to the CS terminal begins charging. While the CS terminal voltage is ≒ 0 to 1.1V, the oscillator frequency is controlled by the CS terminal voltage, thereby controlling the output voltage.

The soft start capacitor charging current is as follows

ICS1 ≒ 25 μA (CS pin voltage ≒ 0 to 1.1V)

ICS2 ≒ 2.5 μA (CS pin voltage ≒ 1.1 to 3.1V (CS pin clamp voltage))

Soft start time (time until CS pin voltage reaches 1.1V)

$$t_{CS}\ [s] \fallingdotseq \frac{1.2 \times C_S\ [\mu F]}{25\ [\mu A]}$$

■ SETTNG THE OVERLOAD DETECTION DELAY TIME

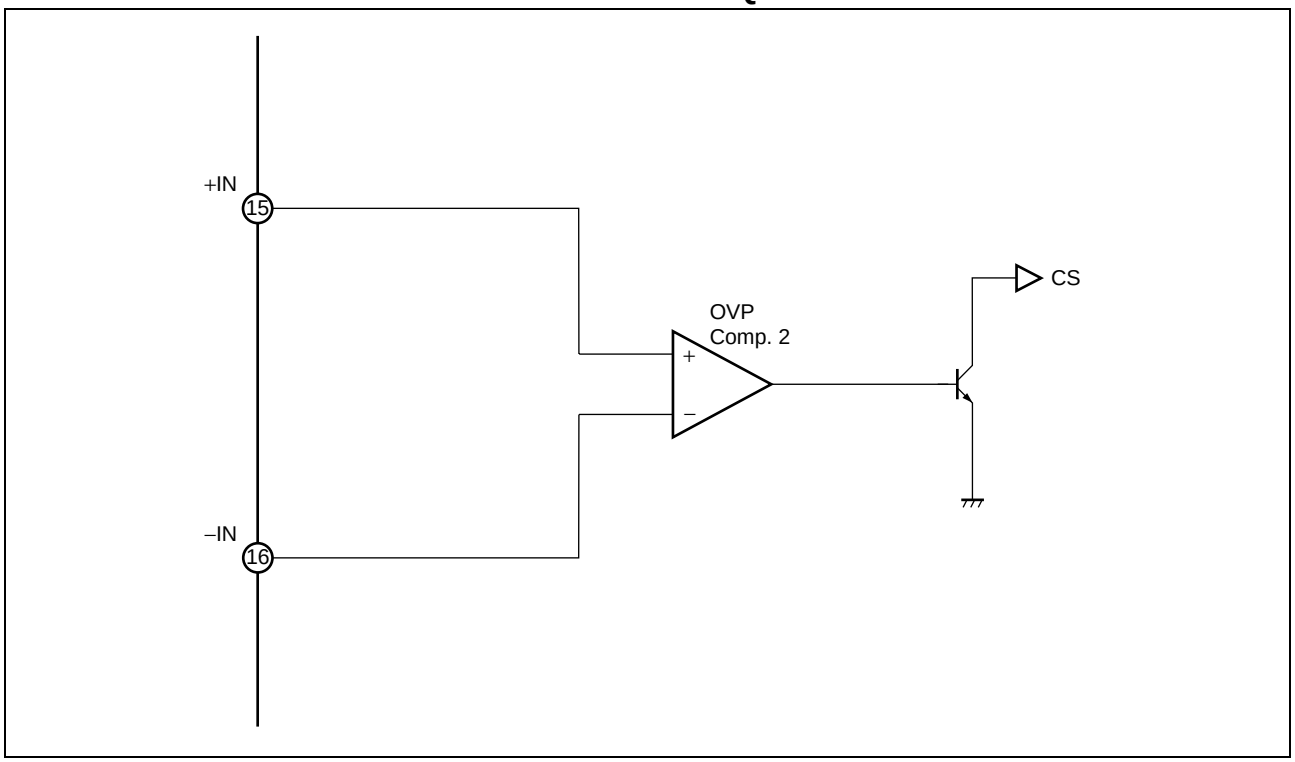
When an overload condition is detected, the delay capacitor (C_D) connected to the CD terminal starts charging (≒ 10 μA), increasing the CD terminal voltage.

When the CD terminal voltage exceeds the threshold voltage (≒ 4V), the error detection latch is set, and the VREF terminal (pin 10) and OUT terminal (pin 8) are set to “L” level.

Overload detection delay time (time from overload detection until error latch is set)

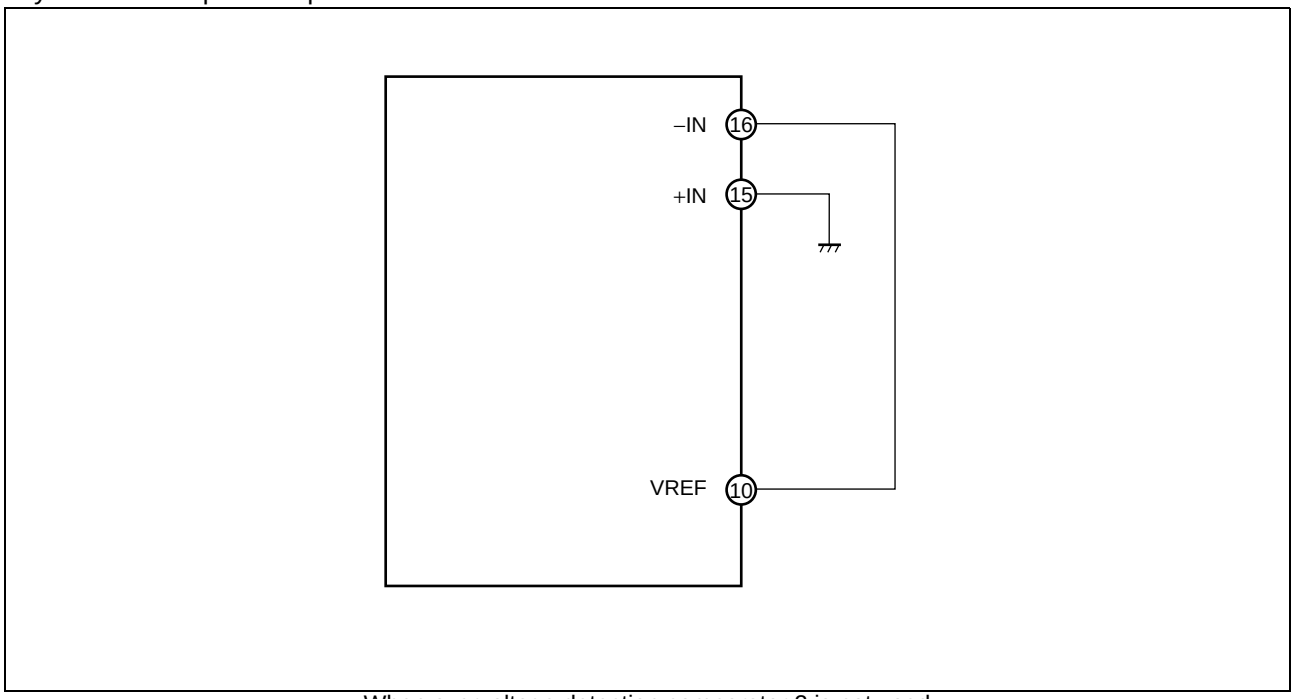
$$t_{CS}\ [s] \fallingdotseq \frac{3.9 \times C_D\ [\mu F]}{10\ [\mu A]}$$

■ OVERVOLTAGE DETECTION COMPARATOR 2 EQUIVALENT CIRCUIT



■ PROCESSING WHEN OVERVOLTAGE DETECTION COMPARATOR 2 IS NOT USED

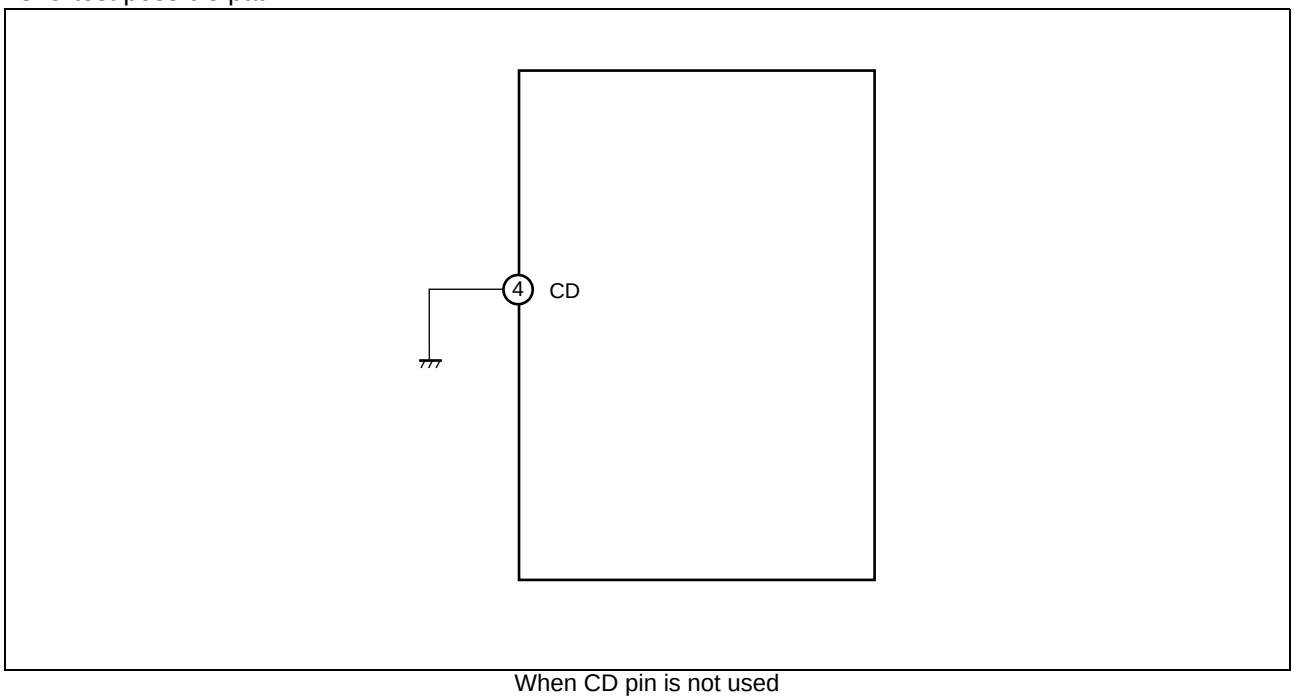
When the overvoltage detection comparator 2 is not used, the +IN terminal (pin 15) should be shorted to GND by the shortest possible path, and the -IN terminal (pin 16) should be connected to the VREF terminal (pin 10) by the shortest possible path.



When overvoltage detection comparator 2 is not used

■ PROCESSING WHEN CD PIN IS NOT USED

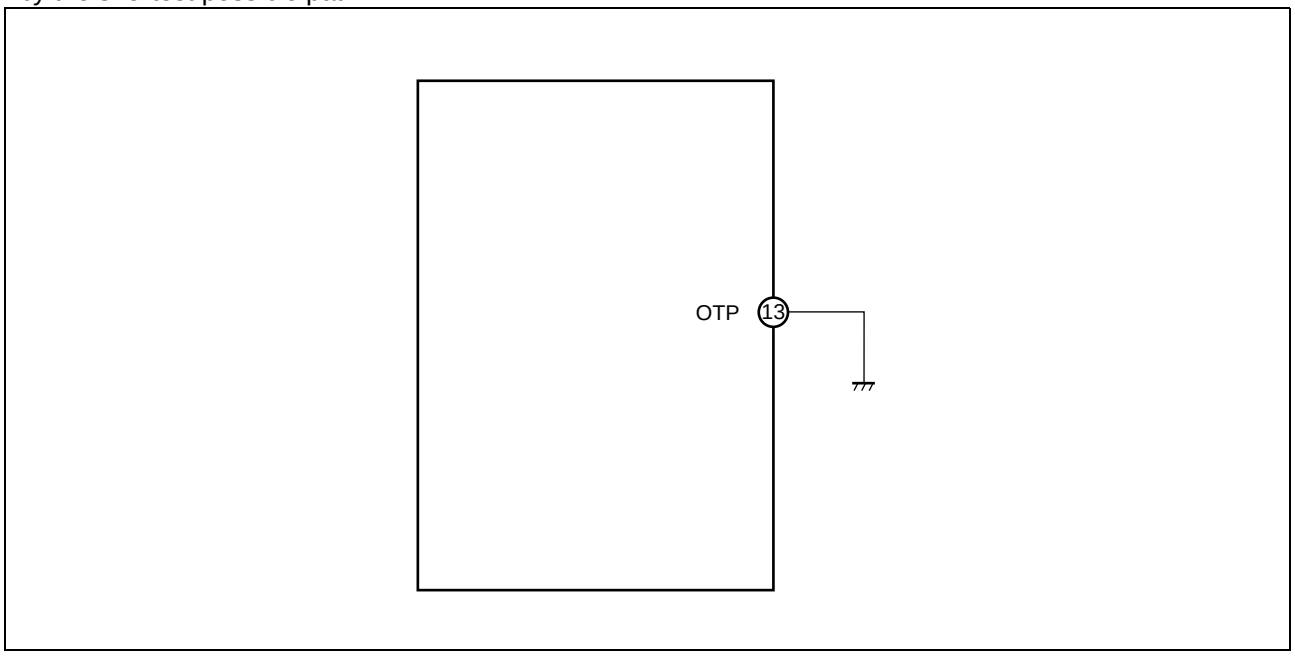
When the overload detection function is not used, the CD terminal (pin 4) should be shorted to GND by the shortest possible path.



When CD pin is not used

■ PROCESSING WHEN OTP PIN IS NOT USED

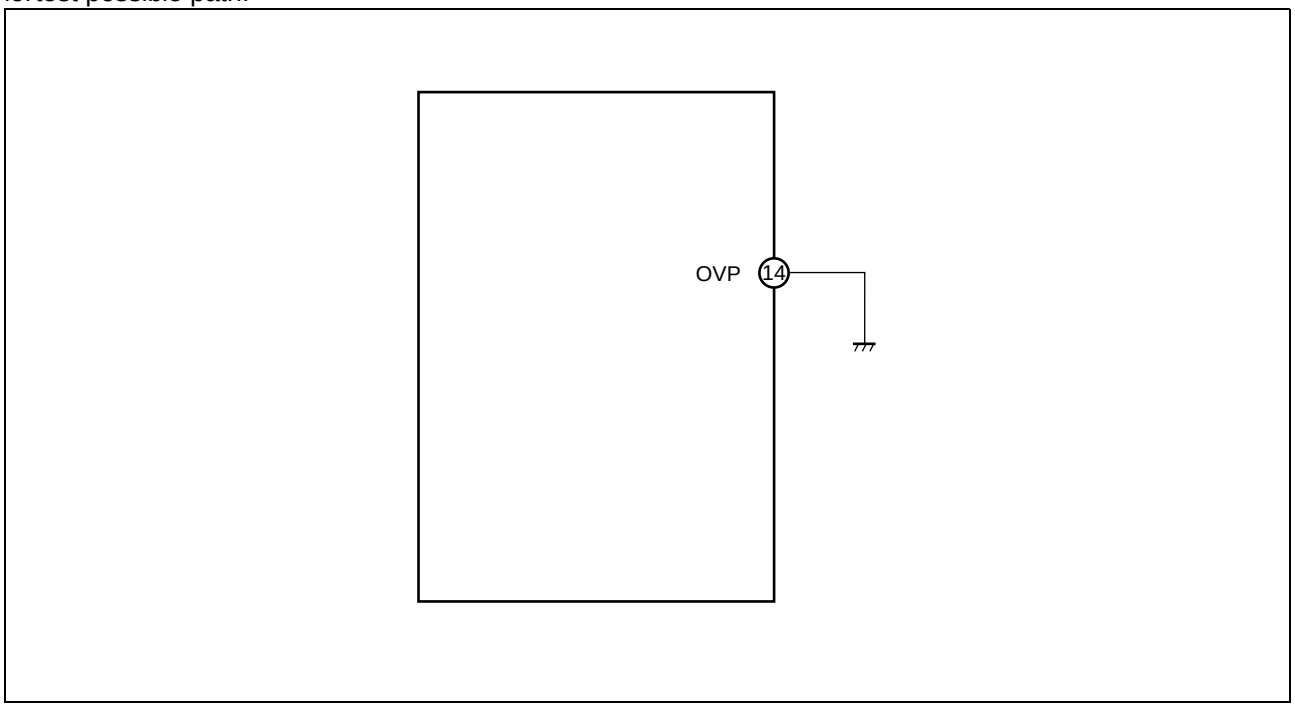
When the over temperature detection function is not used, the OTP terminal (pin 13) should be shorted to GND by the shortest possible path.



When OTP pin is not used

■ PROCESSING WHEN OVP PIN IS NOT USED

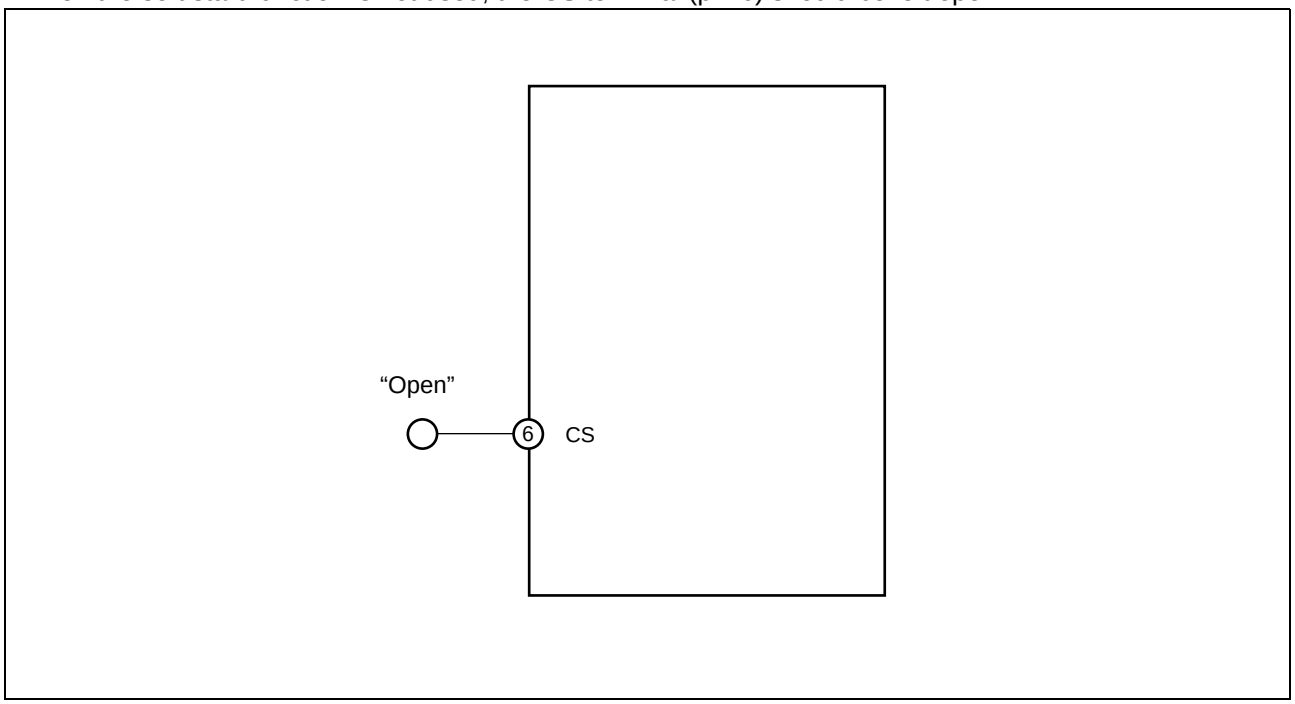
When the overvoltage detection function is not used, the OVP terminal (pin 14) should be shorted to GND by the shortest possible path.



When OVP pin is not used

■ PROCESSING WHEN CS PIN IS NOT USED

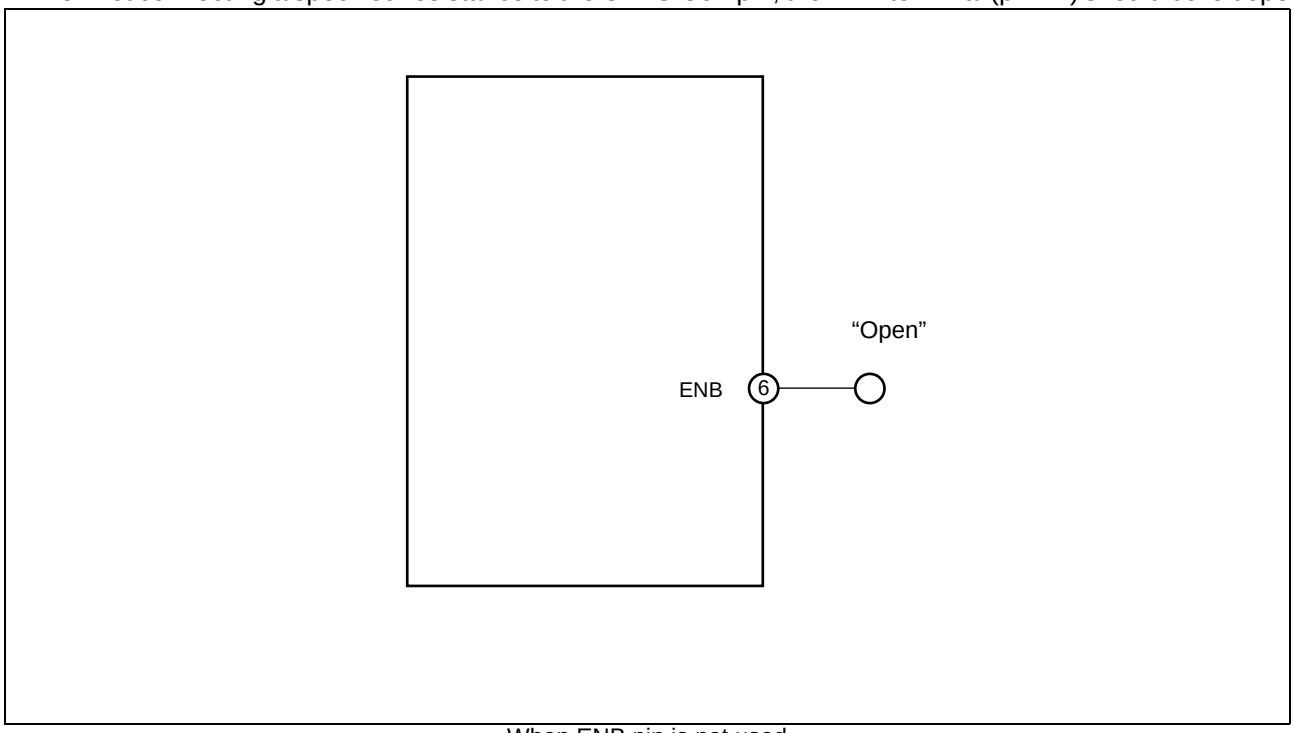
When the soft start function is not used, the CS terminal (pin 6) should be left open.



When the soft start time is not set

■ PROCESSING WHEN ENB PIN IS NOT USED

When not connecting a specified resistance to the UVLO Comp.1, the ENB terminal (pin 12) should be left open.



When ENB pin is not used

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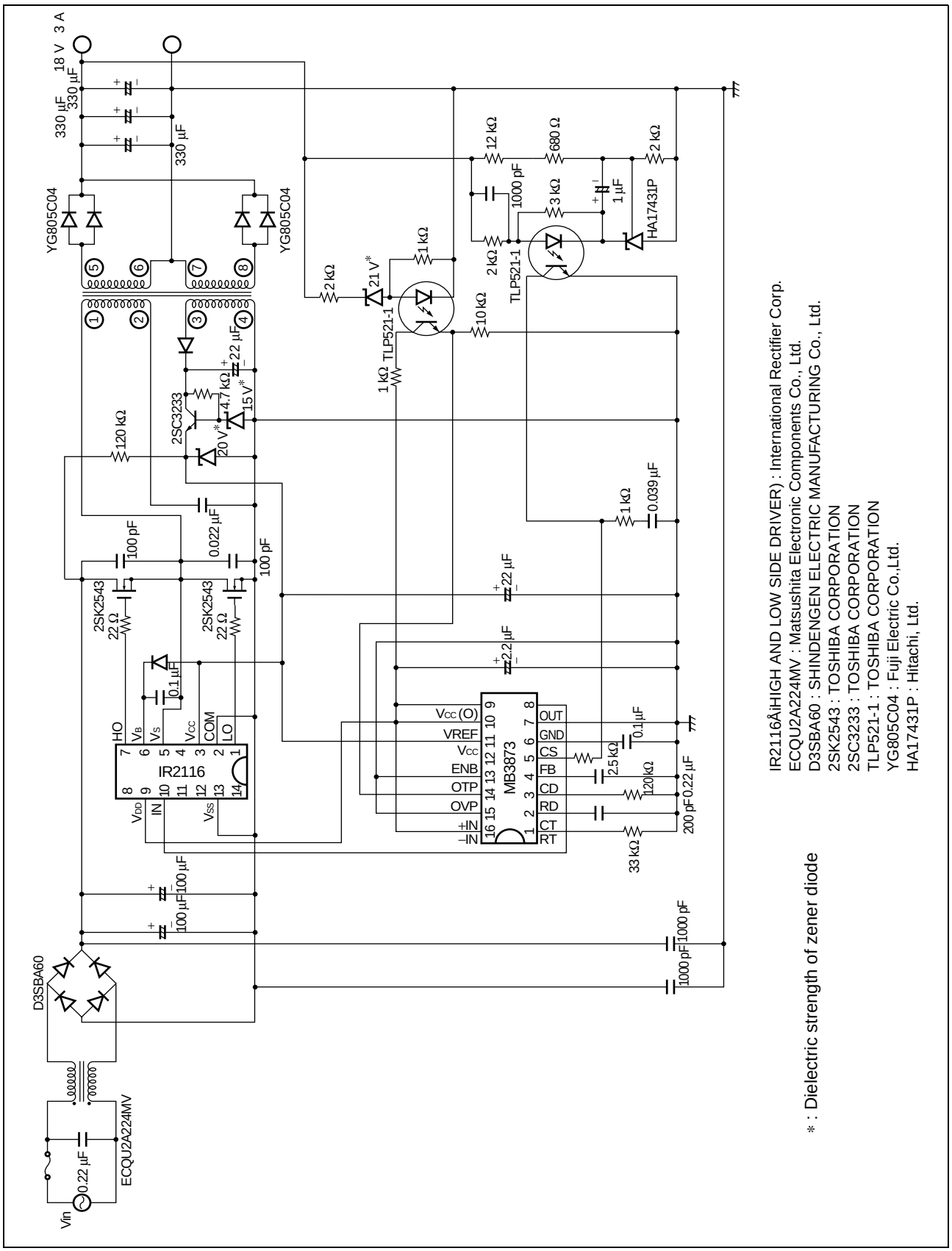
■ APPLICATION EXAMPLE

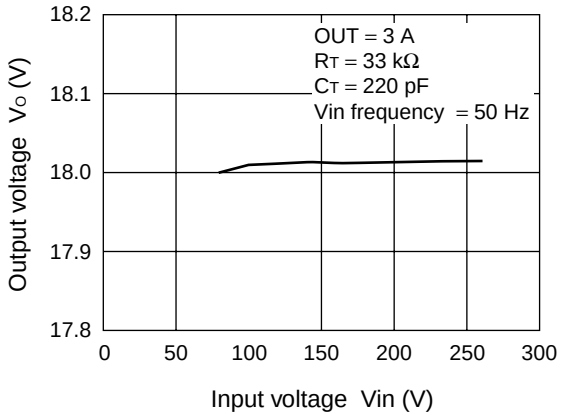


IR2116ÅiHIGH AND LOW SIDE DRIVER) : International Rectifier Corp.
ECQU2A224MV : Matsushita Electronic Components Co., Ltd.
D3SBA60 : SHINDENGEN ELECTRIC MANUFACTURING Co., Ltd.
2SK2543 : TOSHIBA CORPORATION
2SC3233 : TOSHIBA CORPORATION
TLP521-1 : TOSHIBA CORPORATION
YG805C04 : Fuji Electric Co.,Ltd.
HA17431P : Hitachi, Ltd.

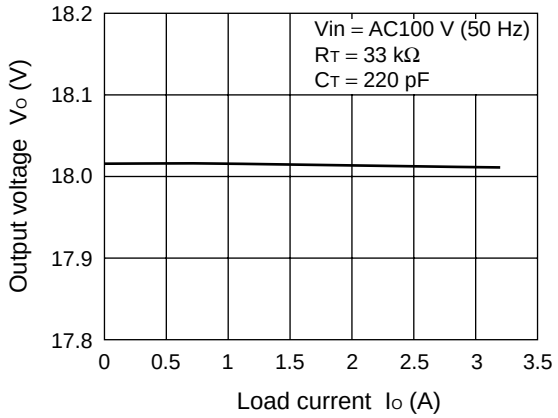
* : Dielectric strength of zener diode

■ REFERENCE DATA

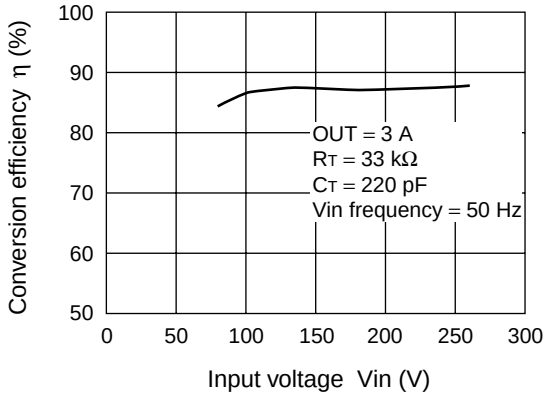
Output voltage vs. input voltage (Output voltage = 18 V)



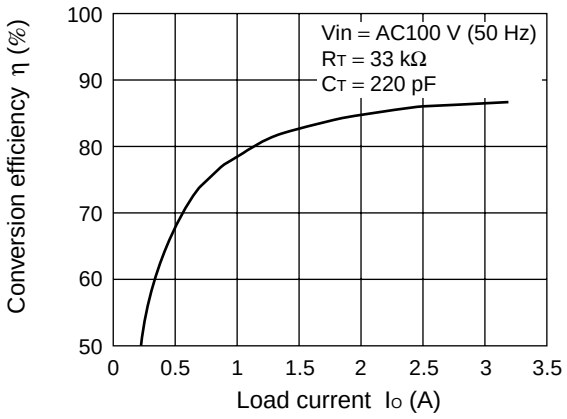
Output voltage vs. load current (Output voltage = 18 V)



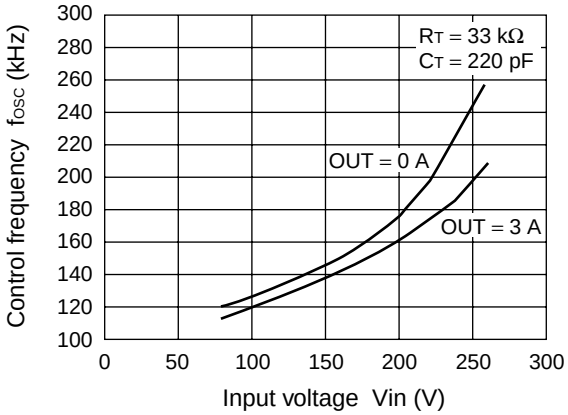
Conversion efficiency vs. input voltage
(Output voltage = 18 V)



Conversion efficiency vs. load current
(Output voltage = 18 V)



Control frequency vs. input voltage
(Output voltage = 18 V)



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■ USAGE PRECAUTIONS

1. Never use settings exceeding maximum rated conditions.

Exceeding maximum rated conditions may cause permanent damage to the LSI.
Also, it is recommended that recommended operating conditions be observed in normal use.
Exceeding recommended operating conditions may adversely affect LSI reliability.

2. Use this device within recommended operating conditions.

Recommended operating conditions are values within which normal LSI operation is warranted. Standard electrical characteristics are warranted within the range of recommended operating conditions and within the listed conditions for each parameter.

3. Printed circuit board ground lines should be set up with consideration for common impedance.

4. Take appropriate static electricity measures.

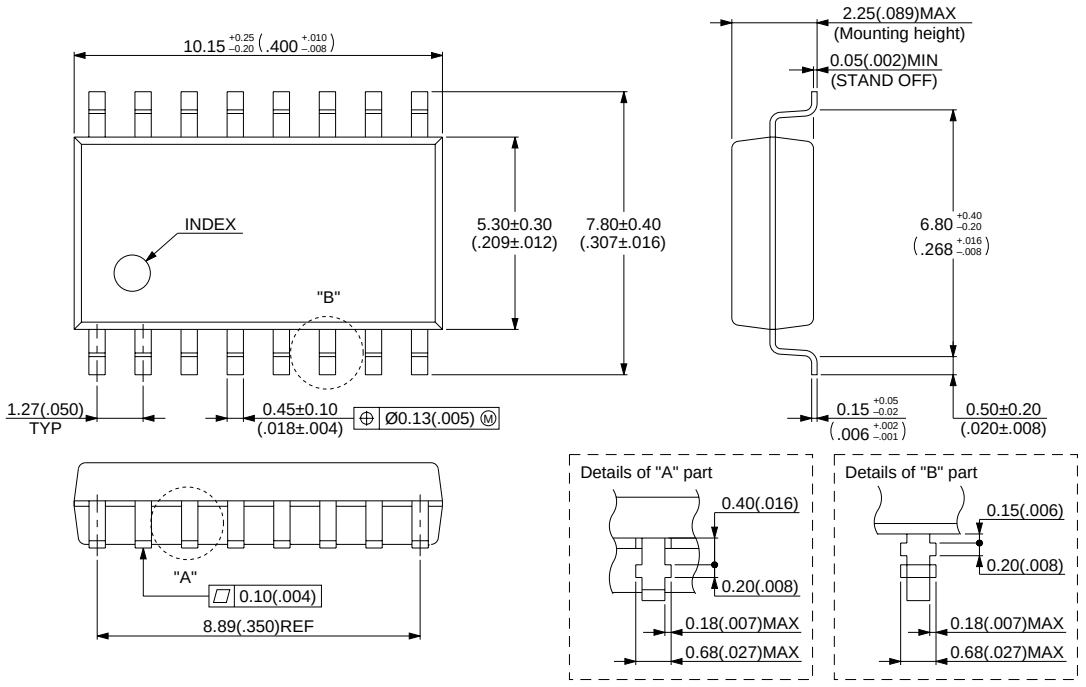
- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB3873PF	16-pin plastic SOP (FPT-16P-M06)	

■ PACKAGE DIMENSION

16-pin Plastic SOP
(FPT-16P-M06)



Dimension in mm (inches)

MB3873

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