FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27203-5E

ASSP

SWITCHING REGULATOR CONTROLLER

MB3778

■ DESCRIPTION

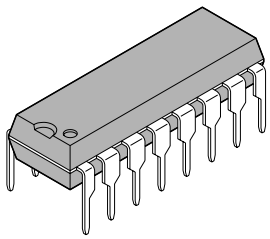
The MB3778 is a dual switching regulator control IC. It has a basic circuit that controls PWM system switching regulator power for two channels. Complete synchronization is achieved by using the same oscillator output. This IC can accept any two of the following types of output voltage: step-down, step-up, or voltage inversion (inverting voltage can be output to only one circuit). The MB3778's low power consumption makes it ideal for use in portable equipment.

■ FEATURES

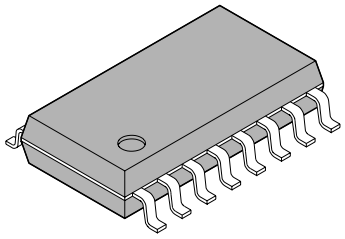
- Wide input voltage range: 3.6V to 18V
- Low current consumption: 1.7mA typ. at operation, 10µA max. at stand-by
- Wide oscillation frequency range: 1kHz to 500kHz
- On-chip timer latched short-circuit sensing circuit
- Under-voltage lockout for low V_{CC} conditions
- On-chip 2.46V reference voltage circuit: 1.23V output can be obtained from R_T terminal
- Variable dead-time provides control over total range
- On-ship stand-by function: power on/off function

■ PACKAGES

(DIP-16P-M04)



(FPT-16P-M06)



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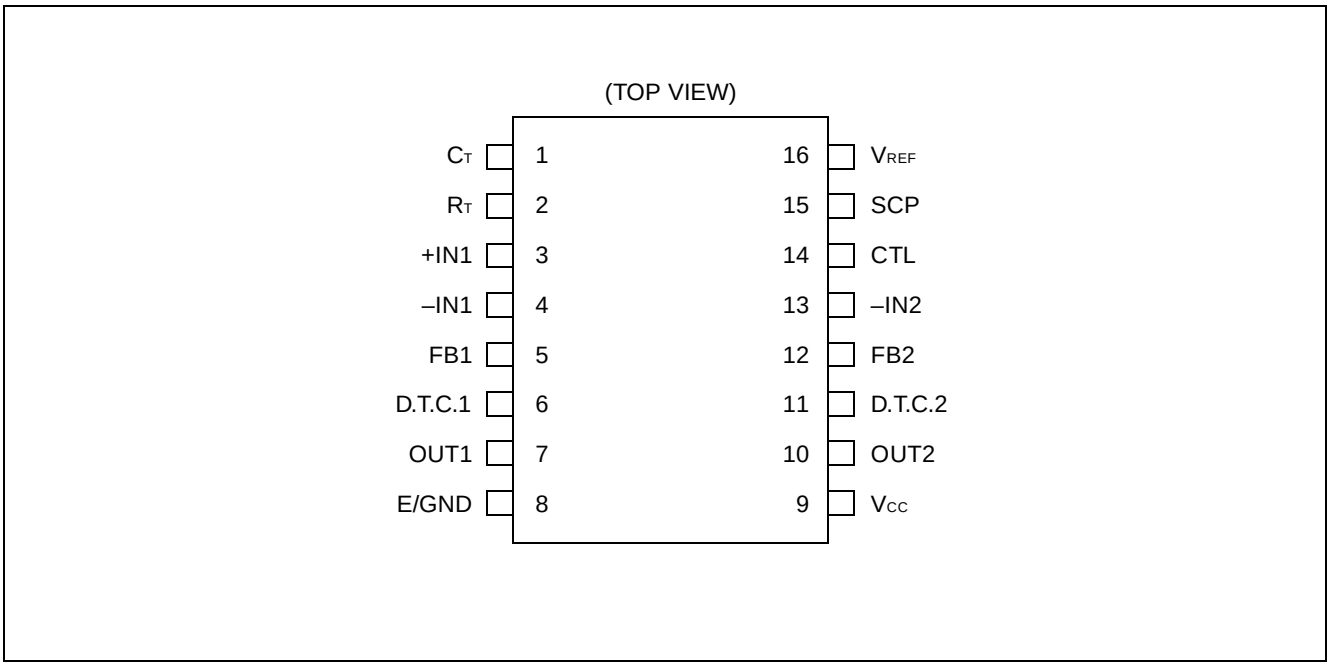
■ PIN ASSIGNMENT



■ ABSOLUTE MAXIMUM RATINGS (See NOTE)

(T_A = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{CC}	—	20	V
Error Amp. Input Voltage	V_{IN}	—	–0.3 to +10	V
Control Input Voltage	V_{CTL}	—	–0.3 to +20	V
Collector Output Voltage	V_{OUT}	—	20	V
Collector Output Current	I_{OUT}	—	75	mA
Power Dissipation	P_D	$T_A \leq 25°C$ (SOP)	*620	mW
		$T_A \leq 25°C$ (DIP)	1000	mW
Operating Temperature	T_{op}	—	–30 to +85	°C
Storage Temperature	T_{stg}	—	–55 to +125	°C

* : The packages are mounted on the epoxy board (4cm × 4cm × 1.5mm)

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ PIN/ASSIGNMENT

No.	Pin	Function
1	C_T	Oscillator timing capacitor pin (150 to 15,000pF).
2	R_T	Oscillator timing resistor pin (5.1 to 100kΩ). $V_{REF} \times 1/2$ is also available at this pin for error amplifier reference input.
3	+IN1	Non-inverted input error amplifier 1.
4	–IN1	Inverted input error amplifier 1.
5	FB1	Output pin error amplifier 1. A resistor and a capacitor are connected between this terminal and the –IN1 terminal to adjust gain and frequency.
6	DTC1	OUT1 dead-time control. Dead-time control is adjusted by an external resistive divider connected to the V_{REF} pin. A capacitor connected between this terminal and GND enables soft-start operation.
7	OUT1	Open collector output. Output transistor has common ground independent of signal ground. This output can source or sink up to 50mA.
8	E/GND	Ground.
9	V_{CC}	Power (3.6 to 18V)
10	OUT2	Open collector output. Output transistor has common ground independent of signal ground. This output can source or sink up to 50mA.
11	DTC2	Sets the dead-time of OUT2. The use of this terminal is the same as that of DTC1.
12	FB2	Output terminal of error amplifier 2. Sets the gain and adjusts the frequency when a resistor and a capacitor are connected between this terminal and the –IN2 terminal. Voltage of $V_{REF} \times 1/2$ is internally connected to the non-inverting input of error amplifier 2. Use error amplifier 2 for positive voltage output.
13	–IN2	Inverting input terminal of error amplifier 2.
14	CTL	Power control terminal. The IC is put in the stand-by state when this terminal is pulled "Low". Current consumption is 10µA or lower in the stand by state. The input can be driven by TTL or CMOS.
15	SCP	Connects the time constant setting capacitor of the timer latch short-circuit protection circuit. Connect a capacitor between this pin and GND. For details, see "How to set time constant for timer latch short-circuit protective circuit".
16	V_{REF}	2.46V reference voltage output terminal which can source up to 1mA. This pin is used to set the reference input and idle period of the error amplifiers.

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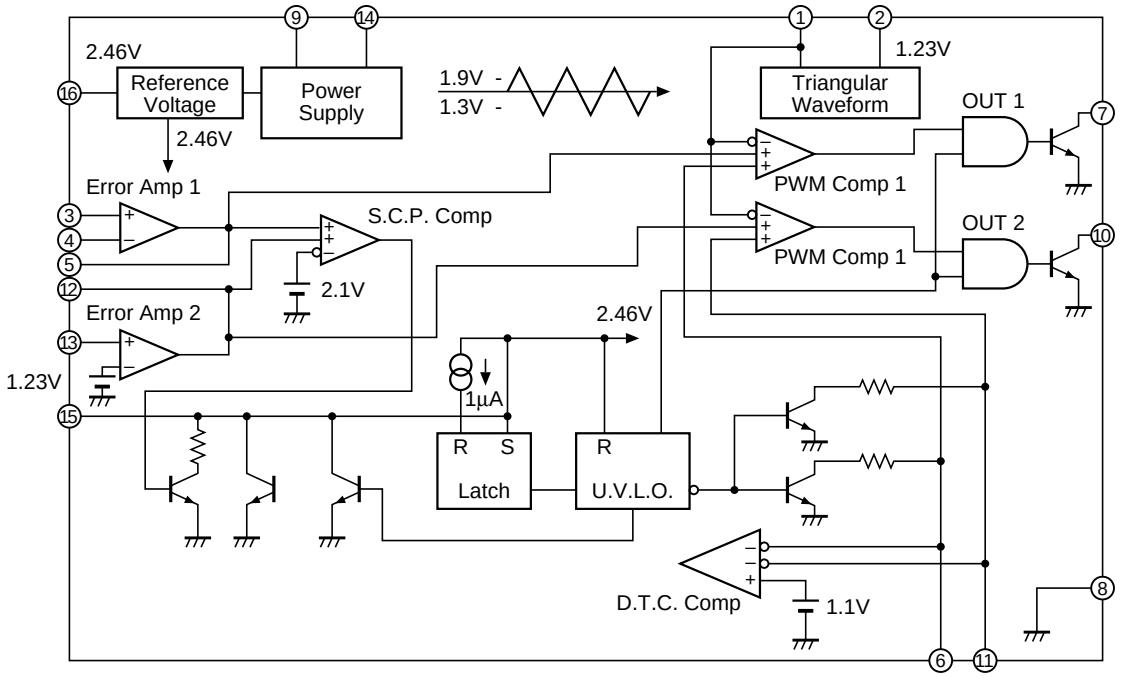
■ BLOCK DIAGRAM

Figure 1 MB3778 Block Diagram



■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	3.6	6.0	18	V
Error Amp. Input Voltage	V_{IN}	1.05	—	1.45	V
Control Input Voltage	V_{CTL}	0	—	18	V
Collector Output Voltage	V_{OUT}	—	—	18	V
Collector Output Current	I_{OUT}	0.3	—	50	mA
Timing Capacitor	C_T	150	—	15000	pF
Timing Resistor	R_T	5.1	—	100	kΩ
Oscillator Frequency	f_{OSC}	1	—	500	kHz
Operating Temperature	T_{op}	–30	25	85	°C

■ OPERATION DESCRIPTION

1. Reference voltage circuit

The reference voltage circuit generates a temperature-compensated reference voltage (= 2.46V) from V_{CC} (pin 9). The reference voltage is used for internal circuit.
The reference is obtained from the V_{REF} terminal (pin 16).

2. Triangular wave oscillator

Triangular waveforms can be generated at any frequency by connecting a timing capacitor and resistor to the C_T terminal (pin 1) and to the R terminal (pin 2).
The amplitude of this waveform is from 1.3V to 1.9V. These waveforms are connected to the non-inverting inputs of the PWM comparator and can be output through the C_T terminal.

3. Error amplifiers (Error Amp.)

The error amplifier detects the output voltage of the switching regulator and outputs PWM control signals.
The in-phase input voltage range is from 1.05V to 1.45V.
The reference voltage obtained by dividing the reference voltage output (recommended value: $V_{REF}/2$) or the R_T pin voltage (1.23V) is supplied to the non-inverting input.
The $V_{REF}/2$ voltage is internally connected to non-inverting input of the other error amplifier.
Any loop gain can be chosen by connecting the feedback resistor and capacitor to the inverting input terminal from the output terminal of the error amplifier.
Stable phase compensation is possible.

4. Timer latch short circuit protection circuit

This circuit detects the output levels of each error amplifier. If the output level of one or both of the error amplifiers is 2.1V or higher, the timer circuit begins charging the externally connected protection enable-capacitor.
If the output level of the error amplifier does not drop below the normal voltage range before the capacitor voltage reaches the transistor base-emitter voltage, V_{BE} ($\fallingdotseq$ 0.65V), the latch circuit turns the output drive transistor off and sets the idle period to 100%.

5. Under voltage Lock-out circuit

The transition state at power-on or a momentary power fluctuation may cause the control IC to malfunction, which may adversely affect or even destory the system. The under voltage lockout circuit monitors V_{CC} with reference to the internal reference voltage and resets the latch circuit to turn the output drive transistor off. The idle period is set to 100%. It also pulls the protection enable terminal (pin 15) "Low".

6. PWM comparator unit

Each PWM comparator has one inverting input and two non-inverting inputs. This voltage-to-pulse-width converter controls the output pulse width according to the input voltage.
The PWM comparator turns the output drive transistor on while triangular waveforms from the oscillator are lower than the error amplifier output and the dead time control terminal voltage.

7. Output drive transistor

The output drive transistors have open collector outputs with common source supply and common grounds independent of V_{CC} and signal ground. The output drive transistors can sink or source up to 50mA.

8. Power control unit

The power control terminal (pin 14) controls power on/off modes (the power supply current in stand-by mode is 10µA or lower).

■ ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{CC} = 6V)

Parameter	Condition	Symbol	Value			Unit
			Min.	Typ.	Max.	
Reference Section						
Output Voltage	I_{OR} = –1mA	V_{REF}	2.41	2.46	2.51	V
Output Temp. Stability	T_A = –30°C to +85°C	V_{RTC}	–2	±0.2	2	%
Input Stability	V_{CC} = 3.6V to 18V	Line	—	2	10	mV
Load Stability	I_{OR} = –0.1mA to –1mA	Load	—	1	7.5	mV
Short Circuit Output Current	V_{REF} = 0V	I_{OS}	–30	–10	–3	mA
Under Voltage Lockout Protection Section						
Threshold Voltage	I_{OR} = –0.1mA	V_{tH}	—	2.72	—	V
	I_{OR} = –0.1mA	V_{tL}	—	2.60	—	V
Hysteresis Width	I_{OR} = –0.1mA	V_{HYS}	80	120	—	mA
Reset Voltage (V_{CC})	—	V_R	1.5	1.9	—	V
Protection Circuit Section						
Input Thresold Voltage	—	V_{tPC}	0.60	0.65	0.7	V
Input Stand by Voltage	No pull up	V_{STB}	—	50	100	mV
Input Latch Voltage	No pull up	V_{IN}	—	50	100	mV
Input Source Current	—	I_{bpc}	–1.4	–1.0	–0.6	µA
Comparator Threshold Voltage	Pin 5, Pin 12	V_{tC}	—	2.1	—	V
Triangular Waveform Oscillator Section						
Oscillator Frequency	C_T = 330pF, R_T = 15kΩ	f_{OSC}	160	200	240	kHz
Frequency Deviation	C_T = 330pF, R_T = 15kΩ	f_{dev}	—	±5	—	%
Frequency Stability (V_{CC})	V_{CC} = 3.6V to 18V	f_{dV}	—	±1	—	%
Frequency Stability (T_A)	T_A = –30°C to +85°C	f_{dT}	–4	—	+4	%
Dead-Time Control Section						
Input Threshold Voltage (f_{OSC} = 10kHz)	Duty Cycle = 0%	V_{t0}	—	1.9	2.25	V
	Duty Cycle = 100%	V_{t100}	1.05	1.3	—	V
On Duty Cycle	V_{dt} = V_R/1.45V	D_{tr}	55	65	75	%
Input Bias Current	—	I_{bd}	—	0.2	1	µA
Latch Mode Sink Current	V_{dt} = 2.5V	I_{dt}	150	500	—	µA
Latch Input Voltage	I_{dt} = 100µA	V_{dt}	—	—	0.3	V

■ ELECTRICAL CHARACTERISTICS (Continued)

(T_A = 25°C, V_{CC} = 6V)

Parameter	Condition	Symbol	Value			Unit
			Min.	Typ.	Max.	
Error Amp. Section						
Input Offset Voltage	V_O = 1.6V	V_{IO}	–6	—	6	mV
Input Offset Current	V_O = 1.6V	I_{IO}	–100	—	100	nA
Input Bias Current	V_O = 1.6V	I_B	–500	–100	—	nA
Common Mode Input Voltage Range	V_{CC} = 3.6V to 18V	V_{ICR}	1.05	—	1.45	V
Voltage Gain	R_{NF} = 200kΩ	A_V	70	80	—	dB
Frequency Badn Width	A_V = 0dB	BW	—	1.0	—	MHz
Common Mode Rejection Ratio	—	CMRR	60	80	—	dB
Max. Output Voltage Width	—	V_{OM+}	V_{REF} –0.3	—	—	V
	—	V_{OM-}	—	0.7	0.9	V
Output Sink Current	V_O = 1.6	I_{OM+}	—	1.0	—	mA
Output Source Current	V_O = 1.6	I_{OM-}	—	–60	—	µA
PWM Comparator Section						
Input Threshold Voltage (f_{OSC} = 10kHz)	Duty Cycle = 0%	V_{t0}	—	1.9	2.25	V
	Duty Cycle = 100%	V_{t100}	1.05	1.3	—	V
Input Sink Current	Pin 5, Pin 12 = 1.6V	I_{IN+}	—	1.0	—	mA
Input Source Current	Pin 5, Pin 12 = 1.6V	I_{IN-}	—	–60	—	µA
Control Section						
Input Off Condition	—	V_{OFF}	—	—	0.7	V
Input On Condition	—	V_{ON}	2.1	—	—	V
Control Terminal Current	V_{CTL} = 10V	I_{CTL}	—	200	400	µA
Output Section						
Output Leak Current	V_O = 18V	Leak	—	—	10	µA
Output Saturation Voltage	I_O = 50mA	V_{SAT}	—	1.1	1.4	V
All Device Section						
Stand by Current	V_{CTL} = 0V	I_{CCS}	—	—	10	µA
Average Supply Current	V_{CTL} = V_{CC}, No Output Load	I_{CCa}	—	1.7	2.4	mA

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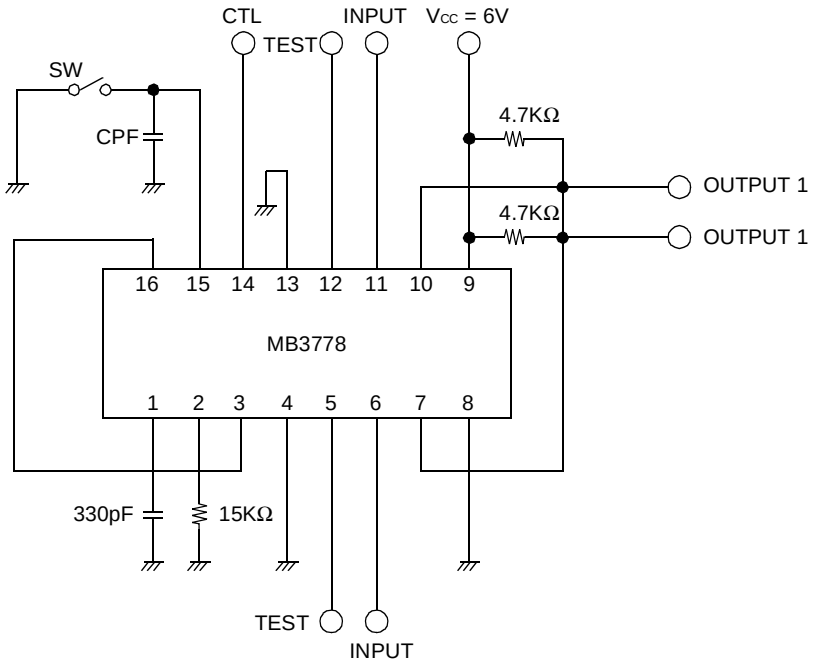
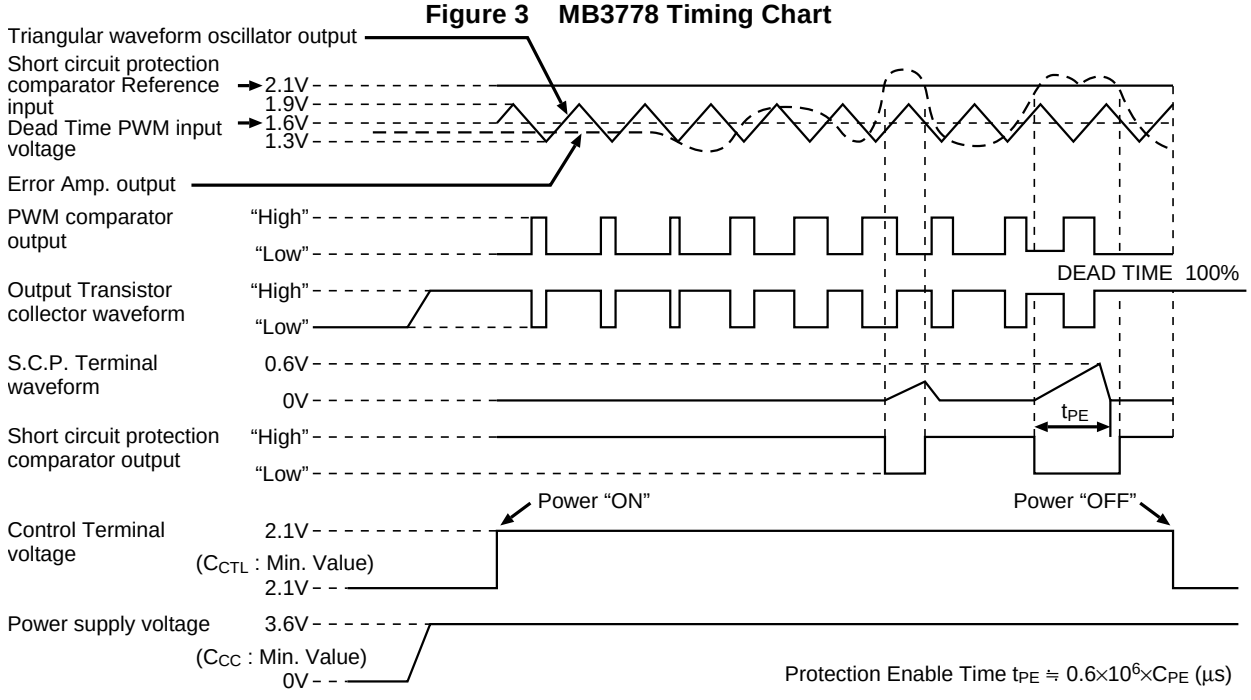
■ TEST CIRCUIT

Figure 2 MB3778 Test Circuit



■ TIMING CHART (Internal Waveform)

Figure 3 MB3778 Timing Chart



■ APPLICATION CIRCUIT

Figure 4 Chopper Type Step Down/Inverting

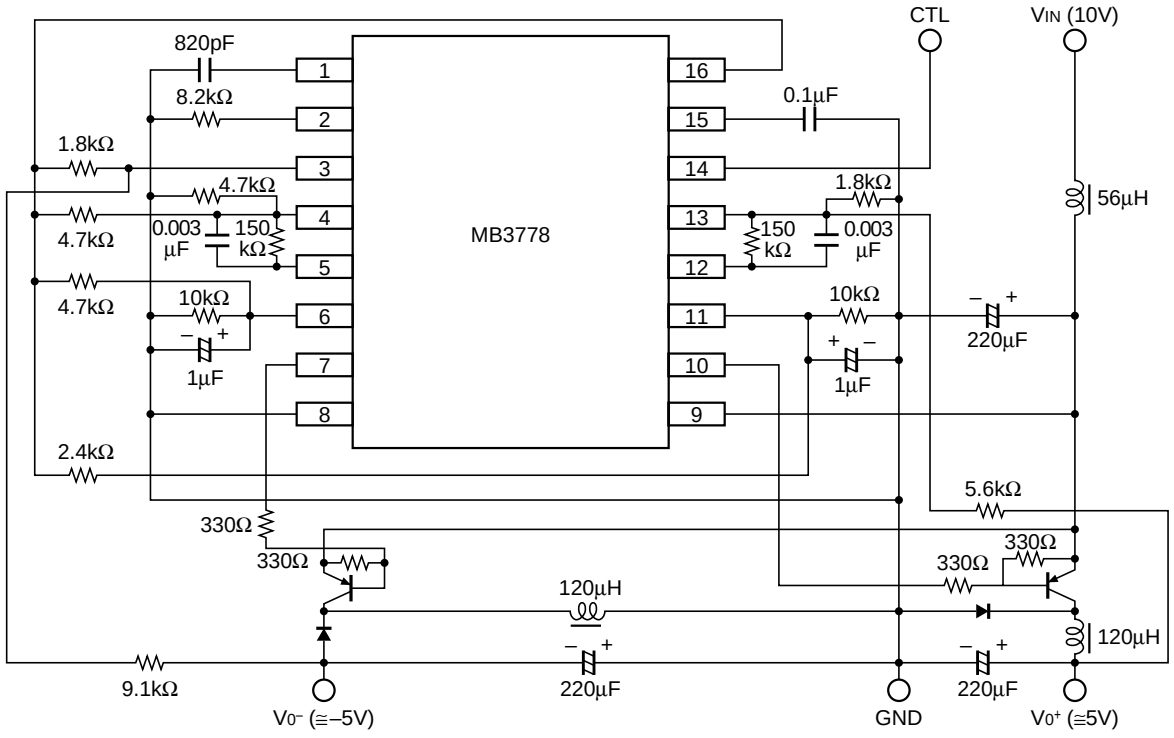
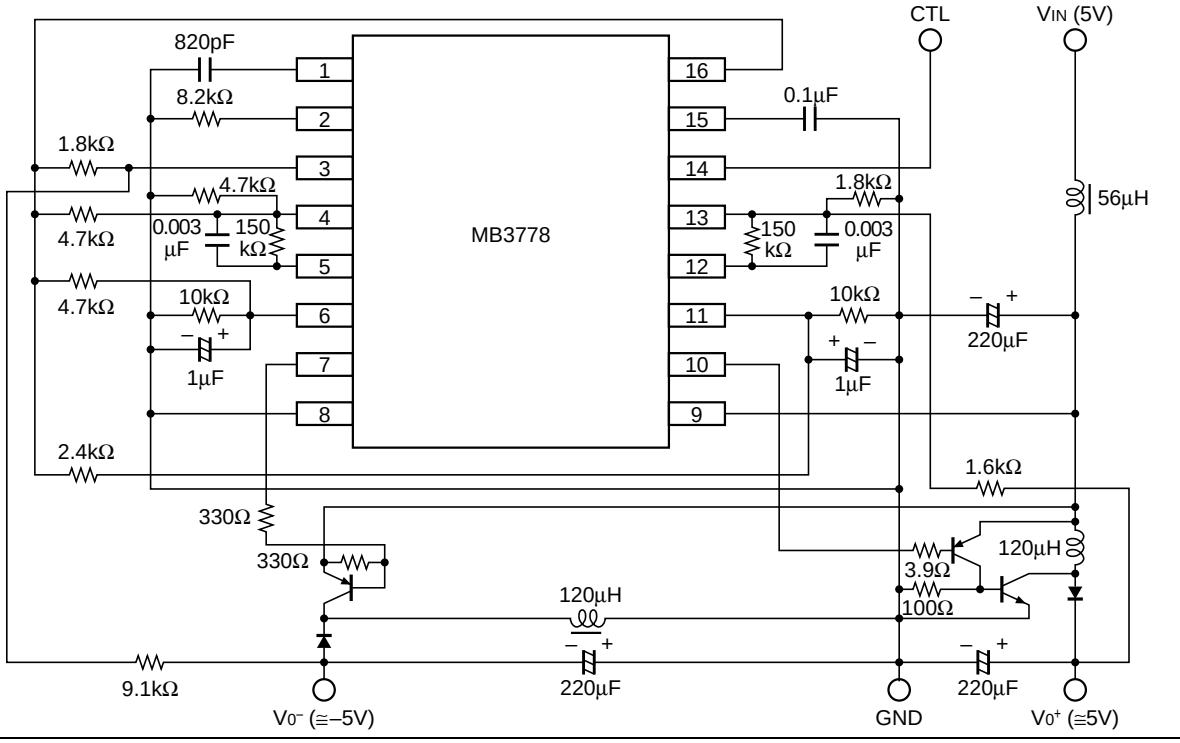


Figure 5 Chopper Type Step Up/Inverting



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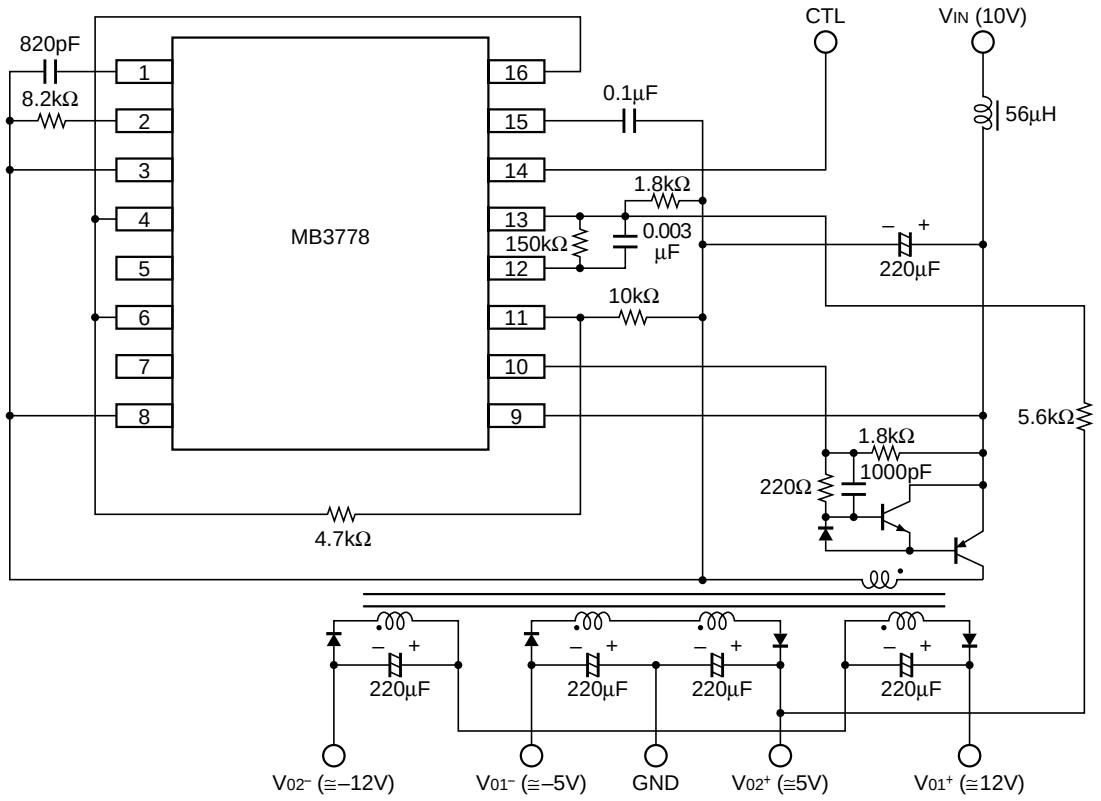
■ APPLICATION CIRCUIT (Continued)

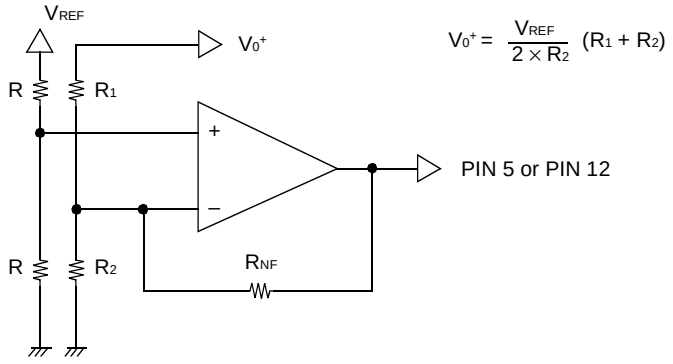
Figure 6 Multi Output Type (Apply Transformer)



■ HOW TO SET THE OUTPUT VOLTAGE

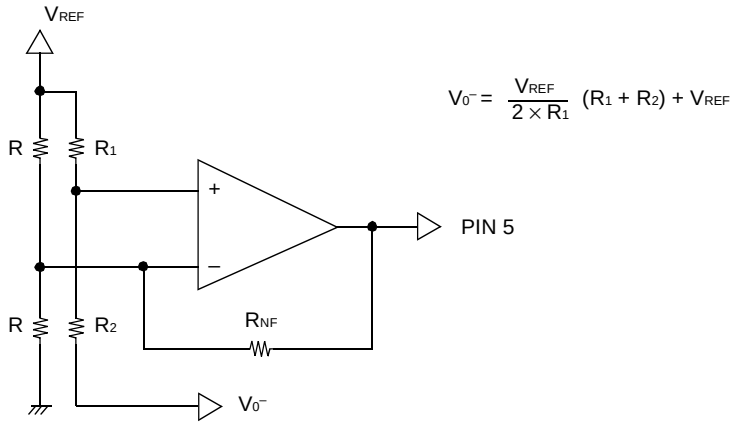
The output voltage is set using the connections shown in Fig. 7 and 8.
The error amplifiers power is supplied by the reference voltage circuit as are the other internal circuits. The in-phase voltage range is from 1.05V to 1.45V.
Set 1.23V ($V_{REF}/2$) to the reference input voltage that is connected to either inverting or non-inverting input terminals.

Figure 7 Connection of Error Amp. Output Voltage $V_0 \geq 0$



$$V_{0^+} = \frac{V_{REF}}{2 \times R_2} (R_1 + R_2)$$

Figure 8 Connection of Error Amp. Output Voltage $V_0 < 0$



$$V_{0^-} = \frac{V_{REF}}{2 \times R_1} (R_1 + R_2) + V_{REF}$$

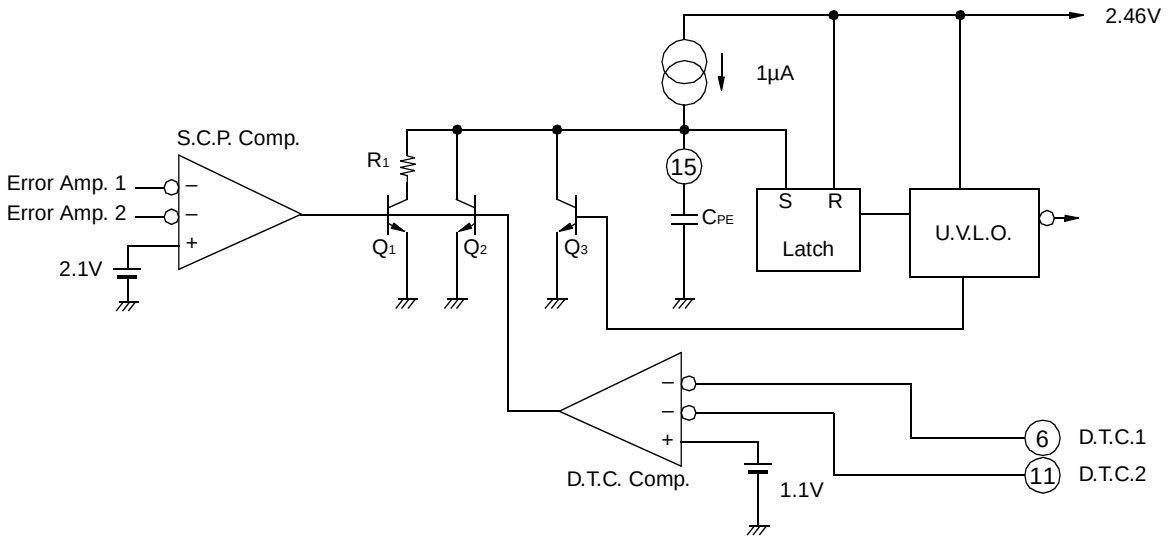
■ HOW TO SET TIME CONSTANT FOR TIMER LATCH SHORT-CIRCUIT PROTECTION CIRCUIT

Fig. 9 shows the configuration of the protection latch circuit.
Each error amplifier outputs is connected to the inverting inputs of the short-circuit protection comparator and are compared with the reference voltage (2.1V) connected to the non-inverting input.
When the load condition of the switching regulator is stable, the error amplifier has no output fluctuation. Thus, short-circuit protection control is also kept in balance, and the protection enable terminal (pin 15) voltage is held at about 50mV.
If the load changes drastically due to a load short-circuit and if the inverting inputs of the short-circuit protection comparator go above 2.1V, the short-circuit protection comparator output goes "Low" to turn off transistor Q_1. The protection enable terminal voltage is discharged, and then the short-circuit protection comparator charges the protection enable capacitor C_{PE} according to the following formula:

$$V_{PE} = 50mV + t_{PE} \times 10^{-6}/C_{PE}$$
$$0.65 = 50mV + t_{PE} \times 10^{-6}/C_{PE}$$
$$C_{PE} = t_{PE}/0.6\ (\mu F)$$

When the protection enable capacitor charges to about 0.65V, the protection latch is set to enable the under voltage lockout circuit and the output drive transistor is turned off. The idle period is also set to 100%.
Once the under voltage lockout circuit is enabled, the protection enable is released; however, the protection latch is not reset if the power is not turned off.
The non-inverting inputs of the D.T.C. comparator (pin 6 or 11) are compared to the reference voltage (about 1.8V) connected to the non-inverting input.
To prevent malfunction of the short-circuit protection-circuit under soft-start operation the D.T.C. comparator outputs a "High" level until the D.T.C. terminal voltage reaches about 1.1V, and then closes the protection enable terminal by turning transistor Q_2 on.

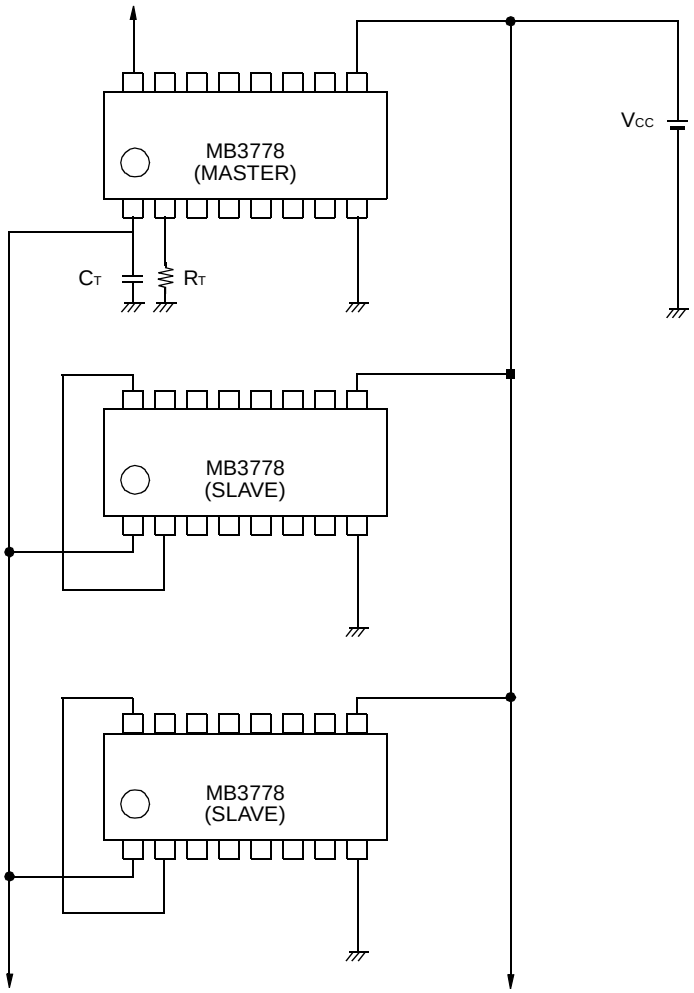
Figure 9 Protection Latch Circuit



■ SYNCHRONIZATION OF ICs

To synchronize MB3778 ICs, the specified capacitor and resistor are connected to the C_T and R_T terminals of the master IC. The R_T terminals (pin 2) of the slave ICs are connected to the V_{REF} terminal (pin 16) to disable the charge/discharge circuit for triangular wave oscillation. The C_T terminals of the master and slave ICs are connected together.

Figure 10 Connection of Master, Slave



■ TYPICAL PERFORMANCE CHARACTERISTICS

Figure 11 Power supply voltage vs. Reference voltage

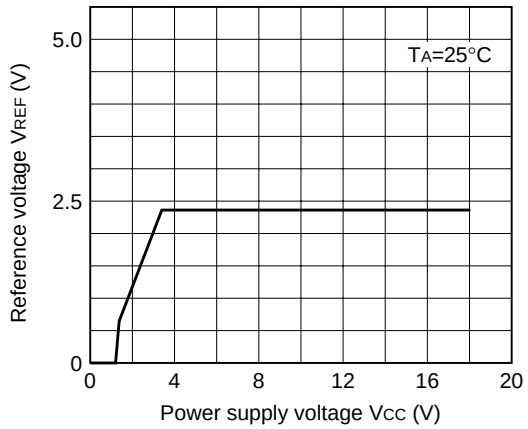


Figure 12 Power supply voltage vs. Average supply current

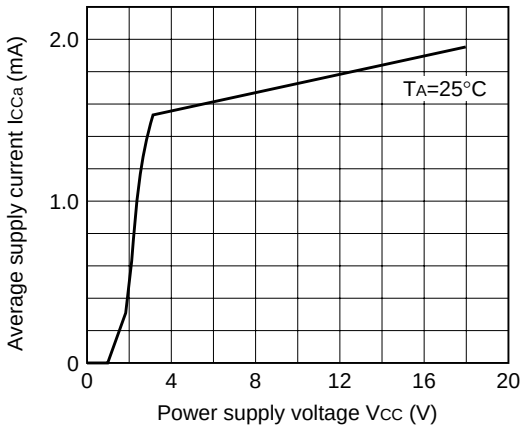


Figure 13 Reference voltage vs. Temp

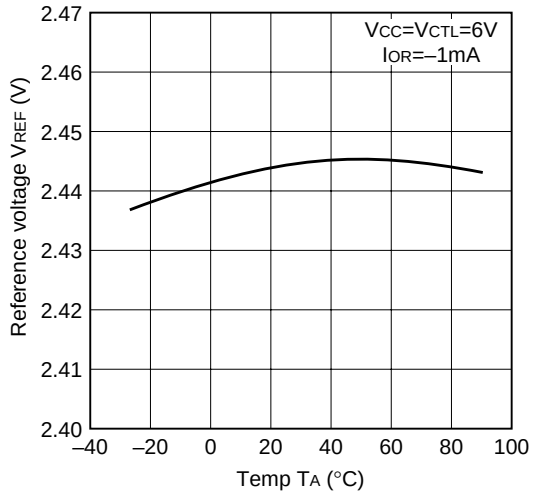


Figure 14 Timing capacitor vs. Triangular waveform Max. Amplitude voltage

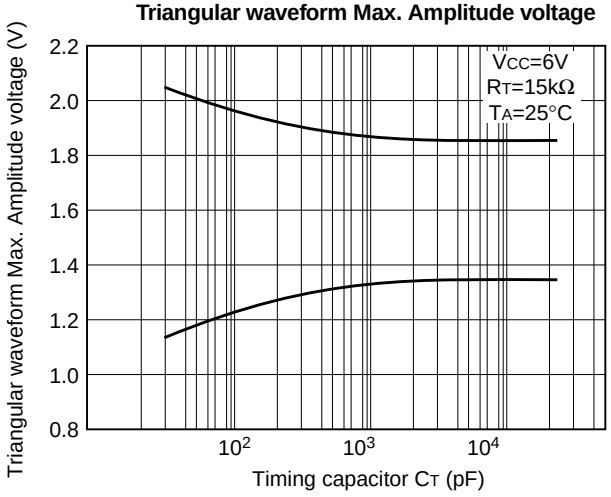


Figure 15 Collector saturation voltage vs. Sink Current

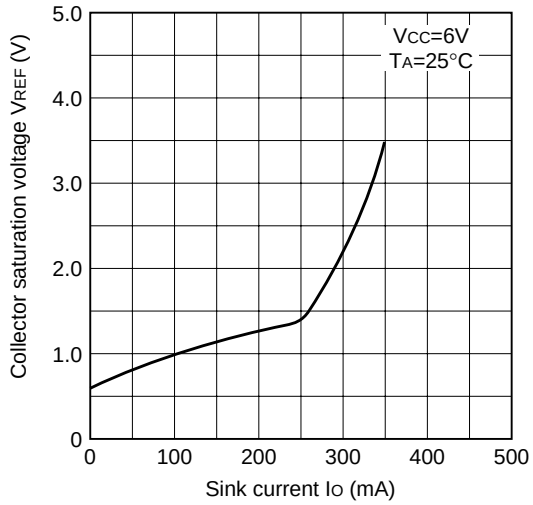
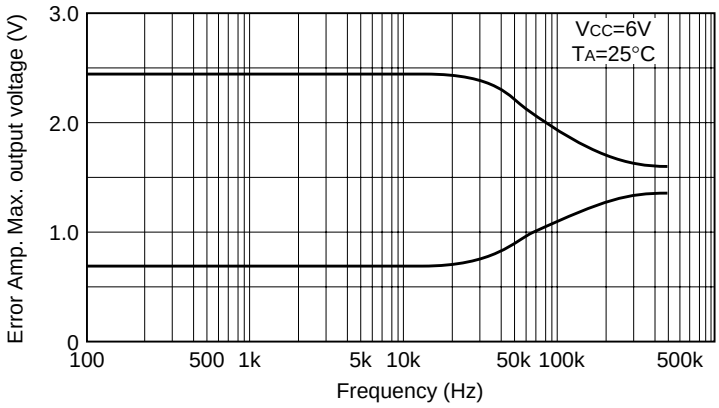


Figure 16 Error Amp. Max. output voltage vs. Frequency



■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Figure 17 Timing resistor vs. Oscillation frequency

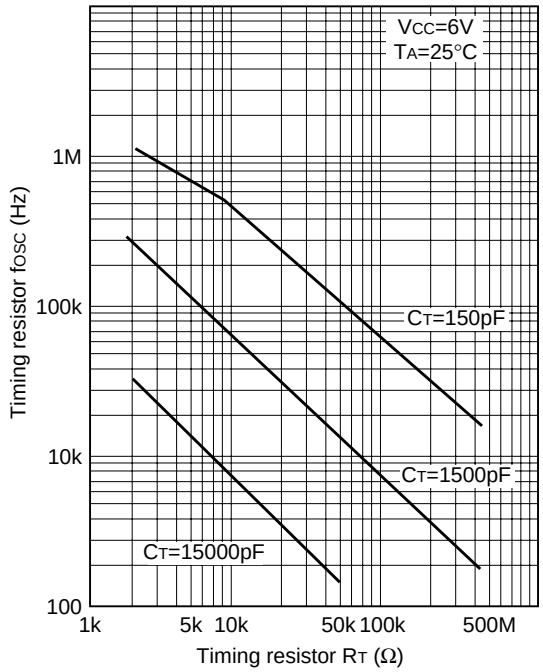


Figure 18 Triangular waveform cycle vs. Timing capacitor

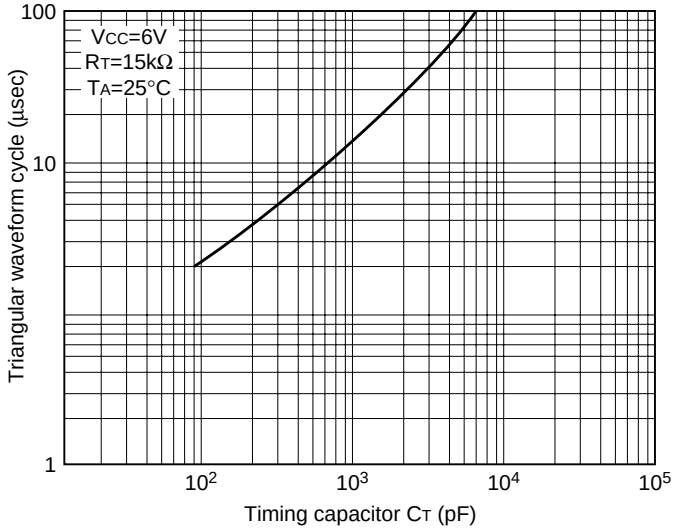


Figure 19 Temp. vs. Oscillation frequency

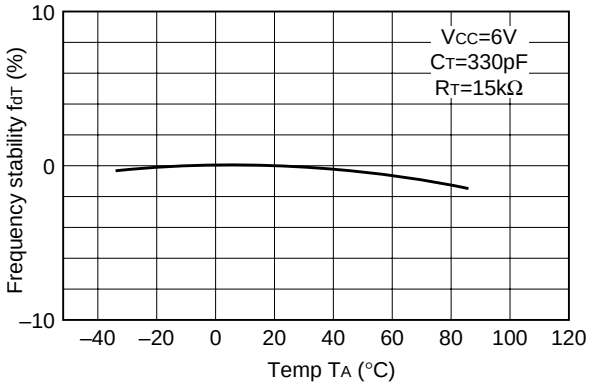


Figure 20 Oscillation frequency vs. Duty

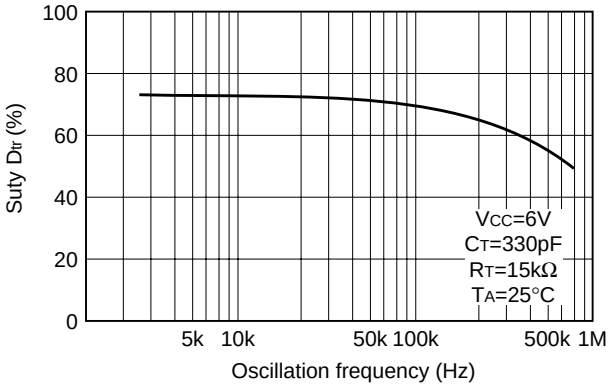


Figure 21 Control voltage vs. Reference voltage

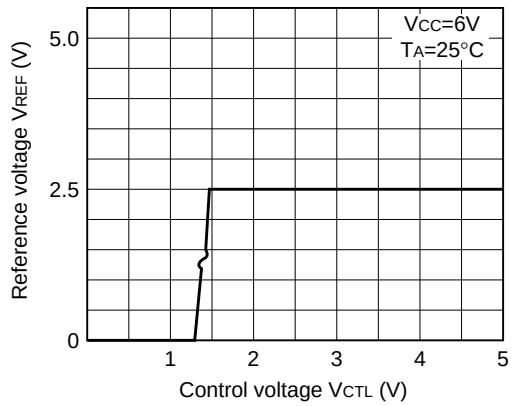
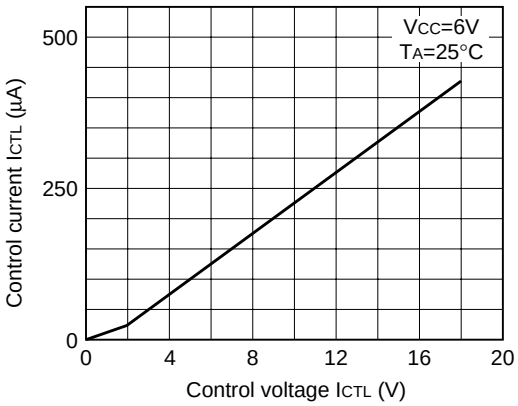


Figure 22 Control input current



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■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Figure 23 Frequency vs. Gain/Phase

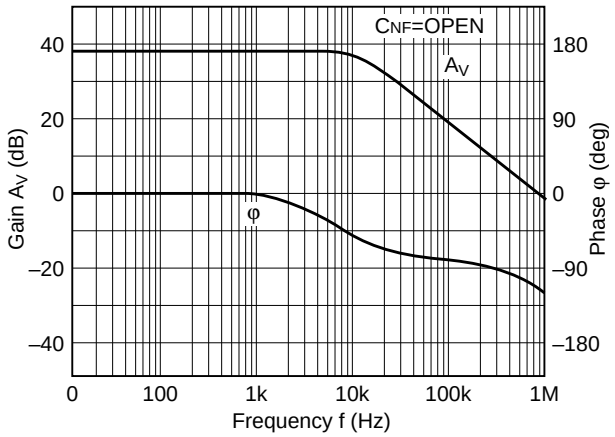


Figure 24 Frequency vs. Gain/Phase (Actual Data)

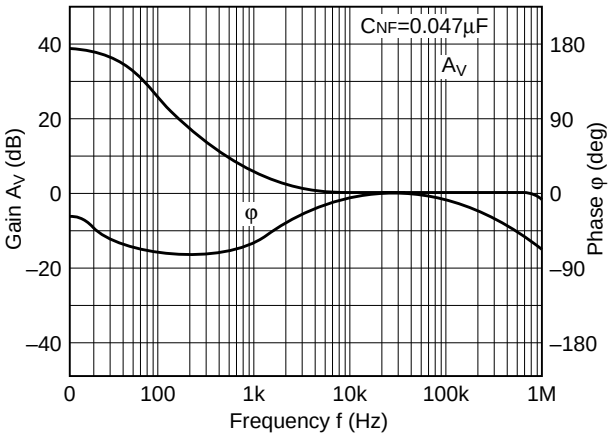


Figure 25 Frequency vs. Gain/Phase (Actual Data)

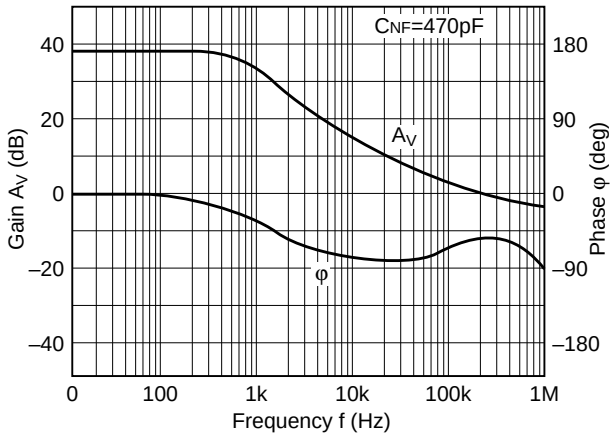


Figure 26 Frequency vs. Gain/Phase (Actual Data)

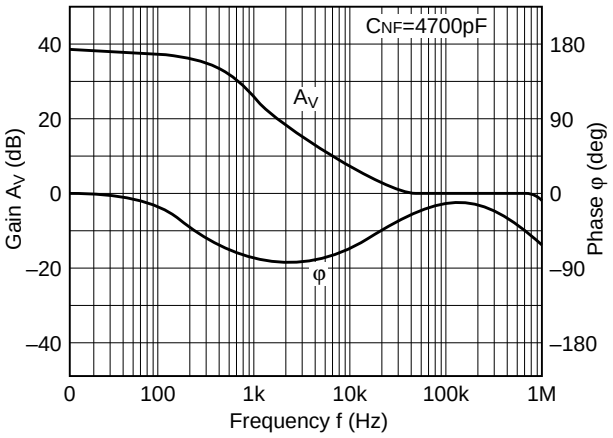
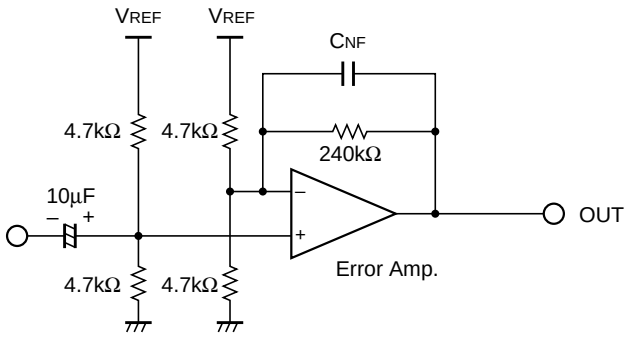


Figure 27 Actual Circuit



■ APPLICATION

1. Equivalent series resistance and stability of smoothing capacitor

The equivalent series resistance (ESR) of the smoothing capacitor in the DC/DC converter greatly affects the loop phase characteristic.
A smoothing capacitor with a high ESR improves system stability because the phase is advanced into the high-frequency range of an ideal capacitor (see Fig. 29 and 30). A smoothing capacitor with a low ESR reduces system stability. Use care when using low ESR electrolytic capacitors (OS capacitors) and tantalum capacitors.

Figure 28 DC/DC Converter Basic Circuit

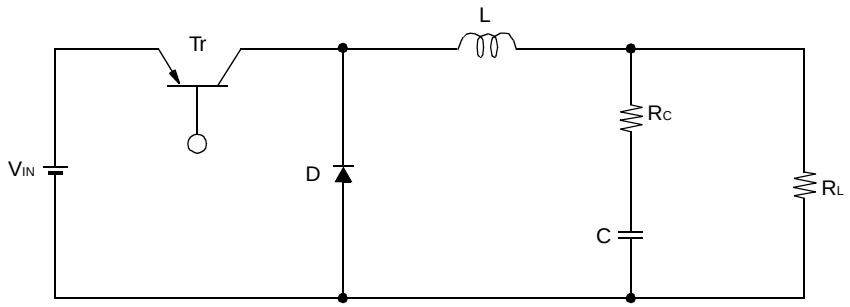


Figure 29 Gain vs. Frequency

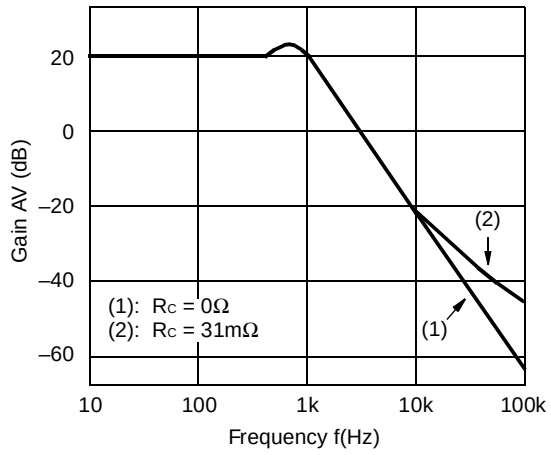
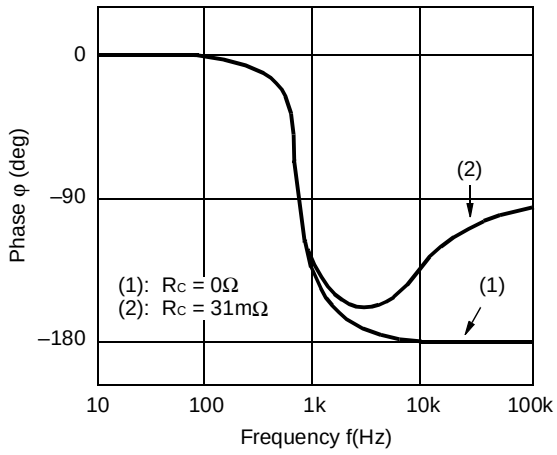


Figure 30 Phase vs. Frequency



Reference data

In an aluminum electrolytic smoothing capacitor ($R_C \cong 1.0\Omega$) is replaced with a low ESR electrolytic capacitor (OS capacitor: $R_C \cong 0.2\Omega$), the phase margin is reduced by half (see Fig. 32 and 33).

Figure 31 DC/DC Converter A_V vs. φ characteristic Test Circuit

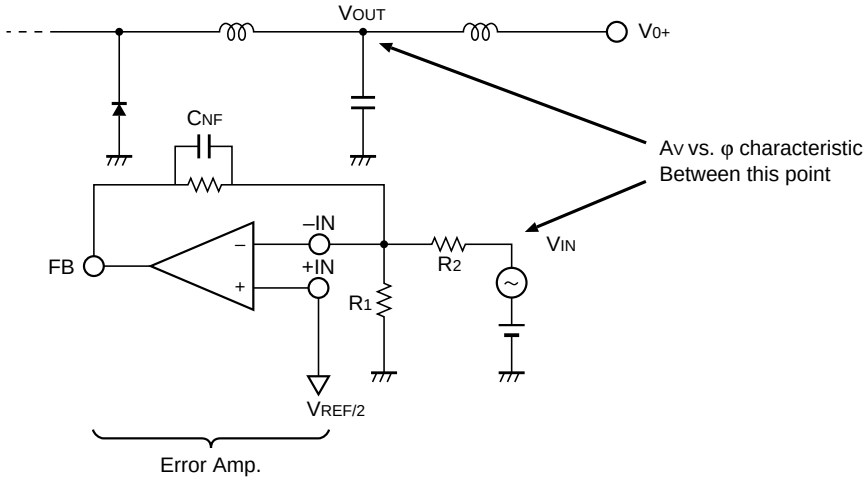


Figure 32 DC/DC Converter +5V output Gain vs. Phase

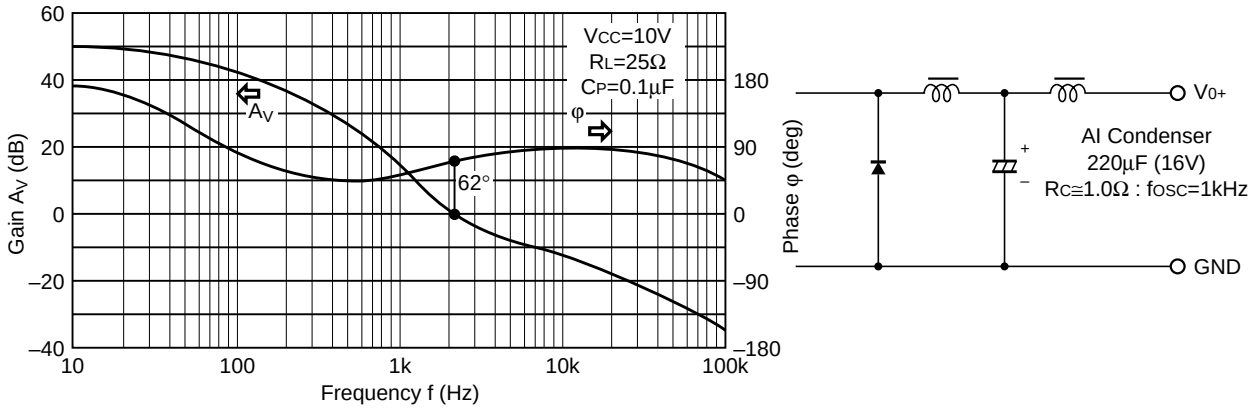
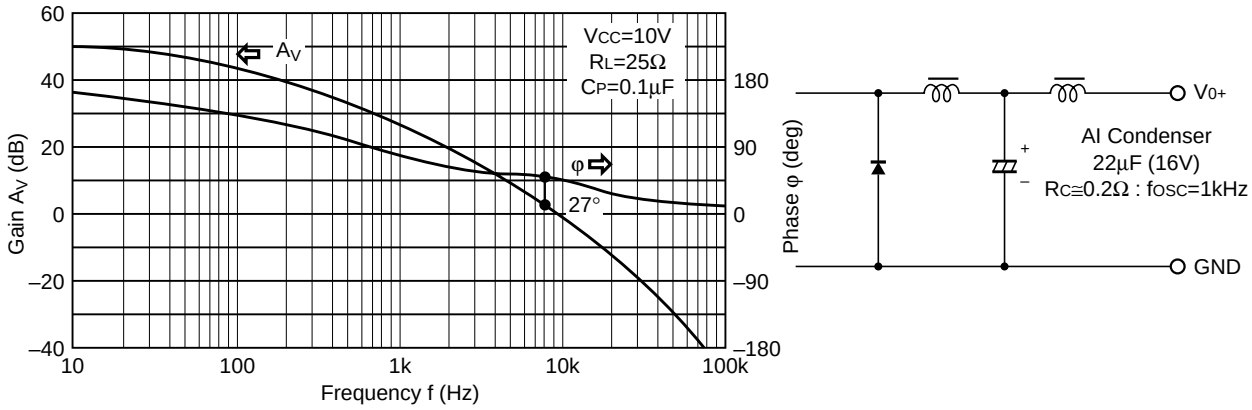
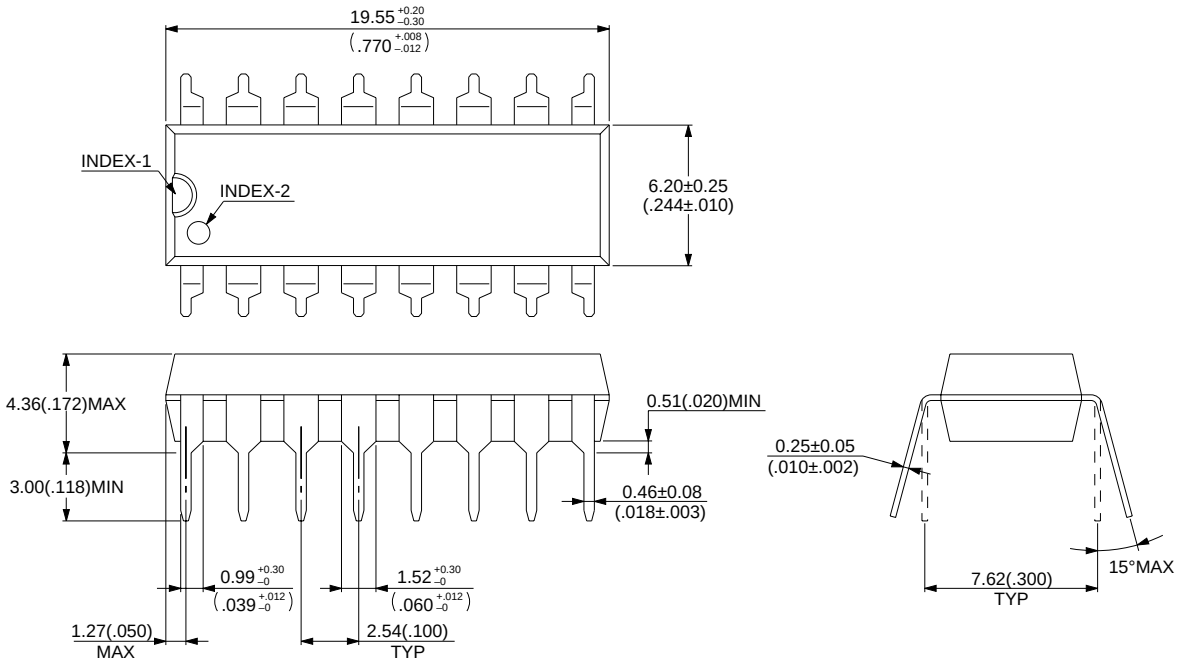


Figure 33 DC/DC Converter +5V output Gain vs. Phase



■ PACKAGE DIMENSIONS

16 pin, Plastic DIP
(DIP-16P-M04)



Dimensions in mm (inches)

(Continued)

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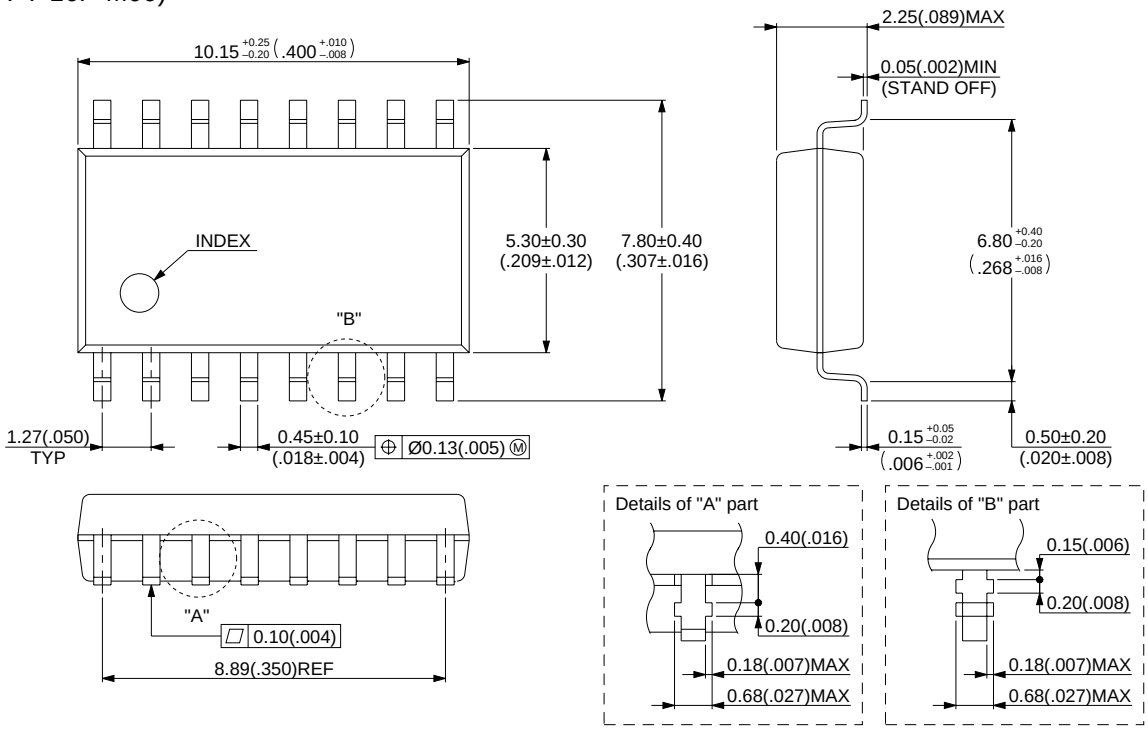
(Continued)

16 pin, Plastic FPT
(FPT-16P-M06)



Dimensions in mm (inches)

MB3778

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