FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-22415-1E

ASSP Communication Control

CMOS

SCSI-II Protocol Controller

(with single-ended driver/receiver)

MB86604L

■ DESCRIPTION

The Fujitsu MB86604L is a single-ended transmission type SCSI-II Protocol Controller (SPC) with a single-ended driver/receiver. The MB86604L facilitates interface control between small/medium host computer and peripheral devices (such as a hard disk and printer). The specifications conform to the SCSI-II Standard.

The MB86604L supports high-speed synchronous transfer, the MPU/DMA independent system data bus, and user programmable command set to enable configuration of high-performance systems.

It can also have the phase-to-phase sequence control function to reduce the program overhead of the host MPU.

The MB86604L incorporate with a single-ended type SCSI driver/receiver which can drive 48 mA of large-current, and so, the device can be directly connected with the SCSI bus.

The device can operate with +5 V single-power supply and in up to 40 MHz clock frequency. As for package, a 100-pin plastic small quad flat package is available.

■ FEATURES

SCSI Bus Interface:

- Conforming to the SCSI-II standard
- Operatable as Initiator and target

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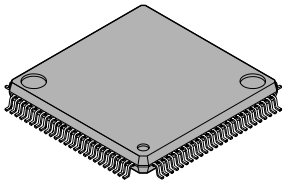
■ PACKAGE

100 pin, Plastic LQFP



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- Two types of high-speed data transfer:
  - Synchronous data transfer (Max. 10 Mbytes/s, max. 32 offsets, 32-step transfer rate)
  - Asynchronous data transfer (Max. 5 Mbyte/s)
- Transfer parameters (transfer mode, transfer rate, transfer offset) can be set for up to 7 connected devices.
- Single-ended transmission type (Maximum cable length: 6 m):
  - On-chip single-ended driver/receiver which can drive 48 mA of "L" level output current
  - Directly connectable with the SCSI bus
- On-chip three-state bidirectional I/O buffers for SCSI $\overline{REQ}$ and ACK pins ($\overline{DB7}$-$\overline{DB0}$, $\overline{DBP}$, $\overline{ATN}$, $\overline{MSG}$, $\overline{C/D}$, $\overline{I/O}$ pins can be selected from either three-state or open-drain buffer by controlling the TEST pins input.)

Transfer Operation:

- Automatic response to selection/reselection (Preset receiving operation can perform at the selection/reselection.):
  - Initiator: Automatically operates until message received without command issue.
  - Target: Automatically operates until command received without command issue.
- Automatic receiving:
  - Initiator: Automatically receives information for new phase to which target transited without command issue.
  - Target: Automatically receives message from initiator when initiator generates attention condition.
- On-chip 32-byte data register (FIFO) for data phase
- On-chip two (send-only and receive-only) 32-byte data buffers for message, command, and status phases
- On-chip 16-bit transfer block register and 24-bit transfer byte register enabling 1 Tbytes transfer (1 Tbytes: 16 Mbytes $\times$ 64 k blocks)
- On-chip independent data transfer bus enabling the MPU operation during the data transfer
- Parity through/generate can be specified.

System Bus Interface:

- 8-bit or 16-bit separate MPU and DMA buses
- Directly connectable with a 80 series or 68 series MPU
- Two types of transfer operation:
  - Program transfer
  - DMA transfer (Burst/Handshake)

Command Set:

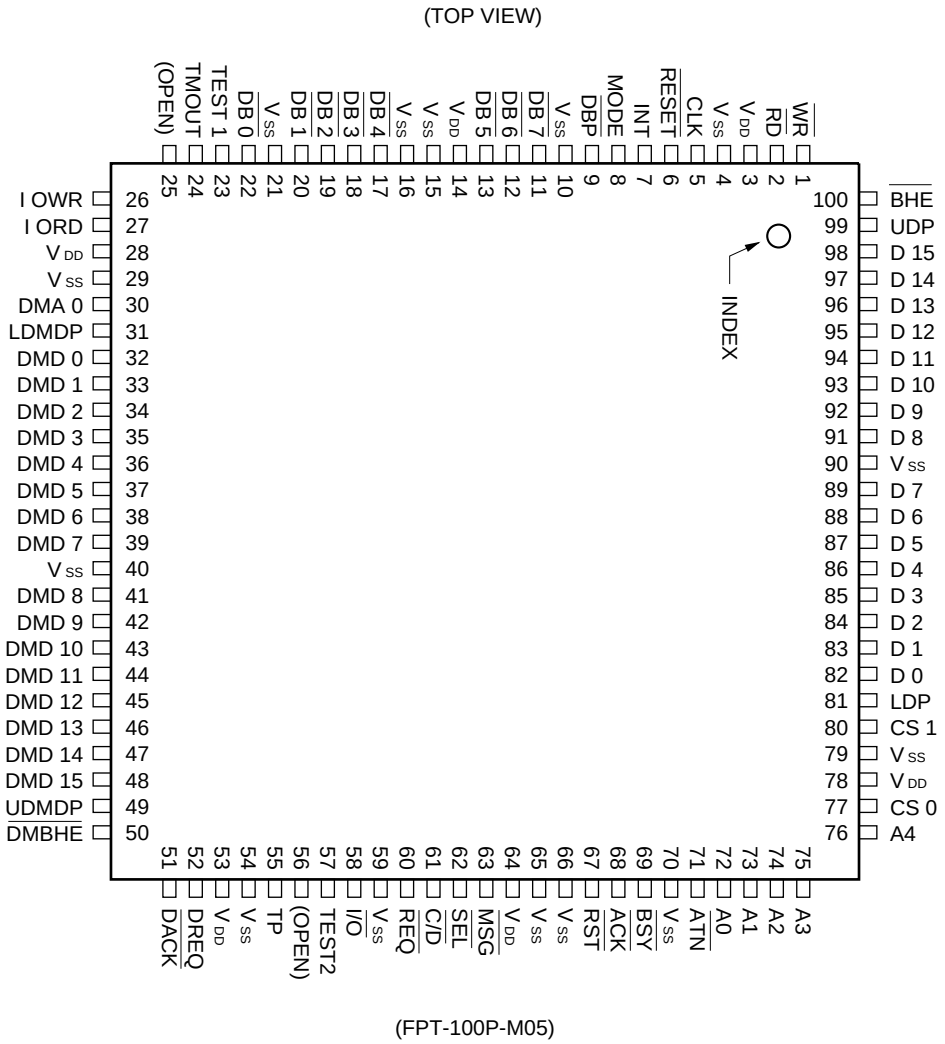
- Supports sequential commands and programmable commands in addition to ordinary commands
- Command queuing (Command can be continuously issued by putting tags to commands in command phase.)
- On-chip 256-byte memory for command programming memory and command queuing buffer

Others

- Process: CMOS process
- Supply Voltage: Single +5 V
- Input System Clock: 20 MHz/30 MHz/40 MHz
- Package: 100-pin plastic LQFP

MB86604L

■ PIN ASSIGNMENT



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■ PIN DESCRIPTION

1. SCSI Interface

Pin number	Symbol	Pin name	I/O	Function
60	$\overline{REQ}$	Request	I/O	Transfer request signal in the information transfer phases from target to initiator. The input signal to this pin is used for the timing control of data transfer sequence. This is a three-state I/O pin and an active low pin.
68	$\overline{ACK}$	Acknowledge	I/O	This pin is for the acknowledge signal from initiator to target for the REQ signal in the information transfer phases. The input signal to this pin is used for the timing control of data transfer sequence. This is a three-state I/O pin and an active low pin.
71	$\overline{ATN}$	Attention	I/O	This pin is for the attention signal that initiator requests target for the message transfer phase. This is an active-low pin.
63	$\overline{MSG}$*	Message	I/O	This pin is for the message signal that specifies type of information transferred on the data bus. This is an active-low pin and becomes “L” when message phase is specified.
61	$\overline{C/D}$*	Control/data	I/O	This pin is for the control/data signal that specifies type of information transferred on the data bus. This an active-low pin and becomes “L” level when command, status, or message phase is specified.
58	$\overline{I/O}$*	Input/output	I/O	This pin is for the input/output signal that specifies direction of information transferred on the data bus. This is an active-low pin. When this pin is “L” level, the information is transferred from target to initiator. When this pin is “H” level, the information is transferred from initiator to target.
69	$\overline{BSY}$	Busy	I/O	This pin is for the SCSI bus busy signal. In the arbitration phase, this is for the request signal for the use of bus acquisition. This is an active-low pin.
62	$\overline{SEL}$	Select	I/O	This pin is for the select signal used by initiator to select target during the selection phase and by target to reselect initiator during the reselection phase. This is an active-low pin.
67	$\overline{RST}$	Reset	I/O	This pin is for the reset signal used by any device on the bus. When the device is an input operation, the reset signal is input to this pin. When output operation, the reset signal is output from this pin. This is an active-low pin.
11, 12, 13, 17, 18, 19, 20, 22	$\overline{DB7}$ to $\overline{DB0}$	Data bus 7 to data bus 0	I/O	These pins are for the bidirectional 8-bit SCSI data bus and 1-bit odd parity line.
9	$\overline{DBP}$	Data bus parity		

* : Regarding the status of information transfer which is indicated by $\overline{MSG}$, $\overline{C/D}$, and $\overline{I/O}$ pins, See Table Phase Status.

Phase name	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	Transfer direction	
				Initiator	Target
Data-out phase	H	H	H	→	
Data-in phase	H	H	L	←	
Command phase	H	L	H	→	
Status phase	H	L	L	←	
Message-out phase	L	L	H	→	
Message-in phase	L	L	L	←	

Note: The SCSI interface input/output pins can be connected to a single-end type SCSI bus.

2. MPU Interface

Pin number	Symbol*	Pin name	I/O	Function
77	$\overline{CS0}$	Chip select 0	I	This is a chip select 0 pin used by MPU to select the SPC as an I/O device. This is an active-low pin.
80	$\overline{CS1}$	Chip select 1	I	This is a chip select 1 pin to select when MPU inputs/outputs the data on DMA bus through SPC. This is an active-low pin.
98, 97, 96, 95, 94, 93, 92, 91	D15 to D8	Data 15 to data 8	I/O	These pins are for the upper byte and parity bit of MPU data bus. When the $\overline{CS0}$ input is valid, these pins serve as I/O ports for the SPC internal registers. When the $\overline{CS1}$ input is valid, these pins serve as I/O ports for the DMA bus data.
99	UDP	Upper data parity		
89, 88, 87, 86, 85, 84, 83, 82	D7 to D0	Data 7 to data 0	I/O	These pins are for the lower byte and parity bit of the MPU data bus. When the $\overline{CS0}$ input is valid, these pins serve as I/O ports for the SPC internal registers. When the $\overline{CS1}$ input is valid, these pins serve as I/O ports for the DMA bus data.
81	LDP	Lower data parity		
76, 75, 74, 73, 72	A4 to A0	Address 4 to address 0	I	These are address input pins to select the SPC internal registers.
2	$\overline{RD}$ (R/$\overline{W}$)	Read (read/write)	I	In the 80-series mode, this is a read signal input pin ($\overline{IORD}$ or $\overline{RD}$) that MPU reads the SPC. This read signal pin is an active-low. In the 68-series mode, this pin functions as the control signal input (R/W) to control the read/write operation to the SPC. In the read operation, this pin is an active-high. In the write operation, this pin is an active-low.
1	$\overline{WR}$ ($\overline{LDS}$)	Write (lower data strobe)	I	In the 80-series mode, this pin is a write signal input pin ($\overline{IOWR}$ or $\overline{WR}$) that MPU writes to the SPC. This write signal input pin is active-low. In the 68-series mode, this pin function as the lower data strobe signal input ($\overline{LDS}$) that MPU outputs when the lower byte of data bus is valid. The $\overline{LDS}$ pin is an active-low.

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Pin number	Symbol*	Pin name	I/O	Function
100	$\overline{BHE}$ ($\overline{UDS}$)	Bus high enable (strobe)	I	In the 80-series mode, this pin is used for input of the bus high enable signal ($\overline{BHE}$) output from the MPU when the upper byte of the data bus is valid. The BHE pin is an active-low. In the 68-series mode, this pin functions as the upper data strobe signal input pin ($\overline{UDS}$) output from the MPU when the upper byte of the data bus is valid. The $\overline{UDS}$ pin is also an active-low.
7	INT ($\overline{INT}$)	Interrupt request	O	The INT and $\overline{INT}$ pins are the interrupt request signal output. The INT pins is used for the 80-series mode (an active-high pin), and the $\overline{INT}$ signal is used for the 68-series mode (an active-low pin).
8	MODE	Mode	I	This input pin is used to select the type of the MPU and DMA buses. In the 80-series mode, a high level is input. In the 68-series mode, a low level is input.

* : The pin symbols in parenthesis are the ones when the MODE input is “L”.

3. DMA Interface

Pin number	Symbol*	Pin name	I/O	Function
52	DREQ	DMA request	O	This is an output pin of DMA transfer request signal to the DMA controller. The data transfer between the SPC and memory via the DMA bus is requested. This pin is an active-high.
51	$\overline{DACK}$	DMA acknowledge	I	This is a DMA acknowledge signal input pin output from the DMA controller that enables the DMA transfer. This pin is an active-low. When this pin is an active state, the DMA cycle (read/write) is valid.
48, 47, 46, 45, 44, 43, 42, 41	DMD15 to DMD8	DMA data 15 to DMA data 8	I/O	These pins are the input/output pins of the upper byte and parity bit of the DMA data bus. When the signal input to the $\overline{CS1}$ pin (pin 80) is valid, these pins are connected directly to the MPU data bus.
49	UDMDP	Upper DMA data parity		
39, 38, 37, 36, 35, 34, 33, 32	DMD7 to DMD0	DMA data 7 to DMA data 0	I/O	These pins are the input/output pins of the lower byte and parity bit of the DMA data bus. When the $\overline{CS1}$ (pin 80) input is valid, these pins are connected directly to the MPU data bus.
31	LDMDP	Lower DMA data parity		
27	$\overline{IORD}$ (DMR/$\overline{W}$)	I/O read (DMA read/write)	I	In the 80-series mode, this pin ($\overline{IORD}$ or $\overline{RD}$) is used for the input pin to output the data from the SPC to the DMA bus. This is an active-low pin. In the 68-series mode, this pin functions as a control signal input pin (DMR/$\overline{W}$) to input/output the data to the SPC by the DMA controller. In the output operation, this pin is on the high-state (active-high state). In the input operation, this pin is on the low-state (active-low state).
26	$\overline{IOWR}$ ($\overline{DMLDS}$)	I/O write (DMA lower data strobe)	I	In the 80-series mode, this ($\overline{IOWR}$ or $\overline{WR}$) is used for the input pin to input the DMA bus data to the SPC. In the 68-series mode, this pin functions as a DMA lower data strobe input ($\overline{DMLDS}$) that DMA controller outputs when the lower byte of the DMA bus data is valid. Both $\overline{IOWR}$ and $\overline{DMLDS}$ pins are an active-low.

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Pin number	Symbol*	Pin name	I/O	Function
50	$\overline{\text{DMBHE}}$ ($\overline{\text{DMUDS}}$)	DMA bus high enable (DMA upper data strobe)	I	In the 80-series mode, this pin is for the DMA bus high enable signal input pin ($\overline{\text{DMBHE}}$) output from the DMA controller when the upper byte of the DMA data bus is valid. This is an active-low pin. In the 68-series mode, this pin functions as the DMA upper data strobe signal input pin ($\overline{\text{DMUDS}}$) output from the DMA controller when the upper byte of data bus is valid. The $\overline{\text{DMUDS}}$ pin is also an active-low.
30	DMA0	DMA address 0	I	In the 80-series mode, this pin is used for the DMA address 0 input pin output from the DMA controller. In the 68-series mode, a high level should be input to this pin.
55	TP	Transfer permission	I	This is a DMA transfer permission signal input pin. When this pin is in active-state, the SPC does the DMA transfer. In case that this pin becomes inactive during the DMA transfer, the DMA transfer is paused on the block boundary. This pin is an active high.

* : The pin symbols in parenthesis are the ones when the MODE input is “L”.

4. Others

Pin number	Symbol*	Pin name	I/O	Function
6	$\overline{\text{RESET}}$	Reset	I	System reset input pin. The input reset active pulse width must have 4 times of the clock cycle at least. This is an active-low pin.
5	CLK	Clock	I	Clock signal input pin. 20 MHz, 30 MHz, or 40 MHz can be applied as the input clock frequency.
3, 14, 28 53, 64, 78	V_{DD}	Power supply	—	+5 V power supply pins.
4, 10, 15 16, 21, 29 40, 54, 59 65, 66, 70 79, 90	V_{SS}	Ground	—	Ground pins.
23	TEST1	TEST	I	This pin is used to select the type of I/O buffer on SCSI data bus pins. In case that $\overline{\text{DBP}}$, $\overline{\text{DB7}}$ – $\overline{\text{DB0}}$ pins are used as an open-drain I/O, connect this pin to V_{SS}. In case of three-state I/O, connect to V_{DD}.
57	TEST2	TEST	I	This pin is used to select the type of I/O buffer on SCSI pins. In case that $\overline{\text{MSG}}$, $\overline{\text{C/D}}$, $\overline{\text{I/O}}$, and $\overline{\text{ATN}}$ pins are used as an open-drain I/O, connect this pin to V_{SS}. In case of three-state I/O, connect to V_{DD}.
24	TMOUT	TIMEOUT	O	This is a SCSI Timeout pin that indicates the SPC has been busy longer than the specified time. A high level is output on this pin if the SPC busy time exceeds the specified time. This pin can be used for the timeout counter.
25, 26	(OPEN)	(Open)	—	These are open pins. Those pins are not connected with the device internally. Those pins must be left open.

* : The pin symbols in parenthesis are the symbols when the MODE input is “L”.

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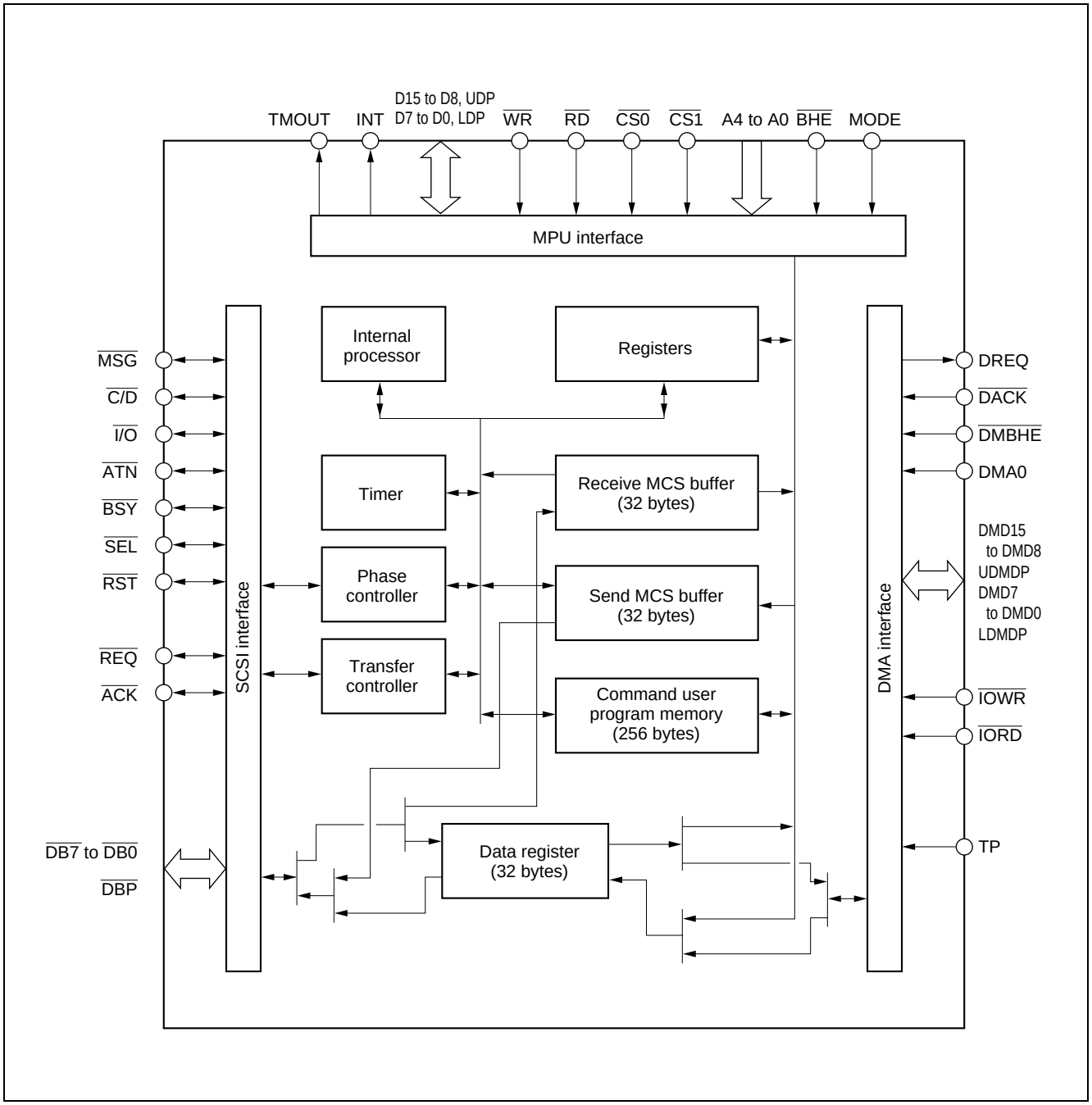
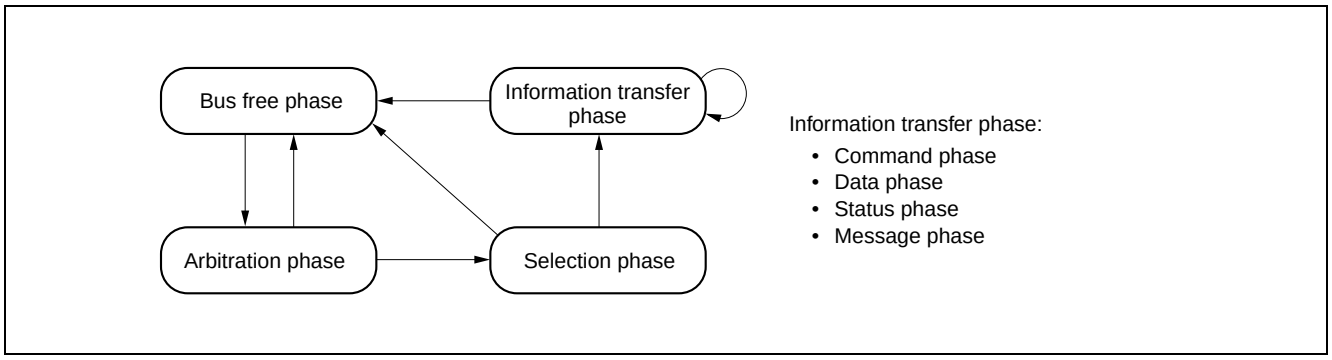
■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

1. International Processor (Sequencer)

Performs sequence control between the SCSI bus phases.



2. Timer

Manages the SCSI time standards.

Also, conducts the following time managements.

- Time until the $\overline{REQ}$ or $\overline{ACK}$ signal is asserted for asychronous transfer data
- Time until selection or reselection is retried
- $\overline{REQ}$ and $\overline{ACK}$ timeout time during transfers:
  Asychronous transfer case
  Target: After the $\overline{REQ}$ is asserted, the time until the initiator asserts the $\overline{ACK}$
  Initiator: After the $\overline{ACK}$ is asserted, the time until the target negates the $\overline{REQ}$
  Synchronous transfer case
  Target: After the $\overline{REQ}$ is sent, the time until an $\overline{ACK}$ signal which makes the offset 0 is received from the initiator
- SPC Timeout
  Manages the SPC timeout indicating the SPC busy time longer than the specified time.

3. Phase Controller

Controls the various phases executed by SCSI such as arbitration, selection/reselection, data in/out, command, status, and message in/out.

4. Transfer Controller

Controls the information (data, command, status, message) transfer phases executed by SCSI.

The following two types of transfer phases are used.

Asychronous transfer: Controls interlock (response confirmation format) between the $\overline{REQ}$ and $\overline{ACK}$ signals.
Synchronous transfer: Controls a maximum 32-byte offset value for the data in or data out phase.

The following two modes exist for the data phase.

Program transfer: Uses data register (address 00/01) via the MPU interface
DMA transfer: Uses DREQ and $\overline{DACK}$ signals via the DMA interface.

The transfer parameter setting values for synchronous transfer (Transfer mode, transfer rate, transfer offset) can be strobe for individual ID device and are automatically established when the data phase is initiated.

The number of transfer bytes is defined as block length $\times$ number of blocks.

5. Register

The main registers are listed.

- Command register
  Command is specified by an 8-bit code.
  Specifies the program head address assigned to the user program memory for user program applications.
- Chip status register
  Shows the chip's operating state, nexus counterpart ID, and data register state.
- SCSI bus status register
  Shows the SCSI control signal state.
- Interrupt status register
  Shows 8-bit code.
- Command step register
  Shows 8-bit code indicating the command execution state.
  Error analysis can be performed by referring to the information in this register and the interrupt status register.
- Group 6/7 command length setting register
  Sets the group 6/7 command length which is undefined by the SCSI standard.
  By setting the command length in this register, the SPC can determine the command length.

6. Receive-MCS Buffer

A receive only, 32-byte data buffer which stores information received via SCSI (message, command, status)

M: Message, C: Command, S: Status

7. Send-MCS Buffer

A send only, 32-byte data buffer which stores information sent via SCSI (message, command, status)

8. Command User Program Memory

Program memory used for establishing programmable commands (256 bytes).

9. Data Register

FIFO-type data register which stores data in SCSI data phase (32 bytes).

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage*	V_{DD}	V_{SS} – 0.5	6.0	V
Input voltage*	V_I	V_{SS} – 0.5	V_{DD} + 0.5	V
Output voltage*	V_O	V_{SS} – 0.5	V_{DD} + 0.5	V
Operating ambient temperature	Top	–25	+85	°C
Storage temperature	Tstg	–40	+125	°C

* : V_{SS} = 0 V

WARNING: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter			Symbol	Value			Unit
				Min.	Typ.	Max.	
Power supply voltage *1			V_{DD}	4.75	5.0	5.25	V
"H" level input voltage *1	CLK		V_{IH}	3.5	—	—	V
	Except SCSI and CLK pins			2.2	—	—	V
	SCSI pins			2.0	—	—	V
"L" level input voltage *1	CLK		V_{IL}	—	—	1.5	V
	Except CLK pin			—	—	0.8	V
"H" level output current *2	Except SCSI pins		I_{OH}	—	—	–2.0	mA
	SCSI pins	Three-state		—	—	–8.0	mA
		Open-drain		—	—	—	mA
"L" level output current *2	Except SCSI pins		I_{OL}	—	—	+3.2	mA
	SCSI pins			—	—	+48	mA
Operating ambient temperature			Ta	0	—	+70	°C

*1: V_{SS} = 0 V

*2: SCSI pins are $\overline{DB7}$ to $\overline{DB0}$, $\overline{DBP}$, $\overline{BSY}$, $\overline{SEL}$, $\overline{RST}$, $\overline{ATN}$, $\overline{REQ}$, $\overline{ACK}$, $\overline{MSG}$, $\overline{C/D}$, $\overline{I/O}$

Note: The recommended operating conditions are the values recommended to ensure correct logic operation of the LSI. The standard values of the electrical characteristics (DC and AC characteristics) are guaranteed within the range of the recommended operating conditions.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{DD} = +5 V±5%, V_{SS} = 0 V, Ta = 0°C to +70°C)

Parameter			Symbol	Condition		Value Min.	Value Max.	Unit
"H" level input voltage	CLK		V_{IH}	—		3.5	—	V
	Except SCSI and CLK pins					2.2	—	V
	SCSI pins					2.0	—	V
"L" level input voltage	CLK		V_{IL}	—		—	1.5	V
	Except CLK pin					—	0.8	V
Input hysteresis of SCSI pins *1			V_{HW}	—		0.3	—	V
"H" level output voltage *1	Except SCSI pins		V_{OH}	I_{OH} = –2.0 mA		4.2	V_{DD}	V
	SCSI pins	Three-state		I_{OH} = –8.0 mA		2.0	—	V
		Open-drain		—		—	—	V
"L" level output voltage *1	Except SCSI pins		V_{OL}	I_{OL} = +3.2 mA		V_{SS}	0.4	V
	SCSI pins			I_{OL} = +48.0 mA		—	0.5	V
Input leakage current			I_{LI}	$V_{SS} \le V_I \le V_{DD}$		–10	+10	µA
Input/output leakage current			I_{LOZ}	$V_{SS} \le V_I \le V_{DD}$, See Note below		–10	+10	µA
Power supply current			I_{DD}	All output pins opened	CLK input = 20 MHz SPC operating clock = 10 MHz	—	45	mA
					CLK input = 30 MHz SPC operating clock = 10 MHz		48	mA
					CLK input = 40 MHz SPC operating clock = 13.3 MHz		55	mA
					CLK input = 30 MHz SPC operating clock = 15 MHz		65	mA
					CLK input = 20 MHz SPC operating clock = 20 MHz		60	mA
					CLK input = 40 MHz SPC operating clock = 20 MHz		70	mA

*1: SCSI pins are $\overline{DB7}$ to $\overline{DB0}$, $\overline{DBP}$, $\overline{BSY}$, $\overline{SEL}$, $\overline{RST}$, $\overline{ATN}$, $\overline{REQ}$, $\overline{ACK}$, $\overline{MSG}$, $\overline{C/D}$, $\overline{I/O}$

Note: Leakage current in the above spec indicates the following currents.
(1) Leakage current at the high-Z state on the three-state output pins.
(2) Leakage current at the output high-Z state (input state) on the bidirectional bus pins.

2. I/O Pin Capacitance

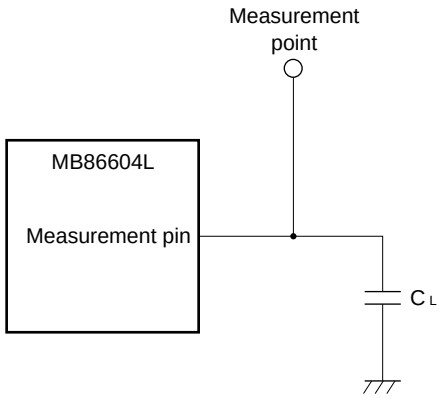
(V_{DD} = V_I = 0 V, f = 1 MHz, Ta = +25°C)

Parameter		Symbol	Value		Unit
			Min.	Max.	
Input pin capacitance		C_{IN}	—	6	pF
Output pin capacitance		C_{OUT}	—	6	pF
I/O pin capacitance	Except SCSI pins	$C_{I/O}$	—	6	pF
	SCSI pins		—	25	pF

3. Load Conditions for AC Characteristics

(V_{DD} = +5 V±5%, V_{SS} = 0 V, Ta = 0°C to +70°C)

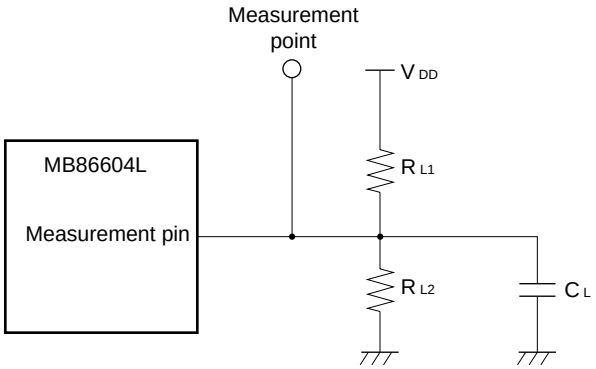
Non-SCSI pins



Pin Symbol	C_L
INT, DREQ	60 pF
D15 to D8, UDP, D7 to D0, LDP DMD15 to DMD8, UDMDP DMD7 to DMD0, LDMDP	85 pF

C_L: Load capacitance

SCSI pins



Load resistance	R_{L1} = 110 Ω
	R_{L2} = 165 Ω
Load capacitance	R_L = 200 pF

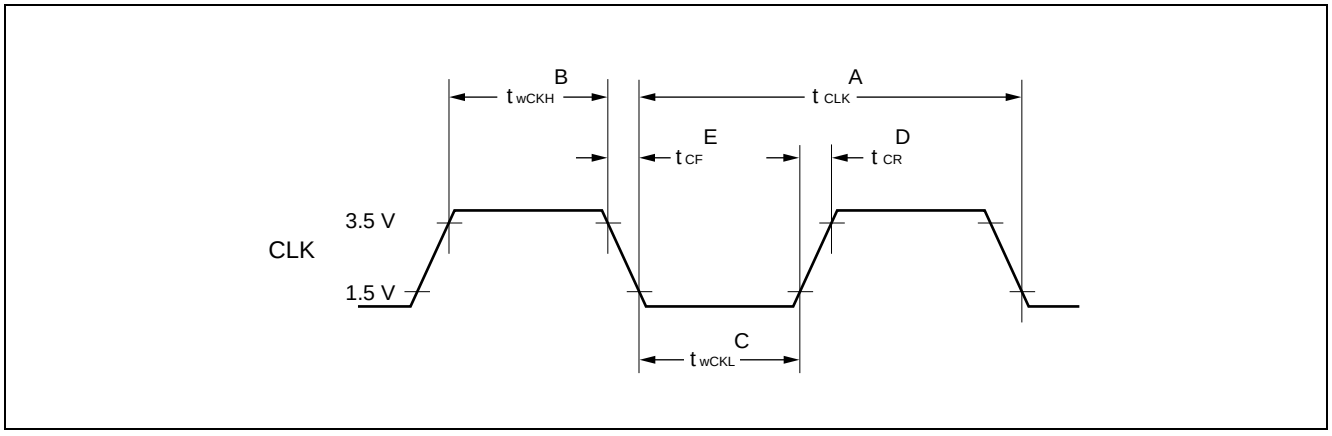
4. AC Characteristics

(1) System clock

Parameter	Symbol		Value		Unit
		Position*	Min.	Max.	
Clock cycle time (CLK)	t_{CLK}	A	25.0	50.0	ns
Clock “H” pulse width	t_{WCKH}	B	10.0	—	ns
Clock “L” pulse width	t_{WCKL}	C	10.0	—	ns
Clock rise time	t_{CR}	D	—	10.0	ns
Clock fall time	t_{CF}	E	—	10.0	ns

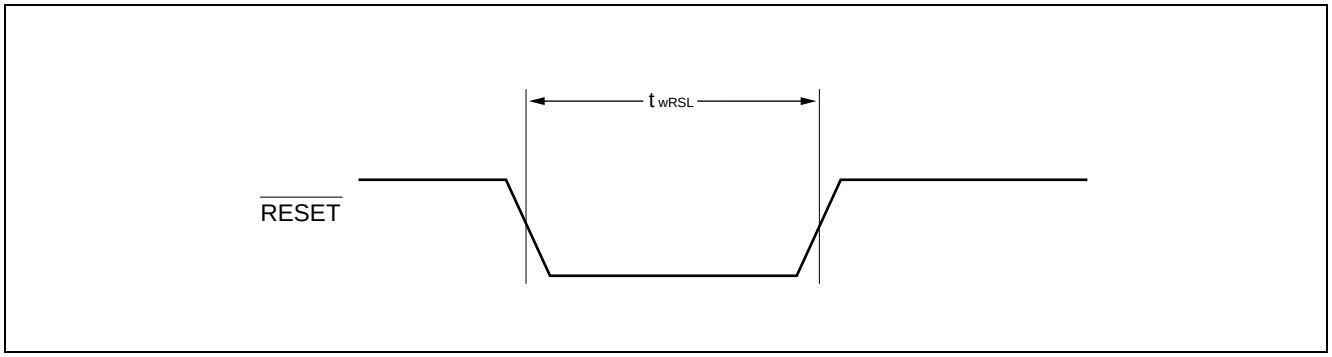
* : The position number indicates the position in the waveform.

Note: In case that the internal clock frequency and the input clock frequency are the same (i.e. when using the divided-by-one mode), the clock pulse width (for “H” and “L”) must have at least 20 ns or longer.



(2) System reset

Parameter	Symbol	Value		Unit
		Min.	Max.	
$\overline{\text{RESET}}$ “L” level pulse width	t_{WRSL}	4 t_{CLK}	—	ns

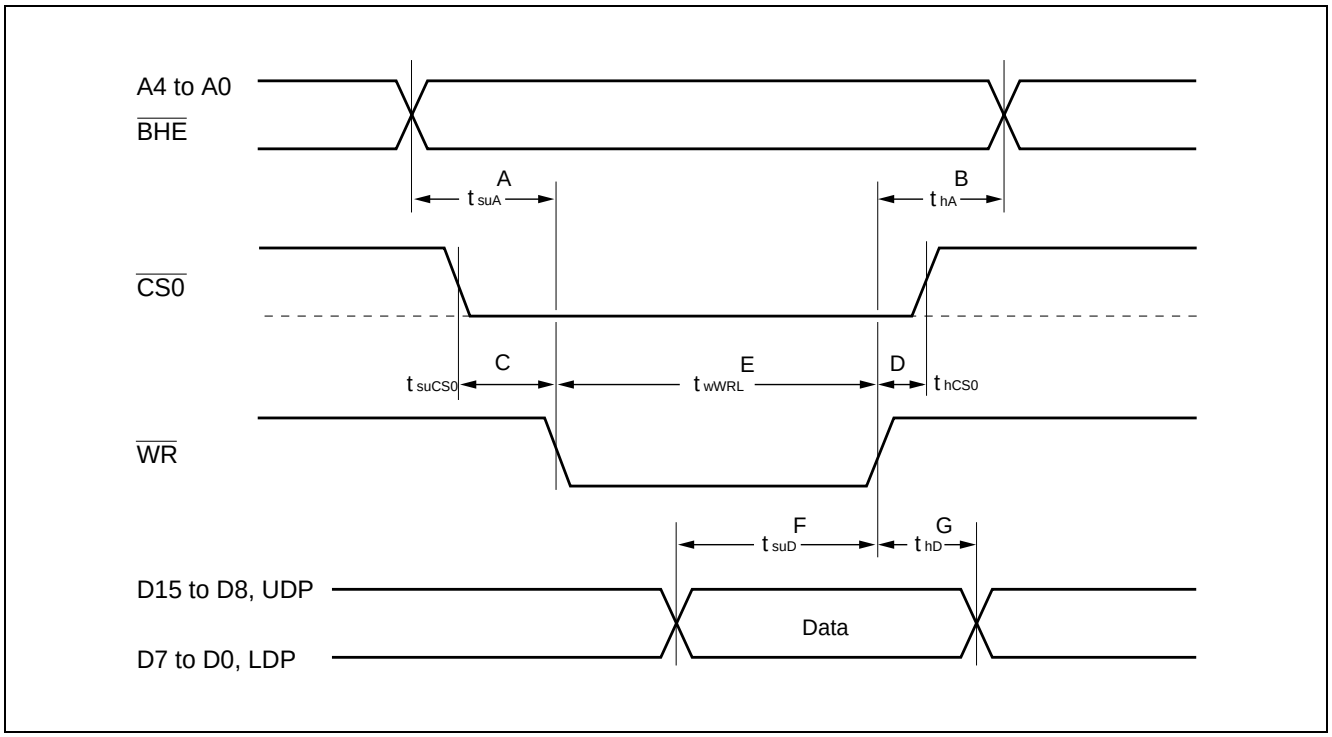


(3) MPU interface (80 series)

- **Register write timing**

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
Address (A4 to A0), $\overline{BHE}$ set up time	$\overline{WR}$ "L"	t_{suA}	A	40	—	ns
Address (A4 to A0), hold time	$\overline{WR}$ "H"	t_{hA}	B	20	—	ns
$\overline{CS0}$ set up time	$\overline{WR}$ "L"	t_{suCS0}	C	20	—	ns
$\overline{CS0}$ hold time	$\overline{WR}$ "H"	t_{hCS0}	D	10	—	ns
$\overline{WR}$ "L" level pulse width	—	t_{wWRL}	E	70	—	ns
Data set up time	$\overline{WR}$ "H"	t_{suD}	F	40	—	ns
Data hold time	$\overline{WR}$ "H"	t_{hD}	G	10	—	ns

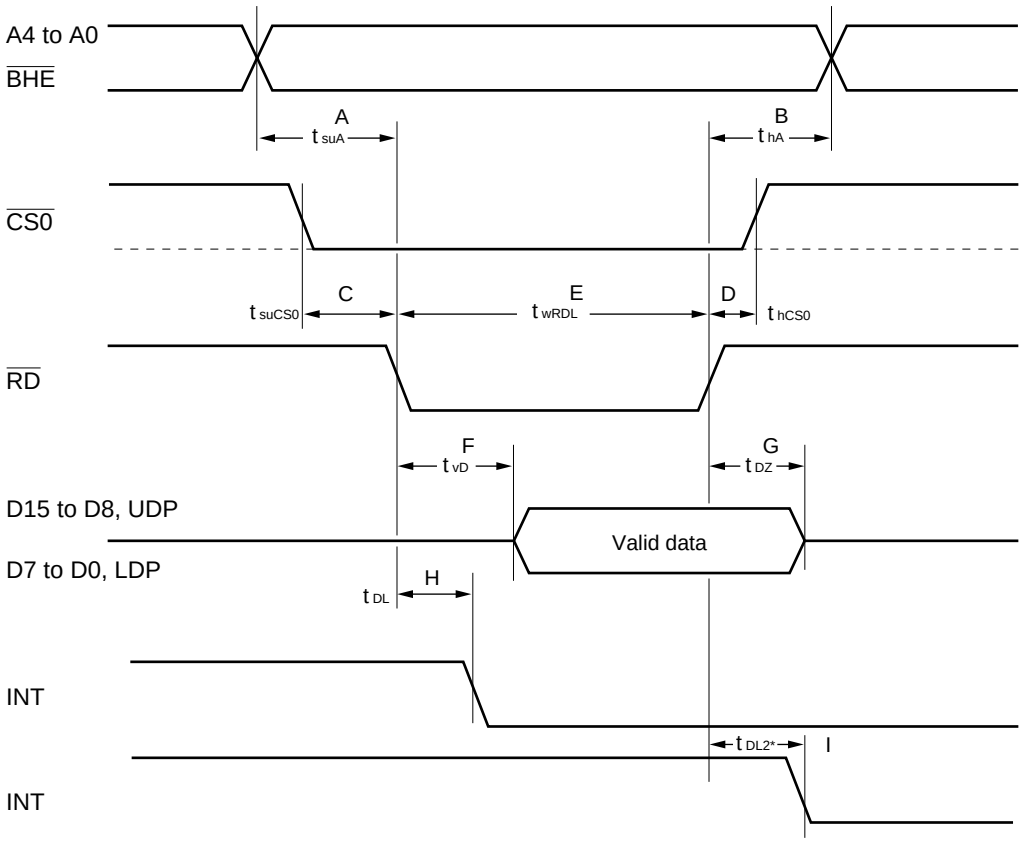
* : The position number indicates the position in the waveform.



- **Register read timing**

Parameter		Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
Address (A4 to A0), $\overline{BHE}$ set up time		$\overline{RD}$ "L"	t_{suA}	A	40	—	ns
Address (A4 to A0), Hold time		$\overline{RD}$ "H"	t_{hA}	B	20	—	ns
$\overline{CS0}$ set up time		$\overline{RD}$ "L"	t_{suCS0}	C	20	—	ns
$\overline{CS0}$ hold time		$\overline{RD}$ "H"	t_{hCS0}	D	10	—	ns
$\overline{RD}$ "L" level pulse width		—	t_{wRDL}	E	70	—	ns
Data output defined time		$\overline{RD}$ "L"	t_{vD}	F	—	70	ns
Data output disable time		$\overline{RD}$ "H"	t_{DZ}	G	10	—	ns
INT signal clear time	for INT non-hold mode	$\overline{RD}$ "L"	t_{DL}	H	—	50	ns
	for INT hold mode	$\overline{RD}$ "H"	t_{DL2}	I	—	n t_{CLK} + 50	ns

* : The position number indicates the position in the waveform.

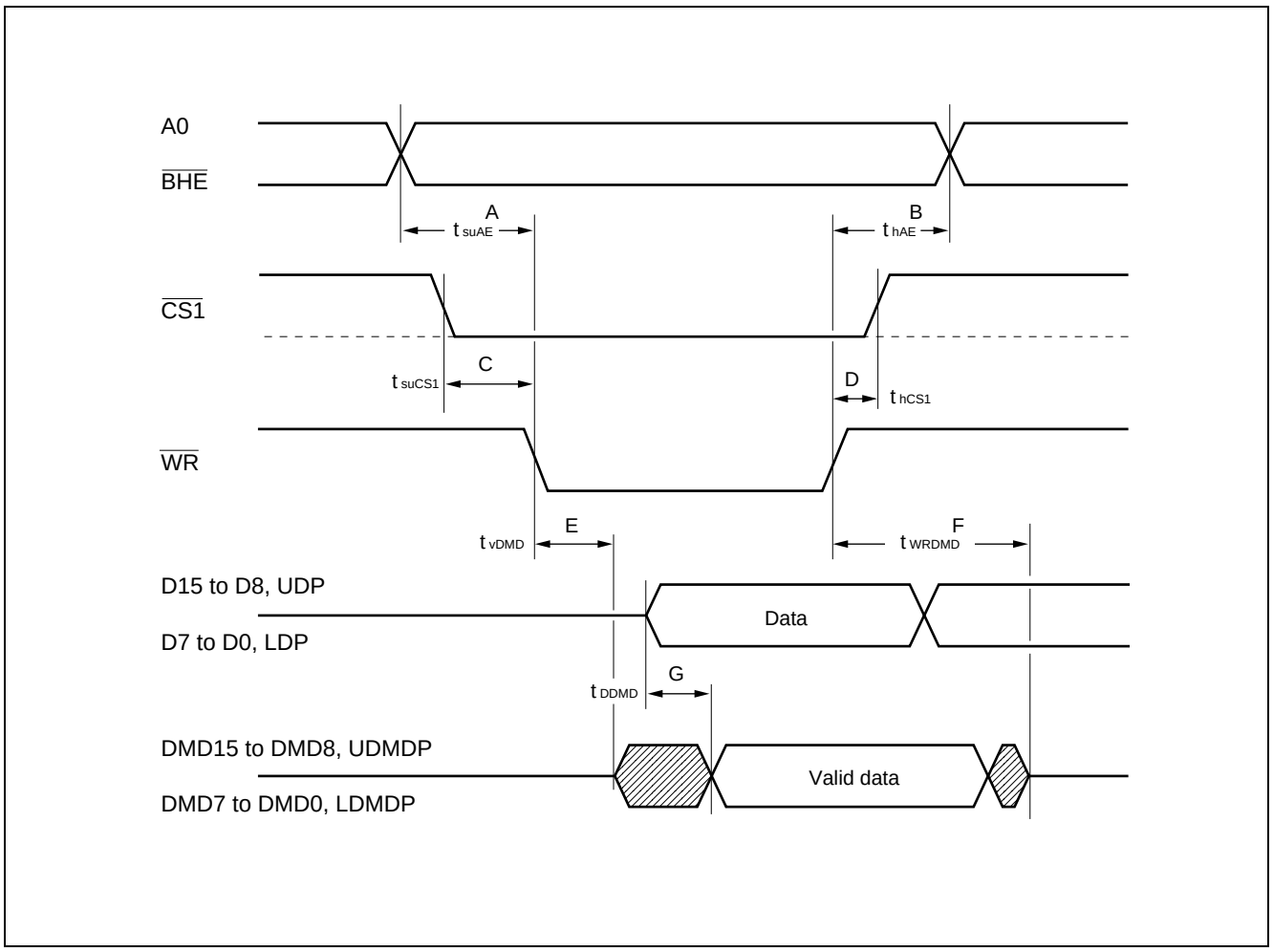


*: t_{DL2} is determined by a rising edge of the strobe signal which reads the step code for the last interrupt source. Also, "n" indicates the division ratio.

- **Register write timing (for external access)**

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
Address (A0), $\overline{BHE}$ set up time	$\overline{WR}$ "L"	t_{suAE}	A	40	—	ns
Address (A0), $\overline{BHE}$ hold time	$\overline{WR}$ "H"	t_{hAE}	B	20	—	ns
$\overline{CS1}$ set up time	$\overline{WR}$ "L"	t_{suCS1}	C	20	—	ns
$\overline{CS1}$ hold time	$\overline{WR}$ "H"	t_{hCS1}	D	10	—	ns
DMA data bus output delay time	$\overline{WR}$ "L"	t_{vDMD}	E	—	70	ns
DMA data bus output undefined time	$\overline{WR}$ "H"	t_{WRDMD}	F	10	—	ns
MPU data → DMA data bus output delay time	—	t_{DDMD}	G	—	40	ns

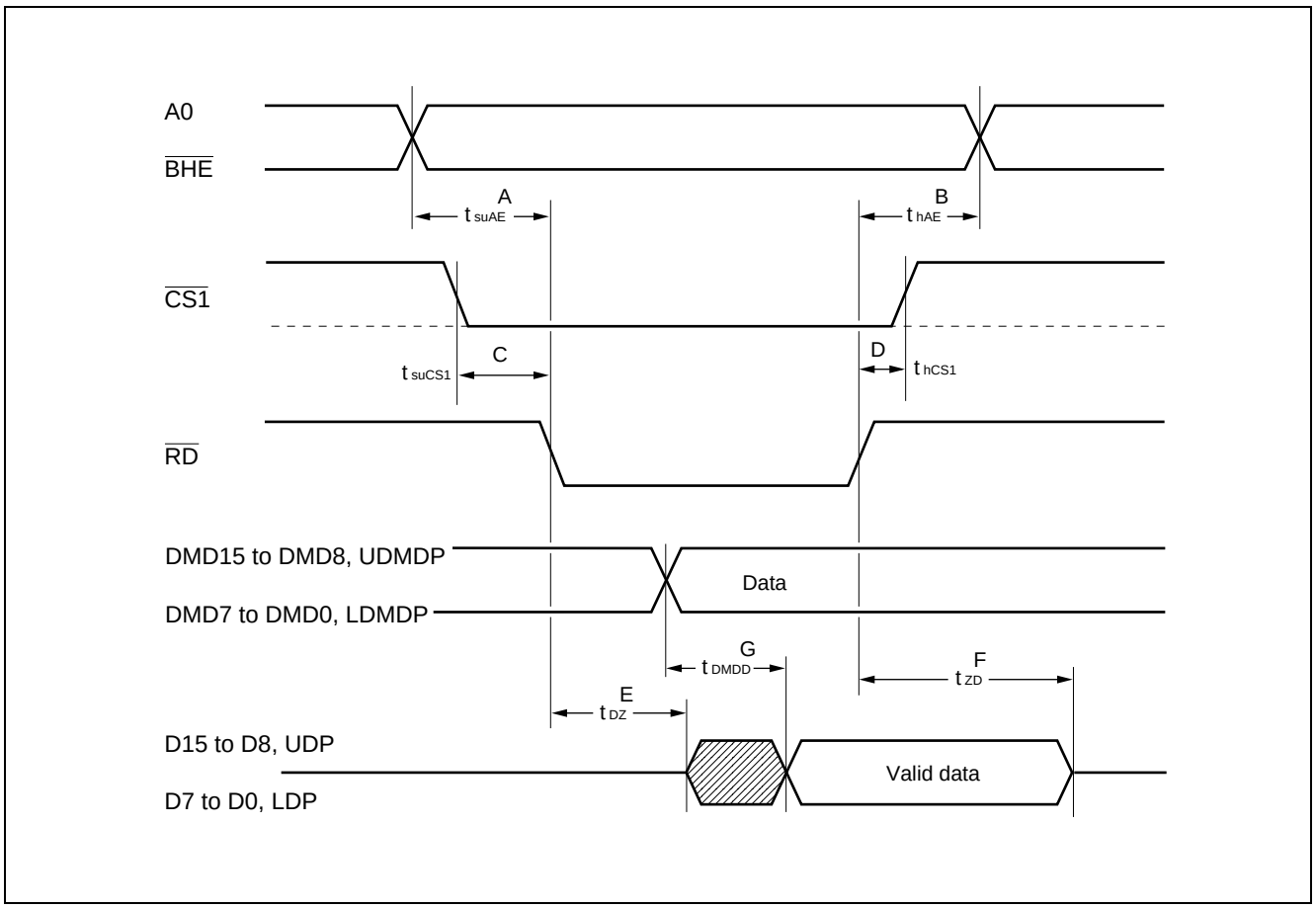
* : The position number indicates the position in the waveform.



- **Register read timing (for external access)**

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
Address (A0), $\overline{BHE}$ set up time	$\overline{RD}$ "L"	t_{suAE}	A	40	—	ns
Address (A0), $\overline{BHE}$ hold time	$\overline{RD}$ "H"	t_{hAE}	B	20	—	ns
$\overline{CS1}$ set up time	$\overline{RD}$ "L"	t_{suCS1}	C	20	—	ns
$\overline{CS1}$ hold time	$\overline{RD}$ "H"	t_{hCS1}	D	10	—	ns
MPU data bus output enable time	$\overline{RD}$ "L"	t_{ZD}	E	—	70	ns
MPU data bus output disable time	$\overline{RD}$ "H"	t_{DZ}	F	10	—	ns
DMA data → MPU data bus output delay time	—	t_{DMDD}	G	—	40	ns

* : The position number indicates the position in the waveform.

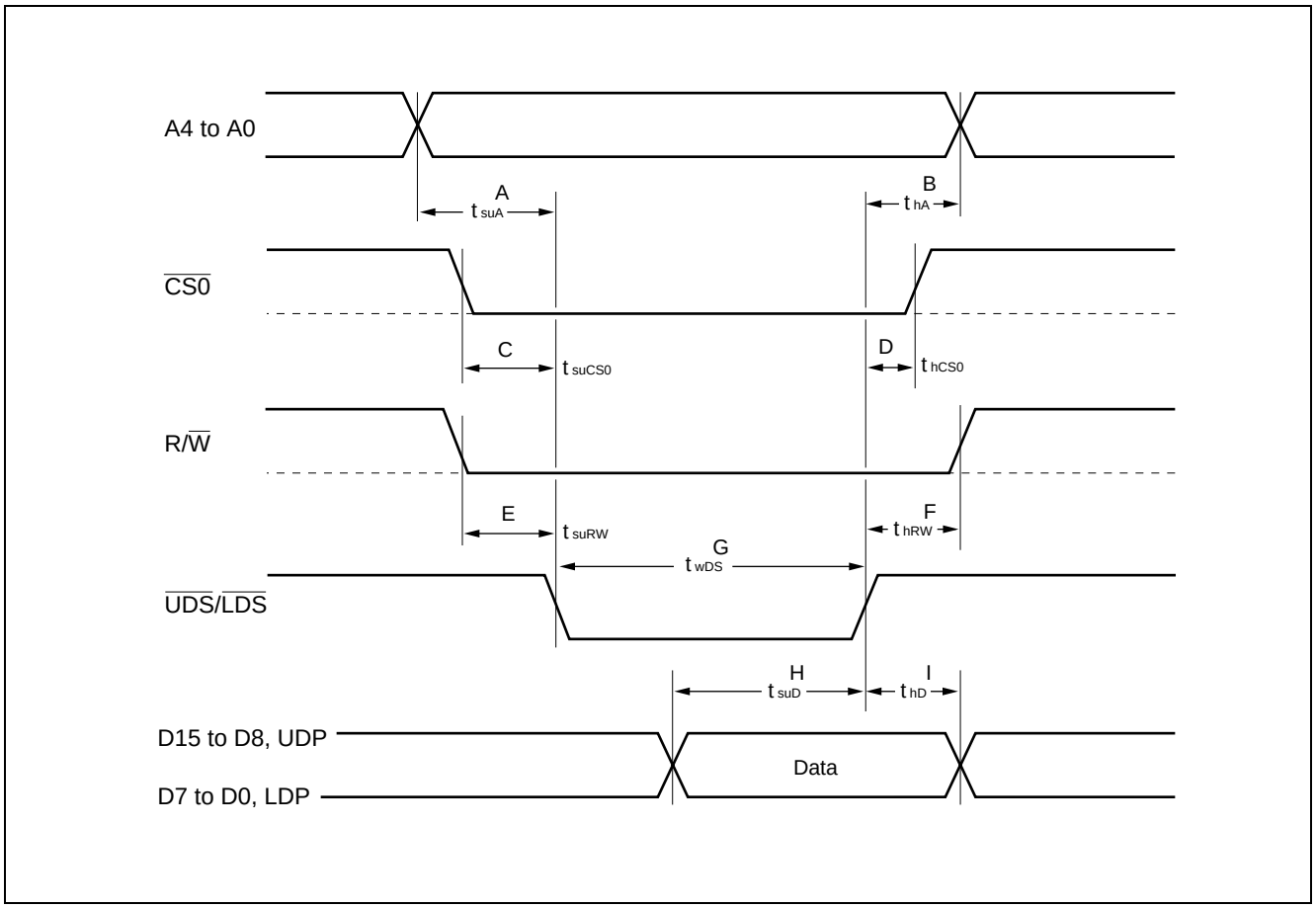


(4) MPU interface (68 series)

- **Register write timing**

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
Address (A4 to A0) set up time	$\overline{UDS}/\overline{LDS}$ "L"	t_{suA}	A	40	—	ns
Address (A4 to A0) hold time	$\overline{UDS}/\overline{LDS}$ "H"	t_{hA}	B	20	—	ns
$\overline{CS0}$ set up time	$\overline{UDS}/\overline{LDS}$ "L"	t_{suCS0}	C	20	—	ns
$\overline{CS0}$ hold time	$\overline{UDS}/\overline{LDS}$ "H"	t_{hCS0}	D	10	—	ns
R/$\overline{W}$ set up time	$\overline{UDS}/\overline{LDS}$ "L"	t_{suRW}	E	20	—	ns
R/$\overline{W}$ hold time	$\overline{UDS}/\overline{LDS}$ "H"	t_{hRW}	F	20	—	ns
$\overline{UDS}/\overline{LDS}$ "L" level pulse width	—	t_{wDS}	G	70	—	ns
Data set up time	$\overline{UDS}/\overline{LDS}$ "H"	t_{suD}	H	40	—	ns
Data hold time	$\overline{UDS}/\overline{LDS}$ "H"	t_{hD}	I	10	—	ns

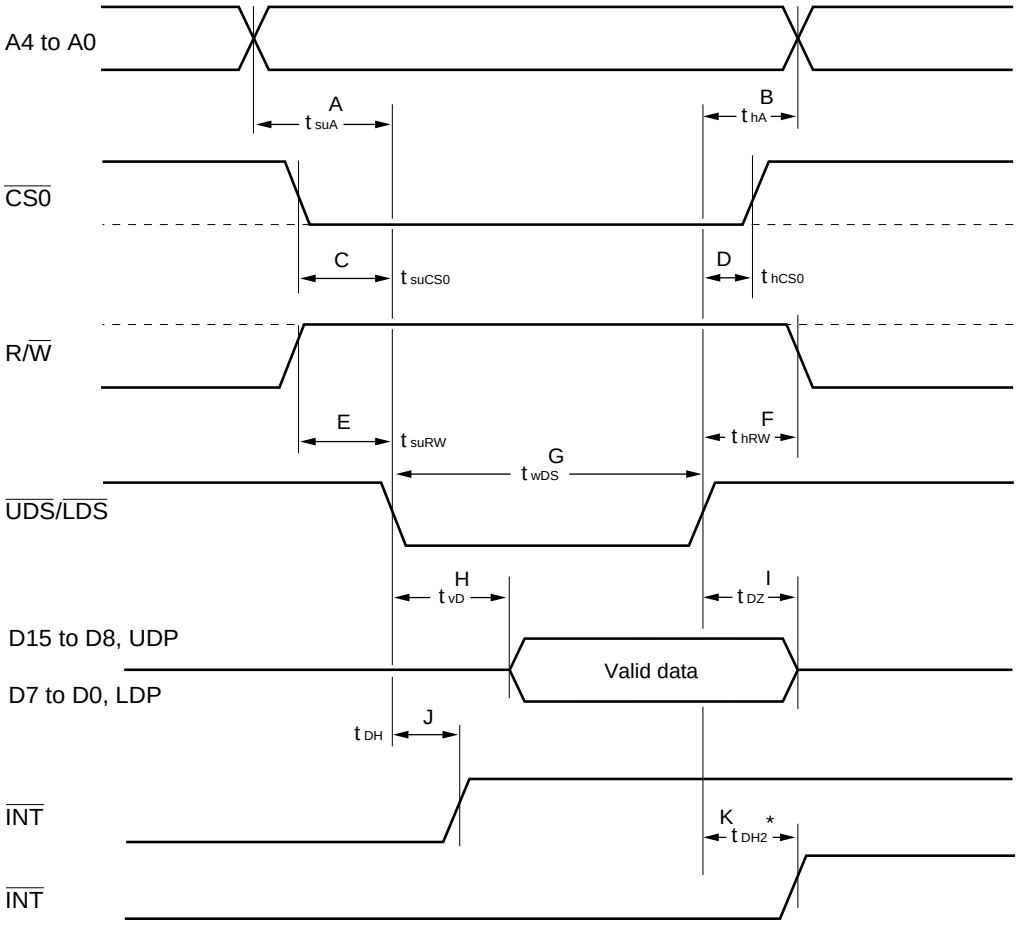
* : The position number indicates the position in the waveform.



- **Register read timing**

Parameter		Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
Address (A4 to A0) set up time		$\overline{UDS}/\overline{LDS}$ "L"	t_{suA}	A	40	—	ns
Address (A4 to A0) hold time		$\overline{UDS}/\overline{LDS}$ "H"	t_{hA}	B	20	—	ns
$\overline{CS0}$ set up time		$\overline{UDS}/\overline{LDS}$ "L"	t_{suCS0}	C	20	—	ns
$\overline{CS0}$ hold time		$\overline{UDS}/\overline{LDS}$ "H"	t_{hCS0}	D	10	—	ns
R/$\overline{W}$ set up time		$\overline{UDS}/\overline{LDS}$ "L"	t_{suRW}	E	20	—	ns
R/$\overline{W}$ hold time		$\overline{UDS}/\overline{LDS}$ "H"	t_{hRW}	F	20	—	ns
$\overline{UDS}/\overline{LDS}$ "L" level pulse time		—	t_{wDS}	G	70	—	ns
Data output confirmation time		$\overline{UDS}/\overline{LDS}$ "L"	t_{vD}	H	—	70	ns
Data output disable time		$\overline{UDS}/\overline{LDS}$ "H"	t_{DZ}	I	10	—	ns
$\overline{INT}$ signal clear time	for INT non-hold mode	$\overline{UDS}/\overline{LDS}$ "L"	t_{DH}	J	—	50	ns
	for INT hold mode	$\overline{UDS}/\overline{LDS}$ "H"	t_{DH2}	K	—	n t_{CLK} + 50	ns

* : The position number indicates the position in the waveform.

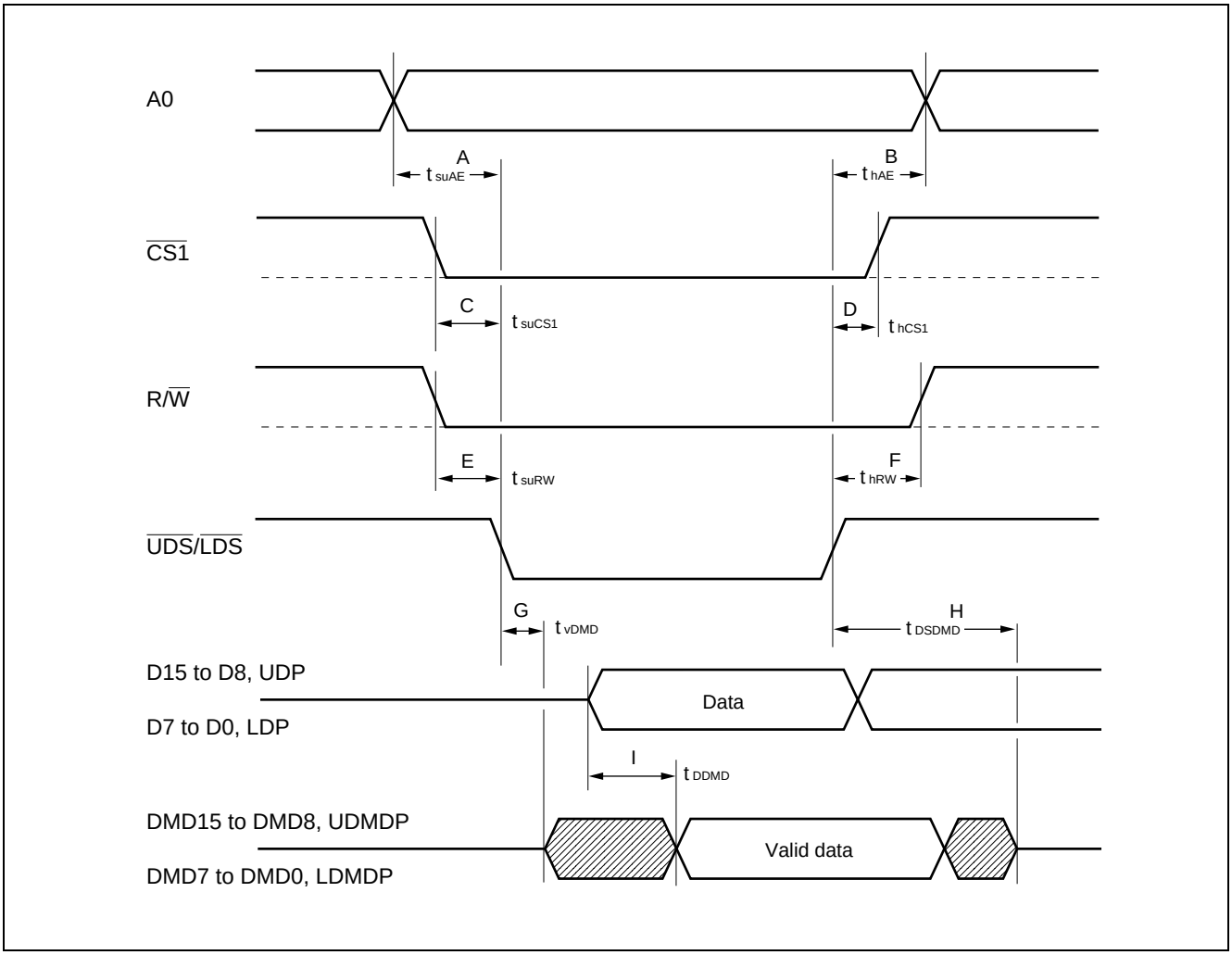


*: t_{DH2} is determined by a rising edge of the strobe signal which reads the step code for the last interrupt source. Also, "n" indicates the division ratio.

- **Register write timing (for external access)**

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
Address (A0) set up time	$\overline{UDS}/\overline{LDS}$ "L"	t_{suAE}	A	40	—	ns
Address (A0) hold time	$\overline{UDS}/\overline{LDS}$ "H"	t_{hAE}	B	20	—	ns
$\overline{CS1}$ set up time	$\overline{UDS}/\overline{LDS}$ "L"	t_{suCS1}	C	20	—	ns
$\overline{CS1}$ hold time	$\overline{UDS}/\overline{LDS}$ "H"	t_{hCS1}	D	10	—	ns
R/$\overline{W}$ set up time	$\overline{UDS}/\overline{LDS}$ "L"	t_{suRW}	E	20	—	ns
R/$\overline{W}$ hold time	$\overline{UDS}/\overline{LDS}$ "H"	t_{hRW}	F	20	—	ns
DMA data bus output delay time	$\overline{UDS}/\overline{LDS}$ "L"	t_{vDMD}	G	—	70	ns
DMA data bus output undefined time	$\overline{UDS}/\overline{LDS}$ "H"	t_{DSDMD}	H	10	—	ns
MPU data → DMA data bus output delay time	—	t_{DDMD}	I	—	40	ns

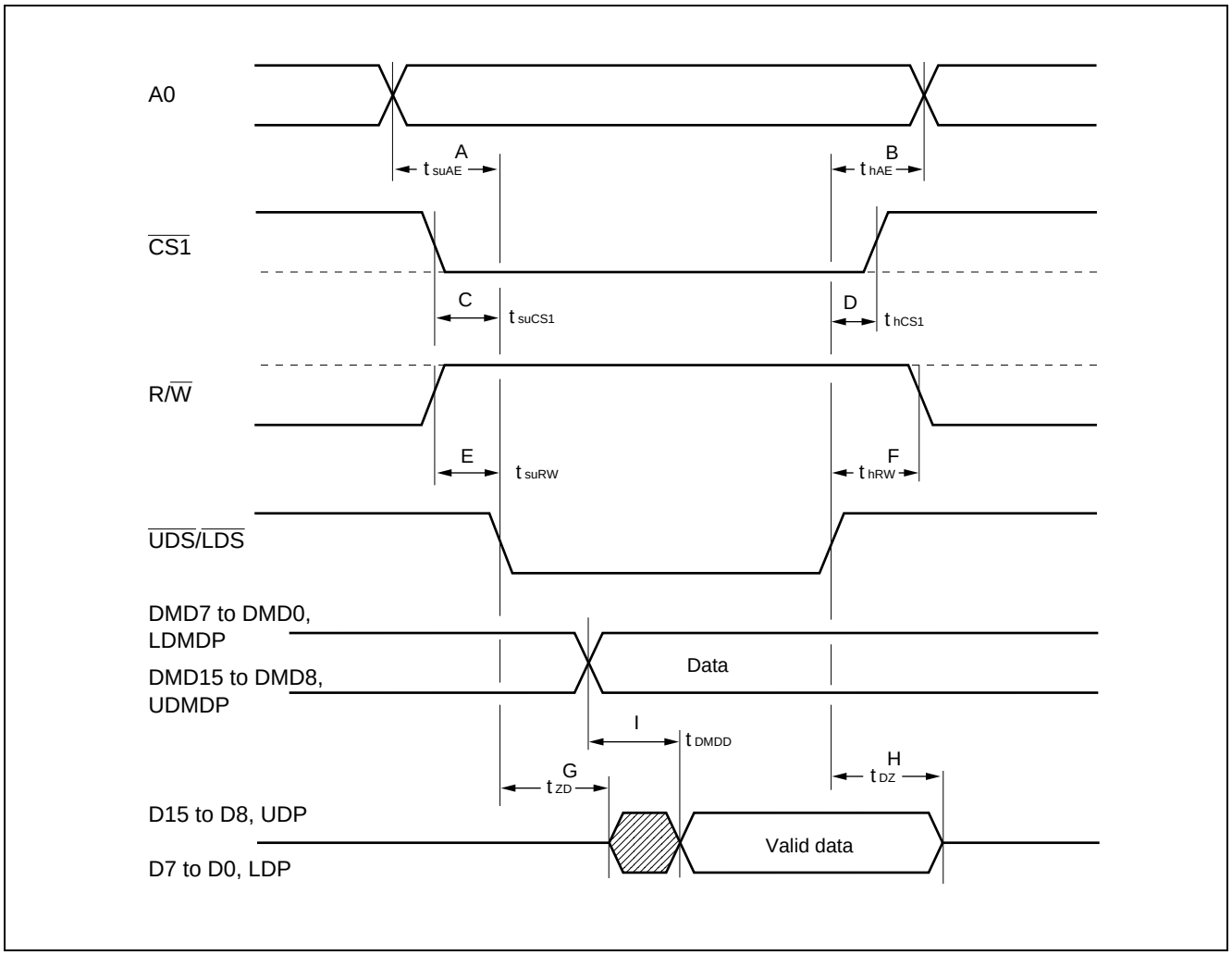
* : The position number indicates the position in the waveform.



- **Register read timing (for external access)**

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
Address (A0) set up time	$\overline{UDS}/\overline{LDS}$ "L"	t_{suAE}	A	40	—	ns
Address (A0) hold time	$\overline{UDS}/\overline{LDS}$ "H"	t_{hAE}	B	20	—	ns
$\overline{CS1}$ set up time	$\overline{UDS}/\overline{LDS}$ "L"	t_{suCS1}	C	20	—	ns
$\overline{CS1}$ hold time	$\overline{UDS}/\overline{LDS}$ "H"	t_{hCS1}	D	10	—	ns
R/$\overline{W}$ set up time	$\overline{UDS}/\overline{LDS}$ "L"	t_{suRW}	E	20	—	ns
R/$\overline{W}$ hold time	$\overline{UDS}/\overline{LDS}$ "H"	t_{hRW}	F	20	—	ns
Data output enable time	$\overline{UDS}/\overline{LDS}$ "L"	t_{ZD}	G	—	70	ns
Data output disable time	$\overline{UDS}/\overline{LDS}$ "H"	t_{DZ}	H	10	—	ns
DMA data → MPU data bus output delay time	—	t_{DMDD}	I	—	40	ns

* : The position number indicates the position in the waveform.



(5) DMA interface

The DMA access timing described in this section is not applicable in the following cases.

During SCSI input, when the data buffer is EMPTY or when one byte is stored
During SCSI output, when the data buffer is FULL or when 31 bytes are stored
When a parity error is detected (target)
When an error which pauses the transfer occurs at the SCSI interface

- **80 series handshake mode**

(a) Write timing

Parameter		Symbol		Value		Unit
	Base signal		Position*	Min.	Max.	
$\overline{DACK}$ “L” assert time	DREQ “H”	t_{RQAK}	A	0	—	ns
DREQ “L” negate time	$\overline{DACK}$ “L”	t_{AKRQ}	B	—	40	ns
DREQ “H” assert time (8 bit)	$\overline{DACK}$ “H”	t_{AKRQ1}	C	—	50	ns
DREQ “H” assert time (16 bit)	$\overline{DACK}$ “H”	t_{AKRQ2}	C	—	$2\ t_{CLK} + 40$	ns
$\overline{IOWR}$ “L” assert time	$\overline{DACK}$ “L”	t_{AKWR}	D	0	—	ns
$\overline{DMBHE}$, DMA0 set up time	$\overline{IOWR}$ “L”	t_{suDA}	E	20	—	ns
$\overline{DMBHE}$, DMA0 hold time	$\overline{IOWR}$ “H”	t_{hDA}	F	20	—	ns
$\overline{IOWR}$ “L” level pulse width	—	t_{wWRL}	G	40	—	ns
$\overline{DACK}$ “H” negate time	$\overline{IOWR}$ “L”	t_{WRAK1}	H	$1\ t_{CLK}$	—	ns
	$\overline{IOWR}$ “H”	t_{WRAK2}	I	0	—	ns
Input data set up time	$\overline{IOWR}$ “H”	t_{suDMD}	J	30	—	ns
Input data hold time	$\overline{IOWR}$ “H”	t_{hDMD}	K	5	—	ns

* : The position number indicates the position in the waveform.

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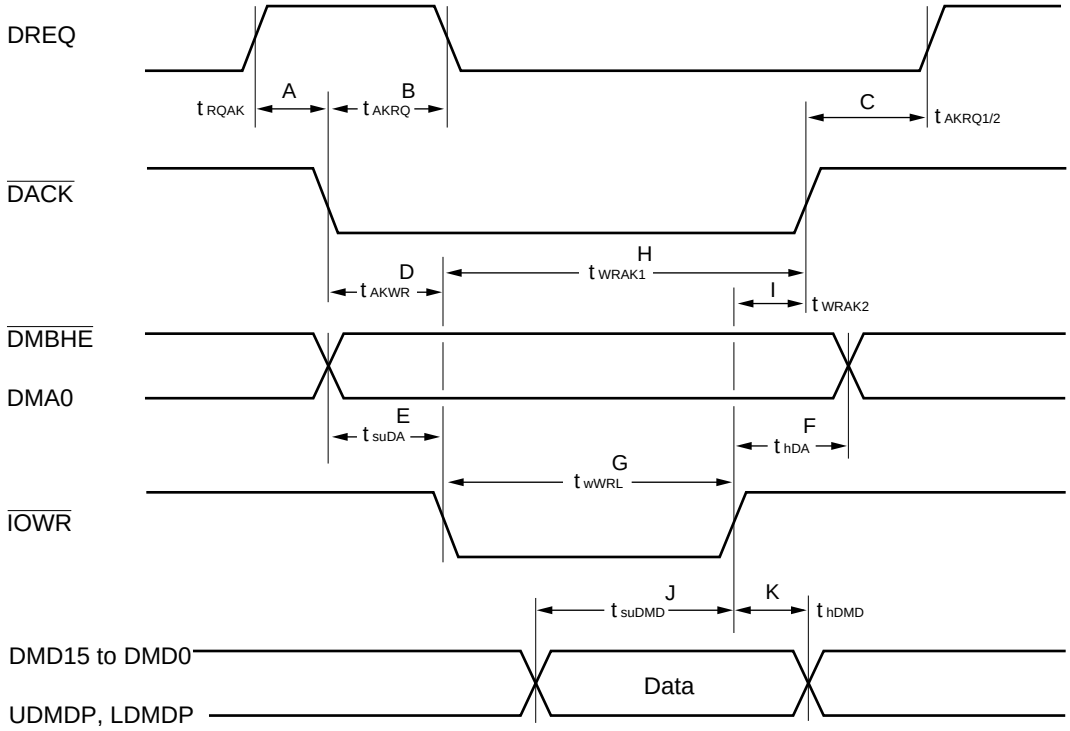
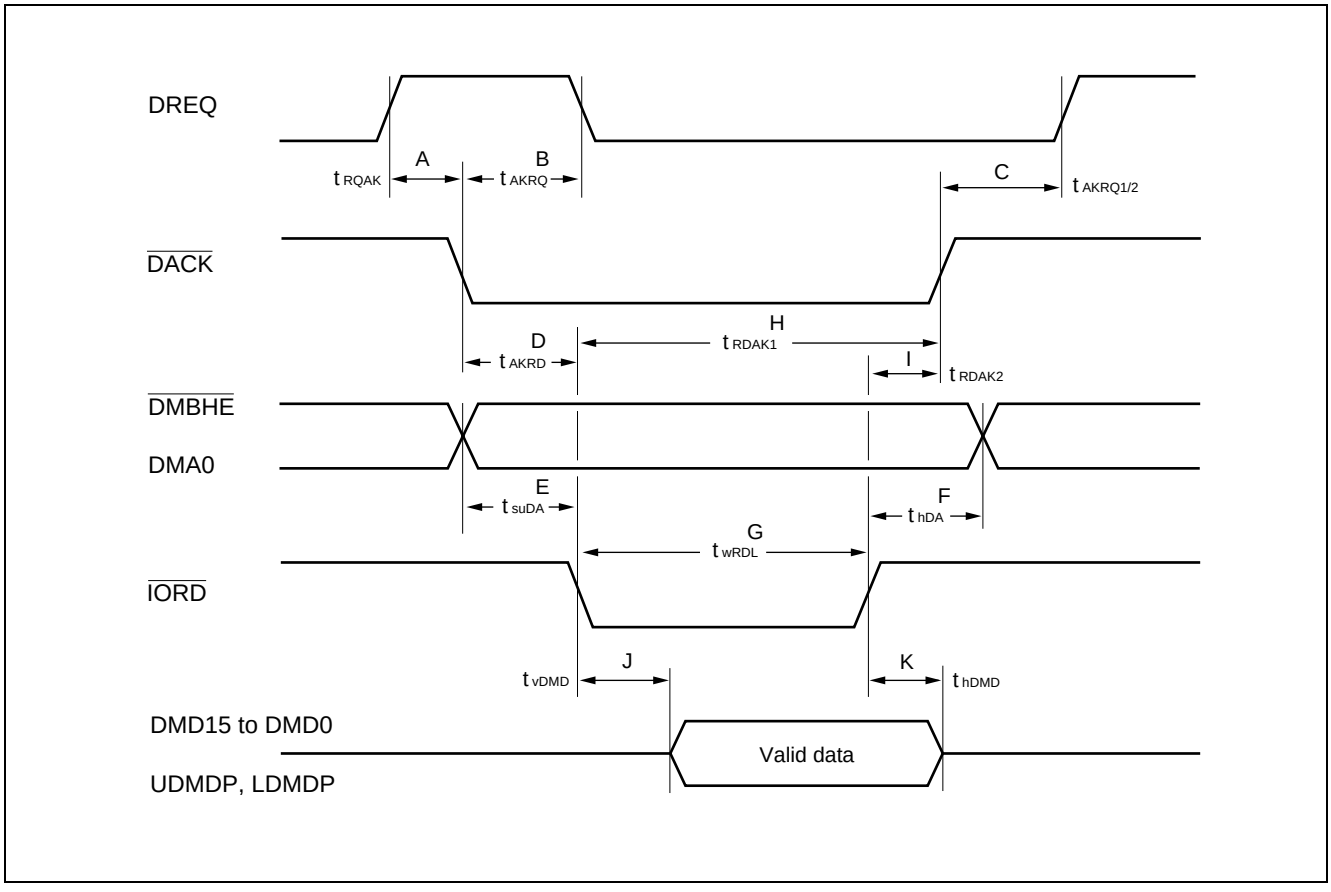

DREQ
A
B
C
t RQAK
t AKRQ
t AKRQ1/2
DACK
D
H
I
t AKWR
t WRAK1
t WRAK2
DMBHE
DMA0
E
F
G
t suDA
t hDA
t wWRL
IOWR
J
K
t suDMD
t hDMD
DMD15 to DMD0
Data
UDMDP, LDMDP

(b) Read timing

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
$\overline{DACK}$ “L” assert time	DREQ “H”	t_{RQAK}	A	0	—	ns
DREQ “L” negate time	$\overline{DACK}$ “L”	t_{AKRQ}	B	—	40	ns
DREQ “H” assert time (8 bit)	$\overline{DACK}$ “H”	t_{AKRQ1}	C	—	50	ns
DREQ “H” assert time (16 bit)	$\overline{DACK}$ “H”	t_{AKRQ2}	C	—	$2\ t_{CLK} + 40$	ns
$\overline{IORD}$ “L” assert time	$\overline{DACK}$ “L”	t_{AKRD}	D	0	—	ns
$\overline{DMBHE}$, DMA0 set up time	$\overline{IORD}$ “L”	t_{suDA}	E	20	—	ns
$\overline{DMBHE}$, DMA0 hold time	$\overline{IORD}$ “H”	t_{hDA}	F	20	—	ns
$\overline{IORD}$ “L” level pulse width	—	t_{wRDL}	G	40	—	ns
$\overline{DACK}$ “H” negate time	$\overline{IORD}$ “L”	t_{RDAK1}	H	$1\ t_{CLK}$	—	ns
	$\overline{IORD}$ “H”	t_{RDAK2}	I	0	—	ns
Data output defined time	$\overline{IORD}$ “L”	t_{vDMD}	J	—	40	ns
Data output hold time	$\overline{IORD}$ “H”	t_{hDMD}	K	10	—	ns

* : The position number indicates the position in the waveform.

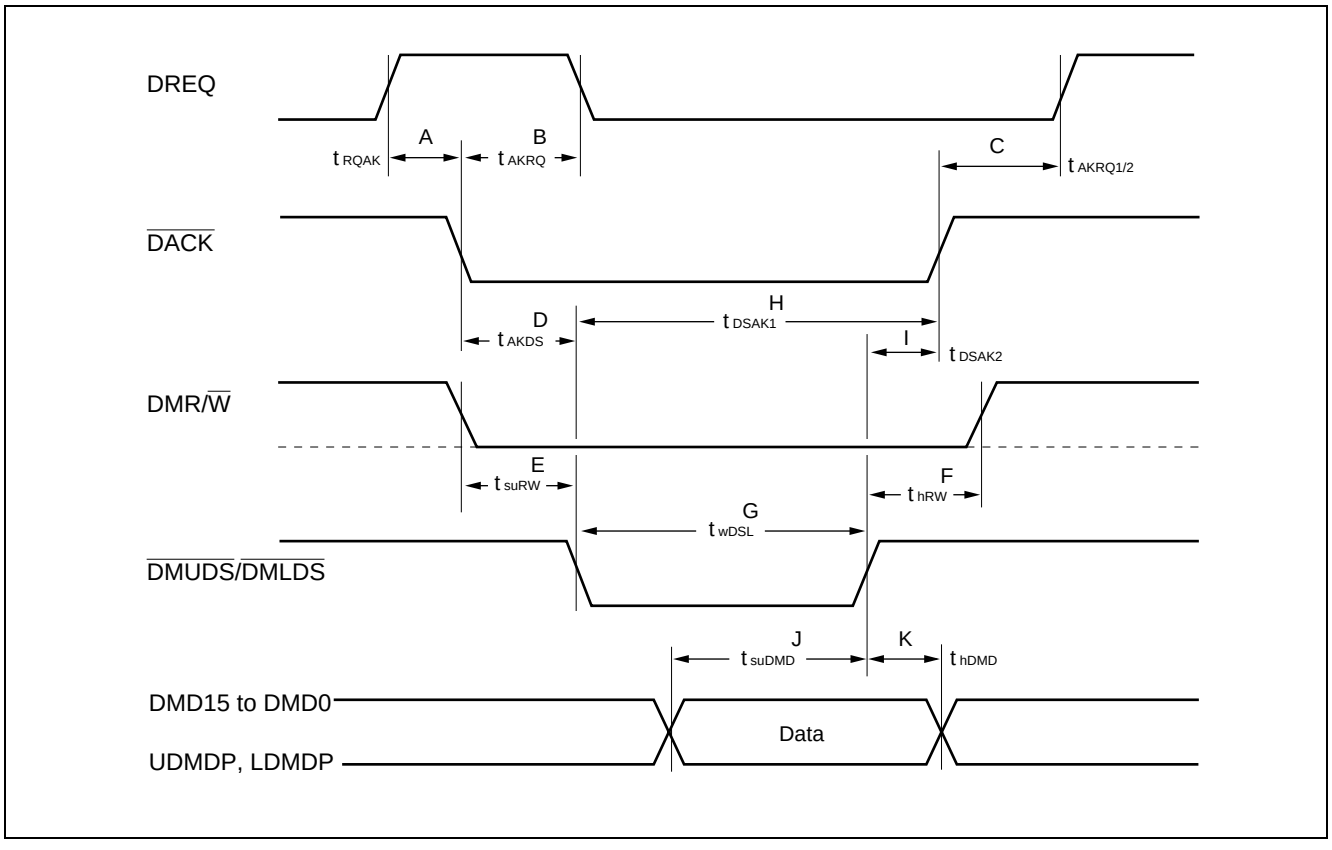


- **68 series handshake mode**

(a) Write timing

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
$\overline{DACK}$ “L” assert time	DREQ “H”	t_{RQAK}	A	0	—	ns
DREQ “L” negate time	$\overline{DACK}$ “L”	t_{AKRQ}	B	—	40	ns
DREQ “H” assert time (8 bit)	$\overline{DACK}$ “H”	t_{AKRQ1}	C	—	50	ns
DREQ “H” assert time (16 bit)	$\overline{DACK}$ “H”	t_{AKRQ2}	C	—	$2\ t_{CLK} + 40$	ns
$\overline{DMUDS}$/$\overline{DMLDS}$ “L” assert time	$\overline{DACK}$ “L”	t_{AKDS}	D	0	—	ns
DMR/$\overline{W}$ set up time	$\overline{DMUDS}$/$\overline{DMLDS}$ “L”	t_{suRW}	E	20	—	ns
DMR/$\overline{W}$ hold time	$\overline{DMUDS}$/$\overline{DMLDS}$ “H”	t_{hRW}	F	20	—	ns
$\overline{DMUDS}$/$\overline{DMLDS}$ “L” level pulse width	—	t_{wDSL}	G	40	—	ns
$\overline{DACK}$ “H” negate time	$\overline{DMUDS}$/$\overline{DMLDS}$ “L”	t_{DSAK1}	H	$1\ t_{CLK}$	—	ns
	$\overline{DMUDS}$/$\overline{DMLDS}$ “H”	t_{DSAK2}	I	0	—	ns
Input data set up time	$\overline{DMUDS}$/$\overline{DMLDS}$ “H”	t_{suDMD}	J	30	—	ns
Input data hold time	$\overline{DMUDS}$/$\overline{DMLDS}$ “H”	t_{hDMD}	K	5	—	ns

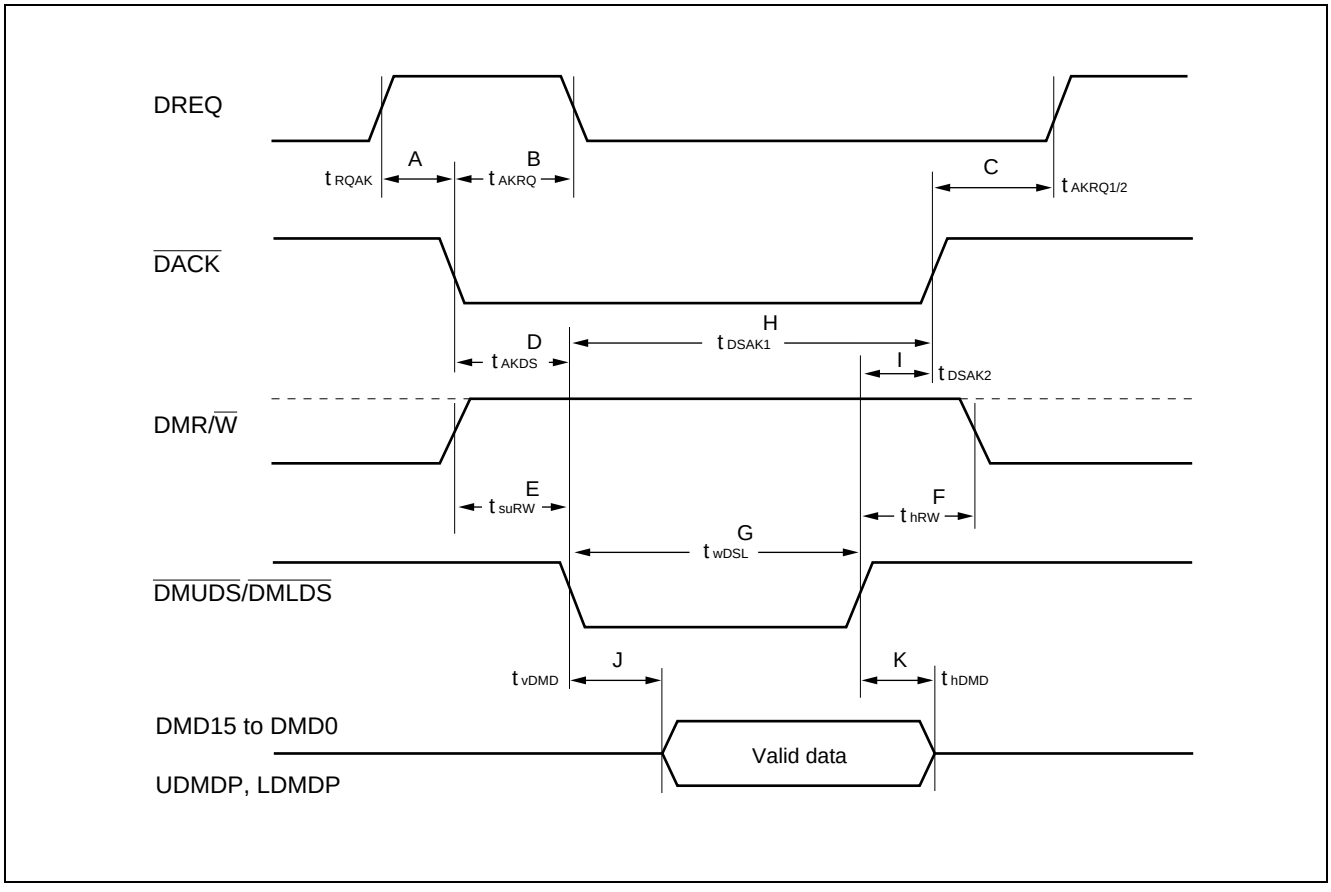
* : The position number indicates the position in the waveform.



(b) Read timing

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
$\overline{DACK}$ “L” assert time	DREQ “H”	t_{RQAK}	A	0	—	ns
DREQ “L” negate time	$\overline{DACK}$ “L”	t_{AKRQ}	B	—	40	ns
DREQ “H” assert time (8 bit)	$\overline{DACK}$ “H”	t_{AKRQ1}	C	—	50	ns
DREQ “H” assert time (16 bit)	$\overline{DACK}$ “H”	t_{AKRQ2}	C	—	$2\ t_{CLK} + 40$	ns
$\overline{DMUDS}$/$\overline{DMLDS}$ “L” assert time	$\overline{DACK}$ “L”	t_{AKDS}	D	0	—	ns
DMR/$\overline{W}$ set up time	$\overline{DMUDS}$/$\overline{DMLDS}$ “L”	t_{suRW}	E	20	—	ns
DMR/$\overline{W}$ hold time	$\overline{DMUDS}$/$\overline{DMLDS}$ “H”	t_{hRW}	F	20	—	ns
$\overline{DMUDS}$/$\overline{DMLDS}$ “L” level pulse width	—	t_{wDSL}	G	40	—	ns
$\overline{DACK}$ “H” negate time	$\overline{DMUDS}$/$\overline{DMLDS}$ “L”	t_{DSAK1}	H	$1\ t_{CLK}$	—	ns
	$\overline{DMUDS}$/$\overline{DMLDS}$ “H”	t_{DSAK2}	I	0	—	ns
Data output defined time	$\overline{DMUDS}$/$\overline{DMLDS}$ “L”	t_{vDMD}	J	—	40	ns
Data output hold time	$\overline{DMUDS}$/$\overline{DMLDS}$ “H”	t_{hDMD}	K	10	—	ns

* : The position number indicates the position in the waveform.

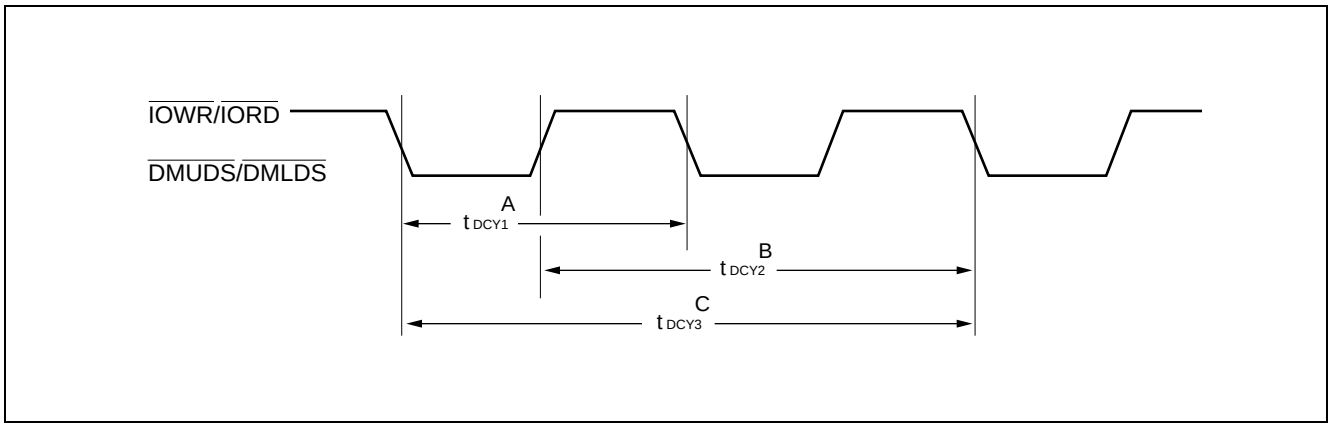


- **Burst mode (80 series/68 series common)**

(a) Data register access cycle time (8 bit)

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
Data register access cycle time 1	—	t_{DCY1}	A	t_{CLK}	—	ns
Data register access cycle time 2	—	t_{DCY2}	B	3 t_{CLK}	—	ns
Data register access cycle time 3	—	t_{DCY3}	C	4 t_{CLK}	—	ns

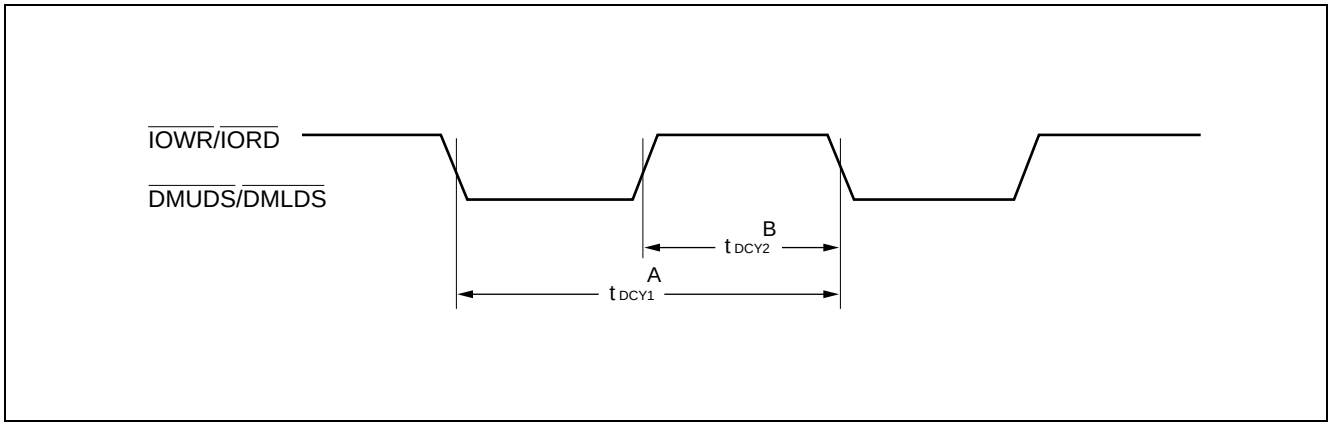
* : The position number indicates the position in the waveform.



(b) Data register access cycle time (16 bit)

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
Data register access cycle time 1	—	t_{DCY1}	A	4 t_{CLK}	—	ns
Data register access cycle time 2	—	t_{DCY2}	B	3 t_{CLK}	—	ns

* : The position number indicates the position in the waveform.

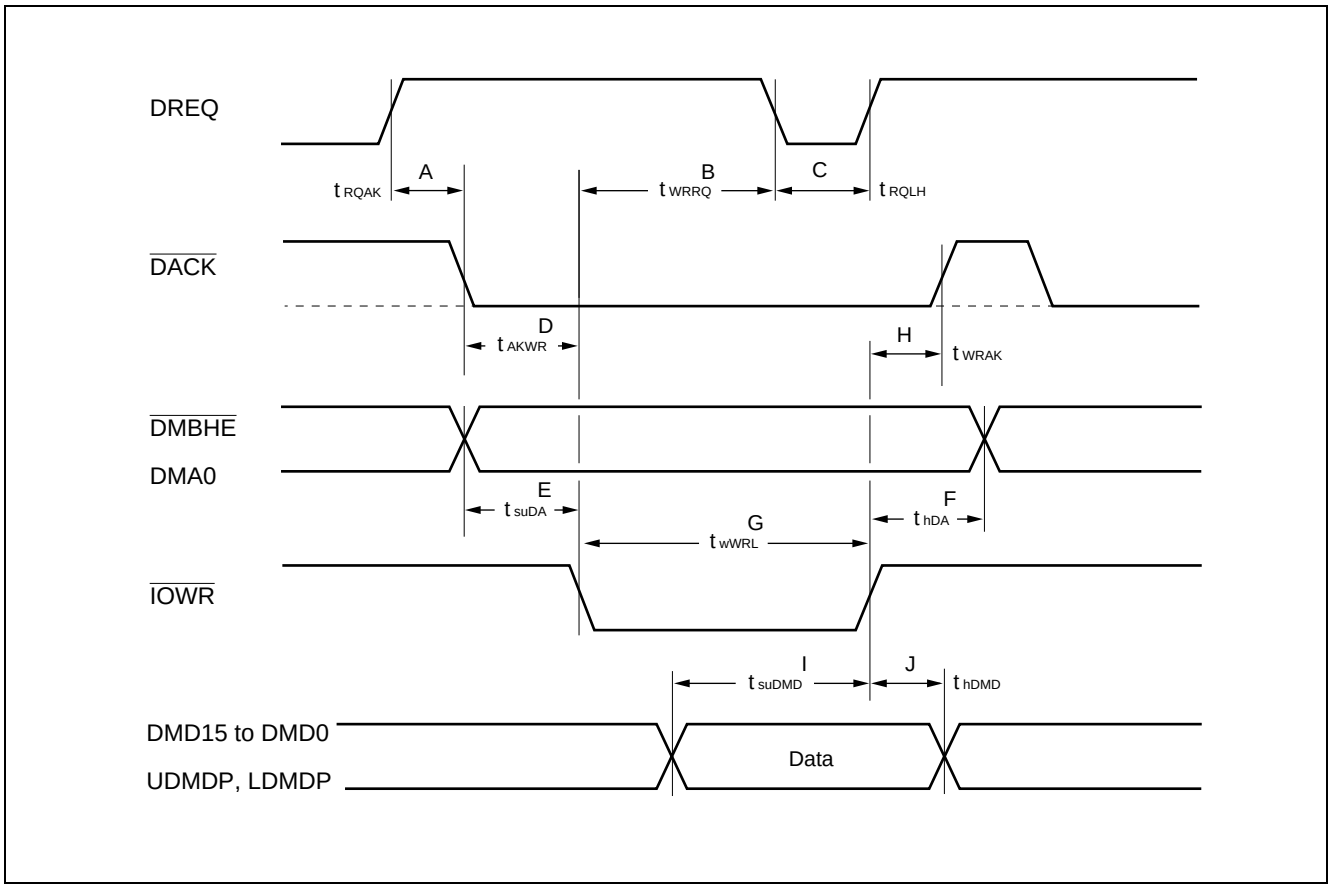


- **80 series burst mode**

(a) Write timing

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
$\overline{DACK}$ “L” assert time	DREQ “H”	t_{RQAK}	A	0	—	ns
DREQ “L” negate time	$\overline{IOWR}$ “L”	t_{WRRQ}	B	—	55	ns
DREQ “L” → DREQ “H” return time	—	t_{RQLH}	C	0	—	ns
$\overline{IOWR}$ “L” assert time	$\overline{DACK}$ “L”	t_{AKWR}	D	0	—	ns
$\overline{DMBHE}$, DMA0 set up time	$\overline{IOWR}$ “L”	t_{suDA}	E	20	—	ns
$\overline{DMBHE}$, DMA0 hold time	$\overline{IOWR}$ “H”	t_{hDA}	F	20	—	ns
$\overline{IOWR}$ “L” level pulse width	—	t_{wWRL}	G	40	—	ns
$\overline{DACK}$ “H” negate time	$\overline{IOWR}$ “H”	t_{WRAK}	H	0	—	ns
Input data set up time	$\overline{IOWR}$ “H”	t_{suDMD}	I	30	—	ns
Input data hold time	$\overline{IOWR}$ “H”	t_{hDMD}	J	5	—	ns

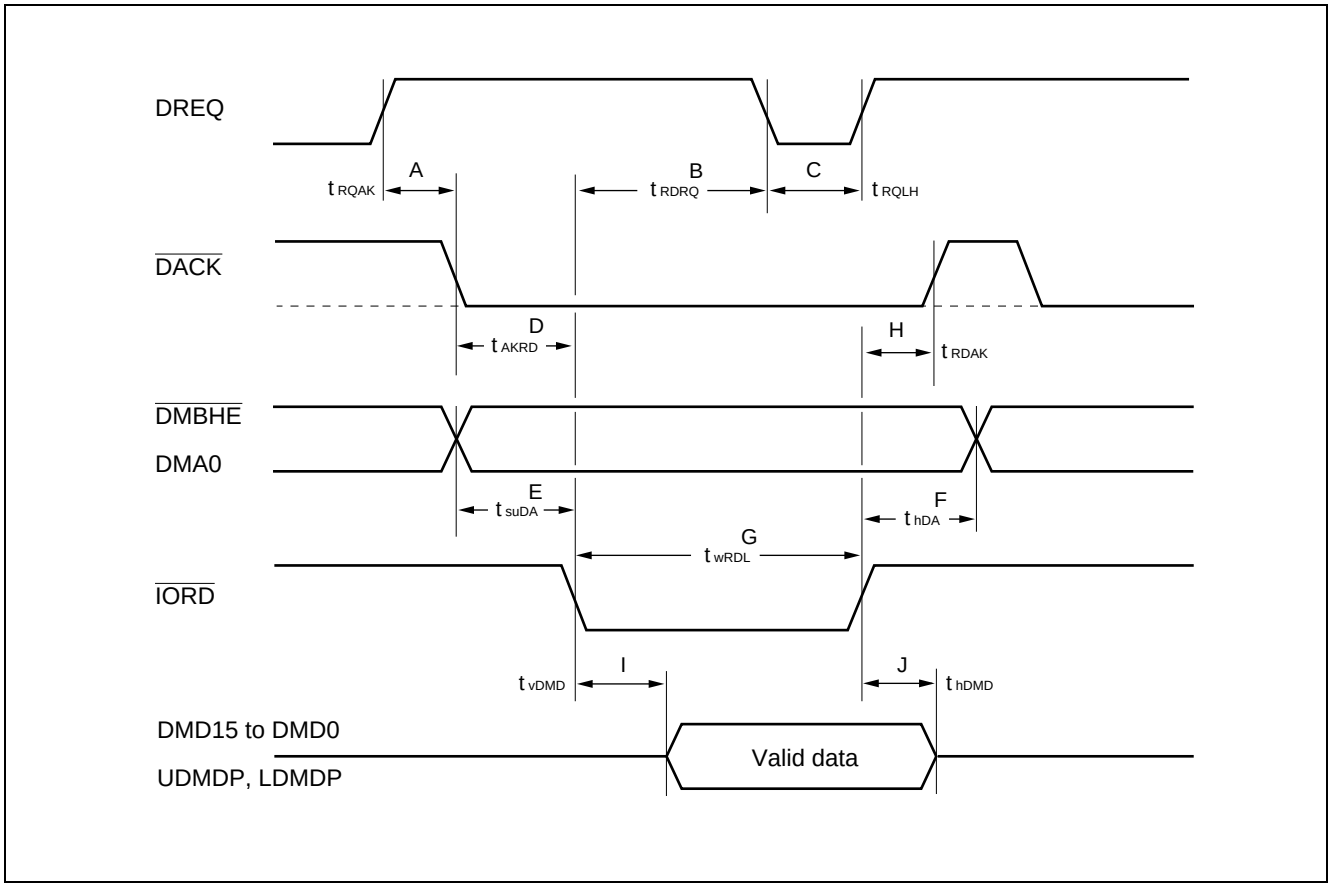
* : The position number indicates the position in the waveform.



(b) Read timing

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
$\overline{DACK}$ “L” assert time	DREQ “H”	t_{RQAK}	A	0	—	ns
DREQ “L” negate time	$\overline{IORD}$ “L”	t_{RDRQ}	B	—	55	ns
DREQ “L” → DREQ “H” return time	—	t_{RQLH}	C	0	—	ns
$\overline{IORD}$ “L” assert time	$\overline{DACK}$ “L”	t_{AKRD}	D	0	—	ns
$\overline{DMBHE}$, DMA0 set up time	$\overline{IORD}$ “L”	t_{suDA}	E	20	—	ns
$\overline{DMBHE}$, DMA0 hold time	$\overline{IORD}$ “H”	t_{hDA}	F	20	—	ns
$\overline{IORD}$ “L” level pulse width	—	t_{wRDL}	G	40	—	ns
$\overline{DACK}$ “H” negate time	$\overline{IORD}$ “H”	t_{RDAK}	H	0	—	ns
Data output defined time	$\overline{IORD}$ “L”	t_{vDMD}	I	—	40	ns
Data output hold time	$\overline{IORD}$ “H”	t_{hDMD}	J	10	—	ns

* : The position number indicates the position in the waveform.

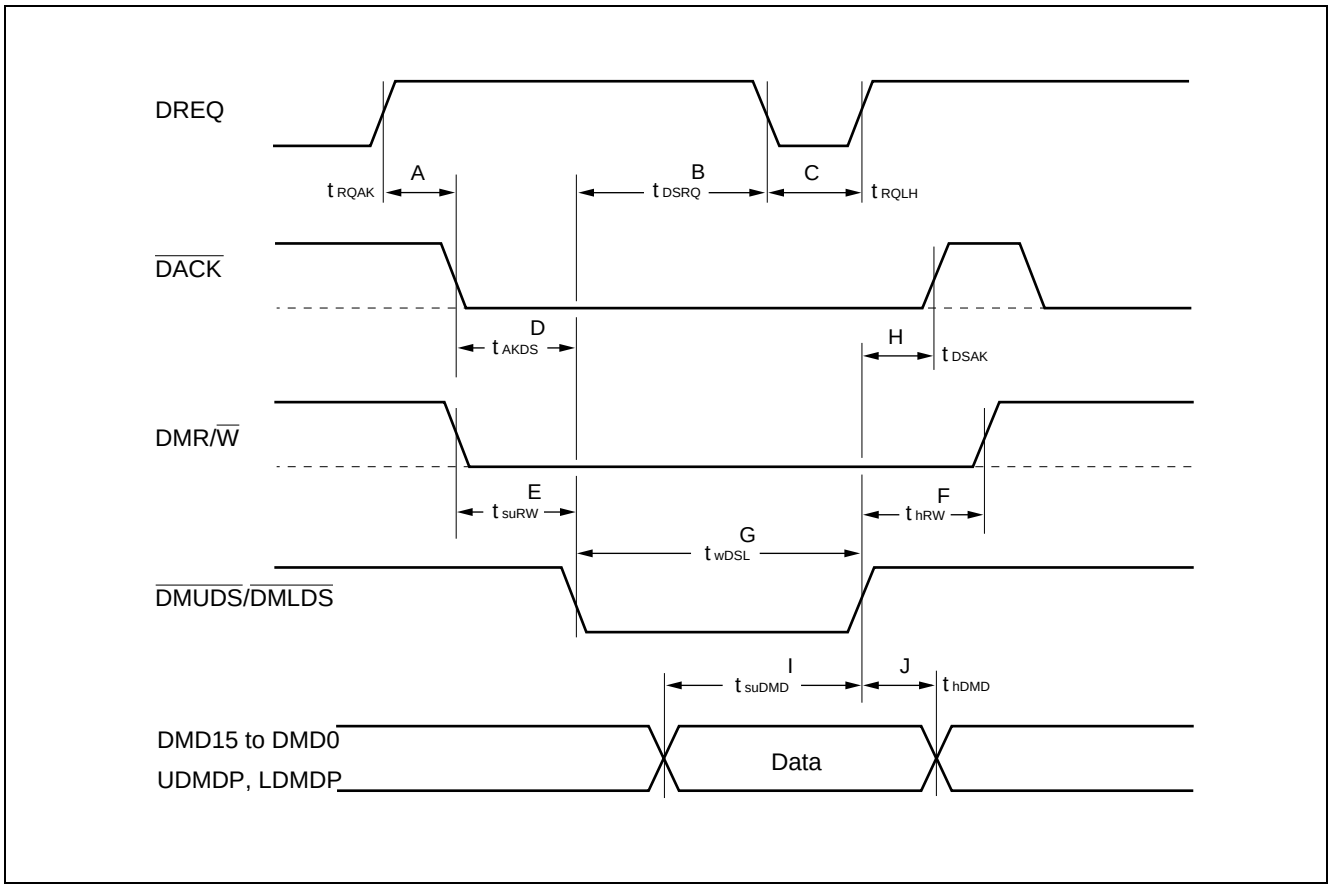


- **68 series burst mode**

(a) Write timing

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
$\overline{DACK}$ “L” assert time	DREQ “H”	t_{RQAK}	A	0	—	ns
DREQ “L” negate time	$\overline{DMUDS}$/$\overline{DMLDS}$ “L”	t_{DSRQ}	B	—	55	ns
DREQ “L” → DREQ “H” return time	—	t_{RQLH}	C	0	—	ns
$\overline{DMUDS}$/$\overline{DMLDS}$ “L” assert time	DACK “L”	t_{AKDS}	D	0	—	ns
DMR/$\overline{W}$ set up time	$\overline{DMUDS}$/$\overline{DMLDS}$ “L”	t_{suRW}	E	20	—	ns
DMR/$\overline{W}$ hold time	$\overline{DMUDS}$/$\overline{DMLDS}$ “H”	t_{hRW}	F	20	—	ns
$\overline{DMUDS}$/$\overline{DMLDS}$ “L” level pulse width	—	t_{wDSL}	G	40	—	ns
$\overline{DACK}$ “H” negate time	$\overline{DMUDS}$/$\overline{DMLDS}$ “H”	t_{DSAK}	H	0	—	ns
Input data set up time	$\overline{DMUDS}$/$\overline{DMLDS}$ “H”	t_{suDMD}	I	30	—	ns
Input data hold time	$\overline{DMUDS}$/$\overline{DMLDS}$ “H”	t_{hDMD}	J	5	—	ns

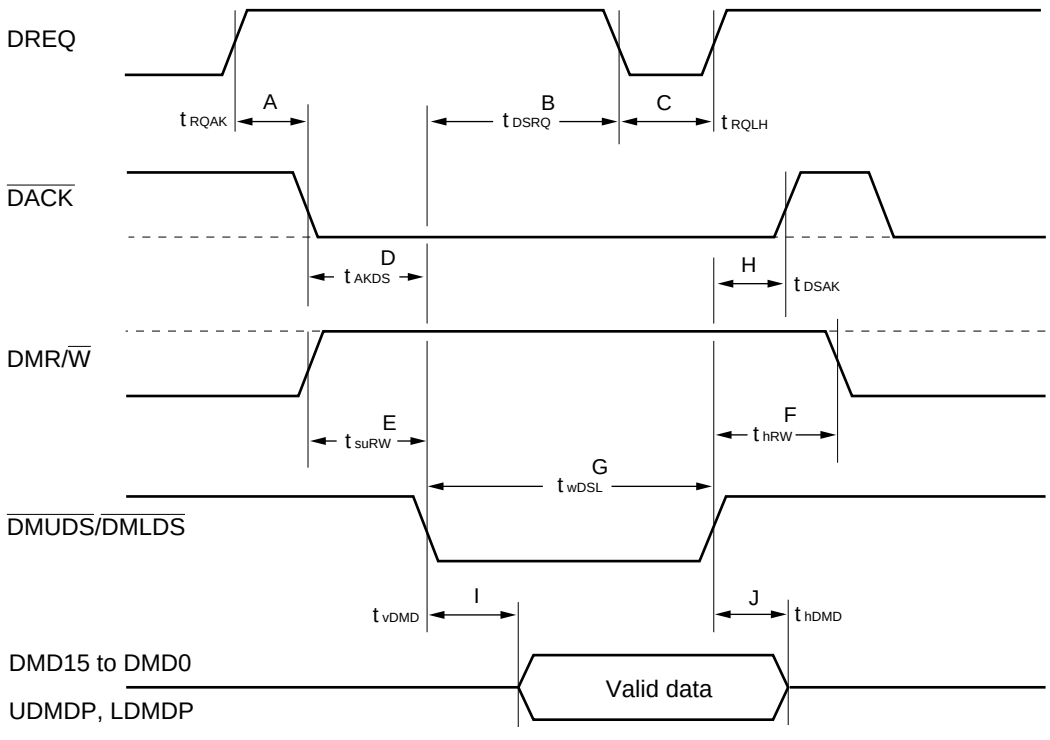
* : The position number indicates the position in the waveform.



(b) Read timing

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
$\overline{DACK}$ “L” assert time	DREQ “H”	t_{RQAK}	A	0	—	ns
DREQ “L” negate time	$\overline{DMUDS}/\overline{DMLDS}$ “L”	t_{DSRQ}	B	—	55	ns
DREQ “L” → DREQ “H” return time	—	t_{RQLH}	C	0	—	ns
$\overline{DMUDS}/\overline{DMLDS}$ “L” assert time	$\overline{DACK}$ “L”	t_{AKDS}	D	0	—	ns
DMR/$\overline{W}$ set up time	$\overline{DMUDS}/\overline{DMLDS}$ “L”	t_{suRW}	E	20	—	ns
DMR/$\overline{W}$ hold time	$\overline{DMUDS}/\overline{DMLDS}$ “H”	t_{hRW}	F	20	—	ns
$\overline{DMUDS}/\overline{DMLDS}$ “L” level pulse width	—	t_{wDSL}	G	40	—	ns
$\overline{DACK}$ “H” negate time	$\overline{DMUDS}/\overline{DMLDS}$ “H”	t_{DSAK}	H	0	—	ns
Data output defined time	$\overline{DMUDS}/\overline{DMLDS}$ “L”	t_{vDMD}	I	—	40	ns
Data output hold time	$\overline{DMUDS}/\overline{DMLDS}$ “H”	t_{hDMD}	J	10	—	ns

* : The position number indicates the position in the waveform.



(6) SCSI interface (as initiator)

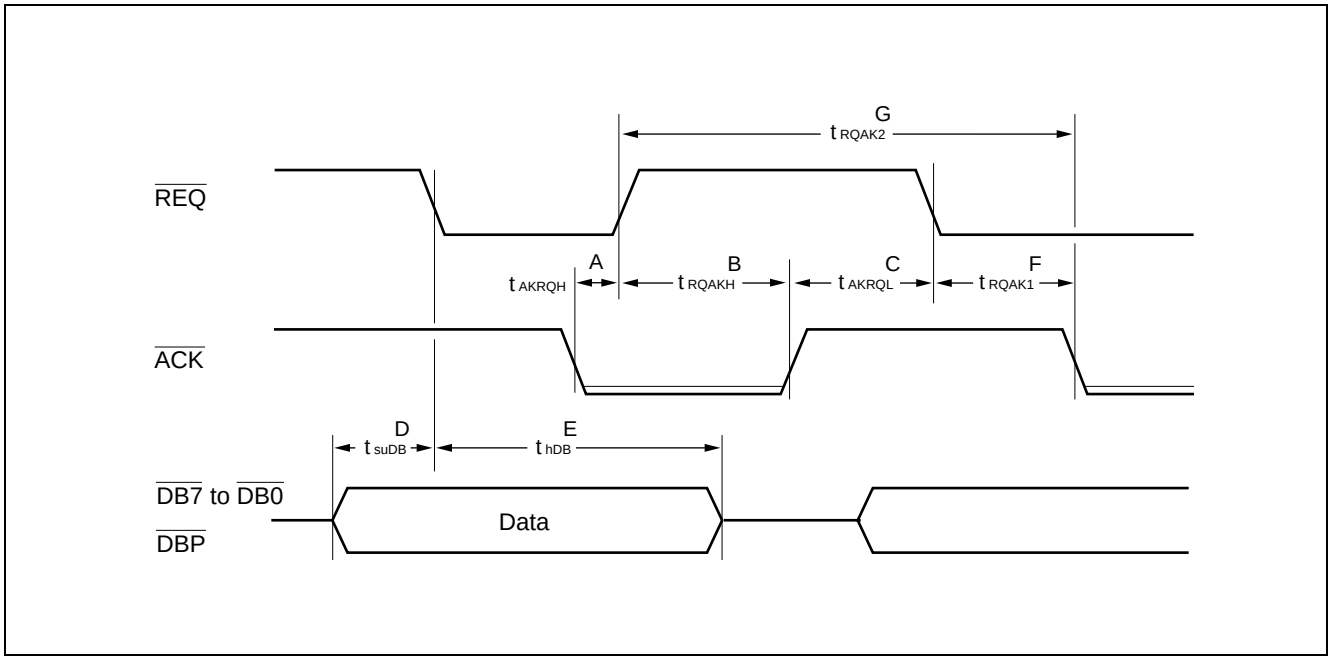
- **Asynchronous transfer mode**

(a) Input timing (target → initiator)

Parameter	Base signal	Symbol	Position*1	Value Min.	Value Max.	Unit
$\overline{REQ}$ "H" negate time	$\overline{ACK}$ "L"	t_{AKRQH}	A	0	—	ns
$\overline{ACK}$ "H" negate time	$\overline{REQ}$ "H"	t_{RQAKH}	B	—	60	ns
$\overline{REQ}$ "L" assert time	$\overline{ACK}$ "H"	t_{AKRQL}	C	10	—	ns
Input data set up time	$\overline{REQ}$ "L"	t_{suDB}	D	10	—	ns
Input data hold time	$\overline{REQ}$ "L"	t_{hDB}	E	20	—	ns
$\overline{ACK}$ "L" assert time 1	$\overline{REQ}$ "L"	t_{RQAK1}	F	—	40	ns
$\overline{ACK}$ "L" assert time 2 *2	$\overline{REQ}$ "H"	t_{RQAK2}	G	—	3 t_{CLK} + 40	ns

*1: The position number indicates the position in the waveform.
*2: The $\overline{REQ}$ "H" → $\overline{ACK}$ "L" time (t_{RQAK2}) is compared with (t_{RQAKH} + t_{AKRQL} + t_{RQAK1}) and the longer value is chosen.

Note: The input timing definition is not applied in the following cases.
- When the data register is FULL in the data phase
- When the final byte is being transferred

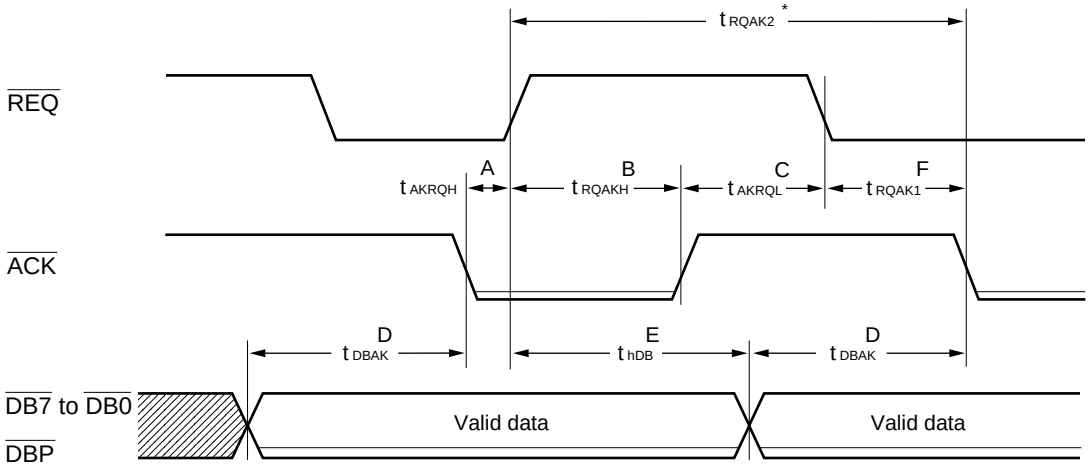


(b) Output timing (initiator → target)

Parameter	Base signal	Symbol	Position*1	Value Min.	Value Max.	Unit
$\overline{REQ}$ "H" negate time	$\overline{ACK}$ "L"	t_{AKRQH}	A	0	—	ns
$\overline{ACK}$ "H" negate time	$\overline{REQ}$ "H"	t_{RQAKH}	B	—	60	ns
$\overline{REQ}$ "L" assert time	$\overline{ACK}$ "H"	t_{AKRQL}	C	10	—	ns
Time from output data valid to $\overline{ACK}$ "L" assert *2	—	t_{DBAK}	D	S • t_{CLK} – 10	—	ns
Output data hold time	$\overline{REQ}$ "H"	t_{hDB}	E	2 t_{CLK}	—	ns
$\overline{ACK}$ "L" assert time	$\overline{REQ}$ "L"	t_{RQAK1}	F	—	40	ns

*1: The position number indicates the position in the waveform.
*2: "S" value is based on the asychronous set up time setting register (address 17h).

Note: The output timing definitions are not applied when the data register is EMPTY in the data phase.



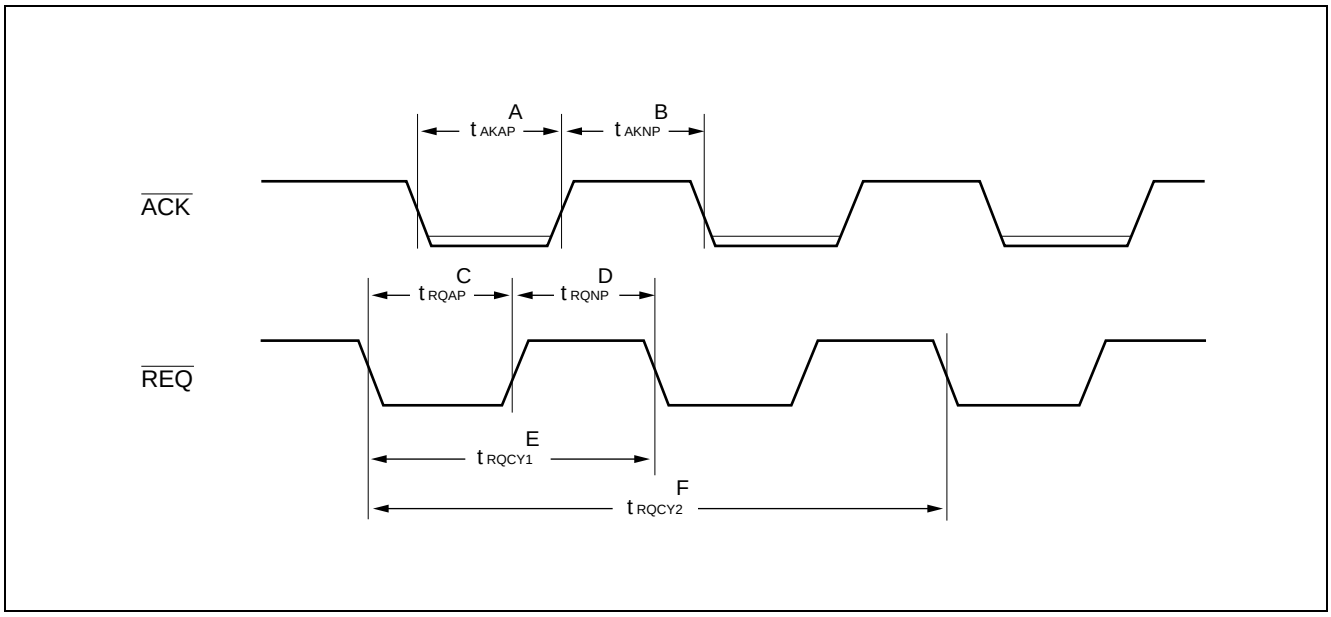
*: The $\overline{REQ}$ "H" → $\overline{ACK}$ "L" time (t_{RQAK2}) is defined by either longer of (t_{RQAKH} + t_{AKRQL} + t_{RQAK1}) or (t_{hDB} + t_{DBAK}) (see the output timing waveform).

- **Synchronous transfer mode**

(a) $\overline{REQ}$/$\overline{ACK}$ signal period

Parameter	Base signal	Symbol	Position*1	Value Min.	Value Max.	Unit
$\overline{ACK}$ assert time *2	—	t_{AKAP}	A	A • t_{CLK} – 12	—	ns
$\overline{ACK}$ negate time *2	—	t_{AKNP}	B	N • t_{CLK} + 2	—	ns
$\overline{REQ}$ assert time	—	t_{RQAP}	C	20	—	ns
$\overline{REQ}$ negate time	—	t_{RQNP}	D	20	—	ns
$\overline{REQ}$ input cycle time 1	—	t_{RQCY1}	E	1 t_{CLK}	—	ns
$\overline{REQ}$ input cycle time 2	—	t_{RQCY2}	F	3 t_{CLK}	—	ns

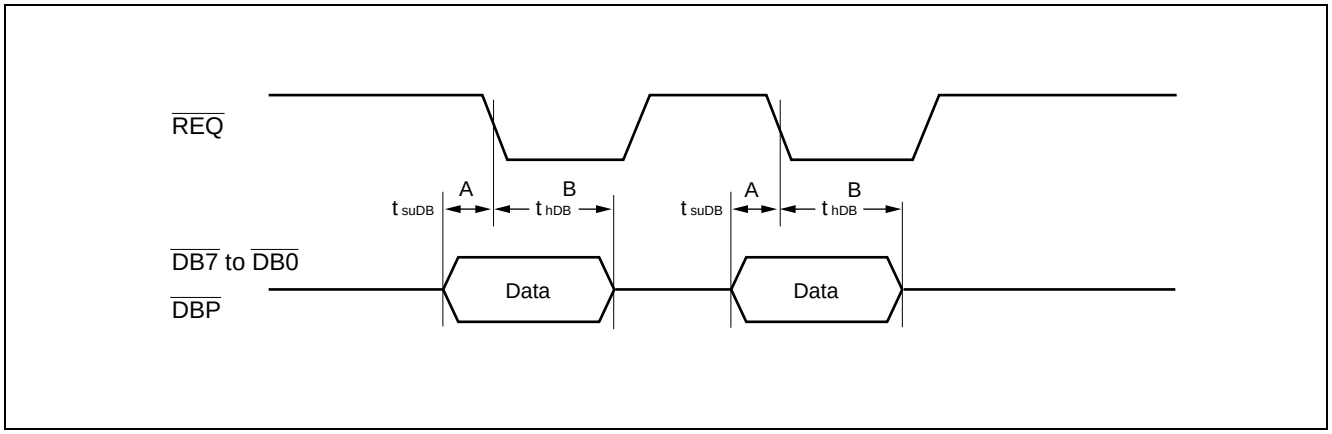
*1: The position number indicates the position in the waveform.
*2: “A” and “N” values are based on the transfer period register (address 0Dh) setting.



(b) Input timing (target → initiator)

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
Input data set up time	$\overline{REQ}$ "L"	t_{suDB}	A	5	—	ns
Input data hold time	$\overline{REQ}$ "L"	t_{hDB}	B	15	—	ns

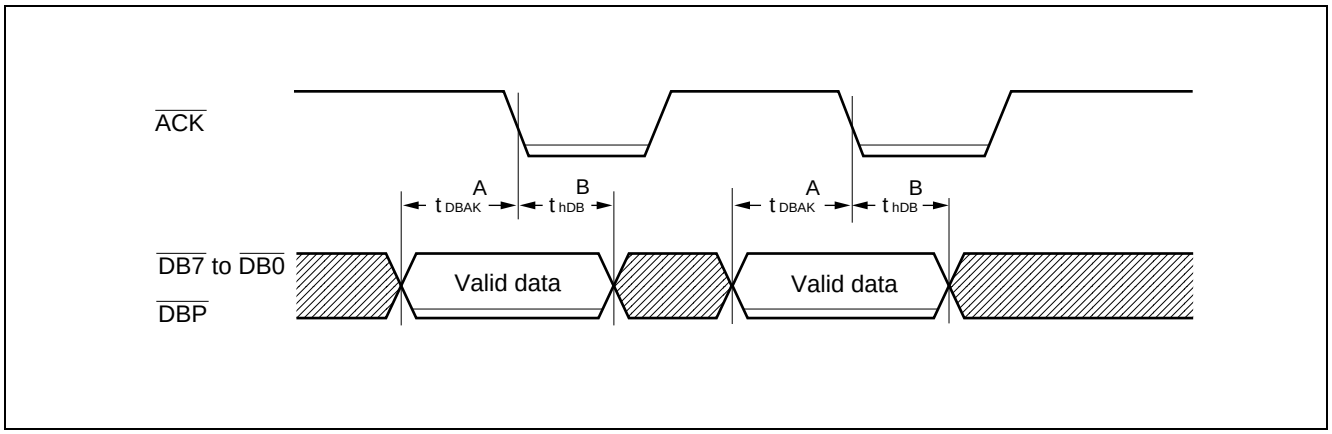
* : The position number indicates the position in the waveform.



(c) Input timing (target → initiator)

Parameter	Base signal	Symbol	Position*1	Value Min.	Value Max.	Unit
Time from output data valid to $\overline{ACK}$ "L" assert *2	—	t_{DBAK}	A	N • t_{CLK} + 2	—	ns
Output data hold time *2	$\overline{ACK}$ "L"	t_{hDB}	B	A • t_{CLK} – 12	—	ns

*1: The position number indicates the position in the waveform.
*2: "A" and "N" values are based on the transfer period register (address 0Dh) setting.



(7) SCSI interface (as initiator)

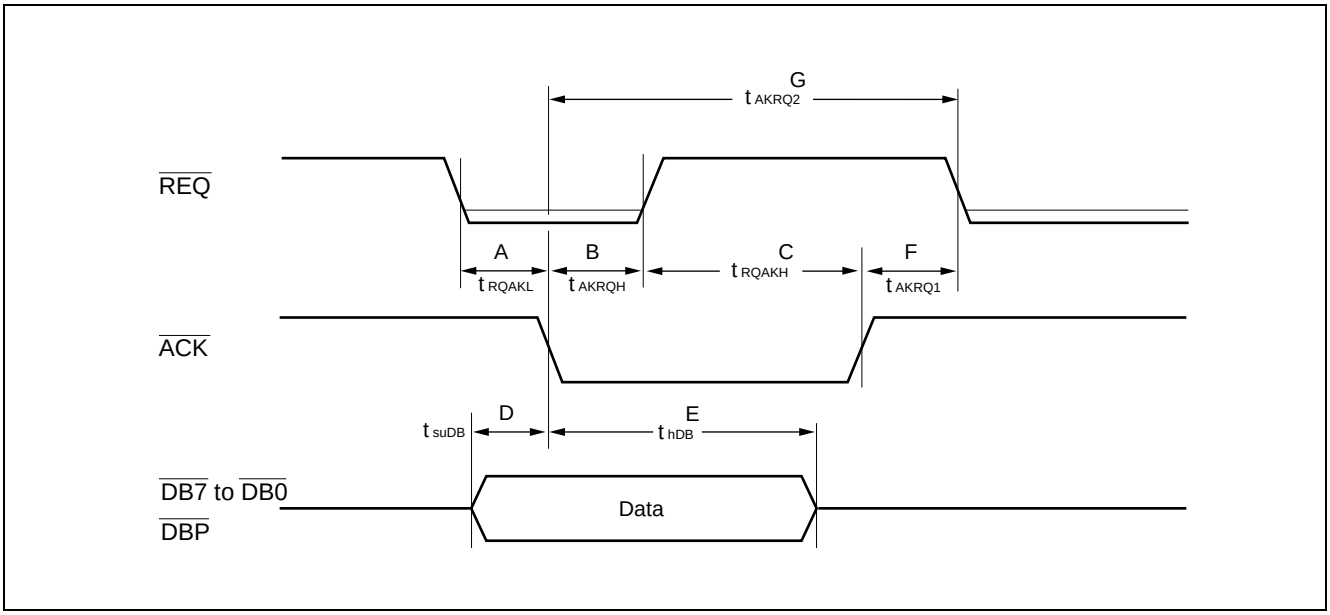
- **Asynchronous transfer mode**

(a) Input timing (initiator → target)

Parameter	Base signal	Symbol	Position*1	Value Min.	Value Max.	Unit
$\overline{ACK}$ "L" assert time	$\overline{REQ}$ "L"	t_{RQAKL}	A	0	—	ns
$\overline{REQ}$ "H" negate time	$\overline{ACK}$ "L"	t_{AKRQH}	B	—	60	ns
$\overline{ACK}$ "H" negate time	$\overline{REQ}$ "H"	t_{RQAKH}	C	0	—	ns
Input data set up time	$\overline{ACK}$ "L"	t_{suDB}	D	10	—	ns
Input data hold time	$\overline{ACK}$ "L"	t_{hDB}	E	20	—	ns
$\overline{ACK}$ "L" assert time 1	$\overline{ACK}$ "H"	t_{AKRQ1}	F	—	40	ns
$\overline{ACK}$ "L" assert time 2 *2	$\overline{ACK}$ "H"	t_{ALRQ2}	G	—	3 t_{CLK} + 40	ns

*1: The position number indicates the position in the waveform.
*2: The REQ "L" → REQ "L" time (t_{AKRQ2}) is compared with (t_{AKRQH} + t_{RQAKH} + t_{AKRQ1}) and the longer value is chosen.

Note: The input timing definition is not applied in the following cases.
- When the data register is FULL in the data phase
- When the final byte is being transferred

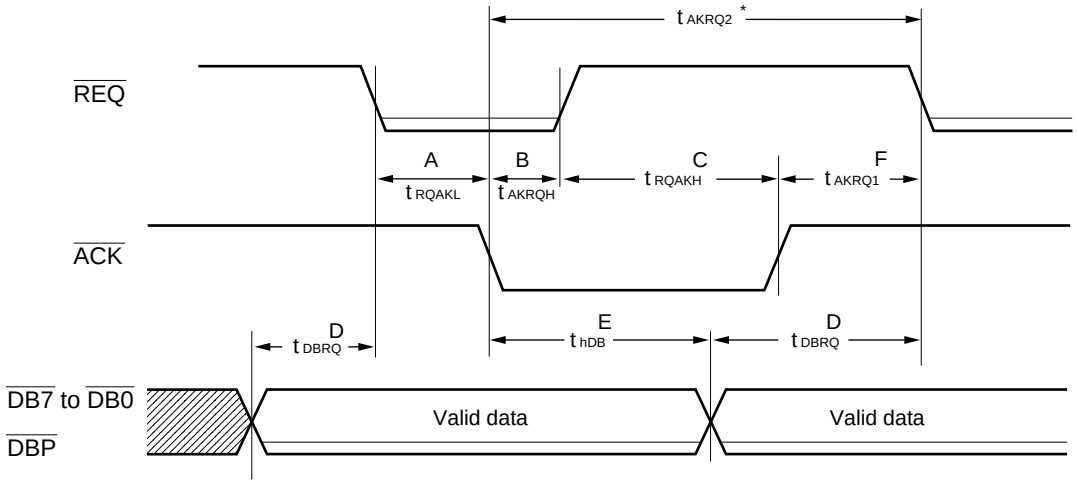


(b) Output timing (target → initiator)

Parameter	Base signal	Symbol	Position*1	Value Min.	Value Max.	Unit
$\overline{ACK}$ "L" assert time	$\overline{REQ}$ "L"	t_{RQAKL}	A	0	—	ns
$\overline{REQ}$ "H" negate time	$\overline{ACK}$ "L"	t_{AKRQH}	B	—	60	ns
$\overline{ACK}$ "H" negate time	$\overline{REQ}$ "H"	t_{RQAKH}	C	0	—	ns
Time from output data valid to $\overline{REQ}$ "L" assert *2	—	t_{DBRQ}	D	S • t_{CLK} – 10	—	ns
Output data hold time	$\overline{ACK}$ "L"	t_{hDB}	E	2 t_{CLK}	—	ns
$\overline{REQ}$ "L" assert time	$\overline{ACK}$ "H"	t_{AKRQ1}	F	—	40	ns

*1: The position number indicates the position in the waveform.
*2: "S" value is based on the asychronous set up time setting register (address 17h).

Note: The output timing definitions are not applied when the data register is EMPTY in the data phase.



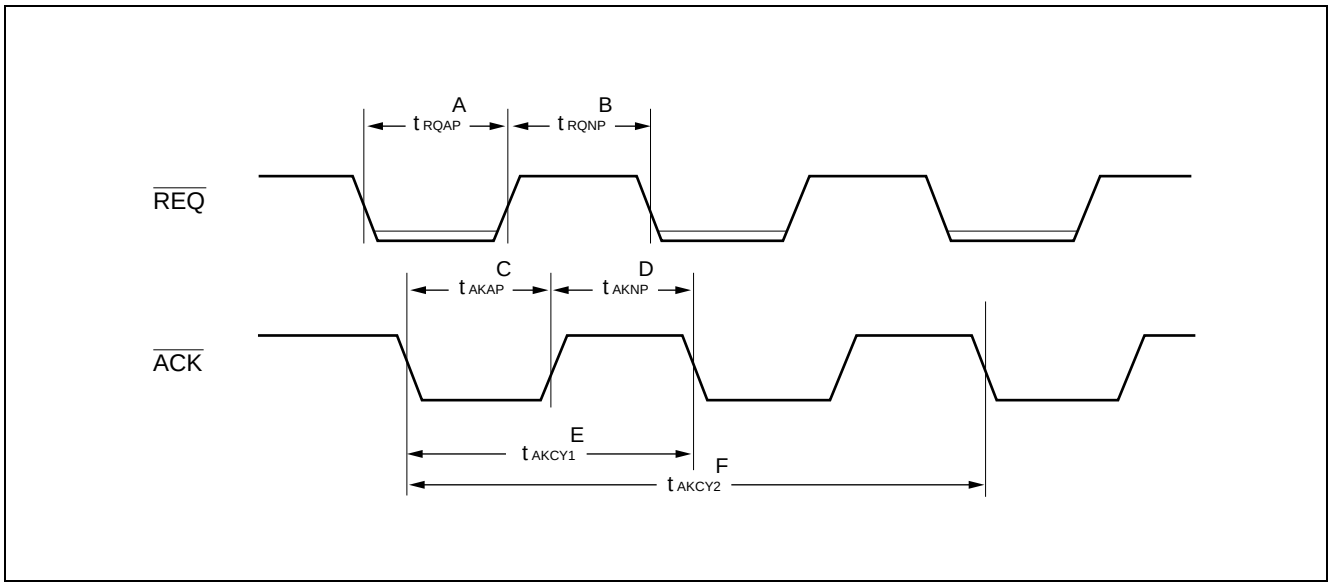
*: The $\overline{ACK}$ "L" → $\overline{REQ}$ "L" time (t_{AKRQ2}) is defined by either longer of (t_{AKRQH} + t_{RQAKH} + t_{AKRQ1}) or (t_{hDB} + t_{DBRQ}).

- **Synchronous transfer mode**

(a) $\overline{REQ}$/$\overline{ACK}$ signal period

Parameter	Symbol	Value			Unit
		Position*1	Min.	Max.	
$\overline{REQ}$ assert time *2	t_{RQAP}	A	A • t_{CLK} – 12	—	ns
$\overline{REQ}$ negate time *2	t_{RQNP}	B	N • t_{CLK} + 2	—	ns
$\overline{ACK}$ assert time	t_{AKAP}	C	20	—	ns
$\overline{ACK}$ negate time	t_{AKNP}	D	20	—	ns
$\overline{ACK}$ input cycle time 1	t_{AKCY1}	E	1 t_{CLK}	—	ns
$\overline{ACK}$ input cycle time 2	t_{AKCY2}	F	3 t_{CLK}	—	ns

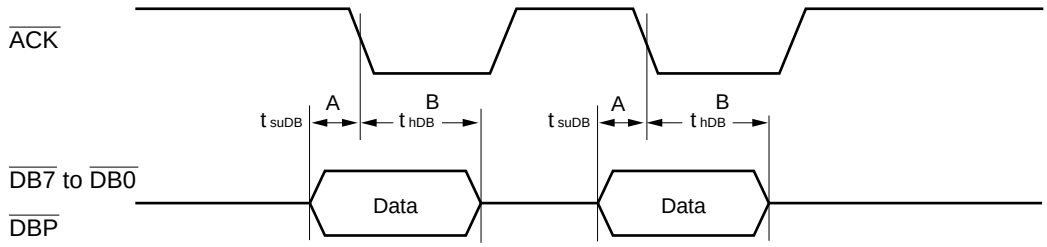
*1: The position number indicates the position in the waveform.
*2: “A” and “N” values are based on the transfer period register (address 0Dh). See (8) for more setting values.



(b) Input timing (initiator → target)

Parameter	Base signal	Symbol	Position*	Value Min.	Value Max.	Unit
Input data set up time	$\overline{ACK}$ "L"	t_{suDB}	A	5	—	ns
Input data hold time	$\overline{ACK}$ "L"	t_{hDB}	B	15	—	ns

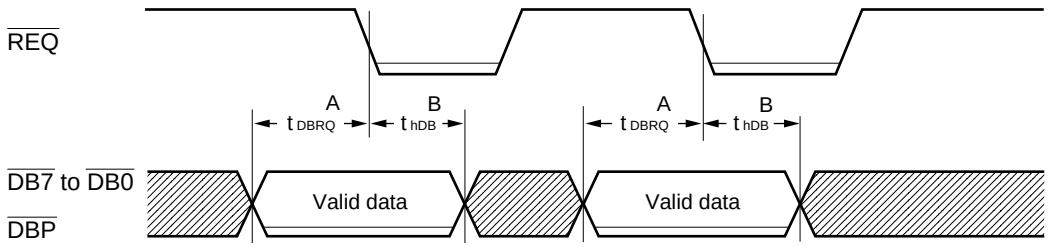
* : The position number indicates the position in the waveform.



(c) Output timing (target → initiator)

Parameter	Base signal	Symbol	Position*1	Value Min.	Value Max.	Unit
Time from output data valid to REQ "L" assert *2	—	t_{DBRQ}	A	N • t_{CLK} + 2	—	ns
Output data hold time *2	$\overline{REQ}$ "L"	t_{hDB}	B	A • t_{CLK} – 12	—	ns

*1: The position number indicates the position in the waveform.
*2: "A" and "N" values are based on the transfer period register (address 0Dh). See (8) for more setting values.



(8) A/N/S values in the SCSI interface timing specification

- **Transfer period register (address 0Dh) and A/N values**

Transfer period register					A	N	Transfer period register					A	N
Bit 4	Bit 3	Bit 2	Bit 1	Bit 0			Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
0	0	0	0	1	Prohibit	Prohibit	1	0	0	0	1	9	8
0	0	0	1	0	1	1	1	0	0	1	0	9	9
0	0	0	1	1	2	1	1	0	0	1	1	10	9
0	0	1	0	0	2	2	1	0	1	0	0	10	10
0	0	1	0	1	3	2	1	0	1	0	1	11	10
0	0	1	1	0	3	3	1	0	1	1	0	11	11
0	0	1	1	1	4	3	1	0	1	1	1	12	11
0	1	0	0	0	4	4	1	1	0	0	0	12	12
0	1	0	0	1	5	4	1	1	0	0	1	13	12
0	1	0	1	0	5	5	1	1	0	1	0	13	13
0	1	0	1	1	6	5	1	1	0	1	1	14	13
0	1	1	0	0	6	6	1	1	1	0	0	14	14
0	1	1	0	1	7	6	1	1	1	0	1	15	14
0	1	1	1	0	7	7	1	1	1	1	0	15	15
0	1	1	1	1	8	7	1	1	1	1	1	16	15
1	0	0	0	0	8	8	0	0	0	0	0	16	16

Note: The A and N values set in the register are the assert period and the negate period respectively (unit is clock cycles)
For the AC characteristics, A/N use numerals.

- **Asynchronous setup time register (address 17h) setting and the S value.**

Asynchronous setup time register				S	Asynchronous setup time register				S
Bit 3	Bit 2	Bit 1	Bit 0		Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	1	1	1	0	0	1	9
0	0	1	0	2	1	0	1	0	10
0	0	1	1	3	1	0	1	1	11
0	1	0	0	4	1	1	0	0	12
0	1	0	1	5	1	1	0	1	13
0	1	1	0	6	1	1	1	0	14
0	1	1	1	7	1	1	1	1	15
1	0	0	0	8	0	0	0	0	16

Note: The S (setup time) value established in the set up time register during asynchronous data transfers indicates the time from setting data in the data bus until the $\overline{REQ}$/$\overline{ACK}$ signals are asserted.
For the AC characteristics, S uses numerals.

■ LIST OF REGISTERS

1. BASIC Control Registers (for write)

Address						Register name	Bit assignment							
Hex.	A4	A3	A2	A1	A0		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	Output data register (first)	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
01	0	0	0	0	1	Output data register (second)	DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8
02	0	0	0	1	0	Direct control register	DC7	0	0	DO4	0	0	0	0
03	0	0	0	1	1	(Reserved)	0	0	0	0	0	0	0	0
04	0	0	1	0	0	SEL/RESEL ID register	SI7	0	0	0	0	SI2	SI1	SI0
05	0	0	1	0	1	Command register	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
06	0	0	1	1	0	Data block register (MSB)	BL15	BL14	BL13	BL12	BL11	BL10	BL9	BL8
07	0	0	1	1	1	Data block register (LSB)	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
08	0	1	0	0	0	Data byte register (MSB)	BY23	BY22	BY21	BY20	BY19	BY18	BY17	BY16
09	0	1	0	0	1	Data byte register	BY15	BY14	BY13	BY12	BY11	BY10	BY9	BY8
0A	0	1	0	1	0	Data byte register (LSB) MC byte register	BY7	BY6	BY5	BY4	BY3	BY2	BY1	BY0
0B	0	1	0	1	1	Diagnostic control register	DG7	DG6	DG5	0	DG3	DG2	DG1	DG0
0C	0	1	1	0	0	Transfer mode register	TM7	0	0	0	0	0	0	0
0D	0	1	1	0	1	Transfer period register	0	0	0	TP4	TP3	TP2	TP1	TP0
0E	0	1	1	1	0	Transfer offset register	0	0	0	TO4	TO3	TO2	TO1	TO0
0F	0	1	1	1	1	Window address register	WA7	WA6	0	0	WA3	WA2	WA1	WA0

2. BASIC Control Registers (for read)

Address						Register name	Bit assignment							
Hex.	A4	A3	A2	A1	A0		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	Input data register (first)	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
01	0	0	0	0	1	Input data register (second)	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
02	0	0	0	1	0	SPC status register	SS7	SS6	SS5	SS4	X	SS2	SS1	SS0
03	0	0	0	1	1	Nexus status register	NS7	NS6	NS5	X	X	NS2	NS1	NS0
04	0	0	1	0	0	Interrupt status register	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
05	0	0	1	0	1	Command step register	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0
06	0	0	1	1	0	Data block register (MSB)	BL15	BL14	BL13	BL12	BL11	BL10	BL9	BL8
07	0	0	1	1	1	Data block register (LSB)	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
08	0	1	0	0	0	Data byte register (MSB)	BY23	BY22	BY21	BY20	BY19	BY18	BY17	BY16
09	0	1	0	0	1	Data byte register	BY15	BY14	BY13	BY12	BY11	BY10	BY9	BY8
0A	0	1	0	1	0	Data byte register (LSB) MC byte register	BY7	BY6	BY5	BY4	BY3	BY2	BY1	BY0
0B	0	1	0	1	1	SCSI control signal status register	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
0C	0	1	1	0	0	Transfer mode register	TM7	X	X	X	X	X	X	X
0D	0	1	1	0	1	Transfer period register	X	X	X	TP4	TP3	TP2	TP1	TP0
0E	0	1	1	1	0	Transfer offset register	X	X	X	TO4	TO3	TO2	TO1	TO0
0F	0	1	1	1	1	Modified byte register	X	X	MB5	BM4	MB3	MB2	MB1	MB0

Note: X indicates data is undefined. (0 or 1).

3. Initial Setting Window (for read/write)

Address						Register name	Bit assignment							
Hex.	A4	A3	A2	A1	A0		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10	1	0	0	0	0	Clock conversion setting	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
11	1	0	0	0	1	Self ID setting	0	0	0	0	0	OI2	OI1	OI0
12	1	0	0	1	0	Response mode setting	AM7	AM6	AM5	AM4	0	0	AM1	AM0
13	1	0	0	1	1	Selection/reselection mode setting	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0
14	1	0	1	0	0	Selection/reselection retry setting	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
15	1	0	1	0	1	Selection/reselection timeout setting	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
16	1	0	1	1	0	REQ/ACK timeout setting	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0
17	1	0	1	1	1	Asynchronous setup time setting	0	0	0	0	AT3	AT2	AT1	AT0
18	1	1	0	0	0	Parity error detection setting	PE7	PE6	PE5	PE4	PE3	0	PE1	PE0
19	1	1	0	0	1	Interrupt enable setting	IE7	0	IE5	IE4	IE3	IE2	IE1	IE0
1A	1	1	0	1	0	Group 6/7 command length setting	GL7	GL6	GL5	GL4	GL3	GL2	GL1	GL0
1B	1	1	0	1	1	DMA system setting	0	0	DM5	MD4	0	0	0	0
1C	1	1	1	0	0	Automatic operation mode setting	OM7	OM6	OM5	OM4	OM3	OM2	OM1	OM0
1D	1	1	1	0	1	SPC Timeout setting	TO7	TO6	TO5	TO4	TO3	TO2	TO1	TO0
1F	1	1	1	1	1	Device revision indication	RV7	RV6	RV5	RV4	RV3	RV2	RV1	RV0

4. MCS Buffer Window

Address						For write	For read
Hex.	A4	A3	A2	A1	A0		
10	1	0	0	0	0	SEND MCS buffer	RECEIVE MCS buffer
11	1	0	0	0	1	SEND MCS buffer	RECEIVE MCS buffer
12	1	0	0	1	0	SEND MCS buffer	RECEIVE MCS buffer
13	1	0	0	1	1	SEND MCS buffer	RECEIVE MCS buffer
14	1	0	1	0	0	SEND MCS buffer	RECEIVE MCS buffer
15	1	0	1	0	1	SEND MCS buffer	RECEIVE MCS buffer
16	1	0	1	1	0	SEND MCS buffer	RECEIVE MCS buffer
17	1	0	1	1	1	SEND MCS buffer	RECEIVE MCS buffer
18	1	1	0	0	0	SEND MCS buffer	RECEIVE MCS buffer
19	1	1	0	0	1	SEND MCS buffer	RECEIVE MCS buffer
1A	1	1	0	1	0	SEND MCS buffer	RECEIVE MCS buffer
1B	1	1	0	1	1	SEND MCS buffer	RECEIVE MCS buffer
1C	1	1	1	0	0	SEND MCS buffer	RECEIVE MCS buffer
1D	1	1	1	0	1	SEND MCS buffer	RECEIVE MCS buffer
1E	1	1	1	1	0	SEND MCS buffer	RECEIVE MCS buffer
1F	1	1	1	1	1	SEND MCS buffer	RECEIVE MCS buffer

5. User Program Memory Window

Address						For write	For read
Hex.	A4	A3	A2	A1	A0		
10	1	0	0	0	0	User program memory	User program memory
11	1	0	0	0	1	User program memory	User program memory
12	1	0	0	1	0	User program memory	User program memory
13	1	0	0	1	1	User program memory	User program memory
14	1	0	1	0	0	User program memory	User program memory
15	1	0	1	0	1	User program memory	User program memory
16	1	0	1	1	0	User program memory	User program memory
17	1	0	1	1	1	User program memory	User program memory
18	1	1	0	0	0	User program memory	User program memory
19	1	1	0	0	1	User program memory	User program memory
1A	1	1	0	1	0	User program memory	User program memory
1B	1	1	0	1	1	User program memory	User program memory
1C	1	1	1	0	0	User program memory	User program memory
1D	1	1	1	0	1	User program memory	User program memory
IE	1	1	1	1	0	User program memory	User program memory
1F	1	1	1	1	1	User program memory	User program memory

■ LIST OF COMMANDS

SPC commands can be specified in the command register or the user program memory and divided into the following main groups.

- Sequential commands
  Commands that perform a consecutive (including phase transitions) sequence operation. Can only be specified in the command register (1-byte).
- Discrete commands
  Commands which perform operations from disassembled sequential commands. Can be specified in the command register (1-byte command) or the user program memory (1/2-byte command).
- Special commands
  Can only be specified in the user program memory (1/2-byte command).

1. Initiator Commands

(1) Sequential commands

No	Command code									Operand (for program)	Command name
1	00H	0	0	0	0	0	0	0	0	(not possible)	Select & CMD
2	01H	0	0	0	0	0	0	0	1	(not possible)	Select & 1-MSG & CMD
3	02H	0	0	0	0	0	0	1	0	(not possible)	Select & N-Byte-MSG & CMD
4	03H	0	0	0	0	0	0	1	1	(not possible)	Select & 1-MSG
5	04H	0	0	0	0	0	1	0	0	(not possible)	Select & N-Byte-MSG
6	05H	0	0	0	0	0	1	0	1	(not possible)	Send N-Byte-MSG
7	06H	0	0	0	0	0	1	1	0	(not possible)	Send N-Byte-CMD
8	07H	0	0	0	0	0	1	1	1	(not possible)	Receive N-Byte-MSG

(2) Discrete commands

No	Command code									Operand (for program)	Command name
9	08H	0	0	0	0	1	0	0	0	—	Select
10	09H	0	0	0	0	1	0	0	1	—	Select with ATN
11	0AH	0	0	0	0	1	0	1	0	—	Set ATN
12	0BH	0	0	0	0	1	0	1	1	—	Reset ATN
13	0CH	0	0	0	0	1	1	0	0	—	Set ACK
14	0DH	0	0	0	0	1	1	0	1	—	Reset ACK
15	10H	0	0	0	1	0	0	0	0	—	Send Data from MPU
16	11H	0	0	0	1	0	0	0	1	—	Send Data from DMA
17	12H	0	0	0	1	0	0	1	0	—	Receive Data to MPU
18	13H	0	0	0	1	0	0	1	1	—	Receive Data to DMA
19	14H	0	0	0	1	0	1	0	0	—	Send DATA from MPU Padding
20	15H	0	0	0	1	0	1	0	1	—	Send DATA from DMA Padding
21	16H	0	0	0	1	0	1	1	0	—	Receive Data to MPU Padding
22	17H	0	0	0	1	0	1	1	1	—	Receive Data to DMA Padding
23	18H	0	0	0	1	1	0	0	0	Address of MSG sent	Send 1-MSG
24	19H	0	0	0	1	1	0	0	1	Address of MSG sent	Send 1-MSG with ATN
25	1AH	0	0	0	1	1	0	1	0	SAVE address of MSG	Receive MSG
26	1BH	0	0	0	1	1	0	1	1	Address of CMD sent	Send CMD
27	1CH	0	0	0	1	1	1	0	0	SAVE address of STATUS	Receive STATUS

2. Target Commands

(1) Sequential commands

No	Command code									Operand (for program)	Command name
1	20H	0	0	1	0	0	0	0	0	(not possible)	Reselect & 1-MSG
2	21H	0	0	1	0	0	0	0	1	(not possible)	Reselect & N-Byte-MSG
3	22H	0	0	1	0	0	0	1	0	(not possible)	Reselect & 1-MSG & Terminate
4	23H	0	0	1	0	0	0	1	1	(not possible)	Reselect & 1-MSG & Link-Terminate
5	24H	0	0	1	0	0	1	0	0	(not possible)	Terminate
6	25H	0	0	1	0	0	1	0	1	(not possible)	Link-Terminate
7	26H	0	0	1	0	0	1	1	0	(not possible)	Disconnect-Sequence
8	27H	0	0	1	0	0	1	1	1	(not possible)	Send N-Byte-MSG
9	28H	0	0	1	0	1	0	0	0	(not possible)	Receive N-Byte-CMD
10	29H	0	0	1	0	1	0	0	1	(not possible)	Receive N-Byte-MSG
11	2AH	0	0	1	0	1	0	1	0	(not possible)	Reselect & N-Byte-MSG & Terminate
12	2BH	0	0	1	0	1	0	1	1	(not possible)	Reselect & N-Byte-MSG & Link-Terminate
13	2CH	0	0	1	0	1	1	0	0	(not possible)	Disconnect-Sequence 2

(2) Discrete commands

No	Command code									Operand (for program)	Command name
14	30H	0	0	1	1	0	0	0	0	—	Reselect
15	31H	0	0	1	1	0	0	0	1	—	Set REQ
16	32H	0	0	1	1	0	0	1	0	—	Reset REQ
17	33H	0	0	1	1	0	0	1	1	—	Disconnect
18	34H	0	0	1	1	0	1	0	0	—	Send Data from MPU
19	35H	0	0	1	1	0	1	0	1	—	Send Data from DMA
20	36H	0	0	1	1	0	1	1	0	—	Receive Data to MPU
21	37H	0	0	1	1	0	1	1	1	—	Receive Data to DMA
22	38H	0	0	1	1	1	0	0	0	Address of MSG sent	Send 1 MSG
23	39H	0	0	1	1	1	0	0	1	SAVE address of MSG	Receive MSG
24	3AH	0	0	1	1	1	0	1	0	Send-status address	Send Status
25	3BH	0	0	1	1	1	0	1	1	SAVE address of CDB	Receive CMD

3. Common Commands

No	Command code									Operand (for program)	Command name
1	40H	0	1	0	0	0	0	0	0	(not possible)	SOFTWARE RESET
2	41H	0	1	0	0	0	0	0	1	(not possible)	TRANSFER RESET
3	42H	0	1	0	0	0	0	1	0	(not possible)	SCSI RESET
4	43H	0	1	0	0	0	0	1	1	(not possible)	SET UP REG
5	44H	0	1	0	0	0	1	0	0	(not possible)	INIT DIAG START
6	45H	0	1	0	0	0	1	0	1	(not possible)	TARG DIAG START
7	46H	0	1	0	0	0	1	1	0	(not possible)	DIAG END
8	47H	0	1	0	0	0	1	1	1	(not possible)	COMMAND PAUSE
9	48H	0	1	0	0	1	0	0	0	(not possible)	SET RST
10	49H	0	1	0	0	1	0	0	1	(not possible)	RESET RST

4. Programmable Commands

The user program is stored in the user program memory and begins operation when the user program head address is written in the command register.

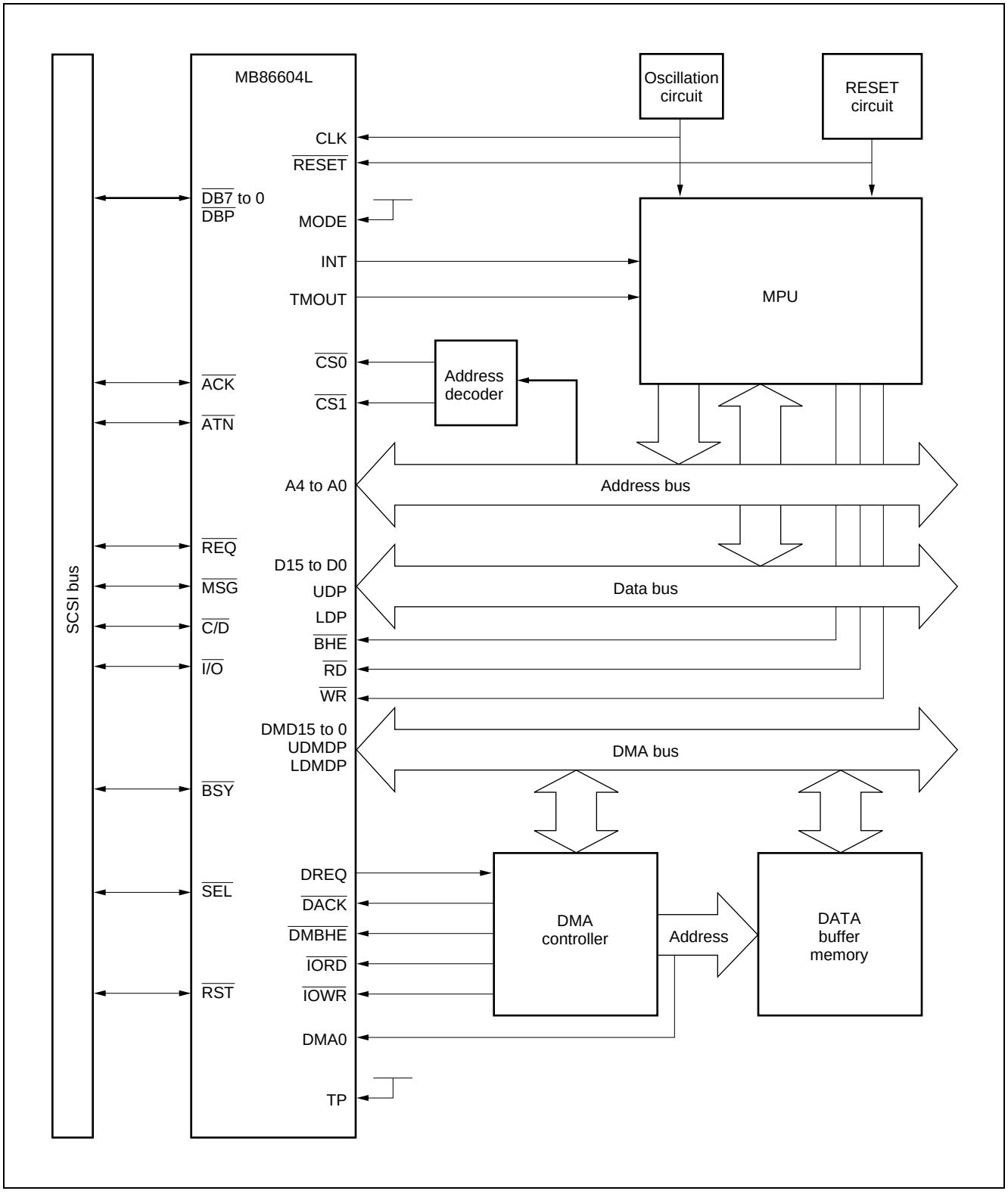
Programmable commands are composed of discrete and special commands and have a command length of one (1) or two (2) bytes.

- **Command field assign**

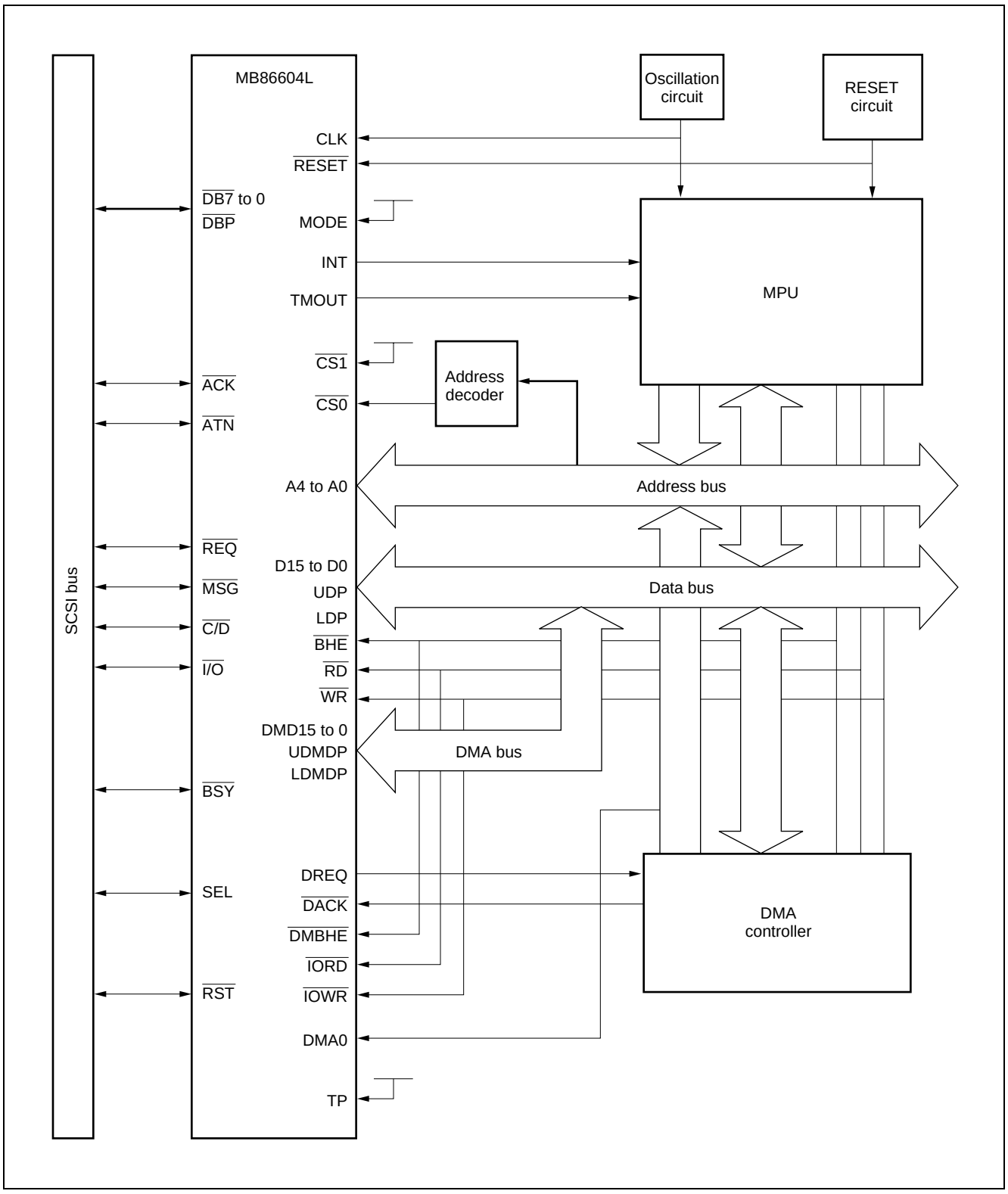
Command type	Command code (1st byte)	Operand (2nd byte)
Discrete commands	Message, command, or status phases send command	Memory address of the data to be sent.
	Message, command, or status phases receive command	Memory address of received data being stored.
	Data phase receive/send command or do not perform transfer command	—
Special commands	AND command	Data for AND operation or memory address of data for AND operation.
	TEST AND command	Data for AND operation or memory address of data for AND operation.
	COMPARE command	Data for COMPARE operation or memory address of data for COMPARE operation.
	Conditional branch command	Jump head address
	MOVE command	Memory address to be moved.
	STOP command	User status code
	NOP command	—

■ SYSTEM CONFIGURATION EXAMPLE

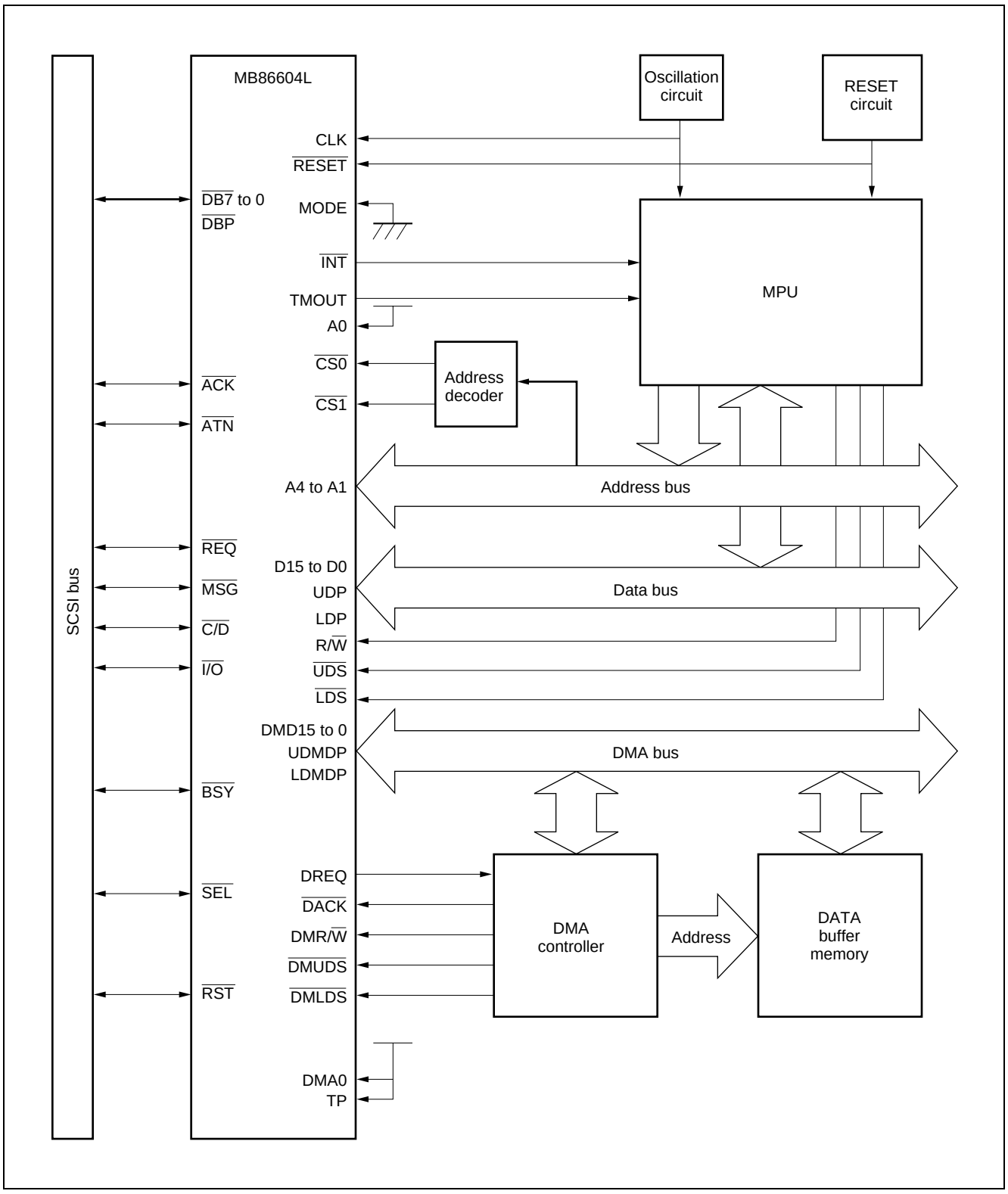
1. 80-Series, Separate Bus Type



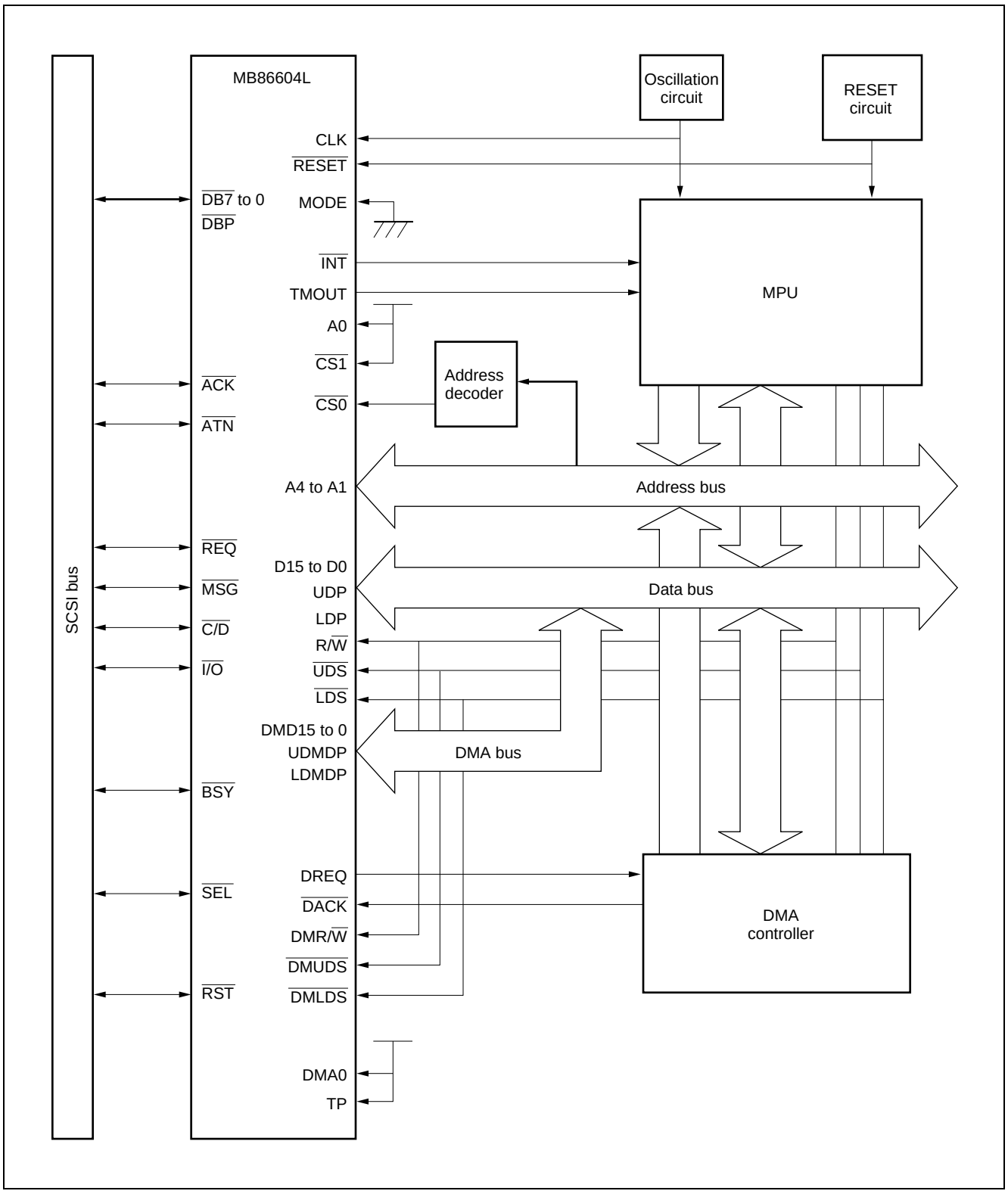
2. 80-Series, Common Bus Type



3. 68-Series, Separate Bus Type



4. 68-Series, Common Bus Type

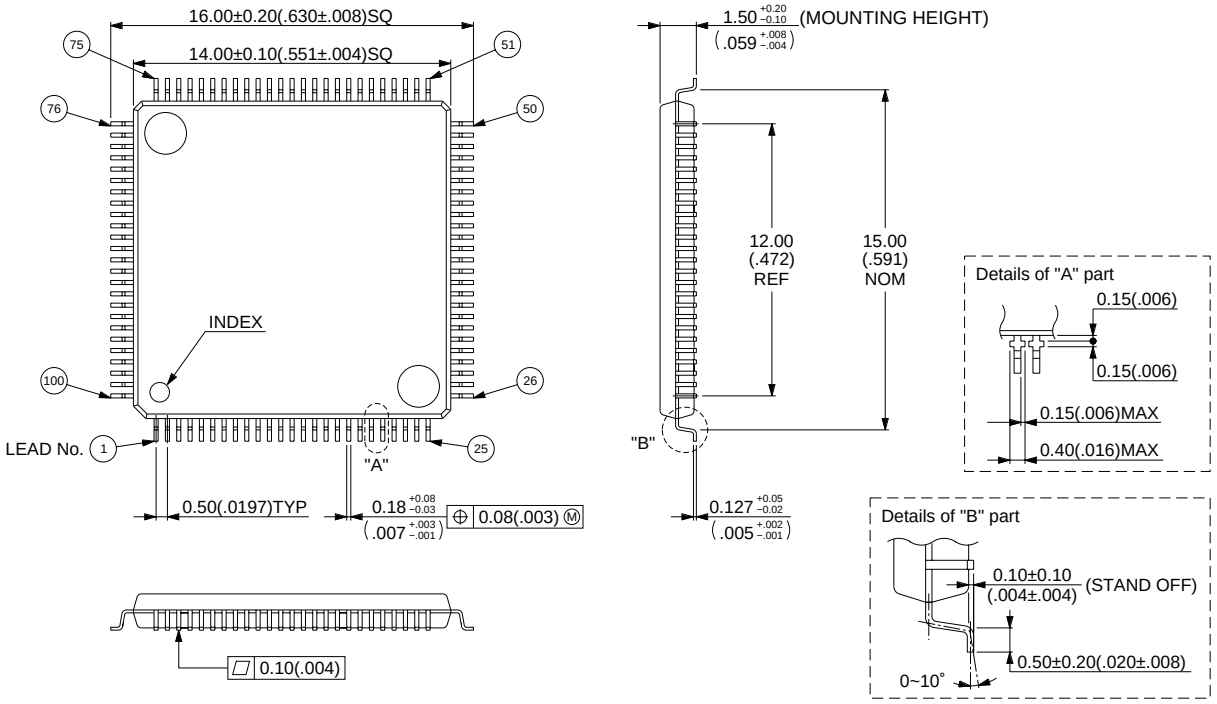


■ ORDERING INFORMATION

Part number	Package	Remarks
MB86604LPFV	100 pin Plastic LQFP (FPT-100P-M05)	

■ PACKAGE DIMENSION

100-pin Plastic LQFP
(FPT-100P-M05)



Dimensions in mm (inches)

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