FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21364-3E

ASSP

Dual Serial Input PLL Frequency Synthesizer

MB15F78SP

■ DESCRIPTION

The Fujitsu MB15F78SP is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 2550 MHz prescaler and a 1200 MHz prescaler. A 32/33 or a 64/65 for the 2550 MHz prescaler, and a 16/17 or a 32/33 for the 1200 MHz prescaler can be selected for the prescaler that enables pulse swallow operation.
The BiCMOS process is used , as a result a supply current is typically 5.5 mA at 2.7 V. The supply voltage range is from 2.4 V to 3.6 V. A refined charge pump supplies well-balanced output current with 1.5 mA and 6 mA selectable by serial data.
The new package (BCC20) decreases an area of MB15F78SP more than 30 % comparing with the former BCC16 (for dual PLL).
MB15F78SP is ideally suited for wireless mobile communications, such as GSM.

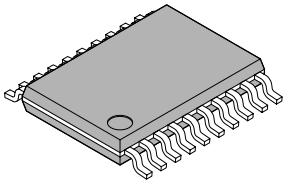
■ FEATURES

- High frequency operatio : RX synthesizer : 2550 MHz max
  : TX synthesizer : 1200 MHz max
- Low power supply voltage : V_{CC} = 2.4 to 3.6 V
- Ultra Low power supply current : I_{CC} = 5.5 mA typ.
  (V_{CC} = Vp = 2.7 V, Ta = +25°C, SW_{TX} = SW_{RX} = 0, in TX/RX locking state)
- Direct power saving function : Power supply current in power saving mode
  Typ. 0.1 µA (V_{CC} = Vp = 2.7 V, Ta = +25°C), Max. 10 µA (V_{CC} = Vp = 2.7 V)
- Software selectable charge pump current: 1.5 mA/6.0 mA typ.

(Continued)

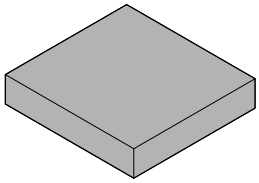
■ PACKAGES

20-pin plastic TSSOP



(FPT-20P-M06)

20-pad plastic BCC



(LCC-20P-M04)

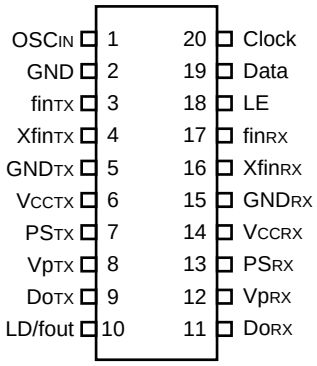
MB15F78SP

(Continued)

- Dual modulus prescaler : 2550 MHz prescaler (32/33 or 64/65)/1200 MHz prescaler (16/17 or 32/33)
- 23-bit shift register
- Serial input binary 14-bit programmable reference divider : R = 3 to 16,383
- Serial input programmable divider consisting of:
  - Binary 7-bit swallow counter : 0 to 127
  - Binary 11-bit programmable counter: 3 to 2,047
- Built-in high-speed tuning, low-noise phase comparator, current-switching type constant current circuit
- On–chip phase control for phase comparator
- Built-in digital locking detector circuit to detect PLL locking and unlocking
- Operating temperature : Ta = –40 to +85°C
- Sireal data format compatible with MB15F08SL

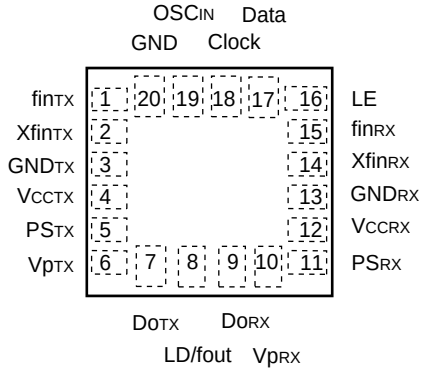
■ PIN ASSIGNMENTS

(TSSOP-20)
TOP VIEW



(FPT-20P-M06)

(BCC-20)
TOP VIEW



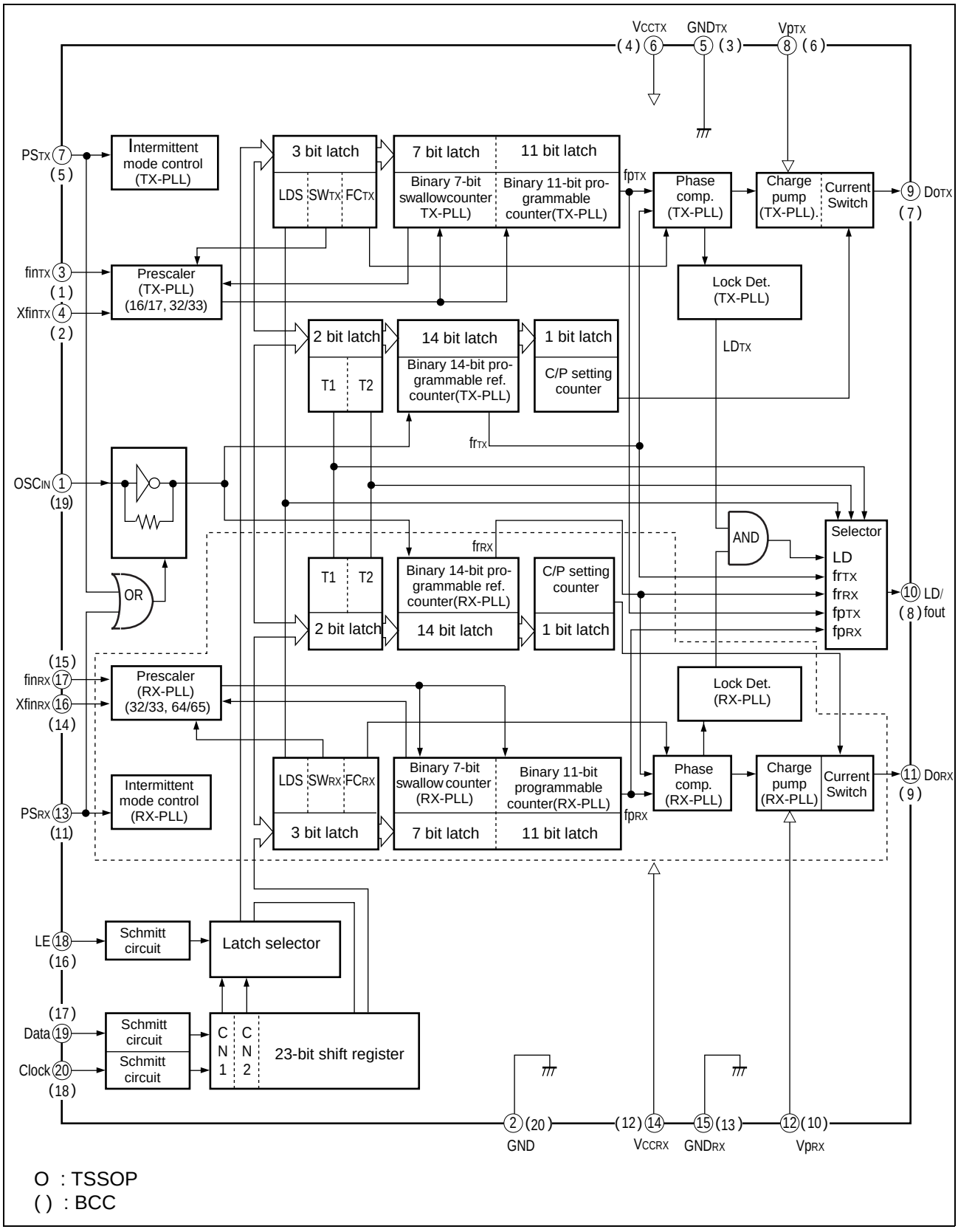
(LCC-20P-M04)

■ PIN DESCRIPTION

Pin no.		Pin name	I/O	Descriptions
TSSOP	BCC			
1	19	OSC_{IN}	I	The programmable reference divider input. TCX0 should be connected with a AC coupling capacitor.
2	20	GND	—	Ground for OSC input buffer and the shift register circuit.
3	1	fin_{TX}	I	Prescaler input pin for the TX-PLL. Connection to an external VCO should be via AC coupling.
4	2	$Xfin_{TX}$	I	Prescaler complimentary input pin for the TX-PLL section. This pin should be grounded via a capacitor.
5	3	GND_{TX}	—	Ground for the TX-PLL section.
6	4	V_{CCTX}	—	Power supply voltage input pin for the TX-PLL section(except for the charge pump circuit), the oscillator input buffer and the shift register.
7	5	PS_{TX}	I	Power saving mode control for the TX-PLL section. This pin must be set at “L” Power-ON. (Open is prohibited.) PS_{TX} = “H” ; Normal mode / PS_{TX} = “L” ; Power saving mode
8	6	Vp_{TX}	—	Power supply voltage input pin for the TX-PLL charge pump.
9	7	D_{OTX}	O	Charge pump output for the TX-PLL section.
10	8	LD/fout	O	Lock detect signal output (LD)/phase comparator monitoring output (fout).The output signal is selected by LDS bit in the serial data. LDS bit = “H” ; outputs fout signal / LDS bit = “L” ; outputs LD signal
11	9	D_{ORX}	O	Charge pump output for the RX-PLL section.
12	10	Vp_{RX}	—	Power supply voltage input pin for the RX-PLL charge pump.
13	11	PS_{RX}	I	Power saving mode control for the RX-PLL section. This pin must be set at “L” Power-ON. (Open is prohibited.) PS_{RX} = “H” ; Normal mode / PS_{RX} = “L” ; Power saving mode
14	12	V_{CCRX}	—	Power supply voltage input pin for the RX-PLL section(except for the charge pump circuit).
15	13	GND_{RX}	—	Ground for the RX-PLL section.
16	14	$Xfin_{RX}$	I	Prescaler complimentary input pin for the RX-PLL section. This pin should be grounded via a capacitor.
17	15	fin_{RX}	I	Prescaler input pin for the RX-PLL. Connection to an external VCO should be via AC coupling.
18	16	LE	I	Load enable signal input(with the schmitt trigger circuit). When LE is set “H”, data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
19	17	Data	I	Serial data input(with the schmitt trigger circuit). A data is transferred to the corresponding latch(TX-ref. counter, TX-prog. counter, RX-ref.counter, RX-prog.counter) according to the control bit in a serial data.
20	18	Clock	I	Clock input for the 23-bit shift register (with a schmitt trigger circuit). One bit of data is shifted into the shift register on a rising edge of the clock.

MB15F78SP

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating		Unit
			Min.	Max.	
Power supply voltage		V_{CC}	–0.5	4.0	V
		Vp	V_{CC}	4.0	V
Input voltage		V_I	–0.5	V_{CC} + 0.5	V
Output voltage	LD/fout	V_O	GND	V_{CC}	V
	Do_{TX}, Do_{RX}	V_{DD}	GND	Vp	V
Storage temperature		Tstg	–55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{CC}	2.4	2.7	3.6	V
	Vp	V_{CC}	2.7	3.6	V
Input voltage	V_I	GND	—	V_{CC}	V
Operating temperature	Ta	–40	—	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.4 V to 3.6 V, Ta = –40 °C to +85 °C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current		I_{CCTX} *1	TX PLL	—	2.2	—	mA
		I_{CCRX} *2	RX PLL	—	3.3	—	mA
Power saving current		I_{PSTX}	PS_{TX} = PS_{RX} = "L"	—	0.1 *8	10	µA
		I_{PSRX}	PS_{TX} = PS_{RX} = "L"	—	0.1 *8	10	µA
Operating frequency	fin_{TX} *3	fin_{TX}	TX PLL	50	—	1200	MHz
	fin_{RX} *3	fin_{RX}	RX PLL	400	—	2550*9	MHz
	OSC_{IN}	f_{OSC}	—	3	—	40	MHz
Input sensitivity	fin_{TX}	$Pfin_{TX}$	TX PLL, 50 Ω system	–15	—	+2	dBm
	fin_{RX}	$Pfin_{RX}$	RX PLL, 50 Ω system	–15 *9	—	+2	dBm
	OSC_{IN}	V_{OSC}	—	0.5	—	V_{CC}	V_{P-P}
"H" level input voltage	Data, LE, Clock	V_{IH}	Schmitt trigger input	0.7 V_{CC} + 0.4	—	—	V
"L" level input voltage		V_{IL}	Schmitt trigger input	—	—	0.3 V_{CC} – 0.4	V
"H" level input voltage	PS_{TX} PS_{RX}	V_{IH}	—	0.7 V_{CC}	—	—	V
"L" level input voltage		V_{IL}	—	—	—	0.3 V_{CC}	V
"H" level input current	Data LE Clock PS_{TX} PS_{RX}	I_{IH} *4	—	–1.0	—	+1.0	µA
"L" level input current		I_{IL} *4	—	–1.0	—	+1.0	µA
"H" level input current	OSC_{IN}	I_{IH}	—	0	—	+100	µA
"L" level input current		I_{IL} *4	—	–100	—	0	µA
"H" level output voltage	LD/fout	V_{OH}	V_{CC} = Vp = 2.7 V, I_{OH} = –1 mA	V_{CC} – 0.4	—	—	V
"L" level output voltage		V_{OL}	V_{CC} = Vp = 2.7 V, I_{OL} = 1 mA	—	—	0.4	V
"H" level output voltage	Do_{TX} Do_{RX}	V_{DOH}	V_{CC} = Vp = 2.7 V, I_{DOH} = –0.5 mA	Vp – 0.4	—	—	V
"L" level output voltage		V_{DOL}	V_{CC} = Vp = 2.7 V, I_{DOL} = 0.5 mA	—	—	0.4	V
High impedance cutoff current	Do_{TX} Do_{RX}	I_{OFF}	V_{CC} = Vp = 2.7 V V_{OFF} = 0.5 V to Vp – 0.5 V	—	—	2.5	nA
"H" level output current	LD/fout	I_{OH} *4	V_{CC} = Vp = 2.7 V	—	—	–1.0	mA
"L" level output current		I_{OL}	V_{CC} = Vp = 2.7 V	1.0	—	—	mA

(Continued)

(Continued)

(V_{CC} = 2.4 V to 3.6 V, Ta = –40 °C to +85 °C)

Parameter		Symbol	Condition		Value			Unit
					Min.	Typ.	Max.	
"H" level output current	DO_{TX} DO_{RX}	I_{DOH} *4	V_{CC} = Vp = 2.7 V, V_{DOH} = Vp/2, Ta = +25 °C	CS bit = "H"	—	–6.0	—	mA
				CS bit = "L"	—	–1.5	—	mA
"L" level output current	DO_{TX} DO_{RX}	I_{DOL}	V_{CC} = Vp = 2.7 V, V_{DOL} = Vp/2, Ta = +25 °C	CS bit = "H"	—	6.0	—	mA
				CS bit = "L"	—	1.5	—	mA
Charge pump current rate	I_{DOL}/I_{DOH}	I_{DOMT} *5	V_{DO} = Vp / 2		—	3	—	%
	vs V_{DO}	I_{DOVD} *6	0.5 V ≤ V_{DO} ≤ Vp – 0.5 V		—	10	—	%
	vs Ta	I_{DOTA} *7	–40 °C ≤ Ta ≤ +85 °C, V_{DO} = Vp / 2		—	10	—	%

*1 : fin_{TX} = 910 MHz, fosc = 12.8 MHz, V_{CCTX} = Vp_{TX} = 2.7 V, SW_{TX} = 0, Ta = +25 °C, in locking state.

*2 : fin_{RX} = 2500 MHz, fosc = 12.8 MHz, V_{CCRX} = Vp_{RX} = 2.7 V, SW_{RX} = 0, Ta = +25 °C, in locking state.

*3 : AC coupling. 1000 pF capacitor is connected under the condition of minimum operating frequency.

*4 : The symbol "–" (minus) means direction of current flow.

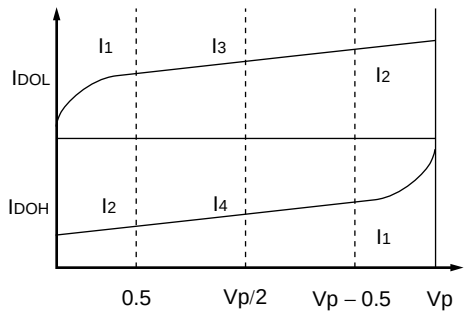
*5 : V_{CC} = Vp = 2.7 V, Ta = +25 °C
$(|I_3| - |I_4|) / [(|I_3| + |I_4|) / 2] \times 100$ (%)

*6 : V_{CC} = Vp = 2.7 V, Ta = +25 °C (Applied to each I_{DOL}, I_{DOH})
$[(|I_2| - |I_1|) / 2] / [(|I_1| + |I_2|) / 2] \times 100$ (%)

*7 : V_{CC} = Vp = 2.7 V, Ta = +25 °C (Applied to each I_{DOL}, I_{DOH})
$[|I_{DO\,(+85°C)}| - |I_{DO\,(-40\,°C)}| / 2] / [(|I_{DO\,(+85°C)}| + |I_{DO\,(-40°C)}|) / 2] \times 100$ (%)

*8 : fosc = 12.8 MHz, V_{CCRX} = Vp_{RX} = V_{CCTX} = Vp_{TX} = 2.7 V, Ta = +25°C

*9 : 2500 MHz to 2550 MHz, V_{CC} = 2.7 V to 3.6 V, Pfinmin = –10 dBm



Charge pump output voltage (V)

■ FUNCTIONAL DESCRIPTION

1. Pulse swallow function

$f_{VCO} = [(P \times N) + A] \times f_{OSC} \div R$

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
P : Preset divide ratio of dual modulus prescaler (16 or 32 for TX-PLL, 32 or 64 for RX-PLL)
N : Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A < N$)
f_{OSC} : Reference oscillation frequency (OSC_{IN} input frequency)
R : Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

2. Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of TX/RX-PLL sections, programmable reference dividers of TX/RX-PLL sections are controlled individually.
Serial data of binary data is entered through Data pin.
On rising edge of Clock, one bit of serial data is transferred into the shift register. On a rising edge of load enable signal, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

	The programmable reference counter for the TX-PLL	The programmable reference counter for the RX-PL	The programmable counter and the swallow counter for the TX-PLL	The programmable counter and the swallow counter for the RX-PLL
CN1	0	1	0	1
CN2	0	0	1	1

(1) Shift Register Configuration

• Programmable Reference Counter

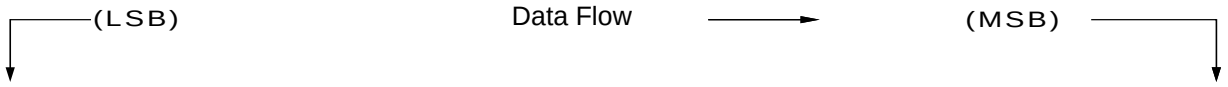
Data Flow (LSB) → (MSB)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	T1	T2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	CS	X	X	X	X

CS : Charge pump currnet select bit
R1 to R14 : Divide ratio setting bits for the programmable reference counter (3 to 16,383)
T1, 2 : Test purpose bit
CN1,2 : Control bit
X : Dummy bits (Set “0” or “1”)

Note : Data input with MSB first.

• Programmable Counter



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	LDS	SW	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127)
N1 to N11 : Divide ratio setting bits for the programmable counter (3 to 2,047)
LDS : LD/fout signal select bit
SW : Divide ratio setting bit for the prescaler
FC : Phase control bit for the phase detector
CN1, 2 : Control bit

Note : Data input with MSB first.

(2) Data setting

• Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 3 is prohibited.

• Binary 11-bit Programmable Counter Data Setting

Divide ratio	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 3 is prohibited.

• Binary 7-bit Swallow Counter Data Setting

Divide ratio	A7	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

MB15F78SP

• Prescaler Data Setting

Divide ratio	SW = "H"	SW = "L"
Prescaler divide ratio TX-PLL	16/17	32/33
Prescaler divide ratio RX-PLL	32/33	64/65

• Charge Pump Current Setting

Current value	CS
±6.0 mA	1
±1.5 mA	0

• LD/fout Output Select Data Setting

LD/fout output signal	LDS
fout signal	1
LD signal	0

• Test Purpose Bit Setting

LD/fout pin state	T1	T2
Outputs fr_{TX}.	0	0
Outputs fr_{RX}.	1	0
Outputs fp_{TX}.	0	1
Outputs fp_{RX}.	1	1

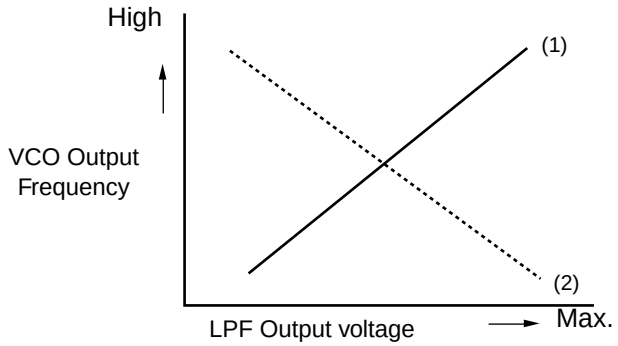
• Phase Comparator Phase Switching Data Setting

Phase comparator input	FC = "H"	FC = "L"
	DO_{TX}/DO_{RX}	DO_{TX}/DO_{RX}
fr > fp	H	L
fr < fp	L	H
fr = fp	Z	Z

Z : High-impedance

Depending upon the VCO and LPF polarity, FC bit should be set.

(1) VCO polarity FC = "H"
(2) VCO polarity FC = "L"



Note : Give attention to the polarity for using active type LPF.

3. Power Saving Mode (Intermittent Mode Control Circut)

Status	PS_{TX}/PS_{RX} pins
Normal mode	H
Power saving mode	L

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pins low, the device enters into the power saving mode, reducing the current consumption. See the Electrical Characteristics chart for the specific value.

The phase detector output, Do, becomes high impedance.

For the dual PLL, the lock detector, LD, is as shown in the LD Output Logic table.

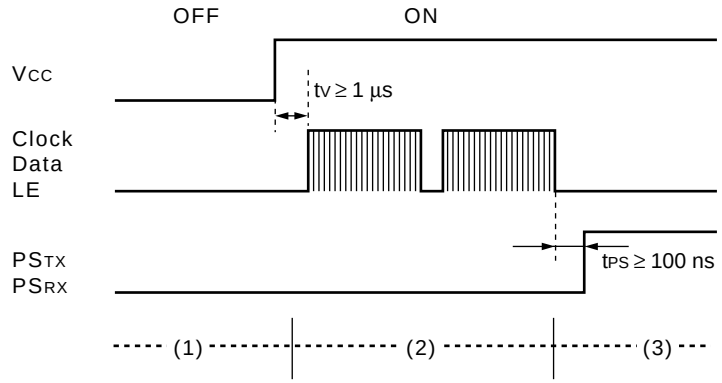
Setting the PS pins high, releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (fp) and the reference frequency (fr) which can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lockup time.

To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

Notes: •When power (V_{CC}) is first applied, the device must be in standby mode, PS_{TX} = PS_{RX} = Low, for at least 1 µs.

•PS pins must be set at “L” for Power-ON

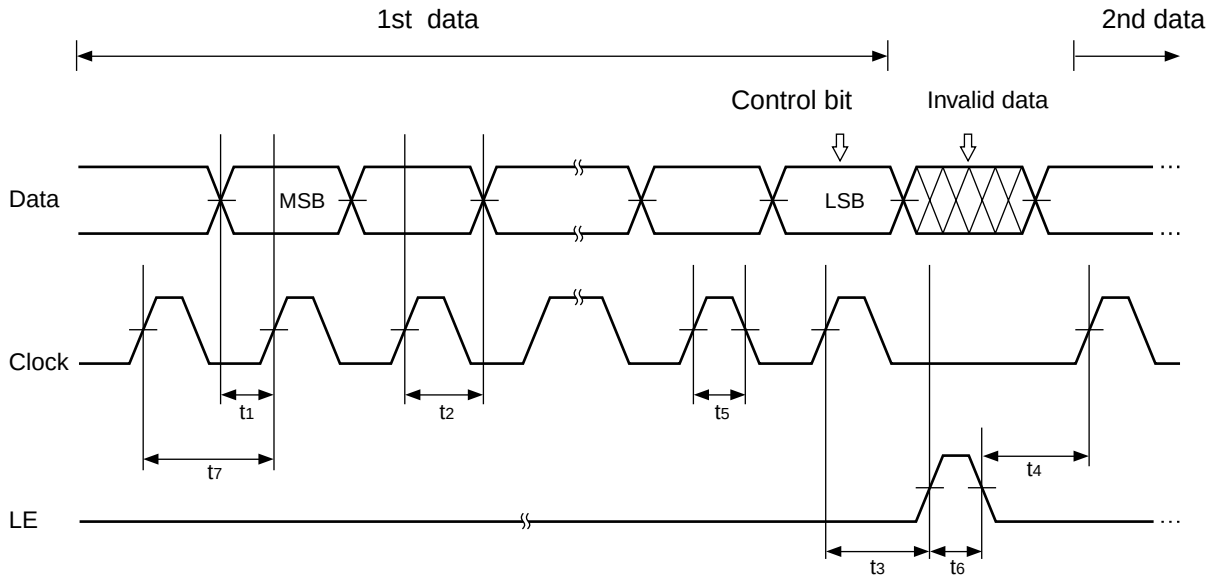


(1) PS_{TX} = PS_{RX} = “L” (power saving mode) at Power-ON
(2) Set serial data 1 µs later after power supply remains stable ($V_{CC} \geq 2.2$ V).
(3) Release power saving mode (PS_{TX}, PS_{RX} : “L” → “H”) 100 ns later after setting serial data.

4. Serial data input timing

Frequency multiplier setting is performed through a serial interface using the Data pin, Clock pin, and LE pin.

Setting data is read into the shift register at the rise of the clock signal, and transferred to a latch at the rise of the LE signal. The following diagram shows the data input timing.

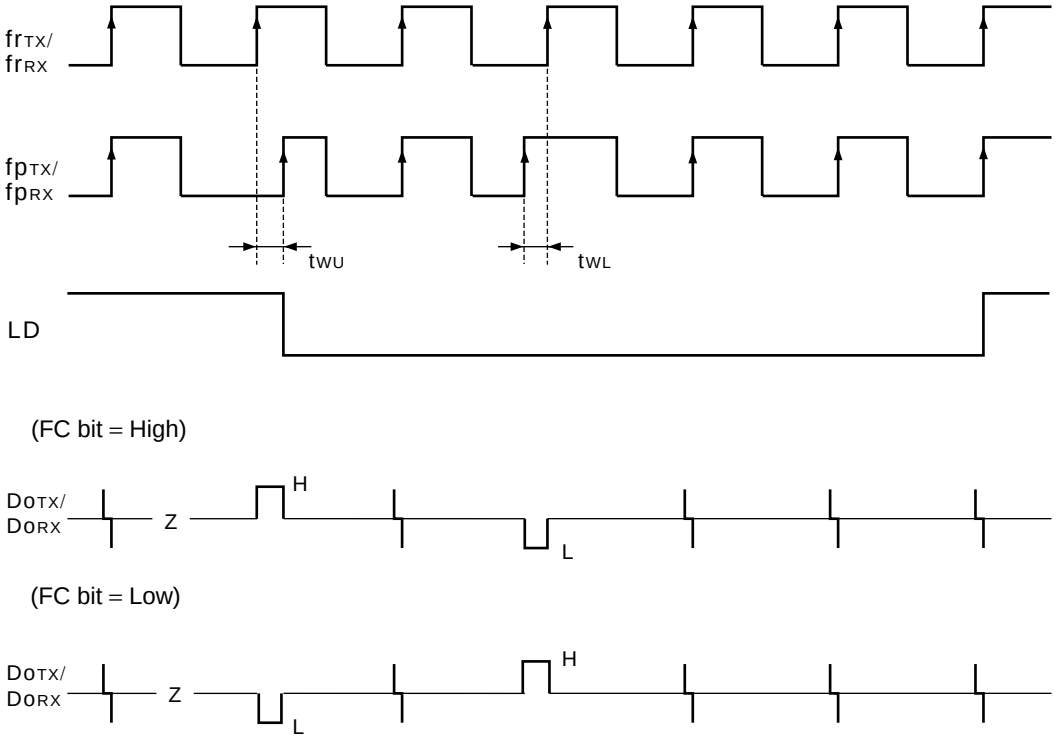


Parameter	Min.	Typ.	Max.	Unit
t_1	20	—	—	ns
t_2	20	—	—	ns
t_3	30	—	—	ns
t_4	20	—	—	ns

Parameter	Min.	Typ.	Max.	Unit
t_5	30	—	—	ns
t_6	100	—	—	ns
t_7	100	—	—	ns

Note : LE should be “L” when the data is transferred into the shift register.

■ PHASE COMPARATOR OUTPUT WAVEFORM



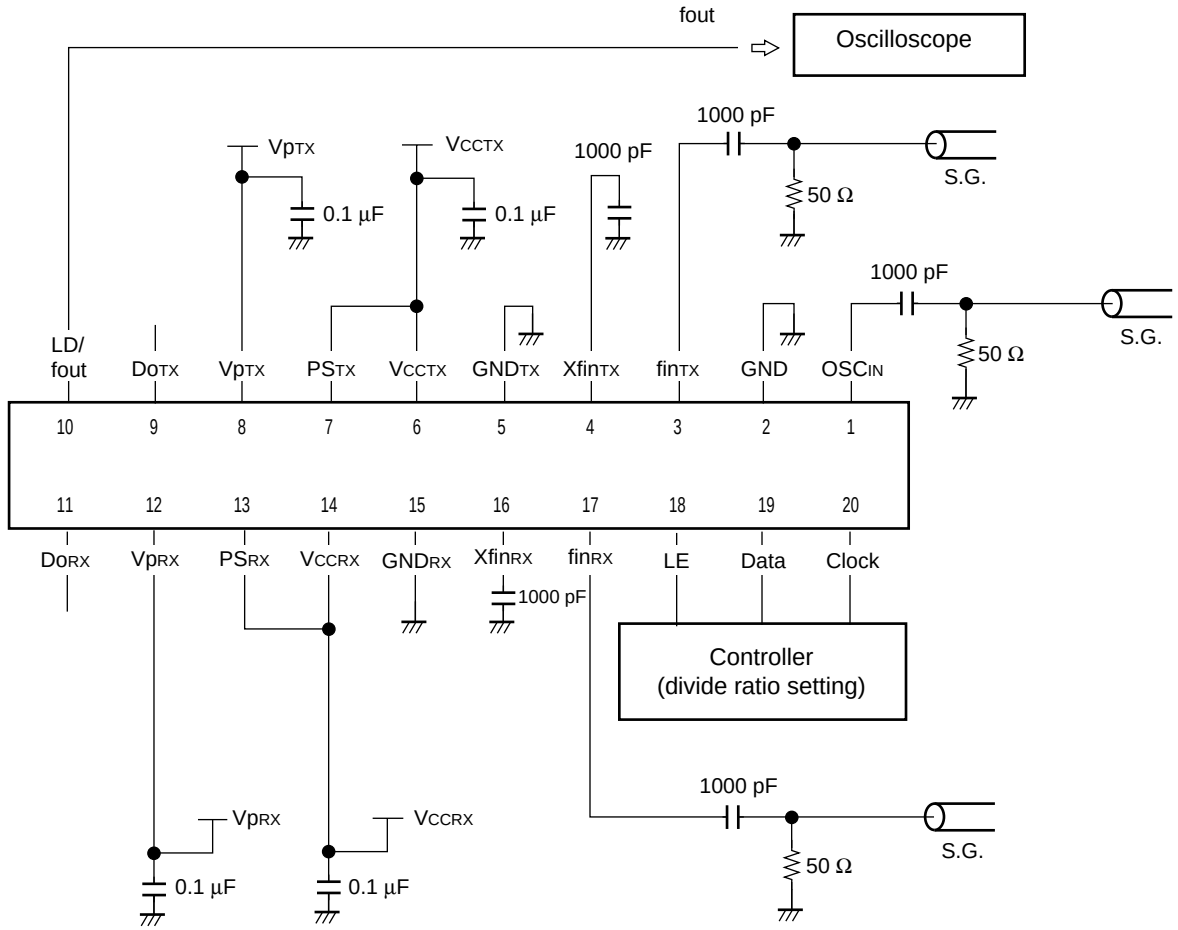
LD Output Logic Table

TX-PLL section	RX-PLL section	LD output
Locking state/Power saving state	Locking state/Power saving state	H
Locking state/Power saving state	Unlocking state	L
Unlocking state	Locking state/Power saving state	L
Unlocking state	Unlocking state	L

Notes:
- Phase error detection range = –2 π to + 2 π
- Pulses on Do_{TX}/Do_{RX} signals are output to prevent dead zone.
- LD output becomes low when phase error is t_{WU} or more.
- LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSC_{IN} input frequency as follows.
  $t_{WU} \geq 2/fosc$: e.g. $t_{WU} \geq 156.3$ ns when fosc = 12.8 MHz
  $t_{WU} \leq 4/fosc$: e.g. $t_{WL} \leq 312.5$ ns when fosc = 12.8 MHz

MB15F78SP

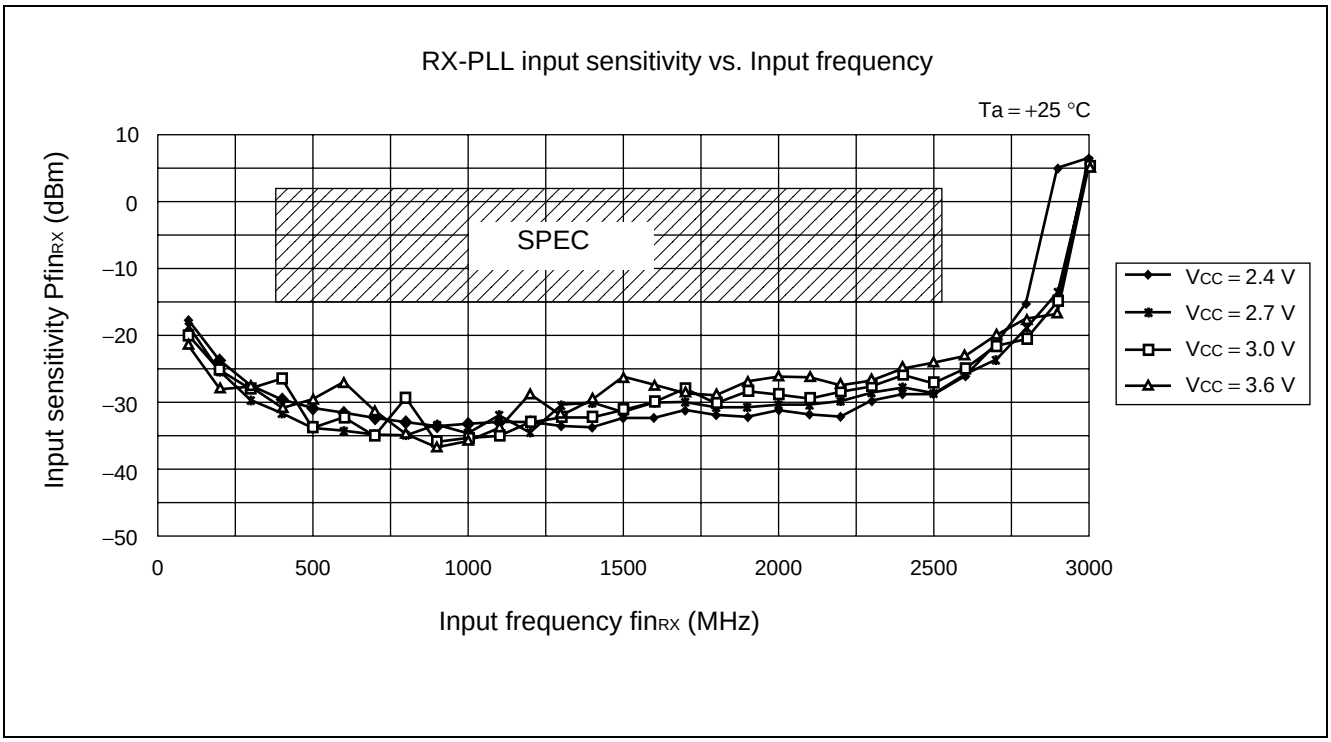
■ TEST CIRCUIT (for Measuring Input Sensitivity fin/OSC_{IN})



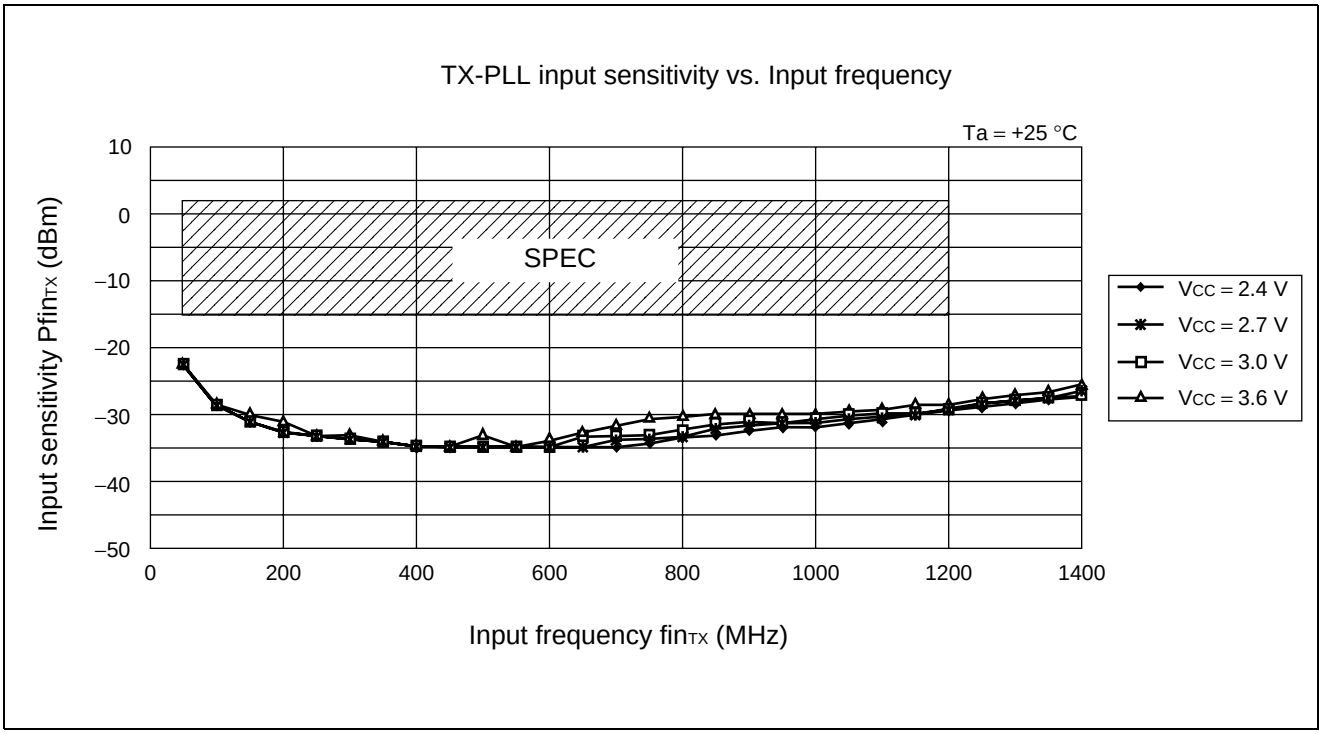
Note : The terminal number shows that of TSSOP-20

■ TYPICAL CHARACTERISTICS

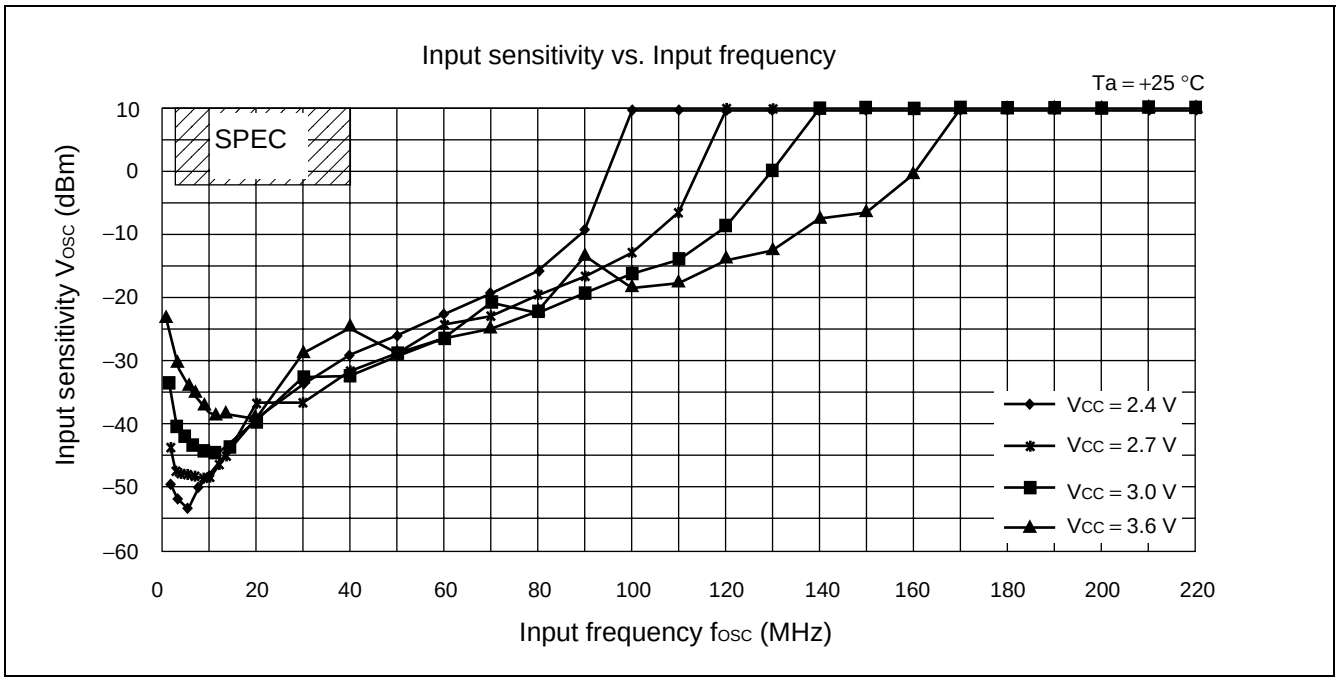
1. fin_{RX} input sensitivity



2. fin_{TX} input sensitivity

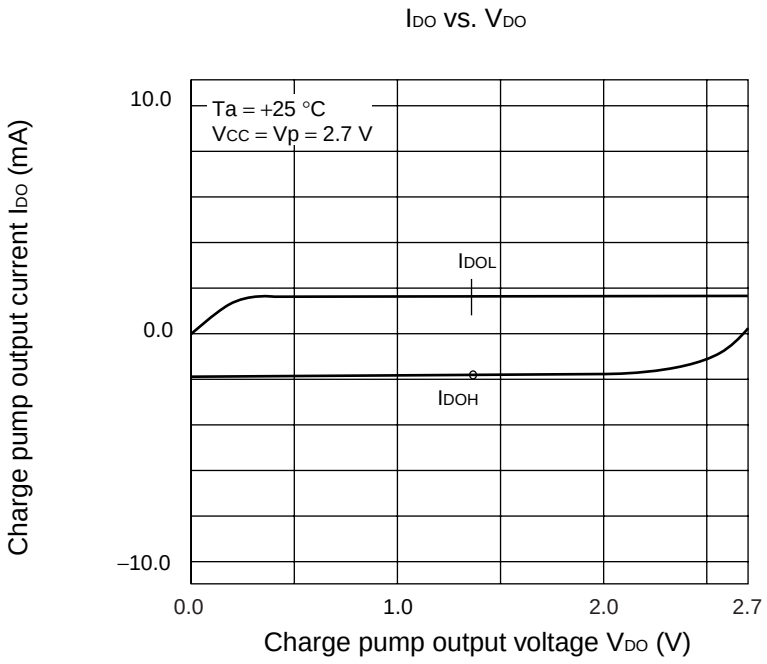


3. OSC_{IN} input sensitivity

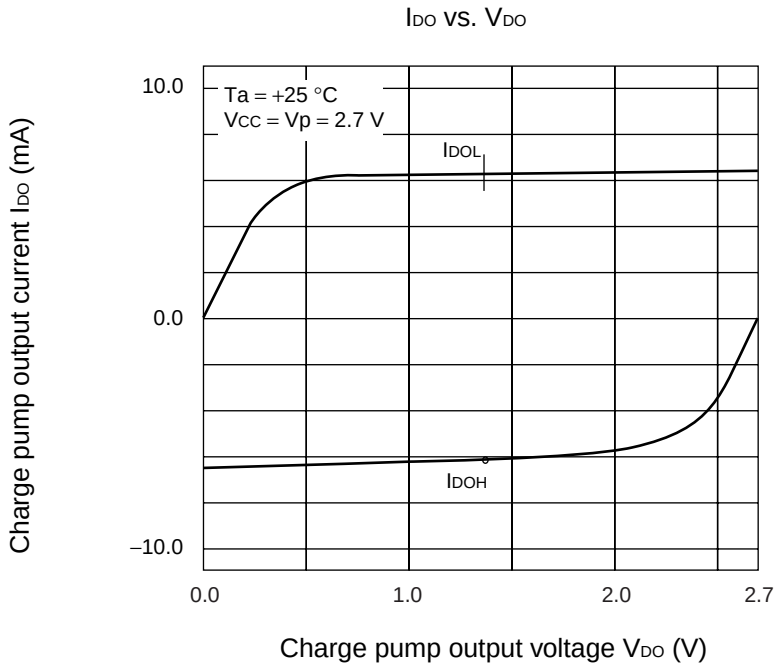


4. Do output current (RX PLL)

- 1.5 mA mode

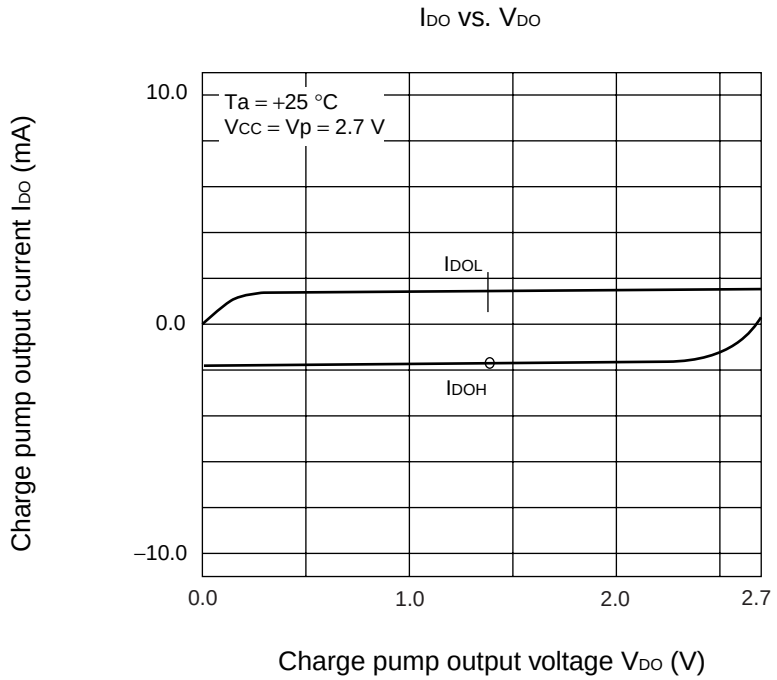


- 6.0 mA mode

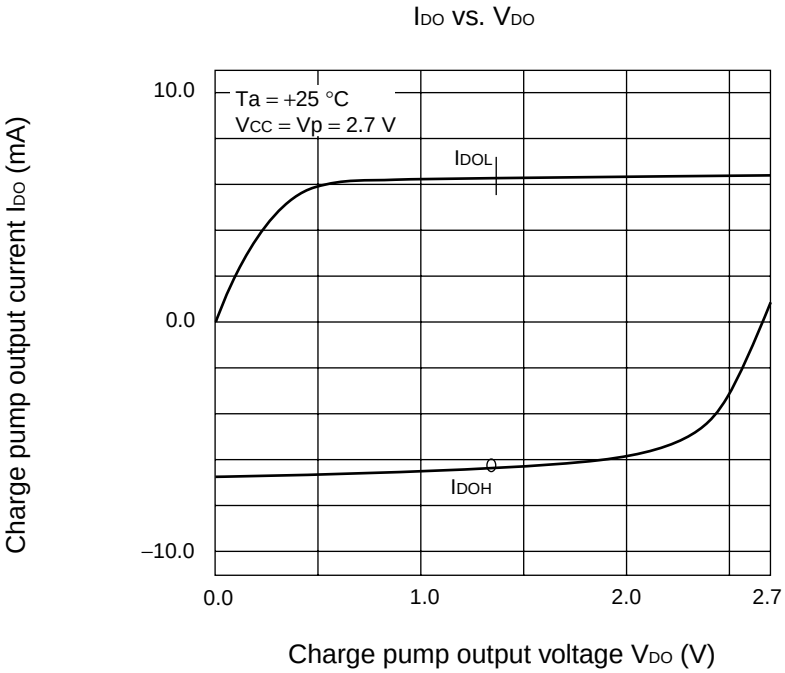


5. Do output current (TX PLL)

- 1.5 mA mode

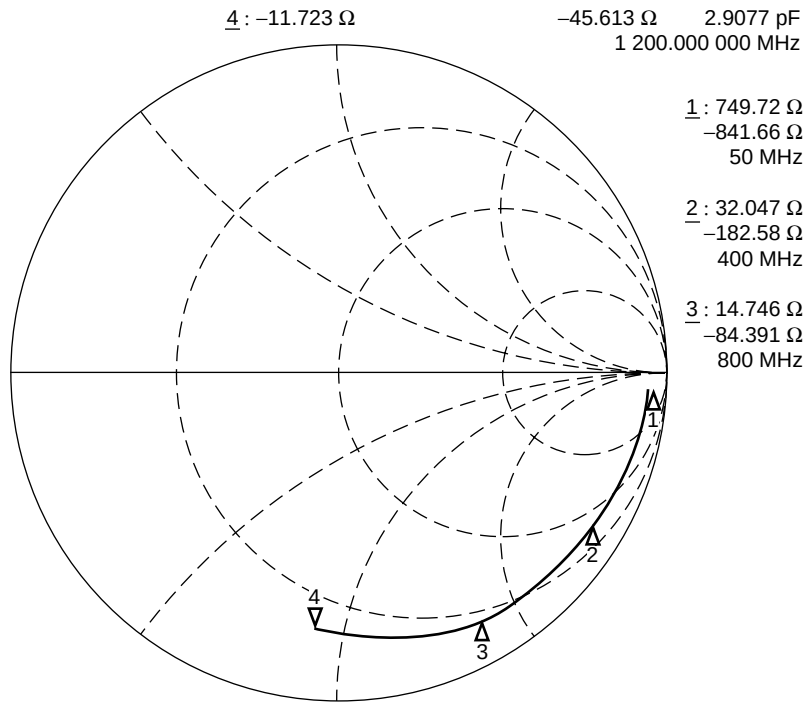


- 6.0 mA mode

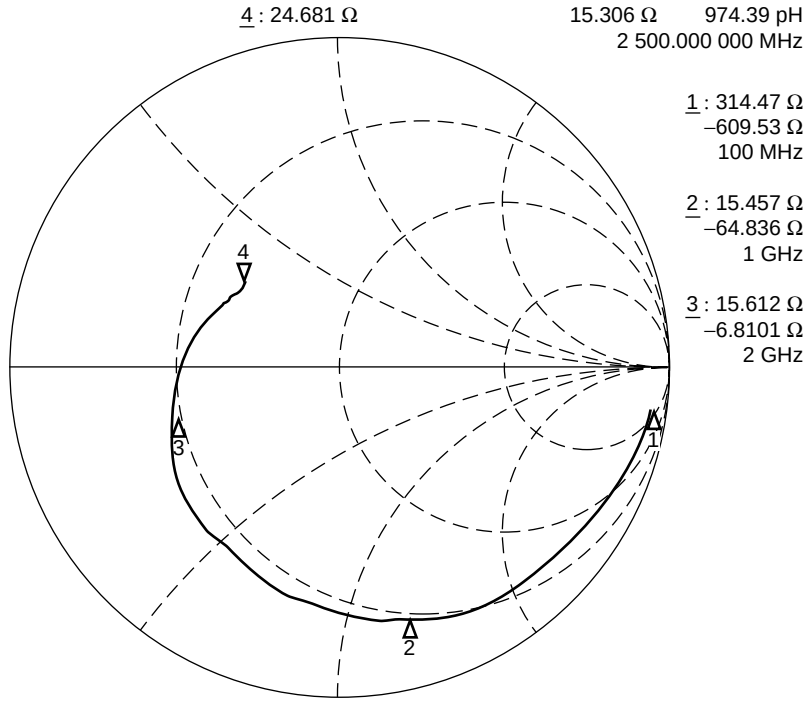


6. fin input impedance

finTX input impedance

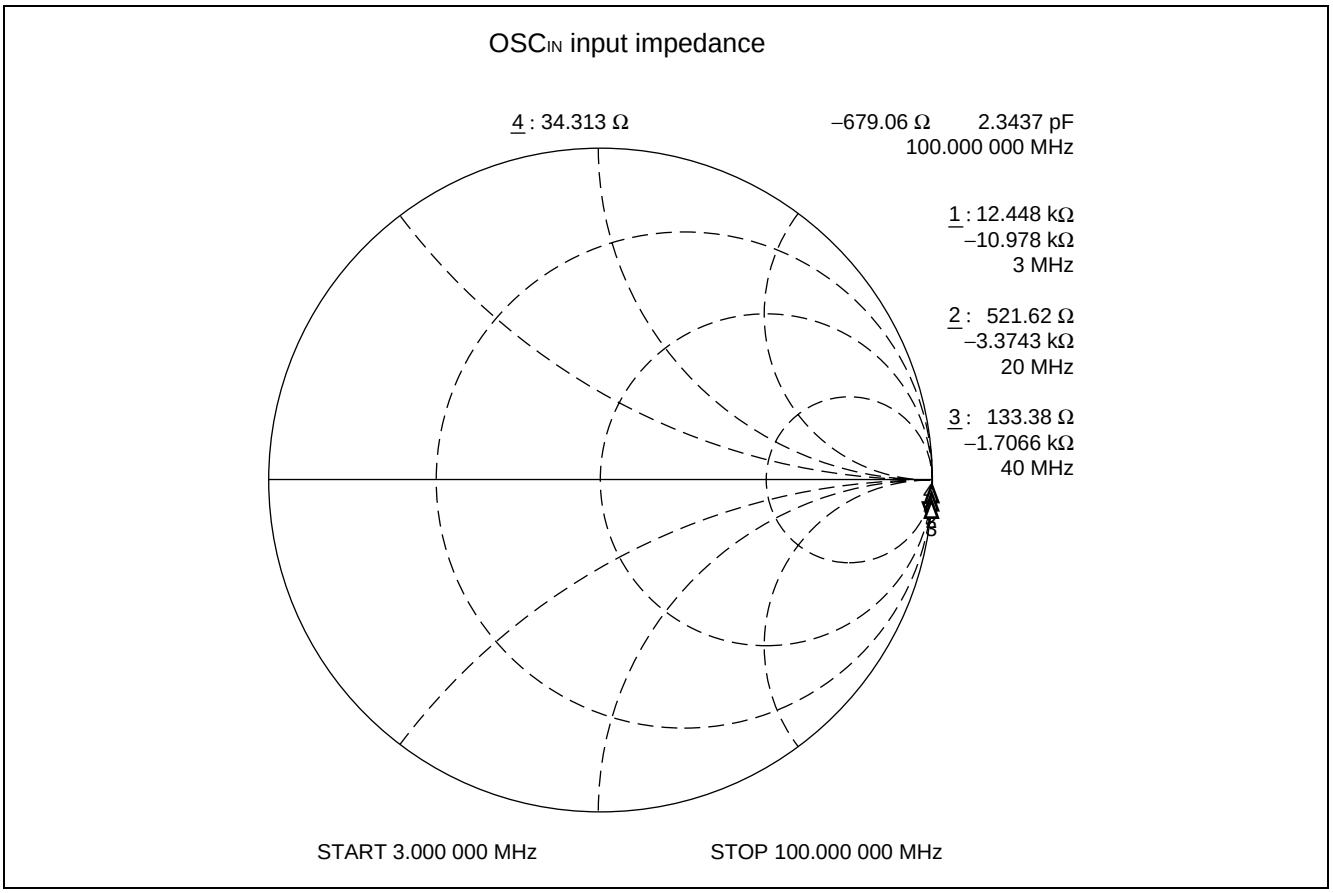


finRX input impedance



MB15F78SP

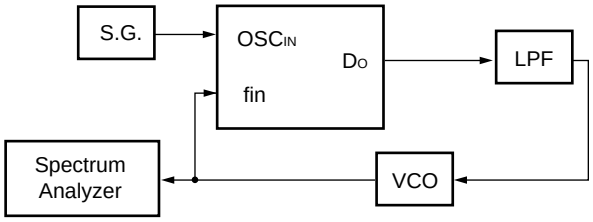
7. OSC_{IN} input impedance



■ REFERENCE INFORMATION

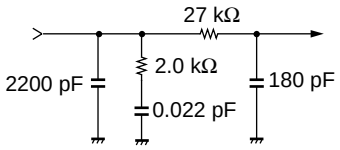
(for Look-up time, Phase noise and Reference leakage)

Test Circuit

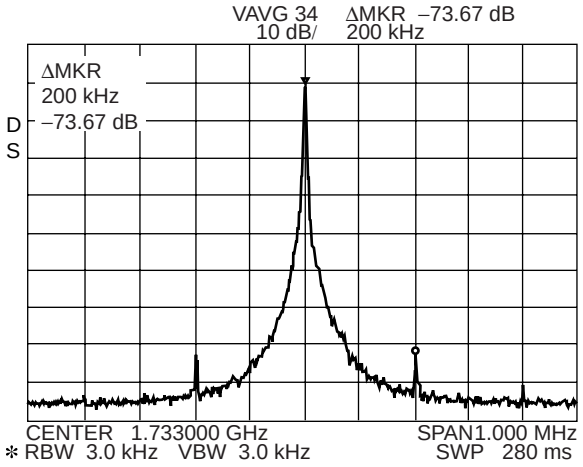


f_{VCO} = 1733 MHz
K_V = 44 MHz/V
fr = 200 kHz
f_{OSC} = 13 MHz
LPF

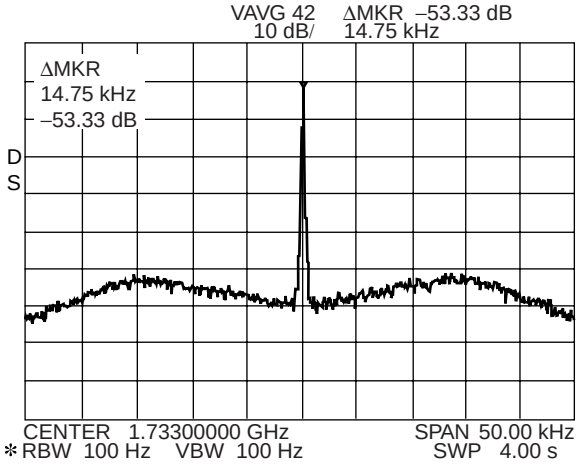
V_{CC} = 3.0 V
V_{VCO} = 3.5 V
Ta = +25 °C
CP : 6 mA mode



- PLL Reference Leakage



- PLL Phase Noise



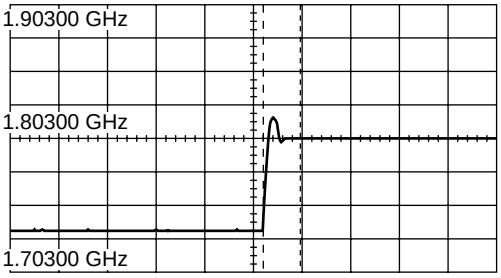
(Continued)

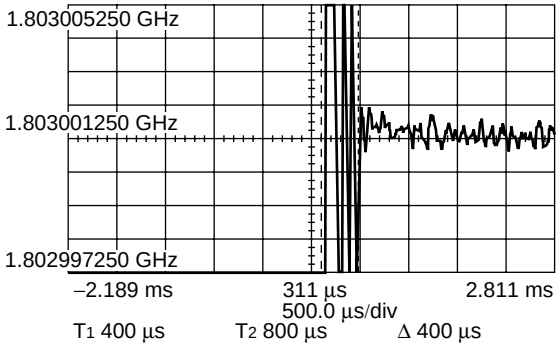
MB15F78SP

(Continued)

• PLL Lock-up time

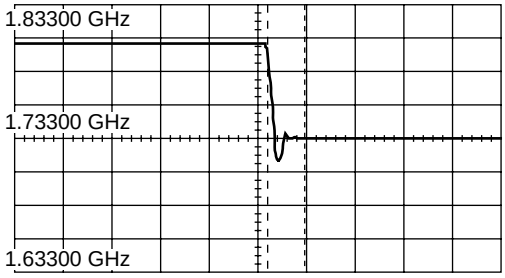
1733 MHz→1803 MHz within ± 1 kHz
Lch→Hch 400 µs

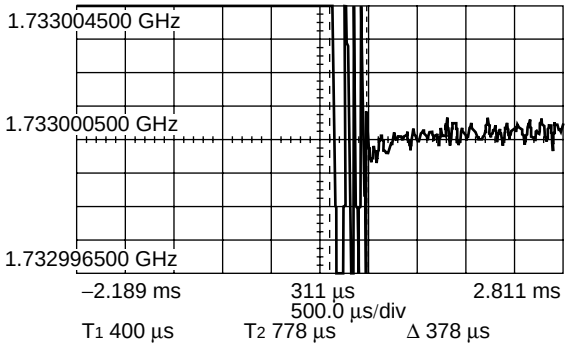




• PLL Lock-up time

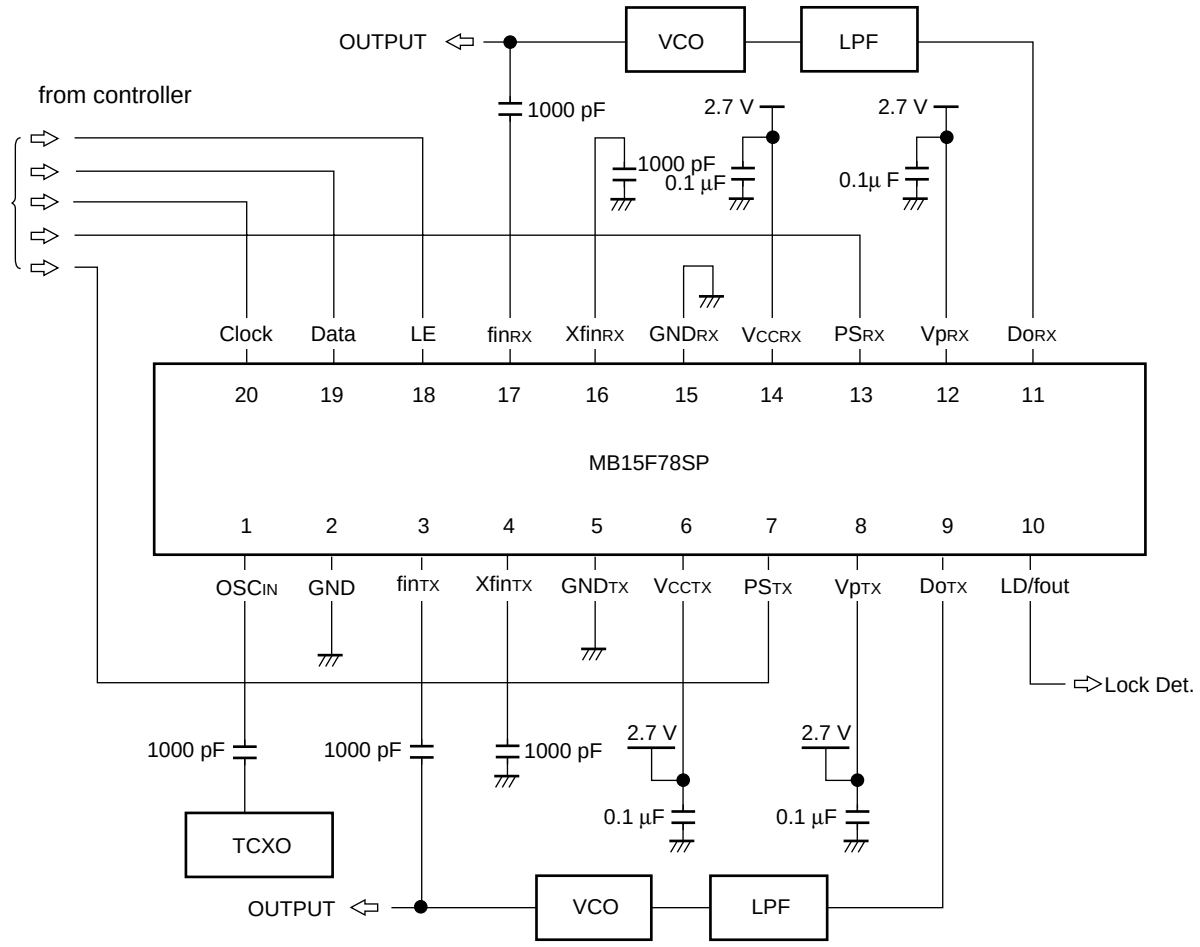
1803 MHz→1733 MHz within ± 1 kHz
Hch→Lch 378 µs





MB15F78SP

■ APPLICATION EXAMPLE



Notes : • Clock, Data, LE : Schmitt trigger circuit is provided (insert a pull-down or pull-up register to prevent oscillation when open-circuit in the input).
• The terminal number shows that of TSSOP-20.

MB15F78SP

■ USAGE PRECAUTIONS

(1) V_{CCRX}, Vp_{RX}, V_{CCTX} and Vp_{TX} must equal equal voltage.
Even if either RX-PLL or TX-PLL is not used, power must be supplied to both V_{CCRX}, Vp_{RX}, V_{CCTX} and Vp_{TX} to keep them equal. It is recommended that the non-use PLL is controlled by power saving function.

(2) To protect against damage by electrostatic discharge, note the following handling precautions:
-Store and transport devices in conductive containers.
-Use properly grounded workstations, tools, and equipment.
-Turn off power before inserting or removing this device into or from a socket.
-Protect leads with conductive sheet, when transporting a board mounted device.

■ ORDERING INFORMATION

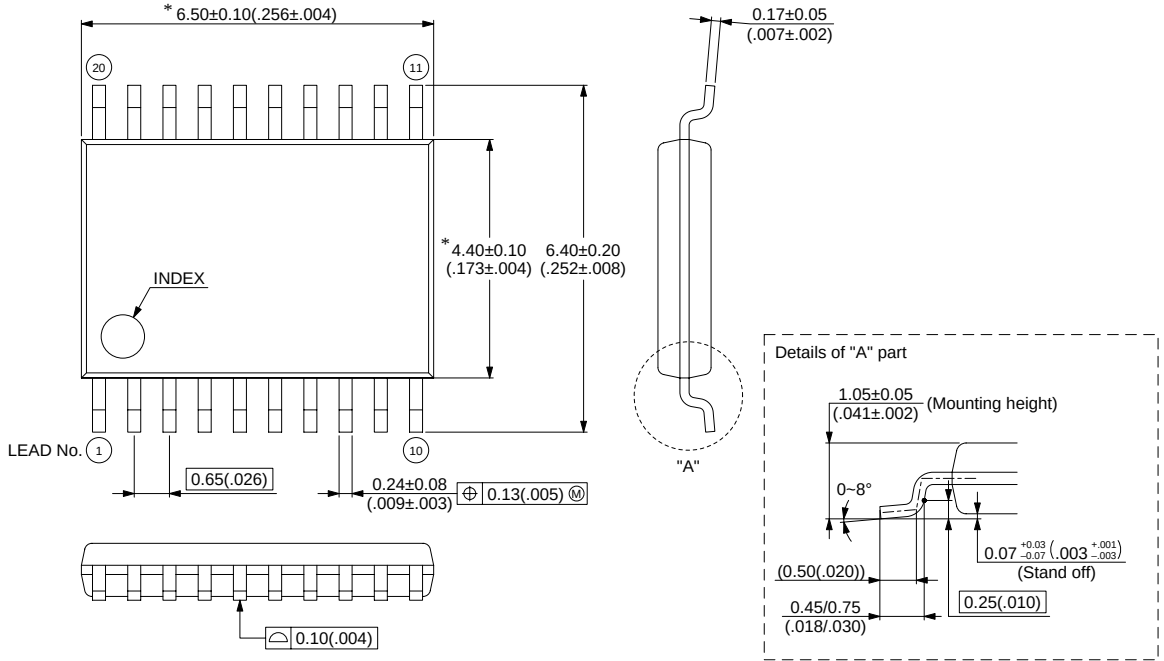
Part number	Package	Remarks
MB15F78SPPFT	20-pin, plastic TSSOP (FPT-20P-M06)	
MB15F78SPPV	20-pad, plastic BCC (LCC-20P-M04)	

■ PACKAGE DIMENSIONS

20-pin plastic TSSOP
(FPT-20P-M06)

Note 1) * : These dimensions do not include resin protrusion.

Note 2) Pins width and pins thickness include plating thickness.



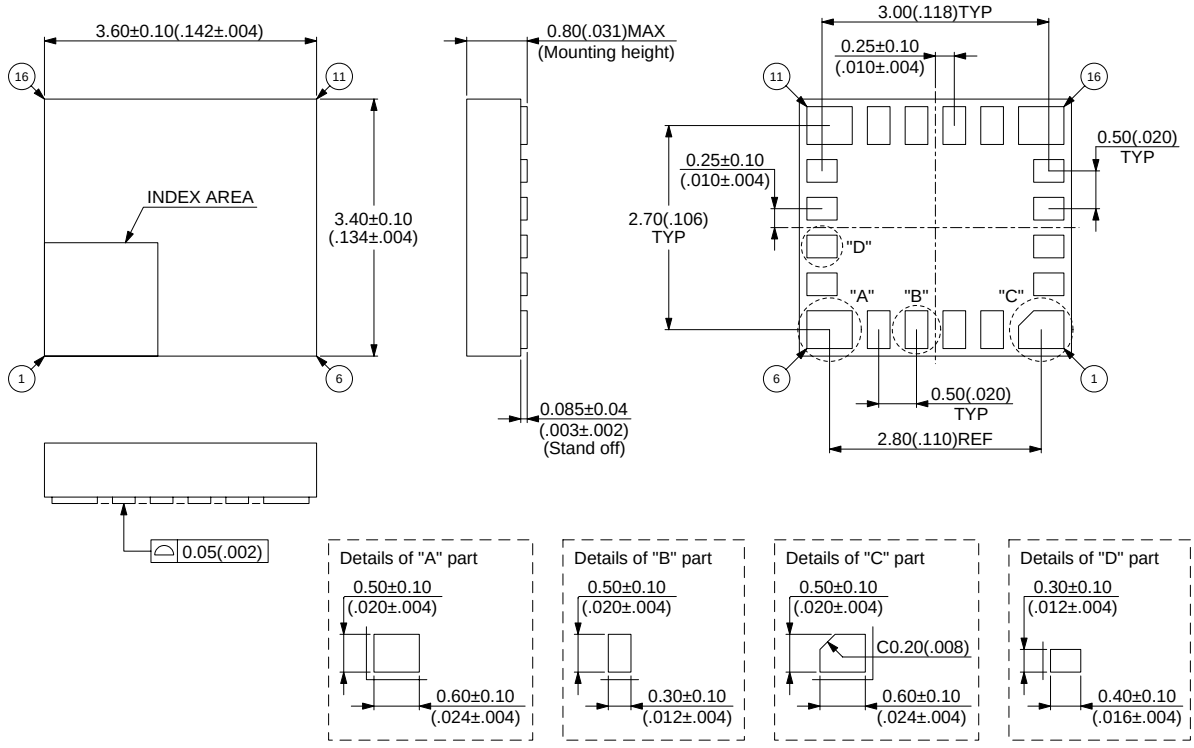
Dimensions in mm (inches)

(Continued)

MB15F78SP

(Continued)

20-pad plastic BCC
(LCC-20P-M04)



Dimensions in mm (inches)

MB15F78SP

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka,
Nakahara-ku, Kawasaki-shi,
Kanagawa 211-8588, Japan
Tel: +81-44-754-3763
Fax: +81-44-754-3329

http://www.fujitsu.co.jp/

North and South America

FUJITSU MICROELECTRONICS, INC.
3545 North First Street,
San Jose, CA 95134-1804, U.S.A.
Tel: +1-408-922-9000
Fax: +1-408-922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: +1-800-866-8608
Fax: +1-408-922-9179

http://www.fujitsumicro.com/

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Am Siebenstein 6-10,
D-63303 Dreieich-Buchschlag,
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

http://www.fujitsu-fme.com/

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LTD.
#05-08, 151 Lorong Chuan,
New Tech Park,
Singapore 556741
Tel: +65-281-0770
Fax: +65-281-0220

http://www.fmap.com.sg/

Korea

FUJITSU MICROELECTRONICS KOREA LTD.
1702 KOSMO TOWER, 1002 Daechi-Dong,
Kangnam-Gu,Seoul 135-280
Korea
Tel: +82-2-3484-7100
Fax: +82-2-3484-7111

F0005

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The contents of this document may not be reproduced or copied without the permission of FUJITSU LIMITED.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipments, industrial, communications, and measurement equipments, personal or household devices, etc.).
CAUTION:
Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.