FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12505-3E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89640 Series

MB89643/645/646/647/P647/PV640

■ DESCRIPTION

The MB89640 series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as dual-clock control system, five operating speed control stages, timers, a PWM timer, serial interface, an A/D converter, a D/A converter, an external interrupt, and a watch prescaler.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

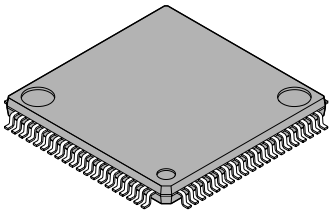
- F²MC-8L family CPU core

Instruction set optimized for controllers
- Multiplication and division instructions
- 16-bit arithmetic operations
- Test and branch instructions
- Bit manipulation instructions, etc.

(Continued)

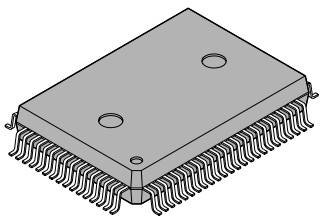
■ PACKAGE

80-pin Plastic QFP



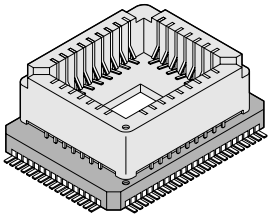
(FPT-80P-M11)

80-pin Plastic QFP



(FPT-80P-M06)

80-pin Ceramic MQFP



(MQP-80C-P01)

MB89640 Series

(Continued)

- Six types of timers
  8-bit PWM timer: 2 channels (also usable reload timer)
  8-bit pulse width counter (continuous measurement capable and applicable to remote control)
  16-bit timer/counter
  21-bit time-base counter
  15-bit watch prescaler
- Two 8-bit serial I/O
  Swichable transfer direction allows communication with various equipment.
- 8-bit A/D converter: 8 channels
  Sense mode function enabling comparison at 12 instructions
  Activation by external input capable
- External interrupt 1, external interrupt 2: 9 channels
- 8-bit D/A converter: 2 channels
  8-bit R-2R type
- Low-power consumption modes (stop mode, sleep mode, watch mode, subclock mode)
- Bus interface functions
  Including hold and ready functions

■ PRODUCT LINEUP

Parameter \ Part number	MB89643	MB89645	MB89646	MB89647	MB89P647	MB89PV640
Classification	Mass production products (mask ROM products)				One-time PROM product	Piggyback/ evaluation product for evaluation and development
ROM size	8 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal mask ROM)	24 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal PROM, programming with general-purpose programmer)	32 K × 8 bits (external ROM)
RAM size	256 × 8 bits	512 × 8 bits	768 × 8 bits	1 K × 8 bits		
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.4 µs/10 MHz to 6.4 µs/10 MHz, or 61.0 µs/32.768 kHz Interrupt processing time: 3.6 µs/10 MHz to 57.6 µs/10 MHz, or 562.5 µs/32.768 kHz					
Ports	Input ports (CMOS): 9 (All also serve as a external interrupt.) Output ports (CMOS): 8 (All also serve as a bus control.) I/O ports (CMOS): 24 (8 ports also serve as peripherals, 16 ports also serve as a bus control.) I/O ports (N-ch open-drain): 8 (All also serve as peripherals.) Output ports (N-ch open-drain): 16 (8 ports also serve as peripherals.) Total: 65					
Clock timer	21 bits × 1 (in main clock mode), 15 bits × 1 (at 32.768 kHz)					
8-bit PWM timer	8-bit reload timer operation × 2 channels 7/8-bit resolution PWM operation × 2 channels 8-bit PPG operation × 1 channel					
8-bit pulse width counter	8-bit timer operation (overflow output capable) 8-bit reload timer operation (toggled output capable) 8-bit pulse width measurement operation (Continuous measurement capable, measurement of “H” width/“L” width/from ↑ to ↓/from ↓ to ↑ capable)					
16-bit timer/ counter	16-bit timer operation 16-bit event counter operation					
8-bit serial I/O	8 bits × 2 channels LSB first/MSB first selectability One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 0.8 µs, 3.2 µs, 12.8 µs)					
8-bit A/D converter	8-bit resolution × 8 channels A/D conversion mode (conversion time: 44 instructions) Sense mode (conversion time: 12 instructions) Continuous activation by an external activation or an internal timer capable Reference voltage input					

(Continued)

(Continued)

Parameter \ Part number	MB89643	MB89645	MB89646	MB89647	MB89P647	MB89PV640
8-bit D/A converter	8-bit resolution × 2 channels, R-2R type					
External interrupt 1, External interrupt 2	9 channels					
Standby modes	Watch mode, subclock mode, sleep mode, and stop mode					
Process	CMOS					
Operating voltage*1	2.2 V to 6.0 V				2.7 V to 6.0 V	
EPROM for use	—					MBM27C256A -20TV

*1: Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89643 MB89645 MB89646 MB89647 MB89P647	MB89PV640
FPT-80P-M11	○	×
FPT-80P-M06	○	×
MQP-80C-P01	×	○

○ : Available × : Not available

Note: For more information about each package, see section "■ External Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89643 register banks 16 to 32 cannot be used.
- On the MB89P647, the program area starts from address 8007_H but on the MB89PV640 and MB89647 starts from 8000_H.

  (On the MB89P647, addresses 8000_H to 8006_H comprise the option setting area, option settings can be read by reading these addresses. On the MB89PV640 and MB89647, addresses 8000_H to 8006_H could also be used as a program ROM. However, do not use these addresses in order to maintain compatibility of the MB89P647.)
- The stack area, etc., is set at the upper limit of the RAM.
- The external areas are used.

2. Current Consumption

- In the case of the MB89PV640, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.
- However, the current consumption in sleep/stop modes is the same. (For more information, see sections "■ Electrical Characteristics" and "■ Example Characteristics.")

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section "■ Mask Options."

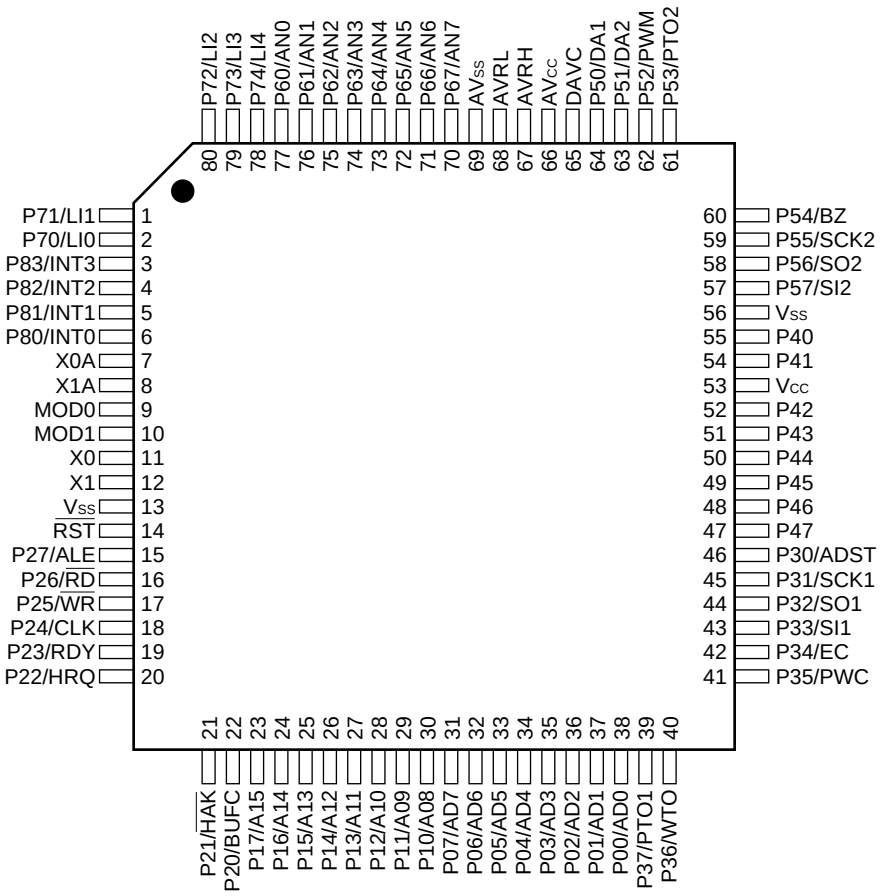
Take particular care on the following points:

- A pull-up resistor cannot be set for P40 to P47 and P50 to P57 on the MB89P647.
- For all products, P60 to P67 are available for no pull-up resistor when an A/D converter is used.
- For all products, P50 to P57 are available for no pull-up resistor when a D/A converter is used.
- Options are fixed on the MB89PV640.

MB89640 Series

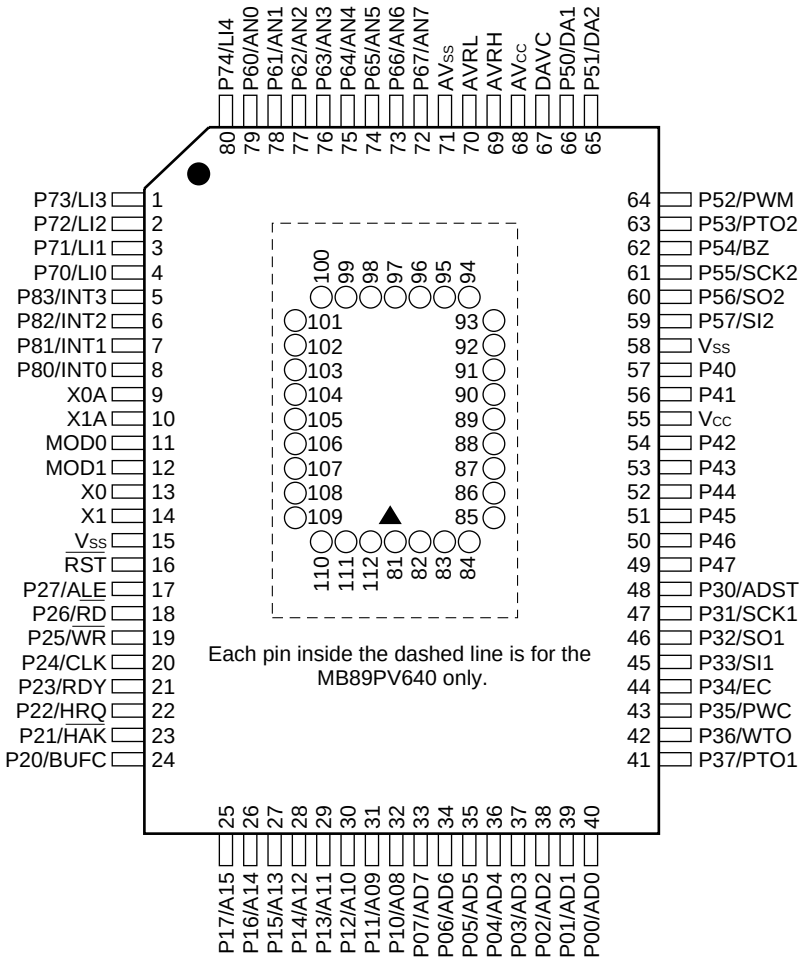
■ PIN ASSIGNMENT

(Top view)



(FPT-80P-M11)

(Top view)



(FPT-80P-M06)

(MQP-80C-P01)

- **Pin assignment on package top (MB89PV640 only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
81	N.C.	89	A2	97	N.C.	105	$\overline{OE}$
82	V_{PP}	90	A1	98	O4	106	N.C.
83	A12	91	A0	99	O5	107	A11
84	A7	92	N.C.	100	O6	108	A9
85	A6	93	O1	101	O7	109	A8
86	A5	94	O2	102	O8	110	A13
87	A4	95	O3	103	$\overline{CE}$	111	A14
88	A3	96	V_{SS}	104	A10	112	V_{CC}

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
QFP*1	QFP*2 MQFP*3			
11	13	X0	A	Main clock crystal oscillator pins (Max. 10 MHz)
12	14	X1		
9	11	MOD0	C	Operating mode selection pins Connect directly to V_{CC} or V_{SS}.
10	12	MOD1		
14	16	$\overline{RST}$	D	Reset I/O pin This pin is an N-ch open-drain output type with pull-up resistor, and a hysteresis input type. “L” is output from this pin by an internal reset source. The internal circuit is initialized by the input of “L”.
38 to 31	40 to 33	P00/AD0 to P07/AD7	E	General-purpose I/O ports Also serve as multiplex pins of lower address output and data I/O.
30 to 23	32 to 25	P10/A08 to P17/A15	E	General-purpose I/O ports Also serve as an upper address output.
22, 21, 18, 15	24, 23, 20, 17	P20/$\overline{BUFC}$, P21/$\overline{HAK}$, P24/CLK, P27/ALE	G	General-purpose output-only ports Also serve as a bus control signal output.
20, 19	22, 21	P22/HRQ, P23/RDY	E	General-purpose output-only ports Also serve as a bus control signal input.
17, 16	19, 18	P25/$\overline{WR}$, P26/$\overline{RD}$	E	General-purpose output-only ports Also serve as a bus control signal output.
46	48	P30/ADST	F	General-purpose I/O port Also serves as an A/D converter external activation. This port is a hysteresis input type.
45	47	P31/SCK1	F	General-purpose I/O port Also serves as the clock I/O for the serial I/O 1. This port is a hysteresis input type.
44, 43	46, 45	P32/SO1, P33/SI1	F	General-purpose I/O ports Also serve as the data output for the serial I/O 1. These ports are a hysteresis input type.
42	44	P34/EC	F	General-purpose I/O port Also serves as the external clock input for the 16-bit timer/counter. This port is a hysteresis input type.

(Continued)

*1: FPT-80P-M11
*2: FPT-80P-M06
*3: MQP-80C-P01

(Continued)

Pin no.		Pin name	Circuit type	Function
QFP*1	QFP*2 MQFP*3			
41	43	P35/PWC	F	General-purpose I/O port Also serves as the measured pulse input for the 8-bit pulse width counter. This port is a hysteresis input type.
40	42	P36/WTO	F	General-purpose I/O port Also serves as the toggle output for the 8-bit pulse width counter. This port is a hysteresis input type.
39	41	P37/PTO1	F	General-purpose I/O port Also serves as the toggle output for the 1-channel PWM timer.
55, 54, 52 to 47	57, 56, 54 to 49	P40 to P47	L	N-ch medium-voltage open-drain output-only ports
64	66	P50/DA1	K	N-ch open-drain I/O port Also serves as a D/A channel 1 output. This port is a hysteresis input type.
63	65	P51/DA2	K	N-ch open-drain I/O port Also serves as a D/A channel 2 output. This port is a hysteresis input type.
62	64	P52/PWM	H	N-ch open-drain I/O port Also serves as the PWM output by the two PWM timers. This port is a hysteresis input type.
61	63	P53/PTO2	H	N-ch open-drain I/O port Also serves as the toggle output for the 2-channel PWM timer. This port is a hysteresis input type.
60	62	P54/BZ	H	N-ch open-drain I/O port Also serves as a buzzer output. This port is a hysteresis input type.
59	61	P55/SCK2	H	N-ch open-drain I/O port Also serves as the clock I/O for the serial I/O 2. This port is a hysteresis input type.
58	60	P56/SO2	H	N-ch open-drain I/O port Also serves as the data output for the serial I/O 2. This port is a hysteresis input type.
57	59	P57/SI2	H	N-ch open-drain I/O port Also serves as the data input for the serial I/O 2. This port is a hysteresis input type.
77 to 70	79 to 72	P60/AN0 to P67/AN7	I	N-ch open-drain output-only ports Also serve as the analog input for the A/D converter. These ports are a hysteresis input type.
2, 1, 80 to 78	4 to 1, 80	P70/LI0 to P74/LI4	J	Input-only ports Also serve as external interrupt 1 input. These ports are a hysteresis input type.

*1: FPT-80P-M11
*2: FPT-80P-M06
*3: MQP-80C-P01

(Continued)

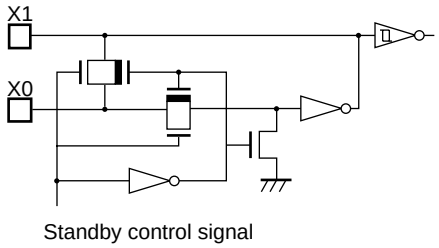
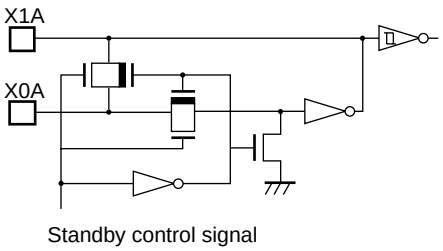
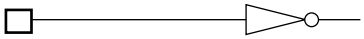
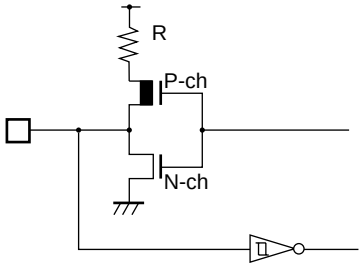
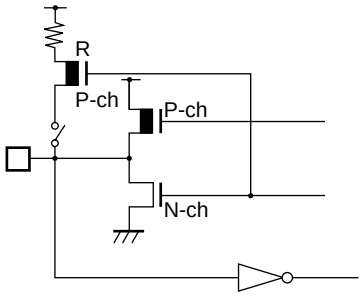
Pin no.		Pin name	Circuit type	Function
QFP*1	QFP*2 MQFP*3			
7	9	X0A	B	Subclock oscillator pins (32.768 kHz)
8	10	X1A		
53	55	V_{CC}	—	Power supply pin
13, 56	15, 58	V_{SS}	—	Power supply (GND) pin
66	68	AV_{CC}	—	A/D converter power supply pin Use this pin at the same voltage as V_{CC}.
67, 68	69, 70	AVRH, AVRL	—	A/D converter reference voltage input pins
65	67	DAVC	—	D/A converter power supply pin Use this pin at the same voltage as V_{CC}.
69	71	AV_{SS}	—	Analog circuit power supply pin Use this pin at the same voltage as V_{SS}.
3 to 6	5 to 8	P83/INT3 to P80/INT0	J	Input-only ports Also serve as an external interrupt 2 input. These ports are a hysteresis input type.

*1: FPT-80P-M11
*2: FPT-80P-M06
*3: MQP-80C-P01

- **External EPROM pins (MB89PV640 only)**

Pin no.	Pin name	I/O	Function
82	V_{PP}	O	“H” level output pin
83 84 85 86 87 88 89 90 91	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
93 94 95	O1 O2 O3	I	Data input pins
96	V_{SS}	O	Power supply (GND) pin
98 99 100 101 102	O4 O5 O6 O7 O8	I	Data input pins
103	$\overline{CE}$	O	ROM chip enable pin Outputs “H” during standby.
104	A10	O	Address output pin
105	$\overline{OE}$	O	ROM output enable pin Outputs “L” at all times.
107 108 109	A11 A9 A8	O	Address output pins
110	A13	O	
111	A14	O	
112	V_{CC}	O	EPROM power supply pin
81 92 97 106	N.C.	—	Internally connected pins Be sure to leave them open.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Main clock • At an oscillation feedback resistor of approximately 1 MΩ/5.0 V
B		Subclock • At an oscillation feedback resistor of approximately 4.5 MΩ/5.0 V
C		
D		• At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • Hysteresis input
E		• CMOS output • CMOS input • Pull-up resistor optional

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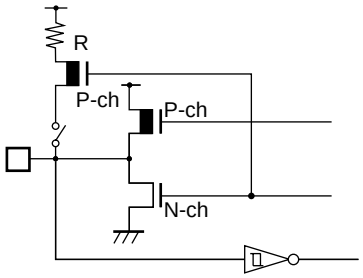
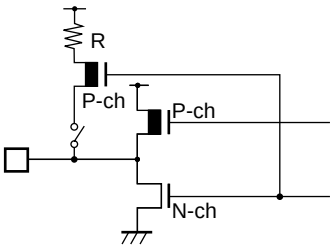
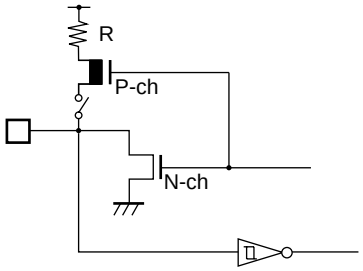
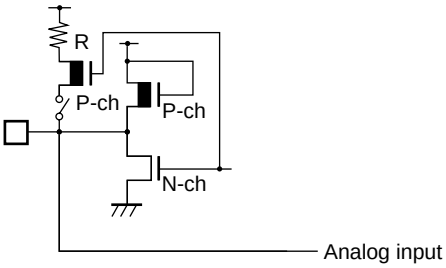
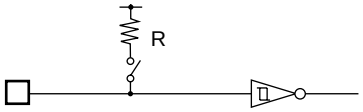
Type	Circuit	Remarks
F		• CMOS output • Hysteresis input • Pull-up resistor optional
G		• CMOS output • Pull-up resistor optional
H		• N-ch open-drain output • Hysteresis input • Pull-up resistor optional
I		• N-ch open-drain output • Analog input • Pull-up resistor optional
J		• Hysteresis input • Pull-up resistor optional

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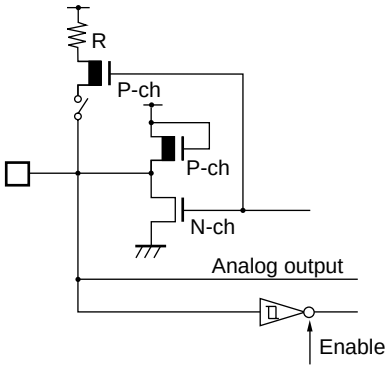
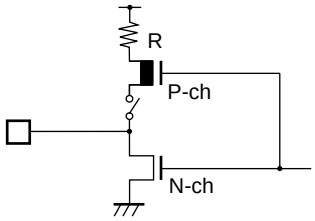
MB89640 Series

(Continued)

Type	Circuit	Remarks
K		• N-ch open-drain output • Hysteresis input • Analog output • Pull-up resistor optional
L		• N-ch open-drain output • Medium voltage • Pull-up resistor optional

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVRH) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVRH = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P647

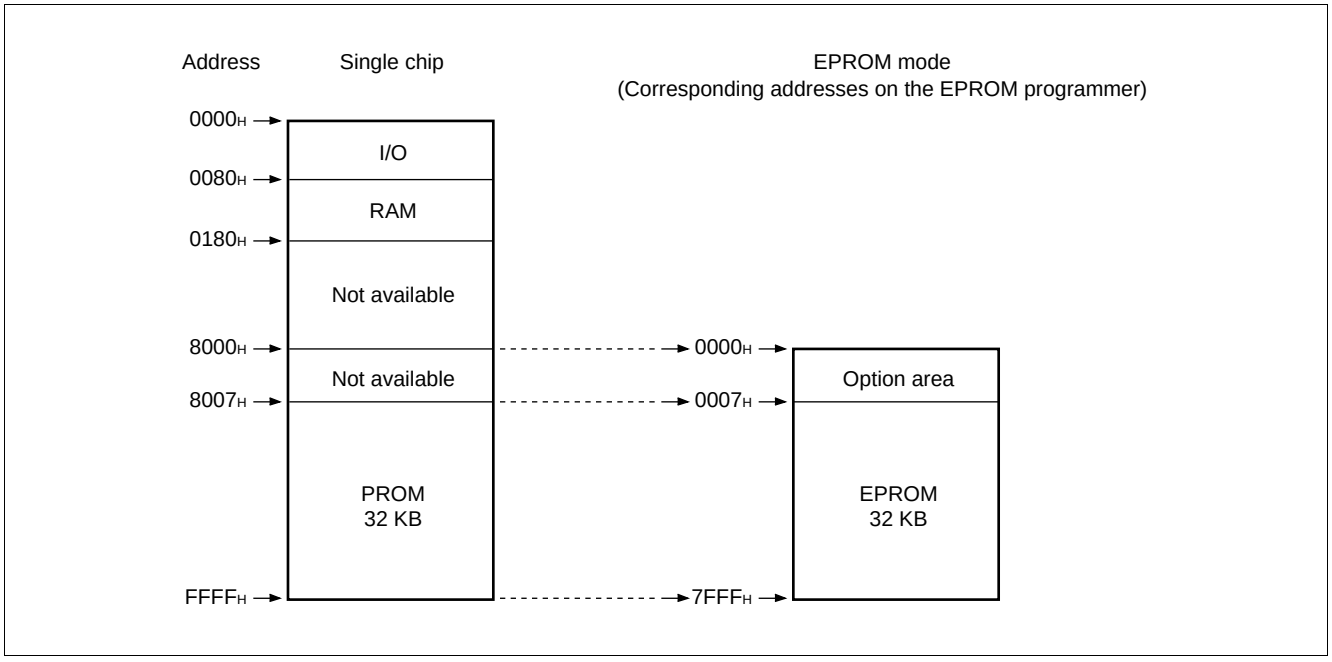
The MB89P647 is an OTPROM version of the MB89640 series.

1. Features

- 32-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in each mode such as 32-Kbyte PROM, option area is diagrammed below.



- **Precautions**

(1) The program area of the MB89P647 is 7 bytes smaller than that of the MB89PV640 and MB89647 to provide an option area. Note this point during program development.

(2) During normal operation, the option data is read when the option area is read from the CPU.

3. Programming to the EPROM

In EPROM mode, the MB89P647 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure**

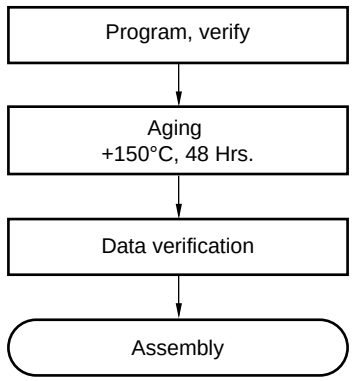
(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0007_H to $7FFF_H$ (note that addresses 8007_H to $FFFF_H$ while operating as internal ROM mode assign to 0007_H to $7FFF_H$ in EPROM mode).
Load option data into addresses 0000_H to 0006_H of the EPROM programmer. (For information about each corresponding option, see “7. Setting OTPROM Options.”)

(3) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
FPT-80P-M06	ROM-80QF-28DP-8L2
FPT-80P-M11	ROM-80QF2-28DP-8L

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

Note: Depending on the EPROM programmer, inserting a capacitor of about 0.1 µF between V_{PP} and V_{SS} or V_{CC} and V_{SS} can stabilize programming operations.

7. Setting OTPROM Options

The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map:

- **OTPROM option bit map**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Single/dual-clock system 1: Dual clock 2: Single clock	Reset pin output 1: Yes 2: No	Power-on reset 1: Yes 2: No	Oscillation stabilization time 00: $2^4/F_{CH}$ 01: $2^{17}/F_{CH}$	 10: $2^{14}/F_{CH}$ 11: $2^{18}/F_{CH}$
0001_H	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
0002_H	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
0003_H	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
0004_H	P67 Pull-up 1: No 0: Yes	P66 Pull-up 1: No 0: Yes	P65 Pull-up 1: No 0: Yes	P64 Pull-up 1: No 0: Yes	P63 Pull-up 1: No 0: Yes	P62 Pull-up 1: No 0: Yes	P61 Pull-up 1: No 0: Yes	P60 Pull-up 1: No 0: Yes
0005_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P74 Pull-up 1: No 0: Yes	P73 Pull-up 1: No 0: Yes	P72 Pull-up 1: No 0: Yes	P71 Pull-up 1: No 0: Yes	P70 Pull-up 1: No 0: Yes
0006_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P83 Pull-up 1: No 0: Yes	P82 Pull-up 1: No 0: Yes	P81 Pull-up 1: No 0: Yes	P80 Pull-up 1: No 0: Yes

Notes: • Set each bit to 1 to erase.
• Do not write 0 to the vacant bit.
The read value of the vacant bit is 1, unless 0 is written to it.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TV

2. Programming Socket Adapter

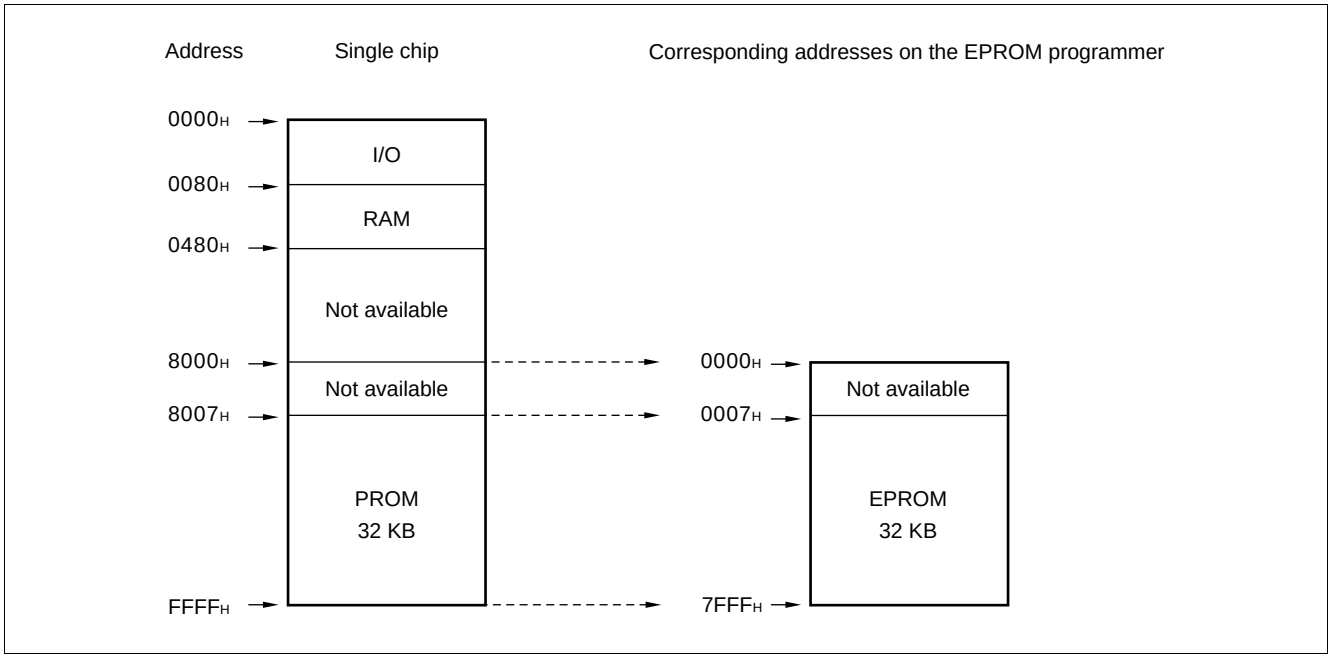
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-YG

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

3. Memory Space

Memory space in each mode, such as 32-Kbyte PROM is diagrammed below.



4. Programming to the EPROM

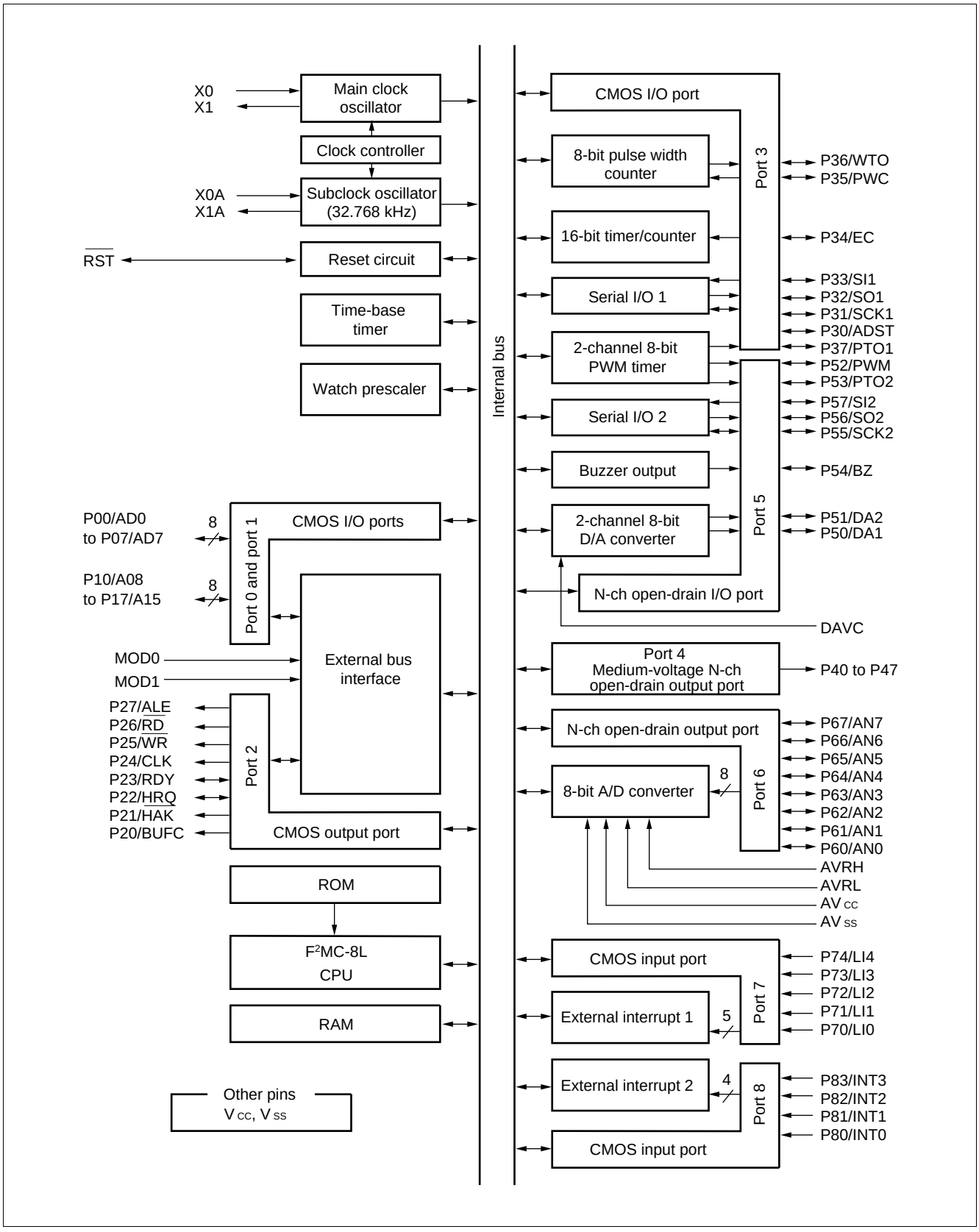
(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0007_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

MB89640 Series

■ BLOCK DIAGRAM

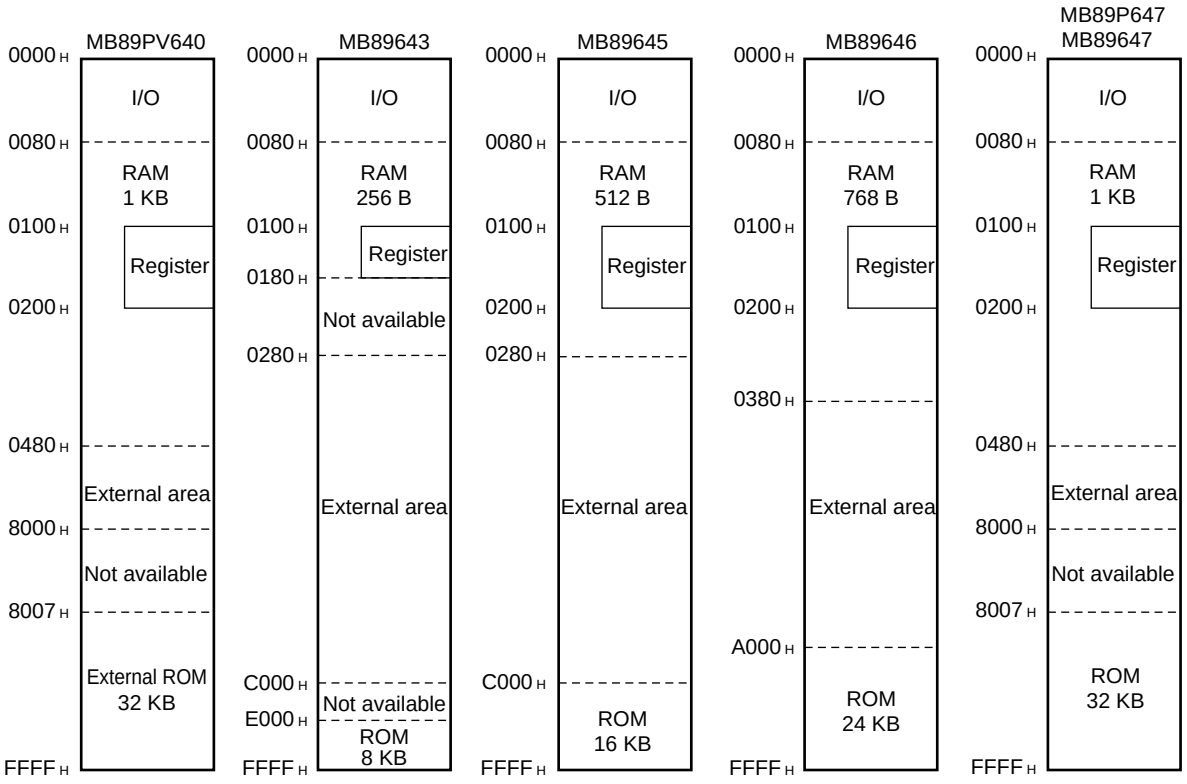


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89640 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89640 series is structured as illustrated below.

Memory Space

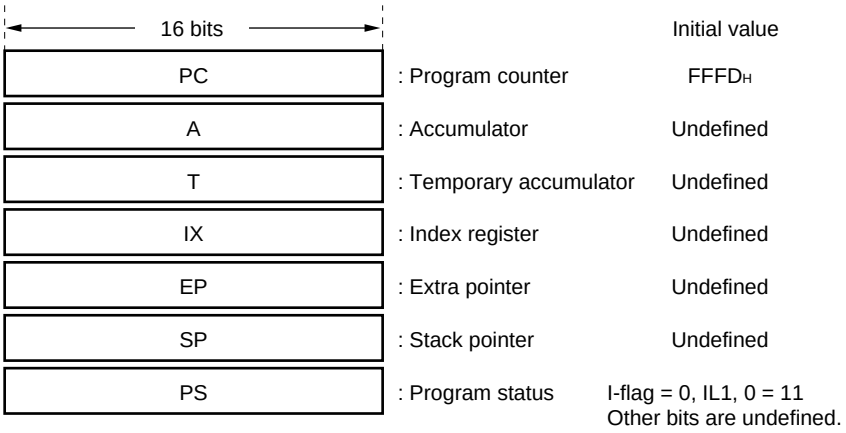


Note: Since addresses 8000H to 8006H for the MB89P647 comprise an option area, do not use this area for the MB89PV640 and MB89647.

2. Registers

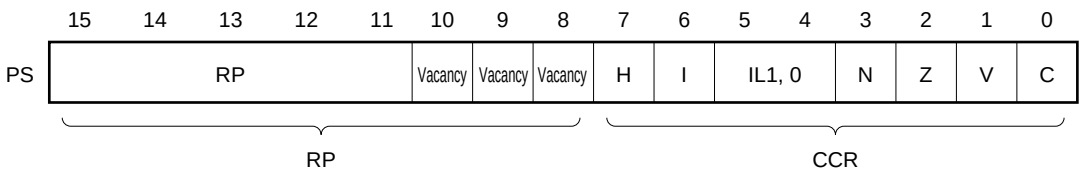
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



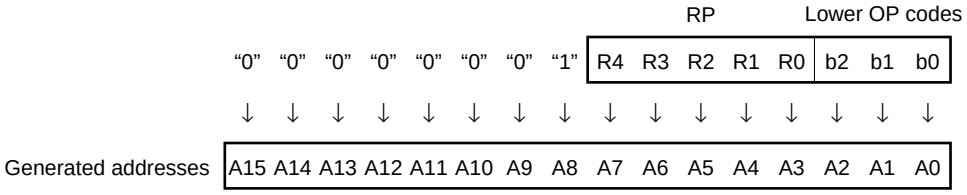
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High ↕ Low = no interrupt
0	1		
1	0	2	
1	1	3	

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

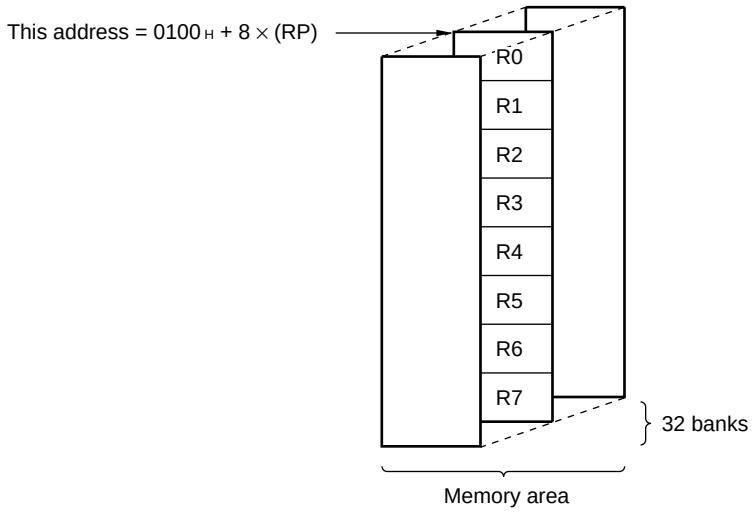
The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 16 banks can be used on the MB89643 and a total of 32 banks can be used on the MB89645/646/647/P647/PV640. The bank currently in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size.

Register Bank Configuration



■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H	(R/W)	PDR1	Port 1 data register
03H	(W)	DDR1	Port 1 data direction register
04H	(R/W)	PDR2	Port 2 data register
05H	(W)	BCTR	External bus control register
06H			Vacancy
07H	(R/W)	SYCC	System clock control register
08H	(R/W)	STBC	Standby control register
09H	(R/W)	WDTC	Watchdog timer control register
0AH	(R/W)	TBCR	Time-base timer control register
0BH	(R/W)	WPCR	Watch prescaler control register
0CH	(R/W)	PDR3	Port 3 data register
0DH	(W)	DDR3	Port 3 data direction register
0EH	(R/W)	PDR4	Port 4 data register
0FH	(R/W)	BUZR	Buzzer register
10H	(R/W)	PDR5	Port 5 data register
11H	(R/W)	PDR6	Port 6 data register
12H	(R)	PDR7	Port 7 data register
13H	(R)	PDR8	Port 8 data register
14H			Vacancy
15H			Vacancy
16H			Vacancy
17H			Vacancy
18H	(R/W)	TMCR	16-bit timer control register
19H	(R/W)	TCHR	16-bit timer count register (H)
1AH	(R/W)	TCLR	16-bit timer count register (L)
1BH			Vacancy
1CH	(R/W)	SMR1	Serial 1 mode register
1DH	(R/W)	SDR1	Serial 1 data register
1EH	(R/W)	SMR2	Serial 2 mode register
1FH	(R/W)	SDR2	Serial 2 data register

(Continued)

(Continued)

Address	Read/write	Register name	Register description
20_H	(R/W)	ADC1	A/D converter control register 1
21_H	(R/W)	ADC2	A/D converter control register 2
22_H	(R/W)	ADCD	A/D converter data register
23_H			Vacancy
24_H	(R/W)	DACR	D/A converter control register
25_H	(W)	DADR1	D/A converter data register 1
26_H	(W)	DADR2	D/A converter data register 2
27_H			Vacancy
28_H	(R/W)	CNTR1	PWM timer control register 1
29_H	(R/W)	CNTR2	PWM timer control register 2
$2A_H$	(R/W)	CNTR3	PWM timer control register 3
$2B_H$	(W)	COMR1	PWM timer compare register 1
$2C_H$	(W)	COMR2	PWM timer compare register 2
$2D_H$	(R/W)	PCR1	PWC pulse width control register 1
$2E_H$	(R/W)	PCR2	PWC pulse width control register 2
$2F_H$	(R/W)	RLBR	PWC reload buffer register
30_H			Vacancy
31_H	(R/W)	EIC1	External interrupt 1 control register 1
32_H	(R/W)	EIC2	External interrupt 1 control register 2
33_H	(R/W)	EIE2	External interrupt 2 enable register
34_H	(R/W)	EIF2	External interrupt 2 flag register
35_H to $7A_H$			Vacancy
$7B_H$			Vacancy
$7C_H$	(W)	ILR1	Interrupt level setting register 1
$7D_H$	(W)	ILR2	Interrupt level setting register 2
$7E_H$	(W)	ILR3	Interrupt level setting register 3
$7F_H$			Vacancy

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC} DAVC	V_{SS} – 0.3	V_{SS} + 7.0	V	*
A/D converter reference input voltage	AVRH	V_{SS} – 0.3	V_{SS} + 7.0	V	AVRH must not exceed AV_{CC} + 0.3 V.
	AVRL	V_{SS} – 0.3	V_{SS} + 7.0	V	AVRL must not exceed AVRH.
Program voltage	V_{PP}	V_{SS} – 0.3	13.0	V	MOD1 pin on MB89P647
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	P52 to P57 with a pull-up resistor and other input ports
	V_{I2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P52 to P57 without a pull-up resistor
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	P40 to P47 and P52 to P57 with a pull-up resistor and other output ports
	V_{O2}	V_{SS} – 0.3	V_{SS} + 17.0	V	P40 to P47 without a pull-up resistor
	V_{O3}	V_{SS} – 0.3	V_{SS} + 7.0	V	P52 to P57 without a pull-up resistor
“L” level maximum output current	I_{OL}	—	20	mA	
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
“L” level total average output current	$\sum I_{OLAV}$	—	40	mA	Average value (operating current × operating rate)
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	
“H” level maximum output current	I_{OH}	—	–20	mA	
“H” level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
“H” level total average output current	$\sum I_{OHAV}$	—	–20	mA	Average value (operating current × operating rate)
“H” level total maximum output current	$\sum I_{OH}$	—	–50	mA	
Power consumption	P_D	—	500	mW	

(Continued)

(Continued)

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

* : Use DAVC and AV_{CC} and V_{CC} set at the same voltage.
Take care so that DAVC and AV_{CC} does not exceed V_{CC}, such as when power is turned on.

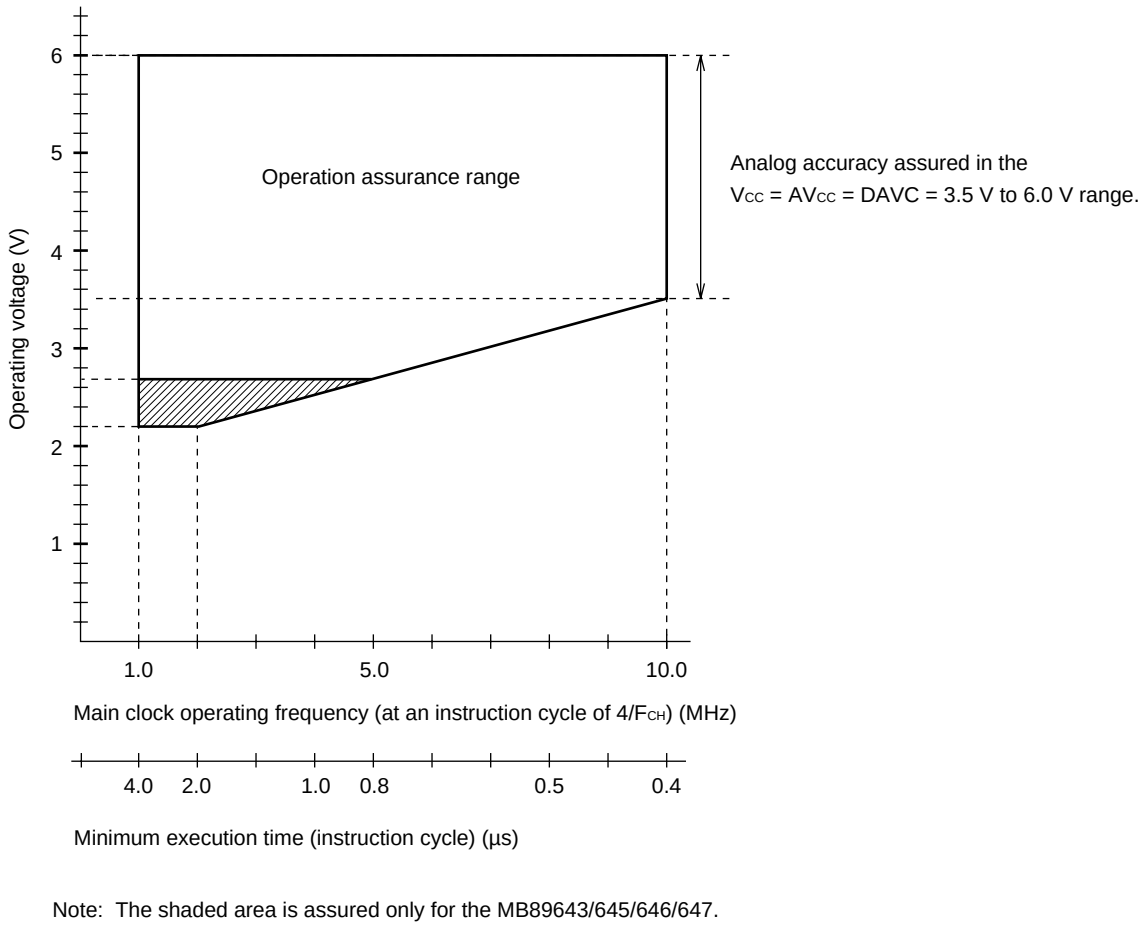
Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC} DAVC	2.2*	6.0*	V	Normal operation assurance range* (MB89643/645/646/647)
		2.7*	6.0*	V	Normal operation assurance range* (MB89P647/PV640)
		1.5	6.0	V	Retains the RAM state in stop mode
A/D converter reference input voltage	AVRH	3.0	AV_{CC}	V	
	AVRL	0.0	2.0	V	
Operating temperature	T_A	–40	+85	°C	

* : These values vary with the operating frequency and analog assurance range. See Figure 1, “5. A/D Converter Electrical Characteristics,” and “6. D/A Converter Electrical Characteristics.”



Note: The shaded area is assured only for the MB89643/645/646/647.

Figure 1 Operating Voltage vs. Main Clock Operating Frequency

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of $4/F_{CH}$.

Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

3. DC Characteristics

(AV_{CC} = DAVC = V_{CC} = +5.0 V, AV_{SS} = V_{SS} = 0.0 V, F_{CH} = 10 MHz, F_{CL} = 32.768 kHz, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage*1	V_{IH}	P00 to P07, P10 to P17, P22, P23	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, P30 to P37, P50, P51, P70 to P74, P80 to P83		0.8 V_{CC}	—	V_{CC} + 0.3	V	
		P52 to P57						With pull-up resistor
	V_{IHS2}	P52 to P57		0.8 V_{CC}	—	V_{SS} + 6.0	V	Without pull-up resistor
"L" level input voltage*1	V_{IL}	P00 to P07, P10 to P17, P22, P23		V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, P30 to P37, P50 to P57, P70 to P74, P80 to P83		V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P40 to P47		V_{SS} – 0.3	—	V_{SS} + 15.0	V	Without pull-up resistor
	V_{D2}	P52 to P57		V_{SS} – 0.3	—	V_{SS} + 6.0	V	Without pull-up resistor
	V_{D3}	P60 to P67		V_{SS} – 0.3	—	V_{CC} + 0.3	V	
		P40 to P47, P52 to P57						With pull-up resistor
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37	I_{OH} = –2.0 mA	2.4	—	—	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67	I_{OL} = +1.8 mA	—	—	0.4	V	
	V_{OL2}	$\overline{RST}$	I_{OL} = +4.0 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P74, P80 to P83, MOD0, MOD1	0.45 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor

(Continued)

(AV_{CC} = DAVC = V_{CC} = +5.0 V, AV_{SS} = V_{SS} = 0.0 V, F_{CH} = 10 MHz, F_{CL} = 32.768 kHz, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P64, P70 to P74, P80 to P83, $\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	Without pull-up resistor
Power supply current	I_{CC1}	V_{CC}	V_{CC} = +5.0 V • Main clock operation • High speed*2	—	10	20	mA	
				—	11	23	mA	MB89P647 only
	I_{CC2}		V_{CC} = +3.0 V • Main clock operation • Low speed*3	—	1.5	2	mA	
				—	2.5	5	mA	MB89P647 only
	I_{CS1}		V_{CC} = +5.0 V • Main clock sleep • High speed*2	—	3	7	mA	
	I_{CS2}		V_{CC} = +3.0 V • Main clock sleep • Low speed*3	—	1	1.5	mA	
	I_{CS3}		V_{CC} = +3.0 V Subclock sleep	—	25	50	µA	
	I_{CCH}		T_A = +25°C Subclock stop	—	—	10	µA	
	I_{CSB}		V_{CC} = +3.0 V Subclock operation (32.768 kHz)	—	50	100	µA	
				—	1	3	mA	MB89P647 only
Power supply current	I_{CCT}	V_{CC}	V_{CC} = +3.0 V Watch mode (32.768 kHz)	—	—	15	µA	
	I_A	AV_{CC}	• Main clock operation • High speed*2	—	1	3	mA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, and V_{SS}	f = 1 MHz	—	10	—	pF	

*1: Connect MOD0 and MOD1 to V_{CC} or V_{SS}.

*2: High-speed operation is the operation when the system clock is set to the maximum speed by the system clock select bit at 10-MHz clock.

*3: Low-speed operation is the operation when the system clock is set to the maximum speed by the system clock select bit at 10-MHz clock.

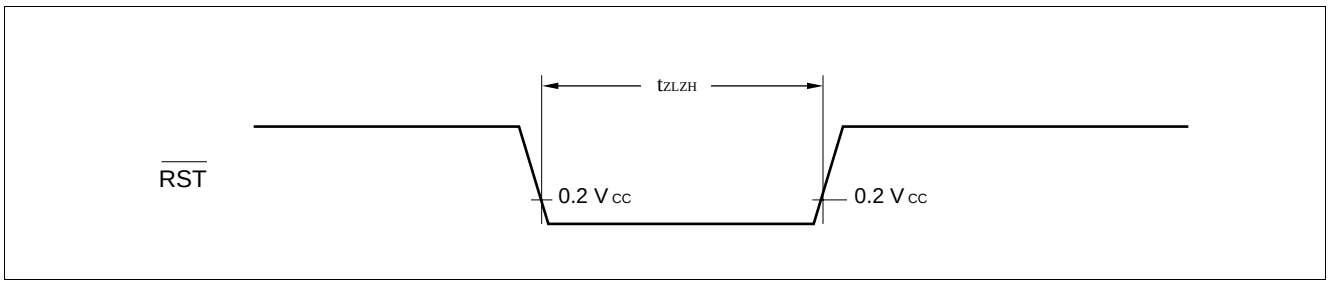
4. AC Characteristics

(1) Reset Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{XCYL}	—	ns	

* : t_{XCYL} is the oscillation cycle ($1/F_{CH}$) to input to the X0 pin.

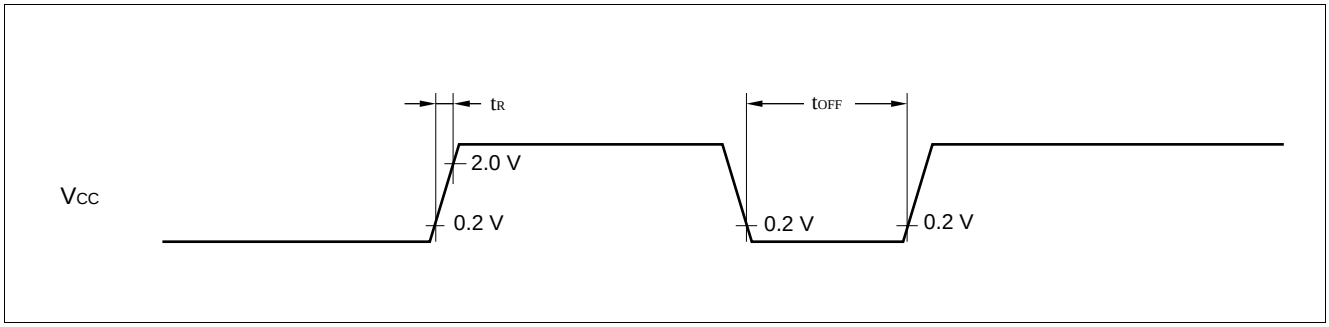


(2) Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operation

Note: Make sure that power supply rises within the selected oscillation stabilization time.
For example, when the main clock is operating at 10 MHz (F_{CH}) and the oscillation stabilization time select option has been set to $2^{14}/F_{CH}$, the oscillation stabilization delay time is 1.6 ms and accordingly the maximum value of power supply rising time is about 1.6 ms.
Keep in mind that abrupt changes in power supply voltage may cause a power-on reset. If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

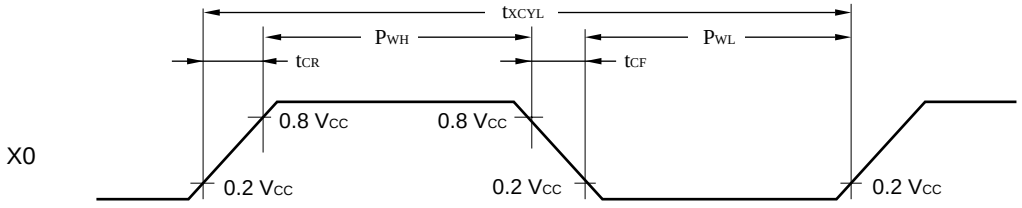


(3) Clock Timing

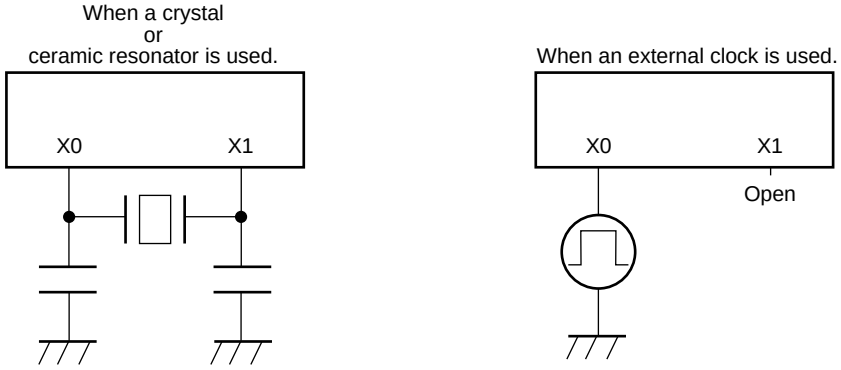
(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	—	1	—	10	MHz	
	F_{CL}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{XCYL}	X0, X1		100	—	1000	ns	
	t_{LXCYL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0		20	—	—	ns	External clock
	P_{WHL} P_{WLL}	X0A		—	30.5	—	µs	
Input clock rising/falling time	t_{CR} t_{CF}	X0		—	—	10	ns	External clock

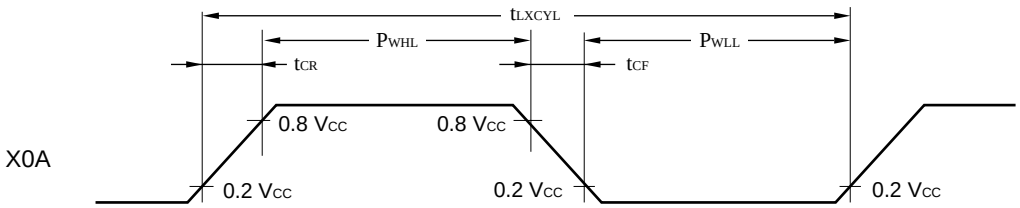
X0 and X1 Timing and Conditions



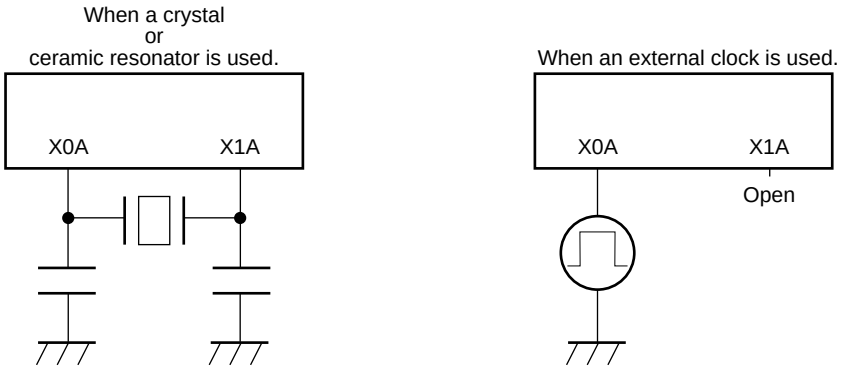
Main Clock Conditions



X0A and X1A Timing and Conditions



Subclock Conditions

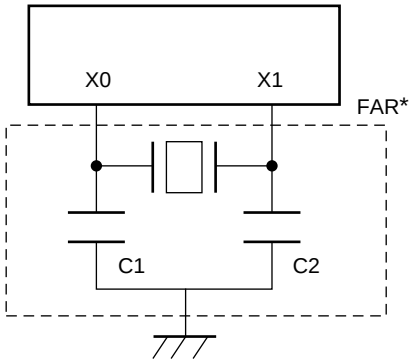


(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	4/F_{CH} system clock selection 11	µs	t_{inst} = 0.4 µs when operating at F_{CH} = 10 MHz
		8/F_{CH} system clock selection 10	µs	t_{inst} = 0.8 µs when operating at F_{CH} = 10 MHz
		16/F_{CH} system clock selection 01	µs	t_{inst} = 1.6 µs when operating at F_{CH} = 10 MHz
		64/F_{CH} system clock selection 00	µs	t_{inst} = 6.4 µs when operating at F_{CH} = 10 MHz

(5) Recommended Resonator Manufacturers

Sample Application of Piezoelectric Resonator (FAR series)

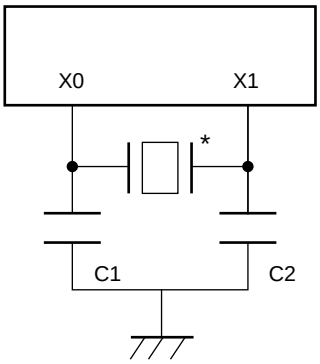


* : Fujitsu Acoustic Resonator
C1 = C2 = 20 pF±8 pF (built-in FAR)

FAR part number (built-in capacitor type)	Frequency	Initial deviation of FAR frequency (T_A = +25°C)	Temperature characteristic of FAR frequency (T_A = –20°C to +60°C)
FAR-C4CB-08000-M02	8.00 MHz	±0.5%	±0.5%
FAR-C4CB-10000-M02	10.00 MHz	±0.5%	±0.5%

Inquiry: FUJITSU LIMITED

Sample Application of Ceramic Resonator



Resonator manufacturer*	Resonator	Frequency	C1 (pF)	C2 (pF)	R (kΩ)
Kyocera Corporation	KBR-7.68MWS	7.68 MHz	33	33	—
	KBR-8.0MWS	8.0 MHz	33	33	—
Murata Mfg. Co., Ltd.	CSA8.00MTZ	8.0 MHz	30	30	—

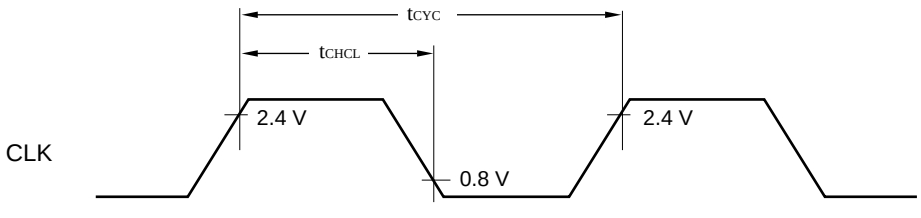
Inquiry: Kyocera Corporation
- AVX Corporation
  North American Sales Headquarters: TEL 1-803-448-9411
- AVX Limited
  European Sales Headquarters: TEL 44-1252-770000
- AVX/Kyocera H.K. Ltd.
  Asian Sales Headquarters: TEL 852-363-3303

Murata Mfg. Co., Ltd.
- Murata Electronics North America, Inc.: TEL 1-404-436-1300
- Murata Europe Management GmbH: TEL 49-911-66870
- Murata Electronics Singapore (Pte.) Ltd.: TEL 65-758-4233

(6) Clock Output Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	—	200	—	ns	t_{XCYL} × 2 at 10 MHz oscillation
CLK ↑→ CLK ↓	t_{CHCL}	CLK		30	100	ns	Approx. t_{CYL}/2 at 10 MHz oscillation

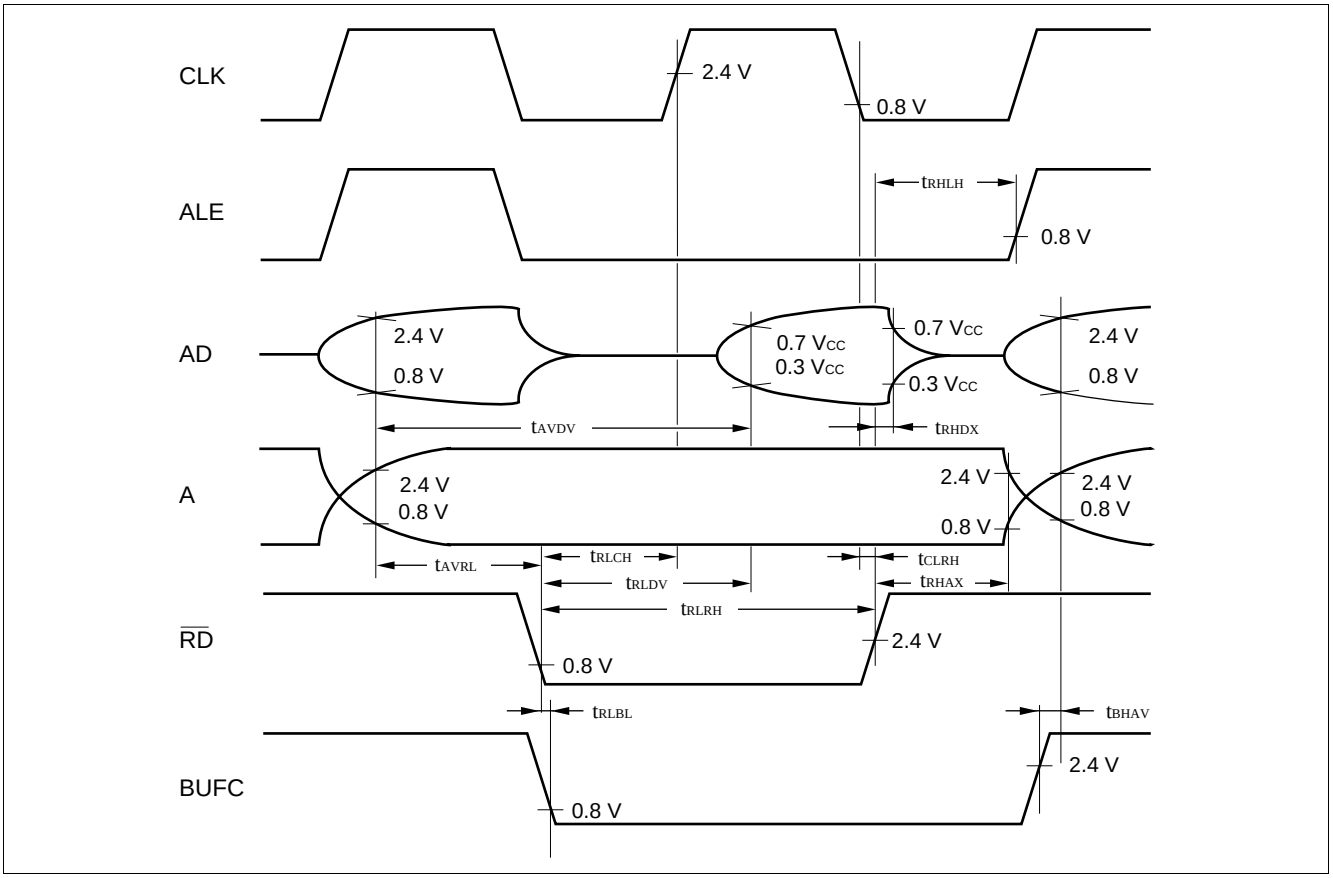


(7) Bus Read Timing

(V_{CC} = +5.0 V±10%, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	$\overline{RD}$, A15 to 08, AD7 to 0	—	1/4 t_{inst}* – 64 ns	—	ns	
$\overline{RD}$ pulse width	t_{RLRH}	RD		1/2 t_{inst}* – 20 ns	—	ns	
Valid address → read data time	t_{AVDV}	AD7 to 0, A15 to 08		1/2 t_{inst}*	200	ns	No wait
$\overline{RD}$ ↓ → read data time	t_{RLDV}	$\overline{RD}$, AD7 to 0		1/2 t_{inst}* – 80 ns	120	ns	No wait
$\overline{RD}$ ↑ → data hold time	t_{RHDX}	AD7 to 0, $\overline{RD}$		0	—	ns	
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		1/4 t_{inst}* – 40 ns	—	ns	
$\overline{RD}$ ↑ → address invalid time	t_{RHAX}	$\overline{RD}$, A15 to 08		1/4 t_{inst}* – 40 ns	—	ns	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		1/4 t_{inst}* – 40 ns	—	ns	
CLK ↓ → $\overline{RD}$ ↑ time	t_{CLRH}	$\overline{RD}$, CLK		0	—	ns	
$\overline{RD}$ ↓ → BUFC ↓ time	t_{RLBL}	$\overline{RD}$, BUFC		–5	—	ns	
BUFC ↑→ Valid address time	t_{BHAV}	A15 to 08, AD7 to 0, BUFC		5	—	ns	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



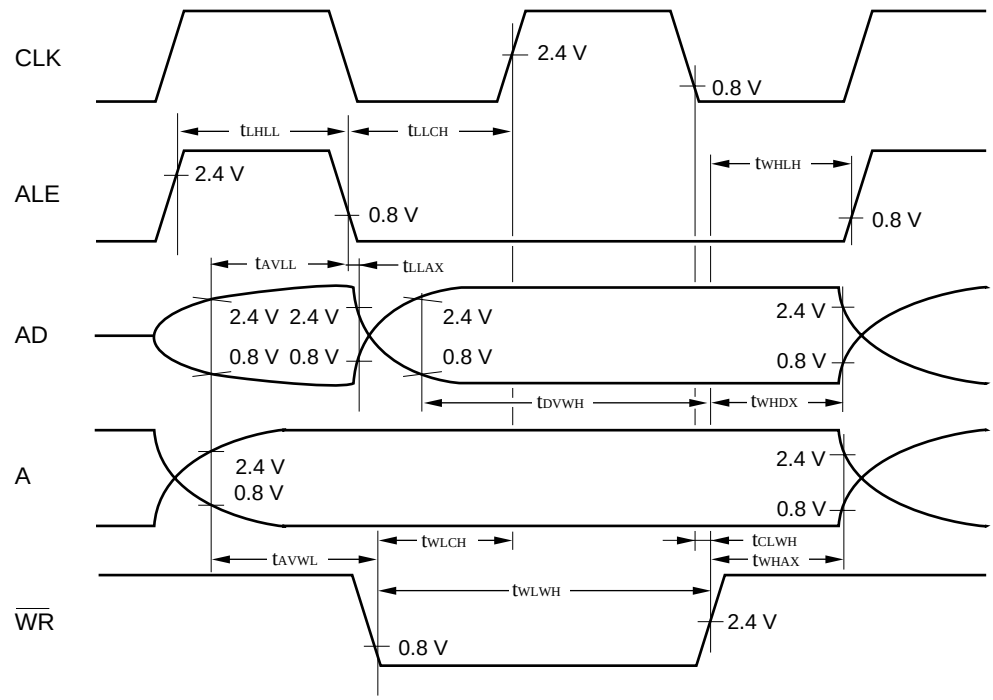
(8) Bus Write Timing

(V_{CC} = +5.0 V±10%, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid address → ALE ↓ time	t_{AVLL}	AD7 to 0, ALE, A15 to 08	—	1/4 t_{inst}*1 – 64 ns*2	—	ns	
ALE ↓ → address invalid time	t_{LLAX}	AD7 to 0, ALE, A15 to 08		5	—	ns	*2
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	$\overline{WR}$, ALE		1/4 t_{inst}*1 – 60 ns	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		1/2 t_{inst}*1 – 20 ns	—	ns	
Write data → $\overline{WR}$ ↑ time	t_{DVWH}	AD7 to 0, $\overline{WR}$		1/2 t_{inst}*1 – 60 ns	—	ns	
$\overline{WR}$ ↑ → address invalid time	t_{WHAX}	$\overline{WR}$, A15 to 08		1/4 t_{inst}*1 – 40 ns	—	ns	
$\overline{WR}$ ↑ → data hold time	t_{WHDX}	AD7 to 0, $\overline{WR}$		1/4 t_{inst}*1 – 40 ns	—	ns	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		1/4 t_{inst}*1 – 40 ns	—	ns	
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		1/4 t_{inst}*1 – 40 ns	—	ns	
CLK ↓ → $\overline{WR}$ ↑ time	t_{CLWH}	$\overline{WR}$, CLK		0	—	ns	
ALE pulse width	t_{LHLL}	ALE		1/4 t_{inst}*1 – 35 ns*2	—	ns	
ALE ↓ → CLK ↑ time	t_{LLCH}	ALE, CLK		1/4 t_{inst}*1 – 30 ns*2	—	ns	

*1: For information on t_{inst}, see “(4) Instruction Cycle.”

*2: These characteristics are also applicable to the bus read timing.

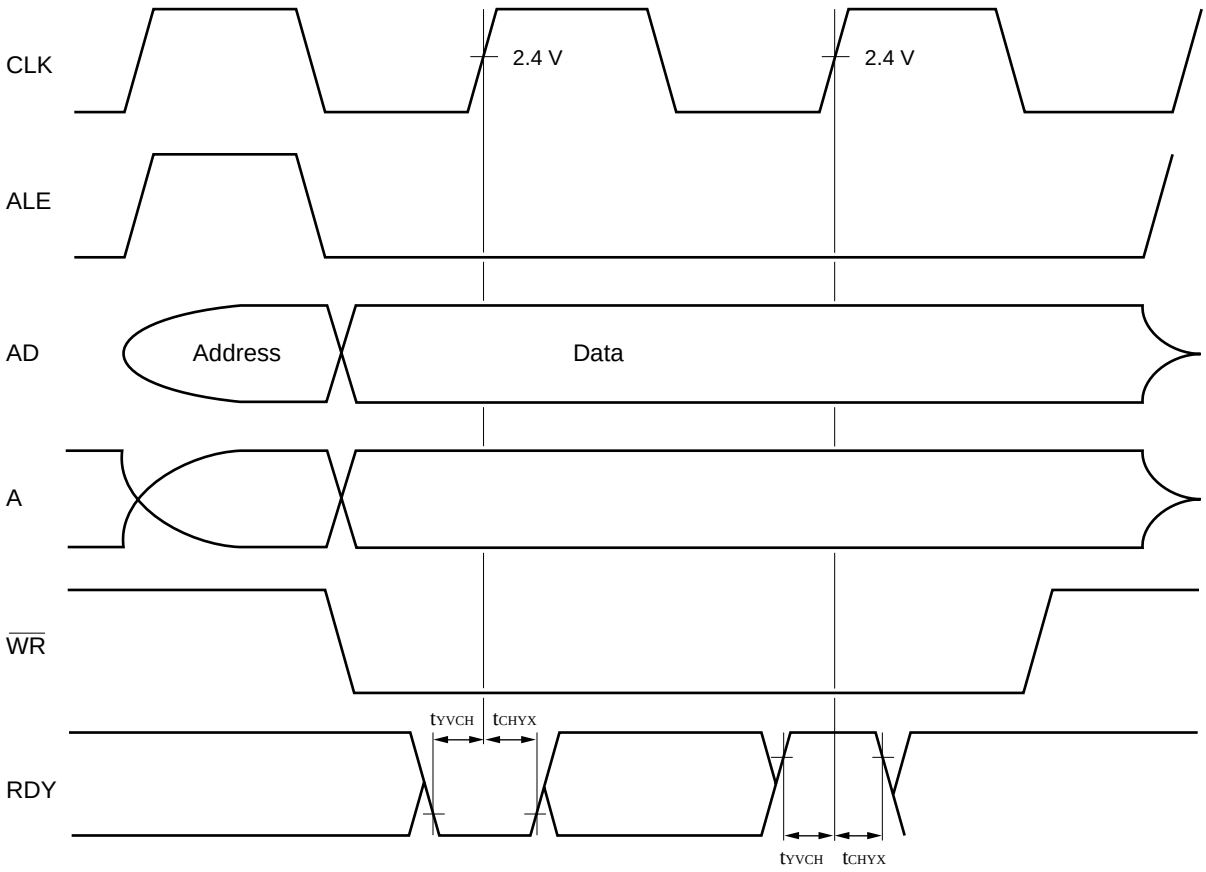


(9) Ready Input Timing

(V_{CC} = +5.0 V±10%, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY valid → CLK ↑ time	t_{YVCH}	RDY, CLK	—	60	—	ns	*
CLK ↑ → RDY invalid time	t_{CHYX}	RDY, CLK		0	—	ns	*

* : These characteristics are also applicable to the read cycle.



Note: The bus cycle is also extended in the read cycle in the same manner.

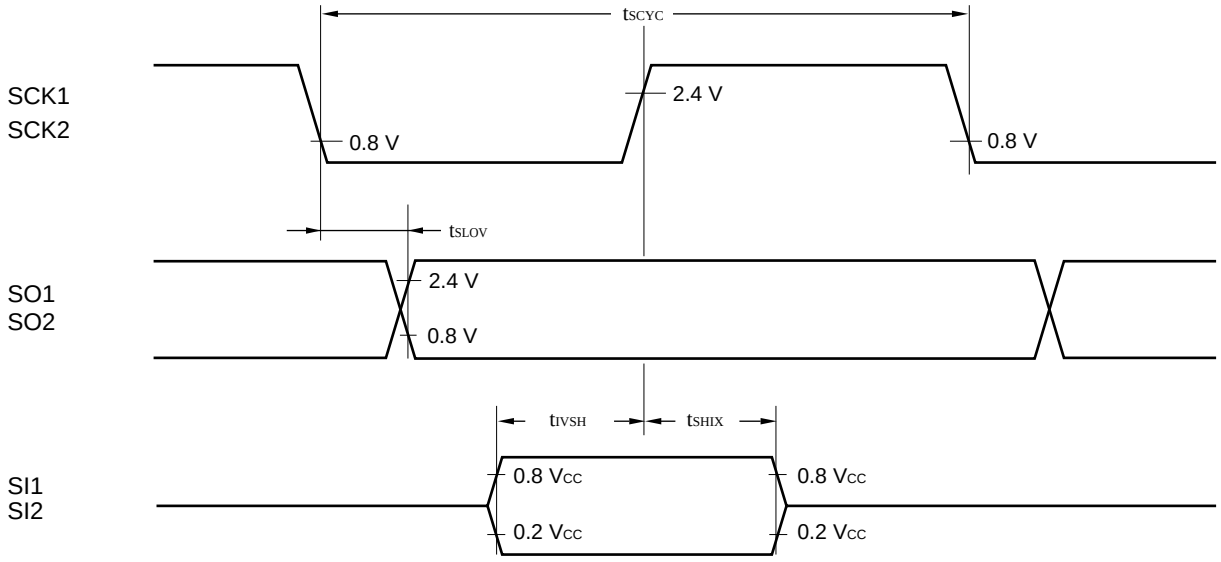
(10) Serial I/O Timing

(V_{CC} = +5.0 V±10%, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

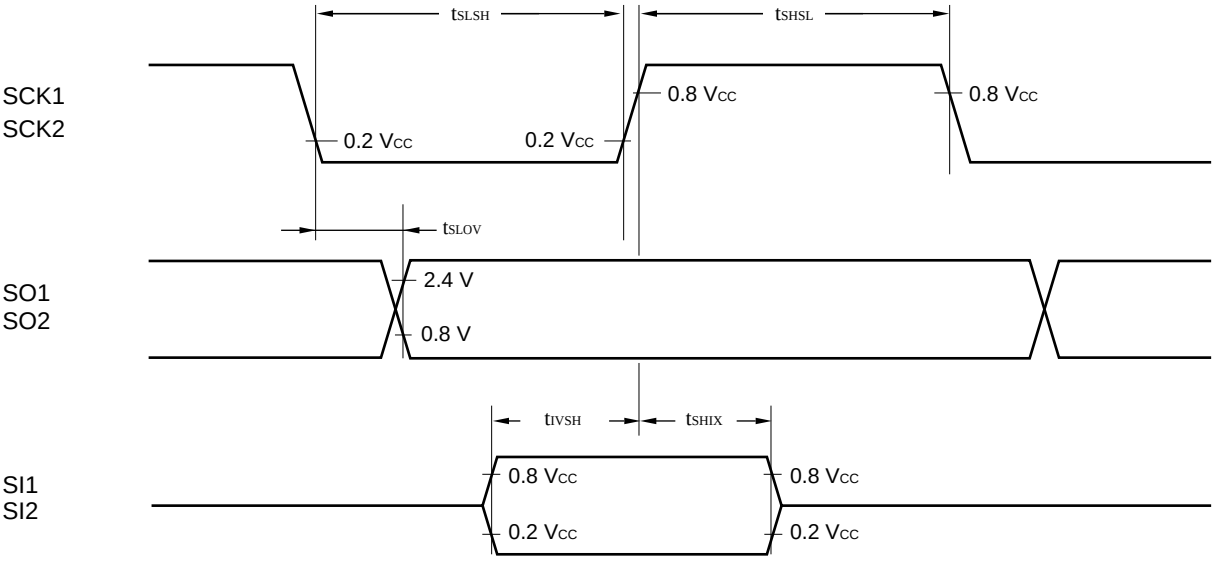
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK1, SCK2	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time SCK2 ↓ → SO2 time	t_{SLOV}	SCK1, SO1 SCK2, SO2		–200	200	ns	
Valid SI1 → SCK1 ↑ Valid SI2 → SCK2 ↑	t_{IVSH}	SI1, SCK1 SI2, SCK2		1/2 t_{inst}*	—	µs	
SCK1 ↑ → valid SI1 hold time SCK2 ↑ → valid SI2 hold time	t_{SHIX}	SCK1, SI1 SCK2, SI2		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK1, SCK2	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	SCK1, SCK2		1 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time SCK2 ↓ → SO2 time	t_{SLOV}	SCK1, SO1 SCK2, SO2		0	200	ns	
Valid SI1 → SCK1 ↑ Valid SI2 → SCK2 ↑	t_{IVSH}	SI1, SCK1 SI2, SCK2		1/2 t_{inst}*	—	µs	
SCK1 ↑ → valid SI1 hold time SCK2 ↑ → valid SI2 hold time	t_{SHIX}	SCK1, SI1 SCK2, SI2		1/2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

Internal Shift Clock Mode



External Shift Clock Mode

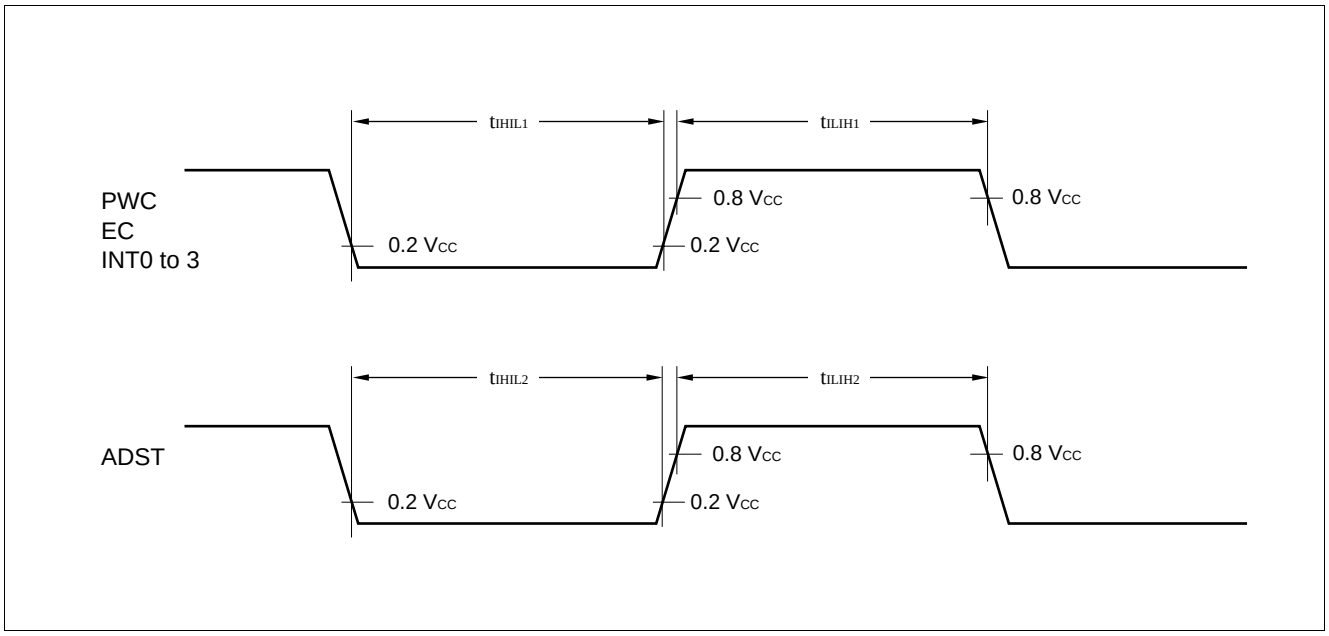


(11) Peripheral Input Timing

(V_{CC} = +5.0 V±10%, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Peripheral input pulse “H” width 1	t_{ILIH1}	PWC, EC, INT0 to INT3	—	2 t_{inst}*	—	µs	
Peripheral input pulse “L” width 1	t_{IHIL1}	PWC, EC, INT0 to INT3		2 t_{inst}*	—	µs	
Peripheral input pulse “H” width 2	t_{ILIH2}	ADST	A/D mode	32 t_{inst}*	—	µs	
Peripheral input pulse “L” width 2	t_{IHIL2}	ADST		32 t_{inst}*	—	µs	
Peripheral input pulse “H” width 2	t_{ILIH2}	ADST	Sense mode	8 t_{inst}*	—	µs	
Peripheral input pulse “L” width 2	t_{IHIL2}	ADST		8 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



5. A/D Converter Electrical Characteristics

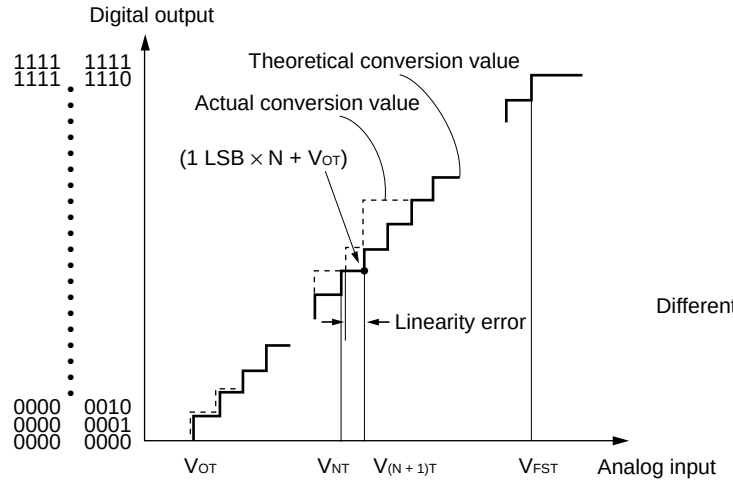
(AV_{CC} = V_{CC} = +3.5 V to +6.0 V, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = AVRL = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—	—	—	—	—	8	bit	
Total error			AVRH = AV_{CC}	—	—	±3.0	LSB	
Linearity error				—	—	±1.0	LSB	
Differential linearity error				—	—	±0.9	LSB	
Zero transition voltage	V_{OT}	—		–1.0	+0.5	+2.0	LSB	
Full-scale transition voltage	V_{FST}			AVRH – 4.5	AVRH – 1.5	AVRH + 1.5	LSB	
Interchannel disparity	—			—	—	0.5	LSB	
A/D mode conversion time			—	—	44	—	t_{inst}*	
Sense mode conversion time				—	12	—	t_{inst}*	
Analog port input current	I_{AIN}	AN0 to AN7		—	—	10	µA	
Analog input voltage	—			0	—	AVRH	V	
Reference voltage	—	AVRH		0	—	AV_{CC}	V	
Reference voltage supply current	I_R		When A/D conversion is activated AVRH = 5.0 V	—	100	—	µA	
	I_{RH}		When A/D conversion is stopped AVRH = 5.0 V	—	—	1	µA	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

(1) A/D Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter.
  When the number of bits is 8, analog voltage can be divided into $2^8 = 256$.
- Linearity error (unit: LSB)
  The deviation of the straight line connecting the zero transition point (“0000 0000” ↔ “0000 0001”) with the full-scale transition point (“1111 1111” ↔ “1111 1110”) from actual conversion characteristics
- Differential linearity error (unit: LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values



$$1\ \text{LSB} = \frac{\text{AVRH} - \text{AVRL}}{256}$$

$$\text{Linearity error} = \frac{V_{NT} - (1\ \text{LSB} \times N + V_{OT})}{1\ \text{LSB}}$$

$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

$$\text{Total error} = \frac{V_{NT} - (1\ \text{LSB} \times N + 1\ \text{LSB})}{1\ \text{LSB}}$$

(2) Precautions

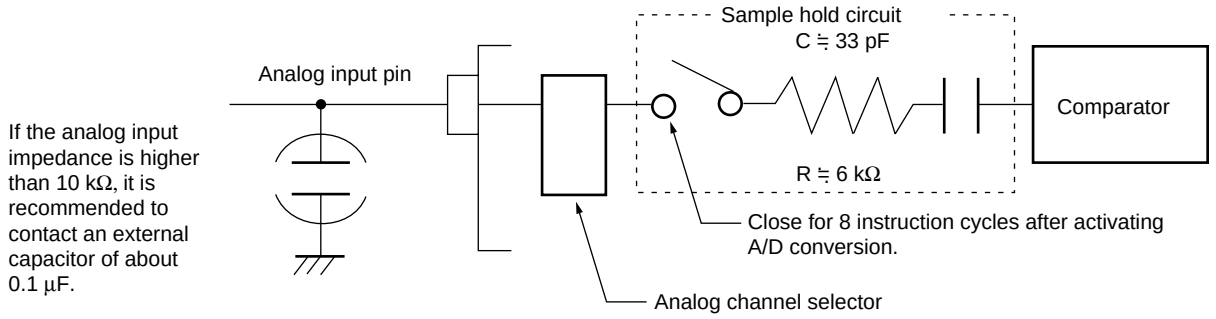
- **Input impedance of the analog input pins**

  The A/D converter used for the MB89640 series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for eight instruction cycles after activating A/D conversion.

  For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 10 kΩ).

  Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 μF for the analog input pin.

Analog Input Equivalent Circuit



- **Error**

  The smaller the | AVRH – AVRL |, the greater the error would become relatively.

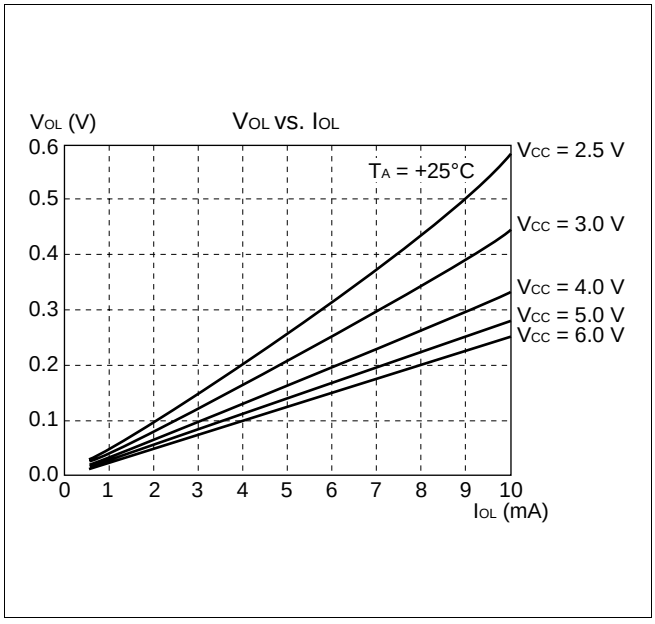
6. D/A Converter Electrical Characteristics

(DAVC = V_{CC} = +3.5 V to +6.0 V, F_{CH}=10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

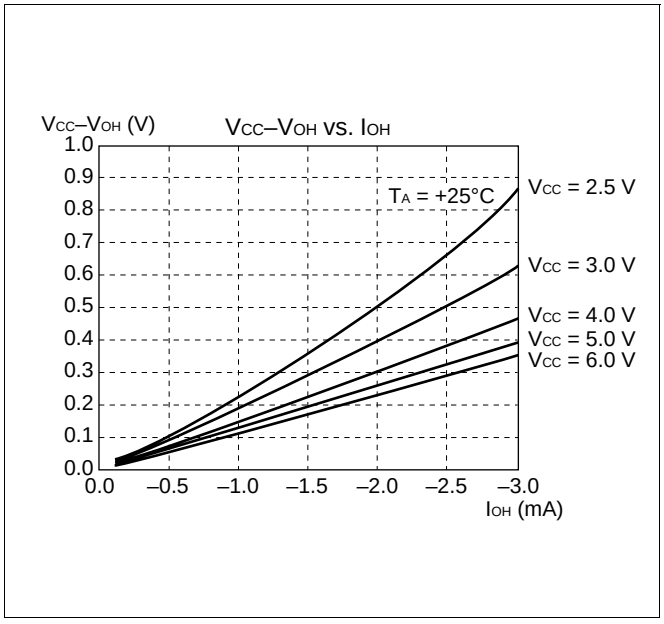
Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Resolution	—	—	—	8	bit	
Linearity error		—	—	±1.0	LSB	DAVC = V_{CC} = 5.0 V
Differential linearity error		—	—	±0.9	LSB	
Output impedance		—	20	—	kΩ	
D/A analog power supply current (for one channel)	I_{DINA}	—	0.1	—	mA	At no load and conversion cycle of 5 µs
	I_{DINS}	—	0.1	—	µA	During power down

■ EXAMPLES CHARACTERISTICS

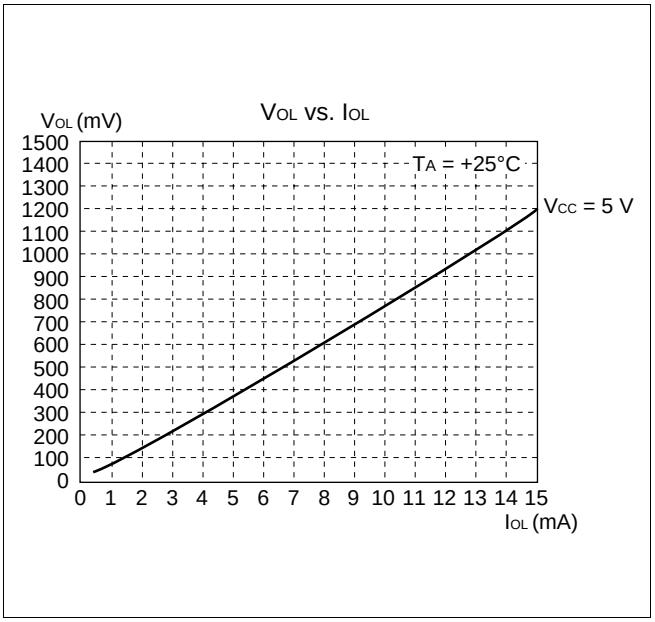
(1) “L” Level Output Voltage (P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P60 to P67)



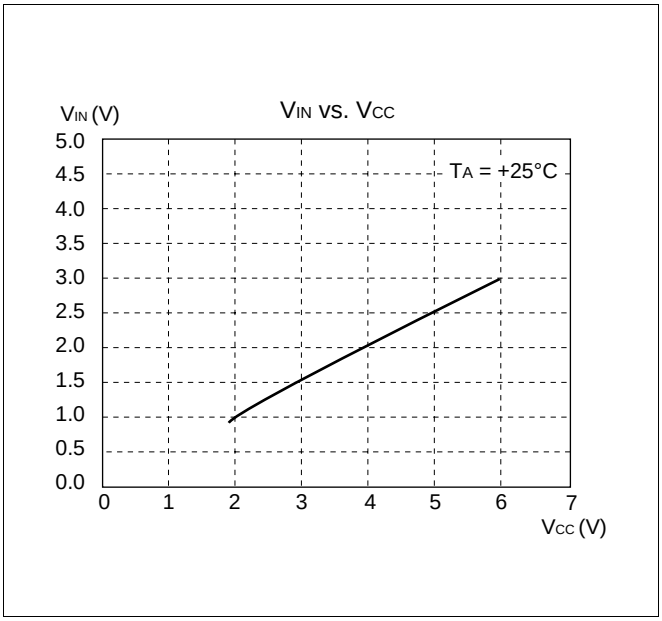
(2) “H” Level Output Voltage (P00 to P07, P10 to P17, P20 to P27, P30 to P37)



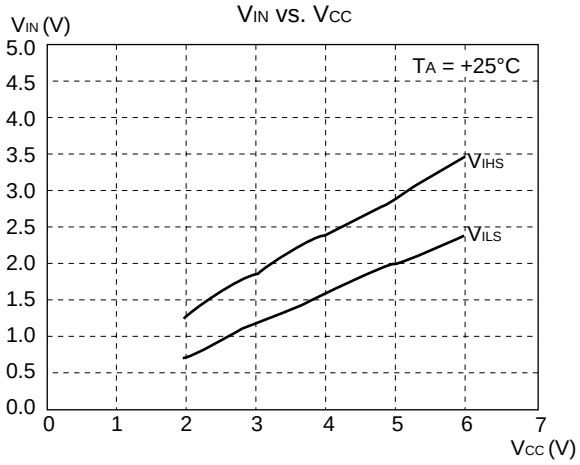
(3) “L” Level Output Voltage (P40 to P47)



(4) “H” Level Input Voltage/“L” Level Input Voltage (CMOS Input)

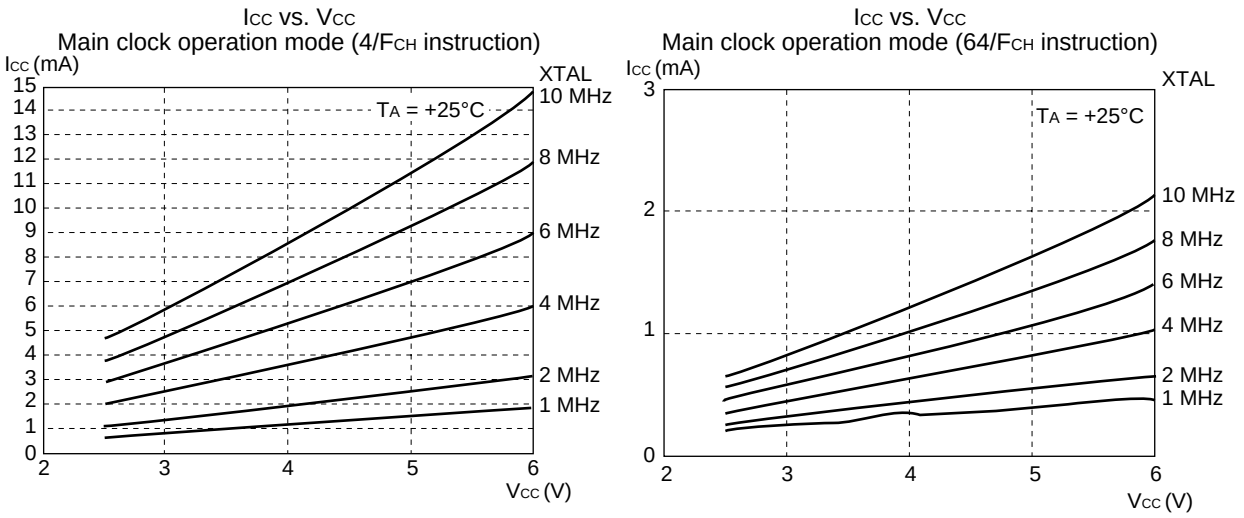


(5) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)



V_{IHS}: Threshold when input voltage in hysteresis characteristics is set to “H” level
V_{ILS}: Threshold when input voltage in hysteresis characteristics is set to “L” level

(6) Power Supply Current (External Clock)



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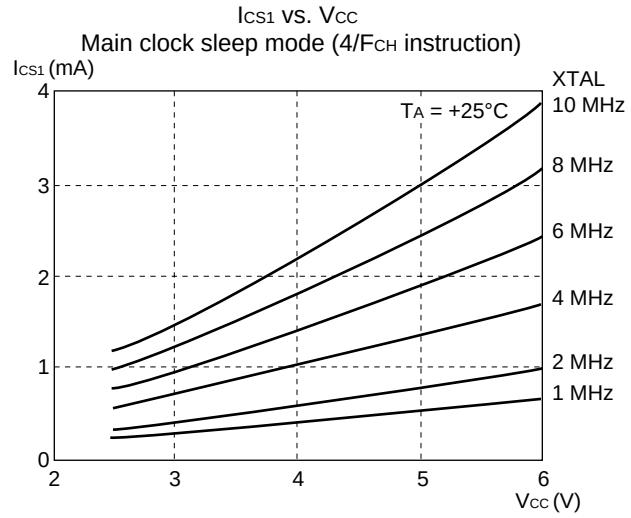
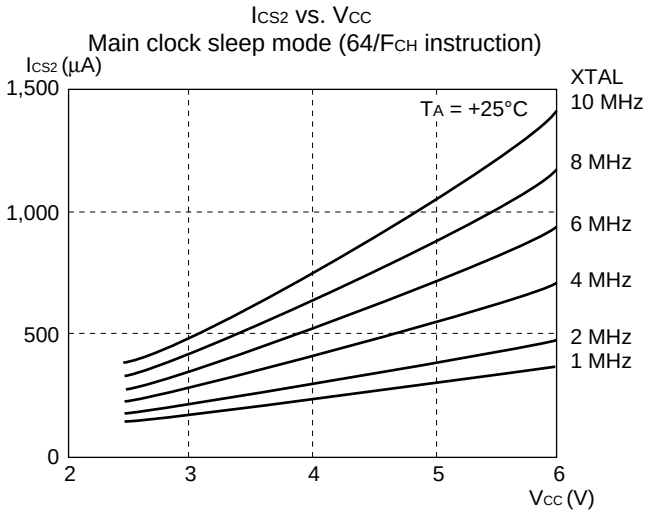
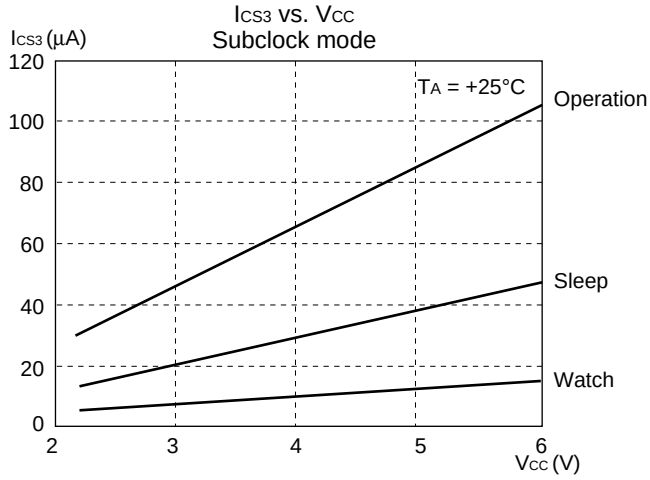
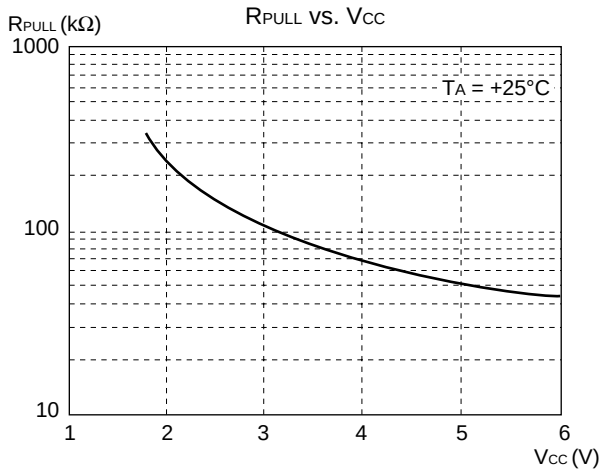






(7) Pull-up Resistance



■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A	–	–	–	+ + – +	03
ROLC A	2	1	C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

No.	Part number	MB89643 MB89645 MB89646 MB89647	MB89P647	MB89PV640
	Specifying procedure	Specify when ordering masking	Set with EPROM programmer	Setting not possible
1	Pull-up resistors P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P74, P80 to P83	Selectable per pin (P60 to P67 must be set to without a pull-up resistor when an A/D converter is used. P51 and P50 are must be set to without a pull-up resistor when a D/A converter is used.)	Can be set per pin (Only P40 to P47 and P50 to P57 are without a pull-up resistor.)	Fixed to without pull-up resistor
2	Power-on reset With power-on reset Without power-on reset	Selectable	Setting possible	Fixed to with power-on reset
3	Main clock oscillation stabilization time selection (when operating at 10 MHz) Approx. $2^{18}/F_{CH}$ (Approx. 26.2 ms) Approx. $2^{17}/F_{CH}$ (Approx. 13.1 ms) Approx. $2^{14}/F_{CH}$ (Approx. 1.6 ms) Approx. $2^{4}/F_{CH}$ (Approx. 0 ms) F_{CH}: Main clock frequency	Selectable	Setting possible	Fixed to approx. $2^{18}/F_{CH}$ (Approx. 26.2 ms)
4	Reset pin output With reset output Without reset output	Selectable	Setting possible	Fixed to with reset output
5	Selection either single- or dual-clock system Single clock Dual clock	Selectable	Setting possible	Fixed to dual-clock system

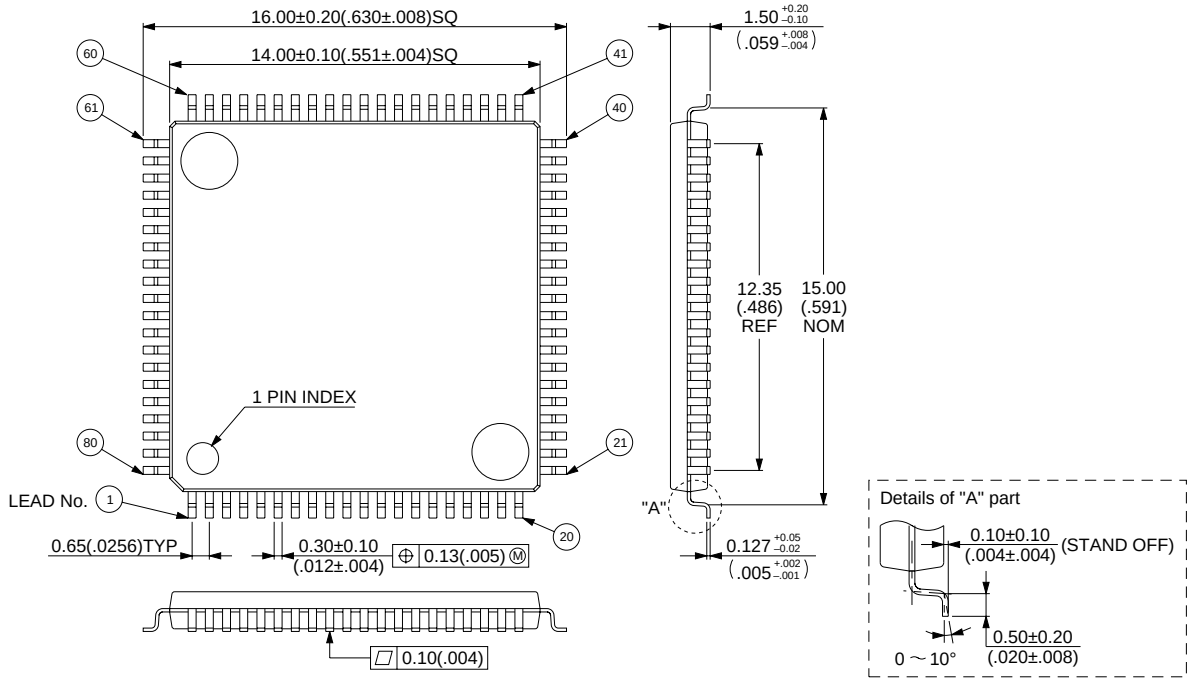
■ ORDERING INFORMATION

Part number	Package	Remarks
MB89647PFM MB89646PFM MB89645PFM MB89643PFM MB89P647PFM	80-pin Plastic QFP (FPT-80P-M11)	
MB89647PF MB89646PF MB89645PF MB89643PF MB89P647PF	80-pin Plastic QFP (FPT-80P-M06)	
MB89PV640CF	80-pin Ceramic MQFP (MQP-80C-P01)	

MB89640 Series

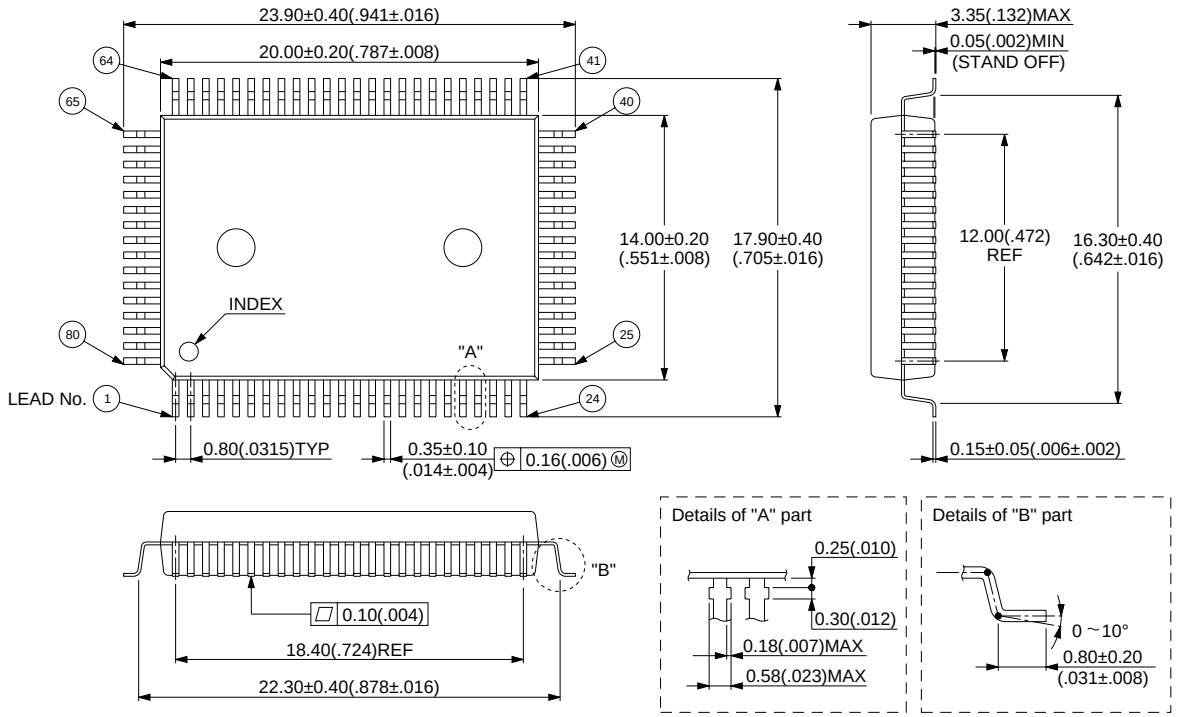
■ PACKAGE DIMENSIONS

80-pin Plastic QFP
(FPT-80P-M11)



Dimensions in mm (inches)

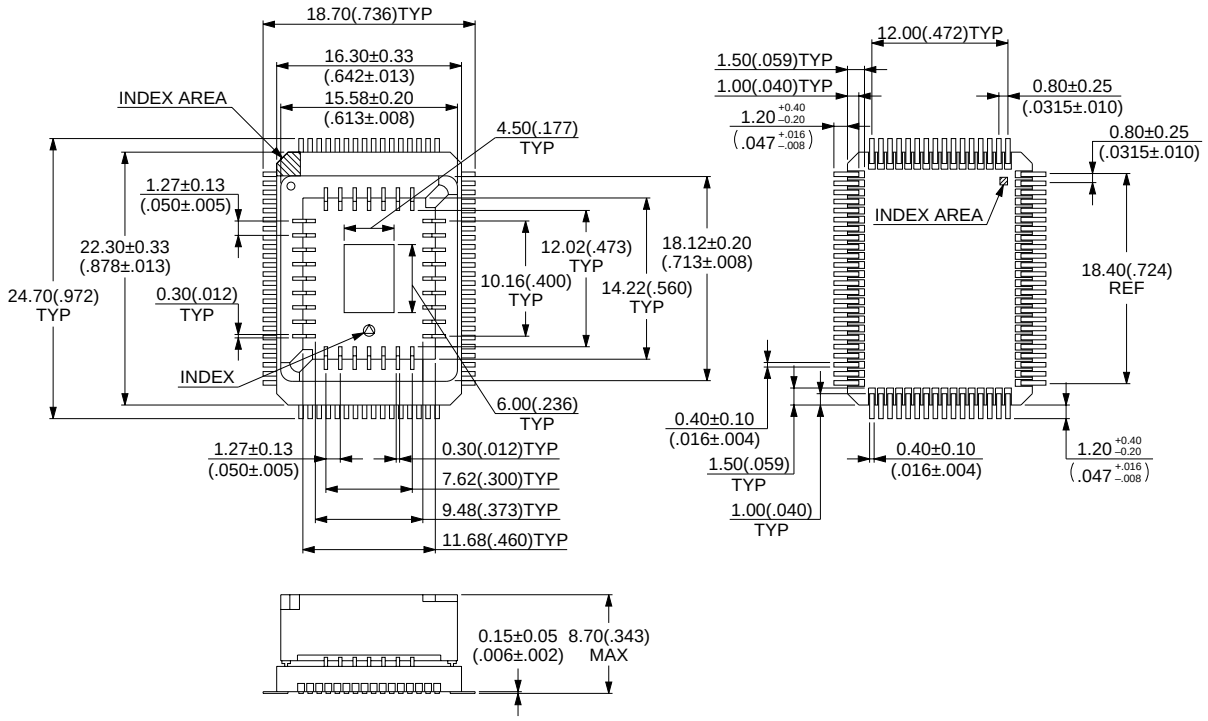
80-pin Plastic QFP
(FPT-80P-M06)



Dimensions in mm (inches)

MB89640 Series

80-pin Ceramic MQFP
(MQP-80C-P01)



Dimensions in mm (inches)

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