**FUJITSU SEMICONDUCTOR
DATA SHEET**

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89150/150A Series

MB89151/151A/152/152A/153/153A/154/154A/155/155A MB89P155/PV150

■ DESCRIPTION

The MB89150/A series has been developed as general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the MB89150 series microcontrollers contain a variety of peripheral functions such as dual-clock control system, five operating speed control stages, timers, a serial interface, a remote control transmission output, external interrupts, an LCD controller/driver, an LCD booster, and a watch prescaler.
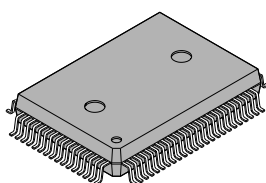
*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- F²MC-8L family CPU core
- Dual-clock system
- High-speed processing at low voltage
- Minimum execution time: 0.95 µs/2.7 V, 1.33 µs/2.2 V
- I/O ports: max. 43 channels
- 21-bit time-base timer
- 8/16-bit timer/counter: 1 channel (8 bits × 2 channels)
- 8-bit serial I/O: 1 channel
- LCD controller/driver: Max. 36 segments × 4 commons (built-in booster)
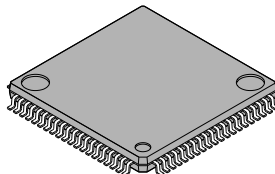- Remote control transmission output

(Continued)

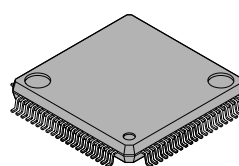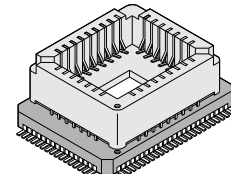### ■ PACKAGE

80-pin Plastic QFP	80-pin Plastic LQFP	80-pin Plastic LQFP	80-pin Ceramic MQFP
(FPT-80P-M06)	(FPT-80P-M11)	(FPT-80P-M05)	(MQP-80C-P01)

MB89150/150A Series

(Continued)
- Buzzer output
- Watch prescaler (15 bits)
- External interrupts (wake-up function)
  Four independent channels with edge detection function plus eight level-interrupt channels

■ PRODUCT LINEUP

Part number / Parameter	MB89151/A	MB89152/A	MB89153/A	MB89154/A	MB89155/A	MB89P155	MB89PV150
Classification	Mass production products (mask ROM products)					One-time PROM product	Piggyback/ evaluation product (for evaluation and development)
ROM size	4 K × 8 bits (internal mask ROM)	6 K × 8 bits (internal mask ROM)	8 K × 8 bits (internal mask ROM)	12 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal PROM, programming with general-purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	128 × 8 bits	256 × 8 bits					512 × 8 bits
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.95 µs/4.2 MHz Interrupt processing time: 8.57 µs/4.2 MHz						
Ports	I/O port (N-ch open-drain): 8 (6 ports also serve as peripherals, 3 ports are a high-current drive type.) Output port (N-ch open-drain): 18 (16 ports also serve as segment pins, 2 ports serve as boost capacitor connection pins.)[*1] I/O port (CMOS): 16 (12 ports also serve as an external interrupt.) Output port (CMOS): 1 (Also serves as a remote control.) Total: 43 (max.)						
Timer/counter	8-bit timer counter × 2 channel or 16-bit event counter × 1 channel						
8-bit serial I/O	8 bits LSB first/MSB first selectability						
LCD controller/ driver	Common output: 4 Segment output: 32 (max.)[*1] Bias power supply pins: 4 LCD display RAM size: 36 × 4 bits Booster for LCD driving: Built-in[*1] Dividing resistor for LCD driving: Built-in (an external resistor selectability)						No reference voltage generator and booster for LCD driving
External interrupts (wake-up function)	4 (edge selectability) 8 (level interrupt only)						
Buzzer output	1 (7 frequencies are selectable by the software.)						

(Continued)

Part number Parameter	MB89151/A	MB89152/A	MB89153/A	MB89154/A	MB89155/A	MB89P155	MB89PV150
Remote control transmission output	1 (Pulse width and cycle are software selectable.)						
Standby modes	Sleep mode, stop mode, and watch mode						
Process	CMOS						
Operating voltage[2]	2.2 V to 6.0 V (single clock)/2.2 V to 4.0 V (dual clock)					2.7 V to 6.0 V	
EPROM for use							MBM27C256A-20TV (LCC package)

*1: Selected by the mask option. See section "■ Mask Options."
*2: Varies with conditions such as the operating frequency and the connected ICE. (See section "■ Electrical Characteristics.")

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89151/A MB89152/A MB89153/A MB89154/A MB89155/A	MB89P155	MB89PV150
FPT-80P-M06	○	○	×
FPT-80P-M11	○	○	×
FPT-80P-M05	○	○	×
MQP-80C-P01	×	×	○

○ : Available   × : Not available

Note: For more information about each package, see section "■ Package Dimensions."

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MB89150/150A Series

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89151/A, addresses 0140$_H$ and later of the register bank cannot be used. On the MB89152/A, 153/A, 154/A, 155/A, and MB89P155, addresses 0180$_H$ and later of each register bank cannot be used.

- On the MB89P155, addresses BFF0$_H$ to BFF6$_H$ comprise the option setting area, option settings can be read by reading these addresses.

- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

- In the case of the MB89PV150, add the current consumed by the EPROM which is connected to the top socket.

- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

  However, the current consumption in sleep/stop modes is the same. (For more information, see sections "■ Electrical Characteristics" and "■ Example Characteristics.")

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.
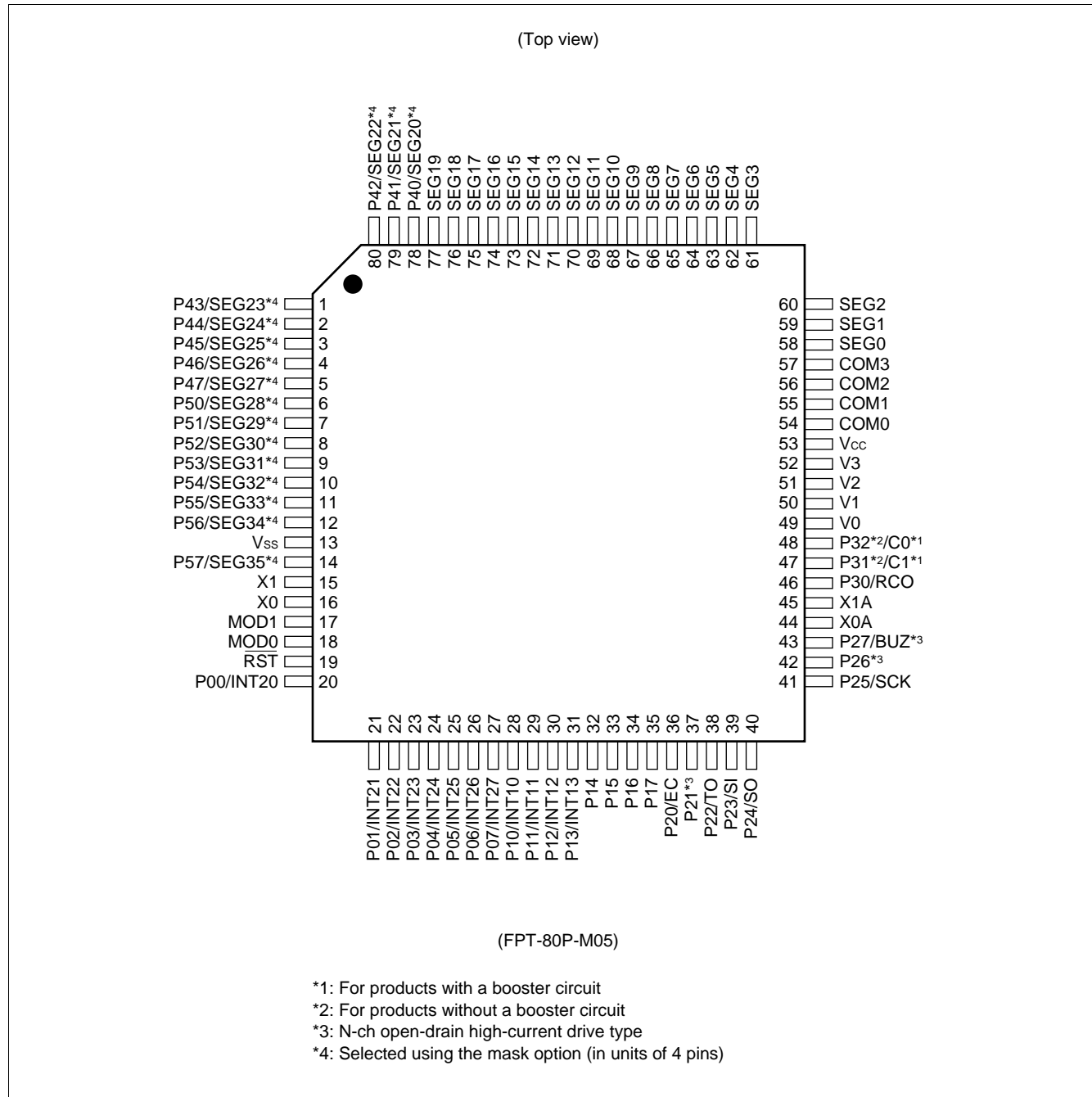
Before using options check section "■ Mask Options."

Take particular care on the following point:

- On the MB89PV150, options are fixed, except for the segment output selection.
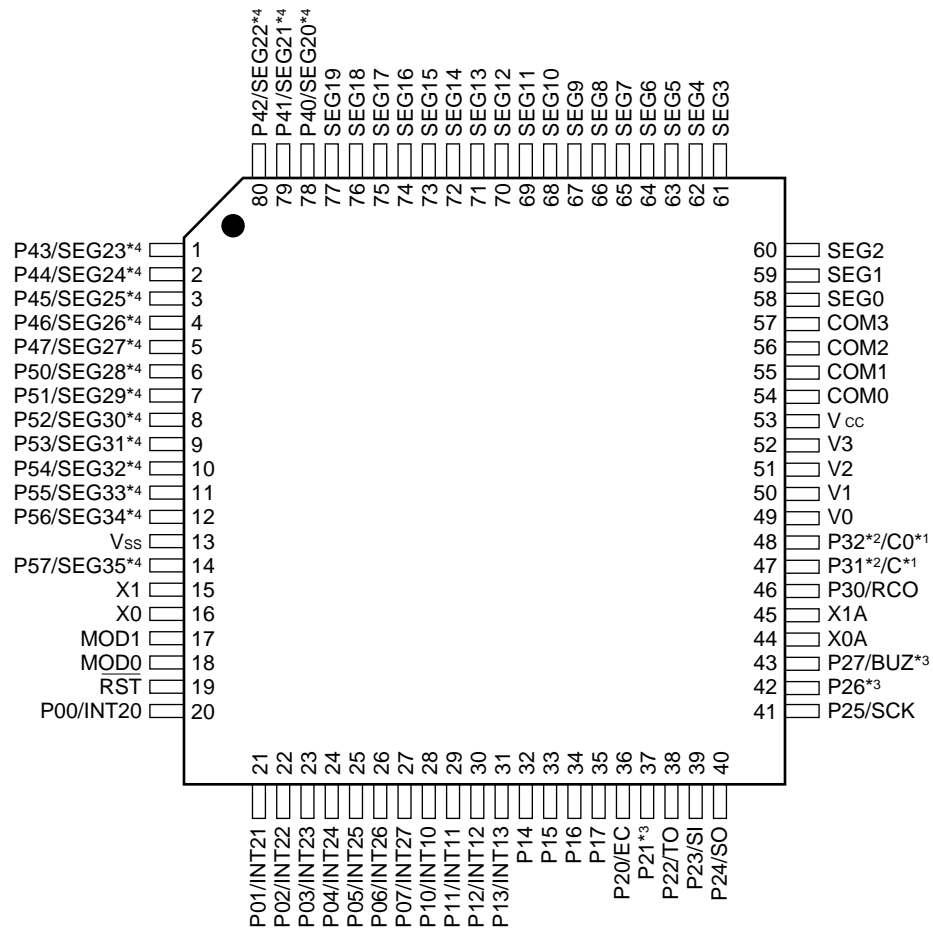
MB89150/150A Series

■ PIN ASSIGNMENT

(Top view)

Top pins (80–61): P42/SEG22*4, P41/SEG21*4, P40/SEG20*4, SEG19, SEG18, SEG17, SEG16, SEG15, SEG14, SEG13, SEG12, SEG11, SEG10, SEG9, SEG8, SEG7, SEG6, SEG5, SEG4, SEG3

Left pins (1–20):
P43/SEG23*4	1
P44/SEG24*4	2
P45/SEG25*4	3
P46/SEG26*4	4
P47/SEG27*4	5
P50/SEG28*4	6
P51/SEG29*4	7
P52/SEG30*4	8
P53/SEG31*4	9
P54/SEG32*4	10
P55/SEG33*4	11
P56/SEG34*4	12
Vss	13
P57/SEG35*4	14
X1	15
X0	16
MOD1	17
MOD0	18
RST	19
P00/INT20	20

Right pins (60–41):
60	SEG2
59	SEG1
58	SEG0
57	COM3
56	COM2
55	COM1
54	COM0
53	V_{CC}
52	V3
51	V2
50	V1
49	V0
48	P32*2/C0*1
47	P31*2/C1*1
46	P30/RCO
45	X1A
44	X0A
43	P27/BUZ*3
42	P26*3
41	P25/SCK

Bottom pins (21–40): P01/INT21, P02/INT22, P03/INT23, P04/INT24, P05/INT25, P06/INT26, P07/INT27, P10/INT10, P11/INT11, P12/INT12, P13/INT13, P14, P15, P16, P17, P20/EC, P21*3, P22/TO, P23/SI, P24/SO
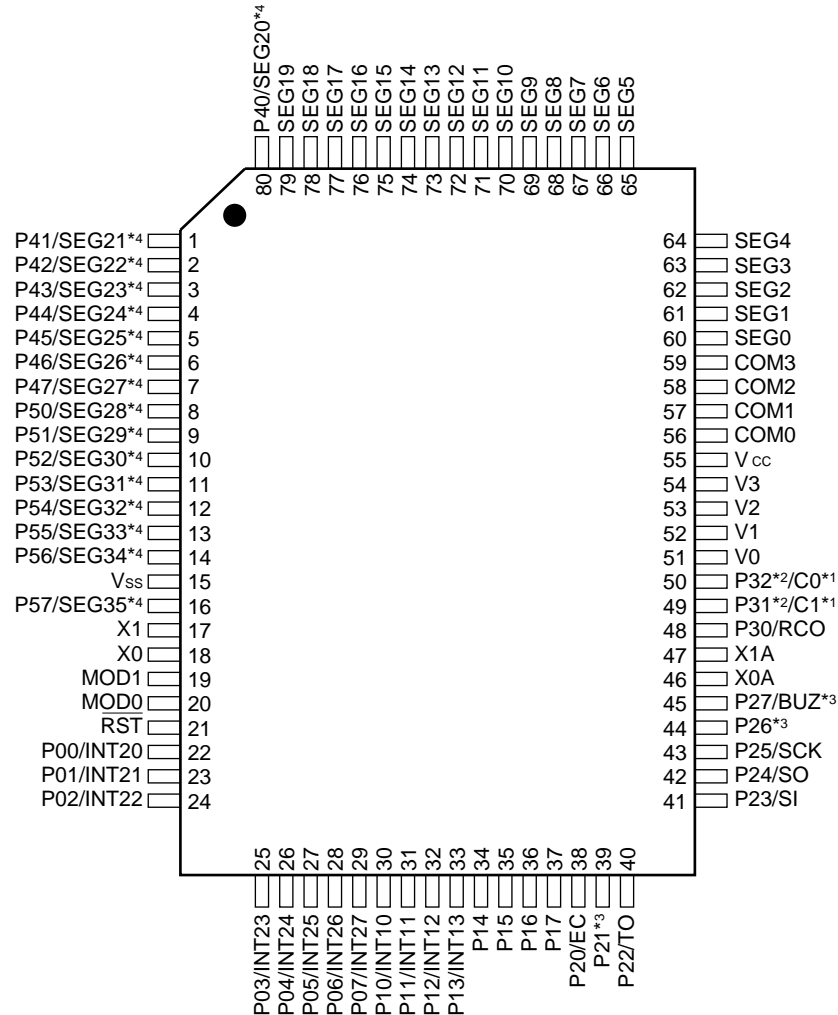
(FPT-80P-M05)

*1: For products with a booster circuit
*2: For products without a booster circuit
*3: N-ch open-drain high-current drive type
*4: Selected using the mask option (in units of 4 pins)

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MB89150/150A Series

(Top view)

(FPT-80P-M11)

*1: For products with a booster circuit
*2: For products without a booster circuit
*3: N-ch open-drain high-current drive type
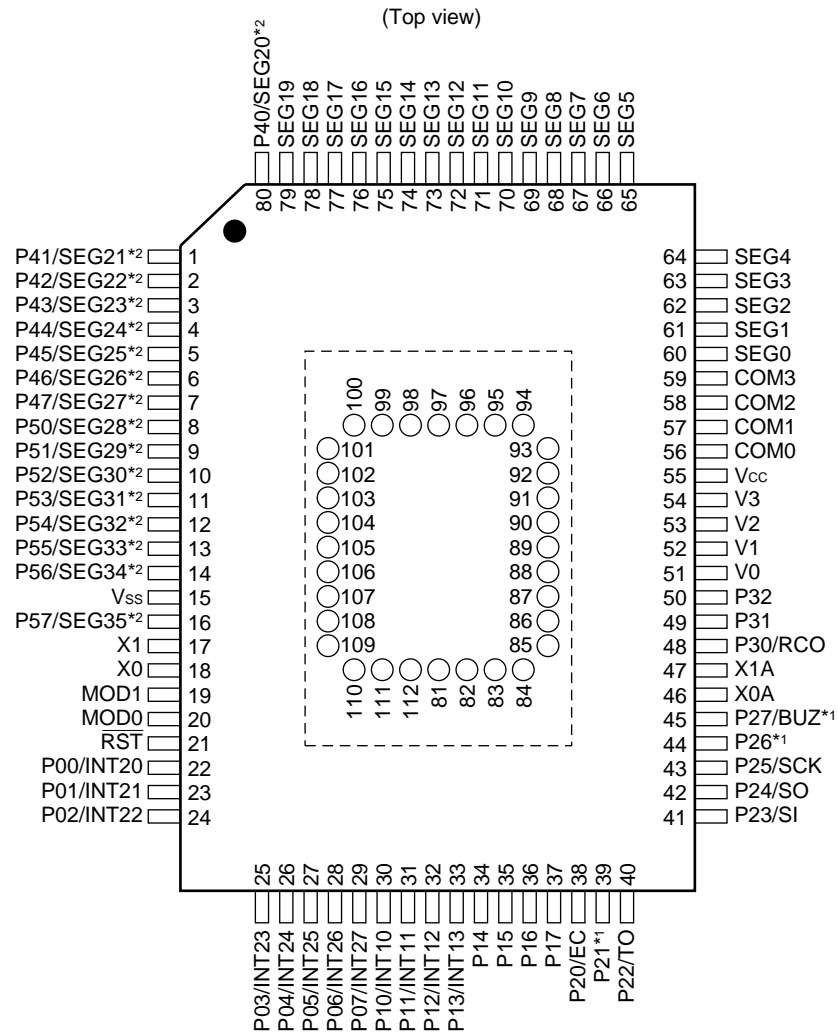*4: Selected using the mask option (in units of 4 pins)

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MB89150/150A Series

(Top view)

Left side pins:
- 1 P41/SEG21*4
- 2 P42/SEG22*4
- 3 P43/SEG23*4
- 4 P44/SEG24*4
- 5 P45/SEG25*4
- 6 P46/SEG26*4
- 7 P47/SEG27*4
- 8 P50/SEG28*4
- 9 P51/SEG29*4
- 10 P52/SEG30*4
- 11 P53/SEG31*4
- 12 P54/SEG32*4
- 13 P55/SEG33*4
- 14 P56/SEG34*4
- 15 Vss
- 16 P57/SEG35*4
- 17 X1
- 18 X0
- 19 MOD1
- 20 MOD0
- 21 RST
- 22 P00/INT20
- 23 P01/INT21
- 24 P02/INT22

Right side pins:
- 64 SEG4
- 63 SEG3
- 62 SEG2
- 61 SEG1
- 60 SEG0
- 59 COM3
- 58 COM2
- 57 COM1
- 56 COM0
- 55 V CC
- 54 V3
- 53 V2
- 52 V1
- 51 V0
- 50 P32*2/C0*1
- 49 P31*2/C1*1
- 48 P30/RCO
- 47 X1A
- 46 X0A
- 45 P27/BUZ*3
- 44 P26*3
- 43 P25/SCK
- 42 P24/SO
- 41 P23/SI

Top pins:
- 80 P40/SEG20*4
- 79 SEG19
- 78 SEG18
- 77 SEG17
- 76 SEG16
- 75 SEG15
- 74 SEG14
- 73 SEG13
- 72 SEG12
- 71 SEG11
- 70 SEG10
- 69 SEG9
- 68 SEG8
- 67 SEG7
- 66 SEG6
- 65 SEG5

Bottom pins:
- 25 P03/INT23
- 26 P04/INT24
- 27 P05/INT25
- 28 P06/INT26
- 29 P07/INT27
- 30 P10/INT10
- 31 P11/INT11
- 32 P12/INT12
- 33 P13/INT13
- 34 P14
- 35 P15
- 36 P16
- 37 P17
- 38 P20/EC
- 39 P21*3
- 40 P22/TO

(FPT-80P-M06)

*1: For products with a booster circuit
*2: For products without a booster circuit
*3: N-ch open-drain high-current drive type
*4: Selected using the mask option (in units of 4 pins)

MB89150/150A Series

(Top view)

(MQP-80C-P01)

*1: N-ch open-drain high-current drive type
*2: Selected using the mask option (in units of 4 pins).

• **Pin assignment on package top**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
81	N.C.	89	A2	97	N.C.	105	$\overline{OE}$
82	V_{PP}	90	A1	98	O4	106	N.C.
83	A12	91	A0	99	O5	107	A11
84	A7	92	N.C.	100	O6	108	A9
85	A6	93	O1	101	O7	109	A8
86	A5	94	O2	102	O8	110	A13
87	A4	95	O3	103	$\overline{CE}$	111	A14
88	A3	96	V_{SS}	104	A10	112	V_{CC}

N.C.: Internally connected. Do not use.

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MB89150/150A Series

■ **PIN DESCRIPTION**

Pin no.		Pin name	Circuit type	Function
LQFP[*1][*3]	MQFP[*4] QFP[*2]			
16	18	X0	A	Main clock oscillator pins
15	17	X1		
18	20	MOD0	C	Operating mode selection pins Connect directly to V_{SS}.
17	19	MOD1		
19	21	$\overline{\text{RST}}$	D	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor and a hysteresis input type. "L" is output from this pin by an internal reset source. The internal circuit is initialized by the input of "L".
20 to 27	22 to 29	P00/INT20 to P07/INT27	E	General-purpose I/O ports Also serve as an external interrupt 2 input (wake-up function). External interrupt 2 input is hysteresis input.
28 to 31	30 to 33	P10/INT10 to P13/INT13	E	General-purpose I/O ports Also serve as external interrupt 1 input. External interrupt 1 input is hysteresis input.
32 to 35	34 to 37	P14 to P17	F	General-purpose I/O ports
36	38	P20/EC	H	N-ch open-drain general-purpose I/O port Also serves as the external clock input for the timer. The peripheral is a hysteresis input type.
37	39	P21	I	N-ch open-drain general-purpose I/O port
38	40	P22/TO	I	N-ch open-drain general-purpose I/O port Also serves as a timer output.
39	41	P23/SI	H	N-ch open-drain general-purpose I/O port Also serves as the data input for the 8-bit serial I/O. The peripheral is a hysteresis input type.
40	42	P24/SO	I	N-ch open-drain general-purpose I/O port Also serves as the data output for the 8-bit serial I/O.
41	43	P25/SCK	H	N-ch open-drain general-purpose I/O port Also serves as the clock I/O for the 8-bit serial I/O. The peripheral is a hysteresis input type.
42	44	P26	I	N-ch open-drain general-purpose I/O port
43	45	P27/BUZ	I	N-ch open-drain general-purpose I/O port Also serves as a buzzer output.

*1: FPT-80P-M11
*2: FPT-80P-M06
*3: FPT-80P-M05
*4: MQP-80C-P01

(Continued)

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MB89150/150A Series

(Continued)

Pin no.		Pin name	Circuit type	Function
LQFP[*1][*3]	**MQFP**[*4] **QFP**[*2]			
48	50	P32	J	Functions as an N-ch open-drain general-purpose output port only in the products without a booster.
		C0	—	Functions as a capacitor connection pin in the products with a booster.
47	49	P31	J	Functions as an N-ch open-drain general-purpose output port only in the products without a booster.
		C1	—	Functions as a capacitor connection pin in the products with a booster.
46	48	P30/RCO	G	General-purpose output-only port Also serves as a remote control transmission output.
14	16	P57/SEG35	J/K	N-ch open-drain general-purpose output ports Also serve as LCD controller/driver segment output. Switching between port and common output is done by the mask option.
12 to 6	14 to 8	P56/SEG34 to P50/SEG28		
5 to 1	7 to 3	P47/SEG27 to P43/SEG23	J/K	
80, 79, 78	2, 1, 80	P42/SEG22, P41/SEG21, P40/SEG20		
77 to 58	79 to 60	SEG19 to SEG0	K	LCD controller/driver segment output-only pins
57 to 54	59 to 56	COM3 to COM0	K	LCD controller/driver common output-only pins
52 to 49	54 to 51	V3 to V0	—	LCD driving power supply pins
44	46	X0A	B	Subclock crystal oscillator pins (32.768 kHz)
45	47	X1A		
53	55	V_{CC}	—	Power supply pin
13	15	V_{SS}	—	Power supply (GND) pin

*1: FPT-80P-M11
*2: FPT-80P-M06
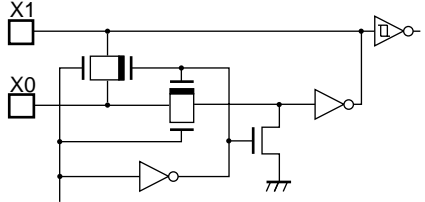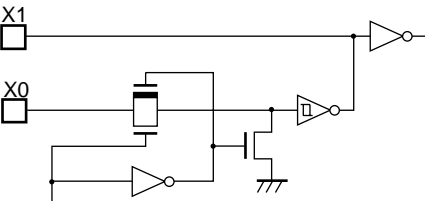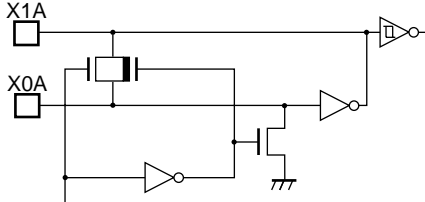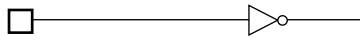*3: FPT-80P-M05
*4: MQP-80C-P01
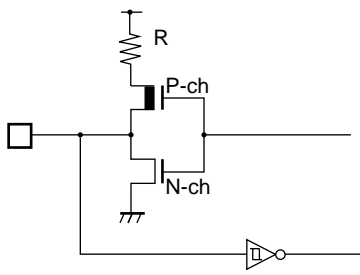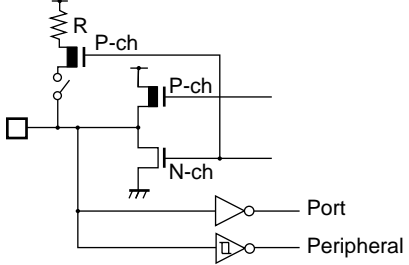
MB89150/150A Series

• **External EPROM pins (MB89PV150 only)**

Pin no.	Pin name	I/O	Function
82	V$_{PP}$	O	"H" level output pin
83 84 85 86 87 88 89 90 91	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
93 94 95	O1 O2 O3	I	Data input pins
96	V$_{SS}$	O	Power supply (GND) pin
98 99 100 101 102	O4 O5 O6 O7 O8	I	Data input pins
103	$\overline{CE}$	O	ROM chip enable pin Outputs "H" during standby.
104	A10	O	Address output pin
105	$\overline{OE}$	O	ROM output enable pin Outputs "L" at all times.
107 108 109	A11 A9 A8	O	Address output pins
110	A13	O	
111	A14	O	
112	V$_{CC}$	O	EPROM power supply pin
81 92 97 106	N.C.	—	Internally connected pins Be sure to leave them open.

MB89150/150A Series

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	X1 X0 Standby control signal	Crystal or ceramic oscillation type (main clock) • At an oscillation feedback resistor of approximately 1 MΩ/5.0 V
	X1 X0 Standby control signal	CR oscillation type (main clock) (except MB89PV150/P155)
B	X1A X0A Standby control signal	Crystal oscillation type (subclock) • At an oscillation feedback resistor of approximately 4.5 MΩ/3.0 V
C		
D	R P-ch N-ch	• At output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • Hysteresis input
E	R P-ch P-ch N-ch Port Peripheral	• CMOS I/O • The peripheral is a hysteresis input type. • Pull-up resistor optional (except MB89PV150)

(Continued)

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(Continued)

Type	Circuit	Remarks
F		• CMOS I/O • Pull-up resistor optional (except MB89PV150)
G		• CMOS output • P-ch output is a high-current drive type.
H		• N-ch open-drain I/O • CMOS input • The peripheral is a hysteresis input type. • Pull-up resistor optional (except MB89PV150/P155)
I		• N-ch open-drain I/O • CMOS input • P21, P26, and P27 are a high-current drive type. • Pull-up resistor optional (except MB89PV150/P155)
J		• N-ch open-drain output • Pull-up resistor optional (except MB89PV150/P155) • P31 and P32 are not provided with a pull-up resistor.
K		• LCD controller/driver segment output

MB89150/150A Series

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on "1. Absolute Maximum Ratings" in section "■ Electrical Characteristics" is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

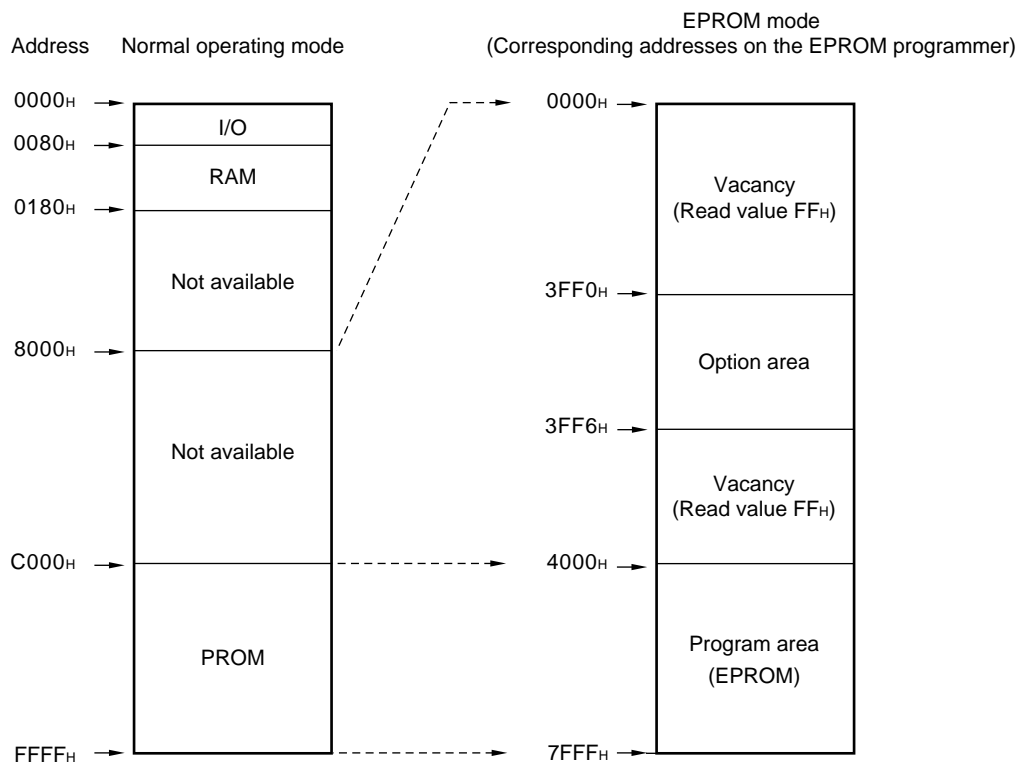## ■ PROGRAMMING TO THE EPROM ON THE MB89P155

The MB89P155 is an OTPROM version of the MB89150/A series.

1. Features

- 16-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in the EPROM mode is diagrammed below.

MB89150/150A Series

3. Programming to the EPROM

In EPROM mode, the MB89P155 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure**

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 4000_H to $7FFF_H$ (note that addresses $C000_H$ to $FFFF_H$ while operating as a normal operating mode assign to 4000_H to $7FFF_H$ in EPROM mode).
Load option data into addresses $3FF0_H$ to $3FF5_H$ of the EPROM programmer. (For information about each corresponding option, see "7. Setting OTPROM Options.")

(3) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.
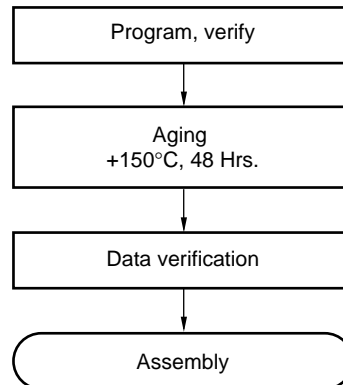
5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
FPT-80P-M05	ROM-80SQF-28DP-8L
FPT-80P-M06	ROM-80QF-28DP-8L3
FPT-80P-M11	ROM-80QF2-28DP-8L2

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

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MB89150/150A Series

7. Setting OTPROM Options

The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map:

- • OTPROM option bit map

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FF0$_H$	Vacancy Readable	Vacancy Readable	Oscillation stabilization time		Vacancy Readable	Reset pin output 1: Yes 0: No	Clock mode selection 1: Dual clock 0: Single clock	Power-on reset 1: Yes 0: No
			WTM1 See section "■ Mask Options."	WTM0				
3FF1$_H$	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
3FF2$_H$	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
3FF3$_H$	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable
3FF4$_H$	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable
3FF5$_H$	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable

Notes: • Set each bit to 1 to erase.
• Do not write 0 to the vacant bit.
  The read value of the vacant bit is 1, unless 0 is written to it.

MB89150/150A Series

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use
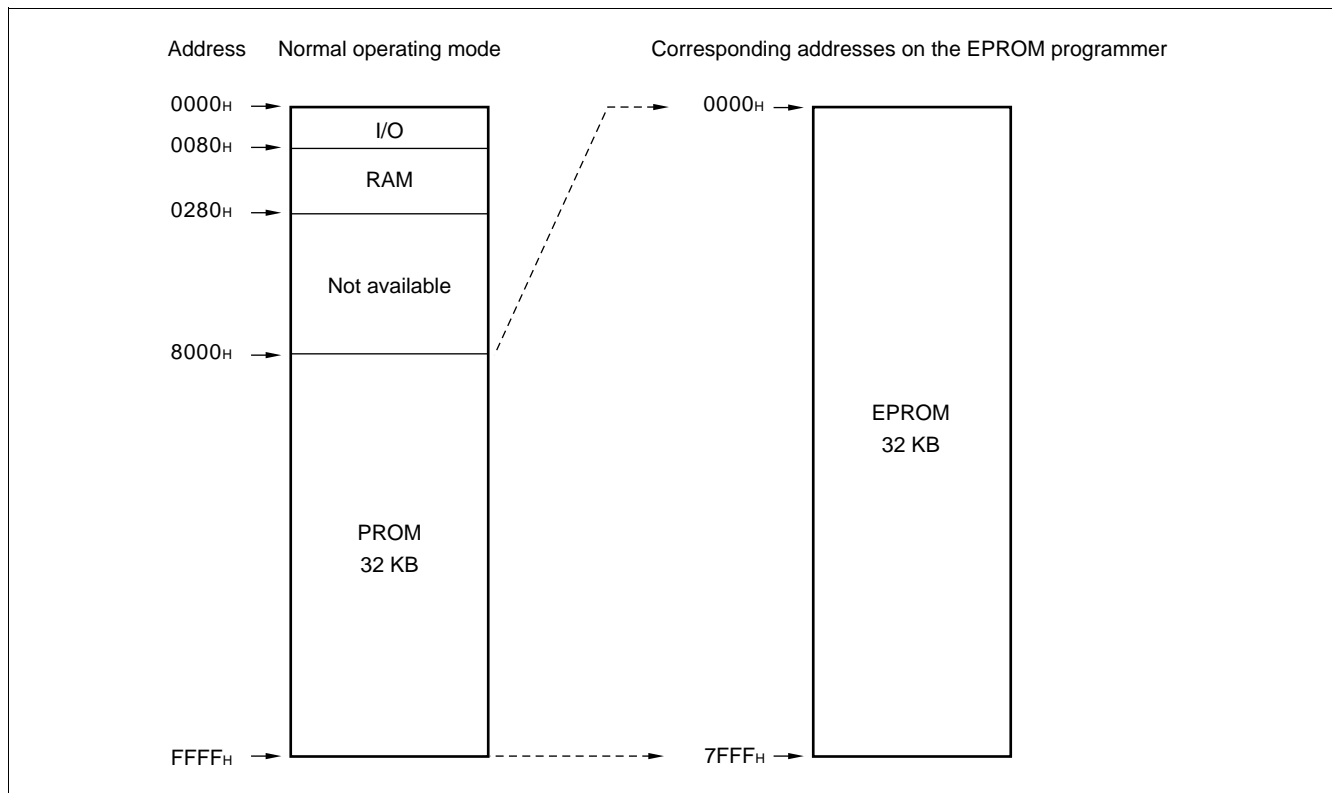
MBM27C256A-20TV

2. Programming Socket Adapter

To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32(Rectangle)	ROM-32LC-28DP-YG
LCC-32(Square)	ROM-32LC-28DP-S

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

3. Memory Space

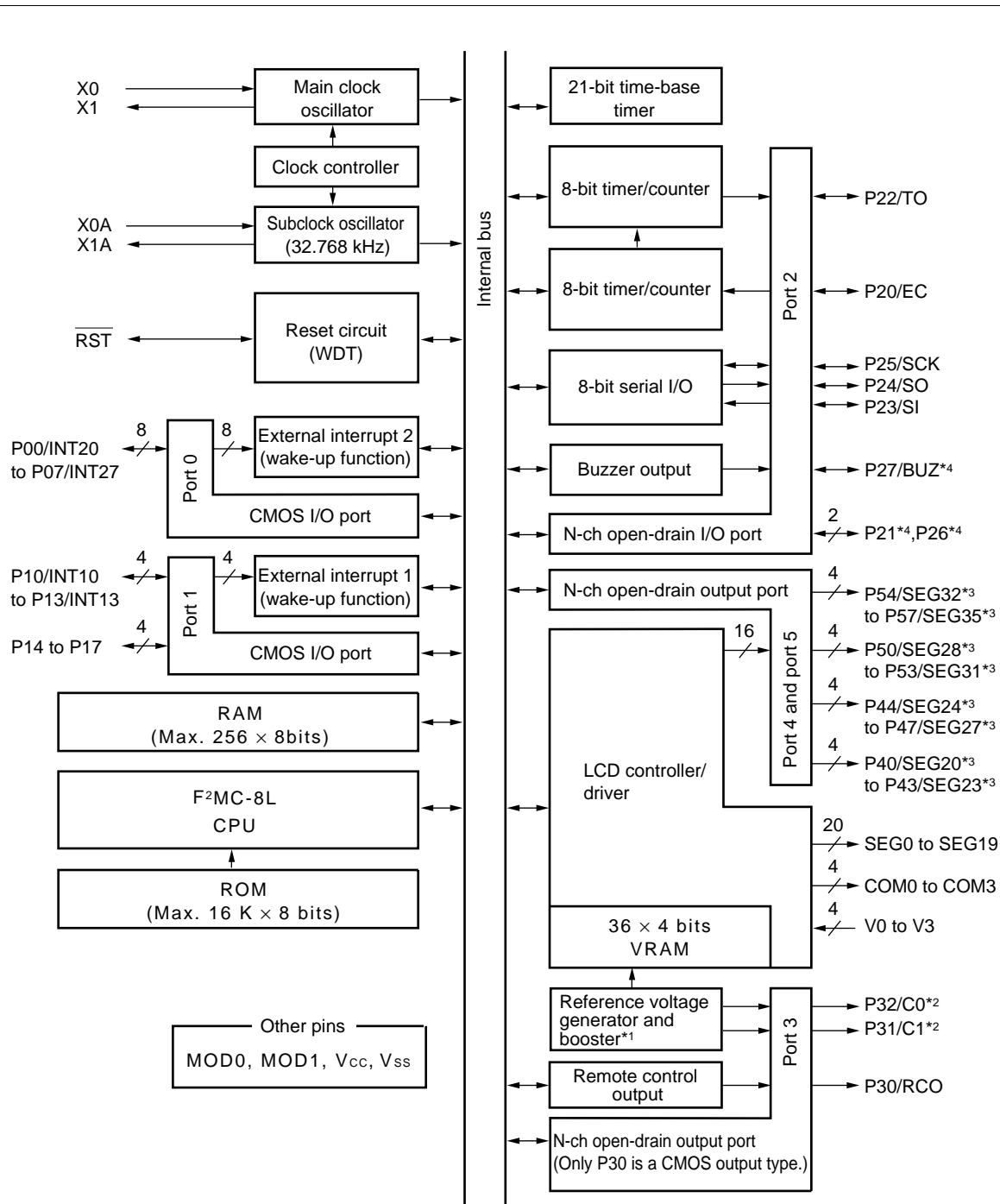Memory space in each mode is diagrammed below.

4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 4000_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

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MB89150/150A Series

■ BLOCK DIAGRAM

*1: Selected by mask option
*2: Used as ports without a reference voltage generator and booster
*3: Functions selected by mask option
*4: N-ch open-drain high-current drive type

MB89150/150A Series

■ CPU CORE

1. Memory Space

The microcontrollers of the MB89150/A series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89150/A series is structured as illustrated below.

Memory Space
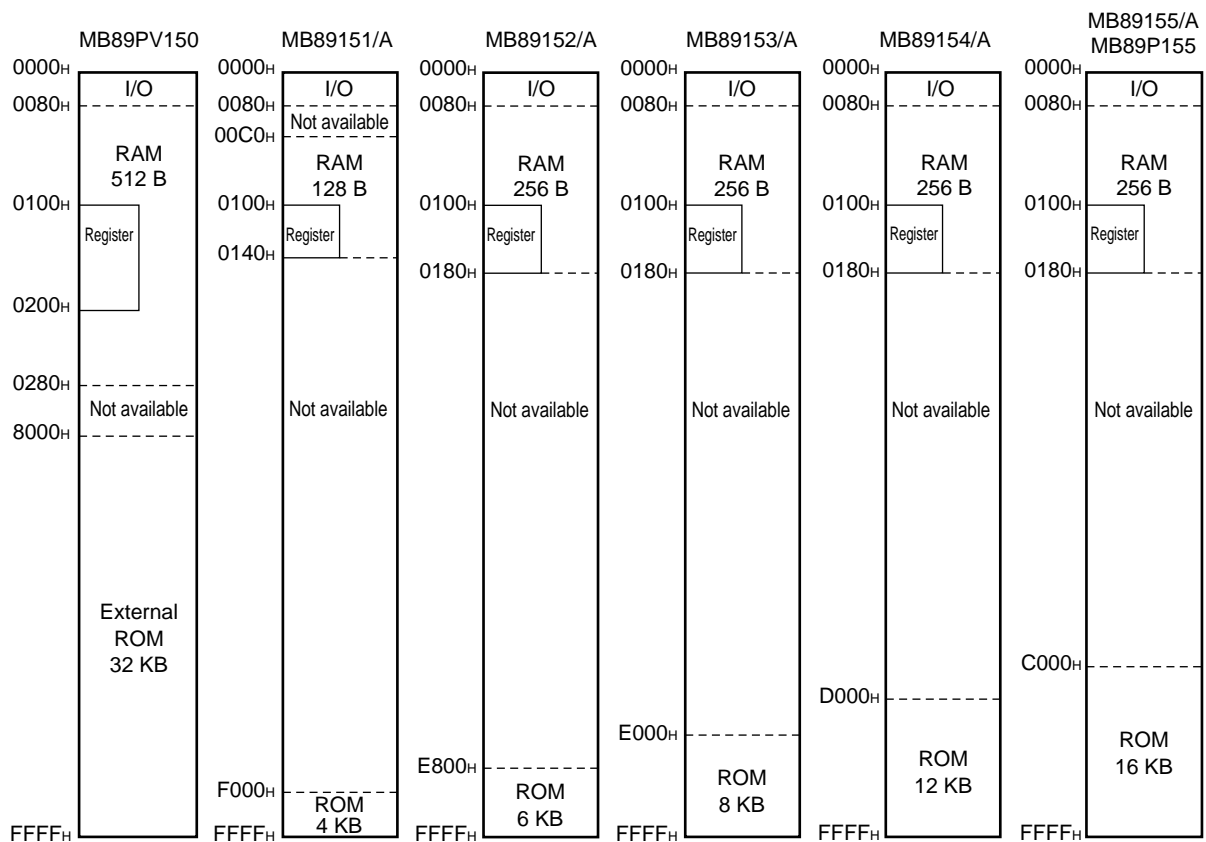
MB89150/150A Series

2. Registers

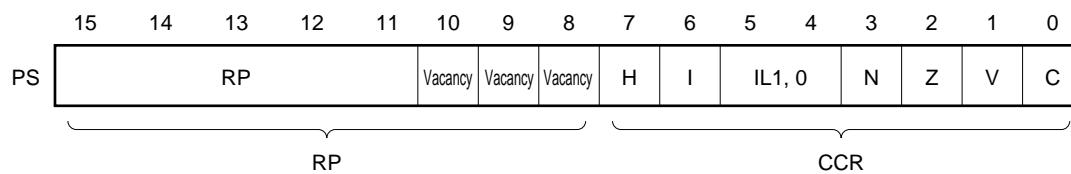The F^{2}MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):   A 16-bit register for indicating instruction storage positions

Accumulator (A):   A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.

Temporary accumulator (T):   A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.

Index register (IX):   A 16-bit register for index modification

Extra pointer (EP):   A 16-bit pointer for indicating a memory address

Stack pointer (SP):   A 16-bit register for indicating a stack area

Program status (PS):   A 16-bit register for storing a register pointer, a condition code

	16 bits		Initial value
PC	: Program counter	FFFD$_H$
A	: Accumulator	Undefined
T	: Temporary accumulator	Undefined
IX	: Index register	Undefined
EP	: Extra pointer	Undefined
SP	: Stack pointer	Undefined
PS	: Program status	I-flag = 0, IL1, 0 = 11 Other bits are undefined.

The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PS			RP			Vacancy	Vacancy	Vacancy	H	I	IL1, 0		N	Z	V	C

RP   CCR

MB89150/150A Series

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area

The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.
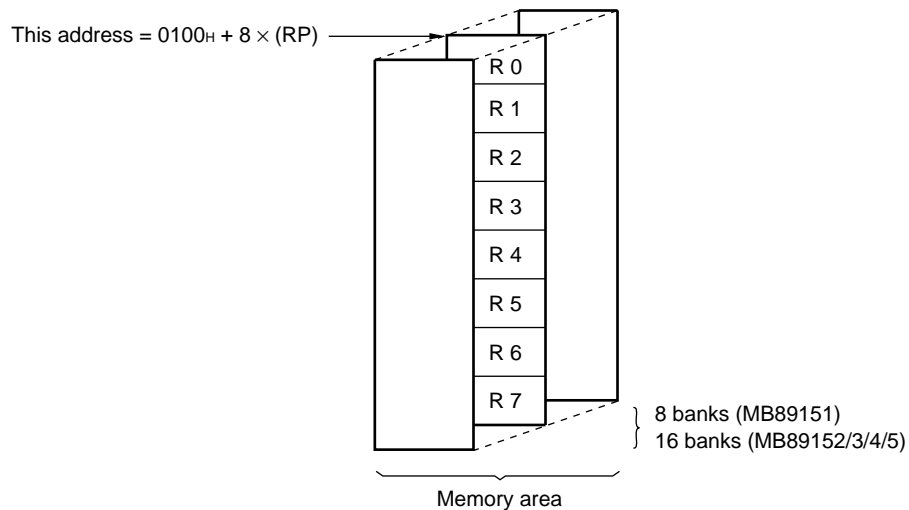
The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 8 banks can be used on the MB89151 (RAM 128 × 8 bits), and a total of 16 banks can be used on the MB89152/3/4/5 (RAM 256 × 8 bits). The bank currently in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size.

Register Bank Configuration

This address = $0100_H + 8 \times$ (RP)

R 0
R 1
R 2
R 3
R 4
R 5
R 6
R 7

8 banks (MB89151)
16 banks (MB89152/3/4/5)

Memory area

MB89150/150A Series

■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H	(R/W)	PDR1	Port 1 data register
03H	(W)	DDR1	Port 1 data direction register
04H	(R/W)	PDR2	Port 2 data register
05H	(W)	DDR2	Port 2 data direction register
06H			Vacancy
07H	(R/W)	SYCC	System clock control register
08H	(R/W)	STBC	Standby control register
09H	(R/W)	WDTC	Watchdog timer control register
0AH	(R/W)	TBTC	Time-base timer control register
0BH	(R/W)	WPCR	Watch prescaler control register
0CH	(R/W)	PDR3	Port 3 data register
0DH			Vacancy
0EH	(R/W)	PDR4	Port 4 data register
0FH	(R/W)	PDR5	Port 5 data register
10H	(R/W)	BZCR	Buzzer register
11H			Vacancy
12H			Vacancy
13H			Vacancy
14H	(R/W)	RCR1	Remote control transmission register 1
15H	(R/W)	RCR2	Remote control transmission register 2
16H			Vacancy
17H			Vacancy
18H	(R/W)	T2CR	Timer 2 control register
19H	(R/W)	T1CR	Timer 1 control register
1AH	(R/W)	T2DR	Timer 2 data register
1BH	(R/W)	T1DR	Timer 1 data register
1CH	(R/W)	SMR1	Serial mode register
1DH	(R/W)	SDR1	Serial data register
1EH to 2FH			Vacancy

(Continued)

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MB89150/150A Series

(Continued)

Address	Read/write	Register name	Register description
30H	(R/W)	EIE1	External interrupt 1 enable register
31H	(R/W)	EIF1	External interrupt 1 flag register
32H	(R/W)	EIE2	External interrupt 2 enable register
33H	(R/W)	EIF2	External interrupt 2 flag register
34H to 5FH			Vacancy
60H to 71H	(R/W)	VRAM	Display data RAM
72H	(R/W)	LCR1	LCD controller/driver control register 1
73H to 7BH			Vacancy
7CH	(W)	ILR1	Interrupt level setting register 1
7DH	(W)	ILR2	Interrupt level setting register 2
7EH	(W)	ILR3	Interrupt level setting register 3
7FH			Vacancy

Note: Do not use vacancies.

MB89150/150A Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

$(V_{SS} = 0.0 V)$

Parameter	Symbol	Value Min.	Value Max.	Unit	Remarks
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	
LCD power supply voltage	V0 to V3	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	V0 to V3 pins on the product with booster
		$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	V0 to V3 pins on the product without booster
Input voltage	V_{I1}	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	V_{I1} must not exceed V_{SS} +7.0 V. All pins except P20 to P27 without a pull-up resistor
	V_{I2}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	P20 to P27 without a pull-up resistor
Output voltage	V_{O1}	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	V_{O1} must not exceed V_{SS} +7.0 V. All pins except P20 to P27, P31, P32, P40 to P47, P50 to P57 without a pull-up resistor
	V_{O2}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	P20 to P27, P31, P32, P40 to P47, and P50 to P57, without a pull-up resistor
"L" level maximum output current	I_{OL1}	—	10	mA	All pins except P21, P26, P27, and power supply pins
	I_{OL2}	—	20	mA	P21, P26, and P27
"L" level average output current	I_{OLAV1}	—	4	mA	Average value (operating current $\times$ operating rate) All pins except P21, P26, P27, and power supply pins.
	I_{OLAV2}	—	8	mA	Average value (operating current $\times$ operating rate) P21, P26, and P27
"L" level total maximum output current	ΣI_{OL}	—	80	mA	
"L" level total average output current	ΣI_{OLAV}	—	40	mA	Average value (operating current $\times$ operating rate)
"H" level maximum output current	I_{OH1}	—	–5	mA	All pins except P30 and power supply pins
	I_{OH2}	—	–10	mA	P30

(Continued)

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MB89150/150A Series

(Continued)

$(V_{SS} = 0.0\ V)$

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
"H" level average output current	I_{OHAV1}	—	–2	mA	Average value (operating current × operating rate) All pins except P30 and power supply pins.
	I_{OHAV2}	—	–4	mA	Average value (operating current × operating rate) P30
"H" level total output current	ΣI_{OH}	—	–20	mA	
"H" level total average output current	ΣI_{OHAV}	—	–10	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

Precautions: Permanent device damage may occur if the above "Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

$(V_{SS} = 0.0\ V)$

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	2.2[*1]	6.0	V	Normal operation assurance range Single clock system of the mask ROM product.
		2.2[*1]	4.0	V	Normal operation assurance range Dual-clock system of the mask ROM product.
		2.7[*1]	6.0	V	MB89P155/PV150
		1.5	6.0	V	Retains the RAM state in stop mode
LCD power supply voltage	V0 to V3	V_{SS}	V_{CC}[*2]	V	V0 to V3 pins
LCD reference power supply input voltage	V_{IR}	1.3	2.2	V	V1 pin on the products with a booster Reference power external input
Operating temperature	T_A	–40	+85	°C	

*1: The minimum operating power supply voltage varies with the execution time (instruction cycle time) setting for the operating frequency.
*2: The LCD power supply voltage range and optimum value vary depending on the characteristics of the liquid-crystal display element.

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MB89150/150A Series

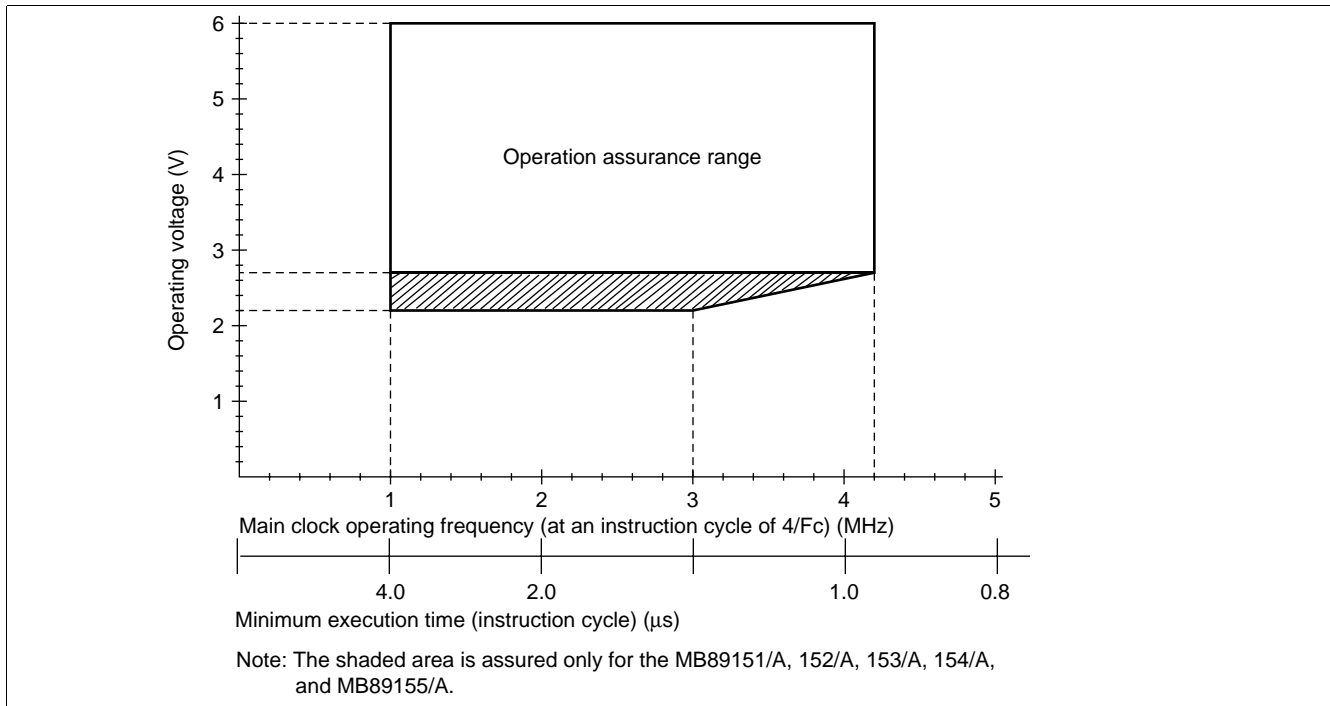**Figure 1   Operating Voltage vs. Main Clock Operating Frequency (MB89P155/PV150, and single-clock MB89151/A, 152/A, 153/A, 154/A, and MB89155/A)**
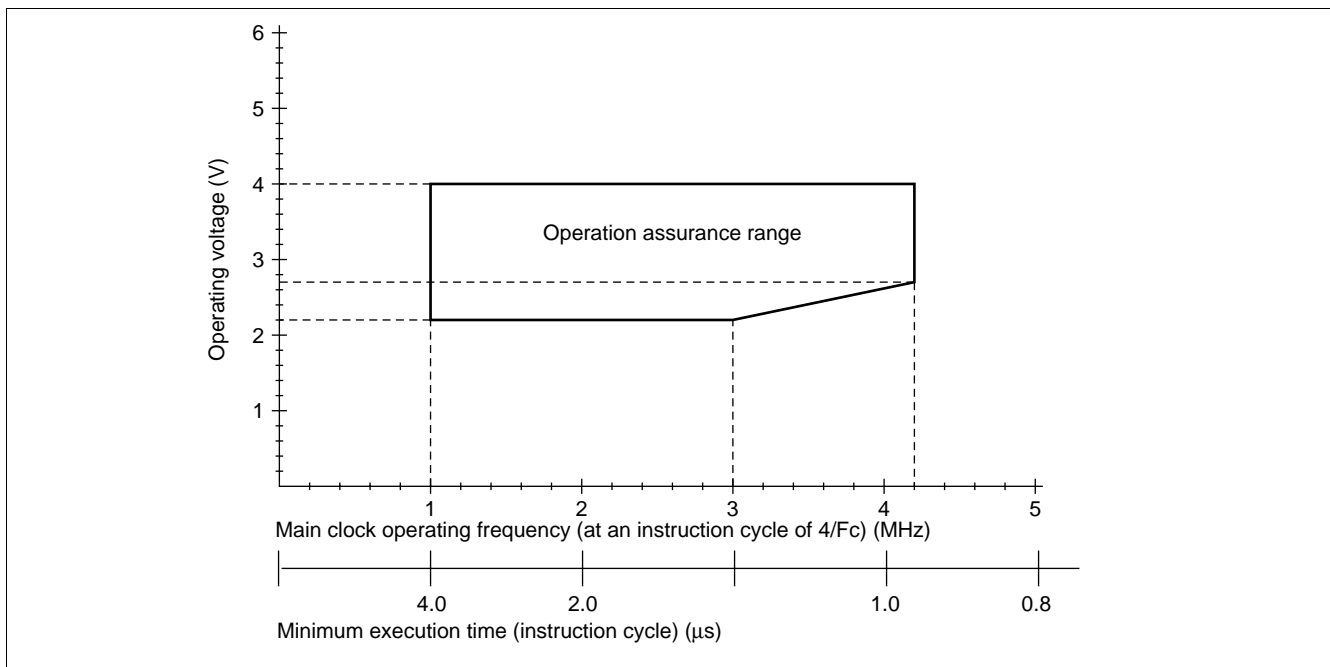

Figure 2   Operating Voltage vs. Main Clock Operating Frequency (Dual-clock MB89151/A, 152/A, 153/A, 154/A, and MB89155/A)

Figures 1 and 2 indicate the operating frequency of the external oscillator at a minimum execution time of $4/F_{CH}$.

Since the operating voltage range is dependent on the minimum execution time, see the minimum execution time if the operating speed is switched using a gear.

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MB89150/150A Series

3. DC Characteristics

$(V_{CC} = +5.0 \text{ V}, V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

Parameter	Symbol	Pin	Condition	Value Min.	Value Typ.	Value Max.	Unit	Remarks
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P27	—	$0.7\ V_{CC}$	—	$V_{CC} + 0.3$	V	CMOS input
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, EC, SI, SCK, INT10 to INT13, INT20 to INT27		$0.8\ V_{CC}$	—	$V_{SS} + 0.3$	V	Hysteresis input
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P20 to P27		$V_{SS} - 0.3$	—	$0.3\ V_{CC}$	V	CMOS input
	V_{ILS}	$\overline{RST}$, MOD0, MOD1, EC, SI, SCK, INT10 to INT13, INT20 to INT27		$V_{SS} - 0.3$	—	$0.2\ V_{CC}$	V	Hysteresis input
Open-drain output pin application voltage	V_D	P20 to P27, P31, P32, P40 to P47, P50 to P57		$V_{SS} - 0.3$	—	$V_{SS} + 6.0$[1]	V	Without pull-up resistor
"H" level output voltage	V_{OH1}	P00 to P07, P10 to P17	$I_{OH} = -2.0$ mA	2.4	—	—	V	
	V_{OH2}	P30	$I_{OH} = -6.0$ mA	4.0	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P10 to P17, P20, P22 to P25, P30 to P32, P40 to P47, P50 to P57	$I_{OL} = 1.8$ mA	—	—	0.4	V	
	V_{OL2}	P21, P26, P27	$I_{OL} = 8.0$ mA	—	—	0.4	V	
	V_{OL3}	$\overline{RST}$	$I_{OL} = 4.0$ mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI1}	MOD0, MOD1, P30, P00 to P07, P10 to P17	$0.0 \text{ V} < V_I < V_{CC}$	—	—	±5	µA	Without pull-up resistor
	I_{LI2}	P20 to P27, P31, P32, P40 to P47, P50 to P57	$0.0 \text{ V} < V_I < 6.0 \text{ V}$	—	—	±1	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P20 to P27, P40 to P47, P50 to P57, $\overline{RST}$	$V_I = 0.0$ V	25	50	100	kΩ	With pull-up resistor
Common output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = 5.0 V	—	—	2.5	kΩ	
Segment output impedance	R_{VSEG}	SEG0 to SEG35	V1 to V3 = 5.0 V	—	—	15	kΩ	
LCD divided resistance	R_{LCD}	—	Between V_{CC} and V0	300	500	750	kΩ	Products without a booster only
LCD leakage current	I_{LCDL}	V0 to V3, COM0 to COM3, SEG0 to SEG35	—	—	—	±1	µA	

(Continued)

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MB89150/150A Series

$(V_{CC} = +5.0 \text{ V}, V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Booster for LCD driving output voltage	V_{OV3}	V3	$V1 = 1.5 \text{ V}$	4.3	4.5	4.7	V	Products with a booster only
	V_{OV2}	V2		2.9	3.0	3.1	V	
Reference output voltage for LCD driving	V_{OV1}	V1	$I_{IN} = 0 \text{ μA}$	1.3	1.5	1.7	V	
Power supply current[*2]	I_{CC1}	V_{CC}	$F_{CH} = 4.2 \text{ MHz}$, $V_{CC} = 5.0 \text{ V}$ t_{inst}[*3] = 0.95 μs Main clock operation	—	3.0	4.5	mA	MB89151/A, 152/A, 153/A, 154/A, 155/A, MB89PV150-101 to 105
				—	3.8	6.0	mA	MB89P155-101 to 105/201 to 205
	I_{CC2}		$F_{CH} = 4.2 \text{ MHz}$, $V_{CC} = 3.0 \text{ V}$ t_{inst}[*3] = 15.2 μs Main clock operation	—	0.25	0.4	mA	MB89151/A, 152/A,153/A, 154/A, 155/A, MB89PV150-101 to 105
				—	0.85	1.4	mA	MB89P155-101 to 105/201 to 205
	I_{CCL}		$F_{CL} = 32.768 \text{ kHz}$, $V_{CC} = 3.0 \text{ V}$ t_{inst}[*3] = 61 μs Subclock operation	—	0.05	0.1	mA	MB89151/A, 152/A, 153/A, 154/A, 155/A, MB89PV150-101 to 105
				—	0.65	1.1	mA	MB89P155-101 to 105/201 to 205
	I_{CCS1}		$F_{CH} = 4.2 \text{ MHz}$, $V_{CC} = 5.0 \text{ V}$ t_{inst}[*3] = 0.95 μs Main clock sleep mode	—	0.8	1.2	mA	
	I_{CCS2}		$F_{CH} = 4.2 \text{ MHz}$, $V_{CC} = 3.0 \text{ V}$ t_{inst}[*3] = 15.2 μs Main clock sleep mode	—	0.2	0.3	mA	
	I_{CCSL}		$F_{CL} = 32.768 \text{ kHz}$, $V_{CC} = 3.0 \text{ V}$ t_{inst}[*3] = 61 μs Subclock sleep mode	—	25	50	μA	

(Continued)

MB89150/150A Series

(Continued)

$(V_{CC} = +5.0 \text{ V}, V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current[2]	I_{CCT}	V_{CC}	$F_{CL} = 32.768 \text{ kHz}$, $V_{CC} = 3.0$ V Watch mode	—	10	15	μA	MB89151/2/3/4/5, MB89P155-101 to 105, MB89PV150-101 to 105
	I_{CCT2}		$F_{CL} = 32.768 \text{ kHz}$, $V_{CC} = 3.0$ V • Watch mode • During reference voltage generator and booster operation	—	250	400	μA	MB89151A/2A/ 3A/4A/5A, MB89P155-201 to 205
	I_{CCH}		$T_A = +25°C$, $V_{CC} = 5.0$ V Stop mode	—	0.1	1	μA	MB89151/2/3/4/5
				—	0.1	10	μA	MB89PV150-101 to 105, MB89P155-101 to 105
Input capacitance	C_{IN}	Other than V_{CC}, V_{SS}	f = 1 MHz	—	10	—	pF	

*1: P31 and P32 are applicable only for products of the MB89150 series (without the "A" suffix). P40 to P47 and P50 to P57 are applicable when selected as ports.

*2: The power supply current is measured at the external clock, open output pins, and the external LCD dividing resistor (or external input for the reference voltage).
In the case of the MB89PV150, the current consumed by the connected EPROM and ICE is not included.

*3: For information on t_{inst}, see "(4) Instruction Cycle" in "4. AC Characteristics."

Note: For pins which serves as the segment (SEG20 to SEG35) and ports (P40 to P47, P50 to P57), see the port parameter when these pins are used as ports and the segment parameter when they are used as segments. P31 and P32 are applicable only for products without a booster (applicable as external capacitor connection pins for products with a booster).
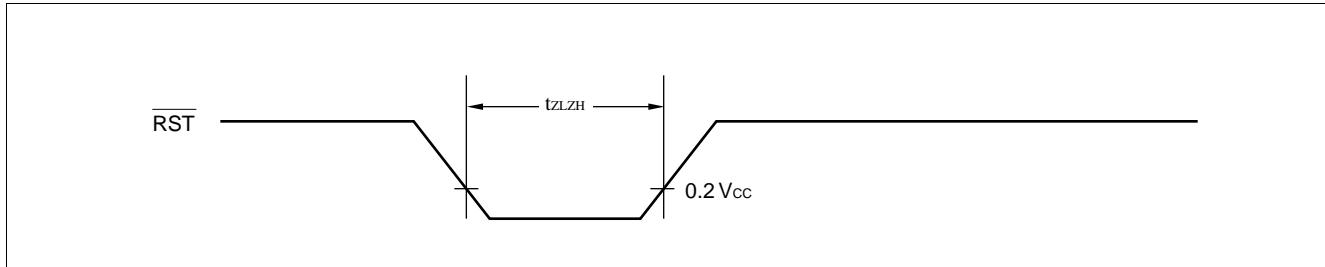
MB89150/150A Series

4. AC Characteristics

(1) Reset Timing

$(V_{SS} = 0.0\ V, T_A = -40°C\ to\ +85°C)$

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}	—	ns	

(2) Power-on Reset

$(V_{SS} = 0.0\ V, T_A = -40°C\ to\ +85°C)$

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.
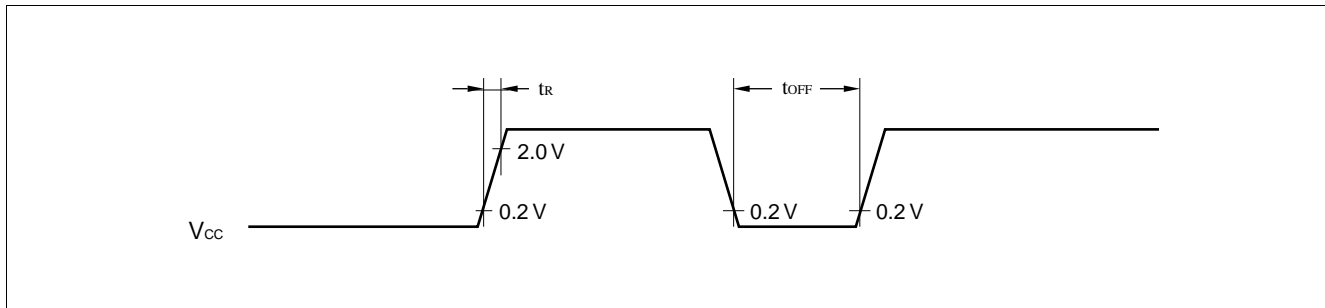
(3) Clock Timing

(V$_{SS}$ = 0.0 V, T$_A$ = –40°C to +85°C)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Clock frequency	F$_{CH}$	X0, X1	1	—	4.2	MHz	Main clock
	F$_{CL}$	X0A, X1A	—	32.768	—	kHz	Subclock
Clock cycle time	t$_{HCYL}$	X0, X1	238	—	1000	ns	Main clock
	t$_{LCYL}$	X0A, X1A	—	30.5	—	μs	Subclock
Input clock pulse width	P$_{WH}$ P$_{WL}$	X0	20	—	—	ns	External clock
	P$_{WHL}$ P$_{WLL}$	X0A	—	15.2	—	μs	
Input clock pulse rising/falling time	t$_{CR}$ t$_{CF}$	X0, X0A	—	—	10	ns	

X0 and X1 Timing and Conditions
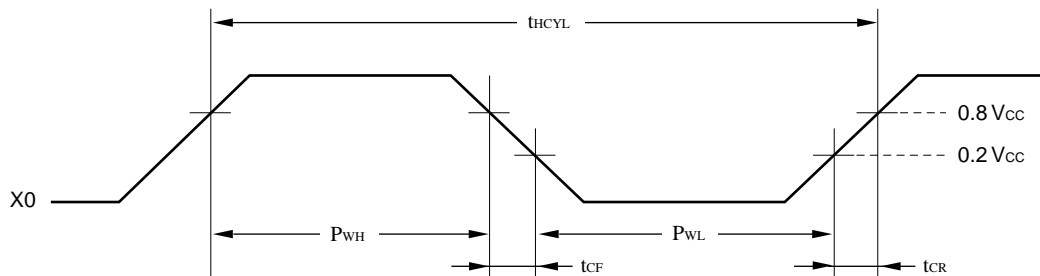
Main Clock Conditions
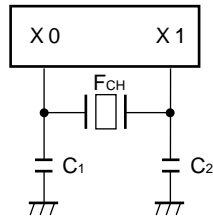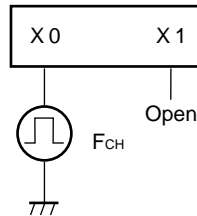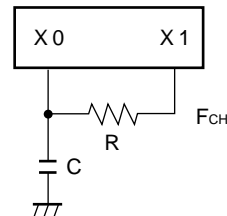
MB89150/150A Series

X0A and X1A Timing and Conditions
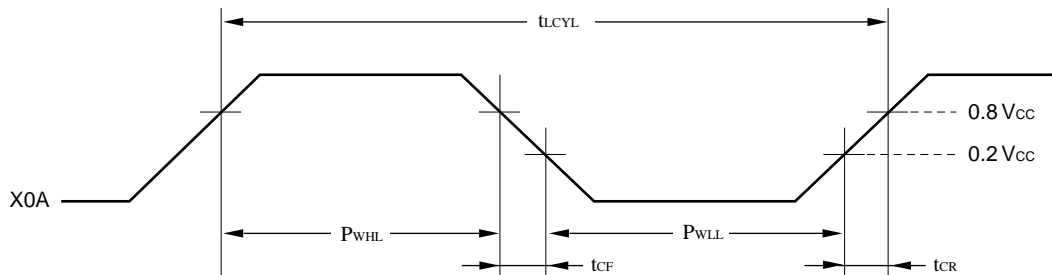
Subclock Conditions
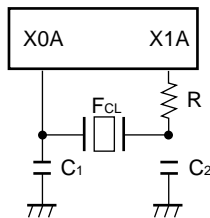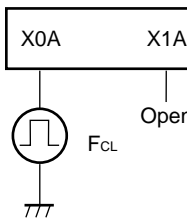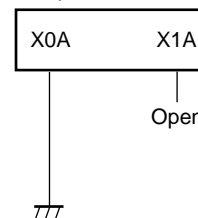
(4) Instruction Cycle

Parameter	Symbol	Value	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	µs	$(4/F_{CH})$ t_{inst} = 0.95 µs when operating at F_{CH} = 4.2 MHz
		$2/F_{CL}$	µs	t_{inst} = 61.036 µs when operating at F_{CL} = 32.768 kHz

(5) Serial I/O Timing

$(V_{CC} = +5.0\ V\pm10\%,\ V_{SS}= 0.0\ V,\ T_A = -40°C\ to\ +85°C)$

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	$2\ t_{inst}$*	—	μs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		−200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		$0.5\ t_{inst}$*	—	μs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		$0.5\ t_{inst}$*	—	μs	
Serial clock "H" pulse width	t_{SHSL}	SCK	External shift clock mode	$1\ t_{inst}$*	—	μs	
Serial clock "L" pulse width	t_{SLSH}	SCK		$1\ t_{inst}$*	—	μs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		$0.5\ t_{inst}$*	—	μs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		$0.5\ t_{inst}$*	—	μs	

* : For information on t_{inst}, see "(4) Instruction Cycle."
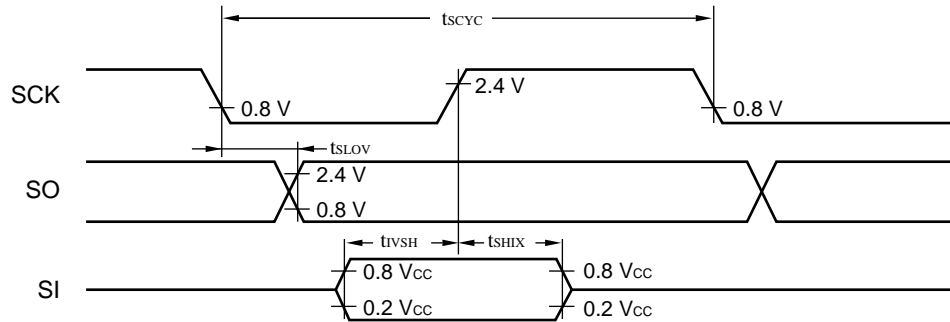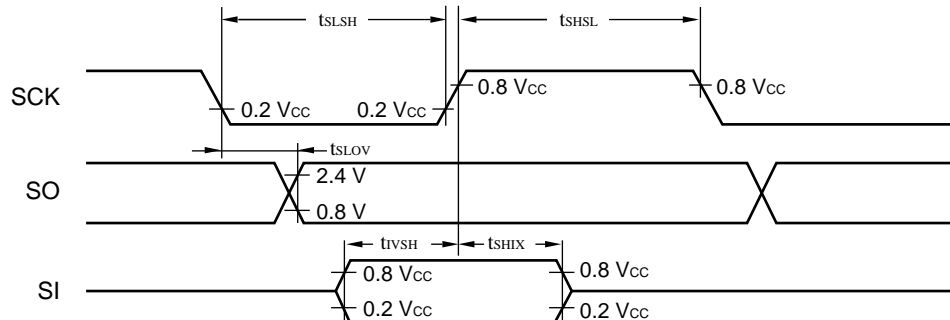
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(6)   Peripheral Input Timing

$(V_{CC} = +5.0\ V\pm10\%,\ V_{SS} = 0.0\ V,\ T_A = -40°C\ to\ +85°C)$

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Peripheral input "H" pulse width 1	t_{ILIH1}	INT10 to INT13, EC	$1\ t_{inst}$*	—	µs	
Peripheral input "L" pulse width 1	t_{IHIL1}		$1\ t_{inst}$*	—	µs	
Peripheral input "H" pulse width 2	t_{ILIH2}	INT20 to INT27	$2\ t_{inst}$*	—	µs	
Peripheral input "L" pulse width 2	t_{IHIL2}		$2\ t_{inst}$*	—	µs	

* : For information on $t_{inst,}$ see "(4) Instruction Cycle."

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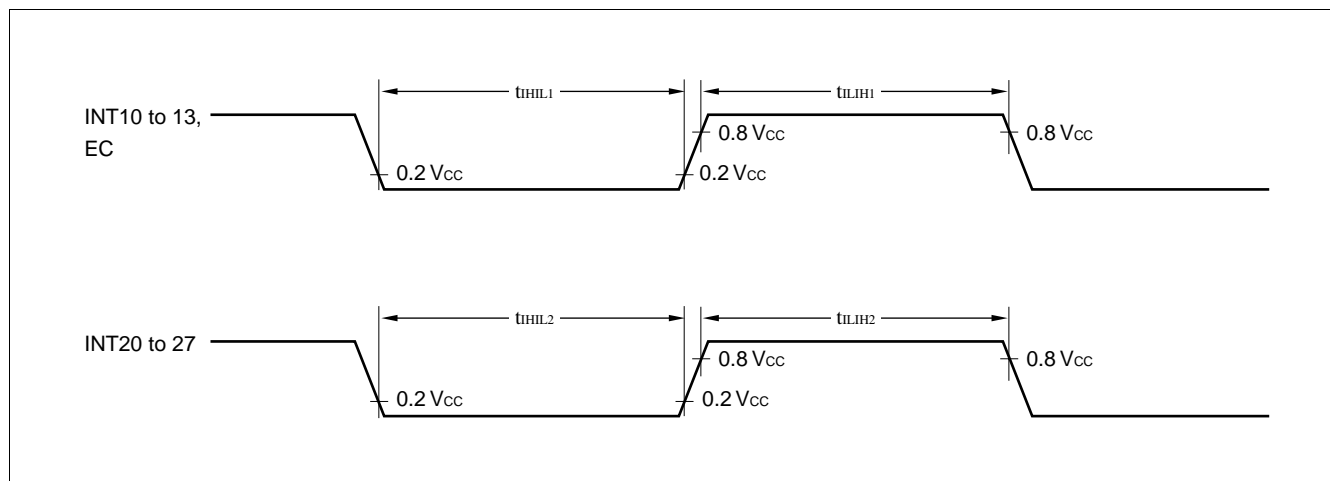
MB89150/150A Series
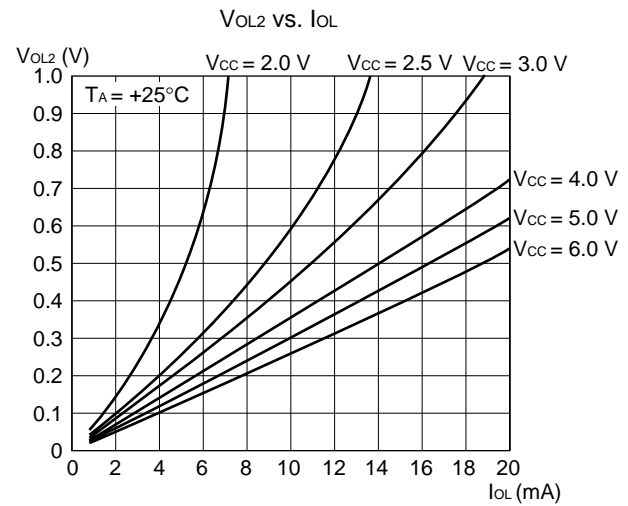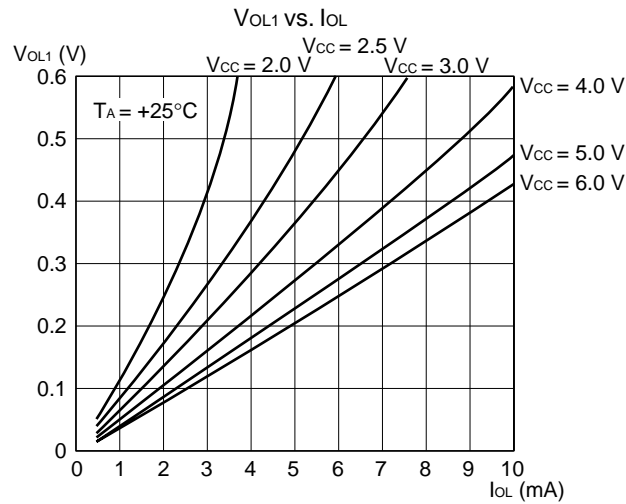
■ EXAMPLE CHARACTERISTICS

(1) "L" Level Output Voltage

V_{OL1} vs. I_{OL}

V_{OL2} vs. I_{OL}

(2) "H" Level Output Voltage

$V_{CC} - V_{OH1}$ vs. I_{OH}

$V_{CC} - V_{OH2}$ vs. I_{OH}

(Continued)

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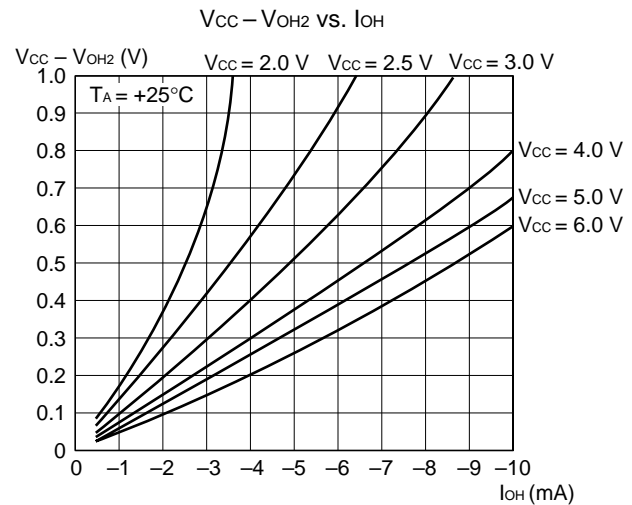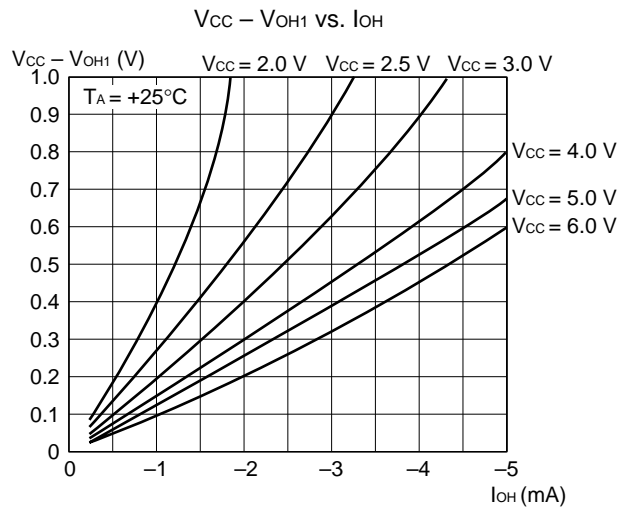
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(3) "H" Level Input Voltage/"L" level Input Voltage

(CMOS input)

V_{IN} vs. V_{CC}

V_{IN} (V)

$T_A = +25°C$

(graph with V_IN (V) on y-axis from 0 to 5.0, V_CC (V) on x-axis from 1 to 7)

(Hysteresis input)

V_{IN} vs. V_{CC}

V_{IN} (V)

$T_A = +25°C$

V_{IHS}

V_{ILS}

(graph with V_IN (V) on y-axis from 0 to 5.0, V_CC (V) on x-axis from 1 to 7)
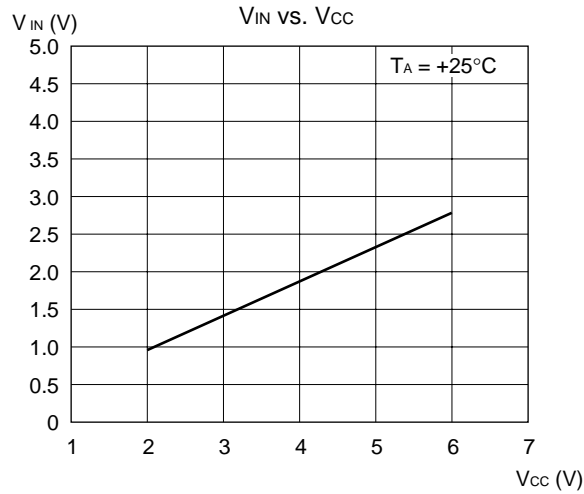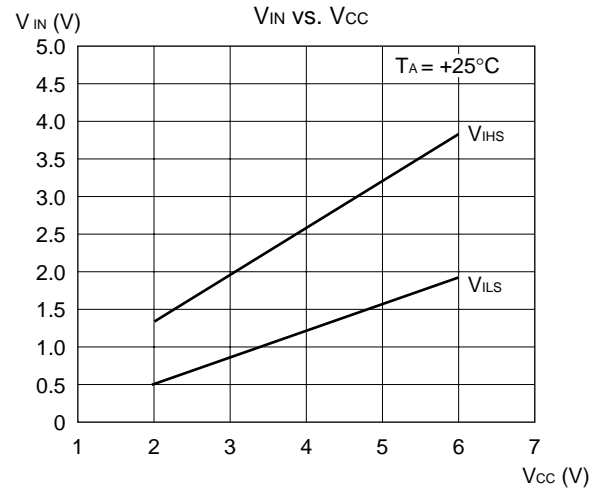
V_{IHS}: Threshold when input voltage in hysteresis characteristics is set to "H" level

V_{ILS}: Threshold when input voltage in hysteresis characteristics is set to "L" level

(4) Power Supply Current (External Clock)

I_{CC1} vs. V_{CC} (Mask ROM product)

I_{CC1} (mA)

$T_A = +25°C$

$F_{CH} = 4.2\,MHz$

$F_{CH} = 3\,MHz$

$F_{CH} = 1\,MHz$

(graph with I_CC1 (mA) on y-axis from 0 to 5.0, V_CC (V) on x-axis from 1 to 7)

I_{CC2} vs. V_{CC} (Mask ROM product)

I_{CC2} (mA)

$T_A = +25°C$

$F_{CH} = 4.2\,MHz$

$F_{CH} = 3\,MHz$

$F_{CH} = 1\,MHz$

(graph with I_CC2 (mA) on y-axis from 0 to 1.0, V_CC (V) on x-axis from 1 to 7)

(Continued)

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I_{CCS1} vs. V_{CC}

I_{CCS1} (mA)

$T_A = +25°C$

$F_{CH} = 4.2$ MHz
$F_{CH} = 3$ MHz
$F_{CH} = 1$ MHz

V_{CC} (V)

I_{CCS2} vs. V_{CC}

I_{CCS2} (mA)

$T_A = +25°C$

$F_{CH} = 4.2$ MHz
$F_{CH} = 3$ MHz
$F_{CH} = 1$ MHz

V_{CC} (V)

I_{CCL} vs. V_{CC} (Mask ROM product)

I_{CCL} (µA)

$T_A = +25°C$

$F_{CL} = 32.768$ kHz

V_{CC} (V)

I_{CCT} vs. V_{CC}

I_{CCT} (µA)

$T_A = +25°C$

$F_{CL} = 32.768$ kHz

V_{CC} (V)

(Continued)

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(Continued)

I_{CCSL} vs. V_{CC}

I_{CCSL} (μA)

T_A = +25°C

F_{CL} = 32.768 kHz

V_{CC} (V)

I_{CCT2} vs. V_{CC}

I_{CCT2} (μA)

T_A = +25°C

F_{CL} = 32.768 kHz

V_{CC} (V)

(5) Pull-up Resistance

R_{PULL} (kΩ)

T_A = +85°C
T_A = +25°C
T_A = −40°C

V_{CC} (V)

40

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■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1   Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

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(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
$\times$	Indicates that the very $\times$ is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
$(\times)$	Indicates that the contents of $\times$ is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
$((\times))$	The address indicated by the contents of $\times$ is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~:   Number of instructions

#:   Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

• "–" indicates no change.
• dH is the 8 upper bits of operation description data.
• AL and AH must become the contents of AL and AH immediately before the instruction is executed.
• 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

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Table 2   Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
　　　• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F^{2}MC-8 family)

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Table 3   Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) − (Ri) − C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) − d8 − C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) − (dir) − C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) − ((IX) +off) − C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) − ((EP)) − C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) − (A) − C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) − (AL) − C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + −	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	− − − −	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	− − − −	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + − −	C0
DEC Ri	4	1	(Ri) ← (Ri) − 1	–	–	–	+ + + −	D8 to DF
DECW EP	3	1	(EP) ← (EP) − 1	–	–	–	− − − −	D3
DECW IX	3	1	(IX) ← (IX) − 1	–	–	–	− − − −	D2
DECW A	3	1	(A) ← (A) − 1	–	–	dH	+ + − −	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	− − − −	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	− − − −	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R −	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R −	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R −	53
CMP A	2	1	(TL) − (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) − (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A ⌐	–	–	–	+ + − +	03
ROLC A	2	1	⌐ C ← A ←	–	–	–	+ + − +	02
CMP A,#d8	2	2	(A) − d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) − (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) − ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) − ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) − (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R −	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R −	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R −	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R −	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R −	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R −	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R −	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R −	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R −	65

(Continued)

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(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4   Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subroutine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5   Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

MB89150/150A Series

■ INSTRUCTION MAP

L\H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir:0	BBC dir:0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir:1	BBC dir:1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A,T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir:2	BBC dir:2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A,T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir:3	BBC dir:3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir:4	BBC dir:4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir:5	BBC dir:5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX+d	CMP A,@IX+d	ADDC A,@IX+d	SUBC A,@IX+d	MOV @IX+d,A	XOR A@,IX+d	AND A,@IX+d	OR A,@IX+d	MOV @IX+d,#d8	CMP @IX+d,#d8	CLRB dir:6	BBC dir:6,rel	MOVW A,@IX+d	MOVW @IX+d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir:7	BBC dir:7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir:0	BBS dir:0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir:1	BBS dir:1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir:2	BBS dir:2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir:3	BBS dir:3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir:4	BBS dir:4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir:5	BBS dir:5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir:6	BBS dir:6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir:7	BBS dir:7,rel	INC R7	DEC R7	CALLV #7	BLT rel

MB89150/150A Series

■ MASK OPTIONS

No.	Part number	MB89151/1A, 2/2A, 3/3A, 4/4A, 5/5A	MB89P155	MB89PV150
	Specifying procedure	Specify when ordering masking	Set with EPROM programmer	Setting not possible
1	Pull-up resistors 　　P00 to P07, P10 to P17	Selectable per pin	Can be set per pin	Fixed to without a pull-up resistor
2	Pull-up resistors 　　P40 to P47, P50 to P57	Selectable per pin (Only when segment output is not selected.)	Fixed to without a pull-up resistor	
3	Pull-up resistors 　　P20 to P27	Selectable by pin	Fixed to without a pull-up resistor	
4	Power-on reset 　　With power-on reset 　　Without power-on reset	Selectable	Selectable	Fixed to with power-on reset
5	Selection of oscillation stabilization time • The initial value of the oscillation stabilization time for the main clock can be set by selecting the values of the WTM1 and WTM0 bits on the right.	Selectable WTM1 WTM0 　0　　0:　　$2^2/F_{CH}$ 　0　　1:　　$2^{12}/F_{CH}$ 　1　　0:　　$2^{16}/F_{CH}$ 　1　　1:　　$2^{18}/F_{CH}$	Selectable WTM1 WTM0 　0　　0:　　$2^2/F_{CH}$ 　0　　1:　　$2^{12}/F_{CH}$ 　1　　0:　　$2^{16}/F_{CH}$ 　1　　1:　　$2^{18}/F_{CH}$	Fixed to oscillation stabilization time of $2^{16}/F_{CH}$
6	Main clock oscillation type 　　Crystal or ceramic resonator 　　CR	Selectable	Fixed to crystal or ceramic only	Fixed to crystal or ceramic
7	Reset pin output 　　With reset output 　　Without reset output	Selectable	Selectable	Fixed to with reset output
8	Clock mode selection 　　Dual-clock mode 　　Single-clock mode	Selectable	Selectable	Fixed to dual-clock mode
9	Segment output selection 36: No ports selection 32: Selection of P57 to P54 28: Selection of P57 to P50 24: Selection of P57 to P50, and P47 to P44. 20: Selection of P57 to P50, and P47 to P40.	Selectable Selection of the number of segments.	-101/201: 36 segments -102/202: 32 segments -103/203: 28 segments -104/204: 24 segments -105/205: 20 segments	-101: 36 segments -102: 32 segments -103: 28 segments -104: 24 segments -105: 20 segments
10	Selection of a built-in booster	Without booster: MB89151/2/3/4/5 With booster: MB89151A/2A/3A/4A/5A	Without booster: -101 to 105 With booster: -201 to 205	Fixed to without booster (-100 to 105 only)

MB89150/150A Series

• **Versions**

Version			Features	
Mass production product	**One-time PROM product**	**Piggyback/evaluation product**	**Number of segment pins**	**Booster**
MB8915151A 152A 153A 154A 155A	MB89P155-201 -202 -203 -204 -205	—	36 32 28 24 20	Yes
MB8915151 152 153 154 155	MB89P155-101 -102 -103 -104 -105	MB89PV150-101 -102 -103 -104 -105	36 32 28 24 20	No

■ ORDERING INFORMATION

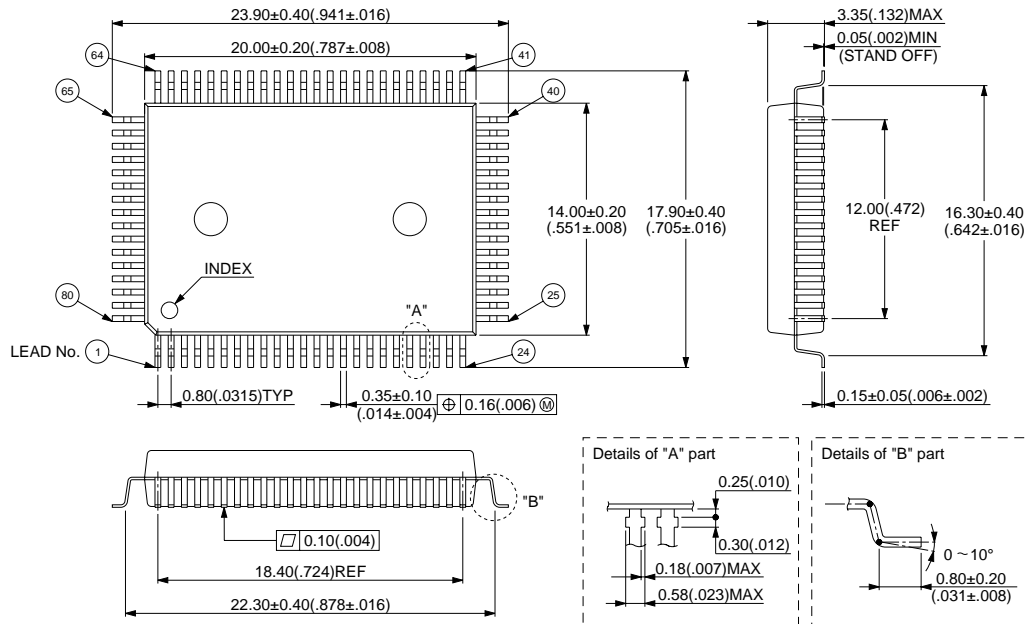| Part number	Package	Remarks
MB89151PF MB89152PF MB89153PF MB89154PF MB89155PF MB89P155PF-101 MB89P155PF-102 MB89P155PF-103 MB89P155PF-104 MB89P155PF-105	80-pin Plastic QFP (FPT-80P-M06)	Without booster
MB89151APF MB89152APF MB89153APF MB89154APF MB89155APF MB89P155PF-201 MB89P155PF-202 MB89P155PF-203 MB89P155PF-204 MB89P155PF-205		With booster

(Continued)

(Continued)

Part number	Package	Remarks
MB89151PFM MB89152PFM MB89153PFM MB89154PFM MB89155PFM MB89P155PFM-101 MB89P155PFM-102 MB89P155PFM-103 MB89P155PFM-104 MB89P155PFM-105	80-pin Plastic LQFP (FPT-80P-M11)	Without booster
MB89151APFM MB89152APFM MB89153APFM MB89154APFM MB89155APFM MB89P155PFM-201 MB89P155PFM-202 MB89P155PFM-203 MB89P155PFM-204 MB89P155PFM-205		With booster
MB89151PFV MB89152PFV MB89153PFV MB89154PFV MB89155PFV MB89P155PFV-101 MB89P155PFV-102 MB89P155PFV-103 MB89P155PFV-104 MB89P155PFV-105	80-pin Plastic LQFP (FPT-80P-M05)	Without booster
MB89151APFV MB89152APFV MB89153APFV MB89154APFV MB89155APFV MB89P155PFV-201 MB89P155PFV-202 MB89P155PFV-203 MB89P155PFV-204 MB89P155PFV-205		With booster
MB89PV150CF-101 MB89PV150CF-102 MB89PV150CF-103 MB89PV150CF-104 MB89PV150CF-105	80-pin Ceramic MQFP (MQP-80C-P01)	Without booster

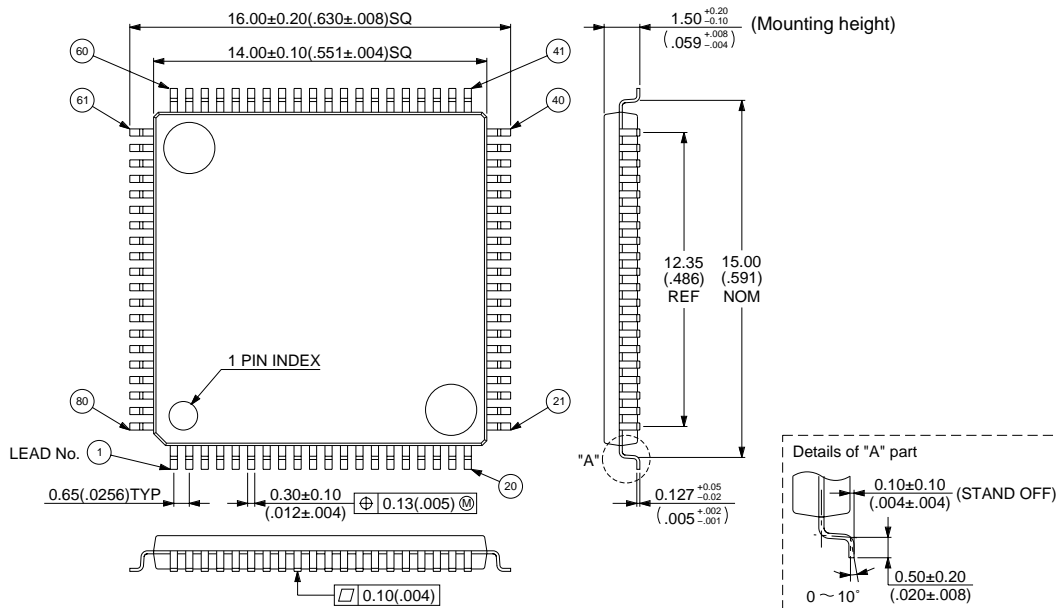# MB89150/150A Series

■ PACKAGE DIMENSIONS

80-pin Plastic QFP
(FPT-80P-M06)

23.90±0.40(.941±.016)
20.00±0.20(.787±.008)
14.00±0.20 (.551±.008)
17.90±0.40 (.705±.016)
INDEX
"A"
LEAD No. 1
0.80(.0315)TYP
0.35±0.10 (.014±.004)
⊕ 0.16(.006) Ⓜ
3.35(.132)MAX
0.05(.002)MIN (STAND OFF)
12.00(.472) REF
16.30±0.40 (.642±.016)
0.15±0.05(.006±.002)
"B"
0.10(.004)
18.40(.724)REF
22.30±0.40(.878±.016)

Details of "A" part
0.25(.010)
0.30(.012)
0.18(.007)MAX
0.58(.023)MAX

Details of "B" part
0 ~ 10°
0.80±0.20 (.031±.008)

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Dimensions in mm (inches)

80-pin Plastic LQFP
(FPT-80P-M11)

16.00±0.20(.630±.008)SQ
14.00±0.10(.551±.004)SQ
1 PIN INDEX
LEAD No. 1
0.65(.0256)TYP
0.30±0.10 (.012±.004)
⊕ 0.13(.005) Ⓜ
1.50 $^{+0.20}_{-0.10}$ (.059 $^{+.008}_{-.004}$) (Mounting height)
12.35 (.486) REF
15.00 (.591) NOM
"A"
0.127 $^{+0.05}_{-0.02}$ (.005 $^{+.002}_{-.001}$)
0.10(.004)

Details of "A" part
0.10±0.10 (.004±.004) (STAND OFF)
0 ~ 10°
0.50±0.20 (.020±.008)

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Dimensions in mm (inches)

50

MB89150/150A Series

80-pin Plastic LQFP
(FPT-80P-M05)

14.00±0.20(.551±.008)SQ

12.00±0.10(.472±.004)SQ

60
41
61
40

INDEX

80
21

LEAD No. 1
20

"A"

0.50±0.08
(.0197±.0031)

$0.18^{+0.08}_{-0.03}$
$\left(.007^{+.003}_{-.001}\right)$

$0.127^{+0.05}_{-0.02}$
$\left(.005^{+.002}_{-.001}\right)$

$1.50^{+0.20}_{-0.10}$ (Mounting height)
$\left(.059^{+.008}_{-.004}\right)$

9.50
(.374)
REF

13.00
(.512)
NOM

Details of "A" part

0.10±0.10 (STAND OFF)
(.004±.004)

0.50±0.20(.020±.008)

0 ~ 10°

0.10(.004)
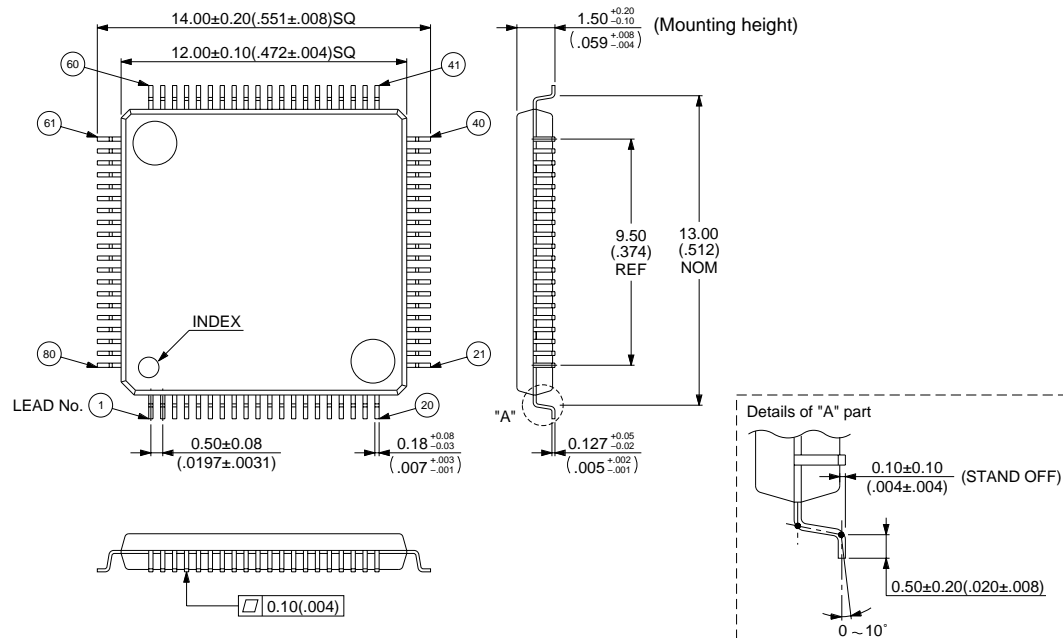
© 1995 FUJITSU LIMITED F80008S-2C-5

Dimensions in mm (inches)

80-pin Ceramic MQFP
(MQP-80C-P01)

18.70(.736)TYP

16.30±0.33
(.642±.013)

15.58±0.20
(.613±.008)

INDEX AREA

4.50(.177)
TYP

1.27±0.13
(.050±.005)

22.30±0.33
(.878±.013)

24.70(.972)
TYP

0.30(.012)
TYP

12.02(.473)
TYP

10.16(.400)
TYP

14.22(.560)
TYP

18.12±0.20
(.713±.008)

INDEX

6.00(.236)
TYP

1.27±0.13
(.050±.005)

0.30(.012)TYP

7.62(.300)TYP

9.48(.373)TYP

11.68(.460)TYP

1.50(.059)TYP
1.00(.040)TYP

$1.20^{+0.40}_{-0.20}$
$\left(.047^{+.016}_{-.008}\right)$

12.00(.472)TYP

0.80±0.25
(.0315±.010)

0.80±0.25
(.0315±.010)

INDEX AREA

18.40(.724)
REF

0.40±0.10
(.016±.004)

1.50(.059)
TYP

1.00(.040)
TYP

0.40±0.10
(.016±.004)

$1.20^{+0.40}_{-0.20}$
$\left(.047^{+.016}_{-.008}\right)$

0.15±0.05
(.006±.002)

8.70(.343)
MAX

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Dimensions in mm (inches)

MB89150/150A Series

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