DS87C550
High-Speed Microcontroller
User's Guide Supplement

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Section 1:Introduction
This document is provided as a supplement to the High-Speed Microcontrollers User's Guide, covering new or modified features specific to the DS87C550. ***This document must be used in conjunction with the High-Speed Microcontroller User's Guide, available from Dallas Semiconductor.*** Addenda are arranged by section number, which correspond to sections in the High-Speed Microcontroller User's Guide.

The following additions and changes, with respect to the High-Speed Microcontroller User's Guide, are contained in this document. This document is a work in progress, and updates/additions will be added as available.

Section 2:Ordering Information
Information on new members of the High-Speed Microcontroller family has been added.

Section 3:Architecture
No Changes. Information containing new architectural features is contained in the DS87C550 data sheet.

Section 4:Programming Model
Descriptions of new and modified Special Function Registers in the DS87C550 have been included.

Section 5:CPU Timing
Descriptions of the clock multiply/divide modes have been added.

Section 6:Memory Access
Information on EPROM size and the DPTR auto-select feature have been added.

Section 7:Power Management
Changes in the power management clock divisor are discussed.

Section 8:Reset Conditions
A discussion of the reset output has been included.

Section 9: Interrupts
The interrupt structure found on the DS87C550 is described.

Section 10:Parallel I/O
Descriptions of the new I/O ports have been added.

Section 11:Programmable Timers
New clock multiply and divide functions added to the DS87C550's Timers are described.

Section 12:Serial I/O
No changes.

Section 13:Timed Access Protection
Additional/modified Timed Access bits in the DS87C550 are listed.

Section 14:Real-Time Clock
No changes.

Section 15:Battery Backup
No changes.

Section 16:Instruction Set Details
No changes.

Section 17:Troubleshoooting
No changes.

Section 18:Analog-to-Digital Converter
This is a new section describing the A/D converter found on the DS87C550.

Section 19:Pulse Width Modulator
This is a new section describing the PWM functions found on the DS87C550.

SECTION 2:ORDERING INFORMATION

The High-Speed Microcontroller family follows the part numbering convention shown below. Note that not all combinations of devices are planned to be made available. Refer to individual data sheet for available versions.

DS87C550-QCL

SPEED:	D	18 MHz
	G	25 MHz
	L	33 MHz
	R	40 MHz
	S	50 MHz
TEMPERATURE:	C	0 °C to 70 °C
PACKAGE:	M	DIP
	Q	PLCC
	E	Thin Quad Flat Pack (TQFP)
	F	Quad Flat Pack (QFP)
	W	Windowed Ceramic DIP
	K	Windowed Ceramic PLCC
OPERATING VOLTAGE:	0	+5V
	3	+3V OR WIDE VOLTAGE
MEMORY TYPE:	0	ROMLESS
	3	FACTORY PROGRAMMED MASK ROM
	7	EPROM (WINDOWED OR OTP PACKAGES)
	9	FLASH

SECTION 3:ARCHITECTURE

No changes.

SECTION 4:PROGRAMMING MODEL

SPECIAL FUNCTION REGISTERS

The following table identifies the complete SFR map for the DS87C550.

DS87C550 SPECIAL FUNCTION REGISTER LOCATIONS : **Table 550UG-1**

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	**ID1**	**ID0**	**TSL**	-	-	-	-	SEL	86h
PCON	SMOD_0	SMOD0	**OFDF**	**OFDE**	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	8Eh
P1	P1.7 ***TXD1***	P1.6 ***RXD1***	P1.5 ***T2EX***	P1.4 ***T2***	P1.3 ***INT5/CT3***	P1.2 ***INT4/CT2***	P1.1 ***INT3/CT1***	P1.0 ***INT2/CT0***	90h
RCON	-	-	-	-	CKRDY	RGMD	RGSL	BGS	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
PMR	CD1	CD0	SWB	**CTM**	**4X / $\overline{2X}$**	ALEOFF	DME1	DME0	9Fh
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0
SADDR0									A1h
SADDR1									A2h
IE	EA	EAD	ES1	ES0	ET1	EX1	ET0	EX0	A8h
CMPL0									A9h
CMPL1									AAh
CMPL2									ABh
CPTL0									ACh
CPTL1									ADh
CPTL2									AEh
CPTL3									AFh
P3	P3.7 $\overline{RD}$	P3.6 $\overline{WR}$	P3.5 T1	P3.4 T0	P3.3 $\overline{INT1}$	P3.2 $\overline{INT0}$	P3.1 TXD0	P3.0 RXD0	B0h
ADCON1	**STRT / $\overline{BSY}$**	**EOC**	**CONT / $\overline{SS}$**	**ADEX**	**WCQ**	**WCM**	**ADON**	**WCIO**	B2h
ADCON2	**OUTCF**	**MUX2**	**MUX1**	**MUX0**	**APS3**	**APS2**	**APS1**	**APS0**	B3h
ADMSB									B4h
ADLSB									B5h
WINHI									B6h
WINLO									B7h
IP	-	**PAD**	***PS1***	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	$\overline{RL2}$	BEh
T2MOD	-	-	-	-	-	-	T2OE	DCEN	BFh

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P4	**P4.7 CMT1**	**P4.6 CMT0**	**P4.5 CMSR5**	**P4.4 CMSR4**	**P4.3 CMSR3**	**P4.2 CMSR2**	**P4.1 CMSR1**	**P4.0 CMSR0**	C0h
ROMSIZE	-	-	-	-	-	RMS2	RMS1	RMS0	C2h
STATUS	PIP	HIP	LIP	-	SPTA1	SPRA1	SPTA0	SPRA0	C5h
TA	1	1	1	1	1	1	1	1	C7h
T2IR	**-**	**CM2F**	**CM1F**	**CM0F**	**IE5/CF3**	**IE4/CF2**	**IE3/CF1**	**IE2/CF0**	C8h
CMPH0									C9h
CMPH1									CAh
CMPH2									CBh
CPTH0									CCh
CPTH1									CDh
CPTH2									CEh
CPTH3									CFh
PSW	CY	AC	F0	RS1	RS0	OV	F1	P	D0h
PW0FG									D2h
PW1FG									D3h
PW2FG									D4h
PW3FG									D5h
PWMADR	**ADRS**	**-**	**-**	**-**	**-**	**-**	**PWE1**	**PWE0**	D6h
SCON1	***SM0/FE_1***	***SM1_1***	***SM2_1***	***REN_1***	***TB8_1***	***RB8_1***	***TI_1***	***RI_1***	D8h
SBUF1									D9h
PWM0									DCh
PWM1									DDh
PWM2									DEh
PWM3									DFh
ACC									E0h
PW01CS	**PW0S2**	**PW0S1**	**PW0S0**	**PW0EN**	**PW1S2**	**PW1S1**	**PW1S0**	**PW1EN**	E1h
PW23CS	**PW2S2**	**PW2S1**	**PW2S0**	**PW2EN**	**PW3S2**	**PW3S1**	**PW3S0**	**PW3EN**	E2h
PW01CON	**PW0F**	**PW0DC**	**PW0OE**	**PW0T/C**	**PW1F**	**PW1DC**	**PW1OE**	**PW1T/C**	E3h
PW23CON	**PW2F**	**PW2DC**	**PW2OE**	**PW2T/C**	**PW3F**	**PW3DC**	**PW3OE**	**PW3T/C**	E4h
RLOADL									E6h
RLOADH									E7h
EIE	ET2	ECM2	ECM1	ECM0	EX5/EC3	EX4/EC2	EX3/EC1	EX2/EC0	E8h
T2SEL	**TF2S**	**TF2BS**	**-**	**TF2B**	**-**	**-**	**T2P1**	**T2P0**	EAh
CTCON	$\overline{\text{CT3}}$	**CT3**	$\overline{\text{CT2}}$	**CT2**	$\overline{\text{CT1}}$	**CT1**	$\overline{\text{CT0}}$	**CT0**	EBh
TL2									ECh
TH2									EDh
SETR	**TGFF1**	**TGFF0**	**CMS5**	**CMS4**	**CMS3**	**CMS2**	**CMS1**	**CMS0**	EEh
RSTR	**CMT1**	**CMT0**	**CMR5**	**CMR4**	**CMR3**	**CMR2**	**CMR1**	**CMR0**	EFh
B									FOh
P6	**P6.7**	**P6.6**	**P6.5**	**P6.4**	**P6.3**	**P6.2**	**P6.1**	**P6.0**	F1h
EIP	PT2	PCM2	PCM1	PCM0	PX5/PC3	PX4/PC2	PX3/PC1	PX2/PC0	F8h
WDCON	***SMOD_1***	***POR***	***EPFI***	***PFI***	***WDIF***	***WTRF***	***EWT***	***RWT***	FFh

Note: Registers and bits in bold are new to the DS87C550. Registers and bits in bold AND Italic existed in previous high-speed microcontrollers, but at different locations.

DS87C550 SPECIAL FUNCTION REGISTER RESET VALUES : Table 550UG-2

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P0	1	1	1	1	1	1	1	1	80h
SP	0	0	0	0	0	1	1	1	81h
DPL	0	0	0	0	0	0	0	0	82h
DPH	0	0	0	0	0	0	0	0	83h
DPL1	0	0	0	0	0	0	0	0	84h
DPH1	0	0	0	0	0	0	0	0	85h
DPS	0	0	0	0	0	1	0	0	86h
PCON	0	0	Special	0	0	0	0	0	87h
TCON	0	0	0	0	0	0	0	0	88h
TMOD	0	0	0	0	0	0	0	0	89h
TL0	0	0	0	0	0	0	0	0	8Ah
TL1	0	0	0	0	0	0	0	0	8Bh
TH0	0	0	0	0	0	0	0	0	8Ch
TH1	0	0	0	0	0	0	0	0	8Dh
CKCON	0	0	0	0	0	0	0	1	8Eh
P1	1	1	1	1	1	1	1	1	90h
RCON	-	-	-	-	Special	Special	Special	0	91h
SCON0	0	0	0	0	0	0	0	0	98h
SBUF0	0	0	0	0	0	0	0	0	99h
PMR	1	0	0	0	0	0	0	0	9Fh
P2	1	1	1	1	1	1	1	1	A0
SADDR0	0	0	0	0	0	0	0	0	A1h
SADDR1	0	0	0	0	0	0	0	0	A2h
IE	0	0	0	0	0	0	0	0	A8h
CMPL0	0	0	0	0	0	0	0	0	A9h
CMPL1	0	0	0	0	0	0	0	0	AAh
CMPL2	0	0	0	0	0	0	0	0	ABh
CPTL0	0	0	0	0	0	0	0	0	ACh
CPTL1	0	0	0	0	0	0	0	0	ADh
CPTL2	0	0	0	0	0	0	0	0	AEh
CPTL3	0	0	0	0	0	0	0	0	AFh
P3	1	1	1	1	1	1	1	1	B0h
ADCON1	0	0	0	0	0	0	0	0	B2h
ADCON2	0	0	0	0	0	0	0	0	B3h
ADMSB	0	0	0	0	0	0	0	0	B4h
ADLSB	0	0	0	0	0	0	0	0	B5h
WINHI	0	0	0	0	0	0	0	0	B6h
WINLO	0	0	0	0	0	0	0	0	B7h
IP	-	0	0	0	0	0	0	0	B8h
SADEN0	0	0	0	0	0	0	0	0	B9h
SADEN1	0	0	0	0	0	0	0	0	BAh
T2CON	0	0	0	0	0	0	0	0	BEh
T2MOD	-	-	-	-	-	-	0	0	BFh
P4	1	1	1	1	1	1	1	1	C0h
ROMSIZE	0	0	0	0	1	1	0	0	C2h
P5	1	1	1	1	1	1	1	1	C4h
STATUS	0	0	0	1	0	0	0	0	C5h
TA	1	1	1	1	1	1	1	1	C7h
T2IR	-	0	0	0	0	0	0	0	C8h
CMPH0	0	0	0	0	0	0	0	0	C9h
CMPH1	0	0	0	0	0	0	0	0	CAh
CMPH2	0	0	0	0	0	0	0	0	CBh
CPTH0	0	0	0	0	0	0	0	0	CCh
CPTH1	0	0	0	0	0	0	0	0	CDh

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
CPTH2	0	0	0	0	0	0	0	0	CEh
CPTH3	0	0	0	0	0	0	0	0	CFh
PSW	0	0	0	0	0	0	0	0	D0h
PW0FG	0	0	0	0	0	0	0	0	D2h
PW1FG	0	0	0	0	0	0	0	0	D3h
PW2FG	0	0	0	0	0	0	0	0	D4h
PW3FG	0	0	0	0	0	0	0	0	D5h
PWMADR	0	-	-	-	-	-	0	0	D6h
SCON1	0	0	0	0	0	0	0	0	D8h
SBUF1	0	0	0	0	0	0	0	0	D9h
PWM0	0	0	0	0	0	0	0	0	DCh
PWM1	0	0	0	0	0	0	0	0	DDh
PWM2	0	0	0	0	0	0	0	0	DEh
PWM3	0	0	0	0	0	0	0	0	DFh
ACC	0	0	0	0	0	0	0	0	E0h
PW01CS	0	0	0	0	0	0	0	0	E1h
PW23CS	0	0	0	0	0	0	0	0	E2h
PW01CON	0	0	0	0	0	0	0	0	E3h
PW23CON	0	0	0	0	0	0	0	0	E4h
RLOADL	0	0	0	0	0	0	0	0	E6h
RLOADH	0	0	0	0	0	0	0	0	E7h
EIE	0	0	0	0	0	0	0	0	E8h
T2SEL	0	0	-	0	-	-	0	0	EAh
CTCON	0	0	0	0	0	0	0	0	EBh
TL2	0	0	0	0	0	0	0	0	ECh
TH2	0	0	0	0	0	0	0	0	EDh
SETR	1		10	0	0	0	0	0	EEh
RSTR	0	0	0	0	0	0	0	0	EFh
B	0	0	0	0	0	0	0	0	FOh
P6	1	-	1	1	1	1	1	1	F1h
EIP	0	0	0	0	0	0	0	0	F8h
WDCON	0	Special	0	Special	0	Special	Special	0	FFh

Port 0 (P0)

	7	6	5	4	3	2	1	0
SFR 80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

P0.7-0 **Port 0.** This port functions as a multiplexed address/data bus during external memory access, and as a general purpose I/O port on devices with internal program memory. During external memory cycles, this port drives the LSB of the address when ALE is high, and data when ALE is low. When used as a general purpose I/O, this port is open-drain and requires pull-ups. Writing a 1 to any pin of this port places it in a high impedance mode, which is required if the pin is to be used as an input. Pull-ups are not required when used as a memory interface.

Stack Pointer (SP)

	7	6	5	4	3	2	1	0
SFR 81h	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-1	RW-1	RW-1

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

SP.7-0 **Stack Pointer.** This stack pointer identifies the location where the stack will begin. The stack pointer is incremented before every PUSH operation. This register defaults to 07h after reset.
Bits 7-0

Data Pointer Low 0 (DPL)

	7	6	5	4	3	2	1	0
SFR 82h	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

DPL.7-0 **Data Pointer Low 0.** This register is the low byte of the standard 80C32 16-bit data pointer. DPL and DPH are used to point to non-scratchpad data RAM.
Bits 7-0

Data Pointer High 0 (DPH)

	7	6	5	4	3	2	1	0
SFR 83h	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

DPH.7-0 **Data Pointer High 0.** This register is the high byte of the standard 80C32 16-bit data pointer. DPL and DPH are used to point to non-scratchpad data RAM.
Bits 7-0

Data Pointer Low 1 (DPL1)

	7	6	5	4	3	2	1	0
SFR 84h	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DL1H.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

DPL1.7-0 Bits 7-0 — **Data Pointer Low 1.** This register is the low byte of the auxiliary 16-bit data pointer. When the SEL bit (DPS.0) is set, DPL1 and DPH1 are used in place of DPL and DPH during DPTR operations.

Data Pointer High 1 (DPH1)

	7	6	5	4	3	2	1	0
SFR 85h	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

DPH1.7-0 Bits 7-0 — **Data Pointer High 1.** This register is the high byte of the auxiliary 16-bit data pointer. When the SEL bit (DPS.0) is set, DPL1 and DPH1 are used in place of DPL and DPH during DPTR operations.

Data Pointer Select (DPS)

	7	6	5	4	3	2	1	0
SFR 86h	ID1	ID0	TSL0	-	-	-	-	SEL
	RW-0	RW-0	RW-0	R-0	R-0	R-0	R-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

ID1, ID0 Bits 7-6 — **Increment/Decrement Select Bits** These bits define how the INC DPTR instruction functions in relation to the current DPTR as selected by SEL.

ID1	ID0	SEL = 0	SEL = 1
0	0	Increment DPTR	Increment DPTR1
0	1	Decrement DPTR	Increment DPTR1
1	0	Increment DPTR	Decrement DPTR1
1	1	Decrement DPTR	Decrement DPTR1

TSL Bit 5 — **Toggle Select Bit Enable** This bit allows any instruction involving the data pointer to toggle the SEL bit automatically. When this bit is logic 1, the SEL bit will automatically toggle, otherwise it will not.

Bits 4-1 — Reserved. Read will be indeterminate.

SEL Bit 0 — **Data Pointer Select.** This bit selects the active data pointer.
0 = Instructions that use the DPTR will use DPL and DPH.
1= Instructions that use the DPTR will use DPL1 and DPH1.

Power Control (PCON)

	7	6	5	4	3	2	1	0
SFR 87h	SMOD_0	SMOD0	OFDF	OFDE	GF1	GF0	STOP	IDLE
	RW-0	RW-0	RW-*	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset; *=see description

SMOD_0
Bit 7

Serial Port 0 Baud Rate Doubler Enable. This bit enables/disables the serial baud rate doubling function for Serial Port 0.

0 = Serial Port 0 baud rate will be that defined by baud rate generation equation.

1 = Serial Port 0 baud rate will be double that defined by baud rate generation equation.

SMOD0

Bit 6

Framing Error Detection Enable. This bit selects function of the SCON0.7 and SCON1.7 bits.

0 = SCON0.7 and SCON1.7 control the SM0 function defined for the SCON0 and SCON1 registers.

1 = SCON0.7 and SCON1.7 are converted to the Framing Error (FE) flag for the respective Serial Port.

OFDF

Bit 5

Oscillator Fail Detect Flag. This bit is set if a reset is caused by oscillator failure and must be cleared by software.

OFDE

Bit 4

Oscillator Fail Detect Enable. This bit enables the oscillator fail detect circuitry when 1 and disables the feature when 0.

GF1
Bit 3

General Purpose User Flag 1. This is a general purpose flag for software control.

GF0
Bit 2

General Purpose User Flag 0. This is a general purpose flag for software control.

STOP
Bit 1

Stop Mode Select. Setting this bit will stop program execution, halt the CPU oscillator and internal timers, and place the CPU in a low-power mode. This bit will always be read as a 0. Setting this bit while the Idle bit is set will place the device in an undefined state.

IDLE
Bit 0

Idle Mode Select. Setting this bit will stop program execution but leave the CPU oscillator, timers, serial ports, and interrupts active. This bit will always be read as a 0.

Timer/Counter Control (TCON)

	7	6	5	4	3	2	1	0
SFR 88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

TF1
Bit 7

Timer 1 Overflow Flag. This bit indicates when Timer 1 overflows its maximum count as defined by the current mode. This bit can be cleared by software and is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.

0 = No Timer 1 overflow has been detected.
1 = Timer 1 has overflowed its maximum count.

TR1
Bit 6

Timer 1 Run Control. This bit enables/disables the operation of Timer 1.

0 = Timer 1 is halted.

1 = Timer 1 is enabled.

TF0
Bit 5

Timer 0 Overflow Flag. This bit indicates when Timer 0 overflows its maximum count as defined by the current mode. This bit can be cleared by software and is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine or by software.

0 = No Timer 0 overflow has been detected.
1 = Timer 0 has overflowed its maximum count.

TR0
Bit 4

Timer 0 Run Control. This bit enables/disables the operation of Timer 0. Halting this timer will preserve the current count in THO and TL0.

0 = Timer 0 is halted.
1 = Timer 0 is enabled.

IE1
Bit 3

Interrupt 1 Edge Detect. This bit is set when an edge/level of the type defined by IT1 is detected. If IT1=1, this bit will remain set until cleared in software or the start of the External Interrupt 1 service routine. If IT1=0, this bit will inversely reflect the state of the $\overline{\text{INT1}}$ pin.

IT1
Bit 2

Interrupt 1 Type Select. This bit selects whether the $\overline{\text{INT1}}$ pin will detect edge or level triggered interrupts.

0 = $\overline{\text{INT1}}$ is level triggered.
1 = $\overline{\text{INT1}}$ is edge triggered.

IE0
Bit 1

Interrupt 0 Edge Detect. This bit is set when an edge/level of the type defined by IT0 is detected. If IT0=1, this bit will remain set until cleared in software or the start of the External Interrupt 0 service routine. If IT0=0, this bit will inversely reflect the state of the $\overline{\text{INT0}}$ pin

IT0
Bit 0

Interrupt 0 Type Select. This bit selects whether the $\overline{\text{INT0}}$ pin will detect edge or level triggered interrupts.

0 = $\overline{\text{INT0}}$ is level triggered.
1 = $\overline{\text{INT0}}$ is edge triggered.

Timer Mode Control (TMOD)

	7	6	5	4	3	2	1	0
SFR 89h	GATE	$C/\overline{T}$	M1	M0	GATE	$C/\overline{T}$	M1	M0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

GATE
Bit 7

Timer 1 Gate Control. This bit enable/disables the ability of Timer 1 to increment.

0 = Timer 1 will clock when TR1=1, regardless of the state of $\overline{INT1}$.

1 = Timer 1 will clock only when TR1=1 and $\overline{INT1}$=1.

$C/\overline{T}$
Bit 6

Timer 1 Counter/Timer Select.

0 = Timer 1 is incremented by internal clocks (timer).

1 = Timer 1 is incremented by pulses on T1 when TR1 (TCON.6) is 1 (counter).

M1, M0
Bits 5-4

Timer 1 Mode Select. These bits select the operating mode of Timer 1.

M1	M0	Mode
0	0	Mode 0: 8 bit with 5-bit prescale
0	1	Mode 1: 16 bit with no prescale.
1	0	Mode 2: 8 bit with auto-reload
1	1	Mode 3: Timer 1 is halted, but holds its count.

GATE
Bit 3

Timer 0 Gate Control. This bit enables/disables that ability of Timer 0 to increment.

0 = Timer 0 will clock when TR0=1, regardless of the state of $\overline{INT0}$.

1 = Timer 0 will clock only when TR0=1 and $\overline{INT0}$ = 1.

$C/\overline{T}$
Bit 2

Timer 0 Counter/Timer Select.

0 = Timer incremented by internal clocks (timer).

1 = Timer 1 is incremented by pulses on T0 when TR0 (TCON.4) is 1 (counter).

M1, M0
Bits 1-0

Timer 0 Mode Select. These bits select the operating mode of Timer 0. When Timer 0 is in mode 3, TL0 is started/stopped by TR0 and TH0 is started/stopped by TR1. Run control for Timer 1 is then provided via the Timer 1 mode selection.

M1	M0	Mode
0	0	Mode 0: 8 bit with 5-bit prescale
0	1	Mode 1: 16 bit no prescale
1	0	Mode 2: 8 bit with auto-reload
1	1	Mode 3: Timer 0 is two 8 bit counters.

Timer 0 LSB (TL0)

	7	6	5	4	3	2	1	0
SFR 8Ah	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

TL0.7-0 **Timer 0 LSB.** This register contains the least significant byte of Timer 0.
Bits 7-0

Timer 1 LSB (TL1)

	7	6	5	4	3	2	1	0
SFR 8Bh	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

TL1.7-0 **Timer 1 LSB.** This register contains the least significant byte of Timer 1.
Bits 7-0

Timer 0 MSB (TH0)

	7	6	5	4	3	2	1	0
SFR 8Ch	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

TH0.7-0 **Timer 0 MSB.** This register contains the most significant byte of Timer 0.
Bits 7-0

Timer 1 MSB (TH1)

	7	6	5	4	3	2	1	0
SFR 8Dh	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

TH1.7-0 **Timer 1 MSB.** This register contains the most significant byte of Timer 1.
Bits 7-0

Clock Control (CKCON)

	7	6	5	4	3	2	1	0
SFR 8Eh	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-1

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

WD1, WD0
Bits 7-6

Watchdog Timer Mode Select 1-0. These bits determine the watchdog timer time-out period. The timer divides the crystal (or external oscillator) frequency by a programmable value as shown below. The divider value is expressed in crystal (oscillator) cycles. The settings of the system clock control bits $4X/\overline{2X}$ (PMR.3) and CD1:0 (PMR.7-6) will affect the clock input to the watchdog timer and therefore its time-out period as shown below. All Watchdog Timer reset time-outs follow the setting of the interrupt flag by 512 clocks. The DS87C550 does not incorporate a watchdog interrupt, but a similar effect may be achieved by polling its flag.

Watchdog Interrupt Flag Time-Out Periods (in crystal clocks)

$4X/\overline{2X}$	CD1:0	WD1:0=00	WD1:0=01	WD1:0=10	WD1:0=11
1	00	2^{15}	2^{18}	2^{21}	2^{24}
0	00	2^{16}	2^{19}	2^{22}	2^{25}
X	01	2^{17}	2^{20}	2^{23}	2^{26}
X	10	2^{17}	2^{20}	2^{23}	2^{26}
X	11	2^{25}	2^{28}	2^{31}	2^{34}

T2M
Bit 5

Timer 2 Clock Select. This bit controls the division of the system clock that drives Timer 2. This bit has no effect when the timer is in baud rate generator or clock output modes. Clearing this bit to 0 maintains 80C32 compatibility. This bit has no effect on instruction cycle timing.

0 = Timer 2 uses a divide by 12 of the crystal frequency.

1 = The divide ratio of Timer 2 is determined by the CD1, CD0, and $4X/\overline{2X}$ as shown below.

T1M
Bit 4

Timer 1 Clock Select. This bit controls the division of the system clock that drives Timer 1. Clearing this bit to 0 maintains 80C32 compatibility. This bit has no effect on instruction cycle timing.

0 = Timer 1 uses a divide by 12 of the crystal frequency.

1 = The divide ratio of Timer 1 is determined by the CD1, CD0, and $4X/\overline{2X}$ as shown below.

T0M
Bit 3

Timer 0 Clock Select. This bit controls the division of the system clock that drives Timer 0. Clearing this bit to 0 maintains 80C32 compatibility. This bit has no effect on instruction cycle timing.

0 = Timer 0 uses a divide by 12 of the crystal frequency.

1 = The divide ratio of Timer 0 is determined by the CD1, CD0, and $4X/\overline{2X}$ as shown below.

Timer 0, 1, and 2 values as a function of various clock control settings

CD1:0	4X/ $\overline{2X}$	OSCILLATOR CYCLES PER MACHINE. CYCLE	OSC CYCLES PER TIMER 0/1/2 CLOCK.		OSC CYCLES PER TIMER 2 CLK, BAUD RATE GEN.	OSC CYCLES PER SERIAL PORT CLK, MODE 0		OSC CYCLES PER SERIAL PORT CLK, MODE 2	
			TxM=0	TxM=1		SM2=0	SM2=1	SMOD=0	SMOD=1
00	1	1	12	1	2	3	1	64	32
00	0	2	12	2	2	6	2	64	32
01	x	Reserved							
10	x	4	12	4	2	12	4	64	32
11	x	1024	3072	1024	512	3072	1024	64	32

MD2, MD1, MD0
Bits 2-0

Stretch MOVX Select 2-0. These bits select the time by which external MOVX cycles are to be stretched. This allows slower memory or peripherals to be accessed without using ports or manual software intervention. The $\overline{RD}$ or $\overline{WR}$ strobe will be stretched by the specified interval, which will be transparent to the software except for the increased time to execute to MOVX instruction. All internal MOVX instructions on devices containing MOVX SRAM are performed at the 2 machine cycle rate.

MD2	MD1	MD0	Stretch Value	MOVX Duration
0	0	0	0	2 Machine Cycles
0	0	1	1	3 Machine Cycles (reset default)
0	1	0	2	4 Machine Cycles
0	1	1	3	5 Machine Cycles
1	0	0	4	9 Machine Cycles
1	0	1	5	10 Machine Cycles
1	1	0	6	11 Machine Cycles
1	1	1	7	12 Machine Cycles

Port 1 (P1)

	7	6	5	4	3	2	1	0
SFR 90h	P1.7 TXD1	P1.6 RXD1	P1.5 T2EX	P1.4 T2	P1.3 $\overline{\text{INT5}}$ / CT3	P1.2 $\overline{\text{INT4}}$ / CT2	P1.1 $\overline{\text{INT3}}$ / CT1	P1.0 $\overline{\text{INT2}}$ / CT0
	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

P1.7-0
Bits 7-0

General Purpose I/O Port 1. This register functions as a general purpose I/O port. In addition, all the pins have an alternative function listed below. P1.2-7 contain functions that are new to the 80C32 architecture. The Timer 2 functions on pins P1.1-0 are available on the 80C32, but not the 80C31. Each of the functions is controlled by several other SFRs. The associated Port 1 latch bit must contain a logic one before the pin can be used in its alternate function capacity.

TXD1
Bit 7

Serial Port 1 Transmit. This pin transmits the serial port 1 data in serial port modes 1, 2, 3 and emits the synchronizing clock in serial port mode 0.

RXD1
Bit 6

Serial Port 1 Receive. This pin receives the serial port 1 data in serial port modes 1, 2, 3 and is a bi-directional data transfer pin in serial port mode 0.

T2EX
Bit 5

Timer 2 Capture/Reload Trigger. A 1 to 0 transition on this pin will cause the value in the T2 registers to be transferred into the capture registers if enabled by EXEN2 (T2CON.3). When in auto–reload mode, a 1 to 0 transition on this pin will reload the timer 2 registers with the value in RCAP2L and RCAP2H if enabled by EXEN2 (T2CON.3).

T2
Bit 4

Timer 2 External Input. A 1 to 0 transition on this pin will cause timer 2 increment or decrement depending on the timer configuration. This mode of operation is enabled by setting the $C/\overline{T2}$ bit (T2CON.1).

$\overline{\text{INT5}}$ / CT3
Bit 3

External Interrupt 5/Capture 3 Input. In normal operation, a falling edge on this pin will cause an external interrupt 5 (if enabled). If capture channel 3 is enabled, this pin acts as a capture command input.

$\overline{\text{INT4}}$ / CT2
Bit 2

External Interrupt 4/Capture 2 Input. In normal operation, a falling edge on this pin will cause an external interrupt 4 (if enabled). If capture channel 2 is enabled, this pin acts as a capture command input.

$\overline{\text{INT3}}$ / CT1
Bit 1

External Interrupt 3/Capture 1 Input. In normal operation, a falling edge on this pin will cause an external interrupt 3 (if enabled). If capture channel 1 is enabled, this pin acts as a capture command input.

$\overline{\text{INT2}}$ / CT0
Bit 0

External Interrupt 2/Capture 0 Input. In normal operation, a falling edge on this pin will cause an external interrupt 2 (if enabled). If capture channel 0 is enabled, this pin acts as a capture command input.

Ring Oscillator Control (RCON)

	7	6	5	4	3	2	1	0
SFR 91h	-	-	-	-	CKRDY	RGMD	RGSL	BGS
					R-*	R-*	RW-*	RT-0

R=Unrestricted Read, W=Unrestricted Write, T=Timed Access Write Only, -n =Value after Reset, * = See Description

Bits 7 – 4 Reserved. Read data will be indeterminate.

CKRDY
Bit 3

Clock Ready This bit indicates the status of the start-up period delay used to establish the crystal oscillator or crystal multiplier warm-up period of 65536 crystal oscillator periods. A 1 indicates that the period is complete otherwise it is not. This bit is cleared after a reset or when exiting STOP mode. It is also cleared when the clock multiplier is enabled (CTM bit of the PMR register set). Once the CKRDY bit is set, the lockout preventing CD1:CD0 from being modified is removed, and clock multiplier may then be selected as the clock source.

RGMD
Bit 2

Ring Oscillator Mode This bit indicates the status of the ring oscillator. If 0, the ring is not being used, and if 1, the system is running from the ring. This bit must be cleared before the RGSL can be modified, before the Clock Control divider bits (CD1:CD0) can be changed to any condition other than divide by 4 mode, and before enabling the clock multiplier (setting the CTM bit).

RGSL
Bit 1

Ring Oscillator Select This bit enables (1) or disables (0) the ring oscillator. If enabled, the ring oscillator will be used as the system clock source after exiting STOP mode until the end of start-up period delay (65536 crystal oscillator periods). At the end of this delay, the crystal oscillator will automatically be switched in as the system clock source. This bit is reset only by a Power-On Reset.

BGS
Bit 0

Band Gap Select This bit enables (1) or disables (0) the band-gap voltage reference in STOP mode.

Serial Port 0 Control (SCON0)

	7	6	5	4	3	2	1	0
SFR 98h	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	T1_0	R1_0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

SM0-2
Bits 7-5

Serial Port Mode These bits control the mode of serial port 0. In addition the SM0 and SM2_0 bits have secondary functions as shown below.

SM0	SM1	SM2	MODE	FUNCTION	LENGTH	PERIOD
0	0	0	0	Synchronous	8 bits	12 t_{CLK}
0	0	1	0	Synchronous	8 bits	4 t_{CLK}
0	1	X	1	Asynchronous	10 bits	Timer 1 or 2 baud rate equation
1	0	0	2	Asynchronous	11 bits	64 t_{CLK} (SMOD=0) 32 t_{CLK} (SMOD=1)
1	0	1	1	Asynchronous w/ Multiprocessor communication	11 bits	64 t_{CLK} (SMOD=0) 32 t_{CLK} (SMOD=1)
1	1	0	3	Asynchronous	11 bits	Timer 1 or 2 baud rate equation
1	1	1	3	Asynchronous w/ Multiprocessor communication	11 bits	Timer 1 or 2 baud rate equation

SM0/FE_0
Bit 7

Framing Error Flag. When SMOD0 (PCON.6)=0, this bit (SM0) is used to select the mode for serial port 0. When SMOD0=1, this bit (FE) will be set upon detection of an invalid stop bit. When used as FE, this bit must be cleared in software. Once the SMOD0 bit is set, modifications to this bit will not affect the serial port mode settings. Although accessed from the same register, internally the data for bits SM0 and FE are stored in different locations.

SM1_0
Bit 6

No alternate function.

SM2_0
Bit 5

Multiple CPU Communications. The function of this bit is dependent on the serial port 0 mode.

Mode 0: Selects 12 t_{CLK} or 4 t_{CLK} period for synchronous serial port 0 data transfers.

Mode 1: When set, reception is ignored (RI_0 is not set) if invalid stop bit received.

Mode 2/3: When this bit is set, multiprocessor communications are enabled in modes 2 and 3. This will prevent the RI_0 bit from being set, and an interrupt being asserted, if the 9th bit received is not 1.

REN_0
Bit 4

Receiver Enable. This bit enable/disables the serial port 0 receiver shift register.

0 = Serial port 0 reception disabled.

1= Serial port 0 receiver enabled (modes 1, 2, 3). Setting this bit will initiate synchronous reception in mode 0.

TB8_0
Bit 3

9th Transmission Bit State. This bit defines the state of the 9th transmission bit in serial port 0 modes 2 and 3.

RB8_0
Bit 2

9th Received Bit State. This bit identifies that state of the 9th reception bit of received data in serial port 0 modes 2 and 3. In serial port mode 1, when SM2_0=0, RB8_0 is the state of the stop bit. RB8_0 is not used in mode 0.

TI_0
Bit 1

Transmitter Interrupt Flag. This bit indicates that data in the serial port 0 buffer has been completely shifted out. In serial port mode 0, TI_0 is set at the end of the 8th data bit. In all other modes, this bit is set at the end of the last data bit. This bit must be manually cleared by software.

RI_0
Bit 0

Receiver Interrupt Flag. This bit indicates that a byte of data has been received in the serial port 0 buffer. In serial port mode 0, RI_0 is set at the end of the 8th bit. In serial port mode 1, RI_0 is set after the last sample of the incoming stop bit subject to the state of SM2_0. In modes 2 and 3, RI_0 is set after the last sample of RB8_0. This bit must be manually cleared by software.

Serial Data Buffer 0 (SBUF0)

	7	6	5	4	3	2	1	0
SFR 99h	SBUF0.7	SBUF0.6	SBUF0.5	SBUF0.4	SBUF0.3	SBUF0.2	SBUF0.1	SBUF0.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

SBUF0.7-0
Bits 7-0

Serial Data Buffer 0. Data for serial port 0 is read from or written to this location. The serial transmit and receive buffers are separate registers, but both are addressed at this location.

Power Management Register (PMR)

	7	6	5	4	3	2	1	0
SFR 9Fh	CD1	CD0	SWB	CTM	$4X/\overline{2X}$	ALEOFF	DME1	DME0
	R*-1	R*-0	RW-0	R*-0	R*-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset; * = See Description

CD1,CD0
Bits 7, 6

Clock Divide Control : These bits select the source of the system clock and determine the number of clocks per machine cycle as indicated in the table.

CD1	CD0	Clock source; divisor
0	**0**	Crystal multiplier; 1 or 2 clocks per machine cycle (as determined by the $4X/\overline{2X}$ bit.
0	**1**	Reserved.
1	**0**	Crystal/external oscillator; 4 clocks per machine cycle (default)
1	**1**	Crystal/external oscillator; 1024 clocks per machine cycle.

A default of 10b is selected after all forms of reset and Stop mode exits. When changing these bits certain restrictions must be observed. The default state is the only state that any other state can be changed to or from. As an example, attempting to change from the crystal multiplier clock source (either divide by 1 or 2) directly to the crystal/external oscillator divided by 1024 will result in CD1 and CD0 remaining unchanged.

SWB
Bit 5

Switch Back Enable This bit enables (1) or disables (0) the switch-back function. When enabled, switchback will allow the processor to automatically switch from divide by 1024 mode to divide by 4 mode when an external interrupt is acknowledged or when a start bit of a serial character is recognized on an active serial port.

CTM
Bit 4

Crystal Multiplier Enable This bit enables (1) or disables (0) the crystal multiplier function. By clearing this bit, the power required by this circuitry can be saved. Setting this bit will automatically clear the CKRDY bit and initiate the start-up period delay. Until the start-up period has elapsed, CKRDY will remain cleared and it will be impossible to change the CD1 & CD0 bits to select the crystal multiplier. Also, CTM cannot be changed unless CD1 & CD0 = 10b and RGMD is cleared to 0. This bit is automatically cleared to 0 when the processor enters Stop mode.

$4X/\overline{2X}$
Bit 3

Clock Multiplier Selection This bit selects the clock multiplication factor as shown.
$4X/\overline{2X}$ = 0 Sets the frequency multiplier to 2 times the incoming clock.
$4X/\overline{2X}$ = 1 Sets the frequency multiplier to 4 times the incoming clock.
This bit can only be altered when the Crystal Multiplier Enable bit (CTM) is cleared. Therefore it must be set for the desired multiplication factor prior to setting the CTM bit.

ALEOFF
Bit 2

ALE Disable When set to 1, this bit disables ALE during on-board memory accesses. Any off-chip memory access will cause ALE to automatically toggle regardless of the state of this bit. When this bit is 0, ALE toggles for all memory accesses whether the memory is inside or outside of the chip.

DME1,DME0
Bits 1, 0

DME1	DME0	Data Memory Range	Memory Access
0	0	0000h – FFFFh	External data memory (default)
0	1	0000h – 03FFh	1K Internal SRAM data memory
		0400h – FFFFh	External data memory
1	0	Reserved	Reserved
1	0	0000h – 3FFFh	1K Internal SRAM data memory
		0400h – FFFBh	Reserved.
		FFFCh	System control byte (EPROM Read-Only).
		FFFDh – FFFF	Reserved.

Port 2 (P2)

	7	6	5	4	3	2	1	0
SFR A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

P2.7-0
Bits 7-0

Port 2. This port functions as an address bus during external memory access, and as a general purpose I/O port on devices which incorporate internal program memory. During external memory cycles, this port will contain the MSB of the address. The Port 2 latch does not control general purpose I/O pins on ROMLESS devices, but is still used to hold the address MSB during register-indirect data memory operations such as MOVX A, @R1.

Slave Address Register 0 (SADDR0)

	7	6	5	4	3	2	1	0
SFR A1h	SADDR0.7	SADDR0.6	SADDR0.5	SADDR0.4	SADDR0.3	SADDR0.2	SADDR0.1	SADDR0.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

SADDR0.7-0
Bits 7-0

Slave Address Register 0. This register is programmed by the user with the given or broadcast address assigned to serial port 0.

Slave Address Register 1 (SADDR1)

	7	6	5	4	3	2	1	0
SFR A2h	SADDR1.7	SADDR1.6	SADDR1.5	SADDR1.4	SADDR1.3	SADDR1.2	SADDR1.1	SADDR1.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

SADDR1.7-0 Bits 7-0 — **Slave Address Register 1.** This register is programmed by the user with the given or broadcast address assigned to serial port 1.

Interrupt Enable (IE)

	7	6	5	4	3	2	1	0
SFR A8h	EA	EAD	ES1	ES0	ET1	EX1	ET0	EX0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

EA Bit 7 — **Global Interrupt Enable.** This bit controls the global masking of all interrupts except Power-Fail Interrupt, which is enabled by the EPFI bit (WDCON.5).

0 = Disable all interrupt sources. This bit overrides individual interrupt mask settings.

1 = Enable all individual interrupt masks. Individual interrupts will occur if enabled.

EAD Bit 6 — **A/D Interrupt Enable.** This bit controls the masking of the A/D Converter interrupt.

0 = Disable the A/D interrupt.

1 = Enable interrupt requests generated by the EOC (ADCON.6) flag.

ES1 Bit 5 — **Enable Serial Port 1 Interrupt.** This bit controls the masking of the Serial Port 1 interrupt.

0 = Disable all Serial Port 1 interrupts.

1 = Enable interrupt requests generated by the RI_1 (SCON1.0) or TI_1 (SCON1.1) flags.

ES0 Bit 4 — **Enable Serial Port 0 Interrupt.** This bit controls the masking of the Serial port 0 interrupt.

0 = Disable all serial port 0 interrupts.

1 = Enable interrupt requests generated by the RI_0 (SCON0.0) or TI_0 (SCON0.1) flags.

ET1 Bit 3 — **Enable Timer 1 Interrupt.** This bit controls the masking of the Timer 1 interrupt.

0 = Disable all Timer 1 interrupts.

1 = Enable all interrupt requests generated by the TF1 flag (TCON.7).

EX1 Bit 2 — **Enable External Interrupt 1.** This bit controls the masking of external interrupt 1.

0 = Disable external interrupt 1.

1 = Enable all interrupt requests generated by the $\overline{INT1}$ pin.

ET0 Bit 1 — **Enable Timer 0 Interrupt.** This bit controls the masking of the Timer 0 interrupt.

0 = Disable all Timer 0 interrupts.

1 = Enable all interrupt requests generated by the TF0 flag (TCON.5).

EX0 Bit 0 — **Enable External Interrupt 0.** This bit controls the masking of external interrupt 0.

0 = Disable external interrupt 0.

1 = Enable all interrupt requests generated by the $\overline{INT0}$ pin.

Compare Register Zero LSB (CMPL0)

	7	6	5	4	3	2	1	0
SFR A9h	CMPL0.7	CMPL0.6	CMPL0.5	CMPL0.4	CMPL0.3	CMPL0.2	CMPL0.1	CMPL0.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CMPL0.7-0 Bits 7-0 — **Compare Register Zero LSB.** This register is one of three used to store the least significant 8-bit value for the Timer 2's comparison functions. When a match occurs between Timer 2 and the contents of 16-bit register pair made of CMPH0 & CMPL0, port pins P4.5 through P4.0 are set if the corresponding compare match set enable bits (CMS5:0=SETR.5:0) are set.

Compare Register One LSB (CMPL1)

	7	6	5	4	3	2	1	0
SFR AAh	CMPL1.7	CMPL1.6	CMPL1.5	CMPL1.4	CMPL1.3	CMPL1.2	CMPL1.1	CMPL1.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CMPL1.7-0 Bits 7-0 — **Compare Register One LSB.** This register is one of three used to store the least significant 8-bit value for the Timer 2's comparison functions. When a match occurs between Timer 2 and the contents of 16-bit register pair made of CMPH1 & CMPL1, port pins P4.5 through P4.0 are reset if the corresponding compare match reset enable bits (CMR5:0=RSTR.5:0) are set.

Compare Register Two LSB (CMPL2)

	7	6	5	4	3	2	1	0
SFR ABh	CMPL2.7	CMPL2.6	CMPL2.5	CMPL2.4	CMPL2.3	CMPL2.2	CMPL2.1	CMPL2.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CMPL2.7-0
Bits 7-0

Compare Register Two LSB. This register is one of three used to store the least significant 8-bit value for the Timer 2's comparison functions. When a match occurs between Timer 2 and the contents of 16-bit register pair made of CMPH2 & CMPL2, port pin P4.6 will toggle if the corresponding compare match toggle enable bit CMTE0 (RSTR.6) is set. Similarly on a match, P4.7 will toggle if the corresponding compare match toggle enable bit CMTE1 (RSTR.7) is set.

Capture Register Zero LSB (CPTL0)

	7	6	5	4	3	2	1	0
SFR ACh	CPTL0.7	CPTL0.6	CPTL0.5	CPTL0.4	CPTL0.3	CPTL0.2	CPTL0.1	CPTL0.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CPTL0.7-0
Bits 7-0

Capture Register Zero LSB. This register is used to capture the least significant 8-bit value for the Timer 2's channel 0 capture function. When a transition occurs on the INT2/CT0 pin, the LSB of Timer 2 is captured in this register on the rising edge if the CT0=CTCON.0 enable bit is set or on the falling edge if the $\overline{CT0}$=CTCON.1 enable is set. Setting both enable bits will cause a capture to occur on both edges.

Capture Register One LSB (CPTL1)

	7	6	5	4	3	2	1	0
SFR ADh	CPTL1.7	CPTL1.6	CPTL1.5	CPTL1.4	CPTL1.3	CPTL1.2	CPTL1.1	CPTL1.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CPTL1.7-0
Bits 7-0

Capture Register One LSB. This register is used to capture the least significant 8-bit value for the Timer 2's channel 1 capture function. When a transition occurs on the INT3/CT1 pin, the LSB of Timer 2 is captured in this register on the rising edge if the CT1=CTCON.1 enable bit is set or on the falling edge if the $\overline{CT1}$=CTCON.3 enable is set. Setting both enable bits will cause a capture to occur on both edges.

Capture Register Two LSB (CPTL2)

	7	6	5	4	3	2	1	0
SFR AEh	CPTL2.7	CPTL2.6	CPTL2.5	CPTL2.4	CPTL2.3	CPTL2.2	CPTL2.1	CPTL2.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CPTL2.7-0
Bits 7-0

Capture Register Two LSB. This register is used to capture the least significant 8-bit value for the Timer 2's channel 2 capture function. When a transition occurs on the INT4/CT2 pin, the LSB of Timer 2 is captured in this register on the rising edge if the CT2=CTCON.4 enable bit is set or on the falling edge if the $\overline{CT2}$=CTCON.5 enable is set. Setting both enable bits will cause a capture to occur on both edges.

Capture Register Three LSB (CPTL3)

	7	6	5	4	3	2	1	0
SFR AFh	CPTL3.7	CPTL3.6	CPTL3.5	CPTL3.4	CPTL3.3	CPTL3.2	CPTL3.1	CPTL3.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CPTL3.7-0
Bits 7-0

Capture Register Three LSB. This register is used to capture the least significant 8-bit value for the Timer 2's channel 3 capture function. When a transition occurs on the INT5/CT3 pin, the LSB of Timer 2 is captured in this register on the rising edge if the CT3=CTCON.6 enable bit is set or on the falling edge if the $\overline{CT3}$=CTCON.7 enable is set. Setting both enable bits will cause a capture to occur on both edges.

Port 3 (P3)

	7	6	5	4	3	2	1	0
SFR B0h	P3.7 $\overline{\text{RD}}$	P3.6 $\overline{\text{WR}}$	P3.5 T1	P3.4 T0	P3.3 $\overline{\text{INT1}}$	P3.2 $\overline{\text{INT0}}$	P3.1 TXD0	P3.0 RXD0
	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

P3.7-0
Bits 7-0

General Purpose I/O Port 3. This register functions as a general purpose I/O port. In addition, all the pins have an alternative function listed below. Each of the functions is controlled by several other SFRs. The associated Port 3 latch bit must contain a logic one before the pin can be used in its alternate function capacity.

$\overline{\text{RD}}$
Bit 7

External Data Memory Read Strobe. This pin provides an active low read strobe to an external memory or peripheral device.

$\overline{\text{WR}}$
Bit 6

External Data Memory Write Strobe. This pin provides an active low write strobe to an external memory or peripheral device.

T1
Bit 5

Timer/Counter External Input. A 1 to 0 transition on this pin will increment Timer 1 if counter mode is enabled.

T0
Bit 4

Timer/Counter External Input. A 1 to 0 transition on this pin will increment Timer 0 if counter mode is enabled.

$\overline{\text{INT1}}$
Bit 3

External Interrupt 1. A falling edge/low level on this pin will cause an external interrupt 1 if enabled.

$\overline{\text{INT0}}$
Bit 2

External Interrupt 0. A falling edge/low level on this pin will cause an external interrupt 0 if enabled.

TXD0
Bit 1

Serial Port 0 Transmit. This pin transmits the serial port 0 data in serial port modes 1, 2, 3 and emits the synchronizing clock in serial port mode 0.

RXD0
Bit 0

Serial Port 0 Receive. This pin receives the serial port 0 data in serial port modes 1, 2, 3 and is a bi-directional data transfer pin in serial port mode 0.

A/D Converter Control Register 1 (ADCON1)

	7	6	5	4	3	2	1	0
SFR B2h	**STRT / $\overline{\text{BSY}}$**	EOC	**CONT / $\overline{\text{SS}}$**	ADEX	WCQ	WCM	ADON	WCIO
	R*-0	RW-0	RW-0	RW-0	RW-0	R-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset; *=See description

STRT / $\overline{\text{BSY}}$
Bit 7

Start/Busy. When this bit is changed from a 0 to a 1, an A/D conversion starts. It remains set for the duration of the conversion process (regardless of attempts to write 0). Hardware automatically clears this bit upon completion of conversion.

EOC
Bit 6

End Of Conversion. This bit is set by hardware when a conversion is complete. It also serves as an interrupt flag qualified by WCQ and enabled by EAD (IE.7). This bit must be cleared by software and can be set or cleared by software anytime.

CONT / $\overline{\text{SS}}$
Bit 5

Continuous/Single Shot. When set to 1, the A/D converter operates in continuous mode and repeatedly runs conversions once a conversion is initiated. When this bit is cleared, the A/D converter performs one conversion and stops.

ADEX
Bit 4

A/D External Start. When set, this bit allows an A/D conversion to be initiated by the detection of a falling edge on the STADC pin.

WCQ
Bit 3

Window Comparator Qualifier. If set, this bit allows an A/D converter interrupt to occur only when both EOC and WCM bits are set at the end of a conversion. If this bit is cleared, an interrupt will occur (if enabled) every time EOC is set.

WCM
Bit 2

Window Comparator Match. This bit is set by hardware at the end of an A/D conversion result that matches the criteria set by WINHI, WINLO, and WCIO. This bit is not set if there is no match, and it must be cleared by software.

ADON
Bit 1

A/D On. This bit enables (ADON=1) or disables (ADON=0) the A/D function. Changing this bit from a 0 to a 1 requires a warm-up period of 4 µs before a proper conversion can be performed. This bit can be cleared to save power when no conversion is required, and clearing it aborts any conversion in progress. This action also resets the STRT / $\overline{\text{BSY}}$ bit.

WCIO
Bit 0

Window Compare Inside/Outside. When set to 1, the window comparison function looks for A/D results that are outside of the window bounded by the limits set by WINHI and WINLO. When this bit is cleared, the check is for values inside these limits.

A/D Converter Control Register 2 (ADCON2)

	7	6	5	4	3	2	1	0
SFR B3h	OUTCF	MUX2	MUX1	MUX0	APS3	APS2	APS1	APS0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

OUTCF
Bit 7

Output Conversion Format. When this bit is set, the ADMSB register contains the two most significant bits of the 10-bit conversion in the two least significant bit positions, and the remaining bits of the register are cleared. The ADLSB will contain the 8 least significant bits of the conversion. When the OUTCF bit is cleared, the ADMSB will contain the 8 most significant bits and ADLSB will contain the 8 least significant bits of the conversion.

MUX2:0
-Bits 6-4

Multiplexer Select Bits. These bits select the A/D analog channel (ADC7:ADC0) that will be sampled and converted.

MUX2	MUX1	MUX0	Channel
0	0	0	ADC0
0	0	1	ADC1
0	1	0	ADC2
0	1	1	ADC3
1	0	0	ADC4
1	0	1	ADC5
1	1	0	ADC6
1	1	1	ADC7

APS3:0
Bits 3-0

A/D Clock Prescaler Select Bits. These bits determine the A/D's clock prescaler value "N" where this clock period is defined as:

$$t_{ACLK} = t_{MCLK} \times (N+1)$$

where t_{MCLK} is the CPU's Machine Cycle Clock (the oscillator or crystal period multiplied by 1, 2, 4, 64 or 1024 as determined by the $4X/\overline{2X}$ and CD1:CD0 bits of the PMR register). The period of t_{ACLK} must be in the range:

$$1.0\ us <= t_{ACLK} <= 6.25us$$

A/D Result Most Significant Byte (ADMSB)

	7	6	5	4	3	2	1	0
SFR B4h	ADMSB.7	ADMSB.6	ADMSB.5	ADMSB.4	ADMSB.3	ADMSB.2	ADMSB.1	ADMSB.0
	R*-0	R*-0	R*-0	R*-0	R*-0	R*-0	R*-0	R*-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset; *=see description

ADMSB7:0
Bit 7-0

A/D Result Most Significant Byte. This register contains either the most significant 8 or 2 bits of the 10-bit A/D conversion result depending on the setting of OUTCF (ADCON2.7). Note that due to the specific implementation of this register, reading back a value written by software will not return identical results. Therefore, writing this register has no practical purpose and should be avoided.

A/D Result Least Significant Byte (ADLSB)

	7	6	5	4	3	2	1	0
SFR B5h	ADLSB.7	ADLSB.6	ADLSB.5	ADLSB.4	ADLSB.3	ADLSB.2	ADLSB.1	ADLSB.0
	R*-0	R*-0	R*-0	R*-0	R*-0	R*-0	R*-0	R*-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset; *=see description

ADLSB7:0
Bit 7-0

A/D Result Least Significant Byte. This register contains the least significant 8 bits of the A/D conversion. Note that due to the specific implementation of this register, reading back a value written by software will not return identical results. Therefore, writing this register has no practical purpose and should be avoided.

A/D Window Comparator High Byte (WINHI)

	7	6	5	4	3	2	1	0
SFR B6h	WINHI.7	WINHI.6	WINHI.5	WINHI.4	WINHI.3	WINHI.2	WINHI.1	WINHI.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

WINHI.7:0
Bit 7-0

A/D Window Comparator High Byte. This register contains the upper limit for the window comparison function. This 8-bit value is compared to the most significant 8-bits of the previous A/D conversion result.

A/D Window Comparator Low Byte (WINLO)

	7	6	5	4	3	2	1	0
SFR B7h	WINLO.7	WINLO.6	WINLO.5	WINLO.4	WINLO.3	WINLO.2	WINLO.1	WINLO.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

WINLO.7:0
Bit 7-0

A/D Window Comparator Low Byte. This register contains the lower limit for the window comparison function. This 8-bit value is compared to the most significant 8-bits of the previous A/D conversion result.

Interrupt Priority (IP)

	7	6	5	4	3	2	1	0
SFR B8h	-	PAD	PS1	PS0	PT1	PX1	PT0	PX0
	-	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

Bit 7 Reserved. Read data is indeterminate.

PAD Bit 6 **A/D Interrupt.** This bit controls the priority of the A/D Converter interrupt.
0 = A/D interrupt priority is determined by the natural priority order.
1 = A/D interrupt is a high priority interrupt.

PS1 Bit 6 **Serial Port 1 Interrupt.** This bit controls the priority of the serial port 1 interrupt.
0 = Serial port 1 priority is determined by the natural priority order.
1 = Serial port 1 is a high priority interrupt.

PS0 Bit 4 **Serial Port 0 Interrupt.** This bit controls the priority of the serial port 0 interrupt.
0 = Serial port 0 priority is determined by the natural priority order.
1 = Serial port 0 is a high priority interrupt.

PT1 Bit 3 **Timer 1 Interrupt.** This bit controls the priority of Timer 1 interrupt.
0 = Timer 1 is determined by the natural priority order.
1 = Timer 1 is a high priority interrupt.

PX1 Bit 2 **External Interrupt 1.** This bit controls the priority of external interrupt 1.
0 = External interrupt 1 is determined by the natural priority order.
1 = External interrupt 1 is a high priority interrupt.

PT0 Bit 1 **Timer 0 Interrupt.** This bit controls the priority of Timer 0 interrupt.
0 = Timer 0 is determined by the natural priority order.
1 = Timer 0 is a high priority interrupt.

PX0 Bit 0 **External Interrupt 0.** This bit controls the priority of external interrupt 0.
0 = External interrupt 0 is determined by the natural priority order.
1 = External interrupt 0 is a high priority interrupt.

Slave Address Mask Enable Register 0 (SADEN0)

	7	6	5	4	3	2	1	0
SFR B9h	SADEN0.7	SADEN0.6	SADEN0.5	SADEN0.4	SADEN0.3	SADEN0.2	SADEN0.1	SADEN0.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

SADEN0.7-0
Bits 7-0

Slave Address Mask Enable Register 0. This register functions as a mask when comparing serial port 0 addresses for automatic address recognition. When a bit in this register is set, the corresponding bit location in the SADDR0 register will be exactly compared with the incoming serial port 0 data to determine if a receiver interrupt should be generated. When a bit in this register is cleared, the corresponding bit in the SADDR0 register becomes a don't care and is not compared against the incoming data. All incoming data will generate a receiver interrupt (if enabled) when this register is cleared.

Slave Address Mask Enable Register 1 (SADEN1)

	7	6	5	4	3	2	1	0
SFR BAh	SADEN1.7	SADEN1.6	SADEN1.5	SADEN1.4	SADEN1.3	SADEN1.2	SADEN1.1	SADEN1.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

SADEN1.7-0
Bits 7-0

Slave Address Mask Enable Register 1. This register functions as a mask when comparing serial port 1 addresses for automatic address recognition. When a bit in this register is set, the corresponding bit location in the SADDR1 register will be exactly compared with the incoming serial port 1 data to determine if a receiver interrupt should be generated. When a bit in this register is cleared, the corresponding bit in the SADDR1 register becomes a don't care and is not compared against the incoming data. All incoming data will generate a receiver interrupt (if enabled) when this register is cleared.

Timer 2 Control (T2CON)

	7	6	5	4	3	2	1	0
SFR BEh	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$\overline{RL2}$
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

TF2
Bit 7

Timer 2 Overflow Flag. This flag will be set when Timer 2 overflows from FFFFh or the count equal to the capture register in down count mode. It must be cleared by software. TF2 will only be set if RCLK and TCLK are both cleared to 0.

EXF2
Bit 6

Timer 2 External Flag. A negative transition on the T2EX pin or timer 2 underflow/overflow will cause this flag to be set based on $\overline{RL2}$, EXEN2, and DCEN (see table below). If set by a negative transition, this flag must be cleared by software. Setting this bit in software or detection of a negative transition on the T2EX pin will force a timer interrupt if enabled.

$\overline{RL2}$	EXEN2	DCEN	RESULT
1	0	X	Negative transitions on T2EX will not affect this bit.
1	1	X	Negative transitions on T2EX will set this bit.
0	0	0	Negative transitions on T2EX will not affect this bit.
0	1	0	Negative transitions on T2EX will set this bit.
0	X	1	Bit toggles whenever timer 2 underflows/overflows and can be used as a 17^{th} bit of resolution. In this mode, EXF2 will not cause an interrupt.

RCLK
Bit 5

Receive Clock Flag. This bit determines the serial port 0 timebase when receiving data in serial modes 1 or 3.
0 = Timer 1 overflow is used to determine receiver baud rate for serial port 0.
1 = Timer 2 overflow is used to determine receiver baud rate for serial port 0. Setting this bit will force timer 2 into baud rate generation mode. The timer will operate from a divide by 2 of the external clock.

TCLK
Bit 4

Transmit Clock Flag. This bit determines the serial port 0 timebase when transmitting data in serial modes 1 or 3.

0 = Timer 1 overflow is used to determine transmitter baud rate for serial port 0.

1 = Timer 2 overflow is used to determine transmitter baud rate for serial port 0. Setting this bit will force timer 2 into baud rate generation mode. The timer will operate from a divide by 2 of the external clock.

EXEN2
Bit 3

Timer 2 External Enable. This bit enables the reload function on the T2EX pin if Timer 2 is not generating baud rates for the serial port.

0 = Timer 2 will ignore all external events at T2EX.

1 = Timer 2 will capture or reload a value if a negative transition is detected on the T2EX pin.

TR2
Bit 2

Timer 2 Run Control. This bit enables/disables the operation of timer 2. Halting this timer will preserve the current count in TH2, TL2.
0 = Timer 2 is halted.
1 = Timer 2 is enabled.

C/$\overline{T2}$
Bit 1

Counter/Timer Select. This bit determines whether timer 2 will function as a timer or counter. Independent of this bit, timer 2 runs at 2 clocks per tick when used in either baud rate generator or clock output mode.
0 = Timer 2 function as a timer. The speed of timer 2 is determined by the T2M bit (CKCON.5).
1 = Timer 2 will count negative transitions on the T2 pin.

$\overline{RL2}$
Bit 0

Reload Enable. This bit determines if the reload function will be used for timer 2. If either RCLK or TCLK is set, this bit will not function and the timer will function in an auto-reload mode following each overflow.
0 = Auto-reloads will occur when timer 2 overflows or a falling edge is detected on T2EX if EXEN2=1.
1 = Timer 2 reload function is disabled.

Timer 2 Mode (T2MOD)

	7	6	5	4	3	2	1	0
SFR BFh	-	-	-	-	-	-	T2OE	DCEN
							RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

Bits 7-2 Reserved. Read data will be indeterminate.

T2OE
Bit 1

Timer 2 Output Enable. This bit enables/disables the clock output function of the T2 pin.
0 = The T2 pin functions as either a standard port pin or as a counter input for timer 2.
1 = Timer 2 will drive the T2 pin with a clock output if C/T2=0. Also, timer 2 rollovers will not cause interrupts in this case.

DCEN
Bit 0

Down Count Enable. This bit, in conjunction with the T2EX pin, controls the direction that timer 2 counts in 16-bit auto-reload mode.

DCEN	T2EX	DIRECTION
1	1	Up
1	0	Down
0	X	Up

Parallel I/O Port Four (P4)

	7	6	5	4	3	2	1	0
SFR C0h	P4.7 CMT1	P4.6 CMT0	P4.5 CMSR5	P4.4 CMSR4	P4.3 CMSR3	P4.2 CMSR2	P4.1 CMSR1	P4.0 CMSR0
	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

P4.7-0
Bits 7-0

General Purpose I/O Port Four. This register functions as a general purpose I/O port. In addition, all the pins have an alternative function listed below. Each of the functions is controlled by several other SFRs. The associated Port 4 latch bit must contain a logic one before the pin can be used in its alternate function capacity.

CMT1
Bit 7

Compare Match Toggle Pin. This pin alternately serves as an output for the Timer 2 compare function. This pin will toggle when a match occurs between Timer 2 and compare registers CMPH2:CMPL2 if the enable bit CMTE1 (RSTR.7) is set.

CMT0
Bit 6

Compare Match Toggle Pin. This pin alternately serves as an output for the Timer 2 compare function. This pin will toggle when a match occurs between Timer 2 and compare registers CMPH2:CMPL2 if the enable bit CMTE0 (RSTR.6) is set.

CMSR5
Bit 5

Compare Match Set/Reset Pin 5. This pin alternately serves as an output for the Timer 2 compare function. It will be set if CMS5 (SETR.5) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH0:CMPL0. It will be reset if CMR5 (RSTR.5) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH1:CMPL1.

CMSR4
Bit 4

Compare Match Set/Reset Pin 4. This pin alternately serves as an output for the Timer 2 compare function. It will be set if CMS4 (SETR.4) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH0:CMPL0. It will be reset if CMR4 (RSTR.4) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH1:CMPL1.

CMSR3
Bit 3

Compare Match Set/Reset Pin 3. This pin alternately serves as an output for the Timer 2 compare function. It will be set if CMS3 (SETR.3) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH0:CMPL0. It will be reset if CMR3 (RSTR.3) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH1:CMPL1.

CMSR2
Bit 2

Compare Match Set/Reset Pin 2. This pin alternately serves as an output for the Timer 2 compare function. It will be set if CMS2 (SETR.2) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH0:CMPL0. It will be reset if CMR2 (RSTR.2) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH1:CMPL1.

CMSR1
Bit 1

Compare Match Set/Reset Pin 1. This pin alternately serves as an output for the Timer 2 compare function. It will be set if CMS1 (SETR.1) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH0:CMPL0. It will be reset if CMR1 (RSTR.1) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH1:CMPL1.

CMSR0
Bit 0

Compare Match Set/Reset Pin 0. This pin alternately serves as an output for the Timer 2 compare function. It will be set if CMS0 (SETR.0) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH0:CMPL0. It will be reset if CMR0 (RSTR.0) is 1 and a match occurs between Timer 2 and 16-bit compare register CMPH1:CMPL1.

ROM Size Select (ROMSIZE)

	7	6	5	4	3	2	1	0
SFR C2h	-	-	-	-	-	RS2	RS1	RS0
						RT-1	RT-0	RT-0

R=Unrestricted Read, W=Unrestricted Write, T=Timed Access Write Only, -n=Value after Reset

Bits 7-3 These bits are reserved. Read data is indeterminate.

ROMSIZE.2-0
Bits 2-0

ROM Size Select 2-0. This register is used to select the maximum on-chip decoded address for ROM. Care must be taken that the memory location of the current program counter will be valid both before and after modification. These bits can only be modified using a timed access procedure. The **$\overline{\text{EA}}$** pin will override the function of these bits when asserted, forcing the device to access external program memory only. Configuring this register to a setting that exceeds the maximum amount of internal memory may corrupt device operation. These bits will default on reset to the maximum amount of internal program memory (i.e., 8K for DS87C550).

RS2	RS1	RS0	MAXIMUM ON-CHIP ROM ADDRESS
0	0	0	0KB/Disable on-chip ROM
0	0	1	1KB/03FFh
0	1	0	2KB/07FFh
0	1	1	4KB/0FFFh
1	0	0	8KB/1FFFh (Default Value on Reset DS87C550)
1	0	1	16KB/3FFFh
1	1	0	132KB/7FFFh
1	1	1	64KB/FFFFh

Parallel I/O Port Five (P5)

	7	6	5	4	3	2	1	0
SFR C4h	P5.7 ADC7	P5.6 ADC6	P5.5 ADC5	P5.4 ADC4	P5.3 ADC3	P5.2 ADC2	P5.1 ADC1	P5.0 ADC0
	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

P5.7-0
Bits 7-0

General Purpose I/O Port Five. This register functions as an open drain 8-bit bi-directional port. In addition, all the pins have an alternative function listed below. Each of the functions is controlled by several other SFRs. The associated Port 5 latch bit must contain a logic one before the pin can be used in its alternate function capacity, otherwise the pin is forced to a strong zero.

ADC7-ADC0
Bits 7-0

A/D Converter Input Pins. These pins provide the inputs to the 8 analog multiplexer channels (7-0) of the A/D converter.

Status Register (STATUS)

	7	6	5	4	3	2	1	0
SFR C5	PIP	HIP	LIP	-	SPTA1	SPRA1	SPTA0	SPRA0
	R-0	R-0	R-0		R-0	R-0	R-0	R-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset, *=See description

PIP
Bit 7

Power Fail Priority Interrupt Status. When set, this bit indicates that software is currently servicing a power-fail interrupt. It is cleared when the program executes the corresponding RETI instruction.

HP
Bit 6

High Priority Interrupt Status. When set, this bit indicates that software is currently servicing a high priority interrupt. It is cleared when the program executes the corresponding RETI instruction.

LIP
Bit 5

Low Priority Interrupt Status. When set, this bit indicates that software is currently servicing a low priority interrupt. It is cleared when the program executes the corresponding RETI instruction.

Bit 4

Reserved.

SPTA1
Bit 3

Serial Port 1 Transmit Activity Monitor. When set, this bit indicates that data is currently being transmitted by serial port 1. It is cleared when the internal hardware sets the TI_1 bit. Do not alter the Clock Divide Control (CD1:0) bits while this bit is set or serial port data may be lost.

SPRA1
Bit 2

Serial Port 1 Receive Activity Monitor. When set, this bit indicates that data is currently being received by serial port 1. It is cleared when the internal hardware sets the RI_1 bit. Do not alter the Clock Divide Control bits (CD1:0) while this bit is set or serial port data may be lost.

SPTA0
Bit 1

Serial Port 0 Transmit Activity Monitor. When set, this bit indicates that data is currently being transmitted by serial port 0. It is cleared when the internal hardware sets the TI_0 bit. Do not alter the Clock Divide Control bits (CD1:0) while this bit is set or serial port data may be lost.

SPRA0
Bit 0

Serial Port 0 Receive Activity Monitor. When set, this bit indicates that data is currently being received by serial port 0. It is cleared when the internal hardware sets the RI_0 bit. Do not alter the Clock Divide Control bits (CD1:0) while this bit is set or serial port data may be lost.

Timed Access Register (TA)

	7	6	5	4	3	2	1	0
SFR C7h	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0
	W-1	W-1	W-1	W-1	W-1	W-1	W-1	W-1

W=Unrestricted Write, -n=Value after Reset

TA.7-0
Bits 7-0

Timed Access Register. Correctly accessing this register permits modification of timed access protected bits. Write AAh to this register first, followed within 3 cycles by writing 55h. Timed access protected bits can then be modified for a period of 3 cycles measured from the writing of the 55h.

External Interrupt Flag Register (T2IR)

	7	6	5	4	3	2	1	0
SFR C8h	-	CM2F	CM1F	CM0F	IE5/CF3	IE4/CF2	IE3/CF2	IE2/CF0
	-	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

Bit 7 — Reserved. Read data is indeterminate.

CM2F
Bit 6 — **Compare Match Interrupt 2 Flag.** This bit will cause an interrupt if enabled by ECM2 (EIE.6) when a match occurs between Timer 2 and the contents of Compare Match 2 registers (CMPH2:CMPL2). Setting this bit with software will cause an interrupt if enabled, and software must always clear this bit.

CM1F
Bit 5 — **Compare Match Interrupt 1 Flag.** This bit will cause an interrupt if enabled by ECM1 (EIE.5) when a match occurs between Timer 2 and the contents of Compare Match 1 registers (CMPH1:CMPL1). Setting this bit with software will cause an interrupt if enabled, and software must always clear this bit.

CM0F
Bit 4 — **Compare Match Interrupt 0 Flag.** This bit will cause an interrupt if enabled by ECM0 = EIE.4) when a match occurs between Timer 2 and the contents of Compare Match 0 registers (CMPH1 & CMPL1). Setting this bit with software will cause an interrupt if enabled, and software must always clear this bit.

IE5/CF3
Bit 3 — **External Interrupt 5 or Capture Interrupt 3 Flag.** This bit serves as an interrupt flag for External Interrupt 5 and alternatively for the capture function (capture register 3) of Timer 2. If either capture trigger bit CT3 or $\overline{CT3}$ (CTCON.6 or 7) is set, then the capture function register 3 is enabled, and this bit will be set when a capture occurs. If neither of these bits are set, this bit serves as a flag for external interrupt 5. Regardless of meaning, this bit will cause an interrupt to occur only if the enable bit EX5/EC3 (EIE.3) is set. Setting this bit with software will cause an interrupt (if enabled), and software must always clear this bit.

IE4/CF2
Bit 2 — **External Interrupt 4 or Capture Interrupt 2 Flag.** This bit serves as an interrupt flag for External Interrupt 4 and alternatively for the capture function (capture register 2) of Timer 2. If either capture trigger bit CT2 or $\overline{CT2}$ (CTCON.4 or 5) is set, then the capture function register 2 is enabled, and this bit will be set when a capture occurs. If neither of these bits are set, this bit serves as a flag for external interrupt 4. Regardless of meaning, this bit will cause an interrupt to occur only if the enable bit EX4/EC2 (EIE.2) is set. Setting this bit with software will cause an interrupt (if enabled), and software must always clear this bit

IE3/CF1
Bit 1

External Interrupt 3 or Capture Interrupt 1 Flag. This bit serves as an interrupt flag for External Interrupt 3 and alternatively for the capture function (capture register 1) of Timer 2. If either capture trigger bit CT1 or $\overline{CT1}$ (CTCON.2 or 3) is set, then the capture function register 1 is enabled, and this bit will be set when a capture occurs. If neither of these bits are set, the this bit serves as a flag for external interrupt 3. Regardless of meaning, this bit will cause an interrupt to occur only if the enable bit EX3/EC1 (EIE.1) is set. Setting this bit with software will cause an interrupt (if enabled), and software must always clear this bit.

IE2/CF0
Bit 0

External Interrupt 2 or Capture Interrupt 0. This bit serves as an interrupt flag for External Interrupt 2 and alternatively for the capture function (capture register 0) of Timer 2. If either capture trigger bit CT0 or CT0\ (CTCON.0 or 2) is set, then the capture function register 0 is enabled, and this bit will be set when a capture occurs. If neither of these bits are set, the this bit serves as a flag for external interrupt 2. Regardless of meaning, this bit will cause an interrupt to occur only if the enable bit EX2/EC0 (EIE.0) is set. Setting this bit with software will cause an interrupt (if enabled), and software must always clear this bit.

Compare Register 0 MSB (CMPH0)

	7	6	5	4	3	2	1	0
SFR C9h	CMPH0.7	CMPH0.6	CMPH0.5	CMPH0.4	CMPH0.3	CMPH0.2	CMPH0.1	CMPH0.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CMPH0.7-0
Bits 7-0

Compare Register 0 MSB. This register is used to store the most significant 8-bit value for one of the three available Timer 2 comparison functions. Register CMPL0 (A9h) contains the least significant byte of this compare function. When a 16-bit match occurs, a Timer 2 interrupt occurs if enabled, and port pins P4.5 through P4.0 are set if the corresponding enable bits are set in the SETR (EEh) register.

Compare Register 1 MSB (CMPH1)

	7	6	5	4	3	2	1	0
SFR CAh	CMPH1.7	CMPH1.6	CMPH1.5	CMPH1.4	CMPH1.3	CMPH1.2	CMPH1.1	CMPH1.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CMPH1.7-0
Bits 7-0

Compare Register 1 MSB. This register is used to store the most significant 8-bit value for one of the three available Timer 2 comparison functions. Register CMPL1 (AAh) contains the least significant byte of this compare function. When a 16-bit match occurs, a Timer 2 interrupt occurs if enabled, and port pins P4.5 through P4.0 are set if the corresponding enable bits are set in the SETR (EEh) register.

Compare Register 2 MSB (CMPH2)

	7	6	5	4	3	2	1	0
SFR CBh	CMPH2.7	CMPH2.6	CMPH2.5	CMPH2.4	CMPH2.3	CMPH2.2	CMPH2.1	CMPH2.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CMPH2.7-0
Bits 7-0

Compare Register 2 MSB. This register is used to store the most significant 8-bit value for one of the three available Timer 2 comparison functions. Register CMPL2 (ABh) contains the least significant byte of this compare function. When a 16-bit match occurs, a Timer 2 interrupt is occurs if enabled and port pins P4.7 or P4.6 are toggled if the corresponding enable bits CMTE1 or CMTE0 are set in the RSTR (EFh) register.

Capture Register 0 MSB (CPTH0)

	7	6	5	4	3	2	1	0
SFR CCh	CPTH0.7	CPTH0.6	CPTH0.5	CPTH0.4	CPTH0.3	CPTH0.2	CPTH0.1	CPTH0.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CPTH0.7-0
Bits 7-0

Capture Register 2 MSB. This register loads the most significant 8-bit value of Timer 2 when a transition occurs on the INT2/CT0 pin if the corresponding capture trigger is enabled by the appropriate bit in register CTCON (EBh). The least significant 8-bit value is loaded into register CPTL0 (ACh).

Capture Register 1 MSB (CPTH1)

	7	6	5	4	3	2	1	0
SFR CDh	CPTH1.7	CPTH1.6	CPTH1.5	CPTH1.4	CPTH1.3	CPTH1.2	CPTH1.1	CPT10.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CPTH1.7-0
Bits 7-0

Capture Register 1 MSB. This register loads the most significant 8-bit value of Timer 2 when a transition occurs on the INT3/CT1 pin if the corresponding capture trigger is enabled by the appropriate bit in register CTCON (EBh). The least significant 8-bit value is loaded into register CPTL1 (ADh).

Capture Register 2 MSB (CPTH2)

	7	6	5	4	3	2	1	0
SFR CEh	CPTH2.7	CPTH2.6	CPTH2.5	CPTH2.4	CPTH2.3	CPTH2.2	CPTH2.1	CPTH2.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CPTH2.7-0
Bits 7-0

Capture Register 2 MSB. This register loads the most significant 8-bit value of Timer 2 when a transition occurs on the INT4/CT2 pin if the corresponding capture trigger is enabled by the appropriate bit in register CTCON (EBh). The least significant 8-bit value is loaded into register CPTL2 (AEh).

Capture Register 3 MSB (CPTH3)

	7	6	5	4	3	2	1	0
SFR CFh	CPTH3.7	CPTH3.6	CPTH3.5	CPTH3.4	CPTH3.3	CPTH3.2	CPTH3.1	CPTH3.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CPTH3.7-0
Bits 7-0

Capture Register 3 MSB. This register loads the most significant 8-bit value of Timer 2 when a transition occurs on the INT5/CT3 pin if the corresponding capture trigger is enabled by the appropriate bit in register CTCON (EBh). The least significant 8-bit value is loaded into register CPTL3 (AEh).

Program Status Word (PSW)

	7	6	5	4	3	2	1	0
SFR D0h	CY	AC	F0	RS1	RS0	0V	F1	PARITY
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CY
Bit 7

Carry Flag. This bit is set when if the last arithmetic operation resulted in a carry (during addition) or a borrow (during subtraction). Otherwise it is cleared to 0 by all arithmetic operations.

AC
Bit 6

Auxiliary Carry Flag. This bit is set to 1 if the last arithmetic operation resulted in a carry into (during addition), or a borrow (during subtraction) from the high order nibble. Otherwise it is cleared to 0 by all arithmetic operations.

F0
Bit 5

User Flag 0. This is a bit-addressable, general purpose flag for software control.

RS1, RS0
Bits 4-3

Register Bank Select 1–0. These bits select which register bank is addressed during register accesses.

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00h – 07h
0	1	1	08h – 0Fh
1	0	2	10h – 17h
1	1	3	18h – 1Fh

OV
Bit 2

Overflow Flag. This bit is set to 1 if the last arithmetic operation resulted in a carry (addition), borrow (subtraction), or overflow (multiply or divide). Otherwise it is cleared to 0 by all arithmetic operations.

F1
Bit 1

User Flag 1. This is a bit-addressable, general purpose flag for software control.

PARITY
Bit 0

Parity Flag. This bit is set to 1 if the modulo-2 sum of the eight bits of the accumulator is 1 (odd parity); and cleared to 0 on even parity.

PWM0 Frequency Generator Register (PW0FG)

	7	6	5	4	3	2	1	0
SFR D2h	PW0FG.7	PW0FG.6	PW0FG.5	PW0FG.4	PW0FG.3	PW0FG.2	PW0FG.1	PW0FG.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PW0FG.7-0
BitS 7-6

PWM0 Clock Generator Register. This register contains the user defined value, N which determines the repetition rate for 8-bit PWM channel 0 or 16-bit PWM channel 0 if PWEO=1. This repetition rate (frequency) is given by the equation: Prescaler-Output-Frequency / (N+1).

PWM1 Frequency Generator Register (PW1FG)

	7	6	5	4	3	2	1	0
SFR D3h	PW1FG.7	PW1FG.6	PW1FG.5	PW1FG.4	PW1FG.3	PW1FG.2	PW1FG.1	PW1FG.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PW1FG.7-0
BitS 7-6

PWM1 Clock Generator Register. This register contains the user defined value, N which determines the repetition rate for 8-bit PWM channel 1. This repetition rate (frequency) is given by the equation: Prescaler-Output-Frequency / (N+1). This register is not used in 16-bit PWM operations.

PWM2 Frequency Generator Register (PW2FG)

	7	6	5	4	3	2	1	0
SFR D4h	PW2FG.7	PW2FG.6	PW2FG.5	PW2FG.4	PW2FG.3	PW2FG.2	PW2FG.1	PW2FG.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PW2FG.7-0
BitS 7-6

PWM2 Clock Generator Register. This register contains the user defined value, N which determines the repetition rate for 8-bit PWM channel 2 or 16-bit PWM channel 1 if PWE1=1. This repetition rate (frequency) is given by the equation: Prescaler-Output-Frequency / (N+1).

PWM3 Frequency Generator Register (PW3FG)

	7	6	5	4	3	2	1	0
SFR D5h	PW3FG.7	PW3FG.6	PW3FG.5	PW3FG.4	PW3FG.3	PW3FG.2	PW3FG.1	PW3FG.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PW3FG.7-0
BitS 7-6

PWM3 Clock Generator Register. This register contains the user defined value, N which determines the repetition rate for 8-bit PWM channel 3. This repetition rate (frequency) is given by the equation: Prescaler-Output-Frequency / (N+1). This register is not used in 16-bit PWM operations.

16-Bit PWM Mode Enable and A/D Reference Select (PWMADR)

	7	6	5	4	3	2	1	0
SFR D6h	ADRS	-	-	-	-	-	PWE1	PWE0
	RW-0	-	-	-	-	-	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

ADRS
Bit 7

A/D Reference Select. When set to 1, this bit selects an external source provided on pins V_{REF}+ and V_{REF}- as the voltage reference for the A/D converter. When cleared to 0, the internal bandgap provides the voltage reference for the A/D.

Bits 6-2

Reserved. Read data will be indeterminate.

PWE1
Bit 1

16-Bit PWM Enable 1. Setting this bit to 1 enables the 16-bit PWM channel 1. Clearing this bit disables 16-bit mode and enables 8-bit mode.

PWE0
Bit 1

16-Bit PWM Enable 0. Setting this bit to 1 enables the 16-bit PWM channel 0. Clearing this bit disables 16-bit mode and enables 8-bit mode.

Serial Port Control (SCON1)

	7	6	5	4	3	2	1	0
SFR D8h	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

SM0-2
Bits 7-5

Serial Port 1 Mode. These bits control the mode of serial port 1 as shown below. In addition, the SM0 and SM2 bits have secondary functions as shown below.

SM0	SM1	SM2	MODE	FUNCTION	LENGTH	PERIOD
0	0	0	0	Synchronous	8 bits	$12t_{CLK}$
0	0	1	0	Synchronous	8 bits	$4t_{CLK}$
0	1	X	1	Asynchronous	10 bits	Timer 1 baud rate equation
1	0	0	2	Asynchronous	11 bits	$64t_{CLK}$ (SMOD=0) $32t_{CLK}$ (SMOD=1)
1	0	1	2	Asynchronous w/ Multiprocessor communication	11 bits	$64t_{CLK}$ (SMOD=0) $32t_{CLK}$ (SMOD=1)
1	1	0	3	Asynchronous	11 bits	Timer 1 baud rate equation
1	1	1	3	Asynchronous w/ Multiprocessor communication	11 bits	Timer 1 baud rate equation

SM0/FE_1
Bit 7

Framing Error Flag. When SMOD0 (PCON.6)=0, this bit (SM0) is used to select the mode for serial port 1. When SMOD0 (PCON.6)=1, this bit (FE) will be set upon detection of an invalid stop bit. When used as FE, this bit must be cleared in software. Once the SMOD0 bit is set, modifications to this bit will not affect the serial port mode settings. Although accessed from the same register, internally the data for bits SM0 and FE are stored in different locations.

SM1_1
Bit 6

No alternate function.

SM2-2
Bit 5

Multiple CPU Communications. The function of this bit is dependent on the serial port 1 mode.

Mode 0: Selects 12 t_{CLK} or $4t_{CLK}$ period for synchronous port 1 data transfers.

Mode 1: When this bit is set, reception is ignored (RI_1 is not set) if invalid stop bit received.

Mode 2/3: When this bit is set, multiprocessor communications are enabled in mode 2 and 3. This will prevent RI_1 from being set, and an interrupt being asserted, if the 9^{th} bit received is not 1.

REN_1
Bit 4

Receive Enable. This bit enables/disables the serial port 1 receiver shift register.

0 = Serial port 1 reception disabled.

1 = Serial port 1 receiver enabled (modes 1, 2, 3). Initiate synchronous reception (mode 0).

TB8_1
Bit 3

9th Transmission Bit State. This bit defines the state of the 9th transmission bit in serial port 1 modes 2 and 3.

RB8_1
Bit 2

9th Received Bit State. This bit identifies the state for the 9th reception bit received data in serial pot 1 modes 2 and 3. In serial port mode 1, when SM2_1=0, RB8_1 is the state of the stop bit. RB8_1 is not used in mode 0.

TI_1
Bit 1

Transmitter Interrupt Flag. This bit indicates that data in the serial port 1 buffer has been completely shifted out. In serial port mode 0, TI_1 is set at the end of the 8th data bit. In all other modes, this bit is set at the end of the last data bit. This bit must be manually cleared by software.

RI_1
Bit 0

Transmitter Interrupt Flag. This bit indicates that a byte of data has been received in the serial port 1 buffer. In serial port mode 1, RI_1 is set at the end of the 8th bit. In serial port mode 1, RI_1 is set after the last sample of the incoming stop bit subject to the state of SM2_1. In modes 2 and 3, RI_1 is set after the last sample of RB8_1. This bit must be manually cleared by software.

Serial Data Buffer 1 (SBUF1)

	7	6	5	4	3	2	1	0
SFR D9h	SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

SBUF1.7-0
Bits 7-0

Serial Data Buffer 1. Data for serial port 1 is read from or written to this location. The serial transmit and receive buffers are separate registers, but both are addressed at this location.

PWM0 Value Register (PWM0)

	7	6	5	4	3	2	1	0
SFR DCh	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PWM0.7-0
Bits 7-0

PWM0 Value Register. This register provides read/write access to timer and compare resources found in the pulse generator section of 8-bit PWM channel 0. When bit PW0T/C (PW01CON.4) is 1, this register provides access to the timer portion. Access to the timer allows precise initialization of the PWM function if desired. When bit PW0T/C is 0, this register provides access to the compare register that determines the duty cycle of channel 0's output. The duty cycle is given by the equation Duty-Cycle (%) = PWM0/256. In 16-bit mode, this register is the LSB value register for 16-bit PWM channel 0, and functions identically to 8-bit mode.

PWM1 Value Register (PWM1)

	7	6	5	4	3	2	1	0
SFR DDh	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PWM1.7-0
Bits 7-0

PWM1 Value Register. This register provides read/write access to timer and compare resources found in the pulse generator section of 8-bit PWM channel 1. When bit PW1T/C (PW01CON.0) is 1, this register provides access to the timer portion. Access to the timer allows precise initialization of the PWM function if desired. When bit PW1T/C is 0, this register provides access to the compare register that determines the duty cycle of channel 1's output. The duty cycle is given by the equation Duty-Cycle (%) = PWM0/256. In 16-bit mode, this register is the MSB value register for 16-bit PWM channel 0, and functions identically to 8-bit mode.

PWM2 Value Register (PWM2)

	7	6	5	4	3	2	1	0
SFR DDh	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PWM2.7-0
Bits 7-0

PWM2 Value Register. This register provides read/write access to timer and compare resources found in the pulse generator section of 8-bit PWM channel 2. When bit PW2T/C (PW23CON.4) is 1, this register provides access to the timer portion. Access to the timer allows precise initialization of the PWM function if desired. When bit PW2T/C is 0, this register provides access to the compare register that determines the duty cycle of channel 2's output. The duty cycle is given by the equation Duty-Cycle (%) = PWM0/256. In 16-bit mode, this register is the LSB value register for 16-bit PWM channel 1, and functions identically to 8-bit mode.

PWM3 Value Register (PWM3)

	7	6	5	4	3	2	1	0
SFR DEh	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PWM3.7-0
Bits 7-0

PWM3 Value Register. This register provides read/write access to timer and compare resources found in the pulse generator section of 8-bit PWM channel 3. When bit PW3T/C (PW23CON.0) is 1, this register provides access to the timer portion. Access to the timer allows precise initialization of the PWM function if desired. When bit PW3T/C is 0, this register provides access to the compare register that determines the duty cycle of channel 3's output. The duty cycle is given by the equation Duty-Cycle (%) = PWM0/256. In 16-bit mode, this register is the MSB value register for 16-bit PWM channel 1, and functions identically to 8-bit mode.

Accumulator A (A or ACC)

	7	6	5	4	3	2	1	0
SFR E0h	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

ACC.7-0
Bits 7-6

Accumulator. This register serves as the accumulator for arithmetic and logical operations. It is functionally identical to the accumulator found in the 80C32.

PWM0 and PWM1 Clock Select Register (PW01CS)

	7	6	5	4	3	2	1	0
SFR E1h	PW0S2	PW0S1	PW0S0	PW0EN	PW1S2	PW1S1	PW1S0	PW1EN
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PW0S2:PW0S0
Bits 7-5

PWM0 Clock Select Bits. These bits determine which of the available prescaler outputs are selected as the PWM0 clock generator inputs as shown below.

PW0S2	PW0S1	PW0S0	Selected Prescaler Output Frequency
0	0	0	Crystal (Oscillator) / 1
0	0	1	Crystal (Oscillator) / 4
0	1	0	Crystal (Oscillator) / 16
0	1	1	Crystal (Oscillator) / 64
1	x	x	PWMC0 (input pin)

PW0EN
Bits 4

PWM0 Clock Generator Enable. This bit enables (1) or disables (0) the clock generator for 8-bit PWM channel 0 or 16-bit PWM channel 0 (when PWE0 = 1).

PW1S2:PW1S0
Bits 3-1.

PWM1 Clock Select Bits. These bits determine which of the available prescaler outputs are selected as the PWM1 clock generator inputs as shown below.

PW1S2	PW1S1	PW1S0	Selected Prescaler Output Frequency
0	0	0	Crystal (Oscillator) / 1
0	0	1	Crystal (Oscillator) / 4
0	1	0	Crystal (Oscillator) / 16
0	1	1	Crystal (Oscillator) / 64
1	x	x	PWMC1 (input pin)

PW1EN
Bit 0

PWM1 Clock Generator Enable. This bit enables (1) or disables (0) the clock generator for 8-bit PWM channel 1. This bit has no effect in 16-bit mode.

PWM2 and PWM3 Clock Select Register (PW23CS)

	7	6	5	4	3	2	1	0
SFR E2h	PW2S2	PW2S1	PW2S0	PW2EN	PW3S2	PW3S1	PW3S0	PW3EN
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PW2S2:PW2S0
Bits 7-5

PWM2 Clock Select Bits. These bits determine which of the available prescaler outputs are selected as the PWM2 clock generator inputs. These bits operate as indicated in the above description of PW01CS.

PW2EN
Bit 4

PWM2 Clock Generator Enable. This bit enables (1) or disables (0) the clock generator for 8-bit PWM channel 2 or 16-bit PWM channel 1 (when PWE0 = 1).

PW3S2:PW3S0
Bits 3-1

PWM3 Clock Select Bits. These bits determine which of the available prescaler outputs are selected as the PWM2 clock generator inputs. These bits operate as indicated in the above description of PW01CS.

PW3EN
Bit 0

PWM3 Clock Generator Enable. This bit enables (1) or disables (0) the clock generator for 8-bit PWM channel 3. This bit has no effect in 16-bit mode.

PWM0 and PWM1 Control Register (PW01CON)

	7	6	5	4	3	2	1	0
SFR E3h	PW0F	PW0DC	PW0OE	PW0T/C	PW1F	PW1DC	PW1OE	PW1T/C
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PW0F
Bit 7

PWM0 Flag. A 1 in this bit indicates that the 8-bit (or 16-bit, if PWE0=1) PWM channel 0 timer has rolled over to zero after the maximum count. This bit must be cleared by software.

PW0DC
Bit 6

PWM0 DC Overdrive. Setting this bit to a 1 forces the 8-bit (or 16-bit, if PWE0=1) PWM channel 0 to output a 1 regardless of the PWM match value.

PW0OE
Bit 5

PWM0 Output Enable. This bit enables (1) or disables (0) the output associated with 8-bit (or 16-bit, if PWE0=1) PWM channel 0. If the PWM output is disabled (reset default condition), its output pin (PWMO0 = P6.0) is available as a standard I/O pin.

PW0T/C Bit 4	**PWM0 Timer/Compare Value Select.** When this bit is cleared (reset default condition), a read or write to register PWM0 accesses the compare register portion of the PWM0 Pulse Generator. When this bit is set, a read or write to register PWM0 access the timer portion of the PWM0 Pulse Generator.
PW1F Bit 3	**PWM1 Flag.** A 1 in this bit indicates that the 8-bit PWM channel 1 timer has rolled over to zero after the maximum count. This bit must be cleared by software, and has no meaning in 16-bit mode.
PW1DC Bit 2	**PWM1 DC Overdrive.** Setting this bit to a 1 forces the 8-bit PWM channel 1 to output a 1 regardless of the PWM match value. This bit has no meaning in 16-bit mode.
PW1OE Bit 1	**PWM1 Output Enable.** This bit enables (1) or disables (0) the output associated with 8-bit PWM channel 1. If the PWM output is disabled (reset default condition), its output pin (PWMO1 = P6.1) is available as a standard I/O pin.
PW1T/C Bit 0	**PWM1 Timer/Capture Value Select.** When this bit is cleared (reset default condition), a read or write to register PWM1 accesses the compare register portion of the PWM1 Pulse Generator. When this bit is set, a read or write to register PWM1 access the timer portion of the PWM1 Pulse Generator.

PWM2 and PWM3 Control Register (PW23CON)

	7	6	5	4	3	2	1	0
SFR E4h	PW2F	PW2DC	PW2OE	PW2T/C	PW3F	PW3DC	PW3OE	PW3T/C
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PW2F
Bit 7

PWM2 Flag. A 1 in this bit indicates that the 8-bit PWM channel 2 (or 16-bit PWM channel 1, if PWE1=1) timer has rolled over to zero after the maximum count. This bit must be cleared by software.

PW2DC
Bit 6

PWM2 DC Overdrive. Setting this bit to a 1 forces the 8-bit PWM channel 2 (or 16-bit PWM channel 1, if PWE0=1) to output a 1 regardless of the PWM match value.

PW2OE
Bit 5

PWM2 Output Enable. This bit enables (1) or disables (0) the output associated with 8-bit PWM channel 2 (or 16-bit PWM channel 1, if PWE0=1). If the PWM output is disabled (reset default condition), its output pin (PWMO2 = P6.2) is available as a standard I/O pin.

PW2T/C
Bit 4

PWM2 Timer/Compare Value Select. When this bit is cleared (reset default condition), a read or write to register PWM2 accesses the compare register portion of the PWM2 Pulse Generator. When this bit is set, a read or write to register PWM2 access the timer portion of the PWM2 Pulse Generator.

PW3F
Bit 3

PWM3 Flag. A 1 in this bit indicates that the 8-bit PWM channel 3 timer has rolled over to zero after the maximum count. This bit must be cleared by software, and has no meaning in 16-bit mode.

PW3DC
Bit 2

PWM3 DC Overdrive. Setting this bit to a 1 forces the 8-bit PWM channel 3 to output a 1 regardless of the PWM match value. This bit has no meaning in 16-bit mode.

PW3OE
Bit 1

PWM3 Output Enable. This bit enables (1) or disables (0) the output associated with 8-bit PWM channel 3. If the PWM output is disabled (reset default condition), its output pin (PWMO3 = P6.3) is available as a standard I/O pin.

PW3T/C
Bit 0

PWM3 Timer/Capture Value Select. When this bit is cleared (reset default condition), a read or write to register PWM3 accesses the compare register portion of the PWM3 Pulse Generator. When this bit is set, a read or write to register PWM3 access the timer portion of the PWM3 Pulse Generator.

Timer 2 Auto Reload Register LSB (RLOADL)

	7	6	5	4	3	2	1	0
SFR E6h	RLOADL.7	RLOADL.6	RLOADL.5	RLOADL.4	RLOADL.3	RLOADL.2	RLOADL.1	RLOADL.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

RLOADL.7-0 **Timer 2 Auto Reload Register LSB.** This register holds the LSB of the 16-bit reload value when Timer 2 is configured in auto-reload mode ($CP/\overline{RL2} = 0$).
Bits 7-0

Timer 2 Auto Reload Register MSB (RLOADH)

	7	6	5	4	3	2	1	0
SFR E7h	RLOADH.7	RLOADH.6	RLOADH.5	RLOADH.4	RLOADH.3	RLOADH.2	RLOADH.1	RLOADH.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

RLOADH.7-0 **Timer 2 Auto Reload Register MSB.** This register holds the MSB of the 16-bit reload value when Timer 2 is configured in auto-reload mode ($CP/\overline{RL2} = 0$).
Bits 7-0

Extended Interrupt Enable (EIE)

	7	6	5	4	3	2	1	0
SFR E8h	ET2	ECM2	ECM1	ECM0	EX5/EC3	EX4/EC2	EX3/EC1	EX2/EC0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

ET2
Bit 7
Enable Timer 2 Interrupt. Setting this bit enables interrupts from the Timer 2 TF2 flag (T2CON.7) and/or T2FB flag (T2SEL.4). Clearing this bit disables this interrupt.

ECM2
Bit 6
Compare Match 2 Interrupt Enable. Setting this bit enables interrupts when Timer 2 and compare register CM2 match. Clearing this bit disables this interrupt.

ECM1
Bit 5
Compare Match 1 Interrupt Enable. Setting this bit enables interrupts when Timer 2 and compare register CM1 match. Clearing this bit disables this interrupt.

ECM0
Bit 4
Compare Match 0 Interrupt Enable. Setting this bit enables interrupts when Timer 2 and compare register CM0 match. Clearing this bit disables this interrupt.

EX5/EC3
Bit 3
External Interrupt 5 or Capture 3 Interrupt Enable. This bit enables (1) or disables (0) interrupts initiated by the proper transition on the INT5/CT3 pin (P1.3). If the capture function associated with this pin is enabled (CT3 CTCON.6 or $\overline{CT3}$ CTCON.7 bit set), a capture will occur also.

EX4/EC2
Bit 2
External Interrupt 4 or Capture 2 Interrupt Enable. This bit enables (1) or disables (0) interrupts initiated by the proper transition on the INT4/CT2 pin (P1.2). If the capture function associated with this pin is enabled (CT2 = CTCON.4 or $\overline{CT2}$ = CTCON.5 bit set), a capture will occur also.

EX3/EC1
Bit 1
External Interrupt 3 or Capture 1 Interrupt Enable. This bit enables (1) or disables (0) interrupts initiated by the proper transition on the INT3/CT1 pin (P1.1). If the capture function associated with this pin is enabled (CT1 = CTCON.2 or $\overline{CT1}$ = CTCON.3 bit set), a capture will occur also.

EX2/EC2
Bit 2
External Interrupt 2 or Capture 0 Interrupt Enable. This bit enables (1) or disables (0) interrupts initiated by the proper transition on the INT2/CT0 pin (P1.2). If the capture function associated with this pin is enabled (CT0 = CTCON.0 or $\overline{CT1}$ = CTCON.1 bit set), a capture will occur also.

Timer 2 Interrupt/Clock Select (T2SEL)

	7	6	5	4	3	2	1	0
SFR EAh	TF2S	TF2BS	-	TF2B	-	-	T2P1	T2P0
	RW-0	RW-0	-	RW-0	-	-	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

TF2S
Bit 7

Timer 2 16-Bit Overflow Interrupt Select. Setting this bit enables interrupts resulting from a Timer 2 16-bit overflow (sets TF2 flag T2CON.7). Clearing this bit disables this interrupt.

TF2BS
Bit 6

Timer 2 8-Bit Overflow Interrupt Select. Setting this bit enables interrupts resulting from a Timer 2 8-bit overflow (sets TF2B flag T2SEL.4). Clearing this bit disables this interrupt.

Bit 5

Reserved. Read data will be indeterminate.

TF2B
Bit 4

Timer 2 8-Bit Overflow Flag. This bit is set by hardware when the Timer 2 LSB overflows. This bit must be cleared by software , and will only be set if RCLK and TCLK are both cleared (T2 now used as a baud rate generator).

Bits 3-2

Reserved. Read data will be indeterminate.

T2P1-T2P0
Bits 1-0

Timer 2 Prescaler Bits. These bits select the prescaler divide values for the Timer 2 input clock as shown:

T2P1	T2P0	Prescaler Divisor
0	0	1
0	1	2
1	0	4
1	1	8

In all but the clock output mode of Timer 2, the clock control bits 4X/2X and CD1:0 determine the input to this prescaler (see further information in Timer 2 section).

Capture Trigger Control Register (CTCON)

	7	6	5	4	3	2	1	0
SFR EBh	$\overline{CT3}$	CT3	$\overline{CT2}$	CT2	$\overline{CT1}$	CT1	$\overline{CT0}$	CT0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

$\overline{CT3}$
Bit 7

Capture Register CPTR3 Negative Trigger Enable. Setting this bit enables the transfer of Timer 2 contents into 16-bit capture register pair CPTH3:CPTL3 on the falling edge of the signal on pin INT5/CT3 (P1.3). When set, this bit also configures External Interrupt 5 to respond to a negative edge (if enabled). Clearing this bit disables both capture and interrupt functions for a falling edge.

CT3
Bit 6

Capture Register CPTR3 Positive Trigger Enable. Setting this bit enables the transfer of Timer 2 contents into 16-bit capture register pair CPTH3:CPTL3 on the rising edge of the signal on pin INT5/CT3 (P1.3). When set, this bit also configures External Interrupt 5 to respond to a positive edge (if enabled). Clearing this bit disables both capture and interrupt functions for a rising edge.

$\overline{CT2}$
Bit 5

Capture Register CPTR2 Negative Trigger Enable. Setting this bit enables the transfer of Timer 2 contents into 16-bit capture register pair CPTH2:CPTL2 on the falling edge of the signal on pin INT4/CT2 (P1.2). When set, this bit also configures External Interrupt 4 to respond to a negative edge (if enabled). Clearing this bit disables both capture and interrupt functions for a falling edge.

CT2
Bit 4

Capture Register CPTR2 Positive Trigger Enable. Setting this bit enables the transfer of Timer 2 contents into 16-bit capture register pair CPTH2:CPTL2 on the rising edge of the signal on pin INT4/CT2 (P1.2). When set, this bit also configures External Interrupt 4 to respond to a negative edge (if enabled). Clearing this bit disables both capture and interrupt functions for a rising edge.

$\overline{CT1}$
Bit 3

Capture Register CPTR1 Negative Trigger Enable. Setting this bit enables the transfer of Timer 2 contents into 16-bit capture register pair CPTH1:CPTL1 on the falling edge of the signal on pin INT3/CT1 (P1.1). When set, this bit also configures External Interrupt 3 to respond to a negative edge (if enabled). Clearing this bit disables both capture and interrupt functions for a falling edge.

CT1
Bit 2

Capture Register CPTR1 Positive Trigger Enable. Setting this bit enables the transfer of Timer 2 contents into 16-bit capture register pair CPTH1:CPTL1 on the falling edge of the signal on pin INT3/CT1 (P1.1). When set, this bit also configures External Interrupt 3 to respond to a positive edge (if enabled). Clearing this bit disables both capture and interrupt functions for a rising edge.

$\overline{\text{CT0}}$
Bit 1

Capture Register CPTR0 Negative Trigger Enable. Setting this bit enables the transfer of Timer 2 contents into 16-bit capture register pair CPTH0:CPTL0 on the falling edge of the signal on pin INT2/CT0 (P1.0). When set, this bit also configures External Interrupt 2 to respond to a negative edge (if enabled). Clearing this bit disables both capture and interrupt functions for a falling edge.

CT0
Bit 0

Capture Register CPTR0 Positive Trigger Enable. Setting this bit enables the transfer of Timer 2 contents into 16-bit capture register pair CPTH0:CPTL0 on the rising edge of the signal on pin INT2/CT0 (P1.0). When set, this bit also configures External Interrupt 2 to respond to a positive edge (if enabled). Clearing this bit disables both capture and interrupt functions for a falling edge.

Timer 2 LSB (T2L)

	7	6	5	4	3	2	1	0
SFR ECh	T2L.7	T2L.6	T2L.5	T2L.4	T2L.3	T2L.2	T2L.1	T2L.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

T2L.7-0
Bits 7-0

Timer 2 LSB. This register contains the least significant byte of timer2.

Timer 2 MSB (T2H)

	7	6	5	4	3	2	1	0
SFR ECh	T2H.7	T2H.6	T2H.5	T2H.4	T2H.3	T2H.2	T2H.1	T2H.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

T2H.7-0
Bits 7-0

Timer 2 MSB. This register contains the most significant byte of timer2.

Compare Match Set Enable Register (SETR)

	7	6	5	4	3	2	1	0
SFR EEh	TGFF1	TGFF0	CMS5	CMS4	CMS3	CMS2	CMS1	CMS0
	R-1	R-1	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

TGFF1
Bit 7

Compare Match Toggle Flip-Flop 1. This bit is used as a toggle flip-flop for Port pin CMT1 (P4.7). This bit toggles when the contents of Timer 2 and the 16-bit register pair CMPH2:CMPL2 match and the toggle function is enabled (CMTE1=1).

TGFF0
Bit 6

Compare / Match Toggle Flip-Flop 0. This bit is used as a toggle flip-flop for Port pin CMT0 (P4.6). This bit toggles when the contents of Timer 2 and the 16-bit register pair CMPH2:CMPL2 match and the toggle function is enabled (CMTE0=1).

CMS5
Bit 5

Compare Match Set Enable 5. Setting this bit enables the set function on port pin CMSR5 (P4.5) when the contents of Timer 2 and 16-bit register pair CMPH0:CMPL0 match. Clearing this bit disables this function.

CMS4
Bit 4

Compare Match Set Enable 4. Setting this bit enables the set function on port pin CMSR4 (P4.4) when the contents of Timer 2 and the 16-bit register pair CMPH0:CMPL0 match. Clearing this bit disables the set function.

CMS3
Bit 3

Compare Match Set Enable 3. Setting this bit enables the set function on port pin CMSR3 (P4.3) when the contents of Timer 2 and the 16-bit register pair CMPH0:CMPL0 match. Clearing this bit disables the set function.

CMS2
Bit 2

Compare Match Set Enable 2. Setting this bit enables the set function on port pin CMSR2 (P4.2) when the contents of Timer 2 and the 16-bit register pair CMPH0:CMPL0 match. Clearing this bit disables the set function.

CMS1
Bit 1

Compare Match Set Enable 1. Setting this bit enables the set function on port pin CMSR1 (P4.1) when the contents of Timer 2 and the 16-bit register pair CMPH0:CMPL0 match. Clearing this bit disables the set function.

CMS0
Bit 4

Compare Match Set Enable 0. Setting this bit enables the set function on port pin CMSR0 (P4.0) when the contents of Timer 2 and the 16-bit register pair CMPH0:CMPL0 match. Clearing this bit disables the set function.

Compare Match Reset/Toggle Enable Register (RSTR)

	7	6	5	4	3	2	1	0
SFR EFh	CMTE1	CMTE0	CMR5	CMR4	CMR3	CMR2	CMR1	CMR0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

CMTE1
Bit 7

Compare Match Toggle Enable 1. Setting this bit enables the toggle function on port pin CMT1 (P4.7) when the contents of Timer 2 and the 16-bit register pair CMPH2:CMPL2 match. Clearing this bit disables the toggle function.

CMTE0
Bit 6

Compare Match Toggle Enable 0. Setting this bit enables the toggle function on port pin CMT0 (P4.6) when the contents of Timer 2 and the 16-bit register pair CMPH2:CMPL2 match. Clearing this bit disables the toggle function.

CMR5
Bit 5

Compare Match Reset Enable 5. Setting this bit enables the reset function on port pin CMSR5 (P4.5) when the contents of Timer 2 and the 16-bit register pair CMPH1:CMPL1 match. Clearing this bit disables the reset function.

CMR4
Bit 4

Compare Match Reset Enable 4. Setting this bit enables the reset function on port pin CMSR4 (P4.4) when the contents of Timer 2 and the 16-bit register pair CMPH1:CMPL1 match. Clearing this bit disables the reset function.

CMR3
Bit 3

Compare Match Reset Enable 3. Setting this bit enables the reset function on port pin CMSR3 (P4.3) when the contents of Timer 2 and the 16-bit register pair CMPH1:CMPL1 match. Clearing this bit disables the reset function.

CMR2
Bit 2

Compare Match Reset Enable 2. Setting this bit enables the reset function on port pin CMSR2 (P4.2) when the contents of Timer 2 and the 16-bit register pair CMPH1:CMPL1 match. Clearing this bit disables the reset function.

CMR1
Bit 1

Compare Match Reset Enable 1. Setting this bit enables the reset function on port pin CMSR1 (P4.1) when the contents of Timer 2 and the 16-bit register pair CMPH1:CMPL1 match. Clearing this bit disables the reset function.

CMR0
Bit 0

Compare Match Reset Enable 0. Setting this bit enables the reset function on port pin CMSR0 (P4.0) when the contents of Timer 2 and the 16-bit register pair CMPH1:CMPL1 match. Clearing this bit disables the reset function.

B Register

	7	6	5	4	3	2	1	0
SFR F0h	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

B.7-0
Bits 7-0

B Register. This register serves as a second accumulator for certain arithmetic operations.

Parallel I/O Port Six (P6)

	7	6	5	4	3	2	1	0
SFR F1h	P6.7 STADC	-	P6.5 PWMC1	P6.4 PWMC0	P6.3 PWMO3	P6.2 PWMO2	P6.1 PWMO1	P6.0 PWMO0
	RW-1	-	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

P6.7,P6.5-0
Bits 7, 5-0

General Purpose I/O Port 6. This register functions as a 7-bit general purpose I/O port. In addition, all the pins have an alternate function listed below. The associated Port 6 latch bit must contain a logic one before the pin can be used in its alternate function capacity.

STADC
Bit 7

Start A/D Conversion. If enabled by ADEX=ADCON1.4=1, a negative transition on this pin will initiate an A/D conversion. Otherwise this pin serves as a standard I/O pin.

Bit 6

Reserved. Read data will be indeterminate.

PWMC1
Bit 5

PWM Clock 1 Input. If enabled by PW2S2 = PW23CS.7 = 1, this pin will provide an externally generated clock signal to PWM channel 2. If enabled by PW3S2 = PW23CS.3 = 1, this pin will provide an externally generated clock signal to PWM channel 3. Otherwise this pin serves as a standard I/O pin.

PWMC0
Bit 4

PWM Clock 0 Input. If enabled by PW0S2 = PW01CS.7 = 1, this pin will provide an externally generated clock signal to PWM channel 0. If enabled by PW1S2 = PW01CS.3 = 1, this pin will provide an externally generated clock signal to PWM channel 1. Otherwise this pin serves as a standard I/O pin.

PWMO3
Bit 3

PWM Channel 3 Output. If enabled by PW3OE = PW23CON.1 = 1, this pin serves as the output for PWM channel 3. Otherwise this pin serves as a standard I/O pin.

PWMO2
Bit 2

PWM Channel 2 Output. If enabled by PW2OE = PW23CON.5 = 1, this pin serves as the output for PWM channel 2. Otherwise this pin serves as a standard I/O pin.

PWMO1
Bit 1

PWM Channel 1 Output. If enabled by PW1OE = PW01CON.1 = 1, this pin serves as the output for PWM channel 1. Otherwise this pin serves as a standard I/O pin.

PWMO0
Bit 0

PWM Channel 0 Output. If enabled by PW0OE = PW01CON.5 = 1, this pin serves as the output for PWM channel 0. Otherwise this pin serves as a standard I/O pin.

Extended Interrupt Priority (EIP)

	7	6	5	4	3	2	1	0
SFR F8h	PT2	PCM2	PCM1	PCM0	PX5/PC3	PX4/PC2	PX3/PC1	PX2/PC0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R=Unrestricted Read, W=Unrestricted Write, -n=Value after Reset

PT2
Bit 7

Timer 2 Overflow Interrupt Priority. The Timer 2 overflow interrupt request will be high when this bit is 1 and normal priority when it is 0.

PCM2
Bit 6

Compare Match 2 Interrupt Priority. The compare match 2 interrupt request will be high priority when this bit is 1 and normal priority when it is 0.

PCM1
Bit 5

Compare Match 1 Interrupt Priority The compare match 1 interrupt request will be high priority when this bit is 1 and normal priority when it is 0.

PCM0
Bit 4

Compare Match 0 Interrupt Priority The compare match 0 interrupt request will be high priority when this bit is 1 and normal priority when it is 0.

PX5/PC3
Bit 3

External Interrupt 5 Priority or Capture 3 Interrupt Priority. This bit determines the priority (0 = normal, 1= high) of the Timer 2 Capture channel 3 if it is in use or External Interrupt 3 if enabled and the capture function is disabled.

PX4/PC2
Bit 2

External Interrupt 4 Priority or Capture 2 Interrupt Priority. This bit determines the priority (0 = normal, 1= high) of the Timer 2 Capture channel 2 if it is in use or External Interrupt 3 if enabled and the capture function is disabled.

PX3/PC1
Bit 1

External Interrupt 3 Priority or Capture 1 Interrupt Priority. This bit determines the priority (0 = normal, 1= high) of the Timer 2 Capture channel 1 if it is in use or External Interrupt 3 if enabled and the capture function is disabled.

PX2/PC0
Bit 0

External Interrupt 2 Priority or Capture 0 Interrupt Priority. This bit determines the priority (0 = normal, 1= high) of the Timer 2 Capture channel 0 if it is in use or External Interrupt 2 if enabled and the capture function is disabled.

Watchdog Control Register (WDCON)

	7	6	5	4	3	2	1	0
SFR FFh	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
	RW-0	RW-*	RW-0	RW-*	RT-0	RW-*	RT-*	RT-0

R=Unrestricted Read, W=Unrestricted Write, T=Timed Access Write Only,
-n=Value after Reset, *=See description

SMOD_1
Bit 7

Serial Port 0 Baud Rate Doubler Enable. This bit enables/disables the serial baud rate doubling function for Serial Port 1 when using Timer 1 as the baud rate generator.

0 = Serial Port 1 baud rate will be that defined by baud rate generation equation.

1 = Serial Port 1 baud rate will be double that defined by baud rate generation equation.

POR
Bit 6

Power-on Reset Flag. This bit indicates whether the last reset was a power-on reset. This bit is typically interrogated following a reset to determine if the reset was caused by power-on. It must be cleared by a Timed Access write before the next reset of any kind or the software may erroneously determine that another power-on reset has occurred. This bit is set following a power-on reset and unaffected by all other resets.

0 = Last reset was from a source other than a power-on reset

1 = Last reset was a power-on reset.

EPF1
Bit 5

Enable Power Fail Interrupt. This bit enables/disables the ability of the internal band-gap reference to generate a power-fail interrupt when V_{CC} falls below approximately 4.5 volts. While in Stop mode, both this bit and the Band-gap Select bit, BGS (EXIF.0), must be set to enable the power-fail interrupt.

0 = Power-fail interrupt disabled.

1 = Power-fail interrupt enabled during normal operation. Power-fail interrupt enabled in Stop mode if BGS is set.

PF1
Bit 4

Power Fail Interrupt Flag. When set, this bit indicates that a power-fail interrupt has occurred. This bit must be cleared in software before exiting the interrupt service routine, or another interrupt will be generated. Setting this bit in software will generate a power-fail interrupt, if enabled.

WDIF
Bit 3

Watchdog Time-Out Flag. This bit is set by a watchdog time-out which occurs 512 clocks prior to a watchdog reset. This bit can be considered a watchdog interrupt flag even though there is no interrupt associated with the watchdog timer in the DS87C550. This bit must be cleared by software and can only be modified using a Timed Access Procedure.

WTRF
Bit 2

Watchdog Timer Reset Flag. When set, this bit indicates that a watchdog timer reset has occurred. It is typically interrogated to determine if a reset was caused by watchdog timer reset. It is cleared by a power- on reset, but otherwise must be cleared by software before the next reset of any kind or software may erroneously determine that a watchdog timer reset has occurred. Setting this bit in software will not generate a watchdog timer reset. If the EWT bit is cleared, the watchdog timer will have no effect on this bit.

EWT
Bit 1

Enable Watchdog Timer Reset. This bit enables/disables the ability of the watchdog timer to reset the device. Clearing this bit will disable the ability of the watchdog timer to generate a reset, but have no affect on the timer itself. This bit can only be modified using a Timed Access Procedure, and it is unaffected by all other resets.

0 = A timeout of the watchdog timer will not cause the device to reset.

1 = A timeout of the watchdog timer will cause the device to reset.

RWT
Bit 0

Reset Watchdog Timer. Setting this bit will reset the watchdog timer count. This bit must be set using a Timed Access procedure before the watchdog timer expires, or a watchdog timer reset will be generated if enabled. This bit will always be 0 when read.

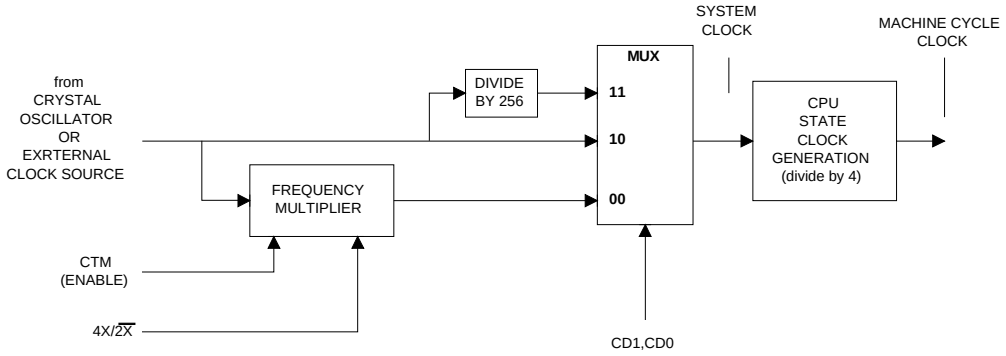
SECTION 5:CPU TIMING

The majority of the information contained in the original "High-Speed Microcontroller User's Guide" applies to the DS87C550. The only differences are found in the clock divider circuits between the crystal oscillator (or external clock source) and the clock distribution circuitry. Early members of the High-Speed Microcontroller family offer the option of 4, 256, or 1024 clocks per machine cycle. The DS87C550 can operate at 1, 2, 4, or 1024 clocks per machine cycle. These selectable clock frequencies not only affect the CPU's frequency of operation (machine cycle clock), but also provide selectable clocks to the on-board timers and other peripherals (system clock). It is important to note the difference in these clocks, as they are sometimes confused, creating errors in timing calculations. The effects of these variable clocks relative to CPU timing are discussed below. Their effect on peripheral timing can be found in the individual peripherals' sections of this document.

Crystal Selection

Some recent introductions to the High-Speed Microcontroller family contain special circuitry to allow more latitude in crystal selection. It is frequently the case that as crystals go up in frequency, they become more expensive, and less likely to be available in fundamental mode. While a fundamental mode, parallel resonant, AT cut crystal is still required for these new family members, a simple clock multiplier has been included to allow selection of more readily available crystals when high frequency operation is required. An illustration of the clock multiplier function specifically and overall system clock generation and control is shown in Figure 5-1.

SYSTEM CLOCK GENERATION AND CONTROL : Figure 5-1



As shown in the figure, the output of the crystal oscillator is provided directly to three blocks of circuitry: the frequency multiplier, a divide by 256 block, and a 3-to-1 multiplexer. The frequency multiplier function is enabled by setting the CTM bit, and produces outputs of Input-times-2 or Input-times-4 as determined by the 4X/$\overline{2X}$ bit. The multiplied clock is then passed to the multiplexer (MUX) that selects the system clock source, and then to the CPU State Clock Generator. This clock multiplication feature allows peak performance of the processor but with the use of a slower, often more available and less expensive crystal. As an example, recall that the maximum frequency of the DS87C550 is 33 MHz. With this clock multiplier feature, a crystal value of 8.25 MHz (33/4) can be used when the frequency multiplier set to Input-times-4 mode. Alternatively with a crystal value of 16.5 MHz, it is possible to recognize peak processor performance when the frequency multiplier is set to input-times 2 mode. Recognize that regardless of the clock multiplication function, there is a maximum operational frequency of the processor given in the specifications as "Oscillator Frequency". Care must be taken not to violate this specification when using the clock multiplier as unpredictable behavior of the processor can result.

The system clock or some derivative there of is provided to all of the peripherals inside the microcontroller and the machine cycle clock provides the basic 4-state clock for all CPU functions. The relationship of the crystal (or external oscillator) to the system clock and machine cycle clock along with the control settings is shown in Table 5-1.

SYSTEM CLOCK CONTROL: Table 5-1.

4X/$\overline{2X}$	**CD1:0**	**System Clock**	**Machine Cycle Clock**
1	00	F_{OSC} * 4	F_{OSC}
0	00	F_{OSC} * 2	F_{OSC} /2
x	01 (Reserved)		
x	10	F_{OSC}	F_{OSC} / 4
x	11	F_{OSC} / 256	F_{OSC} / 1024

The case of CD1:0 = 11 is a special case for power savings, and is described in the section on power management.

Changing System Clock Frequency

The microcontroller incorporates a special locking sequence to ensure "glitch-free" switching of the internal clock signals. All changes to the CD1, CD0 bits must pass through the 10 (divide-by-four) state. For example, to change from 00 (frequency multiplier) to 11 (PMM), the software must change the bits in the following sequence: 00 10 11. Attempts to switch between invalid states will fail, leaving the CD1, CD0 bits unchanged.

The following sequence must be followed when switching to the frequency multiplier as the internal time source. This sequence can only be performed when the device is in divide-by-four operation. The steps must be followed in this order, although it is possible to have other instructions between them. Any deviation from this order will cause the CD1, CD0 bits to remain unchanged. Switching from frequency multiplier to non-multiplier mode requires no steps other than the changing of the CD1, CD0 bits.

1. Ensure that the CD1, CD0 bits are set to 10, and the RGMD (EXIF.2) bit = 0.
2. Clear the CTM (Crystal Multiplier Enable) bit.
3. Set the $4X/\overline{2X}$ bit to the appropriate state.
4. Set the CTM (Crystal Multiplier Enable) bit.
5. Poll the CKRDY bit (EXIF.4), waiting until it is set to 1.
6. Set CD1, CD0 to 00. The frequency multiplier will be engaged on the machine cycle following the write to these bits.

SECTION 6:MEMORY ACCESS

The DS87C550 supports the memory access features of the DS87C520 described in the High-Speed Microcontroller User's Guide. Exceptions are noted below.

INTERNAL PROGRAM MEMORY

The DS87C550 contains 8 kbytes of EPROM as on-board program storage. This memory resides at fixed addresses from 0000h to 1FFFh.

ROMSIZE FEATURE

The ROMSIZE feature is used to select the maximum on-chip decoded address for program memory. The ROMSIZE is selected as follows:

RMS2	RMS1	RMS0	Maximum on-chip Program Address
0	0	0	0K
0	0	1	1K (0h – 03FFh)
0	1	0	2K (0h – 07FFh)
0	1	1	4K (0h – 0FFFh)
1	**0**	**0**	**8K (0h – 1FFFh) default**
1	0	1	Invalid – reserved
1	1	0	Invalid – reserved
1	1	1	Invalid – reserved

DATA MEMORY ACCESS

Two new features related to the dual data pointers found in the High-Speed Microcontroller family have been added to the DS87C550. These are a data pointer decrement capability and the ability to automatically toggle the selection bit between the two data pointers.

Although the 8051 architecture has always had an INC DPTR instruction, users have often wished for the ability to decrement the data pointers as well. To maintain instruction set compatibility, the DS87C550 supports a decrement data pointer feature through unused bits in the DPS register. Setting the ID1:0 (DPS.7-6) bits and the SEL (DPS.0) bit before performing an INC DPTR instruction selects the active data pointer and whether it is to be incremented or decremented. By setting these bits, the user can determine the count direction (increment or decrement) for each data pointer. This allows very efficient movement of data regardless of whether it is more convenient to traverse the data (source or destination) from low to high addresses or high to low addresses. The bits were added, and operate in conjunction with to allow DPTR decrementing as follows:

ID1	ID0	SEL = 0	SEL = 1
0	0	Increment DPTR	Increment DPTR1
0	1	Decrement DPTR	Increment DPTR1
1	0	Increment DPTR	Decrement DPTR1
1	1	Decrement DPTR	Decrement DPTR

The other new feature is the ability to automatically toggle the SEL bit. With this feature enabled, i.e., with TSL bit (DPS.5) set, every time an instruction dealing with the DPTR is executed, the SEL bit is toggled to select the other DPTR. The instructions that affect this automatic toggle function are:

```
INC       DPTR
MOV       DPTR, #data16
MOVC      A, @A+DPTR
MOVX      A, @DPTR
MOVX      @DPTR, A
```

This feature allows further reduction of code for data movement operations, and therefore even higher performance. The following example demonstrates the improved efficiency.

64 BYTE BLOCK MOVE WITH AUTO SELECT

```
; SH and SL are high and low bytes of the source address
; DH and DL are high and low bytes of the destination address
; DPS is the data pointer select bit. Reset condition is DPS = 0 (DPTR selected).
;                                                                    # of cycles
    MOV  R5, #64          ; Number of bytes to move                      3
    MOV  DPTR, #SHSL      ; Load destination address & toggle select bit 2
    MOV  DPTR, #DHDL      ; Load destination address & toggle select bit 2
;
; This loop is executed the number of times contained in R5 (i.e., 64)
    MOVE:
    MOVX A, DPTR          ; Read source data byte & toggle select bit    2
    MOVX @DPTR, A         ; Store at destination & toggle select bit     2
    INC  DPTR             ; Increment source address & toggle select bit 3
    INC  DPTR             ; Increment destination address & toggle select bit 3
    DJNZ R5, MOVE         ; Finished with table                          3
                                                  Total = 7 + (13*64) = 839
```

64 BYTE BLOCK MOVE WITHOUT AUTO SELECT

```
; SH and SL are high and low bytes of the source address
; DH and DL are high and low bytes of the destination address
; DPS is the data pointer select bit. Reset condition is DPS = 0 (DPTR selected).
;                                                                  # of cycles
MOV   R5, #64           ; Number of bytes to move                      3
MOV   DPTR, #SHSL       ; Load source address                          2
INC   DPS               ; Change active DPTR                           2
MOV   DPTR, #DHDL       ; Load destination address                     2
INC   DPS               ; Change active DPTR                           2
;
; This loop is executed the number of times contained in R5 (i.e., 64)
MOVE:
MOVX  A, DPTR           ; Read source data byte                        2
INC   DPS               ; Change active DPTR                           2
MOVX  @DPTR, A          ; Store at destination                         2
INC   DPTR              ; Increment destination address                3
INC   DPS               ; Change active DPTR                           2
INC   DPTR              ; Increment destination address                3
INC   DPS               ; Change active DPTR                           2
```

```
DJNZ   R5, MOVE          ; Finished with table          3
                                                Total = 11+(64*19) = 1,227
```

From this example it is evident that the auto-select feature allows much more efficient block moves. This example demonstrates a block move of 64 bytes of data. Obviously, the larger the block, the more improvement will be realized. It is also worth noting that by appropriately setting the ID1 and ID1 bits, either the source or destination addresses could have been traversed in the reverse direction (decrement DPTR) without any other changes.

DATA MEMORY TIMING

Data memory timing of the DS87C550 is identical to earlier members of the High-Speed Microcontroller family with one exception regarding the implementation of the Stretch MOVX feature. In all members of this family (including the DS87C550), increasing the stretch value from 0 to 1 causes setup and hold times to be increased by 1 crystal clock period each. In older members of the family, there is no further change in setup and hold times regardless of the stretch value selected. In the DS87C550 however, when a stretch value of 4 or above is selected the timing of the interface changes dramatically to allow for very slow peripherals.

For stretch values of 4 or above, the ALE high period is increased one machine cycle that increases the address setup time into the peripheral by this amount. The address is then held on the bus for one additional machine cycle increasing the address hold time by this amount. The Read or Write signal is also increased by one machine cycle. Finally, the data is held on the bus (for a write cycle) one additional machine cycle which increases the available peripheral hold time. For every stretch value greater than 4, the setup and hold times remain constant, and only the width of the read or write signals is increased.

A full description of this new stretch MOVX arrangement is given in the DS87C550 data sheet (MOVX Characteristics) along with timing diagrams and timing tables. Please refer to that document for more detail.

SECTION 7: POWER MANAGEMENT

The DS87C550 supports the general power management features of the DS87C520 described in the High-Speed Microcontroller. Exceptions are noted below.

Power Management Modes

Power management mode 2 (divide by 1024) is supported on the DS87C550. However, power management mode 1 (divide by 256) is not.

Switching between clock sources

The ring oscillator on the DS87C550 is similar to that on the DS80C320. As such it does not support the "run from ring" feature which allows the microprocessor to use the ring oscillator as a clock source after the external crystal has stabilized (CKRY=1).

SECTION 8: RESET CONDITIONS

The reset conditions of the DS87C550 are generally described in the High-Speed Microcontroller User's Guide and specific reset default conditions of the SFR bits may be found in the data sheet. However two features have been added to the DS87C550. These new features are discussed below.

Oscillator Fail Detect Reset

Most members of the High-Speed Microcontroller family contain a watchdog timer. The intent of this timer is to force the processor into a known "good" state (reset) if it ever entered a runaway situation where it was not executing code properly. This is very powerful feature, but could be made stronger with a simple addition. Since the watchdog timer clock was derived from the main crystal oscillator, it was possible (though very unlikely) that the oscillator would fail (stop) leaving the processor in an undesirable state. Since the watchdog timer runs from the same clock, the timer would stop counting which prevented a time-out and a resulting reset. This possibility is eliminated in the DS87C550 by the inclusion of an oscillator fail detection circuit. When enabled, this circuit causes the processor to be reset if the oscillator frequency falls below TBD kHz. This puts the processor into a known good state regardless of the watchdog timer if the main crystal oscillator should ever fail. Although the oscillator has failed when this reset occurs, the processor is clocked into the normal reset state by other internal clocks.

The oscillator fail detect feature is enabled by setting the OFDE (PCON.4) bit with software. This bit can be modified at any time. When an oscillator fail detection occurs, the flag OFDF (PCON.5) bit is set by hardware when the processor enters reset. This bit must be cleared by software.

RST Pin as an Output

The DS87C550 is the first member of Dallas' High-Speed Microcontroller family to make the reset pin (RST) both an input and an output. Normally, this pin is an active high input for a reset signal generated elsewhere in the system. With the DS87C550, this pin functions as an input as before, but now will also provide an output when the reset originates from within the processor.

The possible internal sources of reset from the DS87C550 are:

1. Power–on/Power-Fail reset
2. Watchdog Timer reset
3. Oscillator Fail reset

The reset output pulse duration is a function of the internal source of the reset. The worst case (minimum pulse duration) occurs when the reset source is the watchdog timer whose reset cycle may be a single machine-cycle long. When the watchdog timer creates a reset, the RST pin is set at the beginning of the next machine cycle, and will remain active for one full machine cycle. When the internal source of the reset is the power-fail circuit, the RST pin will be set at the beginning of the next machine cycle after the reset trip point, and will remain as long as power will sustain it. When power returns, the RST pin will be held active while the processor is held in power-up reset (65565 clocks). If the internal source of reset is the oscillator fail detection circuit, the RST pin will be driven active asynchronously immediately after the detection, and will be held there as long as the processor is in a reset state (presumably until the oscillator begins operation again).

Since the RST pin is designed so that it can be overdriven by an LS-TTL gate output, it is important to keep this pin lightly loaded (resistance and capacitance). For best results, a single buffer should be connected to the RST pin when it used as an output for a system-wide reset signal. Under no

circumstances should an R-C timing circuit be connected to the RST pin of the DS87C550. If the RST pin is too heavily loaded (capacitance), it may be necessary to add a pull-up resistor to speed up the low-to-high transition. This will of course determine what type of output device will be capable of overdriving the pin when used as an input. Careful analysis of these tradeoffs will ensure desired results.

SECTION 9: INTERRUPTS

The DS87C550 uses the same interrupt and interrupt priority system as all other members of the High-Speed Microcontroller family. The specific interrupts and their related flags and control bits are identified in Table 9-1 below.

INTERRUPT SUMARY : Table 9-1

Interrupt	Vector	Natural Priority	Flag	Enable	Priority Control
Power Fail	33h	0	PFI (WDCON.4)	EPFI (WDCON.5)	N/A
Ext. Interrupt 0	03h	1	IE0 (TCON.1)**	EX0 (IE.0)	PX0 (IP.0)
Serial Port 1	0Bh	2	RI_1 (SCON1.0) TI_1 (SCON1.1	ES1 (IE.5)	PS1 (IP.5)
A/D	13h	3	EOC (ADCON1.0)	EAD (IE.6)	PAD (IP.6)
Timer 0 Overflow	1Bh	4	TF0 (TCON.5)*	ET0 (IE.1)	PT0 (IP.1)
Ext. Interrupt 2 / Capture 0	23h	5	IE2/CF0 (T2IR.0)	EX2/EC0 (EIE.0)	PX2/PC0 (EIP.0)
Compare Match 0	2Bh	6	CM0F (T2IR.4)	ECM0 (EIE.4)	PCM0 (EIP.4)
Ext. Interrupt 1	3Bh	7	IE1 (TCON.3)**	EX1 (IE.2)	PX1 (IP.2)
Ext. Interrupt 3 / Capture 1	43h	8	IE3/CF1 (T2IR.1)	EX3/EC1 (EIE.1)	PX3/PC1 (EIP.1)
Compare Match 1	4Bh	9	CM1F (T2IR.5)	ECM1 (EIE.5)	PCM1 (EIP.5)
Timer 1 Overflow	53h	10	TF1 (TCON.7)*	ET1 (IE.3)	PT1 (IP.3)
Ext. Interrupt 4 / Capture 2	5Bh	11	IE4/CF2 (T2IR.2)	EX4/EC2 (EIE.2)	PX4/PC2 (EIP.2)
Compare Match 2	63h	12	CM2F (T2IR.6)	ECM2 (EIE.6)	PCM2 (EIP.6)
Serial Port 0	6Bh	13	RI_0 (SCON0.0) TI_0 (SCON0.1)	ES0 (IE.4)	PS0 (IP.4)
Ext. Interrupt 5 / Capture 3	73h	14	IE5/CF3 (T2IR.3)	EX5/EC3 (EIE.3)	PX5/PC3 (EIP.3)
Timer 2 Overflow	7Bh	15	TF2 (T2CON.7) TF2B (T2SEL.4)	ET2 (EIE.7)	PT2 (EIP.7)

Unless marked, these flags must be cleared manually by software.

* - Cleared automatically by hardware when the interrupt service routine is vectored to.

** - If edge triggered, cleared automatically by hardware when the service routine is vectored to. If level triggered, flag follows the state of the pin.

SECTION 10: PARALLEL I/O

The DS87C550 contains 55 parallel I/O pins. Ports 0 through 3 follow the standard 8051 I/O configuration as described in the High-Speed Microcontroller User's Guide. Some secondary functions are assigned to different pins than on other members of the family, but their functionality is the same. Ports 4, 5 and 6 are new, and are described in the DS87C550 data sheet. Ports 4 and 6 operate as quasi bi-directional I/O pins, while port 5 function as an 8-bit open-drain bi-directional I/O port. Port 6 contains only 7 I/O lines. The alternate functions of all port pins are identified below.

P0.0 AD0 Multiplexed address/data bus bit 0
P0.1 AD1 Multiplexed address/data bus bit 1
P0.2 AD2 Multiplexed address/data bus bit 2
P0.3 AD3 Multiplexed address/data bus bit 3
P0.4 AD4 Multiplexed address/data bus bit 4
P0.5 AD5 Multiplexed address/data bus bit 5
P0.6 AD6 Multiplexed address/data bus bit 6
P0.7 AD7 Multiplexed address/data bus bit 7
P1.0 INT2/CT0 External Interrupt 2/Capture Trigger 0
P1.1 INT3/CT1 External Interrupt 3/Capture Trigger 1
P1.2 INT4/CT2 External Interrupt 4/Capture Trigger 2
P1.3 INT5/CT3 External Interrupt 5/Capture Trigger 3
P1.4 T2 External I/O for T2
P1.5 T2EX Timer/Counter 2 Capture/Reload Trigger
P1.6 RXD1 Serial Port1 Input
P1.7 TXD1 Serial Port1 Output
P2.0 A8 MSB Address bus bit 8
P2.1 A9 MSB Address bus bit 9
P2.2 A10 MSB Address bus bit 10
P2.3 A11 MSB Address bus bit 11
P2.4 A12 MSB Address bus bit 12
P2.5 A13 MSB Address bus bit 13
P2.6 A14 MSB Address bus bit 14
P2.7 A15 MSB Address bus bit 15
P3.0 RXD0 Serial Port 0 input
P3.1 TXD0 Serial port 0 Output
P3.2 $\overline{INT0}$ External Interrupt 0
P3.3 $\overline{INT1}$ External Interrupt 1
P3.4 T0 Timer 0 External Input
P3.5 T1 Timer 1 External Input
P3.6 $\overline{WR}$ External Data Memory Write Strobe
P3.7 $\overline{RD}$ External Data Memory Read Strobe
P4.0 CMSR0 Timer 2 compare match set/reset output 0
P4.1 CMSR1 Timer 2 compare match set/reset output 1
P4.2 CMSR2 Timer 2 compare match set/reset output 2
P4.3 CMSR3 Timer 2 compare match set/reset output 3
P4.4 CMSR4 Timer 2 compare match set/reset output 4
P4.5 CMSR5 Timer 2 compare match set/reset output 5
P4.6 CMT0 Timer 2 compare match toggle output 0
P4.7 CMT1 Timer 2 compare match toggle output1
P5.0 ADC0 A/D Converter input channel 0
P5.1 ADC1 A/D Converter input channel 1
P5.2 ADC2 A/D Converter input channel 2
P5.3 ADC3 A/D Converter input channel 3
P5.4 ADC4 A/D Converter input channel 4
P5.5 ADC5 A/D Converter input channel 5
P5.6 ADC6 A/D Converter input channel 6
P5.7 ADC7 A/D Converter input channel 7
P6.0 PWMO0 PWM channel 0 output
P6.1 PWMO1 PWM channel 1 output
P6.2 PWMO2 PWM channel 2 output
P6.3 PWMO3 PWM channel 3 output
P6.4 PWMC0 PWM0 clock input
P6.5 PWMC1 PWM1 clock input
P6.7 STADC Ext. A/D conversion start signal

SECTION 11: PROGRAMMABLE TIMERS

The DS87C550 contains the three timer/counters found on all other Dallas High-Speed Microcontrollers. Timers 0 and 1 have exactly the same functionality as in other members of the family, but have new clock features for the timer functions. Timer 2 also has the same functionality as earlier members of the family, but also has new capture and compare functions not found on earlier members. While earlier members of the family had a capture function associated with timer 2, this capture function is significantly different. Timer 2 also offers new clock features when operated in timer mode. These three timer/counters are described briefly below. Further detail may be found in the original High-Speed Microcontroller User's Guide. The new features will be described in detail below.

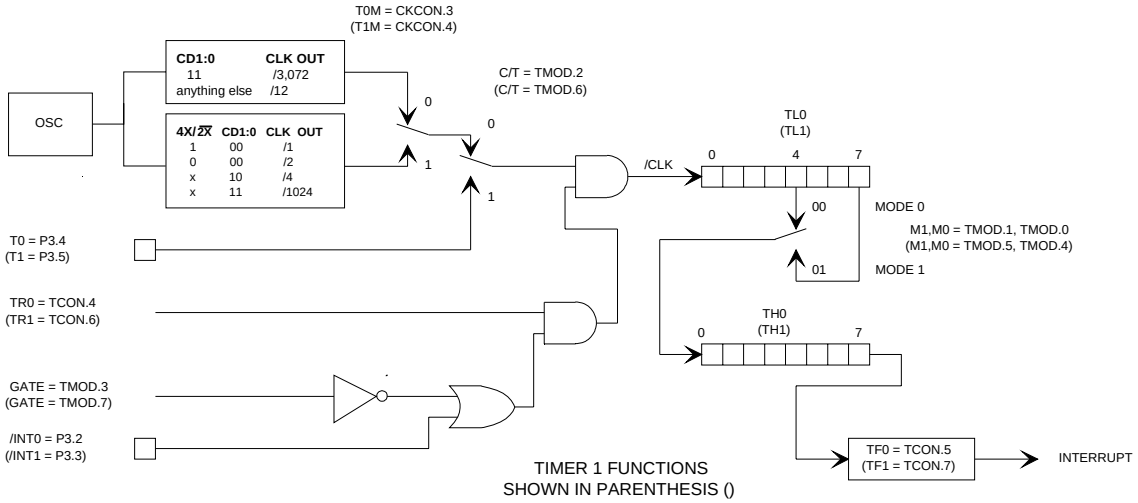
The functionality of these three timers is summarized as follows:

Timer 0	**Timer 1**	**Timer 2**
13-bit timer/counter	13-bit timer/counter	16-bit timer/counter
16-bit timer/counter	16-bit timer/counter	16-bit timer with capture
8-bit timer w auto-reload	8-bit timer w auto-reload	16-bit auto-reload timer/counter
Two 8-bit timer/counters	Ext. control pulse timer/counter	16-bit auto-reload up/down counter/timer
Ext. control pulse timer/counter	Baud rate generator	Baud rate generator
		Timer output clock generator
		16-bit timer/counter with compare

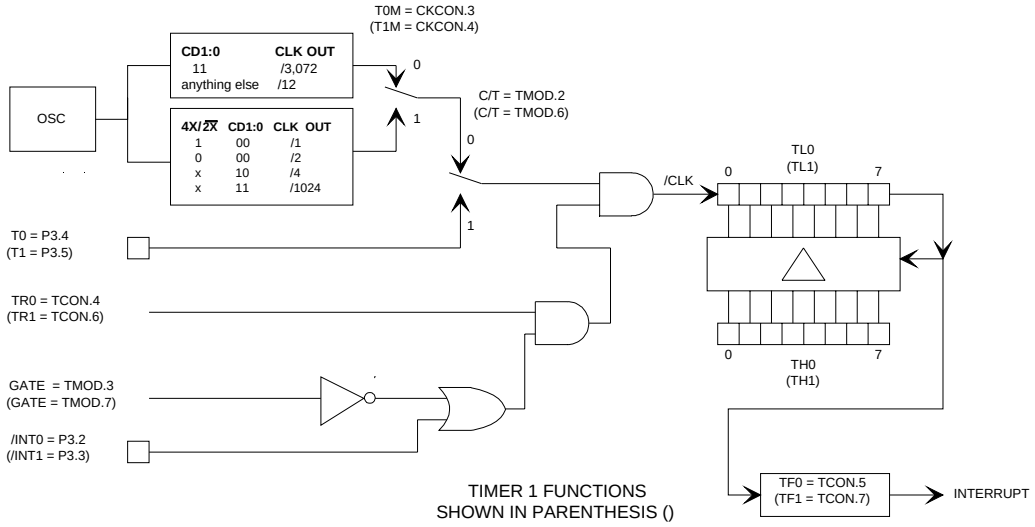
TIMERS 0 AND 1

As stated earlier, the only differences in timer/counter 0 and 1 contained in older members of the High-Speed Microcontroller family and those found in the DS87C550 are in the clock selection possibilities. Drawings of these possibilities for various modes are given below.

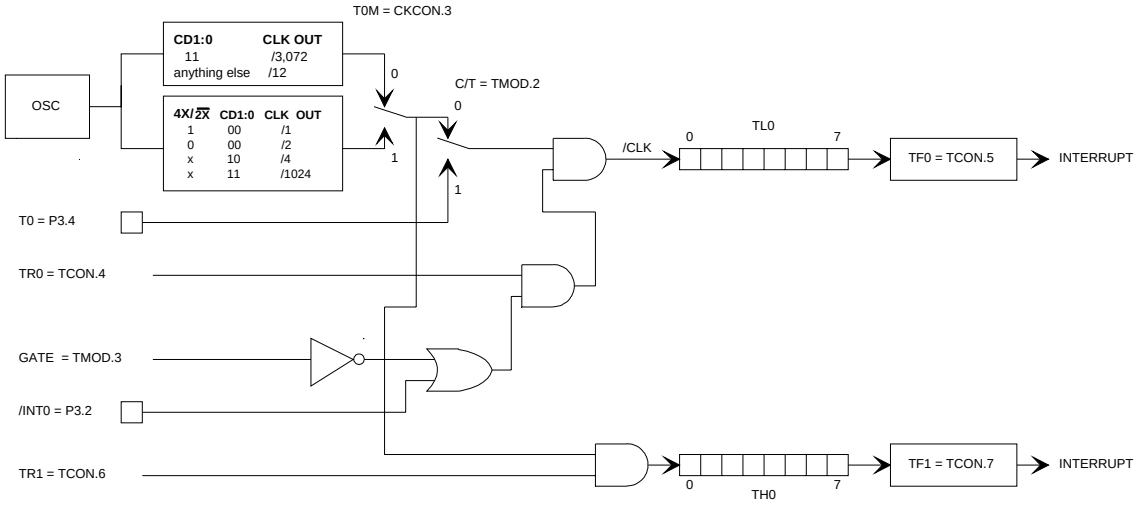
TIMER/COUNTER 0 AND 1, MODES 0 AND 1: Figure 11-1.



TIMER/COUNTER 0 AND 1, MODE 2: Figure 11-2.



TIMER/COUNTER 0, MODE 3: Figure 11-3.



From the drawings, Table 11-1 can be derived. This table shows that when the timer/counter is used as a timer (i.e., it counts some number of system clocks), the frequency of timer clocks is a function of the crystal oscillator (or external oscillator) and timer clock source settings. The bits CD1, CD0, and 4X/$\overline{2X}$ determine the system clock available to the timer, and the bits TxM (i.e., T0M and T1M) determine the clock source. The specific timer mode (8-bit, 16-bit, reload, etc.) does not affect the number of oscillator clocks per timer clock.

OSCILLATOR CLOCKS PER TIMER 0 or 1 CLOCK : Table 11-1

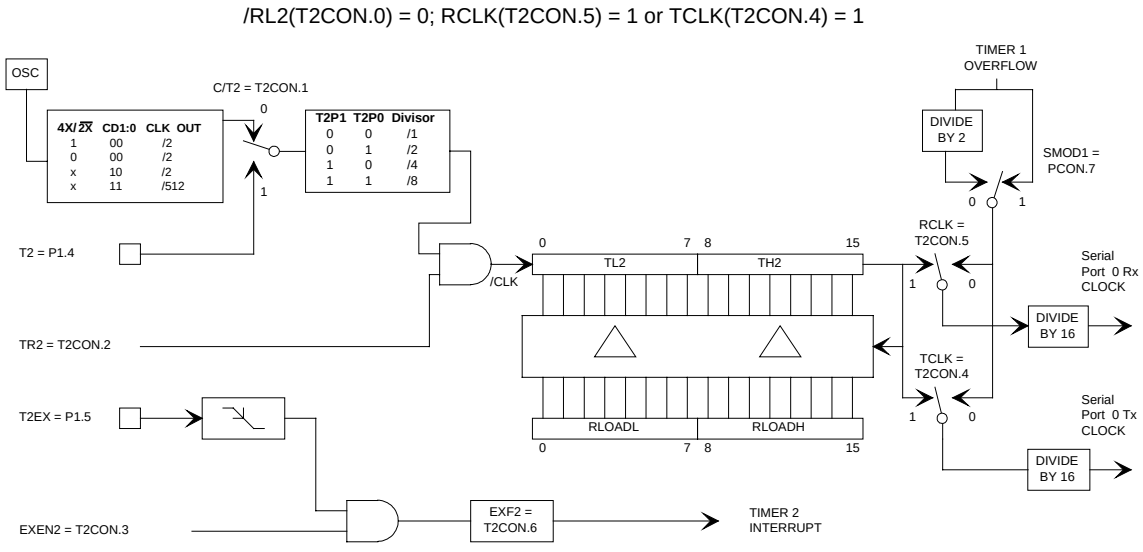
CD1	CD0	4X/$\overline{2X}$	TxM = 0	TxM = 1
0	0	1	12	1
0	0	0	12	2
0	1	X	Reserved	Reserved
1	0	X	12	4
1	1	X	3,072	1,024

Where TxM is either the T0M or T1M SFR bit

TIMER 2

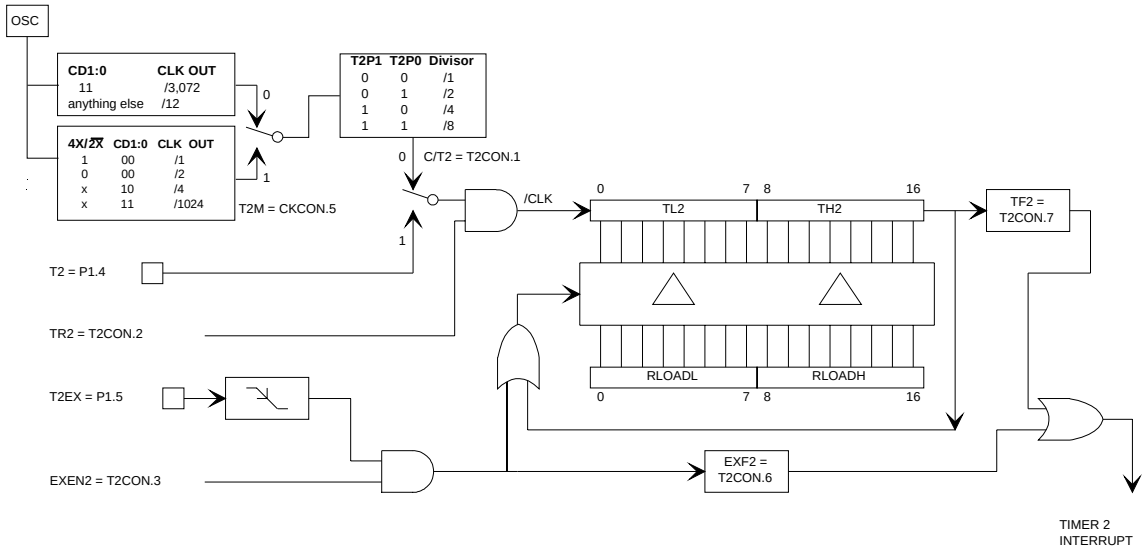
As stated earlier, the functionality of Timer/Counter 2 in the DS87C550 is a superset of the functions found on earlier members of the High-Speed Microcontroller family. However, for the same functions, the clock selection options are slightly different. The available clock selection options for various Timer 2 modes are shown in the drawings below.

TIMER/COUNTER 2, BAUD RATE GENERATOR MODE: Figure 11-4.

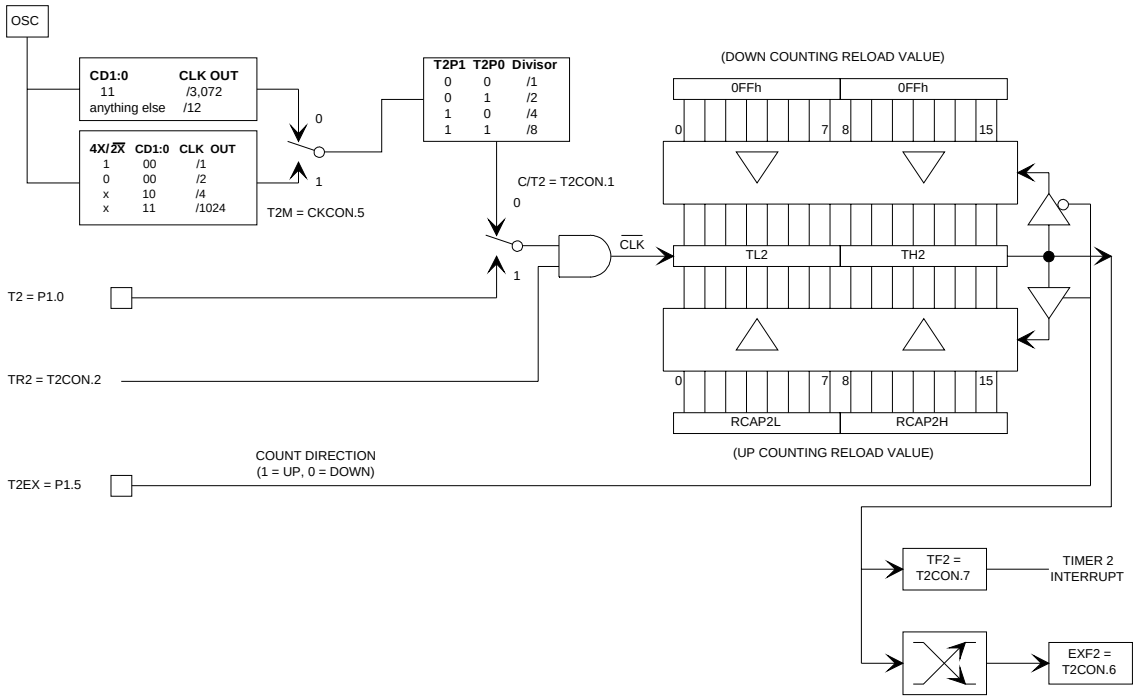


TIMER/COUNTER 2, AUTO RELOAD MODE (/RL2 = 0): Figure 11-5.

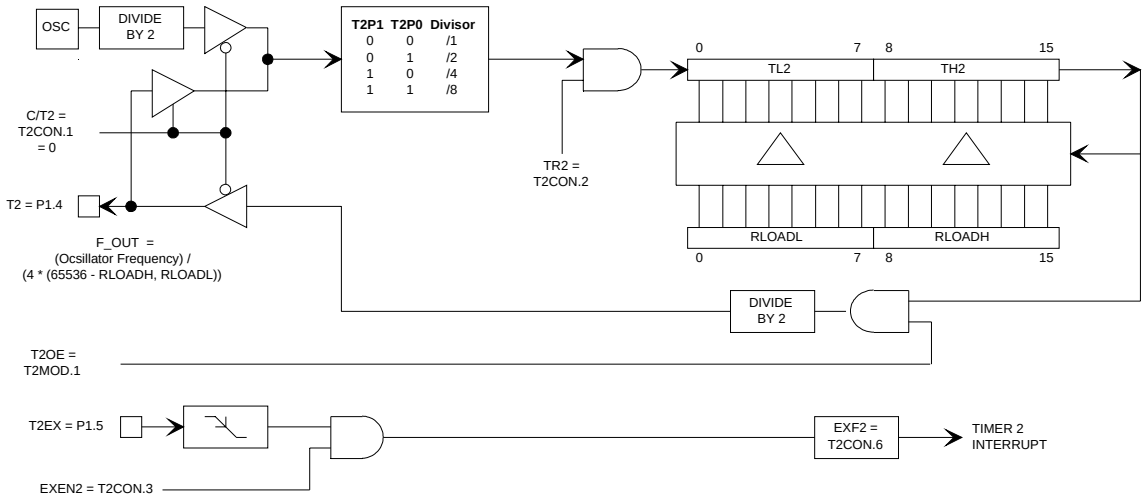
(a) DCEN = 0



(b) DCEN = 1



TIMER/COUNTER 2, CLOCK OUTPUT MODE: Figure 11-6.



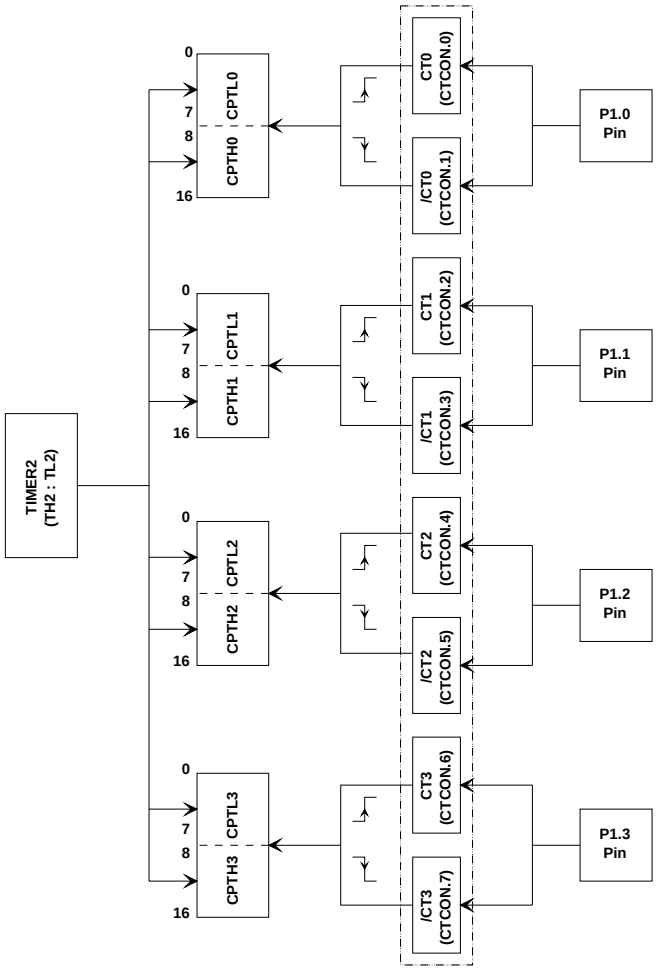
TIMER 2 CAPTURE MODE

The capture mode of Timer 2 in the DS87C550 is slightly different from that function implemented on other High-Speed Microcontrollers. In the DS87C550, there are four 16-bit registers (eight 8-bit registers concatenated) that can capture values. Timer 2's output is the value that is captured when appropriate. It should be noted that Timer 2 can be configured in a number of different ways (i.e., counter, timer, auto-reload, etc.) and still be used for the capture mode. Regardless of the meaning of Timer 2's value, it is this timer's output that is captured under the pre-established conditions.

The secondary function of four I/O pins (P1.0 – P1.3) is used to trigger one of the individual capture functions. If an appropriate edge occurs on the particular pin (as determined by of bits CTCON.7), then Timer 2's output at that time (all 16-bits) will be written into the associated capture register (CPTH0:CPTL0, CPTH1:CPTL1, CPTH2:CPTH2, CPTH3; CPTL3). By setting or clearing the bits on the CTCON register appropriately, the user can determine whether the rising or falling edge of the pin causes a capture.

It should be noted that the pins used to cause a Timer 2 capture are shared with the external interrupt pins. When used as an external interrupt, each pin can be programmed to be active high or low using the same bits (CTCON7:0). This functionality is illustrated in Figure 11-7 below.

TIMER/COUNTER 2 CAPTURE MODE: Figure 11-7.



TIMER 2 COMPARE MODE

Timer 2 of the DS87C550 offers a compare mode not previously included in any of the earlier high-speed microcontroller family members. The actual comparison takes place between Timer 2's 16-bit output and three 16-bit (actually six 8-bit concatenated) compare registers CMPH0:CMPL0, CMPH1:CMPL1, CMPH2:CMPL2. These compare registers are initialized by the user's software, and when/if a match occurs between Timer 2's output and one or more of the compare registers, the related interrupt flag is set and the interrupt is serviced if enabled. There are three separate interrupt flags with related enable and priority bits shown in the table below.

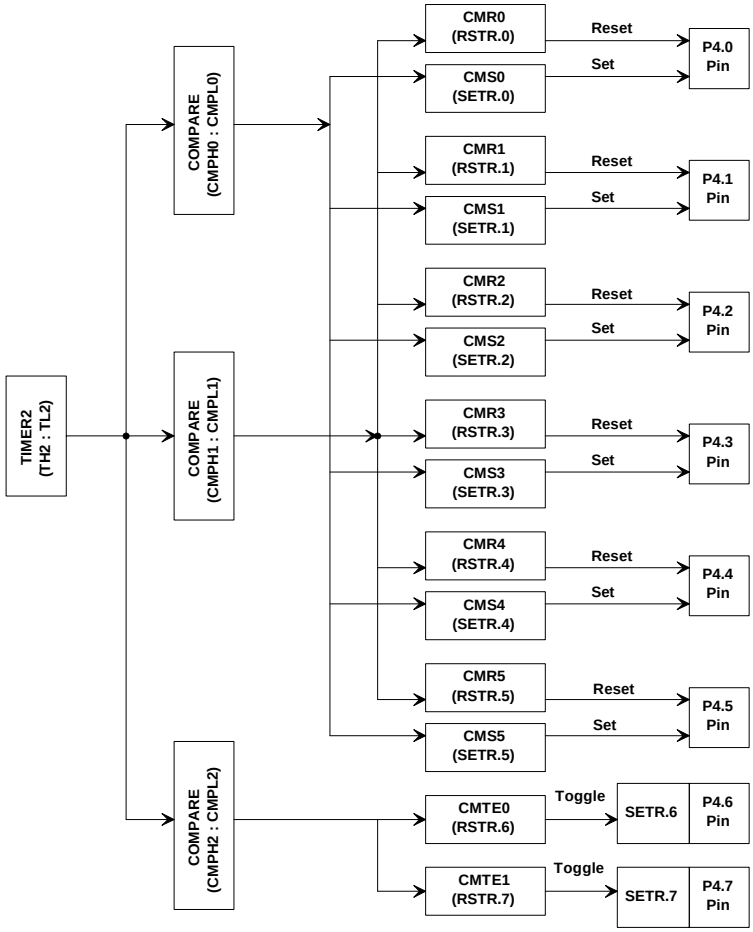
TIMER/COUNTER 2 CAPTURE MODE: Table 11-2.

COMPARE	FLAG	ENABLE	PRIORITY
0	CM0F (T2IR.4)	ECM0 (EIE.4)	PCM0 (EIP.4)
1	CM1F (T2IR.5)	ECM1 (EIE.5)	PCM1 (EIP.5)
2	CM2F (T2IR.6)	ECM2 (EIE.6)	PCM2 (EIP.5)

In addition to causing an interrupt, it is also possible to cause certain pins of the device (P4.0 – 4.7) to be set, reset or toggled in response to a match. This function is useful for building "PWM-like" operations

using Timer 2. Registers SETR and RSTR contain bits to enable this function. If a match occurs between Timer 2's output and CMPH0:CMPL0, port pins P4.0 to 4.5 are set when the corresponding bits in the set enable register (SETR) are logic 1. If the match is with CMPH1:CMPL1, port pins 4.0 to 4.5 are reset when the corresponding bits of the reset/toggle enable register (RSTR) are logic 1. A match with CMPH2:CMPL2 toggles port pins P4.6 and P4.7 if the corresponding bits in the reset/toggle enable register (RSTR) are logic 1. If any of the bits in SETR or RSTR are 0, then the corresponding port pin function is disabled. This functionality is further illustrated in Figure 11-8.

TIMER/COUNTER 2 COMPARE MODE: Figure 11-8.



WATCHDOG TIMER

The DS87C550 contains a watchdog timer that is very similar to that found in other members of the high-speed microcontroller family. It is driven directly off of the internal crystal oscillator (or external clock attached to XTAL1), and offers several divider chains to provide a wide variety of time-out selections. The watchdog timer in the DS87C550 is slightly different in several minor ways from that found in other high-speed microcontrollers. For one, the available divisors and hence the resulting time-out values are different. In earlier members of the family, divisors of 2^{17}, 2^{20}, 2^{23}, and 2^{26} were available. In the DS87C550, divisors of 2^{15}, 2^{18}, 2^{21}, and 2^{24} are available. Additionally, the system clock generation offers divisors of 1, 2, 3 and 256. Combining these two divisor chains, watchdog time-out periods ranging from 993 us to 130.2 s (2^{15} to 2^{32}) are possible with a 33 MHz crystal (or oscillator). With a crystal of 11.0952 MHz, time-out values from 2.963 ms up to 387.1 s (6.42 minutes) are possible. As can be seen, the

watchdog timer can provide extremely log time-out periods that would be more difficult to achieve with the standard 8051 timers.

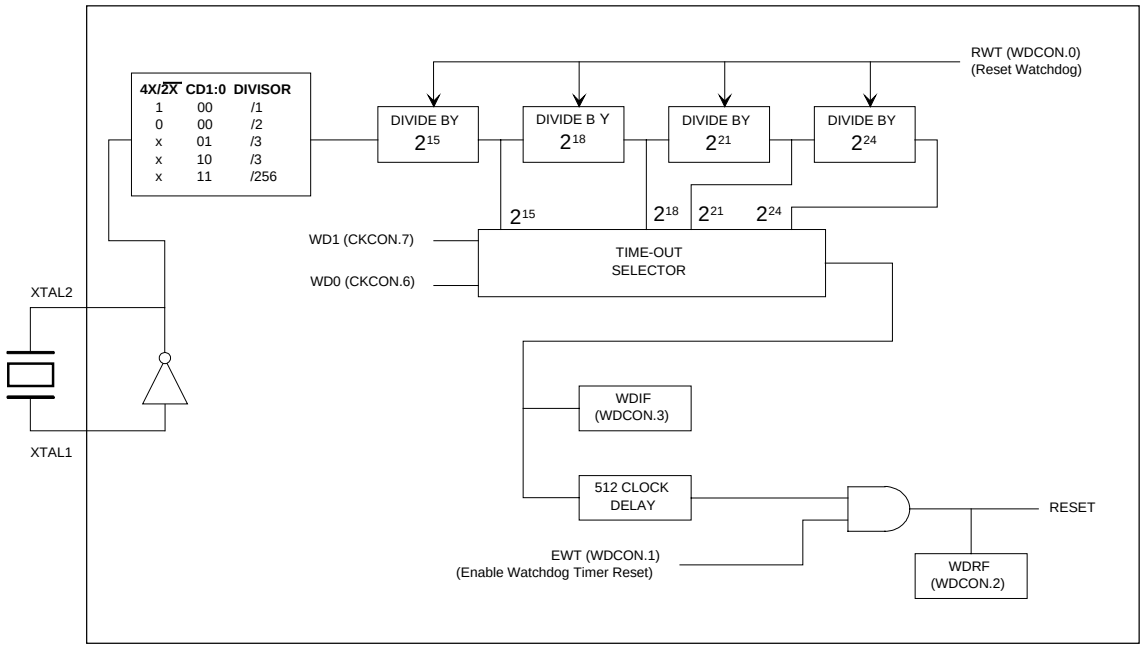
Another difference unique to the watchdog timer on the DS87C550 is the fact that there is no interrupt associated with it. Since there are so many other interrupt sources on the DS87C550, it was decided that an interrupt for the watchdog was less important than others and therefore not provided. While the interrupt flag still exists (WDCON.3) and it can be polled, there is no actual interrupt or interrupt vector location associated with this flag.

The possible settings for the watchdog interrupt time-out period are given in table 11-3. Remember that the actual reset (if enabled) occurs 512 clocks after the interrupt flag is set.

WATCHDOG TIMER INTERRUPT TIME-OUT PERIOD (in clocks): Table 11-3.

4X/$\overline{2X}$	**CD1:0**	**WD1:0=00**	**WD1:0=01**	**WD1:0=10**	**WD1:0=11**
1	00	2^{15}	2^{18}	2^{21}	2^{24}
0	00	2^{16}	2^{19}	2^{22}	2^{25}
X	01	2^{17}	2^{20}	2^{23}	2^{26}
X	10	2^{17}	2^{20}	2^{23}	2^{26}
X	11	2^{25}	2^{28}	2^{31}	2^{34}

WATCHDOG TIMER: Figure 11-9.



Other than those differences described above, the watchdog timer is operated in the same way as earlier versions of the design. The time-out period is selected using the WD1 and WD0 bits (CKCON7:6). As the watchdog timer is a free running timer, it should be reset using the Reset Watchdog Timer bit (RWT= WDCON.0) before enabling the reset with the Enable Watchdog Timer Reset bit (EWT = WDCON.1) This will place the timer into a known state before the reset is enabled. As in the earlier designs, the RWT and EWT bits are timed access protected.

Crystal Failure Detection

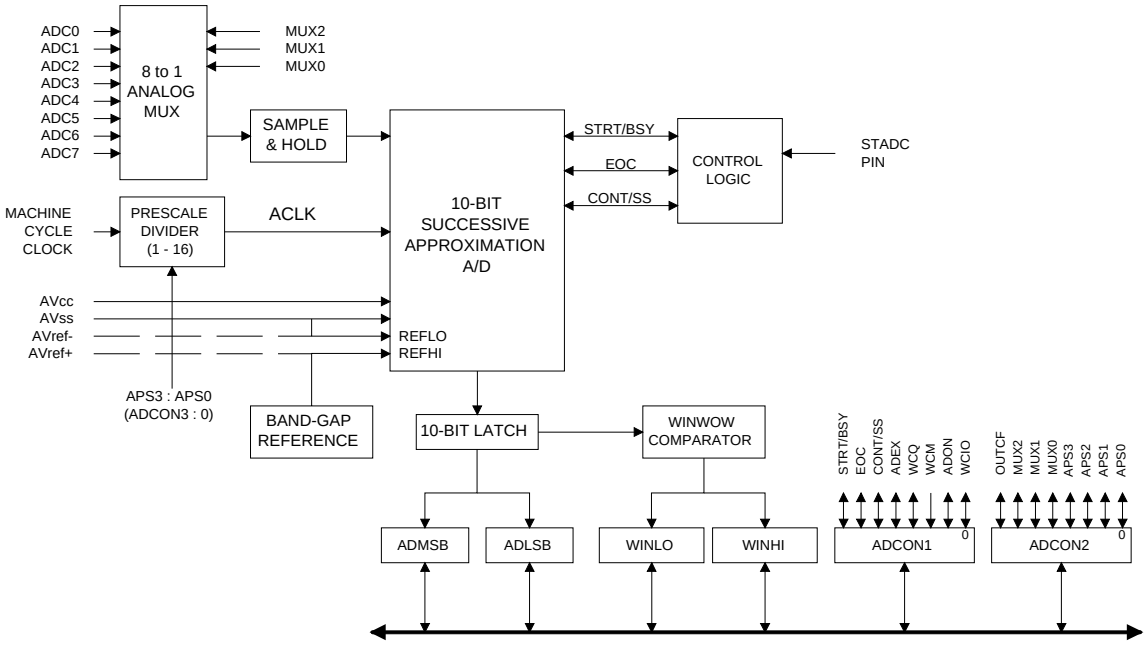
An additional feature first introduced on the DS87C550 is the crystal failure detection circuit. While this feature is not directly related to the watchdog timer, it is discussed here because of its intended use. In earlier high-speed microcontroller designs, the watchdog timer was tied directly to the crystal oscillator just as it is in the DS87C550. While it has never been known to happen, it was theorized that it would be possible for the oscillator to stop functioning at a time when the processor was commanding some external action to take place. Since in this case, there is no oscillator to drive the watchdog timer, it would never reach its time-out value causing a processor to be reset. Since this could result in undesirable system performance, the crystal oscillator failure detection circuitry was added. In the event of an oscillator failure, this circuitry will cause the processor to be reset. If the oscillator frequency falls below TBD kHz, the circuitry will be triggered and will cause a processor reset. This feature is enabled by setting the OFDE bit (PCON.4), and disabled by clearing it.

SECTION 18: ANALOG TO DIGITAL CONVERTOR

Some members of the High-Speed Microcontroller family (DS87C550 for example) incorporate an on-board Analog-to-Digital Converter (A/D). When incorporated, these devices provide eight channels of analog input, internal sample & hold circuitry, a 10-bit successive approximation A/D converter, and related output and control registers. Additionally, a window comparison function is provided that allows conversion results to be ignored unless they are "of interest" where "of interest" is defined by the user as being within (or alternatively outside) a particular range of values. An internal precision voltage reference for the A/D function is also provided, along with the ability to select an externally supplied voltage reference for maximum flexibility.

The 10-bit output of the conversion process is read by the processor through two 8-bit registers, and the arrangement of this result is available in two formats as selected by the user. In 8-bit output mode, the most significant 8-bits of the result are placed in the A/D MSB result register (ADMSB). In 10-bit output mode, the two most significant bits of the result ADR9:ADR8 are placed in the two least significant bit positions of the ADMSB result register, and the eight least significant bits of the result are placed in the A/D LSB result register (ADLSB). A prescaler clock divider is included which allows a wide range of conversion clock frequencies to be selected.

A/D CONVERTER BLOCK DIAGRAM : Figure AD1



A block diagram of the complete A/D function is shown in Figure AD1. As can be seen, operation and control of the A/D is very straight forward, and is controlled via ADCON1, ADCON2, and the A/D reference select bit ADRS in the PWMADR register. If the window comparison function is used, then the WINHI and WINLO registers contain the user supplied window comparison values. If the A/D is configured for interrupt driven operation (rather than polled mode), then interrupt enable bits EA (IE.7) EAD (IE.6) bits must also be set.

A/D OPERATIONAL OVERVIEW

To enable the A/D function, the ADON bit (ADCON1.1) must be set. Following the setting of the ADON bit, software should delay 4 µs before performing a conversion to allow the A/D converter to complete its power-up initialization. The A/D converter will measure one of the eight available input pins, ADC7-0, selected using the MUX2:MUX0 bits of the ADCON2 register. The initial conversion can be started by

writing a "1" to the STRT/BSY bit of the ADCON1 register, or alternately by a falling edge on the STADC pin when the ADEX bit of the ADCON1 is set. When the conversion starts, the analog value on the selected pin is held in the sample and hold circuitry for the remainder of the conversion.

The "latched" analog signal is applied to the input of the 10-bit successive approximation converter. The converter requires 16-clock cycles (provided from the prescaler) to perform a conversion. Due to the dynamic nature of the conversion process, the clock into the converter (t_{ACLK}) must be in the range of 1.0 µs ≤ t_{ACLK} ≤ 6.25 µs. Therefore the fastest possible conversion requires 16.0 µs, and the slowest conversion requires 100 µs. During the conversion process, the STRT/BSY (ADCON1.7) bit remains high until the conversion is complete at which time the hardware resets it. The hardware also sets the EOC bit (ADCON1.6) when the conversion is complete, and software must clear it if it is to be used on the next conversion.

After the first conversion is complete, another can be initiated using the STRT/BSY bit as described. Alternately, another conversion will be started automatically at the end of the first conversion if the CONT/SS bit (ADCON1.5) is set. In this continuous conversion mode, it is probably most convenient to enable the A/D interrupt function otherwise continuous polling (and clearing) the EOC bit would be required.

At the end of a conversion, the result is latched into a 10-bit latch, and is made available to the two A/D result registers ADMSB and ADLSB. As discussed above, the result may be presented in either 10-bit mode or 8-bit mode as selected by the user. Further details of the A/D functions are discussed below.

PRESCALER

The A/D clock Prescaler allows a wide selection of clock frequencies to be used for the conversion process. It divides the machine cycle clock frequency by the value written to the APS3:0 bits (ADCON1.3:0), and provides this resulting clock to the successive approximation converter. Since the machine cycle clock can be osc/1, osc/2, ocs/4, or osc/1024 as determined by bits CD1:0 and 4X/$\overline{2X}$ of the PMR register, then the period of the clock output from the prescaler is given in Table AD1.

A/D Conversion Clock Period Calculation : Table A/D1

4X/$\overline{2X}$	**CD1:0**	**t_{ACLK}**
1	00	(t_{OSC}*1)*(APS3:0+1)
0	00	(t_{OSC}*2)*(APS3:0+1)
X	01	(t_{OSC}*4)*(APS3:0+1)
X	10	(t_{OSC}*4)*(APS3:0+1)
X	11	(t_{OSC}*1024)*(APS3:0+1)

As an brief example of this calculation, assume that the processor is running using a 33.0 MHz crystal, and is in its reset default condition for the machine clock. If it is desired to set the A/D for its fastest possible conversion time (recalling that 1.0 µs ≤ t_{ACLK} ≤ 6.25 µs), to what value what should APS3:0 be set. From row 3 of Table A/D1, it can be seen that 8 is the desired value.

(1/33Mhz * 4) * (8+1) = 1.091 µs

As a further example, if the clock multiplier is used in 2X mode along with an 11.0592 MHz crystal , then from row two of the table it can be shown that 5 is the desired value.

(1/11.0592MHz * 2) *(5 + 1) = 1.085 µs

A/D REFERENCE VOLTAGE

A precision reference voltage is required by the A/D conversion process. Since this reference voltage is used in all conversions, it must be precise and stable. Otherwise the A/D result will be similarly unstable or imprecise (see the A/D result equation below). This reference may be obtained either from an internal band-gap or from a user supplied external source as selected by the ADRS (PWMADR.7) bit.

$$\text{A/D Result} = 1024(Vin - AV_{REF-}) / (AV_{REF+} - AV_{REF-})$$

When the ADRS bit is cleared (reset default condition), the internal band-gap is selected as the A/D's positive reference voltage, and analog ground is the negative reference. This internal band-gap produces a positive A/D reference voltage of 2.5 volts typically (see DC specifications) and therefore limits the range of analog voltages on the input pins to the range of 0 to 2.5 volts. If a larger analog input voltage is desirable, an external reference voltage may be used.

When the ADRS bit is set, the user may provide an external voltage reference to the A/D on pins AV_{REF+} and AV_{REF-}. These voltages have minimum and maximum specifications associated with them which must be followed (see DS specifications). However, AV_{REF+} may be in the range of the analog supply voltage AV_{CC} which is most frequently 5 volts. Therefore a larger range of analog input voltages (0 to 5 volts) is possible when an external voltage reference is used.

A/D INTERRUPT

The interrupt flag for the A/D converter is the EOC bit (ADCON1.6) and is set by hardware when the current conversion completes. Once set it must be cleared by software. This interrupt is qualified by several settings. First for an A/D interrupt to be acknowledged, the EAD (Enable A/D Interrupt, IE.6) bit must be set. Additionally as with all interrupts, the global interrupt enable bit, EA (IE.7) must be set before any interrupt will be acknowledged. The A/D interrupt is also qualified by the WCM bit (ADCON1.2) when the user selects the window comparison function by setting the WCQ (ADCON1.3) bit. With WCQ set, an A/D interrupt will occur only when the comparison function is true. If WCQ is not set, then an A/D interrupt will occur any time when EOC is set and enable bits EAD and EA are set. A more detailed description of the window comparison function follows.

WINDOWED COMPARATOR

The A/D Converter found in some Dallas High-Speed Microcontrollers has a unique feature associated with it called the Window Comparator. This feature allows the user to establish boundaries against which each A/D converter result is compared. If the results of the A/D are "of interest" as defined by the user supplied boundary conditions, the feature will allow an interrupt to be generated. Otherwise no interrupt is generated, and the results can be ignored. This relieves the processor of the burden of acknowledging data that is not of interest.

The user enables this feature by setting the Window Comparator Qualifier bit WCQ (ADCON1.3). Of course as described in the discussion of interrupts, the A/D interrupt enable and global interrupt enable bits must also be set for an interrupt to be acknowledged. The user sets the boundaries with the two 8-bit registers WINHI and WINLO. The values loaded into these registers are compared to each A/D result. It is important to note that the comparison is performed between one of these registers and the eight MSBs of the A/D result. This comparison takes place before the 10-bit A/D result is passed to the two 8-bit result registers ADMSB and ADLSB. Therefore the user selected method of displaying the 10-bit result has no affect on the comparison function. The comparison is always performed on the eight MSBs of the

A/D result. This must be taken into account when selecting the values to be loaded into the WINHI and WINLO registers.

The equations for the window comparison function are as follows:

$$WCM = (WINHI > ADMSB) \text{ AND } (ADMSB \geq WINLO) \text{ when } WCIO = 0$$

Or

$$WCM = (WINHI \leq ADMSB) \text{ OR } (ADMSB < WINLO) \text{ when } WCIO = 1$$

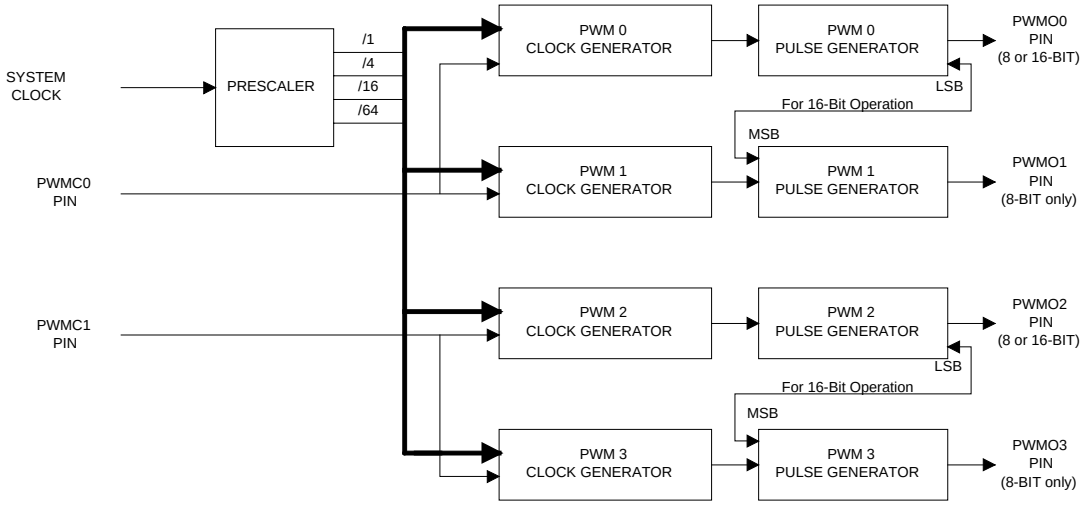
The WCIO bit defines whether the data of interest is inside (WCIO = 0) or outside (WCIO = 1) the boundaries defined by the contents of WINHI and WINLO. As a specific example suppose that you want to use the windowed comparison function to allow an A/D interrupt to occur when the A/D results are in the range of 256_{10} and 511_{10}. The first thing to recognize is that the comparison takes place between the 8-MSbs of the A/D result and the 8-bit WINHI and WINLO registers which leaves the two LSBs of the result unused. Converting the base 10 numbers to base 16 and truncating to the 8-MSBs, it can be seen that the WINLO register should be loaded with 40_{16} and the WINHI register with $7F_{16}$. Since the two LSBs of the A/D result are ignored in the comparison, the interrupt will occur for values from 256_{10} and 508_{10}. This slight inaccuracy is inherent due to the 8-bit comparison. By setting the global interrupt enable bit EA (IE.7), A/D interrupt enable EAD (IE.6) bit, the Window Compartor qualifier bit WCQ (ADCON1.3), and clearing the Window Compare Inside/Outside bit WCIO (ADCON1.0) the desired function will be implemented. By simply setting the WCIO bit, the data outside the stated boundaries can be acknowledged.

SECTION 19: PULSE WIDTH MODULATION

Some members of the High-Speed Microcontroller family incorporate Pulse Width Modulation (PWM) capability. When incorporated, there are four independent 8-bit channels provided, each of which can operate at a different repetition rate and with an independent pulse width setting. For more precise PWM requirements, two 8-bit PWM channels can be combined into one 16-bit PWM channel. For 16-bit operation, channels PWM0 and PWM1 are combined and/or PWM2 and PWM3 are combined. As shown in Figure PWM1, each channel of PWM can accept any one of four clock signals derived from the processor's machine cycle clock, or an externally generated clock available on the PWMC0 or PWMC1 pins. These two PWM external clock input pins are distributed to the four channels as shown. Each PWM channel has its own output pin that is a second function for one of the processor's parallel I/O pins.

The PWM function is divided into three functional modules: the prescaler, the Clock Generator, and the Pulse Generator. Each of these modules is described in detail below.

PWM Block Diagram (8-Bit Mode) : Figure PWM1.



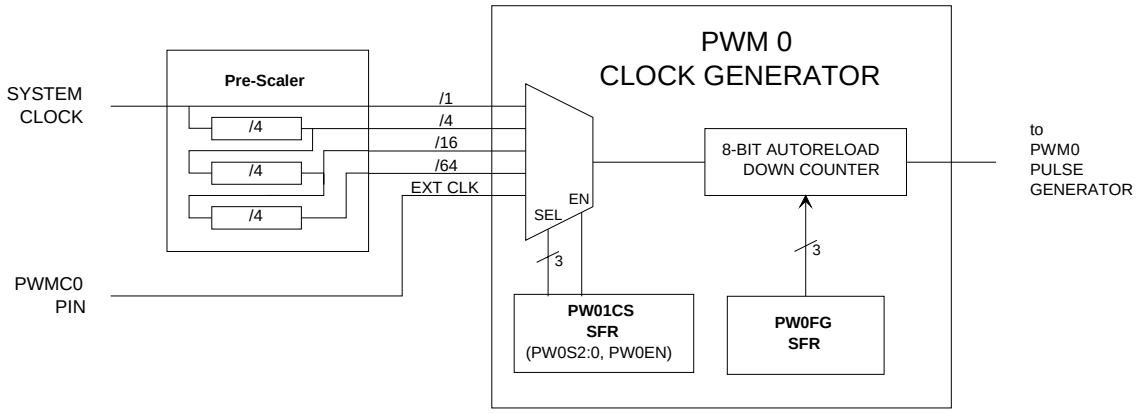
PRESCALER

There is a single prescaler that divides the machine cycle clock by 1, 4, 16, or 64, and each of these outputs is available to all four PWM channels simultaneously. Since the machine cycle clock is an integer division of the crystal oscillator (or external clock source connected to XTAL1), and this division factor is determined by the user's setting of CD1: 0 and $4X/\overline{2X}$, then these bits will also affect the frequency of operation of the PWM channels as well. The selection of one of the four clock sources available as outputs from the prescaler or one of the externally supplied clocks is made individually, channel by channel with the PW0S2:0 (PW01CS7:5), PW1S2:0 (PW01CS3:1), PW2S2:0 (PW23CS7:5), and PW3S2-0 (PW23CS3:1) bits in SFRs.

CLOCK GENERATOR

As shown in Figure PWM1, the four clock outputs available from the prescaler are all provided to each of the four Clock Generator modules along with the two external PWM clock inputs. The Clock Generator modules simply select one of the available clocks, use this selection to clock an 8-bit auto-reload counter, and provide the output of this counter to the Pulse Generator module. The logical behavior of PWM0's Clock Generator module is shown in Figure PWM2. All other Clock Generators operate in the same way.

PWM0 CLOCK GENERATOR : Figure PWM2



Special Function Registers PW01CS and PW23CS contain the bits that select the prescaler output and also enable/disable the Clock Generator module. The SFR PW01CS contains enable bits for PWM channels 0 (PW0EN = PW01CS.4) and 1 (PW1EN = PW01CS.0). The SFR PW23CS contains similar enables for PWM channels 2 (PW2EN = PW23CS.4) and 3 (PW3EN = PW23CS.0). These enable bits are cleared to 0 (disabled) on a reset, and therefore must be set to 1 before the PWM function can be used.

As illustrated in Figure PWM2, the Clock Generator is an 8-bit auto-reloadable down counter. When the counter decrements to zero in response to the selected clock input, it is reloaded with the value stored by the application software in the PWM frequency generator registers PW0FG, PW1FG, PW2FG, and PW3FG. Because of the design of these counters, the frequency of the clock output from the Clock Generator module is defined as:

PWM-Clock = prescaler Output / (N+1)
where N = contents of PWxFG register
or
N = (prescaler Output/PWM-Clock)-1

Therefore if the frequency generator register (PW0FG, PW1FG, PW2FG, or PW3FG) is loaded with the value of 0, then the clock is divided by 1, and passed to the Pulse Generator module. If the value of 1 is loaded, the clock is divided by 2 and passed to the Pulse Generator. If the value of 255 (maximum value) is loaded, then the clock passed to the Pulse Generator is the prescaler clock divided by 256. With the ability to select the prescaler output (/1, /4, /16, or /64), and the ability to select its divisor from a value between 1 and 256 (inclusive), a large range of PWM-Clock rates is possible. Table PWM1 shows the equations for determining the PWM-Clock rate.

PWM Clock Generation : Table PWM1

4X/$\overline{2X}$	**CD 1:0**	PWxS2:0=000	**PWxS2:0=001**	**PWxS2:0=010**	**PWxS2:0=011**	**PWxS2:0=1xx**
1	00	(osc/1)/(N+1)	(osc/4)/(N+1)	(osc/16)/(N+1)	(osc/64)/(N+1)	PWMCx/(N+1)
0	00	(osc/2)/(N+1)	(osc/8)/(N+1)	(osc/32)/(N+1)	(osc/128)/(N+1)	PWMCx/(N+1)
x	01	(osc/4)/(N+1)	(osc/16)/(N+1)	(osc/64)/(N+1)	(osc/256)/(N+1)	PWMCx/(N+1)
x	10	(osc/4)/(N+1)	(osc/16)/(N+1)	(osc/64)/(N+1)	(osc/256)/(N+1)	PWMCx/(N+1)
x	11	(osc/1,024)/(N+1)	4,096/(N+1)	(osc/16,384)/(N+1)	(osc/65,536)/(N+1)	PWMCx/(N+1)

where: osc = frequency of the attached crystal or external clock source attached to XTAL1
N = contents of PWxFG register
PWMCx = Frequency of the external PWM clock input PWMC0 (P6.4) or PWMC1 (P6.5)

As a simple example of this timing information, assume that the processor is in its reset default condition running from an 11.0592 MHz crystal (or external clock), and the user wants to establish the maximum repetition rate for PWM0 while maintaining a machine cycle clock of divide by 4. In this case, $4X/\overline{2X}$ = xx, CD1:0 = 10b, PW01S2:0 = 000b, and PW0FG = 00000000b. Since N = 00h (i.e., PW0FG = 00h), the equation shows this combination will provide the maximum PWM clock rate. Performing the calculation:

$$\begin{aligned}\text{PWM Clock} &= \frac{\text{Osc} / 4}{N+1} \\ &= \frac{11.0592\ \text{MHz} /4}{0+1} \\ &= 2.76\ \text{MHz}\end{aligned}$$

Since the PWM Pulse Generator section is basically an 8-bit counter (in 8-bit PWM mode), 256 clocks are required for the counter to make one complete cycle. This dictates that the repetition rate of the PWM channel will be the PWM clock/256. Therefore in this example, the repetition rate of PWM0 will be:

$$\begin{aligned}\text{Repetition Rate (8-bit mode)} &= \frac{\text{PWM Clock}}{256} \\ &= \frac{2.76\ \text{MHz}}{256} \\ &= 10.80\ \text{kHz} \\ &\therefore\ 92.59\ \text{us}\end{aligned}$$

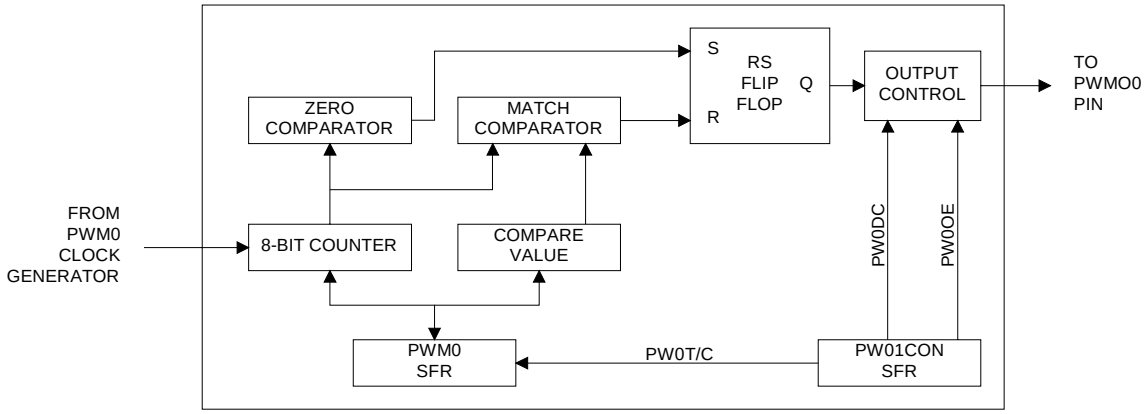
PULSE GENERATOR

The Pulse Generator portion of the PWM function generates the PWM output. The logical operation of the Pulse Generator section of PWM0 in 8-bit mode is illustrated in Figure PWM3. All other PWM channels operate in a similar fashion. From the user's perspective, the Pulse Generator can be considered simply an 8-bit up counter driven by the PWM Clock. As this 8-bit counter rolls over from 0FFh to 00h, the corresponding PWM output is set high. As the counter continues to count up and pass through the user selected value stored in register PWM0, PWM1, PWM2, or PWM3, the PWM output is cleared to zero. In this way, the duty cycle of the PWM output is determined by the value loaded by the user into the PWMx (i.e., PWM0, PWM1, PWM2, PWM3) registers. The duty cycle of the PWM function is given by the following equation:

$$\text{PWM Duty Cycle(\%)} = \frac{\text{PWMx}}{256}$$

With the minimum value of zero loaded into PWM register, the equation illustrates that this produces a 0% duty cycle signal (never goes high). With the maximum value of 255 loaded into the PWM register, a duty cycle of 99.609% is generated. If a duty-cycle of precisely 100% is required, the DC override bits PW0DC (PW01CON.6), PW1DC (PW01CON.2), PW2DC (PW23CON.6), and PW3DC (PW23CON.2) will force the PWM output to be high for the entire cycle when set.

PWM0 PULSE GENERATOR : Figure PWM3.



The user supplied value contained in the PWMx register is reloaded into the compare value register when there is a match between the counter and the value. This means that changing the value of PWMx more frequently than once every 256 PWM-Clocks will have no effect. This prevents software from creating "glitches" in the PWM output.

The PWMx registers also provide a means to read or write the value of the associated 8-bit counter. When the bits PW0T/C (PW01CON.4), PW1T/C (PW01CON.0), PW2T/C (PW23CON.4), or PW3T/C (WP23CON.0) are cleared (reset default condition), reading or writing the associated PWMx register accesses the PWM user supplied comparison value. When these bits are set, reading or writing the associated PWMx register accesses the Pulse Generator's 8-bit counter. If it is important that the first cycle of the PWM have precisely correct timing, then this feature may be used to initialize the 8-bit counter to zero.

The rollover condition of the Pulse Generator from 0FFh to 00h is detected and causes the PWM output to be set as described previously. This condition also causes the corresponding flag bit PW0F (PW01CON.7), PW1F (PW01CON.3), PW2F (PW23CON.7), or PW3F (PW23CON.3) to be set providing a means for software to determine when the rollover occurs. Software is the only mechanism to clear these bits once they are set.

The outputs of the PWM channels share pins with parallel I/O port pins. To enable the PWM channel's output, the corresponding PWM Output Enable bit must be set. These enable bits PW0OE (PW01CON.5), PW1OE (PW01CON.1), PW2OE (PW23CON.5), and PW3OE (PW23CON.1) are all cleared by reset, and must be set before using the PWM outputs.

16-Bit PWM Mode

The four 8-bit PWM functions offer the unique ability to be cascaded into two 16-bit PWM functions. By setting PWE0 (PWMADR.0) or PWE1 (PWMADR.1), 16-bit mode is enabled for PWM0 or PWM1 respectively. Note that the 16-bit PWM function called PWM1 is actually a concatenation of resources from 8-bit PWM2 and PWM3 functions. As an example, the output pin of 16- bit PWM1 is PWMO2, which is normally the output pin for 8-bit PWM2. This relationship is true for a number of registers and bits used in the 16-bit PWM1 function. For 16-bit PWM0, the output pin will be PWMO0 as would be expected. These differences will be detailed in the following discussion.

Achieving 16-bit PWM operation involves the concatenation of resources found in the Pulse Generator section of the PWM function. This is illustrated in Figure PWM4. As shown, two 8-bit counters are combined to form a 16-bit counter and two 8-bit compare value registers are combined to form a 16-bit compare value register. Additionally, two 8-bit zero comparators are combined to form a 16-bit zero comparator, and two 8-bit match comparators are combined to form a 16-bit match comparator.

Other than this concatenation of 8-bit blocks into 16-bit blocks, operation of the Pulse Generator section is the same as in 8-bit mode. As the 16-bit counter passes through zero, the output of the PWM is set. As the counter continues to count and passes through the user supplied value, the PWM output is reset. Therefore the user-supplied value determines the pulse width of the PWM output. The equation for the duty cycle is given by the following equation:

$$\text{PWM Duty Cycle}(\%) = \frac{\text{PWMx}}{65{,}536}$$

where PWMx is the 16-bit user-supplied value

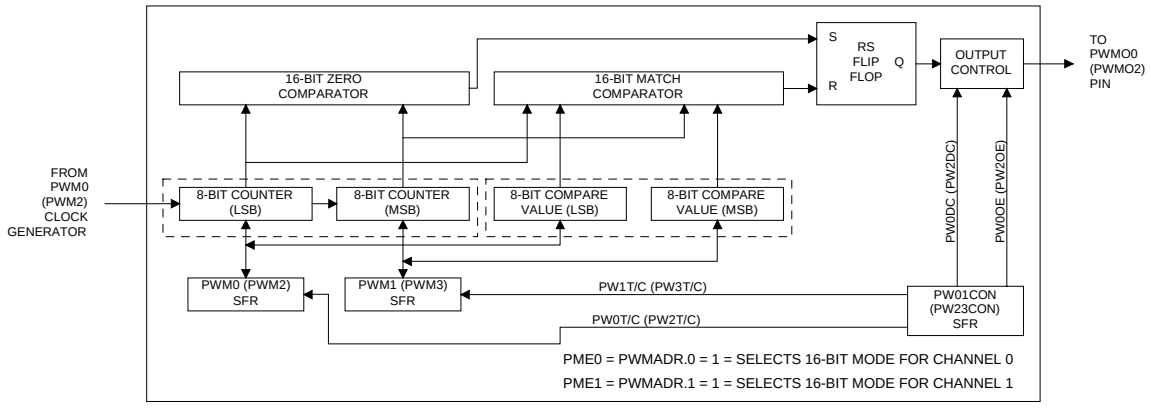
The 16-bit user defined value is loaded through two 8-bit SFRs. For the 16-bit PWM0 function, SFR PWM0 loads the LSB of the user defined value, and PWM1 loads the MSB of the user defined value. For the 16-bit PWM1 function, PWM2 loads the LSB and PWM3 loads the MSB. Note that in Figure PWM4, all registers and bits associated with the 16-bit PWM0 function are shown without parentheses. All registers and bits associated with the 16-bit PWM1 functions are shown in parentheses.

If a duty cycle of exactly 100% is required, setting the bit PW0DC (PW01CON.6) forces the output of 16-bit PWM0 high for the entire counter cycle. Similarly, setting the bit PW2DC (PW23CON.6) forces the output of 16-bit PWM1 high for the entire counter cycle.

The user-supplied value loaded into the PWMx registers is reloaded into the associated compare value register when there is a match between the counter and the user supplied value. Therefore, changing the value of PWMx more frequently than once every 65,536 PWM-Clocks will have no effect.

As illustrated in Figure PWM4, the PWMx registers can access either the counters or the compare value register. Setting bit PW0T/C (PW01CON.4) allows register PWM0 to access the LSB of the 16-bit counter. Clearing it accesses the LSB compare value register.

16-BIT PWM MODE PULSE GENERATOR : Figure PWM4.



Similarly, setting bit PW1T/C (PW01CON.0) allows register PWM1 to access the MSB of the 16-bit counter. Clearing it accesses the MSB compare value register.

As described in 8-bit mode, flags PW0F (PW01CON.7) and PW2F (PWM23CON.7) indicate a rollover from 0FFh to 00h of the counters for 16-bit PWM0 and PWM1 respectively.

The PWM outputs are disabled on all forms of reset. To enable the output of 16-bit PWM0 on pin PWMO0, the bit PW0OE (PW01CON.5) must be set, and to enable the output of 16-bit PWM1 on pin PWMO2, the bit PW2OE must be set.

All of the Clock Generator sections operate exactly as they did in 8-bit mode. The thing to remember is that only registers and bits for Clock Generators used for 8-bit PWM0 and PWM2 will function in 16-bit mode. Other registers and bits used in 8-bit mode (PWM1, PWM3 as examples) no longer serve a purpose in 16-bit mode.

As before, bits PW0S2:0 and PW0EN (PW01CS7:4) will enable the prescaler and will determine the selected PWM-Clock input for 16-bit PWM0. Similarly, bits PW2S2:0 and PW2EN (PW23CS7:4)) will enable the prescaler and will determine the selected PWM-Clock input for 16-bit PWM1. Bits PW01CS3:0 and PW23CS3:0 have no effect when the corresponding PWM channel is set for 16-bit mode.

The same is true for the Clock Generator divisors. Only those associated with 8-bit PWM functions 0 and 2 will have any effect. It is important to recognize that while the Clock Generators operate in the same way and produce the same clock frequencies as they did in 8-bit mode, the repetition rate will be much longer since the clock now operates a 16-bit counter in the Pulse Generator module. Therefore the equation for the 16-bit mode repetition rate is as follows:

$$\text{Repetition Rate (8-bit mode)} = \frac{\text{PWM Clock}}{65{,}536}$$

Using the previous example where the PWM clock was 2.76 MHz, the 16-bit repetition rate becomes:

$$\begin{aligned}\text{Repetition Rate (8-bit mode)} &= \frac{\text{PWM Clock}}{65{,}536} \\ &= \frac{2.76\ \text{MHz}}{65{,}536} \\ &= 42.11\ \text{Hz} \\ &\therefore\ 23.74\ \text{ms}\end{aligned}$$

Since 16-bit mode typically results in a fairly slow repetition rate, it may be desirable to adjust the CD1:0 and $4X/\overline{2X}$ bits to select a divide by 1 or divide by 2 of the crystal as the machine cycle clock. This results in an increased frequency being available to the PWM function.