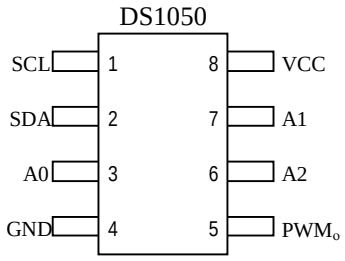
DALLAS SEMICONDUCTOR

DS1050/DS1052
5-Bit Programmable Pulse Width Modulator

FEATURES

- Single 5-bit programmable pulse width modulator (PWM)
- Adjustable Duty Cycle: 0% to 100%
- 2.5V to 5.5V Operation
- Standard Frequency Values: 1 kHz, 5 kHz, 10 kHz, and 100 kHz
- 2-Wire Addressable Interface
- Packages: 8-Pin DIP, 8-Pin (150 mil) SOIC and 8-Pin (118 mil) µSOP
- Operating Temperature: -40°C to +85°C

PIN ASSIGNMENT



8L-DIP
8L-(150 mil) SOIC
8L-(118 mil) µSOP

Ordering Information

Part Number	Frequency	Package
DS1050M-001	1 kHz	8-P 300 mil DIP
DS1050M-005	5 kHz	8-P 300 mil DIP
DS1050M-010	10 kHz	8-P 300 mil DIP
DS1052M-100	100 kHz	8-P 300 mil DIP
DS1050Z-001	1 kHz	8-P 150-mil SOIC
DS1050Z-005	5 kHz	8-P 150-mil SOIC
DS1050Z-010	10 kHz	8-P 150-mil SOIC
DS1052Z-100	100 kHz	8-P 150-mil SOIC
DS1050U-001	1 kHz	8-P 118-mil µSOP
DS1050U-005	5 kHz	8-P 118-mil µSOP
DS1050U-010	10 kHz	8-P 118-mil µSOP
DS1052U-100	100 kHz	8-P 118-mil µSOP

PIN DESCRIPTION

V_{CC}	2.5V to 5.5V Power Supply
PWM_O	PWM Ouput
A0,A1,A2	Device Address
SDA	Serial Data I/O
SCL	Serial Clock Input
GND	Ground

DESCRIPTION

The DS1050/DS1052 is a programmable 5-bit pulse width modulator featuring a 2-wire addressable controlled interface. The DS1050/DS1052 provides operation from power supplies ranging from 2.5 volts up to 5.5 volts. The PWM output provides a signal that swings from 0 volt to V_{CC} (power supply). The DS1050 requires a typical operating current of 500 µA and a programmable shutdown supply current of 1 µA. The DS1052 requires a typical operating current of 500 µA and a programmable shutdown supply current of 1 µA.

Four standard PWM output frequencies are offered and include 1 kHz, 5 kHz, 10 kHz, and 100 kHz. The 2-wire addressable interface allows operation of multiple devices on a single 2-wire bus and provides compatibility with other Dallas Semiconductor 2-wire devices: including real-time clocks (RTCs), digital thermometers, and digital potentiometers.

The device is ideal for low cost LCD contrast and/or brightness control, power supply voltage adjustment, battery charging or current adjustment. The DS1050/DS1052 is offered in standard integrated circuit packaging including the 8-L DIP, 8-L (150 mil) SOIC, and the space saving 8-L (118 mil) µSOP.

OPERATION

Interface protocol is simplified to an 8-bit control byte and 8-bit data-byte. Information can be read or written to the DS1050/DS1052 including a commanded shutdown operation.

Power-up Configuration

The DS1050/DS1052 powers-up to half-scale (10000B) providing 50% duty-cycle. Once powered, the PWM output can be changed via the 2-wire addressable serial port.

Pin Description

V_{cc}- Power supply terminal. The DS1050/DS1052 will support operation from power supply voltages ranging from +2.5 volts to +5.5 volts.

GND - Ground terminal.

PWM_O – Pulse-width modulated output. This output is a square-wave having amplitudes from 0 volt to V_{CC}. The duty cycle of this output is governed by a 5-bit control register. Output duty cycles range from 0% to 96.88%. An additional command sequence will provide a 100% duty cycle or “full-on”.

SCL – Serial clock input.

SDA – Serial bi-directional data I/O.

A0,A1,A2 - Device address (chip selects).

2-Wire Addressable Serial Port Control.

The 2-wire serial port interface supports a bi-directional data transmission protocol with device addressing. A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master". The devices that are controlled by the master are "slaves". The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1050/DS1052 operates as a slave on the 2-wire bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

The following I/O terminals control the 2-wire serial port: SDA, SCL, A0, A1, A2. A 2-wire serial port overview and timing diagrams for the 2-wire serial port can be found in Figures 2 and 3, respectively. Timing information for the 2-wire serial port is provided in the “AC Electrical Characteristics” table for 2-wire serial communications.

The following bus protocol has been defined (See Figure 2).

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.
Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Figure 2 details how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Within the bus specifications, a regular mode (100 kHz clock rate) and a fast mode (400 kHz clock rate) are defined. The DS1050/DS1052 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the command/control byte. Next follows a number of data bytes. The slave returns an “acknowledge” bit after each received. byte.

2. **Data transfer from a slave transmitter to a master receiver.** The first byte (the command/control byte) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' is returned.

The master device generates all serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1050/DS1052 may operate in the following two modes:

1. **Slave receiver mode**: Serial data and clock are received through SDA and SCL, respectively. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave (device) address and direction bit.

2. **Slave transmitter mode**: The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1050/DS1052 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

SLAVE ADDRESS

A command/control byte is the first byte received following the START condition from the master device. The command/control byte consists of a four bit control code. For the DS1050/DS1052, this is set as ***0101*** binary for read/write operations. The next three bits of the command/control byte are the device select bits or slave address (A2, A1, A0). They are used by the master device to select which of eight possible devices is to be accessed. When reading or writing the DS1050/DS1052, the device select bits must match the device select pins (A2,A1,A0). The last bit of the command/control byte (R/W) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The command control byte is presented in Figure 3.

Following the START condition, the DS1050/DS1052 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 0101 control code, the appropriate device address bits, and the read/write bit, the slave device outputs an “acknowledge” signal on the SDA line.

COMMAND AND PROTOCOL

The command and protocol structure of the DS1050/DS1052 allows the user to read or write the PWM configuration register or place the device in a low-current state (shut-down mode) and recall the device from a low-current state.. Additionally, the 2-wire command/protocol structure of the DS1050/DS1052 will support eight different devices that can be uniquely controlled.

Figure 4a,b,c,d, & e show the five different command and protocol bytes for the DS1050/DS1052. These include the following command operations: 1) Set PWM Duty Cycle, 2) Set PWM Duty Cycle 100%, 3) Set shutdown mode, 4) Set recall mode, 5) Read PWM configuration register.

The command operation **“Set PWM Duty Cycle”** is used to configure the output duty cycle of the device. The DS1050/DS1052 has a 5-bit resolution and is capable of setting the duty cycle output from 0% up to 96.88% in steps of 3.125%. A binary value of (00000B) sets the duty cycle output at 0% while a binary value of (11111B) sets the duty cycle output at 96.88%.

The command operation **“Set PWM Duty Cycle 100%”** is used to configure the output duty cycle of the device to a “full-on”. This command is provided in addition to the Set PWM Duty Cycle command for flexibility and convenience in total duty cycle coverage. It allows the user to provide a total duty cycle range from 0% to 100%.

The command operation **“Set shutdown mode”** is used to provide a low-current (inactive state) state for the DS1050/DS1052. When in a low-current state the DS1050/DS1052 will draw currents less than or equal to 1 μA. The PWM_O output will be high impedance.

The command operation **"Set Recall Mode"** is used to recall the DS1050/DS1052 from a low-current state. The value of the PWM_O output is recalled to that prior to initiating a "Set shutdown mode" command.

The **"Read PWM Duty Cycle"** command is used to read the current setting of the PWM configuration register. Information returned by this command includes PWM output value, as well as, whether the device is in a shutdown configuration.

PWM data values and control/ command values are always transmitted most significant bit (MSB) first. During communications, the receiving unit always generates the "acknowledge".

Reading the DS1050/DS1052

As shown in Figure 4e, the DS1050/DS1052 provides one ***read command operation***. This operation allows the user to read the current setting of the PWM configuration register. Specifically, the R/W bit of the command/control byte is set equal to a 1 for a read operation. Communication to read the DS1050/DS1052 begins with a START condition which is issued by the master device. The command/control byte from the master device will follow the START condition. Once the command/control byte has been received by the DS1050/DS1052, the part will respond with an ACKNOWLEDGE. The read/write bit of the command/control byte, as stated, should be set equal to '1' for reading the DS1050/DS1052.

When the master has received the ACKNOWLEDGE from the DS1050/DS1052, the master can then begin to receive the PWM configuration register data. As mentioned this data will be transmitted MSB first. Once the eight bits of the PWM configuration register have been transmitted, the master will need to issue an ACKNOWLEDGE, unless it is the only byte to be read, in which case the master issues a NOT ACKNOWLEDGE. If desired the master may stop the communication transfer at this point by issuing the STOP condition. Final communication transfer is terminated by issuing the STOP command. Again, the flow of the read operation is presented in Figure 4e.

Writing the DS1050/DS1052

A data flow diagram for writing the DS1050/DS1052 is shown in Figure 4a,b,c, & d. The DS1050/DS1052 has three write commands that are used to change the PWM configuration register or the shutdown and recall mode of the device.

All the write operations begin with a START condition. Following the START condition, the master device will issue the command/control byte. The read/write bit of the command/control byte will be set to '0' for writing the DS1050/DS1052. Once the command/control byte has been issued and the master receives the acknowledgment from the DS1050/DS1052, PWM configuration data is transmitted to the DS1050/DS1052 by the master device.

A data byte for the DS1050/DS1052 will contain *PWM configuration data* and *shutdown/recall command data*. The five least significant bits of data specify the PWM configuration value while the three most significant bits specify the whether the device is to be shutdown or recalled. When the DS1050/DS1052 has received the data byte, it will respond with an ACKNOWLEDGE. At this point, the new PWM configuration register value and shutdown/recall command value will be updated in the DS1050/DS1052. The master device, after the receipt of the ACKNOWLEDGE, can continue to transmit additional data bytes or if the transaction is complete respond with the STOP condition. The 2-wire serial timing diagram is presented in Figure 5.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +6.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those conditions indicated in the operation section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-40°C to +85°C; V_{CC} = 2.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply voltage	V_{CC}	+2.5		+5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; V_{CC} = 2.5V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current Active	I_{CC}	DS1050 DS1052		50 500		µA µA	2 2
Input Leakage	I_{LI}				+1	µA	
Input Logic 1	V_{IH}				V_{CC}+0.5	V	1,3
Input Logic 0	V_{IL}				0.3 V_{CC}	V	1,3
Input Logic Levels A0, A1, A2		Input Logic 1 Input Logic 0	0.7 V_{CC} GND-0.5		0.3 V_{CC} 0.3 V_{CC}	V	4
Input Current each I/O pin		0.4<$V_{I/O}$<0.9 V_{CC}	-10		10	µA	
Standby Current 3V 5V	Istby			0.5	1	µA	5
LOW level ouput voltage	V_{OL1}	3 mA sink current	0.0		0.4	V	
	V_{OL2}	3 mA sink current	0.0		0.6	V	
I/O Capacitance	$C_{I/O}$			10		pF	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}		0		50	ns	

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC} = 2.5V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
SCL clock frequency	f_{SCL}		0 0		400 100	kHz	*,6 **
Bus free time between STOP and START condition	t_{BUF}		1.3 4.7			µs	*,6 **
Hold time (repeated) START condition	$t_{HD:STA}$		0.6 4.0			µs	*,7,6 **
Low period of SCL clock	t_{LOW}		1.3 4.7			µs	*,6 **
High period of SCL clock	t_{HIGH}		0.6 4.0			µs	*,6 **
Data hold time	$t_{HD:DAT}$		0 0		0.9	µs	*,6,8,9 **
Data set-up time	$t_{SU:DAT}$		100 250			ns	*,6 **
Rise time of both SDA and SCL signals	t_R		$20+0.1C_B$		300 1000	ns	*,10 **
Fall time of both SDA and SCL signals	t_F		$20+0.1C_B$		300 300	ns	*,10 **
Set-up time for STOP condition	$t_{SU:STO}$		0.6 4.0			µs	* **
Capacitive load for each bus line	CB				400	pF	10
PWM Output Change	t_{PWMo}			2		periods	11

* fast mode
** standard mode

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC} = 2.5V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Output Frequency Tolerance			-20		+20	%	12
Output Impedance					200	Ω	
Full-scale duty cycle				96.88		%	13
Zero-scale duty cycle				0		%	13
Absolute Linearity			-0.5		+0.5	LSB	14
Relative Linearity			-0.25		+0.25	LSB	15
Resolution				5		Bits	13

NOTES:

1. All voltages are referenced to ground.
2. I_{STBY} specified for V_{CC} between 3.0V and 5.0V. control port logic pins are driven to the appropriate logic levels. Appropriate logic levels specify that logic inputs are within a 0.5V of ground or V_{CC} for the corresponding inactive state.
3. I/O pins of fast mode devices must not obstruct the SDA and SCL lines if V_{CC} is switched off.
4. Address Inputs, A0, A1, and A2, should be tied to either V_{CC} or GND depending on the desired address selections.
5. I_{STBY} specified for V_{CC} between 3.0V and 5.0V, control port logic pins are driven to the appropriate logic levels.
6. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT} > 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT} = 1000+250=1250$ ns before the SCL line is released.
7. After this period, the first clock pulse is generated.
8. The maximum $t_{SU:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
9. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
10. C_B - total capacitance of one bus line in picofarads, timing referenced to $(0.9)(V_{CC})$ and $(0.1)(V_{CC})$.
11. A PWM output duty cycle change will occur with 2 periods of the output frequency when a change is initiated.
12. The absolute frequency output of the PWM can be expected to fall within a ±20% range from the nominal specified value of the device.
13. The DS1050/DS1052 is a 5-Bit PWM. The output duty cycles of the device range from 0% to 100% in step sizes of 3.125%. The “Set PWM Duty Cycle 100%, allows the PWM output to be set to “full-on”.
14. Absolute Linearity is used to compare measured duty cycle against expected duty cycle as determined by the DAC setting. The DS1050/DS1052 is specified to provide an absolute linearity of ±0.5 LSB.
15. Relative Linearity is used to determine the change in duty cycle between adjacent or successive DAC settings. The DS1050/DS1052 is specified to provide a relative linearity specification of ±0.25 LSB.

Figure 1 **BLOCK DIAGRAM**

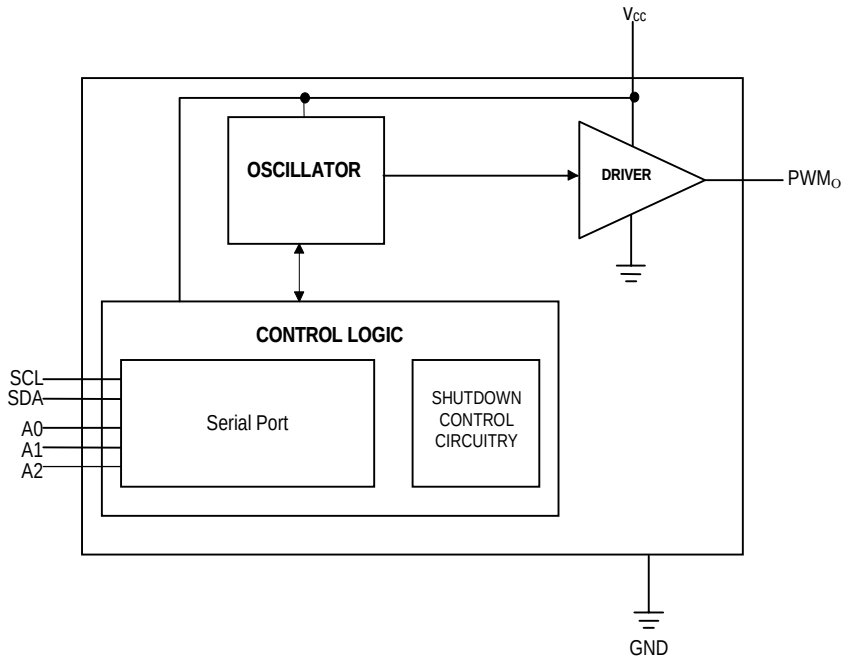


Figure 2 **2-WIRE ADDRESSABLE SERIAL PORT OVERVIEW**

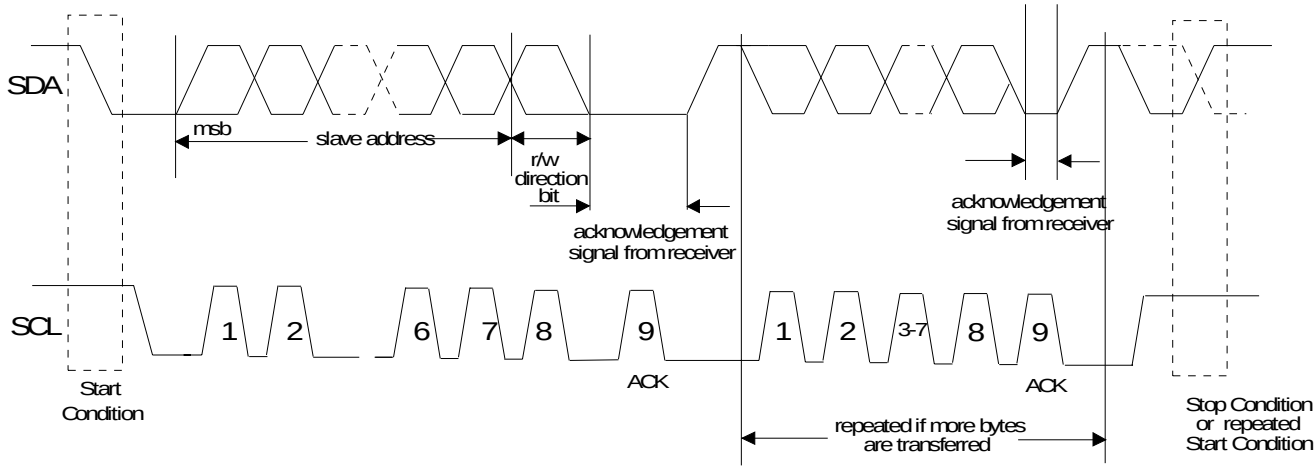


Figure 3 **COMMAND/CONTROL BYTE**

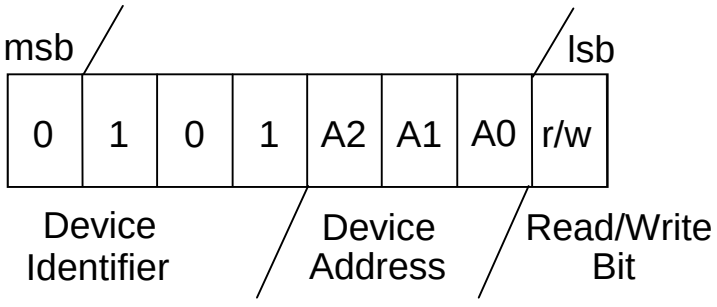


Figure 4 **DS1050/DS1052 COMMANDS AND PROTOCOL**

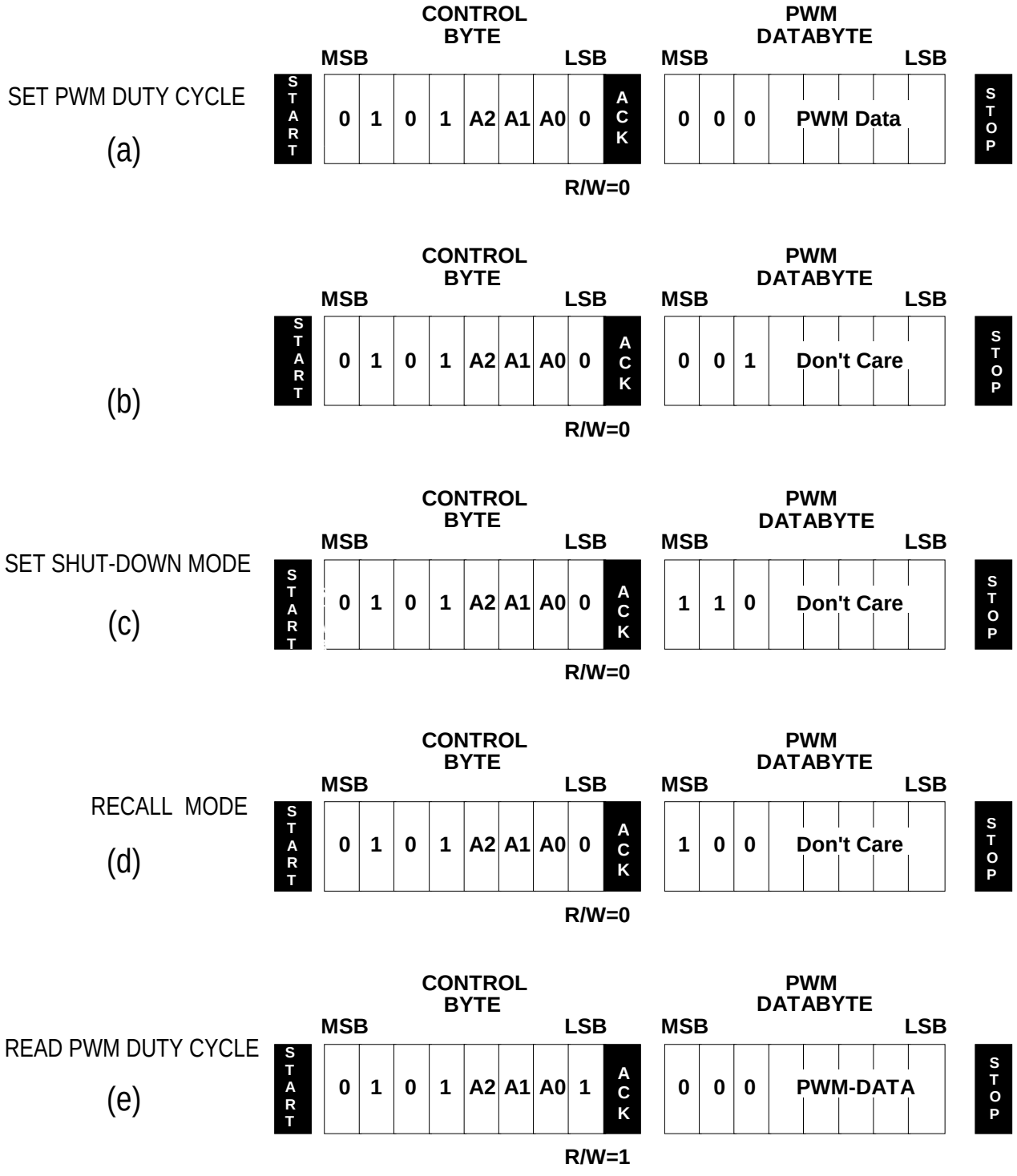


Figure 5 **2-WIRE SERIAL DIAGRAMS**