

DESCRIPTION

This application note discusses the extended features for the following PC Real Time Clocks (RTCs): DS1585/87, DS1685/87, DS1688/91, DS17285/87, DS17485/87, DS17A84/86, and DS17885/87. Also included is an initialization flow chart for the PC RTCs. All of these devices incorporate these extended features unless otherwise noted.

EXTENDED FEATURES

Auxiliary Battery Input (V_{BAUX})

The auxiliary battery input, V_{BAUX} , provides the power required to use the kickstart, wake up, power-on output, and the 32 kHz square wave in the absence of system power. The timekeeping and RAM data can also be maintained by this power source. If this input is going to be used, bit 7 in control register 4Bh (ABE) must be set to a logic 1. If this input is not going to be used then ABE must be set to a logic 0 and the V_{BAUX} input tied to ground.

Kickstart Input (\overline{KS})

The kickstart pin is intended to be used in the battery backed mode in conjunction with the \overline{PWR} signal providing systems with power management control. A signal providing a ground closure will force the \overline{PWR} signal to transition low. The \overline{KS} pin can also be used as an interrupt input while V_{CC} is applied.

Power-On Output (\overline{PWR})

This output is open drain and requires an external pull-up resistor for proper operation. This signal is intended to be used in conjunction with \overline{KS} and the wakeup alarm for power management features.

32 KHz Square Wave Output (SQW)

The SQW output pin can provide a 32-kHz square wave for power management purposes. The DS1685/87, DS1688/91, DS17285/87, DS17485/87, and DS17885/87 will provide the 32 kHz each time the system power, V_{CC} , is applied. The DS1585/87, DS1689/93, and DS17A84/86 must be programmed, to output the 32 KHz, after the system power is applied.

Silicon Serial Number

A unique 64-bit silicon serial number is located in bank 1 registers 40h – 47h. The serial number is divided into three separate parts. The first byte, location 40h, contains a model number to identify the device type and revision. The following is a list of the model numbers currently assigned for the devices mentioned above:

Model #	Part #
70h	DS1585/87
71h	DS1685/87
72h	DS17285/87
73h	DS1688/91
73h	DS1689/93
74h	DS17485/87
78h	DS17885/87

The second part of the serial number is a unique 48-bit binary number located in registers 41h – 46h. The third part of the serial number is located in register 47h and contains a CRC number used to validate the data in registers 40h – 46h. This 8-byte serial number is read only.

Century Byte

The century byte, located in bank 1 register 48h, will update every 100 years keeping track of the century.

Date Alarm Byte

The date alarm byte, located in bank 1 register 49h, can be used in conjunction with the time of day alarm providing a system with a wakeup alarm programmable up to 31 days.

Control Registers 4Ah and 4Bh

See the Register Description section.

Extended RAM Software Port

The extended user RAM can be accessed through software via three internal registers located in bank 1 locations 50h, 51h, and 53h. Locations 50h and 51h are used for the RAM address and location 53h is used for the data transfer. This unique feature eliminates the need for external hardware and at the same time provides the ability to switch RAM densities without any hardware modification required. This feature is not available on the DS1688/91 or DS1689/93.

V_{CC} Elapsed Time Counter

A 32-bit V_{CC} powered elapsed time counter, located in bank 1 registers 54h (LSB) through 57h (MSB), will keep track of how long system power has been applied. This counter will update once per second as long as V_{CC} is within nominal limits and the oscillator and countdown chain are enabled. When V_{CC} falls outside of the nominal limits the counter is halted and the elapsed time is retained. This counter can be read or written at the user's discretion. This feature is available only on the DS1688/91 and DS1689/93.

V_{BAT} Elapsed Time Counter

A 32-bit V_{BAT} powered elapsed time counter, located in bank 1 registers 58h (LSB) through 5Bh (MSB), will keep track of how long the system has been in service. This counter will run continuously and update once per second as long as V_{BAT} or V_{BAUX} is within nominal limits and the oscillator and countdown chain are enabled. This counter can be read or written at the user's discretion. This feature is available only on the DS1688/91 and DS1689/93.

Power Cycle Counter

A 16-bit power cycle counter, located in bank 1 registers 5Ch (LSB) and 5Dh (MSB), will keep track of the number of times a system is powered on and off. Each time system power, V_{CC}, is applied within nominal limits, the counter will be incremented by one. This counter can be read and written at the user's discretion. This feature is available only on the DS1688/91 and DS1689/93.

Additional Serial Number

An additional 64-bit customer specific serial number or ROM is located in bank 1 registers 60h through 67h. This feature is available only on the DS1688/91 and DS1689/93.

Burst Mode

The DS17285/87, DS17485/87, and DS17885/87 are the only devices which provide the burst mode option. The model byte uniquely identifies these devices as having burst mode.

REGISTER DESCRIPTION

LOCATION	DESCRIPTION
0Ah	Control Register A
Bit 7	Update In Progress (UIP) – (read only) 0=time/date can be read 1=update in progress
Bits 6 – 4	Oscillator Control (DV2-DV0) DV2=countdown chain 0=countdown chain enabled 1=resets countdown chain only if DV1=1 DV1=oscillator enable 0=oscillator off 1=oscillator on DV0=bank select 0=original bank 1=extended registers
Bits 3 – 0	Rate Selection (RS3-RS0) These bits define the square wave output frequency and the periodic interrupt rate.

LOCATION	DESCRIPTION
0Bh	<p>Control Register B</p> <p>Bit 7 Halt Clock Updates (SET) 0=updates time/date once per second 1=time/date updates are inhibited</p> <p>Bit 6 Periodic Interrupt Enable (PIE) 0=disabled 1=enabled</p> <p>Bit 5 Alarm Interrupt Enable (AIE) 0=disabled 1=enabled</p> <p>Bit 4 Update-Ended Interrupt Enable (UIE) 0=disabled 1=enabled</p> <p>Bit 3 Square Wave Enable (SQWE) 0=disabled 1=enabled</p> <p>Bit 2 Time and Date Data Mode (DM) 0=binary coded decimal (BDC) format 1=binary format</p> <p>Bit 1 Hour Format (24/12) 0=12 hour mode 1= 24 hour mode</p> <p>Bit 0 Daylight Savings Time Enable (DSE) 0=disabled 1=enabled</p>
0Ch	<p>Status Register C (read only)</p> <p>Bit 7 Interrupt Request Flag (IRQF) – (read only)</p> <p>Bit 6 Periodic Interrupt (PF) – (read only)</p> <p>Bit 5 Alarm Interrupt Flag (AG) – (read only)</p> <p>Bit 4 Update-Ended Interrupt Flag (UF) – (read only)</p> <p>Bit 3 – 0 Reserved (read only logic 0)</p>

LOCATION	DESCRIPTION
0Dh	Status Register D (read only) Bit 7 Valid RAM and Time (VRT) – (read only) 0=battery low; CMOS RAM invalid 1=battery good; CMOS RAM valid Bit 6 – 0 Reserved (read only logic 0)
04Ah	Extended Control Register 4A Bit 7 Valid RAM and Time 2 (VRT2) – (read only) 0=auxiliary battery is low 1=auxiliary battery is good Bit 6 Increment in Progress (INCR) – (read only) 0=time/date has been updated 1=time/date is incrementing and checking alarms Bit 5 Burst Mode Enable (BME) – See Note 1 0=single-byte extended RAM reads and writes 1=auto-increments address for extended RAM reads and writes Bit 4 Reserved Bit 3 Power Active Bar (PAB) 0= $\overline{\text{PWR}}$ pin is in the active low state 1= $\overline{\text{PWR}}$ pin is in the inactive high state Bit 2 RAM Clear Flag (RF) 0=cleared state (must be written) 1=high to low transition detected on $\overline{\text{RCLR}}$ if RCE=1 Bit 1 Wakeup Alarm Flag (WF) 0=cleared state (must be written) 1=wakeup alarm condition has occurred Bit 0 Kickstart Flag (KF) 0=cleared state (must be written) 1=high to low transition detected on $\overline{\text{KS}}$ input

LOCATION	DESCRIPTION
04Bh	<p>Extended Control Register 4B</p> <p>Bit 7 Auxiliary Battery Enable (ABE) 0=auxiliary battery input not being used 1=auxiliary battery input used for extended features</p> <p>Bit 6 Enable 32 KHz (E32K) 0=32 KHz disabled 1=32 KHz enabled to be output on the SQW pin</p> <p>Bit 5 Crystal Selection (CS) – See Note 2 0=oscillator configured for a crystal with a load capacitance of 6 pF 1=oscillator configured for a crystal with a load capacitance of 12.5 pF</p> <p>Bit 4 RAM Clear Enable (RCE) 0=RAM clear function is disabled 1=allows $\overline{\text{RCLR}}$ pin to clear user RAM</p> <p>Bit 3 Power Active Bar Reset Select (PRS) – See Note 3 0=$\overline{\text{PWR}}$ pin will go High-Z when entering power fail 1=$\overline{\text{PWR}}$ pin remains active when entering power fail</p> <p>Bit 2 RAM Clear Interrupt Enable (RIE) 0=disabled 1=enables RAM clear function to generate interrupts</p> <p>Bit 1 Wakeup Alarm Interrupt Enable (WIE) 0=disabled 1=enables wakeup alarm to generate interrupts</p> <p>Bit 0 Kickstart Interrupt Enable (KSE) 0=disabled 1=enables $\overline{\text{KS}}$ to generate interrupts</p>

NOTES:

1. Burst Mode Enable (BME) is available only on the DS17285/87, DS17485/87, and DS17885/87 devices.
2. Crystal Selection (CS) is not available on the DS1585/87 or DS17A84/86 devices.
3. Power Active Bar Reset Select (PRS) is not available on the DS1585/87 or DS17A84/86 devices.

PC RTC INITIALIZATION PROCEDURE











