Application Note 362
Replacing the TDK 78P7200/2241 with the DS3150

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INTRODUCTION

The DS3150 is a full-featured Line Interface Unit (LIU) that performs all of the functions necessary for interfacing at the physical layer to T3, E3, and STS-1 lines. The DS3150 is pin compatible with the TDK 78P2241 and the 78P7200 devices.

The purpose of this application note is to illustrate how to replace the TDK devices in a design with the DS3150 and to use the advanced features of the DS3150 in that design.

This application note has two separate sections for general pin comparisons – one for the 78P2241 and one for the 78P7200. A single section for transmitter/receiver discrete component selection for both devices is included at the end of the document. As a general comment, the 78P2241 is a closer match to the DS3150 than the 78P7200 because the former device operates at 3.3 volt rather than 5 volt and because it supports more features.

REPLACING THE 78P2241 WITH THE DS3150

Replacing the TDK 78P2241 with the DS3150 is a simple task. If the goal is to mimic the operation of the TDK device without enabling the additional features of the DS3150, the DS3150 can be placed in the TDK footprint with no changes to the artwork.

When keeping the exact same layout, the most significant issue to keep in mind is that the TDK device derives its timing from the receiver via an internal PLL circuit. The DS3150, on the other hand, can be clocked from three different sources: 1) from an external master clock supplied to the MCLK pin; 2) from an externally supplied clock to the TCLK pin (if MCLK is tied high or left floating); or 3) from an internal oscillator (if MCLK is tied low). When trying to mimic the TDK operation, the second option is the most straightforward. To implement this second option, the PLL filter capacitor connected between the LF1 pin and ground in the TDK design should not be installed, allowing the MCLK pin to float. Also the resistor value placed between the RFO pin and ground should not be installed.

ADDITIONAL FEATURES OF THE DS3150

The DS3150 also provides several additional features compared to the 78P2241, including the following:

- Integrated $2^{15} - 1$ and $2^{23} - 1$ Pseudo Random Bit Sequence (PRBS) generator and detector:
- Jitter Attenuator that can be placed in receive or transmit path
- Complete T3 AIS generator according to ANSI T1.107
- Unframed all ones generator (E3 AIS)
- Unframed 101010… generation
- Excessive zeroes detection
- External master clock support for higher accuracy operation

Additional features on the DS3150 are enabled and controlled by redefining some of the no-connect and ground pins of the 78P2241 as active pins on the DS3150 and by adding a third “floating” state to some of the existing input pins. The pins that have changed are listed in Table 1.

DS3150 / TDK 78P2241 Pin Comparison Table 1

DS3150	78P2241	NOTES
DM* (Driver Monitor) This active low output is asserted when the driver monitor detects a problem with the transmit line driver. This signal is not bonded out in the PLCC package.	GND	Since DM* is open-drain, using the DS3150 in a 78P2241 application which has this pin tied low is no problem.
EFE (Enhanced Feature Enable) 0 = Enhanced features disabled 1 = Enhanced features enabled Float = Test mode enabled	GND	EFE affects the operation of TDS0, TDS1/OFSEL, PRBS and DM*. If EFE is set to 0, TDS0 and TDS1/ OFSEL are ignored and PRBS and DM* are tri-stated.
LOS* (Loss of Signal) This output is asserted upon detection of 192 consecutive zeros. Signals lower than 21 dB below nominal are squelched. LOS* is deasserted when there are no Excessive Zero occurrences over a span of 192 clock periods.	LOS* (Loss of Signal) Asserted when receiver signal is below the threshold level.	The LOS* monitors for low signal levels on the receiver for both devices. However, the DS3150 also monitors for excessive zeroes.
MCLK (Master Clock) If used, should be connected to a ±20 ppm clock source. If tied high, TCLK is used as the master clock. If tied low, an internal oscillator is enabled as the master clock. The frequency of the internal oscillator is set by a resistor between the OFSEL pin and ground.	LF1 (Rx PLL Filter Cap)	Master clock for DS3150 at rate of T3, E3, or STS-1. The LF1 connection is not needed on the DS3150.
PRBS (PRBS Detector) If EFE = 1, this output remains high when the PRBS detector is out of sync. When the PBRS detector is in sync, this pin remains low and pulses high for each bit error detected. If EFE = 0, this pin is tri-stated. This pin is not bonded out in the PLCC package.	GND	To use the DS3150 in a 78P2241 application where this pin is tied low, EFE must also be tied low to tri-state the PRBS output driver.

DS3150 / TDK 78P2241 Pin Comparison Table 1 (cont.)

DS3150	78P2241	NOTES
RMON (Receive Monitor Mode) 0 = Disable 20 dB gain stage and disable Rx Jitter Attenuator 1 = Enable 20 dB gain stage and disable Rx Jitter Attenuator float = disable 20 dB gain stage and enable Rx Jitter Attenuator	MON (Monitor Select) 0 = Disable 20 dB gain stage 1 = Enable 20 dB gain stage	RMON emulates the MON pin but also adds a floating state which enables the Rx Jitter Attenuator
TDS0 (Tx Data Select Bit 0)	GND	If EFE = 1, These TDS0/1 pins select the source of the transmit data (see Table 2). If MCLK is tied low, TDS1 is internally pulled low. If EFE=0, these signals are ignored.
TDS1/OFSEL (Tx Data Select Bit 1 / Oscillator Frequency Select) If MCLK is tied low, a resistor connected between this pin (OFSEL) and ground determines the frequency of an internal oscillator as shown below: E3: 5.11 kΩ T3: 3.83 kΩ STS1: 3.24 kΩ	RFO resistor to GND sets oscillator speed	
TTS* (Transmit Tri-state Output Driver) 0 = Tri-state Tx driver and disable Tx Jitter Attenuator 1= Enable Tx driver and disable Tx Jitter Attenuator Float = Enable Tx driver and Tx Jitter Attenuator	TXEN (Transmitter Enable) 0 = Tri-state Tx driver 1 = Enable Tx driver	TTS* behaves like the TXEN pin but also adds the floating state to enable the Tx Jitter Attenuator
ZCSE* (Zero Code Suppression Enable) 0 = B3ZS/HDB3 encoder/decoder enabled 1 = B3ZS/HDB3 encoder/decoder disabled	ENDEC* 0 = enabled 1 = disabled	ZCSE* emulates the ENDEC pin but also adds a floating state to enable factory test mode

TRANSMIT DATA MODE SELECT PIN DESCRIPTIONS Table 2

TDS1	TDS0	TESS	Transmit Mode Selected
0	0	X	Transmit data normally as input at TPOS and TNEG
0	1	X	Transmit Unframed All Ones
1	0	0 or float	Transmit an Unframed 101010… pattern
1	0	1	Transmit T3 AIS as per ANSI T1.107
1	1	0	Transmit a $2^{23} – 1$ PRBS pattern as per ITU O.151
1	1	1 or float	Transmit a $2^{15} – 1$ PRBS pattern as per ITU O.151

NOTES:

1. TESS = 0 for E3; TESS = 1 for T3; TESS = float for STS-1
2. TDS0 and TDS0 are ignored when EFE is tied low and the device will transmit TPOS / TNEG data.

REPLACING THE 78P7200 WITH THE DS3150

Replacing the TDK 78P7200 with the DS3150 is a simple task. If the goal is to mimic the operation of the TDK device without enabling the additional features of the DS3150, the DS3150 can be placed in the TDK footprint with no changes or minimal changes to the artwork.

When keeping the exact same layout, the most significant issue to keep in mind is that the TDK device derives its timing from the receiver via an internal PLL circuit. The DS3150, on the other hand, can be clocked from three different sources: 1) from an external master clock supplied to the MCLK pin; 2) from an externally supplied clock to the TCLK pin (if MCLK is tied high or left floating); or 3) from an internal oscillator (if MCLK is tied low). When trying to mimic the TDK operation, the second option is the most straightforward. To implement this second option, the PLL filter capacitor connected between the LF1 pin and ground in the TDK design should not be installed, allowing the MCLK pin to float. Also the resistor value placed between the RFO pin and ground should not be installed.

One additional modification should be made as well. The CPD pin for the TDK device is used to place a decoupling capacitor between the peak detector node and Vcc. For the DS3150, this pin (LPBK*) is used to enable/disable the internal loopback functionality. For an existing TDK design, the capacitor should be replaced with a zero ohm resistor, which will disable loopback functionality on the DS3150.

ADDITIONAL FEATURES OF THE DS3150

The DS3150 also provides several additional features compared to the 78P7200, including the following:

- Jitter Attenuator that can be placed in receive or transmit path
- Complete T3 AIS generator according to ANSI T1.107
- Unframed all ones generator (E3 AIS)
- Unframed 101010… generation
- Excessive zeroes detection
- External master clock support for higher accuracy operation
- NRZ support (available on 78P2241, but not on 78P7200)
- 3.3V operation (78P2241 is a 3.3V device, but 78P7200 is a 5V device)
- Loopback support (available on 78P2241, but not on 78P7200)

Additional features on the DS3150 are enabled and controlled by redefining some of the no-connect and ground pins of the 78P7200 as active pins on the DS3150 and by adding a third “floating” state to some of the existing input pins. The pins that have changed are listed in Table 3.

DS3150 / TDK 78P7200 Pin Comparison Table 3

DS3150	78P7200	NOTES
EFE (Enhanced Feature Enable) 0 = Enhanced features disabled 1 = Enhanced features enabled Float = Test mode enabled	GND	EFE affects the operation of TDS0, TDS1/OFSEL, PRBS and DM*. If EFE is set to 0, TDS0 and TDS1/OFSEL are ignored and PRBS and DM are tri-stated.
ICE (Invert Clock Enable) 0 = Normal RCLK/TCLK operation 1 = Normal RCLK, Inverted TCLK float = Inverted RCLK, Inverted TCLK	NCT – tied to ground	ICE supports clock inversion for RCLK and TCLK.
LOS* (Loss of Signal) This output is asserted upon detection of 192 consecutive zeros. Signals lower than 21 dB below nominal are squelched. LOS* is deasserted when there are no Excessive Zero occurrences over a span of 192 clock periods.	LOS* (Loss of Signal) Asserted when receiver signal is below the threshold level.	The LOS* monitors for low signal levels on the receiver for both devices. However, the DS3150 also monitors for excessive zeroes.
LPBK* (Loopback Select) 0 = Analog loopback enabled 1 = No loopback enabled Float = Digital loopback enabled	CPD – capacitor to RVcc to reduce signal dependent ripple	The DS3150 does not require a capacitor on this node. Instead the pin is used to support loopback operation.
MCLK (Master Clock) If used, should be connected to a ±20 ppm clock source. If tied high, TCLK is used as the master clock. If tied low, an internal oscillator is enabled as the master clock. The frequency of the internal oscillator is set by a resistor between the OFSEL pin and ground.	LF1 (RC loop filter network for PLL)	Master clock for DS3150 at rate of T3, E3, or STS-1. RC network not necessary for DS3150.
RMON (Receive Monitor Mode) 0 = Disable 20 dB gain stage and disable Rx Jitter Attenuator 1 = Enable 20 dB gain stage and disable Rx Jitter Attenuator float = disable 20 dB gain stage and enable Rx Jitter Attenuator	MON (Monitor Select) 0 = Disable 20 dB gain stage 1 = Enable 20 dB gain stage	RMON emulates the MON pin but also adds a floating state which enables the Rx Jitter Attenuator
RPOS/RNRZ	RPOS	The 78P7200 does not support NRZ operation

DS3150 / TDK 78P7200 Pin Comparison Table 3 (cont.)

DS3150	78P7200	NOTES
TDS0 (Tx Data Select Bit 0)	NCR – tied to ground	If EFE = 1, These TDS0/1 pins select the source of the transmit data (see Table 2). If MCLK is tied low, TDS1 is internally pulled low. If EFE=0, these signals are ignored.
TDS1/OFSEL (Tx Data Select Bit 1 / Oscillator Frequency Select) If MCLK is tied low, a resistor connected between this pin (OFSEL) and ground determines the frequency of an internal oscillator as shown below: E3: 5.11 kΩ T3: 3.83 kΩ STS1: 3.24 kΩ	RFO resistor to GND sets oscillator speed	
TESS (T3/E3/STS-1 Select) 0 = E3 1 = T3 Float = STS-1	OPT1 – Transmit Option 1 0 = E3 operation 1 = T3 or STS-1 operation	The only difference in operation is for STS-1 selection
TPOS/TNRZ	TPOS	The 78P7200 does not support NRZ operation
TTS* (Transmit Tri-state Output Driver) 0 = Tri-state Tx driver and disable Tx Jitter Attenuator 1= Enable Tx driver and disable Tx Jitter Attenuator Float = Enable Tx driver and Tx Jitter Attenuator	OPT2 (Transmit Option 2) 0 = Tri-state Tx drivers 1 = Enable Tx drivers	TTS* behaves like the OPT2 pin but also adds the floating state to enable the Tx Jitter Attenuator
ZCSE* (Zero Code Suppression Enable) 0 = B3ZS/HDB3 encoder/decoder enabled 1 = B3ZS/HDB3 encoder/decoder disabled	LF2 (RC loop filter network for PLL)	RC network not necessary for DS3150.

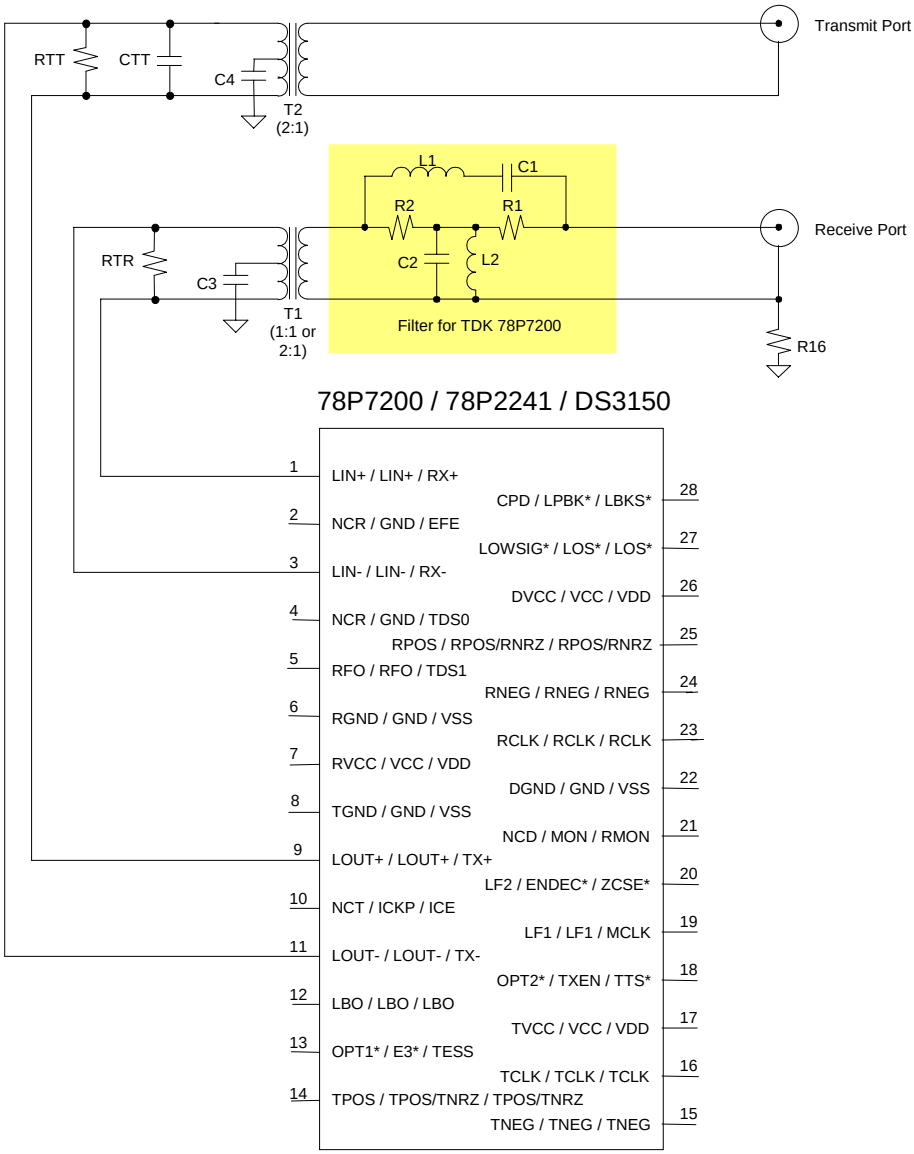
FRONT END COMPONENT CONSIDERATIONS

When replacing the TDK 78P7200 or 78P2241 with the DS3150, some attention should be paid to the discrete components selected for the receiver and transmitter. Figure 1 illustrates TDK's recommended design. The DS3150 can be used in this configuration. However, for best results the following alterations are suggested:

- Remove CTT
- Change C3 and C4 to 0.05 µF
- Change RTR and RTT to 330Ω ±1%
- T1 should be a 1:2 transformer

Also note that the filter circuit required for the 78P7200 is not required for the DS3150. Table 4 lists the recommended values for the discrete components for the different LIUs.

Line Interface Unit Schematic: Figure 1



COMPONENT SELECTION Table 4

Component	DS3150	78P7200	78P2241
R1	short, 0Ω	75Ω	short, 0Ω
R2	short, 0Ω	75Ω	short, 0Ω
RTR	330Ω	422Ω	75Ω
RTT	330Ω	301Ω (T3, STS-1) 604 (E3)	301Ω
C1	not installed	1000 pF	not installed
C2	not installed	82 pF	not installed
C3	0.05 µF	0.01 µF	not installed
C4	0.05 µF	0.1 µF	0.1 µF
CTT	not installed	10 pF (T3, STS-1) 3 pF (E3)	not installed
L1	not installed	0.47 µH	not installed
L2	not installed	6.8 µH	not installed
T1	1:2	1:2	1:1
T2	1:2	1:2	1:2