



Application Note 2

The DS87C550 as an Upgrade for 8051 Derivatives

INTRODUCTION

The DS87C550 High-Speed Microcontroller with A/D and PWM was designed to be highly compatible with many 8051 derivatives. It was designed with the same pinout and basic resources as the 87C552, but has significantly enhanced performance capabilities and a number of additional resources. Since the instruction set and pinout are the same, many situations allow it to be used as a drop-in replacement for that device. When doing so however, there are some issues that must be taken into account. This application note discusses those issues.

PROCESSOR SPEED

While the DS87C550 is 100 percent compatible with the 8051 instruction set, the execution of the instructions has been streamlined for increased performance. A single byte instruction that previously required 12 clocks to complete now executes in 4 clocks. In addition, the DS87C550 can accept clock speeds up to 33 MHz where in some versions of the 8032 the maximum was 12 MHz. Because of this higher performance, there are speed-related issues that must be considered when evaluating the DS87C550 as a replacement for traditional 8051 microcontrollers.

Memory Interface Timing

The reduced instruction execution time of the DS87C550 can, for the same frequency crystal, result in faster external memory access times. For example, the data sheet for the 8032 stipulates that, when using a 12 MHz crystal, the program memory must have an address access time of 302 ns or less (neglecting any address latch overhead). A DS87C550 also using a 12 MHz crystal requires a memory with an address access time of 230 ns or less. Since most available memories today offer much faster access times, this is not likely to be an important design consideration.

Software Loops

Another speed-related issue is the use of software timing. It is frequently the case that software writers will use the presumed constant execution speed of a processor as a real time reference. Often a tight loop that requires a known number of clocks to execute will be used for generating delays. Since the DS87C550 executes instructions much more quickly than the standard 8032, these previously designed timing loops will no longer produce the originally intended results. While the use of software timing loops is generally discouraged, in practice they are used rather frequently in embedded applications. The DS87C550 was designed so that the internal timers default to a condition where they behave exactly as the timers in the 8032. If application code is written to make use of these timers rather than software delays, the code will run as originally intended.

INTERRUPTS

The accommodation of the expanded features of the High-Speed Microcontroller Family required a slight reorganization of the interrupt vector address map compared with other 8051 derivatives as shown in the following table.

Interrupt Name	Interrupt Description	Vector Addresses		
		DS87C550	87C552	DS80C320
$\overline{\text{INT0}}$	External Interrupt 0	03h	03h	03h
SCON1	Serial Port 1	0Bh	-	3Bh
A/D	A/D Converter	13h	53h	-
TF0	Timer 0	1Bh	0Bh	0Bh
INT2/CF0	External Interrupt 2 or Capture 0	23h	33h	43h
CM0F	Compare Match 0	2Bh	5Bh	-
PFI	Power Fail Interrupt	33h	-	33h
$\overline{\text{INT1}}$	External Interrupt 1	3Bh	13h	13h
$\overline{\text{INT3}}/\text{CF1}$	External Interrupt 3 or Capture 1	43h	-	4Bh
CM1F	Compare Match 1	4Bh	63h	-
TF1	Timer 1	53h	1Bh	1Bh
INT4/CF2	External Interrupt 2 or Capture 2	5Bh	-	53h
CM2F	Compare Match 2	63h	6Bh	-
SCON0	Serial port 0	6Bh	23h	23h
$\overline{\text{INT5}}/\text{CF3}$	External Interrupt 5 or Capture 3	73h	-	5Bh
TF2	Timer 2	7Bh	73h	2Bh

POWER-ON / POWER-FAIL RESET

The DS87C550 incorporates circuitry to generate its own power-on reset function. This eliminates the cost and board-space associated with an external component. While the RST pin may still be connected to an external reset generating circuit, this internal feature allows the option of removing the external component as a cost reduction. Although these features are designed to be transparent if not needed, there are a few situations where the internal power-fail reset feature could interact with an existing design in undesired ways. One such instance might be if the design requires the reset voltage to be at a specific point or exist for specific duration. Another case might be where battery backed RAM is relied upon for data storage. If the RAM contains its own voltage detection circuitry and does not become unprotected at the same voltage as the DS87C550 leaves reset (4.0 volts), then the processor could erroneously access protected RAM. While these cases are not common, they remain something to consider for each specific application.

POWER CONSUMPTION

In addition to being a higher performance device, the DS87C550 is also a lower power device than the 8032 when equivalent work is considered. All CMOS parts exhibit the property that they consume more power as their speed goes up. Since the DS87C550 is a higher performance part, it will consume more power for a given crystal frequency. However, if an equivalent amount of work is considered, it consumes slightly less power than a conventional 8032. This difference in power consumption is probably only

important for battery powered applications, in which case Stop mode power is likely to be an important consideration.

SPECIAL FUNCTION REGISTER CHANGES

The Special Function Register (SFR) map of the DS87C550 differs slightly from other members of the 8051 family to accommodate the new feature set. The following table highlights DS87C550 SFR locations with different functions on either the 87C552 or DS80C320/8051. The use assembler/compiler header files specifically designed for the DS87C550 will remove any confusion when porting software from other members of the 8051 family.

Address	DS87C550	87C552	DS80C320	Notes
86h	DPS	-	DPS	DS87C550 has new bits.
87h	PCON	PCON	PCON	DS87C550 has new bits.
90h	P1	P1	P1	DS87C550 alternate pin functions changed
91h	RCON	-	EXIF	
9Fh	PMR	-	-	
A1h	SADDR0	-	-	
A2h	SADDR1	-	-	
A9h	CMPL0	CML0	SADDR0	
AAh	CMPL1	CML1	SADDR1	
B8h	IP	IP0	IP	DS87C550 adds PAD bit
BEh	T2CON	-	-	
BFh	T2MOD	-	-	
C0h	P4	-	SCON1	
C1h	-	-	SBUF1	
C4h	P5	P5	PMR	
C8h	T2IR	TM2IR	T2CON	
C9h	CMPH0	CMH0	T2MOD	
CAh	CMPH1	CMH1	RCAP2L	
CBh	CMPH2	CMH2	RCAP2H	
CCh	CPTH0	CTH0	TL2	
CDh	CPTH1	CTH1	TH2	
D8h	SCON1	S1CON	WDCON	
D9h	SBUF1	S1STA	-	
ECh	TL2	TML2	-	
EDh	TH2	TMH2	-	
FFh	WDCON	T3	-	