DALLAS SEMICONDUCTOR

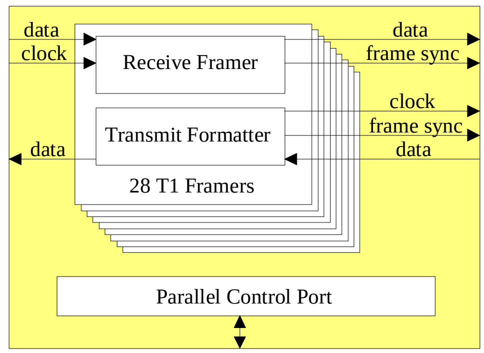
DS3120
28 Channel T1 Framer

www.dalsemi.com

FEATURES

- 28 T1 DS1/ISDN–PRI/J1 framing transceivers
- All 28 framers are fully independent
- Directly supports loop timing & external timing
- Supports H.100 / MVIP 8 MHz backplanes
- Frames to D4, ESF, & SLC-96
- Transparent framing mode
- Frame bit clock gapping option
- Hardware based signaling option
- Fully independent transmit and receive functionality
- Integral HDLC controller with 64-byte buffers; configurable for FDL or DS0 operation
- Generates and detects in–band loop codes from 1 to 8 bits in length
- DS0 monitor capability
- Per DS0 channel loopback
- Software compatible with other Dallas Semiconductor T1 framers
- 1.8V core supply with 5V tolerant I/O; low power .18 um CMOS
- 27 mm x 27 mm, 316 lead 1.27 mm pitch PBGA package
- IEEE 1149.1 support

FUNCTIONAL DIAGRAM



PIN DESCRIPTION

DS3120 - (0^0 C to 70^0 C)
DS3120N - (-40^0 C to $+85^0$ C)

DESCRIPTION

The DS3120 is a highly dense version of Dallas Semiconductor's popular T1 framer series. It shares the same register structure as the DS2151, DS2152, DS21352, DS21552, DS21Q352, DS21Q552, DS2141A, DS21Q41B, DS21Q42, DS21FT42, and DS21FF42. The DS3120 contains 28 fully independent framers that are configured and read through a common microprocessor compatible parallel port. The device fully meets all of the latest T1 specifications including ANSI T1.403–1999, ANSI T1.231–1993, AT&T TR 62411 (12–90), AT&T TR54016, and ITU G.704 and G.706.

1. INTRODUCTION

The DS3120 is a highly dense version of the other popular Dallas Semiconductor T1 framers. Due to high density of framers and since the DS3120 is intended to be used primarily in channelized T3 applications, a number of features that are found on Dallas Semiconductor's other T1 framers are not available in the DS3120. These missing features are listed in Table 1-1 below. Please see the separate Application Note for a more complete discussion of missing features and the differences between the DS3120 and other Dallas Semiconductor framers. A list of the main features in the DS3120 is detailed in Table 1-2.

Features Not Available in DS3120 Table 1-1

- No bipolar interface
- No receive side signaling re-insertion function
- Limited elastic store functionality
- Missing signals include RCHBLK, TCHBLK, RCHCLK, TCHCLK, TLINK, TLCLK, RLINK, RLCLK, RMSYNC, RFSYNC, RLOS/LOTC, and FMS

DS3120 Main Features List Table 1-2

- 28 T1 DS1/ISDN–PRI/J1 framing transceivers
- All 28 framers are fully independent
- Frames to D4, ESF, and SLC–96 formats
- Framing transparent mode
- Can operate in both loop timing and external timing (common transmit clock) configurations
- Framing bit clock gapping mode supported
- Supports H.100 / MVIP 8 MHz interfaces
- 8–bit parallel control port supports both multiplexed & non–multiplexed buses (Intel or Motorola)
- Extracts and inserts robbed bit signaling via either software (processor based) or hardware signals
- Signaling freezing
- Interrupt generated on change of signaling data
- Detects and generates yellow (RAI) and blue (AIS) alarms
- Detects carrier loss (RCL), AIS-CI, and loss of sync (RLOS)
- Fully independent transmit and receive functionality
- Generates and detects in–band loop codes from 1 to 8 bits in length including CSU loop codes
- Contains ANSI one's density monitor and enforcer
- Large path and line error counters including EXZ, CRC6, and framing bit errors
- HDLC controller with 64–byte buffers in both transmit and receive paths; configurable for FDL or DS0 access
- Per–channel code insertion in both transmit and receive paths
- Ability to monitor one DS0 channel in both the transmit and receive paths
- 1.544 MHz to 8.192 MHz clock synthesizer
- Per–channel loopback

- Ability to calculate and check CRC6 according to the Japanese standard
- Ability to pass the F–Bit position through the elastic stores in the H.100 / MVIP 8 MHz backplane mode
- IEEE 1149.1 support
- 1.8V & 3.3V supply with 5V tolerant I/O; low power CMOS

Reader's Note: This data sheet assumes a particular nomenclature of the T1 operating environment. In each 125 us frame, there are 24 8–bit channels plus a framing bit. It is assumed that the framing bit is sent first followed by channel 1. Each channel is made up of 8 bits which are numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. Throughout this data sheet, the following abbreviations will be used:

D4	Superframe (12 frames per multiframe) Multiframe Structure
SLC–96	Subscriber Loop Carrier – 96 Channels (SLC–96 is an AT&T registered trademark)
ESF	Extended Superframe (24 frames per multiframe) Multiframe Structure
B8ZS	Bipolar with 8 Zero Substitution
CRC	Cyclical Redundancy Check
Ft	Terminal Framing Pattern in D4
Fs	Signaling Framing Pattern in D4
FPS	Framing Pattern in ESF
MF	Multiframe
BOC	Bit Oriented Code
HDLC	High Level Data Link Control
FDL	Facility Data Link

DOCUMENT REVISION HISTORY

Revision	Notes
V1 07-15-99	Initial Release.
V2 09-22-99	1. Added mechanical specifications (Section 22). 2. Added signal/lead assignment (Section 2). 3. Swapped the signal order of the RNRZ12 and VDD_CORE signals (Section 2). 4. Swapped the signal order of the VDD_CORE and TCLK22/RSIG22 signals (Section 2). 5. Removed the TCLK11/RSIG11 signal duplication with TSYNC11/TSIG11 signal (Section 2). 6. Added JTAG boundary scan control bit description (Table 19-2). 7. Added tD2 timing parameter to 8 MHz IBO timing specifications (Figure 21-9). 8. Added special test mode that is invoked via the TEST and FIACT* signals (Section 2).
V3 02-16-00	1. Fixed errors in Table 18-2 (8 MHz IBO Channel Assignment)

DS3120 28 CHANNEL T1 FRAMER Figure 1-1

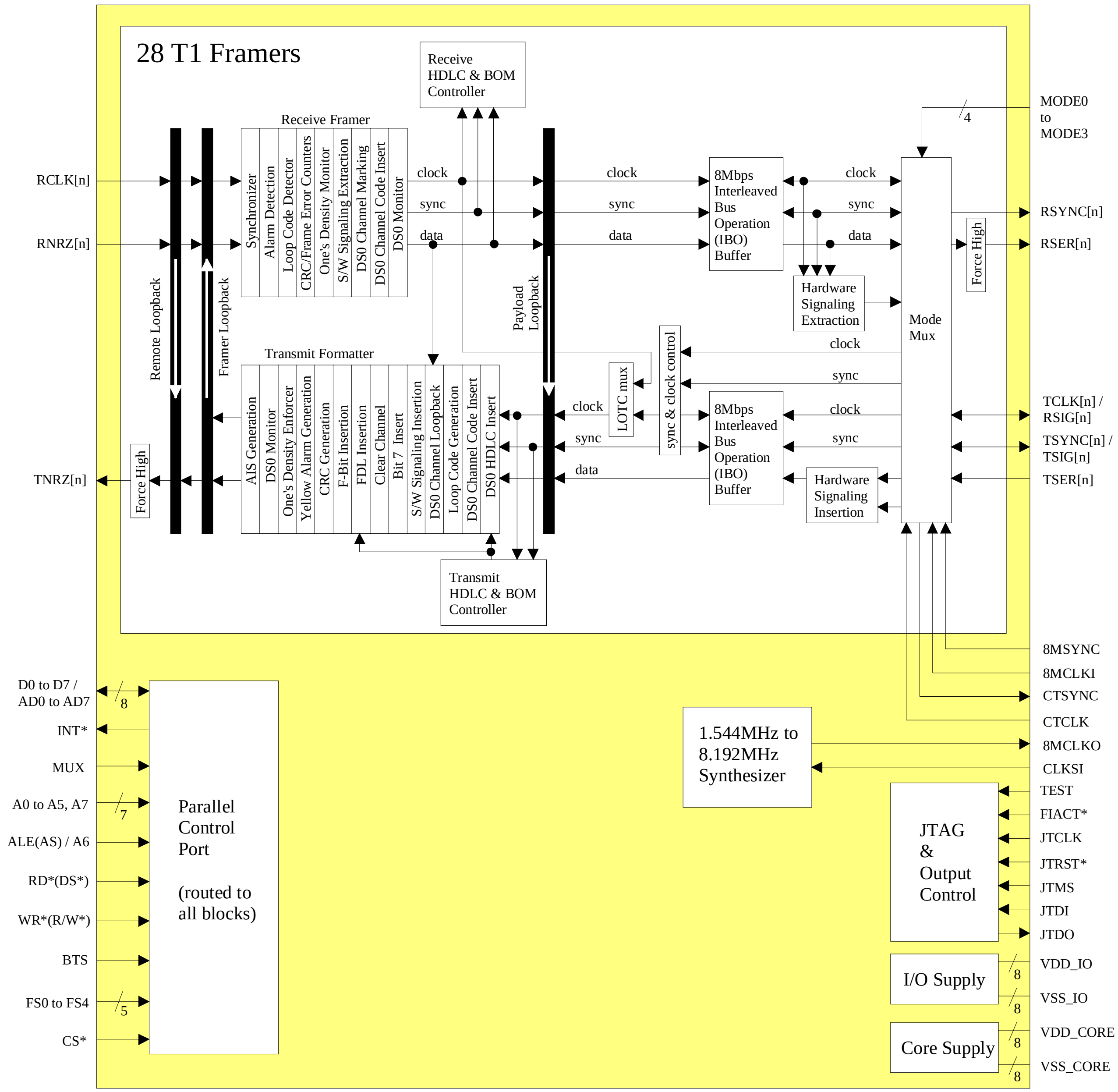


TABLE OF CONTENTS

2. DS3120 SIGNAL DESCRIPTION

Signal Description / Lead List (Sorted by Signal Name) Table 2-1

LEAD	SIGNAL	TYPE	SIGNAL DESCRIPTION
C11	8MCLKI	I	8 MHz Interleaved Bus Operation (IBO) Clock Input.
C12	8MCLKO	O	8 MHz Clock Synthesizer Output.
E11	8MSYNC	I	8 MHz Interleaved Bus Operation (IBO) Sync Input.
A8	A0	I	Address Bus Bit 0; LSB.
B8	A1	I	Address Bus Bit 1.
A7	A2	I	Address Bus Bit 2.
C8	A3	I	Address Bus Bit 3.
E8	A4	I	Address Bus Bit 4.
D8	A5	I	Address Bus Bit 5.
A6	A6/ALE (AS)	I	Address Bus Bit 6 / Address Latch Enable (Address Strobe).
B7	A7	I	Address Bus Bit 7; MSB.
B11	BTS	I	Bus Type Select for Parallel Control Port
B12	CLKSI	I	8MCLK Clock Reference Input .
B5	CS*	I	Chip Select. Active low.
A12	CTCLK	I	Common Transmit T1 Clock.
D11	CTSYNC	O	Common Transmit 8 kHz Frame Sync Pulse.
D10	D0 or AD0	I/O	Data Bus Bit or Address/Data Bit 0; LSB.
C10	D1 or AD1	I/O	Data Bus Bit or Address/Data Bit 1.
A9	D2 or AD2	I/O	Data Bus Bit or Address/Data Bit 2.
B9	D3 or AD3	I/O	Data Bus Bit or Address/Data Bit 3.
C9	D4 or AD4	I/O	Data Bus Bit or Address/Data Bit 4.
E10	D5 or AD5	I/O	Data Bus Bit or Address/Data Bit 5.
E9	D6 or AD6	I/O	Data Bus Bit or Address/Data Bit 6.
D9	D7 or AD7	I/O	Data Bus Bit or Address/Data Bit 7; MSB.
A3	FIACT*	I	Force Inactive. Active low.
C7	FS0	I	Framer Select 0 for Parallel Control Port; LSB.
E7	FS1	I	Framer Select 1 for Parallel Control Port.
D7	FS2	I	Framer Select 2 for Parallel Control Port.
B6	FS3	I	Framer Select 3 for Parallel Control Port.
A4	FS4	I	Framer Select 4 for Parallel Control Port; MSB.
B10	INT*	O (od)	Receive Alarm Interrupt for all 28 Framers. Active low.
A2	JTCLK	I	JTAG Test Clock.
C5	JTDI	I	JTAG Test Data Input.
D5	JTDO	O	JTAG Test Data Output.
B4	JTMS	I	JTAG Test Mode Select.
A1	JTRST*	I	JTAG Reset. Active low.
C2	MODE0	I	Mode Select Bit 0.
E4	MODE1	I	Mode Select Bit 1.
E3	MODE2	I	Mode Select Bit 2.

LEAD	SIGNAL	TYPE	SIGNAL DESCRIPTION
D2	MODE3	I	Mode Select Bit 3.
C6	MUX	I	Non-Multiplexed or Multiplexed Bus Select.
D3	NC	-	No Connect. Do not connect any signal to this lead.
W3	NC	-	No Connect. Do not connect any signal to this lead.
V4	NC	-	No Connect. Do not connect any signal to this lead.
U4	NC	-	No Connect. Do not connect any signal to this lead.
T5	NC	-	No Connect. Do not connect any signal to this lead.
D18	NC	-	No Connect. Do not connect any signal to this lead.
E16	NC	-	No Connect. Do not connect any signal to this lead.
D17	NC	-	No Connect. Do not connect any signal to this lead.
C18	NC	-	No Connect. Do not connect any signal to this lead.
B3	NC	-	No Connect. Do not connect any signal to this lead.
B2	NC	-	No Connect. Do not connect any signal to this lead.
C4	NC	-	No Connect. Do not connect any signal to this lead.
C3	NC	-	No Connect. Do not connect any signal to this lead.
B1	NC	-	No Connect. Do not connect any signal to this lead.
D4	NC	-	No Connect. Do not connect any signal to this lead.
E5	NC	-	No Connect. Do not connect any signal to this lead.
Y7	RCLK1	I	Receive Clock for Framer 1.
T8	RCLK2	I	Receive Clock for Framer 2.
Y5	RCLK3	I	Receive Clock for Framer 3.
U7	RCLK4	I	Receive Clock for Framer 4.
V6	RCLK5	I	Receive Clock for Framer 5.
Y3	RCLK6	I	Receive Clock for Framer 6.
V5	RCLK7	I	Receive Clock for Framer 7.
U3	RCLK8	I	Receive Clock for Framer 8.
V2	RCLK9	I	Receive Clock for Framer 9.
R4	RCLK10	I	Receive Clock for Framer 10.
V1	RCLK11	I	Receive Clock for Framer 11.
P4	RCLK12	I	Receive Clock for Framer 12.
P3	RCLK13	I	Receive Clock for Framer 13.
N5	RCLK14	I	Receive Clock for Framer 14.
N3	RCLK15	I	Receive Clock for Framer 15.
M5	RCLK16	I	Receive Clock for Framer 16.
N1	RCLK17	I	Receive Clock for Framer 17.
L4	RCLK18	I	Receive Clock for Framer 18.
M1	RCLK19	I	Receive Clock for Framer 19.
K5	RCLK20	I	Receive Clock for Framer 20.
K1	RCLK21	I	Receive Clock for Framer 21.
J5	RCLK22	I	Receive Clock for Framer 22.
H2	RCLK23	I	Receive Clock for Framer 23.
H5	RCLK24	I	Receive Clock for Framer 24.
F1	RCLK25	I	Receive Clock for Framer 25.
G4	RCLK26	I	Receive Clock for Framer 26.

LEAD	SIGNAL	TYPE	SIGNAL DESCRIPTION
D1	RCLK27	I	Receive Clock for Framer 27.
F3	RCLK28	I	Receive Clock for Framer 28.
A10	RD*/(DS*)	I	Read Input (Data Strobe). Active low.
V8	RNRZ1	I	Receive NRZ Data for Framer 1.
U8	RNRZ2	I	Receive NRZ Data for Framer 2.
V7	RNRZ3	I	Receive NRZ Data for Framer 3.
Y4	RNRZ4	I	Receive NRZ Data for Framer 4.
T7	RNRZ5	I	Receive NRZ Data for Framer 5.
Y2	RNRZ6	I	Receive NRZ Data for Framer 6.
U5	RNRZ7	I	Receive NRZ Data for Framer 7.
T4	RNRZ8	I	Receive NRZ Data for Framer 8.
T3	RNRZ9	I	Receive NRZ Data for Framer 9.
Y1	RNRZ10	I	Receive NRZ Data for Framer 10.
R3	RNRZ11	I	Receive NRZ Data for Framer 11.
P5	RNRZ12	I	Receive NRZ Data for Framer 12.
T1	RNRZ13	I	Receive NRZ Data for Framer 13.
P2	RNRZ14	I	Receive NRZ Data for Framer 14.
P1	RNRZ15	I	Receive NRZ Data for Framer 15.
N2	RNRZ16	I	Receive NRZ Data for Framer 16.
M2	RNRZ17	I	Receive NRZ Data for Framer 17.
L3	RNRZ18	I	Receive NRZ Data for Framer 18.
L1	RNRZ19	I	Receive NRZ Data for Framer 19.
K4	RNRZ20	I	Receive NRZ Data for Framer 20.
J1	RNRZ21	I	Receive NRZ Data for Framer 21.
J4	RNRZ22	I	Receive NRZ Data for Framer 22.
G1	RNRZ23	I	Receive NRZ Data for Framer 23.
H4	RNRZ24	I	Receive NRZ Data for Framer 24.
E1	RNRZ25	I	Receive NRZ Data for Framer 25.
G5	RNRZ26	I	Receive NRZ Data for Framer 26.
E2	RNRZ27	I	Receive NRZ Data for Framer 27.
C1	RNRZ28	I	Receive NRZ Data for Framer 28.
B13	RSER1	O	Receive Serial Data from Framer 1.
D13	RSER2	O	Receive Serial Data from Framer 2.
D14	RSER3	O	Receive Serial Data from Framer 3.
E14	RSER4	O	Receive Serial Data from Framer 4.
D16	RSER5	O	Receive Serial Data from Framer 5.
E17	RSER6	O	Receive Serial Data from Framer 6.
C20	RSER7	O	Receive Serial Data from Framer 7.
G17	RSER8	O	Receive Serial Data from Framer 8.
H17	RSER9	O	Receive Serial Data from Framer 9.
H20	RSER10	O	Receive Serial Data from Framer 10.
J19	RSER11	O	Receive Serial Data from Framer 11.
K20	RSER12	O	Receive Serial Data from Framer 12.
L17	RSER13	O	Receive Serial Data from Framer 13.

LEAD	SIGNAL	TYPE	SIGNAL DESCRIPTION
M17	RSER14	O	Receive Serial Data from Framer 14.
N16	RSER15	O	Receive Serial Data from Framer 15.
R19	RSER16	O	Receive Serial Data from Framer 16.
P16	RSER17	O	Receive Serial Data from Framer 17.
T18	RSER18	O	Receive Serial Data from Framer 18.
V18	RSER19	O	Receive Serial Data from Framer 19.
W18	RSER20	O	Receive Serial Data from Framer 20.
Y19	RSER21	O	Receive Serial Data from Framer 21.
T14	RSER22	O	Receive Serial Data from Framer 22.
U13	RSER23	O	Receive Serial Data from Framer 23.
W13	RSER24	O	Receive Serial Data from Framer 24.
Y13	RSER25	O	Receive Serial Data from Framer 25.
W11	RSER26	O	Receive Serial Data from Framer 26.
U10	RSER27	O	Receive Serial Data from Framer 27.
T9	RSER28	O	Receive Serial Data from Framer 28.
A14	RSYNC1	O	Receive Sync from Framer 1.
A16	RSYNC2	O	Receive Sync from Framer 2.
B16	RSYNC3	O	Receive Sync from Framer 3.
A19	RSYNC4	O	Receive Sync from Framer 4.
B18	RSYNC5	O	Receive Sync from Framer 5.
E18	RSYNC6	O	Receive Sync from Framer 6.
F18	RSYNC7	O	Receive Sync from Framer 7.
G16	RSYNC8	O	Receive Sync from Framer 8.
H16	RSYNC9	O	Receive Sync from Framer 9.
J17	RSYNC10	O	Receive Sync from Framer 10.
J20	RSYNC11	O	Receive Sync from Framer 11.
L20	RSYNC12	O	Receive Sync from Framer 12.
M20	RSYNC13	O	Receive Sync from Framer 13.
N20	RSYNC14	O	Receive Sync from Framer 14.
N17	RSYNC15	O	Receive Sync from Framer 15.
P17	RSYNC16	O	Receive Sync from Framer 16.
R17	RSYNC17	O	Receive Sync from Framer 17.
T17	RSYNC18	O	Receive Sync from Framer 18.
T16	RSYNC19	O	Receive Sync from Framer 19.
V16	RSYNC20	O	Receive Sync from Framer 20.
Y18	RSYNC21	O	Receive Sync from Framer 21.
V14	RSYNC22	O	Receive Sync from Framer 22.
T13	RSYNC23	O	Receive Sync from Framer 23.
U12	RSYNC24	O	Receive Sync from Framer 24.
W12	RSYNC25	O	Receive Sync from Framer 25.
Y11	RSYNC26	O	Receive Sync from Framer 26.
V10	RSYNC27	O	Receive Sync from Framer 27.
U9	RSYNC28	O	Receive Sync from Framer 28.
D12	TCLK1/RSIG1	I/O	Transmit Clock / Receive Signaling for/from Framer 1.

LEAD	SIGNAL	TYPE	SIGNAL DESCRIPTION
E13	TCLK2/RSIG2	I/O	Transmit Clock / Receive Signaling for/from Framer 2.
A17	TCLK3/RSIG3	I/O	Transmit Clock / Receive Signaling for/from Framer 3.
D15	TCLK4/RSIG4	I/O	Transmit Clock / Receive Signaling for/from Framer 4.
C16	TCLK5/RSIG5	I/O	Transmit Clock / Receive Signaling for/from Framer 5.
C19	TCLK6/RSIG6	I/O	Transmit Clock / Receive Signaling for/from Framer 6.
F17	TCLK7/RSIG7	I/O	Transmit Clock / Receive Signaling for/from Framer 7.
F19	TCLK8/RSIG8	I/O	Transmit Clock / Receive Signaling for/from Framer 8.
F20	TCLK9/RSIG9	I/O	Transmit Clock / Receive Signaling for/from Framer 9.
H19	TCLK10/RSIG10	I/O	Transmit Clock / Receive Signaling for/from Framer 10.
J18	TCLK11/RSIG11	I/O	Transmit Clock / Receive Signaling for/from Framer 11.
K19	TCLK12/RSIG12	I/O	Transmit Clock / Receive Signaling for/from Framer 12.
L16	TCLK13/RSIG13	I/O	Transmit Clock / Receive Signaling for/from Framer 13.
M16	TCLK14/RSIG14	I/O	Transmit Clock / Receive Signaling for/from Framer 14.
N18	TCLK15/RSIG15	I/O	Transmit Clock / Receive Signaling for/from Framer 15.
P18	TCLK16/RSIG16	I/O	Transmit Clock / Receive Signaling for/from Framer 16.
R18	TCLK17/RSIG17	I/O	Transmit Clock / Receive Signaling for/from Framer 17.
U19	TCLK18/RSIG18	I/O	Transmit Clock / Receive Signaling for/from Framer 18.
W19	TCLK19/RSIG19	I/O	Transmit Clock / Receive Signaling for/from Framer 19.
V17	TCLK20/RSIG20	I/O	Transmit Clock / Receive Signaling for/from Framer 20.
U15	TCLK21/RSIG21	I/O	Transmit Clock / Receive Signaling for/from Framer 21.
U14	TCLK22/RSIG22	I/O	Transmit Clock / Receive Signaling for/from Framer 22.
W14	TCLK23/RSIG23	I/O	Transmit Clock / Receive Signaling for/from Framer 23.
Y14	TCLK24/RSIG24	I/O	Transmit Clock / Receive Signaling for/from Framer 24.
V12	TCLK25/RSIG25	I/O	Transmit Clock / Receive Signaling for/from Framer 25.
V11	TCLK26/RSIG26	I/O	Transmit Clock / Receive Signaling for/from Framer 26.
T10	TCLK27/RSIG27	I/O	Transmit Clock / Receive Signaling for/from Framer 27.
V9	TCLK28/RSIG28	I/O	Transmit Clock / Receive Signaling for/from Framer 28.
D6	TEST	I	3-state Control for all Output and I/O Pins.
W8	TNRZ1	O	Transmit NRZ Data from Framer .
Y6	TNRZ2	O	Transmit NRZ Data from Framer 2.
W7	TNRZ3	O	Transmit NRZ Data from Framer 3.
W6	TNRZ4	O	Transmit NRZ Data from Framer 4.
W5	TNRZ5	O	Transmit NRZ Data from Framer 5.
U6	TNRZ6	O	Transmit NRZ Data from Framer 6.
W4	TNRZ7	O	Transmit NRZ Data from Framer 7.
V3	TNRZ8	O	Transmit NRZ Data from Framer 8.
W2	TNRZ9	O	Transmit NRZ Data from Framer 9.
U2	TNRZ10	O	Transmit NRZ Data from Framer 10.
W1	TNRZ11	O	Transmit NRZ Data from Framer 11.
T2	TNRZ12	O	Transmit NRZ Data from Framer 12.
R2	TNRZ13	O	Transmit NRZ Data from Framer 13.
N4	TNRZ14	O	Transmit NRZ Data from Framer 14.
R1	TNRZ15	O	Transmit NRZ Data from Framer 15.
M4	TNRZ16	O	Transmit NRZ Data from Framer 16.

LEAD	SIGNAL	TYPE	SIGNAL DESCRIPTION
M3	TNRZ17	O	Transmit NRZ Data from Framer 17.
L5	TNRZ18	O	Transmit NRZ Data from Framer 18.
L2	TNRZ19	O	Transmit NRZ Data from Framer 19.
K2	TNRZ20	O	Transmit NRZ Data from Framer 20.
K3	TNRZ21	O	Transmit NRZ Data from Framer 21.
J2	TNRZ22	O	Transmit NRZ Data from Framer 22.
J3	TNRZ23	O	Transmit NRZ Data from Framer 23.
H3	TNRZ24	O	Transmit NRZ Data from Framer 24.
G2	TNRZ25	O	Transmit NRZ Data from Framer 25.
G3	TNRZ26	O	Transmit NRZ Data from Framer 26.
F2	TNRZ27	O	Transmit NRZ Data from Framer 27.
F4	TNRZ28	O	Transmit NRZ Data from Framer 28.
E12	TSER1	I	Transmit Serial Data for Framer 1.
B14	TSER2	I	Transmit Serial Data for Framer 2.
B15	TSER3	I	Transmit Serial Data for Framer 3.
A18	TSER4	I	Transmit Serial Data for Framer 4.
B17	TSER5	I	Transmit Serial Data for Framer 5.
C17	TSER6	I	Transmit Serial Data for Framer 6.
B20	TSER7	I	Transmit Serial Data for Framer 7.
D20	TSER8	I	Transmit Serial Data for Framer 8.
G19	TSER9	I	Transmit Serial Data for Framer 9.
G20	TSER10	I	Transmit Serial Data for Framer 10.
K16	TSER11	I	Transmit Serial Data for Framer 11.
K17	TSER12	I	Transmit Serial Data for Framer 12.
L18	TSER13	I	Transmit Serial Data for Framer 13.
M18	TSER14	I	Transmit Serial Data for Framer 14.
P20	TSER15	I	Transmit Serial Data for Framer 15.
T20	TSER16	I	Transmit Serial Data for Framer 16.
T19	TSER17	I	Transmit Serial Data for Framer 17.
W20	TSER18	I	Transmit Serial Data for Framer 18.
U18	TSER19	I	Transmit Serial Data for Framer 19.
U16	TSER20	I	Transmit Serial Data for Framer 20.
Y20	TSER21	I	Transmit Serial Data for Framer 21.
W16	TSER22	I	Transmit Serial Data for Framer 22.
Y16	TSER23	I	Transmit Serial Data for Framer 23.
Y15	TSER24	I	Transmit Serial Data for Framer 24.
T11	TSER25	I	Transmit Serial Data for Framer 25.
U11	TSER26	I	Transmit Serial Data for Framer 26.
W10	TSER27	I	Transmit Serial Data for Framer 27.
W9	TSER28	I	Transmit Serial Data for Framer 28.
A13	TSYNC1/TSIG1	I/O	Transmit Sync / Transmit Signaling for Framer 1.
C13	TSYNC2/TSIG2	I/O	Transmit Sync / Transmit Signaling for Framer 2.
C14	TSYNC3/TSIG3	I/O	Transmit Sync / Transmit Signaling for Framer 3.
C15	TSYNC4/TSIG4	I/O	Transmit Sync / Transmit Signaling for Framer 4.

LEAD	SIGNAL	TYPE	SIGNAL DESCRIPTION
A20	TSYNC5/TSIG5	I/O	Transmit Sync / Transmit Signaling for Framer 5.
B19	TSYNC6/TSIG6	I/O	Transmit Sync / Transmit Signaling for Framer 6.
D19	TSYNC7/TSIG7	I/O	Transmit Sync / Transmit Signaling for Framer 7.
E19	TSYNC8/TSIG8	I/O	Transmit Sync / Transmit Signaling for Framer 8.
G18	TSYNC9/TSIG9	I/O	Transmit Sync / Transmit Signaling for Framer 9.
H18	TSYNC10/TSIG10	I/O	Transmit Sync / Transmit Signaling for Framer 10.
J16	TSYNC11/TSIG11	I/O	Transmit Sync / Transmit Signaling for Framer 11.
K18	TSYNC12/TSIG12	I/O	Transmit Sync / Transmit Signaling for Framer 12.
L19	TSYNC13/TSIG13	I/O	Transmit Sync / Transmit Signaling for Framer 13.
M19	TSYNC14/TSIG14	I/O	Transmit Sync / Transmit Signaling for Framer 14.
N19	TSYNC15/TSIG15	I/O	Transmit Sync / Transmit Signaling for Framer 15.
P19	TSYNC16/TSIG16	I/O	Transmit Sync / Transmit Signaling for Framer 16.
U20	TSYNC17/TSIG17	I/O	Transmit Sync / Transmit Signaling for Framer 17.
V20	TSYNC18/TSIG18	I/O	Transmit Sync / Transmit Signaling for Framer 18.
V19	TSYNC19/TSIG19	I/O	Transmit Sync / Transmit Signaling for Framer 19.
U17	TSYNC20/TSIG20	I/O	Transmit Sync / Transmit Signaling for Framer 20.
W17	TSYNC21/TSIG21	I/O	Transmit Sync / Transmit Signaling for Framer 21.
V15	TSYNC22/TSIG22	I/O	Transmit Sync / Transmit Signaling for Framer 22.
W15	TSYNC23/TSIG23	I/O	Transmit Sync / Transmit Signaling for Framer 23.
V13	TSYNC24/TSIG24	I/O	Transmit Sync / Transmit Signaling for Framer 24.
T12	TSYNC25/TSIG25	I/O	Transmit Sync / Transmit Signaling for Framer 25.
Y12	TSYNC26/TSIG26	I/O	Transmit Sync / Transmit Signaling for Framer 26.
Y10	TSYNC27/TSIG27	I/O	Transmit Sync / Transmit Signaling for Framer 27.
Y9	TSYNC28/TSIG28	I/O	Transmit Sync / Transmit Signaling for Framer 28.
A5	VDD_CORE	-	Positive Supply Voltage for the Core Logic.
A15	VDD_CORE	-	Positive Supply Voltage for the Core Logic.
E20	VDD_CORE	-	Positive Supply Voltage for the Core Logic.
H1	VDD_CORE	-	Positive Supply Voltage for the Core Logic.
R20	VDD_CORE	-	Positive Supply Voltage for the Core Logic.
U1	VDD_CORE	-	Positive Supply Voltage for the Core Logic.
Y17	VDD_CORE	-	Positive Supply Voltage for the Core Logic.
Y8	VDD_CORE	-	Positive Supply Voltage for the Core Logic.
E6	VDD_IO	-	Positive Supply Voltage for the Input & Output Buffers.
E15	VDD_IO	-	Positive Supply Voltage for the Input & Output Buffers.
F5	VDD_IO	-	Positive Supply Voltage for the Input & Output Buffers.
F16	VDD_IO	-	Positive Supply Voltage for the Input & Output Buffers.
J9	VDD_IO	-	Positive Supply Voltage for the Input & Output Buffers.
J12	VDD_IO	-	Positive Supply Voltage for the Input & Output Buffers.
M9	VDD_IO	-	Positive Supply Voltage for the Input & Output Buffers.
M12	VDD_IO	-	Positive Supply Voltage for the Input & Output Buffers.
R5	VDD_IO	-	Positive Supply Voltage for the Input & Output Buffers.
R16	VDD_IO	-	Positive Supply Voltage for the Input & Output Buffers.
T6	VDD_IO	-	Positive Supply Voltage for the Input & Output Buffers.
T15	VDD_IO	-	Positive Supply Voltage for the Input & Output Buffers.

LEAD	SIGNAL	TYPE	SIGNAL DESCRIPTION
J10	VSS	-	Signal Ground for the Input & Output Buffers & the Core.
J11	VSS	-	Signal Ground for the Input & Output Buffers & the Core.
K9	VSS	-	Signal Ground for the Input & Output Buffers & the Core.
K10	VSS	-	Signal Ground for the Input & Output Buffers & the Core.
K11	VSS	-	Signal Ground for the Input & Output Buffers & the Core.
K12	VSS	-	Signal Ground for the Input & Output Buffers & the Core.
L9	VSS	-	Signal Ground for the Input & Output Buffers & the Core.
L10	VSS	-	Signal Ground for the Input & Output Buffers & the Core.
L11	VSS	-	Signal Ground for the Input & Output Buffers & the Core.
L12	VSS	-	Signal Ground for the Input & Output Buffers & the Core.
M10	VSS	-	Signal Ground for the Input & Output Buffers & the Core.
M11	VSS	-	Signal Ground for the Input & Output Buffers & the Core.
A11	WR*/(R/W*)	I	Write Input (Read/Write). Active low.

TRANSMIT SIDE SIGNALS

Signal Name: **TCLK1 to TCLK28 / RSIG1 to RSIG28**
Signal Description: **Transmit Clock / Receive Signaling Output**
Signal Type: **Input/Output / Output**

Mode	Mode Description	Function of TCLK/RSIG Signal
1	Normal Loop Timed with no Gapped Clocks on RSYNC & TSYNC	Outputs a T1 clock which is based on the receive clock (RCLK) from the associated receive side framer.
2	Normal Loop Timed with Gapped Clocks on RSYNC & TSYNC	Outputs a T1 clock which is based on the receive clock (RCLK) from the associated receive side framer.
3	Normal External Timed with no Gapped Clocks on RSYNC & TSYNC	Outputs a T1 clock which is based on the clock applied at CTCLK.
4	Normal External Timed with Gapped Clocks on RSYNC & TSYNC	Outputs a T1 clock which is based on the clock applied at CTCLK.
5	RSIG/TSIG Access Loop Timed with no Gapped Clocks on RSYNC	Outputs receive side signaling bits in a PCM format. Updated on the rising edge of RCLK.
6	RSIG/TSIG Access Loop Timed with Gapped Clocks on RSYNC	Outputs receive side signaling bits in a PCM format. Updated on the rising edge of RCLK.
7	RSIG/TSIG Access External Timed with no Gapped Clocks on RSYNC	Outputs receive side signaling bits in a PCM format. Updated on the rising edge of RCLK.
8	RSIG/TSIG Access External Timed with Gapped Clocks on RSYNC	Outputs receive side signaling bits in a PCM format. Updated on the rising edge of RCLK.
9	8 Mbps IBO Loop Timed	Outputs receive side signaling bits in a PCM format. Updated on the rising edge of 8MCLKI.
10	8 Mbps IBO External Timed	Outputs receive side signaling bits in a PCM format. Updated on the rising edge of 8MCLKI.

Mode	Mode Description	Function of TCLK/RSIG Signal
11	Independent TCLK Timing with TSYNC an Input and no Gapped Clocks on RSYNC & TSYNC	Inputs an independent T1 clock for each of the 28 formatters.
12	Independent TCLK Timing with TSYNC an Output and no Gapped Clocks on RSYNC & TSYNC	Inputs an independent T1 clock for each of the 28 formatters.
13	Independent TCLK Timing with TSYNC an Output and Gapped Clocks on RSYNC & TSYNC	Inputs an independent T1 clock for each of the 28 formatters.

Signal Name: **CTCLK**
Signal Description: **Common Transmit Clock**
Signal Type: **Input**
Transmit T1 (1.544 MHz) clock that can be used for all 28 transmit formatters.

Signal Name: **CTSYNC**
Signal Description: **Common Transmit Frame Sync**
Signal Type: **Output**
An output that pulses high for one CTCLK or 8MCLKI during the F-bit position to indicate the transmit 8 kHz frame boundary.

Signal Name: **TSYNC1 to TSYNC28 / TSIG1 to TSIG28**
Signal Description: **Transmit Sync / Transmit Signaling Input**
Signal Type: **Input/Output / Input**

Mode	Mode Description	Function of TSYNC/TSIG Signal
1	Normal Loop Timed with no Gapped Clocks on RSYNC & TSYNC	Outputs a one TCLK wide 8 kHz frame sync pulse.
2	Normal Loop Timed with Gapped Clocks on RSYNC & TSYNC	Outputs a gapped T1 clock which suppresses a clock pulse during the F-Bit position.
3	Normal External Timed with no Gapped Clocks on RSYNC & TSYNC	Outputs a one TCLK wide 8 kHz frame sync pulse.
4	Normal External Timed with Gapped Clocks on RSYNC & TSYNC	Outputs a gapped T1 clock which suppresses a clock pulse during the F-Bit position.
5	RSIG/TSIG Access Loop Timed with no Gapped Clocks on RSYNC	Inputs transmit side signaling bits in a PCM format. Sampled on the falling edge of RCLK.
6	RSIG/TSIG Access Loop Timed with Gapped Clocks on RSYNC	Inputs transmit side signaling bits in a PCM format. Sampled on the falling edge of RCLK.
7	RSIG/TSIG Access External Timed with no Gapped Clocks on RSYNC	Inputs transmit side signaling bits in a PCM format. Sampled on the falling edge of CTCLK.
8	RSIG/TSIG Access External Timed with Gapped Clocks on RSYNC	Inputs transmit side signaling bits in a PCM format. Sampled on the falling edge of CTCLK.

Mode	Mode Description	Function of TSYNC/TSIG Signal
9	8 Mbps IBO Loop Timed	Inputs transmit side signaling bits in a PCM format. Sampled on the falling edge of 8MCLKI.
10	8 Mbps IBO External Timed	Inputs transmit side signaling bits in a PCM format. Sampled on the falling edge of 8MCLKI.
11	Independent TCLK Timing with TSYNC an Input and no Gapped Clocks on RSYNC & TSYNC	Inputs a 8 kHz frame sync pulse which establishes the frame boundaries independently for each of the 28 formatters.
12	Independent TCLK Timing with TSYNC an Output and no Gapped Clocks on RSYNC & TSYNC	Outputs a one TCLK wide 8 kHz frame sync pulse.
13	Independent TCLK Timing with TSYNC an Output and Gapped Clocks on RSYNC & TSYNC	Outputs a gapped T1 clock which suppresses a clock pulse during the F-Bit position.

Signal Name: **TNRZ1 to TNRZ28**
Signal Description: **Transmit NRZ Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLK or CTCLK with the NRZ data out of the transmit side formatter.

Signal Name: **TSER1 to TSER28**
Signal Description: **Transmit Serial Data**
Signal Type: **Input**
Transmit NRZ serial data. Sampled on the falling edge of TCLK, CTCLK or 8MCLKI.

RECEIVE SIDE SIGNALS

Signal Name: **RNRZ1 to RNRZ28**
Signal Description: **Receive NRZ Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLK for data to be clocked through the receive side framer.

Signal Name: **RCLK1 to RCLK28**
Signal Description: **Receive Clock Input**
Signal Type: **Input**
T1 input clock used to clock data through the receive side framer.

Signal Name: **RSER1 to RSER28**
Signal Description: **Receive Serial Data**
Signal Type: **Output**
Received NRZ serial data. Updated on the rising edge of RCLK or 8MCLKI.

Signal Name: **RSYNC1 to RSYNC28**
Signal Description: **Receive Sync**
Signal Type: **Output**
In Modes 1, 3, 5, 7, 9, 10, 11, & 12, RSYNC provides an extracted 8 kHz pulse, one RCLK wide which identifies frame boundaries. In Modes 2, 4, 6, 8, and 13, RSYNC provides a “gapped” RCLK which has the clock pulse during the F-Bit position suppressed. See Section 20 for timing details.

8 MHZ SIGNALS

Signal Name: **CLKSI**
Signal Description: **8 MHz Clock Reference**
Signal Type: **Input**
A 1.544 MHz reference clock used in the generation of 8MCLK.

Signal Name: **8MCLK**
Signal Description: **8 MHz Clock**
Signal Type: **Output**
A 8.192 MHz output clock that is referenced to the T1 clock that is input at the CLKSI signal.

Signal Name: **8MCLKI**
Signal Description: **8 MHz IBO Clock**
Signal Type: **Input**
A 8.192 MHz clock used in Modes 9 & 10 to support Interleaved Bus Operation (IBO). Should be tied low in modes other than 9 & 10.

Signal Name: **8MSYNC**
Signal Description: **8 kHz Frame Sync for the 8 MHz IBO Mode**
Signal Type: **Input**
A 8 kHz frame sync that is referenced to the 8MCLKI signal to indicate frame boundaries; supports Interleaved Bus Operation (IBO) in Modes 9 & 10. Should be tied low in modes other than 9 & 10.

MODE SELECT SIGNALS

Signal Name: **MODE0 to MODE3**
Signal Description: **Device Operating Mode Select**
Signal Type: **Input**

MODE0 to MODE3 select the operating mode for the device. The device should be reset when changing device modes.

MODE3/MODE2/MODE1/MODE0				Mode	Mode Description
0	0	0	0	1	Normal Loop Timed with no Gapped Clocks on RSYNC & TSYNC
0	0	0	1	2	Normal Loop Timed with Gapped Clocks on RSYNC & TSYNC
0	0	1	0	3	Normal External Timed with no Gapped Clocks on RSYNC & TSYNC
0	0	1	1	4	Normal External Timed with Gapped Clocks on RSYNC & TSYNC
0	1	0	0	5	RSIG/TSIG Access Loop Timed with no Gapped Clocks on RSYNC
0	1	0	1	6	RSIG/TSIG Access Loop Timed with Gapped Clocks on RSYNC
0	1	1	0	7	RSIG/TSIG Access External Timed with no Gapped Clocks on RSYNC
0	1	1	1	8	RSIG/TSIG Access External Timed with Gapped Clocks on RSYNC
1	0	0	0	9	8 Mbps IBO Loop Timed
1	0	0	1	10	8 Mbps IBO External Timed
1	0	1	0	11	Independent TCLK Timing with TSYNC an Input and no Gapped Clocks on RSYNC & TSYNC
1	0	1	1	12	Independent TCLK Timing with TSYNC an Output and no Gapped Clocks on RSYNC & TSYNC
1	1	0	0	13	Independent TCLK Timing with TSYNC an Output and Gapped Clocks on RSYNC & TSYNC
1	1	0	1	-	Reserved
1	1	1	0	-	Reserved
1	1	1	1	-	Reserved

PARALLEL CONTROL PORT SIGNALS

Signal Name: **INT***
Signal Description: **Interrupt**
Signal Type: **Output (open drain)**

Flags host controller during important change of conditions in device status. Active low, open drain output.

Signal Name: **MUX**
Signal Description: **Bus Operation**
Signal Type: **Input**
Set low to select non–multiplexed bus operation. Set high to select multiplexed bus operation.

Signal Name: **D0 to D7 / AD0 to AD7**
Signal Description: **Data Bus / Address/Data Bus**
Signal Type: **Input /Output**
In non–multiplexed bus operation (MUX = 0), serves as the data bus. In multiplexed bus operation (MUX = 1), serves as a 8–bit multiplexed address / data bus.

Signal Name: **A0 to A5, A7**
Signal Description: **Address Bus**
Signal Type: **Input**
In non–multiplexed bus operation (MUX = 0), serves as the address bus. In multiplexed bus operation (MUX = 1), these pins are not used and should be tied low.

Signal Name: **ALE(AS) / A6**
Signal Description: **A6 or Address Latch Enable (Address Strobe)**
Signal Type: **Input**
In non–multiplexed bus operation (MUX = 0), serves as address bit 6. In multiplexed bus operation (MUX = 1), serves to demultiplex the bus on a positive–going edge.

Signal Name: **BTS**
Signal Description: **Bus Type Select**
Signal Type: **Input**
Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the RD*(DS*), ALE(AS), and WR*(R/W*) pins. If BTS = 1, then these pins assume the function listed in parenthesis ().

Signal Name: **RD*(DS*)**
Signal Description: **Read Input (Data Strobe)**
Signal Type: **Input**
RD* and DS* are active low signals. Refer to bus timing diagrams in Section 21.

Signal Name: **CS***
Signal Description: **Chip Select**
Signal Type: **Input**
Must be low to read or write to the device. CS* is an active low signal.

Signal Name: **WR*(R/W*)**
Signal Description: **Write Input(Read/Write)**
Signal Type: **Input**
WR* is an active low signal.

Signal Name: **FS0 to FS4**
Signal Description: **Framer Selects**
Signal Type: **Input**
Selects which of the 28 framers to be accessed.

FS4	FS3	FS2	FS1	FS0	Framer Accessed	FS4	FS3	FS2	FS1	FS0	Framer Accessed
0	0	0	0	0	1	1	0	0	0	0	17
0	0	0	0	1	2	1	0	0	0	1	18
0	0	0	1	0	3	1	0	0	1	0	19
0	0	0	1	1	4	1	0	0	1	1	20
0	0	1	0	0	5	1	0	1	0	0	21
0	0	1	0	1	6	1	0	1	0	1	22
0	0	1	1	0	7	1	0	1	1	0	23
0	0	1	1	1	8	1	0	1	1	1	24
0	1	0	0	0	9	1	1	0	0	0	25
0	1	0	0	1	10	1	1	0	0	1	26
0	1	0	1	0	11	1	1	0	1	0	27
0	1	0	1	1	12	1	1	0	1	1	28
0	1	1	0	0	13	1	1	1	0	0	reserved
0	1	1	0	1	14	1	1	1	0	1	reserved
0	1	1	1	0	15	1	1	1	1	0	reserved
0	1	1	1	1	16	1	1	1	1	1	ISR1/2/3/4

Note:
The ISR1/2/3/4 registers are accessed when FS0 to FS4 is set to 11111.

TEST ACCESS PORT SIGNALS

Signal Name: **TEST**
Signal Description: **3–State Control**
Signal Type: **Input**
Set high to 3–state all output and I/O pins (including the parallel control port) when JTRST* is tied low. Set low for normal operation. Ignored when JTRST* = 1. Useful in board level testing. Note: TEST should not be tied high when FIACT* is active (i.e., FIACT* = 0) as this will place the device into a special test mode.

Signal Name: **FIACT***
Signal Description: **Force RSER, TNRZ, and INT* Inactive**
Signal Type: **Input**
Set low for force INT* high (i.e., open drain) and RSER1 to RSER28 and TNRZ1 to TNRZ28 high. Set high for normal operation. Ignored when JTRST* = 1 or TEST = 1. Useful for placing the major outputs of the device into a known state on power-up. Note: FIACT* should not be tied low when TEST is active (i.e., TEST = 1) as this will place the device into a special test mode.

Signal Name: **JTRST***
Signal Description: **IEEE 1149.1 Test Reset**
Signal Type: **Input**
This signal is used to asynchronously reset the test access port controller. At power up, JTRST* must be set low and then high. This action will set the device into the DEVICE ID mode allowing normal device operation. If boundary scan is not used, this pin should be tied to ground. This pin is pulled up internally by a 10K ohm resistor.

Signal Name: **JTMS**
Signal Description: **IEEE 1149.1 Test Mode Select**
Signal Type: **Input**
This pin is sampled on the rising edge of JTCLK and is used to place the test port into the various defined IEEE 1149.1 states. This pin is pulled up internally by a 10K ohm resistor. If not used, this pin should be left unconnected.

Signal Name: **JTCLK**
Signal Description: **IEEE 1149.1 Test Clock Signal**
Signal Type: **Input**
This signal is used to shift data into JTDI pin on the rising edge and out of JTDO pin on the falling edge. If not used, this pin should be connected to ground.

Signal Name: **JTDI**
Signal Description: **IEEE 1149.1 Test Data Input**
Signal Type: **Input**
Test instructions and data are clocked into this pin on the rising edge of JTCLK. This pin is pulled up internally by a 10K ohm resistor. If not used, this pin should be left unconnected.

Signal Name: **JTDO**
Signal Description: **IEEE 1149.1 Test Data Output**
Signal Type: **Output**
Test instructions and data are clocked out of this pin on the falling edge of JTCLK.

SUPPLY SIGNALS

Signal Name: **VDD_CORE**
Signal Description: **Positive Supply for the Core Logic**
Signal Type: **Supply**
1.8 (± 5%) volts.

Signal Name: **VDD_IO**
Signal Description: **Positive Supply for the Input & Output Buffers**
Signal Type: **Supply**
3.3 (± 10%) volts.

Signal Name: **VSS**
Signal Description: **Signal Ground for the Input & Output Buffers and the Core Logic**
Signal Type: **Supply**
0.0 volts. All VSS signals should be tied together.

3. DEVICE OPERATING MODES

The DS3120 can be operated in one of 13 different modes. The operating mode of the device is selected via the MODE0 to MODE3 signals. See Table 13-1.

The various operating modes of the device can be broken down into one of four major configurations:

Normal	Standard configuration with data and frame syncs output on the receive side. On the transmit side, clock and frame sync are output and data is sampled
Hardware Based Signaling	Robbed bit signaling is accessible via the RSIG and TSIG signals; RSIG is made available at the expense of the transmit clock output and TSIG is made available at the expense of the transmit frame sync output
8 MHz IBO (supports H.100 & MVIP applications)	Backplane option that aggregates four T1 data streams into a single 8.192 MHz data stream; see Section 18 for a more detailed explanation of this mode
Independent TCLK	Allows each transmit framer to be clocked independently

Each of the configurations above can be set up as either "Loop Timed" or External Timed" as described below.

Loop Timed	The clock and frame sync from each receive side framer is routed back to the respective transmit side formatter
External Timed	The transmit side clock and frame sync are generated from a common externally supplied T1 clock source

Also each configuration allows the RSYNC, TSYNC and CTSYNC frame sync signals to supply either a 8 kHz frame sync pulse or a gapped clock.

No Gapped Clocks	The sync signals supply a one clock wide 8 kHz frame sync pulse
Gapped Clocks	The sync signals supply a T1 clock that is gapped (i.e., the clock pulse is suppressed) during the F bit position

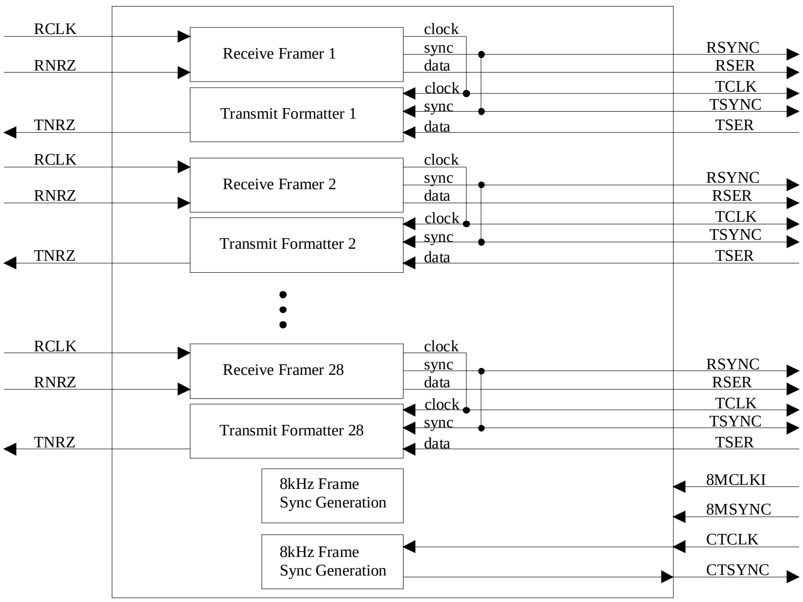
DS3120 Mode Selection Table 13-1

MODE3/MODE2/MODE1/MODE0				**Mode**	**Mode Description**
0	0	0	0	1	Normal Loop Timed with no Gapped Clocks on RSYNC & TSYNC
0	0	0	1	2	Normal Loop Timed with Gapped Clocks on RSYNC & TSYNC
0	0	1	0	3	Normal External Timed with no Gapped Clocks on RSYNC & TSYNC
0	0	1	1	4	Normal External Timed with Gapped Clocks on RSYNC & TSYNC
0	1	0	0	5	RSIG/TSIG Access Loop Timed with no Gapped Clocks on RSYNC
0	1	0	1	6	RSIG/TSIG Access Loop Timed with Gapped Clocks on RSYNC
0	1	1	0	7	RSIG/TSIG Access External Timed with no Gapped

MODE3/MODE2/MODE1/MODE0				Mode	Mode Description
					Clocks on RSYNC
0	1	1	1	8	RSIG/TSIG Access External Timed with Gapped Clocks on RSYNC
1	0	0	0	9	8 Mbps IBO Loop Timed
1	0	0	1	10	8 Mbps IBO External Timed
1	0	1	0	11	Independent TCLK Timing with TSYNC an Input and no Gapped Clocks on RSYNC & TSYNC
1	0	1	1	12	Independent TCLK Timing with TSYNC an Output and no Gapped Clocks on RSYNC & TSYNC
1	1	0	0	13	Independent TCLK Timing with TSYNC an Output and Gapped Clocks on RSYNC & TSYNC
1	1	0	1	-	Reserved
1	1	1	0	-	Reserved
1	1	1	1	-	Reserved

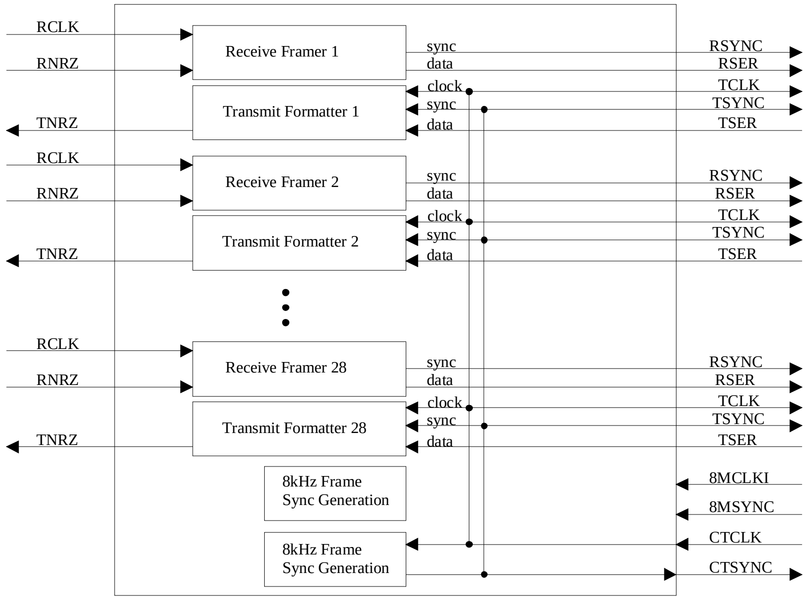
Mode 1 **Normal Loop Timed with no Gapped Clocks on RSYNC & TSYNC**
Mode 2 **Normal Loop Timed with Gapped Clocks on RSYNC & TSYNC**

Modes 1 and 2 Figure 3-1



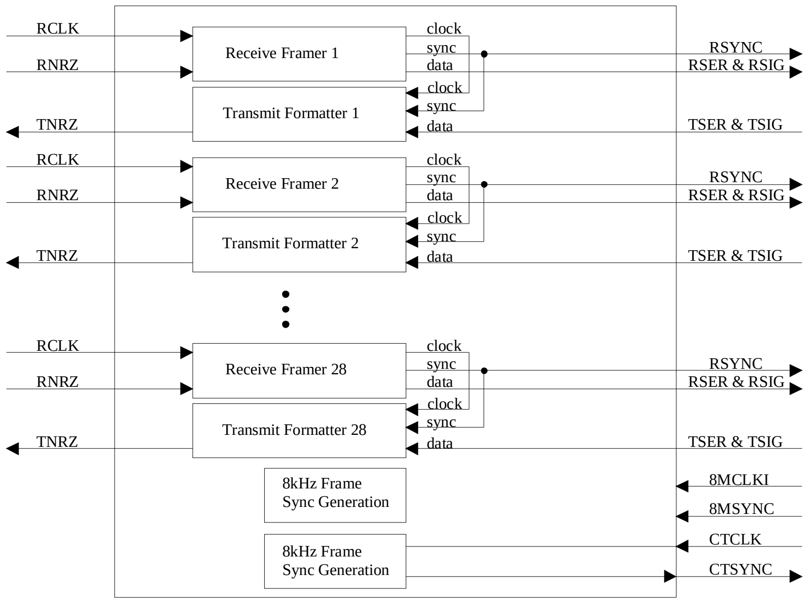
Mode 3 Normal External Timed with no Gapped Clocks on RSYNC & TSYNC
Mode 4 Normal External Timed with Gapped Clocks on RSYNC & TSYNC

Modes 3 and 4 Figure 3-2



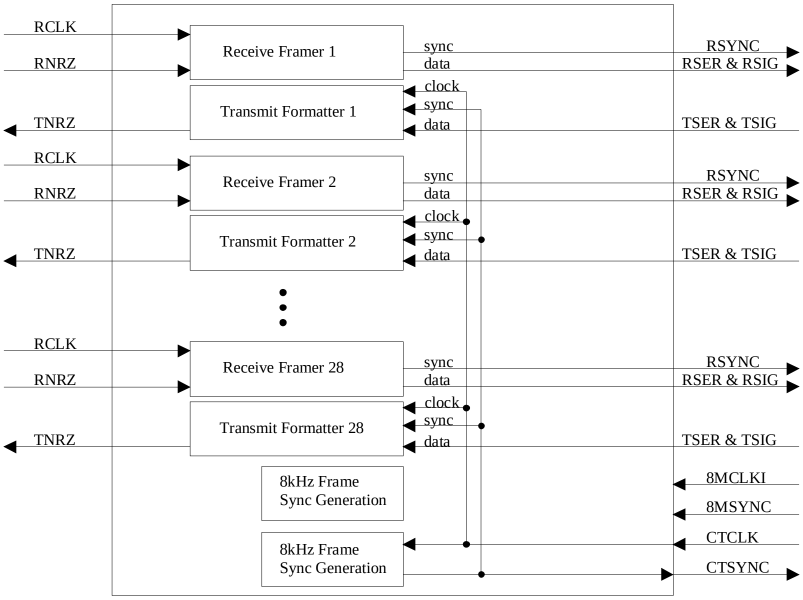
Mode 5 RSIG/TSIG Access Loop Timed with no Gapped Clocks on RSYNC
Mode 6 RSIG/TSIG Access Loop Timed with Gapped Clocks on RSYNC

Modes 5 and 6 Figure 3-3



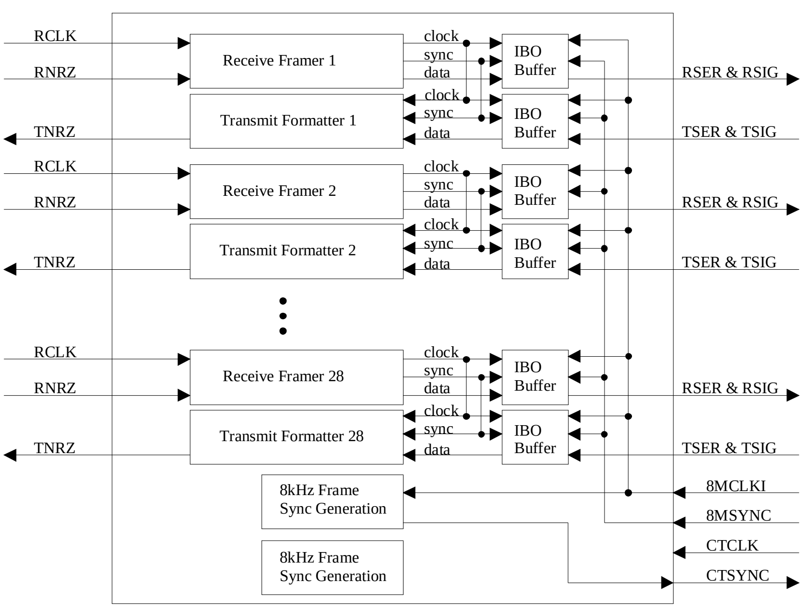
Mode 7 RSIG/TSIG Access External Timed with no Gapped Clocks on RSYNC
Mode 8 RSIG/TSIG Access External Timed with Gapped Clocks on RSYNC

Modes 7 and 8 Figure 3-4



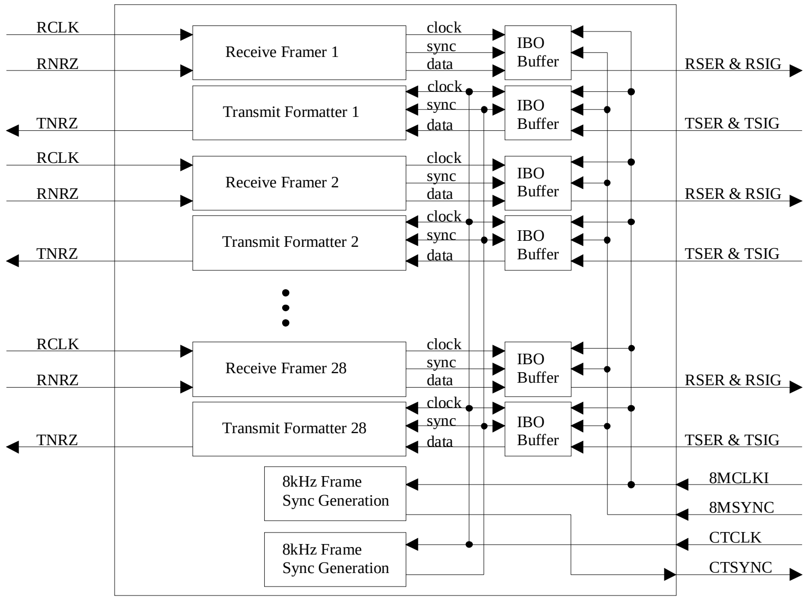
Mode 9 8 Mbps IBO Loop Timed

Mode 9 Figure 3-5



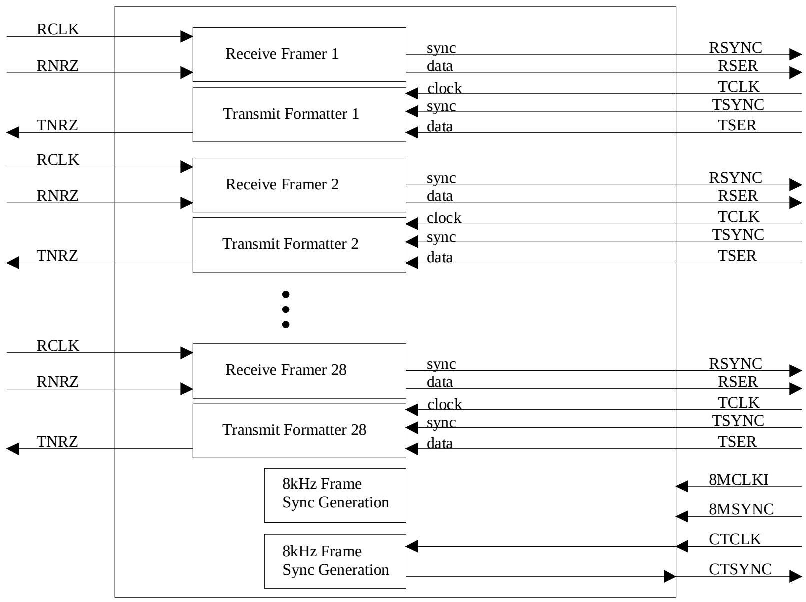
Mode 10 8 Mbps IBO External Timed

Mode 10 Figure 3-6



Mode 11 Independent TCLK Timing with TSYNC an Input and no Gapped Clocks on RSYNC & TSYNC

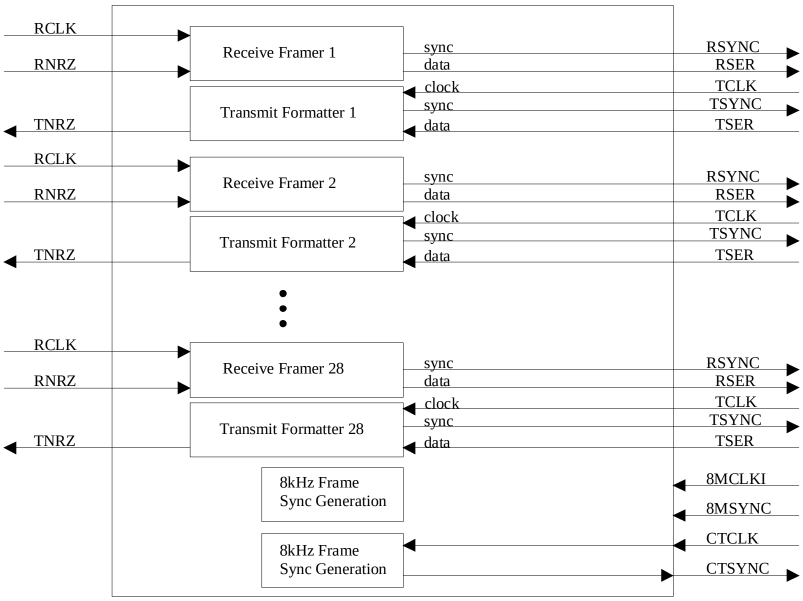
Mode 11 Figure 3-7



Mode 12 **Independent TCLK Timing with TSYNC an Output and no Gapped Clocks on RSYNC & TSYNC**

Mode 13 **Independent TCLK Timing with TSYNC an Output and Gapped Clocks on RSYNC & TSYNC**

Modes 12 and 13 Figure 3-8



4. DS3120 REGISTER MAP

Register Map Sorted by Address Table 4-1

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
00	R/W	HDLC Control	HCR
01	R/W	HDLC Status	HSR
02	R/W	HDLC Interrupt Mask	HIMR
03	R/W	Receive HDLC Information	RHIR
04	R/W	Receive Bit Oriented Code	RBOC
05	R	Receive HDLC FIFO	RHFR
06	R/W	Transmit HDLC Information	THIR
07	R/W	Transmit Bit Oriented Code	TBOC
08	W	Transmit HDLC FIFO	THFR
09	–	Not used	(set to 00h)
0A	R/W	Common Control 7	CCR7
0B	–	Not used	(set to 00h)
0C	–	Not used	(set to 00h)
0D	–	Not used	(set to 00h)
0E	–	Not used	(set to 00h)
0F	R	Device ID	IDR
10	R/W	Receive Information 3	RIR3
11	R/W	Common Control 4	CCR4

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
12	R/W	In–Band Code Control	IBCC
13	R/W	Transmit Code Definition	TCD
14	R/W	Receive Up Code Definition	RUPCD
15	R/W	Receive Down Code Definition	RDNCD
16	R/W	Transmit Channel Control 1	TCC1
17	R/W	Transmit Channel Control 2	TCC2
18	R/W	Transmit Channel Control 3	TCC3
19	R/W	Common Control 5	CCR5
1A	R	Transmit DS0 Monitor	TDS0M
1B	R/W	Receive Channel Control 1	RCC1
1C	R/W	Receive Channel Control 2	RCC2
1D	R/W	Receive Channel Control 3	RCC3
1E	R/W	Common Control 6	CCR6
1F	R	Receive DS0 Monitor	RDS0M
20	R/W	Status 1	SR1
21	R/W	Status 2	SR2
22	R/W	Receive Information 1	RIR1
23	R	Line Code Violation Count 1	LCVCR1
24	R	Line Code Violation Count 2	CVCR2
25	R	Path Code Violation Count 1	PCVCR1
26	R	Path Code violation Count 2	PCVCR2
27	R	Multiframe Out of Sync Count 2	MOSCR2
28	R	Receive FDL Register	RFDL
29	R/W	Receive FDL Match 1	RMTCH1
2A	R/W	Receive FDL Match 2	RMTCH2
2B	R/W	Receive Control 1	RCR1
2C	R/W	Receive Control 2	RCR2
2D	R/W	Receive Mark 1	RMR1
2E	R/W	Receive Mark 2	RMR2
2F	R/W	Receive Mark 3	RMR3
30	R/W	Common Control 3	CCR3
31	R/W	Receive Information 2	RIR2
32	R/W	Transmit Channel Blocking 1	TCBR1
33	R/W	Transmit Channel blocking 2	TCBR2
34	R/W	Transmit Channel Blocking 3	TCBR3
35	R/W	Transmit Control 1	TCR1
36	R/W	Transmit Control 2	TCR2
37	R/W	Common Control 1	CCR1
38	R/W	Common Control 2	CCR2
39	R/W	Transmit Transparency 1	TTR1
3A	R/W	Transmit Transparency 2	TTR2
3B	R/W	Transmit Transparency 3	TTR3
3C	R/W	Transmit Idle 1	TIR1
3D	R/W	Transmit Idle 2	TIR2

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
3E	R/W	Transmit Idle 3	TIR3
3F	R/W	Transmit Idle Definition	TIDR
40	R/W	Transmit Channel 9	TC9
41	R/W	Transmit Channel 10	TC10
42	R/W	Transmit Channel 11	TC11
43	R/W	Transmit Channel 12	TC12
44	R/W	Transmit Channel 13	TC13
45	R/W	Transmit Channel 14	TC14
46	R/W	Transmit Channel 15	TC15
47	R/W	Transmit Channel 16	TC16
48	R/W	Transmit Channel 17	TC17
49	R/W	Transmit Channel 18	TC18
4A	R/W	Transmit Channel 19	TC19
4B	R/W	Transmit Channel 20	TC20
4C	R/W	Transmit Channel 21	TC21
4D	R/W	Transmit Channel 22	TC22
4E	R/W	Transmit Channel 23	TC23
4F	R/W	Transmit Channel 24	TC24
50	R/W	Transmit Channel 1	TC1
51	R/W	Transmit Channel 2	TC2
52	R/W	Transmit Channel 3	TC3
53	R/W	Transmit Channel 4	TC4
54	R/W	Transmit Channel 5	TC5
55	R/W	Transmit Channel 6	TC6
56	R/W	Transmit Channel 7	TC7
57	R/W	Transmit Channel 8	TC8
58	R/W	Receive Channel 17	RC17
59	R/W	Receive Channel 18	RC18
5A	R/W	Receive Channel 19	RC19
5B	R/W	Receive Channel 20	RC20
5C	R/W	Receive Channel 21	RC21
5D	R/W	Receive Channel 22	RC22
5E	R/W	Receive Channel 23	RC23
5F	R/W	Receive Channel 24	RC24
60	R	Receive Signaling 1	RS1
61	R	Receive Signaling 2	RS2
62	R	Receive Signaling 3	RS3
63	R	Receive Signaling 4	RS4
64	R	Receive Signaling 5	RS5
65	R	Receive Signaling 6	RS6
66	R	Receive Signaling 7	RS7
67	R	Receive Signaling 8	RS8
68	R	Receive Signaling 9	RS9
69	R	Receive Signaling 10	RS10

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
6A	R	Receive Signaling 11	RS11
6B	R	Receive Signaling 12	RS12
6C	R/W	Receive Channel Blocking 1	RCBR1
6D	R/W	Receive Channel Blocking 2	RCBR2
6E	R/W	Receive Channel Blocking 3	RCBR3
6F	R/W	Interrupt Mask 2	IMR2
70	R/W	Transmit Signaling 1	TS1
71	R/W	Transmit Signaling 2	TS2
72	R/W	Transmit Signaling 3	TS3
73	R/W	Transmit Signaling 4	TS4
74	R/W	Transmit Signaling 5	TS5
75	R/W	Transmit Signaling 6	TS6
76	R/W	Transmit Signaling 7	TS7
77	R/W	Transmit Signaling 8	TS8
78	R/W	Transmit Signaling 9	TS9
79	R/W	Transmit Signaling 10	TS10
7A	R/W	Transmit Signaling 11	TS11
7B	R/W	Transmit Signaling 12	TS12
7C	–	Not used	(set to 00h)
7D	R/W	Test 1	TEST1 (set to 00h)
7E	R/W	Transmit FDL Register	TFDL
7F	R/W	Interrupt Mask Register 1	IMR1
80	R/W	Receive Channel 1	RC1
81	R/W	Receive Channel 2	RC2
82	R/W	Receive Channel 3	RC3
83	R/W	Receive Channel 4	RC4
84	R/W	Receive Channel 5	RC5
85	R/W	Receive Channel 6	RC6
86	R/W	Receive Channel 7	RC7
87	R/W	Receive Channel 8	RC8
88	R/W	Receive Channel 9	RC9
89	R/W	Receive Channel 10	RC10
8A	R/W	Receive Channel 11	RC11
8B	R/W	Receive Channel 12	RC12
8C	R/W	Receive Channel 13	RC13
8D	R/W	Receive Channel 14	RC14
8E	R/W	Receive Channel 15	RC15
8F	R/W	Receive Channel 16	RC16
90	R/W	Receive HDLC DS0 Control Register 1	RDC1
91	R/W	Receive HDLC DS0 Control Register 2	RDC2
92	R/W	Transmit HDLC DS0 Control Register 1	TDC1
93	R/W	Transmit HDLC DS0 Control Register 2	TDC2
94	R/W	Interleave Bus Operation Register	IBO
95	–	Not used	(set to 00h)

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
96	R/W	Test 2	TEST2 (set to 00h)
97	–	Not used	(set to 00h)
98	–	Not used	(set to 00h)
99	–	Not used	(set to 00h)
9A	–	Not used	(set to 00h)
9B	–	Not used	(set to 00h)
9C	–	Not used	(set to 00h)
9D	–	Not used	(set to 00h)
9E	–	Not used	(set to 00h)
9F	–	Not used	(set to 00h)

NOTES:

1. Test Registers 1 and 2 are used only by the factory; these registers must be cleared (set to all zeros) on power– up initialization to insure proper operation.
2. Register banks AxH, BxH, CxH, DxH, ExH, and FxH are not accessible.

5. PARALLEL PORT

The DS3120 is controlled via either a non-multiplexed (MUX = 0) or a multiplexed (MUX = 1) bus by an external microcontroller or microprocessor. The DS3120 can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). The external microcontroller will determine which framer is to be accessed via the setting of the FS0 to FS4 signals. See Table 5-1. See the timing diagrams in the A.C. Electrical Characteristics in Section 21 for more details.

Framer Select Decode Table 5-1

FS4	FS3	FS2	FS1	FS0	Framer Accessed	FS4	FS3	FS2	FS1	FS0	Framer Accessed
0	0	0	0	0	1	1	0	0	0	0	17
0	0	0	0	1	2	1	0	0	0	1	18
0	0	0	1	0	3	1	0	0	1	0	19
0	0	0	1	1	4	1	0	0	1	1	20
0	0	1	0	0	5	1	0	1	0	0	21
0	0	1	0	1	6	1	0	1	0	1	22
0	0	1	1	0	7	1	0	1	1	0	23
0	0	1	1	1	8	1	0	1	1	1	24
0	1	0	0	0	9	1	1	0	0	0	25
0	1	0	0	1	10	1	1	0	0	1	26
0	1	0	1	0	11	1	1	0	1	0	27
0	1	0	1	1	12	1	1	0	1	1	28
0	1	1	0	0	13	1	1	1	0	0	reserved
0	1	1	0	1	14	1	1	1	0	1	reserved
0	1	1	1	0	15	1	1	1	1	0	reserved
0	1	1	1	1	16	1	1	1	1	1	ISR1/2/3/4

Note:

The ISR1/2/3/4 registers are accessed when FS0 to FS4 is set to 11111.

6. CONTROL, ID AND TEST REGISTERS

The operation of each framer within the DS3120 is configured via a set of eleven control registers. Typically, the control registers are only accessed when the system is first powered up. Once a channel in the DS3120 has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Register (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), and seven Common Control Registers (CCR1 to CCR7). Each of the eleven registers are described in this section. There is a device Identification Register (IDR) at address 0Fh.

Power–Up Sequence

The DS3120 does not automatically clear its register space on power–up. After the supplies are stable, each of the 28 framer's register space should be configured for operation by writing to all of the internal registers. This includes setting the Test and all unused registers to 00 Hex.

This can be accomplished using a two-pass approach on each framer within the DS3120.

1. Clear each framer's register space by writing 00h to the addresses 00h through 09Fh.
2. Program required registers to achieve desired operating mode.

IDR: DEVICE IDENTIFICATION REGISTER (Address=0F Hex)

(MSB)							(LSB)
T1E1	0	0	0	ID3	ID2	ID1	ID0

SYMBOL	POSITION	NAME AND DESCRIPTION
T1E1	IDR.7	**T1 or E1 Chip Determination Bit.** 0=T1 chip 1=E1 chip
ID3	IDR.3	**Chip Revision Bit 3.** MSB of a decimal code that represents the chip revision.
ID2	IDR.1	**Chip Revision Bit 2.**
ID1	IDR.2	**Chip Revision Bit 1.**
ID0	IDR.0	**Chip Revision Bit 0.** LSB of a decimal code that represents the chip revision.

RCR1: RECEIVE CONTROL REGISTER 1 (Address=2B Hex)

(MSB)							(LSB)
1	ARC	OOF1	OOF2	SYNCC	SYNCT	SYNCE	RESYNC

SYMBOL	POSITION	NAME AND DESCRIPTION
1	RCR1.7	This control bit must be set to one.
ARC	RCR1.6	**Auto Resync Criteria.** 0 = Resync on OOF or RCL event 1 = Resync on OOF only
OOF1	RCR1.5	**Out Of Frame Select 1.** 0 = 2/4 frame bits in error 1 = 2/5 frame bits in error
OOF2	RCR1.4	**Out Of Frame Select 2.** 0 = follow RCR1.5 1 = 2/6 frame bits in error
SYNCC	RCR1.3	**Sync Criteria.** **In D4 Framing Mode.** 0 = search for Ft pattern, then search for Fs pattern 1 = cross couple Ft and Fs pattern **In ESF Framing Mode.** 0 = search for FPS pattern only 1 = search for FPS and verify with CRC6
SYNCT	RCR1.2	**Sync Time.** 0 = qualify 10 bits 1 = qualify 24 bits
SYNCE	RCR1.1	**Sync Enable.** 0 = auto resync enabled 1 = auto resync disabled
RESYNC	RCR1.0	**Resync.** When toggled from low to high, a resynchronization of the receive side framer is initiated. Must be cleared and set again for a subsequent resync.

RCR2: RECEIVE CONTROL REGISTER 2 (Address=2C Hex)

(MSB)							(LSB)
RCS	0	0	0	1	RD4YM	FSBE	MOSCRF

SYMBOL	POSITION	NAME AND DESCRIPTION
RCS	RCR2.7	**Receive Code Select.** See Section 11 for more details. 0 = idle code (7F Hex) 1 = digital milliwatt code (1E/0B/0B/1E/9E/8B/8B/9E Hex)
0	RCR2.6	This control bit must be set to zero.
0	RCR2.5	This control bit must be set to zero.
0	RCR2.4	This control bit must be set to zero.
1	RCR2.3	This control bit must be set to one.
RD4YM	RCR2.2	**Receive Side D4 Yellow Alarm Select.** 0 = zeros in bit 2 of all channels 1 = a one in the S–bit position of frame 12
FSBE	RCR2.1	**PCVCR Fs–Bit Error Report Enable.** 0 = do not report bit errors in Fs–bit position; only Ft bit position 1 = report bit errors in Fs–bit position as well as Ft bit position
MOSCRF	RCR2.0	**Multiframe Out of Sync Count Register Function Select.** 0 = count errors in the framing bit position 1 = count the number of multiframes out of sync

TCR1: TRANSMIT CONTROL REGISTER 1 (Address=35 Hex)

(MSB)							(LSB)
LOTCMC	TFPT	TCPT	TSSE	GB7S	TFDLS	TBL	TYEL

SYMBOL	POSITION	NAME AND DESCRIPTION
LOTCMC	TCR1.7	**Loss Of Transmit Clock Mux Control.** Determines whether the transmit side formatter should switch to RCLK if the TCLK input should fail to transition (see Figure 1-1 for details). 0 = do not switch to RCLK if TCLK stops 1 = switch to RCLK if TCLK stops
TFPT	TCR1.6	**Transmit F–Bit Pass Through.** (see note below) 0 = F bits sourced internally 1 = F bits sampled at TSER
TCPT	TCR1.5	**Transmit CRC Pass Through.** (see note below) 0 = source CRC6 bits internally 1 = CRC6 bits sampled at TSER during F–bit time
TSSE	TCR1.4	**Software Signaling Insertion Enable.** (see note below) 0 = no signaling is inserted in any channel 1 = signaling is inserted in all channels from the TS1-TS12 registers (the TTR registers can be used to block insertion on a channel by channel basis)
GB7S	TCR1.3	**Global Bit 7 Stuffing.** (see note below) 0 = allow the TTR registers to determine which channels containing all zeros are to be Bit 7 stuffed 1 = force Bit 7 stuffing in all 0-byte channels regardless of how the TTR registers are programmed
TFDLS	TCR1.2	**TFDL Register Select.** (see note below) 0 = source FDL or Fs bits from the internal TFDL register (legacy FDL support mode) 1 = source FDL or Fs bits from the internal HDLC/BOC controller or TSER
TBL	TCR1.1	**Transmit Blue Alarm.** (see note below) 0 = transmit data normally 1 = transmit an unframed all one’s code at TNRZ
TYEL	TCR1.0	**Transmit Yellow Alarm.** (see note below) 0 = do not transmit yellow alarm 1 = transmit yellow alarm

NOTE:

For a description of how the bits in TCR1 affect the transmit side formatter, see Figure 20-5.

TCR2: TRANSMIT CONTROL REGISTER 2 (Address=36 Hex)

(MSB) **(LSB)**

0	0	0	0	0	TSIO	TD4YM	TB7ZS

SYMBOL	POSITION	NAME AND DESCRIPTION
0	TCR2.7	This control bit must be set to zero.
0	TCR2.6	This control bit must be set to zero.
0	TCR2.5	This control bit must be set to zero.
0	TCR2.4	This control bit must be set to zero.
0	TCR2.3	This control bit must be set to zero.
TSIO	TCR2.2	**TSYNC I/O Select.** This bit should only be set to one in Modes 12 & 13; it should be set to zero in all other Modes. 0 = TSYNC is an input 1 = TSYNC is an output (Mode 12 & 13 only)
TD4YM	TCR2.1	**Transmit Side D4 Yellow Alarm Select.** 0 = zeros in bit 2 of all channels 1 = a one in the S–bit position of frame 12
TB7ZS	TCR2.0	**Transmit Side Bit 7 Zero Suppression Enable.** 0 = no stuffing occurs 1 = Bit 7 force to a one in channels with all zeros

CCR1: COMMON CONTROL REGISTER 1 (Address=37 Hex)

(MSB) **(LSB)**

TESE	1	RSAO	1	1	RESE	PLB	FLB

SYMBOL	POSITION	NAME AND DESCRIPTION
TESE	CCR1.7	**Transmit Elastic Store Enable.** This bit should only be set to one in Modes 9 & 10; it should be set to zero in all other Modes. 0 = elastic store is bypassed 1 = elastic store is enabled (Modes 9 & 10 only)
1	CCR1.6	This control bit must be set to one.
RSAO	CCR1.5	**Receive Signaling All One's.** This bit should not be enabled if hardware signaling is being utilized. See Section 10 for more details. 0 = allow robbed signaling bits to appear at RSER 1 = force all robbed signaling bits at RSER to one
1	CCR1.4	This control bit must be set to one.
1	CCR1.3	This control bit must be set to one.
RESE	CCR1.2	**Receive Elastic Store Enable.** This bit should only be set to one in Modes 9 & 10; it should be set to zero in all other Modes. 0 = elastic store is bypassed 1 = elastic store is enabled (Modes 9 & 10 only)
PLB	CCR1.1	**Payload Loopback.** 0 = loopback disabled 1 = loopback enabled
FLB	CCR1.0	**Framer Loopback.** 0 = loopback disabled 1 = loopback enabled

Payload Loopback

When CCR1.1 is set to a one, the DS3120 will be forced into Payload LoopBack (PLB). Normally, this loopback is only enabled when ESF framing is being performed but can be enabled also in D4 framing applications. In a PLB situation, the DS3120 will loop the 192 bits of payload data from the receive section back to the transmit section. The FPS framing pattern, CRC6 calculation, and the FDL bits are not looped back, they are reinserted by the DS3120. When PLB is enabled, the following will occur:

1. data will be transmitted from TNRZ synchronous with RCLK instead of TCLK or CTCLK
2. all of the receive side signals will continue to operate normally
3. data at the TSER, and TSIG pins is ignored.

Framer Loopback

When CCR1.0 is set to a one, the DS3120 will enter a Framer LoopBack (FLB) mode. This loopback is useful in testing and debugging applications. In FLB, the DS3120 will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

1. an unframed all one's code will be transmitted at TNRZ
2. data at RNRZ will be ignored
3. RSER, RSIG, and RSYNC will take on timing synchronous with TCLK instead of RCLK

Please note that it is not acceptable to enable this loopback in Looped Timed Modes because this will cause an unstable condition.

CCR2: COMMON CONTROL REGISTER 2 (Address=38 Hex)

(MSB)							(LSB)
TFM	0	TSLC96	TZSE	RFM	EXZS	RSLC96	RZSE

SYMBOL	POSITION	NAME AND DESCRIPTION
TFM	CCR2.7	**Transmit Frame Mode Select.** 0 = D4 framing mode 1 = ESF framing mode
0	CCR2.6	This control bit must be set to zero.
TSLC96	CCR2.5	**Transmit SLC–96 / Fs–Bit Insertion Enable.** Only set this bit to a one in D4 framing applications. Must be set to one to source the Fs pattern. See Section 15 for details. 0 = SLC–96/Fs–bit insertion disabled 1 = SLC–96/Fs–bit insertion enabled
TZSE	CCR2.4	**Transmit FDL Zero Stuffer Enable.** Set this bit to zero if using the internal HDLC/BOC controller instead of the legacy support for the FDL. See Section 15 for details. 0 = zero stuffer disabled 1 = zero stuffer enabled
RFM	CCR2.3	**Receive Frame Mode Select.** 0 = D4 framing mode 1 = ESF framing mode
EXZS	CCR2.2	**EXcessive Zero (EXZ) Select.** 0 = 16 consecutive zeros 1 = 8 consecutive zeros
RSLC96	CCR2.1	**Receive SLC–96 Enable.** Only set this bit to a one in D4/SLC–96 framing applications. See Section 15 for details. 0 = SLC–96 disabled 1 = SLC–96 enabled
RZSE	CCR2.0	**Receive FDL Zero Destuffer Enable.** Set this bit to zero if using the internal HDLC/BOC controller instead of the legacy support for the FDL. See Section 15 for details. 0 = zero destuffer disabled 1 = zero destuffer enabled

CCR3: COMMON CONTROL REGISTER 3 (Address=30 Hex)

(MSB)							(LSB)
0	0	0	0	PDE	ECUS	TLOOP	0

SYMBOL	POSITION	NAME AND DESCRIPTION
0	CCR3.7	This control bit must be set to zero.
0	CCR3.6	This control bit must be set to zero.
0	CCR3.5	This control bit must be set to zero.
0	CCR3.4	This control bit must be set to zero.
PDE	CCR3.3	**Pulse Density Enforcer Enable.** 0 = disable transmit pulse density enforcer 1 = enable transmit pulse density enforcer
ECUS	CCR3.2	**Error Counter Update Select.** See Section 8 for details. 0 = update error counters once a second 1 = update error counters every 42 ms (333 frames)
TLOOP	CCR3.1	**Transmit Loop Code Enable.** See Section 16 for details. 0 = transmit data normally 1 = replace normal transmitted data with repeating code as defined in TCD register
0	CCR3.0	This control bit must be set to zero.

Pulse Density Enforcer

The Framer always examines both the transmit and receive data streams for violations of the following rules which are required by ANSI T1.403:

– no more than 15 consecutive zeros
– at least N ones in each and every time window of 8 x (N +1) bits where N = 1 through 23

Violations for the transmit and receive data streams are reported in the RIR2.0 and RIR2.1 bits respectively. When the CCR3.3 is set to one, the DS3120 will force the transmitted stream to meet this requirement no matter the content of the transmitted stream.

CCR4: COMMON CONTROL REGISTER 4 (Address=11 Hex)

(MSB) **(LSB)**

0	RPCSI	RFSA1	RFE	RFF	THSE	TPCSI	TIRFS

SYMBOL	POSITION	NAME AND DESCRIPTION
0	CCR4.7	This control bit must be set to zero.
RPCSI	CCR4.6	**Receive Per-Channel Stuffing Insert.** See Sections 10 & 12 for more details. 0 = do not use RCHBLK to determine which channels should be stuffed to one. 1 = use RCHBLK to determine which channels should be stuffed to one.
RFSA1	CCR4.5	**Receive Force Signaling All Ones.** See Section 10 for more details. 0 = do not force extracted robbed–bit signaling bit positions to a one 1 = force extracted robbed–bit signaling bit positions to a one
RFE	CCR4.4	**Receive Freeze Enable.** See Section 10 for details. 0 = no freezing of receive signaling data will occur 1 = allow freezing of receive signaling data at RSIG.
RFF	CCR4.3	**Receive Force Freeze.** Freezes receive side signaling at RSIG; will override Receive Freeze Enable (RFE). See Section 10 for details. 0 = do not force a freeze event 1 = force a freeze event
THSE	CCR4.2	**Transmit Hardware Signaling Insertion Enable.** See Sections 10 & 12 for details. 0 = do not insert signaling from the TSIG pin into the data stream presented at the TSER pin. 1 = Insert the signaling from the TSIG pin into data stream presented at the TSER pin.
TPCSI	CCR4.1	**Transmit Per–Channel Signaling Insert.** See Section 10 for details. 0 = do not use TCHBLK to determine which channels should have signaling inserted from the TSIG pin. 1 = use TCHBLK to determine which channels should have signaling inserted from the TSIG pin.
TIRFS	CCR4.0	**Transmit Idle Registers (TIR) Function Select.** See Section 11 for timing details. 0 = TIRs define in which channels to insert idle code 1 = TIRs define in which channels to insert data from RSER (i.e., Per = Channel Loopback function)

CCR5: COMMON CONTROL REGISTER 5 (Address=19 Hex)

(MSB) **(LSB)**

TJC	–	–	TCM4	TCM3	TCM2	TCM1	TCM0

SYMBOL	POSITION	NAME AND DESCRIPTION
TJC	CCR5.7	**Transmit Japanese CRC6 Enable.** 0 = use ANSI/AT&T/ITU CRC6 calculation (normal operation) 1 = use Japanese standard JT–G704 CRC6 calculation
–	CCR5.6	**Not Assigned.** Must be set to zero when written.
–	CCR5.5	**Not Assigned.** Must be set to zero when written.
TCM4	CCR5.4	**Transmit Channel Monitor Bit 4.** MSB of a channel decode that determines which transmit channel data will appear in the TDS0M register. See Section 9 for details.
TCM3	CCR5.3	**Transmit Channel Monitor Bit 3.**
TCM2	CCR5.2	**Transmit Channel Monitor Bit 2.**
TCM1	CCR5.1	**Transmit Channel Monitor Bit 1.**
TCM0	CCR5.0	**Transmit Channel Monitor Bit 0.** LSB of the channel decode.

CCR6: COMMON CONTROL REGISTER 6 (Address=1E Hex)

(MSB) **(LSB)**

RJC	RESALGN	TESALGN	RCM4	RCM3	RCM2	RCM1	RCM0

SYMBOL	POSITION	NAME AND DESCRIPTION
RJC	CCR6.7	**Receive Japanese CRC6 Enable.** 0 = use ANSI/AT&T/ITU CRC6 calculation (normal operation) 1 = use Japanese standard JT–G704 CRC6 calculation
RESALGN	CCR6.6	**Receive Elastic Store Align.** Setting this bit from a zero to a one may force the receive elastic store’s write/read pointers to a minimum separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less then half a frame, the command will be executed and data will be disrupted. Should be toggled after 8MCLKI has been applied and is stable. Must be cleared and set again for a subsequent align. See Section 13 for details.
TESALGN	CCR6.5	**Transmit Elastic Store Align.** Setting this bit from a zero to a one may force the transmit elastic store’s write/read pointers to a minimum separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less then half a frame, the command will be executed and data will be disrupted. Should be toggled after 8MCLKI has been applied and is stable. Must be cleared and set again for a subsequent align. See Section 13 for details.
RCM4	CCR6.4	**Receive Channel Monitor Bit 4.** MSB of a channel decode that determines which receive channel data will appear in the RDS0M register. See Section 9 for details.

SYMBOL	POSITION	NAME AND DESCRIPTION
RCM3	CCR6.3	**Receive Channel Monitor Bit 3.**
RCM2	CCR6.2	**Receive Channel Monitor Bit 2.**
RCM1	CCR6.1	**Receive Channel Monitor Bit 1.**
RCM0	CCR6.0	**Receive Channel Monitor Bit 0**. LSB of the channel decode.

CCR7: COMMON CONTROL REGISTER 7 (Address=0A Hex)

(MSB) **(LSB)**

–	RLB	RESR	TESR	–	–	–	–

SYMBOL	POSITION	NAME AND DESCRIPTION
–	CCR7.7	**Not Assigned.** Should be set to zero when written to.
RLB	CCR7.6	**Remote Loopback.** 0 = loopback disabled 1 = loopback enabled
RESR	CCR7.5	**Receive Elastic Store Reset.** Setting this bit from a zero to a one will force the receive elastic store to a depth of one frame. Receive data is lost during the reset. Should be toggled after 8MCLKI has been applied and is stable. Do not leave this bit set high.
TESR	CCR7.4	**Transmit Elastic Store Reset.** Setting this bit from a zero to a one will force the transmit elastic store to a depth of one frame. Transmit data is lost during the reset. Should be toggled after 8MCLKI has been applied and is stable. Do not leave this bit set high.
–	CCR7.3	**Not Assigned.** Should be set to zero when written to.
–	CCR7.2	**Not Assigned.** Should be set to zero when written to.
–	CCR7.1	**Not Assigned.** Should be set to zero when written to.
–	CCR7.0	**Not Assigned.** Should be set to zero when written to.

Remote Loopback

When CCR7.6 is set to a one, the DS3120 will be forced into Remote LoopBack (RLB). In this loopback, data input via the RNRZ signal will be transmitted back to TNRZ. Data will continue to pass through the receive side framer of the DS3120 as it would normally and the data from the transmit side formatter will be ignored. Please see Figure 1-1 for more details.

7. STATUS AND INFORMATION REGISTERS

There is a set of nine registers per channel that contain information on the current real time status of a framer in the DS3120, Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Registers 1 to 3 (RIR1/RIR2/RIR3) and a set of four registers for the onboard HDLC and BOC controller. The specific details on the four registers pertaining to the HDLC and BOC controller are covered in Section 15 but they operate the same as the other status registers in the DS3120 and this operation is described below.

When a particular event has occurred (or is occurring), the appropriate bit in one of these nine registers will be set to a one. All of the bits in SR1, SR2, RIR1, RIR2, and RIR3 registers operate in a latched fashion. This means that if an event or an alarm occurs and a bit is set to a one in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again (or in the case of the RBL, RYEL, LRCL, and RLOS alarms, the bit will remain set if the alarm is still present). There are bits in the four HDLC and BOC status registers that are not latched and these bits are listed in Section 14.

The user will always precede a read of any of the nine registers with a write. The byte written to the register will inform the DS3120 which bits the user wishes to read and have cleared. The user will write a byte to one of these registers, with a one in the bit positions he or she wishes to read and a zero in the bit positions he or she does not wish to obtain the latest information on. When a one is written to a bit location, the read register will be updated with the latest information. When a zero is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This write–read– write scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS3120 with higher–order software languages.

The SR1, SR2, and HSR registers have the unique ability to initiate a hardware interrupt via the INT* output pin. Each of the alarms and events in the SR1, SR2, and HSR can be either masked or unmasked from the interrupt pin via the Interrupt Mask Register 1 (IMR1), Interrupt Mask Register 2 (IMR2), and HDLC Interrupt Mask Register (HIMR) respectively. The HIMR register is covered in Section 14. The Interrupt Status Registers (IMR1/2/3/4) can be used to determine which framer is requesting interrupt servicing.

The interrupts caused by alarms in SR1 (namely RYEL, RCL, RBL, RLOS and LOTC) act differently than the interrupts caused by events in SR1 and SR2 (namely LUP, LDN, RSLIP, RMF, TMF, SEC, RFDL, TFDL, RMTCH, RAF, and RSC) and HIMR. The alarm caused interrupts will force the INT* pin low whenever the alarm changes state (i.e., the alarm goes active or inactive according to the set/clear criteria in Table 7-1). The INT* pin will be allowed to return high (if no other interrupts are present) when the user reads the alarm bit that caused the interrupt to occur even if the alarm is still present.

The event caused interrupts will force the INT* pin low when the event occurs. The INT* pin will be allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

Interrupt Status Registers

Interrupt Status Registers 1 to 4 report the real time status on the interrupts from each T1 framer. Figure 7-1 provides a visual description of the signal flow to each bit in the ISR1 register. The other ISR registers are similar.

ISR1: INTERRUPT STATUS REGISTER1

(Address 00 Hex when FS0 to FS4 = 11111)

(MSB)							(LSB)
FR8	FR7	FR6	FR5	FR4	FR3	FR2	FR1

ISR2: INTERRUPT STATUS REGISTER2

(Address 01 Hex when FS0 to FS4 = 11111)

(MSB)							(LSB)
FR16	FR15	FR14	FR13	FR12	FR11	FR10	FR9

ISR3: INTERRUPT STATUS REGISTER3

(Address 02 Hex when FS0 to FS4 = 11111)

(MSB)							(LSB)
FR24	FR23	FR22	FR21	FR20	FR19	FR18	FR17

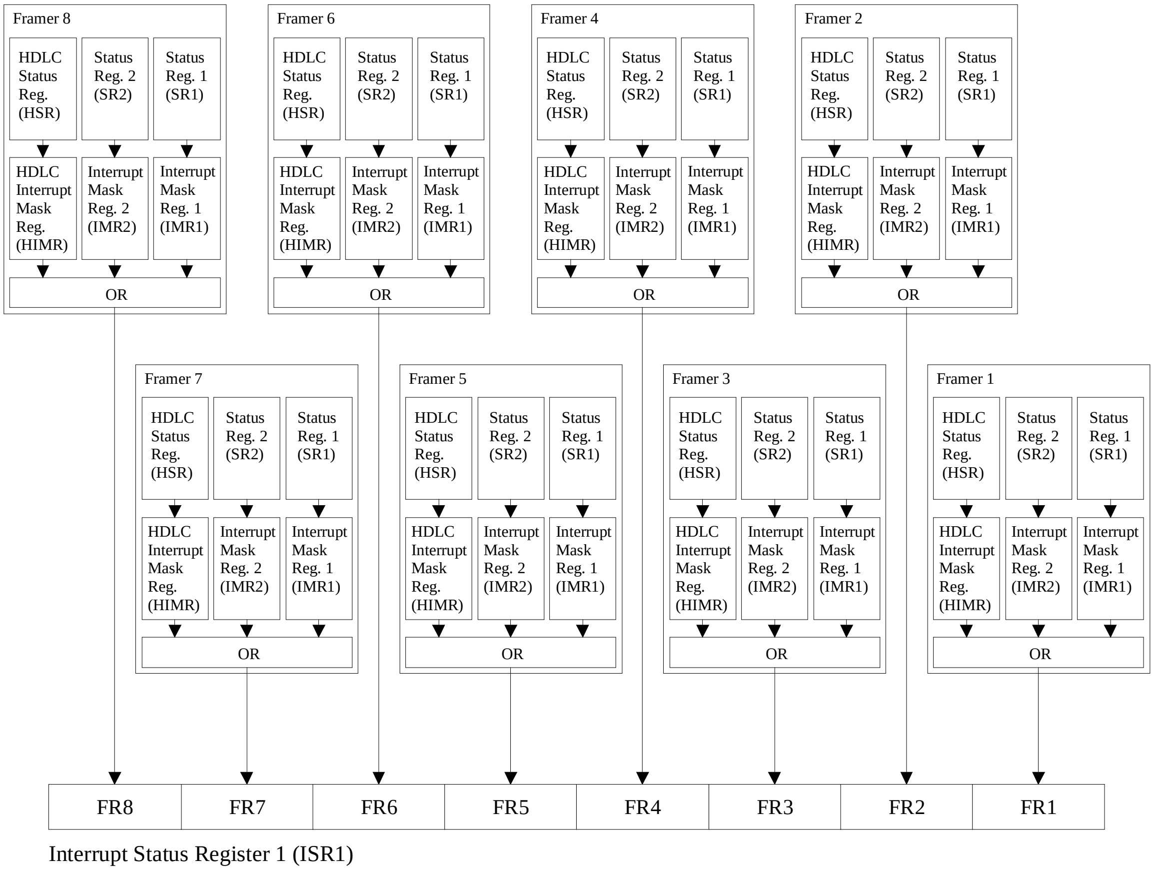
ISR4: INTERRUPT STATUS REGISTER4

(Address 03 Hex when FS0 to FS4 = 11111)

(MSB)							(LSB)
-	-	-	-	FR28	FR27	FR26	FR25

SYMBOL	POSITION	NAME AND DESCRIPTION
FRn (where n = 1 to 28)	ISRi.j (where i = 1 to 4; j = 1 to 7)	**FRAMER n (n = 1 to 28) INTERRUPT REQUEST.** 0 = No interrupt request pending. 1 = Interrupt request pending.
-	ISR4.j (where j = 4 to 7)	**NOT ASSIGNED.** Could be any value when read.

Interrupt Status Register 1 Signal Flow Figure 7-1



RIR1: RECEIVE INFORMATION REGISTER 1 (Address=22 Hex)

(MSB)							(LSB)
COFA	8ZD	16ZD	RESF	RESE	SEFE	-	FBE

SYMBOL	POSITION	NAME AND DESCRIPTION
COFA	RIR1.7	**Change of Frame Alignment.** Set when the last resync resulted in a change of frame or multiframe alignment.
8ZD	RIR1.6	**Eight Zero Detect.** Set when a string of at least eight consecutive zeros (regardless of the length of the string) have been received at RPOS and RNEG.
16ZD	RIR1.5	**Sixteen Zero Detect.** Set when a string of at least sixteen consecutive zeros (regardless of the length of the string) have been received at RPOS and RNEG.
RESF	RIR1.4	**Receive Elastic Store Full.** Set when the receive elastic store buffer fills and a frame is deleted.
RESE	RIR1.3	**Receive Elastic Store Empty.** Set when the receive elastic store buffer empties and a frame is repeated.
SEFE	RIR1.2	**Severely Errored Framing Event.** Set when 2 out of 6 framing bits (Ft or FPS) are received in error.
-	RIR1.1	This status bit is not assigned and could be any value when read.
FBE	RIR1.0	**Frame Bit Error.** Set when a Ft (D4) or FPS (ESF) framing bit is received in error.

RIR2: RECEIVE INFORMATION REGISTER 2 (Address=31 Hex)

(MSB)							(LSB)
RLOSC	RCLC	TESF	TESE	TSLIP	RBLC	RPDV	TPDV

SYMBOL	POSITION	NAME AND DESCRIPTION
RLOSC	RIR2.7	**Receive Loss of Sync Clear.** Set when the framer achieves synchronization; will remain set until read.
RCLC	RIR2.6	**Receive Carrier Loss Clear.** Set when the carrier signal is restored; will remain set until read. See Table 7-1.
TESF	RIR2.5	**Transmit Elastic Store Full.** Set when the transmit elastic store buffer fills and a frame is deleted.
TESE	RIR2.4	**Transmit Elastic Store Empty.** Set when the transmit elastic store buffer empties and a frame is repeated.
TSLIP	RIR2.3	**Transmit Elastic Store Slip Occurrence.** Set when the transmit elastic store has either repeated or deleted a frame.
RBLC	RIR2.2	**Receive Blue Alarm Clear.** Set when the Blue Alarm (AIS) is no longer detected; will remain set until read. See Table 7-1.
RPDV	RIR2.1	**Receive Pulse Density Violation.** Set when the receive data stream does not meet the ANSI T1.403 requirements for pulse density.
TPDV	RIR2.0	**Transmit Pulse Density Violation.** Set when the transmit data stream does not meet the ANSI T1.403 requirements for pulse density.

RIR3: RECEIVE INFORMATION REGISTER 3 (Address=10 Hex)

(MSB) **(LSB)**

–	–	–	LORC	–	–	–	RAIS-CI

SYMBOL	POSITION	NAME AND DESCRIPTION
–	RIR3.7	**Not Assigned.** Could be any value when read.
–	RIR3.6	**Not Assigned.** Could be any value when read.
–	RIR3.5	**Not Assigned.** Could be any value when read.
LORC	RIR3.4	**Loss of Receive Clock.** Set when the RCLK signal has not transitioned for at least 2 us (3 us ± 1 us).
–	RIR3.3	**Not Assigned.** Could be any value when read.
–	RIR3.2	**Not Assigned.** Could be any value when read.
–	RIR3.1	**Not Assigned.** Could be any value when read.
RAIS-CI	RIR3.0	**Receive AIS-CI Detect.** Set when the AIS-CI pattern is detected.

SR1: STATUS REGISTER 1 (Address=20 Hex)

(MSB) **(LSB)**

LUP	LDN	LOTC	RSLIP	RBL	RYEL	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
LUP	SR1.7	**Loop Up Code Detected.** Set when the loop up code as defined in the RUPCD register is being received. See Section 16 for details.
LDN	SR1.6	**Loop Down Code Detected.** Set when the loop down code as defined in the RDNCD register is being received. See Section 16 for details.
LOTC	SR1.5	**Loss of Transmit Clock.** Set when the TCLK pin has not transitioned for one channel time (or 5.2 us). Will force transmit side formatter to switch to RCLK if so enabled via TCR1.7.
RSLIP	SR1.4	**Receive Elastic Store Slip Occurrence.** Set when the receive elastic store has either repeated or deleted a frame.
RBL	SR1.3	**Receive Blue Alarm.** Set when an unframed all one's code is received at RNRZ.
RYEL	SR1.2	**Receive Yellow Alarm.** Set when a yellow alarm is received at RNRZ.
RCL	SR1.1	**Receive Carrier Loss.** Set when a red alarm is received at RNRZ.
RLOS	SR1.0	**Receive Loss of Sync.** Set when the device is not synchronized to the receive T1 stream.

ALARM CRITERIA Table 7-1

ALARM	SET CRITERIA	CLEAR CRITERIA
Blue Alarm (AIS) (see note 1 below)	when over a 3 ms window, 5 or less zeros are received	when over a 3 ms window, 6 or more zeros are received
Yellow Alarm (RAI) 1. D4 bit 2 mode(RCR2.2=0) 2. D4 12th F–bit mode (RCR2.2=1; this mode is also referred to as the “Japanese Yellow Alarm”) 3. ESF mode	when bit 2 of 256 consecutive channels is set to zero for at least 254 occurrences when the 12th framing bit is set to one for two consecutive occurrences when 16 consecutive patterns of 00FF appear in the FDL	when bit 2 of 256 consecutive channels is set to zero for less than 254 occurrences when the 12th framing bit is set to zero for two consecutive occurrences when 14 or less patterns of 00FF hex out of 16 possible appear in the FDL
Red Alarm (RCL) (this alarm is also referred to as Loss Of Signal)	when 192 consecutive zeros are received	when 14 or more ones out of 112 possible bit positions are received starting with the first one received

NOTES:

1. The definition of Blue Alarm (or Alarm Indication Signal) is an unframed all ones signal. Blue alarm detectors should be able to operate properly in the presence of a 10–3 error rate and they should not falsely trigger on a framed all ones signal. The blue alarm criteria in the DS3120 has been set to achieve this performance. It is recommended that the RBL bit be qualified with the RLOS bit.

2. ANSI specifications use a different nomenclature than the DS3120 does; the following terms are equivalent:

RBL = AIS
RCL = LOS
RLOS = LOF
RYEL = RAI

SR2: STATUS REGISTER 2 (Address=21 Hex)

(MSB)							(LSB)
RMF	TMF	SEC	RFDL	TFDL	RMTCH	RAF	RSC

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	SR2.7	**Receive Multiframe.** Set on receive multiframe boundaries.
TMF	SR2.6	**Transmit Multiframe.** Set on transmit multiframe boundaries.
SEC	SR2.5	**One Second Timer.** Set on increments of one second based on RCLK; will be set in increments of 999 ms, 999 ms, and 1002 ms every 3 seconds (or every 42 ms if CCR3.2 = 1).
RFDL	SR2.4	**Receive FDL Buffer Full.** Set when the receive FDL buffer (RFDL) fills to capacity (8 bits).
TFDL	SR2.3	**Transmit FDL Buffer Empty.** Set when the transmit FDL buffer (TFDL) empties.
RMTCH	SR2.2	**Receive FDL Match Occurrence.** Set when the RFDL matches either RMTCH1 or RMTCH2.
RAF	SR2.1	**Receive FDL Abort.** Set when eight consecutive one's are received in the FDL.
RSC	SR2.0	**Receive Signaling Change.** Set when the DS3120 detects a change of state in any of the robbed–bit signaling bits.

IMR1: INTERRUPT MASK REGISTER 1 (Address=7F Hex)

(MSB)							(LSB)
LUP	LDN	LOTC	SLIP	RBL	RYEL	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
LUP	IMR1.7	**Loop Up Code Detected.** 0 = interrupt masked 1 = interrupt enabled
LDN	IMR1.6	**Loop Down Code Detected.** 0 = interrupt masked 1 = interrupt enabled
LOTC	IMR1.5	**Loss of Transmit Clock.** 0 = interrupt masked 1 = interrupt enabled
SLIP	IMR1.4	**Elastic Store Slip Occurrence.** 0 = interrupt masked 1 = interrupt enabled
RBL	IMR1.3	**Receive Blue Alarm.** 0 = interrupt masked 1 = interrupt enabled
RYE	IMR1.2	**Receive Yellow Alarm.** 0 = interrupt masked 1 = interrupt enabled

SYMBOL	POSITION	NAME AND DESCRIPTION
RCL	IMR1.1	**Receive Carrier Loss.** 0 = interrupt masked 1 = interrupt enabled
RLOS	IMR1.0	**Receive Loss of Sync.** 0 = interrupt masked 1 = interrupt enabled

IMR2: INTERRUPT MASK REGISTER 2 (Address=6F Hex)

(MSB) **(LSB)**

RMF	TMF	SEC	RFDL	TFDL	RMTCH	RAF	RSC

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	IMR2.7	**Receive Multiframe.** 0 = interrupt masked 1 = interrupt enabled
TMF	IMR2.6	**Transmit Multiframe.** 0 = interrupt masked 1 = interrupt enabled
SEC	IMR2.5	**One Second Timer.** 0 = interrupt masked 1 = interrupt enabled
RFDL	IMR2.4	**Receive FDL Buffer Full.** 0 = interrupt masked 1 = interrupt enabled
TFDL	IMR2.3	**Transmit FDL Buffer Empty.** 0 = interrupt masked 1 = interrupt enabled
RMTCH	IMR2.2	**Receive FDL Match Occurrence.** 0 = interrupt masked 1 = interrupt enabled
RAF	IMR2.1	**Receive FDL Abort.** 0 = interrupt masked 1 = interrupt enabled
RSC	IMR2.0	**Receive Signaling Change.** 0 = interrupt masked 1 = interrupt enabled

8. ERROR COUNT REGISTERS

There are a set of three counters in each framer that record EXcessive Zeros (EXZ), errors in the CRC6 code words, framing bit errors, and number of multiframes that the device is out of receive synchronization. Each of these three counters are automatically updated on either one second boundaries (CCR3.2=0) or every 42 ms (CCR3.2=1) as determined by the timer in Status Register 2 (SR2.5). Hence, these registers contain performance data from either the previous second or the previous 42 ms. The user can use the interrupt from the one second (or 42 ms) timer to determine when to read these registers. The user has a full second (or 42 ms) to read the counters before the data is lost. All three counters will saturate at their respective maximum counts and they will not rollover.

Line Code Violation Count Register (LCVCR)

Line Code Violation Count Register 1 (LCVCR1) is the most significant word and LCVCR2 is the least significant word of a 16–bit counter that records code violations (CVs). CVs are defined as EXcessive Zeros (EXZ). See Table 8-1 for details of exactly what the LCVCRs count This counter is always enabled; it is not disabled during receive loss of synchronization (RLOS=1) conditions.

LCVCR1: LINE CODE VIOLATION COUNT REGISTER 1 (Address = 23 Hex)
LCVCR2: LINE CODE VIOLATION COUNT REGISTER 2 (Address = 24 Hex)

(MSB)							(LSB)	
LCV15	LCV14	LCV13	LCV12	LCV11	LCV10	LCV9	LCV8	LCVCR1
LCV7	LCV6	LCV5	LCV4	LCV3	LCV2	LCV1	LCV0	LCVCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
LCV15	LCVCR1.7	**MSB of the 16–bit code violation count**
LCV0	LCVCR2.0	**LSB of the 16–bit code violation count**

LINE CODE VIOLATION COUNTING ARRANGEMENTS Table 8-1

EXcessive Zero Select (CCR2.2)	WHAT IS COUNTED IN THE LCVCRs
0	16 consecutive zero occurrences
1	8 consecutive zeros occurrences

Path Code Violation Count Register (PCVCR)

When the receive side of a framer is set to operate in the ESF framing mode (CCR2.3=1), PCVCR will automatically be set as a 12–bit counter that will record errors in the CRC6 code words. When set to operate in the D4 framing mode (CCR2.3=0), PCVCR will automatically count errors in the Ft framing bit position. Via the RCR2.1 bit, a framer can be programmed to also report errors in the Fs framing bit position. The PCVCR will be disabled during receive loss of synchronization (RLOS=1) conditions. See Table 8-2 for a detailed description of exactly what errors the PCVCR counts.

PCVCR1: PATH VIOLATION COUNT REGISTER 1 (Address = 25 Hex)
PCVCR2: PATH VIOLATION COUNT REGISTER 2 (Address = 26 Hex)

(MSB)							(LSB)	
(note 1)	(note 1)	(note 1)	(note 1)	CRC/ FB11	CRC/ FB10	CRC/ FB9	CRC/ FB8	PCVCR1
CRC/ FB7	CRC/ FB6	CRC/ FB5	CRC/ FB4	CRC/ FB3	CRC/ FB2	CRC/ FB1	CRC/ FB0	PCVCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC/FB11	PCVCR1.3	**MSB of the 12–Bit CRC6 Error or Frame Bit Error Count** (note #2)
CRC/FB0	PCVCR2.0	**LSB of the 12–Bit CRC6 Error or Frame Bit Error Count** (note #2)

NOTES:

1. The upper nibble of the counter at address 25h is used by the Multiframes Out of Sync Count Register
3. PCVCR counts either errors in CRC code words (in the ESF framing mode; CCR2.3=1) or errors in the framing bit position (in the D4 framing mode; CCR2.3=0).

PATH CODE VIOLATION COUNTING ARRANGEMENTS Table 8-2

FRAMING MODE (CCR2.3)	COUNT Fs ERRORS? (RCR2.1)	WHAT IS COUNTED IN THE PCVCRs
D4	no	errors in the Ft pattern
D4	yes	errors in both the Ft & Fs patterns
ESF	don’t care	errors in the CRC6 code words

MULTIFRAMES OUT OF SYNC COUNT REGISTER (MOSCR)

Normally the MOSCR is used to count the number of multiframes that the receive synchronizer is out of sync (RCR2.0=1). This number is useful in ESF applications needing to measure the parameters Loss Of Frame Count (LOFC) and ESF Error Events as described in AT&T publication TR54016. When the MOSCR is operated in this mode, it is not disabled during receive loss of synchronization (RLOS=1) conditions. The MOSCR has alternate operating mode whereby it will count either errors in the Ft framing pattern (in the D4 mode) or errors in the FPS framing pattern (in the ESF mode). When the MOSCR is operated in this mode, it is disabled during receive loss of synchronization (RLOS = 1) conditions. See Table 8-3 for a detailed description of what the MOSCR is capable of counting.

MOSCR1: MULTIFRAMES OUT OF SYNC COUNT REGISTER 1

(Address = 25 Hex)

MOSCR2: MULTIFRAMES OUT OF SYNC COUNT REGISTER 2

(Address = 27 Hex)

(MSB)							(LSB)	
MOS/FB11	MOS/FB10	MOS/FB9	MOS/FB8	(note 1)	(note 1)	(note 1)	(note 1)	MOSCR 1
MOS/FB7	MOS/FB6	MOS/FB5	MOS/FB4	MOS/FB3	MOS/FB2	MOS/FB1	MOS/FB0	MOSCR 2

SYMBOL	POSITION	NAME AND DESCRIPTION
MOS/FB11	MOSCR1.7	**MSB of the 12–Bit Multiframes Out of Sync or F–Bit Error Count** (note #2)
MOS/FB0	MOSCR2.0	**LSB of the 12–Bit Multiframes Out of Sync or F–Bit Error Count** (note #2)

NOTES:

1. The lower nibble of the counter at address 25h is used by the Path Code Violation Count Register
2. MOSCR counts either errors in framing bit position (RCR2.0=0) or the number of multiframes out of sync (RCR2.0=1)

MULTIFRAMES OUT OF SYNC COUNTING ARRANGEMENTS Table 8-3

FRAMING MODE (CCR2.3)	COUNT MOS OR F–BIT ERRORS (RCR2.0)	WHAT IS COUNTED IN THE MOSCRs
D4	MOS	number of multiframes out of sync
D4	F–Bit	errors in the Ft pattern
ESF	MOS	number of multiframes out of sync
ESF	F–Bit	errors in the FPS pattern

9. DS0 MONITORING FUNCTION

Each framer in the DS3120 has the ability to monitor one DS0 64 Kbps channel in the transmit direction and one DS0 channel in the receive direction at the same time. In the transmit direction the user will determine which channel is to be monitored by properly setting the TCM0 to TCM4 bits in the CCR5 register. In the receive direction, the RCM0 to RCM4 bits in the CCR6 register need to be properly set. The DS0 channel pointed to by the TCM0 to TCM4 bits will appear in the Transmit DS0 Monitor (TDS0M) register and the DS0 channel pointed to by the RCM0 to RCM4 bits will appear in the Receive DS0 (RDS0M) register. The TCM4 to TCM0 and RCM4 to RCM0 bits should be programmed with the decimal decode of the appropriate T1 channel. Channels 1 through 24 map to register values 0 through 23. For example, if DS0 channel 6 (timeslot 5) in the transmit direction and DS0 channel 15 (timeslot 14) in the receive direction needed to be monitored, then the following values would be programmed into CCR5 and CCR6:

TCM4 = 0	RCM4 = 0
TCM3 = 0	RCM3 = 1
TCM2 = 1	RCM2 = 1
TCM1 = 0	RCM1 = 1
TCM0 = 1	RCM0 = 0

CCR5: COMMON CONTROL REGISTER 5 (Address=19 Hex)

[repeated here from Section 6 for convenience]

(MSB)							(LSB)
TJC	–	–	TCM4	TCM3	TCM2	TCM1	TCM0

SYMBOL	POSITION	NAME AND DESCRIPTION
TJC	CCR5.7	**Transmit Japanese CRC Enable.** See Section 6 for details.
–	CCR5.5	**Not Assigned.** Must be set to zero when written.
–	CCR5.5	**Not Assigned.** Must be set to zero when written.
TCM4	CCR5.4	**Transmit Channel Monitor Bit 4.** MSB of a channel decode that determines which transmit DS0 channel data will appear in the TDS0M register.
TCM3	CCR5.3	**Transmit Channel Monitor Bit 3.**
TCM2	CCR5.2	**Transmit Channel Monitor Bit 2.**
TCM1	CCR5.1	**Transmit Channel Monitor Bit 1.**
TCM0	CCR5.0	**Transmit Channel Monitor Bit 0.** LSB of the channel decode that determines which transmit DS0 channel data will appear in the TDS0M register.

TDS0M: TRANSMIT DS0 MONITOR REGISTER (Address=1A Hex)

(MSB) **(LSB)**

B1	B2	B3	B4	B5	B6	B7	B8

SYMBOL	POSITION	NAME AND DESCRIPTION
B1	TDS0M.7	**Transmit DS0 Channel Bit 1.** MSB of the DS0 channel (first bit to be transmitted).
B2	TDS0M.6	**Transmit DS0 Channel Bit 2.**
B3	TDS0M.5	**Transmit DS0 Channel Bit 3.**
B4	TDS0M.4	**Transmit DS0 Channel Bit 4.**
B5	TDS0M.3	**Transmit DS0 Channel Bit 5.**
B6	TDS0M.2	**Transmit DS0 Channel Bit 6.**
B7	TDS0M.1	**Transmit DS0 Channel Bit 7.**
B8	TDS0M.0	**Transmit DS0 Channel Bit 8.** LSB of the DS0 channel (last bit to be transmitted).

CCR6: COMMON CONTROL REGISTER 6 (Address=1E Hex)

[repeated here from Section 6 for convenience]

(MSB) **(LSB)**

RJC	RESALGN	TESALGN	RCM4	RCM3	RCM2	RCM1	RCM0

SYMBOL	POSITION	NAME AND DESCRIPTION
RJC	CCR6.7	**Receive Japanese CRC6 Enable.** 0 = use ANSI/AT&T/ITU CRC6 calculation (normal operation) 1 = use Japanese standard JT–G704 CRC6 calculation
RESALGN	CCR6.6	**Receive Elastic Store Align.** Setting this bit from a zero to a one will force the receive elastic store's write/read pointers to a minim separation of half a frame. If pointer separation is already greater than half a frame, setting this bit will have no effect. Should be toggled after 8MCLKI has been applied and is stable. Must be cleared and set again for a subsequent align. See Section 13 for details.
TESALGN	CCR6.5	**Transmit Elastic Store Align.** Setting this bit from a zero to a one will force the transmit elastic store's write/read pointers to a minimum separation of half a frame. If pointer separation is already greater than half a frame, setting this bit will have no effect. Should be toggled after 8MCLKI has been applied and is stable. Must be cleared and set again for a subsequent align. See Section 13 for details.
RCM4	CCR6.4	**Receive Channel Monitor Bit 4.** MSB of a channel decode that determines which receive channel data will appear in the RDS0M register.
RCM3	CCR6.3	**Receive Channel Monitor Bit 3.**
RCM2	CCR6.2	**Receive Channel Monitor Bit 2.**
RCM1	CCR6.1	**Receive Channel Monitor Bit 1.**

SYMBOL	POSITION	NAME AND DESCRIPTION
RCM0	CCR6.0	**Receive Channel Monitor Bit 0**. LSB of the channel decode.

RDS0M: RECEIVE DS0 MONITOR REGISTER (Address=1F Hex)

(MSB)							(LSB)
B1	B2	B3	B4	B5	B6	B7	B8

SYMBOL	POSITION	NAME AND DESCRIPTION
B1	RDS0M.7	**Receive DS0 Channel Bit 1.** MSB of the DS0 channel (first bit received).
B2	RDS0M.6	**Receive DS0 Channel Bit 2.**
B3	RDS0M.5	**Receive DS0 Channel Bit 3.**
B4	RDS0M.4	**Receive DS0 Channel Bit 4.**
B5	RDS0M.3	**Receive DS0 Channel Bit 5.**
B6	RDS0M.2	**Receive DS0 Channel Bit 6.**
B7	RDS0M.1	**Receive DS0 Channel Bit 7.**
B8	RDS0M.0	**Receive DS0 Channel Bit 8.** LSB of the DS0 channel (last bit received).

10. SIGNALING OPERATION

Each framer in the DS3120 contains provisions for both processor based (i.e., software based) signaling bit access and for hardware based access. Both the processor based access and the hardware based access can be used simultaneously if necessary. The processor based signaling is covered in Section 10.1 and the hardware based signaling is covered in Section 10.2. Hardware based signaling is only available in Modes 5 through 10. See Section 3 for more details on the different modes of operation for the DS3120. Processor based signaling is available in all modes of operation.

10.1 PROCESSOR BASED SIGNALING

The robbed–bit signaling bits embedded in the T1 stream can be extracted from the receive stream and inserted into the transmit stream by each framer. There is a set of 12 registers for the receive side (RS1 to RS12) and 12 registers on the transmit side (TS1 to TS12). The signaling registers are detailed below. The CCR1.5 bit is used to control the robbed signaling bits as they appear at RSER. If CCR1.5 is set to zero, then the robbed signaling bits will appear at the RSER pin in their proper position as they are received. If CCR1.5 is set to a one, then the robbed signaling bit positions will be forced to a one at RSER. If hardware based signaling is being used, then CCR1.5 must be set to zero.

RS1 TO RS12: RECEIVE SIGNALING REGISTERS (Address=60 to 6B Hex)

(MSB)							(LSB)	
A(8)	A(7)	A(6)	A(5)	A(4)	A(3)	A(2)	A(1)	RS1 (60)
A(16)	A(15)	A(14)	A(13)	A(12)	A(11)	A(10)	A(9)	RS2 (61)
A(24)	A(23)	A(22)	A(21)	A(20)	A(19)	A(18)	A(17)	RS3 (62)
B(8)	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)	B(1)	RS4 (63)
B(16)	B(15)	B(14)	B(13)	B(12)	B(11)	B(10)	B(9)	RS5 (64)
B(24)	B(23)	B(22)	B(21)	B(20)	B(19)	B(18)	B(17)	RS6 (65)
A/C(8)	A/C(7)	A/C(6)	A/C(5)	A/C(4)	A/C(3)	A/C(2)	A/C(1)	RS7 (66)
A/C(16)	A/C(15)	A/C(14)	A/C(13)	A/C(12)	A/C(11)	A/C(10)	A/C(9)	RS8 (67)
A/C(24)	A/C(23)	A/C(22)	A/C(21)	A/C(20)	A/C(19)	A/C(18)	A/C(17)	RS9 (68)
B/D(8)	B/D(7)	B/D(6)	B/D(5)	B/D(4)	B/D(3)	B/D(2)	B/D(1)	RS10 (69)
B/D(16)	B/D(15)	B/D(14)	B/D(13)	B/D(12)	B/D(11)	B/D(10)	B/D(9)	RS11 (6A)
B/D(24)	B/D(23)	B/D(22)	B/D(21)	B/D(20)	B/D(19)	B/D(18)	B/D(17)	RS12 (6B)

SYMBOL	POSITION	NAME AND DESCRIPTION
D(24)	RS12.7	**Signaling Bit D in Channel 24**
A(1)	RS1.0	**Signaling Bit A in Channel 1**

Each Receive Signaling Register (RS1 to RS12) reports the incoming robbed bit signaling from eight DS0 channels. In the ESF framing mode, there can be up to four signaling bits per channel (A, B, C, and D). In the D4 framing mode, there are only two signaling bits per channel (A and B). In the D4 framing mode, the framer will replace the C and D signaling bit positions with the A and B signaling bits from the previous multiframe. Hence, whether the framer is operated in either framing mode, the user needs only to retrieve the signaling bits every 3 ms. The bits in the Receive Signaling Registers are updated on multiframe boundaries so the user can utilize the Receive Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The Receive Signaling Registers are frozen and not updated during a loss of sync condition (SR1.0=1). They will contain the most recent signaling information before the “OOF” occurred. The signaling data reported in RS1 to RS12 is also available at the RSIG and RSER signals.

A change in the signaling bits from one multiframe to the next will cause the RSC status bit (SR2.0) to be set. The user can enable the INT* pin to toggle low upon detection of a change in signaling by setting the IMR2.0 bit. Once a signaling change has been detected, the user has at least 2.75 ms to read the data out of the RS1 to RS12 registers before the data will be lost.

TS1 TO TS12: TRANSMIT SIGNALING REGISTERS (Address=70 to 7B Hex)

(MSB)							(LSB)	
A(8)	A(7)	A(6)	A(5)	A(4)	A(3)	A(2)	A(1)	TS1 (70)
A(16)	A(15)	A(14)	A(13)	A(12)	A(11)	A(10)	A(9)	TS2 (71)
A(24)	A(23)	A(22)	A(21)	A(20)	A(19)	A(18)	A(17)	TS3 (72)
B(8)	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)	B(1)	TS4 (73)
B(16)	B(15)	B(14)	B(13)	B(12)	B(11)	B(10)	B(9)	TS5 (74)
B(24)	B(23)	B(22)	B(21)	B(20)	B(19)	B(18)	B(17)	TS7 (75)
A/C(8)	A/C(7)	A/C(6)	A/C(5)	A/C(4)	A/C(3)	A/C(2)	A/C(1)	TS7 (76)
A/C(16)	A/C(15)	A/C(14)	A/C(13)	A/C(12)	A/C(11)	A/C(10)	A/C(9)	TS8 (77)
A/C(24)	A/C(23)	A/C(22)	A/C(21)	A/C(20)	A/C(19)	A/C(18)	A/C(17)	TS9 (78)
B/D(8)	B/D(7)	B/D(6)	B/D(5)	B/D(4)	B/D(3)	B/D(2)	B/D(1)	TS10 (79)
B/D(16)	B/D(15)	B/D(14)	B/D(13)	B/D(12)	B/D(11)	B/D(10)	B/D(9)	TS11 (7A)
B/D(24)	B/D(23)	B/D(22)	B/D(21)	B/D(20)	B/D(19)	B/D(18)	B/D(17)	TS12 (7B)

SYMBOL	POSITION	NAME AND DESCRIPTION
D(24)	TS12.7	**Signaling Bit D in Channel 24**
A(1)	TS1.0	**Signaling Bit A in Channel 1**

Each Transmit Signaling Register (TS1 to TS12) contains the Robbed Bit signaling for eight DS0 channels that will be inserted into the outgoing stream if enabled to do so via TCR1.4. In the ESF framing mode, there can be up to four signaling bits per channel (A, B, C, and D). On multiframe boundaries, the framer will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the device. The user can utilize the Transmit Multiframe Interrupt in Status Register 2 (SR2.6) to know when to update the signaling bits. In the ESF framing mode, the interrupt will come every 3 ms and the user has a full 3 ms to update the TSRs. In the D4 framing mode, there are only two signaling bits per channel (A and B). However in the D4 framing mode, the framer uses the C and D bit positions as the A and B bit positions for the next multiframe. The framer will load the values in the TSRs into the outgoing shift register every other D4 multiframe.

10.2 HARDWARE BASED SIGNALING

Note:

Hardware Based Signaling requires access to the TSIG and RSIG signals which are only available in Modes 5 to 10. See Section 3 for more details on the various modes of operation in the DS3120.

Receive Side

In hardware based signaling, the device extracts the signaling bits from the receive data stream and buffers them over a four multiframe depth and then outputs them in a serial PCM fashion on a channel–by–channel basis at the RSIG output. In the ESF framing mode, the ABCD signaling bits are output on RSIG in the lower nibble of each channel. The RSIG data is updated once a multiframe (3 ms) unless a freeze is in effect. In the D4 framing mode, the AB signaling bits are output twice on RSIG in the lower nibble of each channel. Hence, bits 5 and 6 contain the same data as bits 7 and 8 respectively in each channel. The RSIG data is updated once a multiframe (1.5 ms) unless a freeze is in effect. See the timing diagrams in Section 20 for some examples.

In hardware based signaling, the user has the option to replace all of the extracted robbed–bit signaling bit positions with ones. This option is enabled via the RFSA1 control bit (CCR4.5) and it can be invoked on a per–channel basis by setting the RPCSI control bit (CCR4.6) high and then programming RCHBLK appropriately just like the per–channel signaling re–insertion operates. How to control the operation of RCHBLK is covered in Section 12.

The signaling data in the four multiframe buffer will be frozen in a known good state upon either a loss of synchronization (OOF event), carrier loss, or frame slip. This action meets the requirements of BellCore TR– TSY–000170 for signaling freezing. To allow this freeze action to occur, the RFE control bit (CCR4.4) should be set high. The user can force a freeze by setting the RFF control bit (CCR4.3) high. The four multiframe buffer provides a three multiframe delay in the signaling bits provided at the RSIG pin. When freezing is enabled (RFE=1), the signaling data will be held in the last known good state until the corrupting error condition subsides. When the error condition subsides, the signaling data will be held in the old state for at least an additional 9 ms (or 4.5 ms in D4 framing mode) before being allowed to be updated with new signaling data.

Transmit Side

Via the THSE control bit (CCR4.2), the framer can be set up to take the signaling data presented at the TSIG pin and insert the signaling data into the PCM data stream that is being input at the TSER pin. The user has the ability to control which channels are to have signaling data from the TSIG pin inserted into them on a channel–by–channel basis by setting the TPCSI control bit (CCR4.1) high. When TPCSI is enabled, channels in which the TCHBLK signal has been programmed to be set high in, will not have signaling data from the TSIG pin inserted into them. How to control the operation of TCHBLK is covered in Section 12.

11. PER–CHANNEL CODE (IDLE) GENERATION AND LOOPBACK

Each framer in the DS3120 can replace data on a channel–by–channel basis in both the transmit and receive directions. The transmit direction is from the backplane to the T1 line and is covered in Section 11.1. The receive direction is from the T1 line to the backplane and is covered in Section 11.2.

11.1 TRANSMIT SIDE CODE GENERATION

In the transmit direction there are two methods by which channel data from the backplane can be overwritten with data generated by the framer. The first method which is covered in Section 11.1.1 only allows the same 8-bit value to be placed in one or more of the 24 DS0 channels but it also has an alternate function to enable a per-channel loopback feature. The second method which is covered in Section 11.1.2 allows a different 8-bit value to be placed in each of the 24 DS0 channels.

11.1.1 Simple Idle Code Insertion and Per–Channel Loopback

The first method involves using the Transmit Idle Registers (TIR1/2/3) to determine which of the 24 DS0 channels should be overwritten with the code placed in the Transmit Idle Definition Register (TIDR). This method allows the same 8–bit code to be placed into any of the 24 T1 channels. If this method is used, then the CCR4.0 control bit must be set to zero.

Each of the bit position in the Transmit Idle Registers (TIR1/TIR2/TIR3) represent a DS0 channel in the outgoing frame. When these bits are set to a one, the corresponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR). Robbed bit signaling and Bit 7 stuffing will occur over the programmed Idle Code unless the DS0 channel is made transparent by the Transmit Transparency Registers.

The Transmit Idle Registers (TIRs) have an alternate function that allow them to define a Per–Channel LoopBack (PCLB). If the TIRFS control bit (CCR4.0) is set to one, then the TIRs will determine which channels (if any) from the backplane should be replaced with the data from the receive side or in other words, off of the T1 line. If this mode is enabled, then transmit and receive clocks and frame syncs must be synchronized. Hence, Per–Channel LoopBack (PCLB) is only functional in the Loop Timed Modes (i.e., Modes 1, 2, 5, 6, and 9)

TIR1/TIR2/TIR3: TRANSMIT IDLE REGISTERS (Address=3C to 3E Hex)

[Also used for Per–Channel Loopback]

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (3C)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (3D)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (3E)

SYMBOLS	POSITIONS	NAME AND DESCRIPTION
CH1 - 24	TIR1.0 - 3.7	**Transmit Idle Code Insertion Control Bits.** 0 = do not insert the Idle Code in the TIDR into this channel 1 = insert the Idle Code in the TIDR into this channel

NOTE:

If CCR4.0=1, then a zero in the TIRs implies that channel data is to be sourced from TSER and a one implies that channel data is to be sourced from the output of the receive side framer (i.e., Per–Channel Loopback; see Figure 1–1).

TIDR: TRANSMIT IDLE DEFINITION REGISTER (Address=3F Hex)

(MSB)							(LSB)
TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0

SYMBOL	POSITION	NAME AND DESCRIPTION
TIDR7	TIDR.7	MSB of the Idle Code (this bit is transmitted first)
TIDR0	TIDR.0	LSB of the Idle Code (this bit is transmitted last)

11.1.2 Per–Channel Code Insertion

The second method involves using the Transmit Channel Control Registers (TCC1/2/3) to determine which of the 24 T1 channels should be overwritten with the code placed in the Transmit Channel Registers (TC1 to TC24). This method is more flexible than the first in that it allows a different 8–bit code to be placed into each of the 24 T1 channels.

TC1 TO TC24: TRANSMIT CHANNEL REGISTERS

(Address=40 to 4F and 50 to 57 Hex)

(for brevity, only channel one is shown; see Table 4-1 for other register address)

(MSB)							(LSB)	
C7	C6	C5	C4	C3	C2	C1	C0	TC1 (50)

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	TC1.7	MSB of the Code (this bit is transmitted first)
C0	TC1.0	LSB of the Code (this bit is transmitted last)

TCC1/TCC2/TCC3: TRANSMIT CHANNEL CONTROL REGISTER

(Address=16 to 18 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCC1 (16)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCC2 (17)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCC3 (18)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH1 - 24	TCC1.0 - 3.7	**Transmit Code Insertion Control Bits** 0 = do not insert data from the TC register into the transmit data stream 1 = insert data from the TC register into the transmit data stream

11.2 RECEIVE SIDE CODE GENERATION

In the receive direction there are also two methods by which channel data to the backplane can be overwritten with data generated by the framer. The first method which is covered in Section 11.2.1 while the second method is covered in Section 11.2.2.

11.2.1 Simple Code Insertion

The first method on the receive side involves using the Receive Mark Registers (RMR1/2/3) to determine which of the 24 T1 channels should be overwritten with either a 7Fh idle code or with a digital milliwatt pattern. The RCR2.7 bit will determine which code is used. The digital milliwatt code is an 8 byte repeating pattern that represents a 1 kHz sine wave (1E/0B/0B/1E/9E/8B/8B/9E). Each bit in the RMRs, represents a particular channel. If a bit is set to a one, then the receive data in that channel will be replaced with one of the two codes. If a bit is set to zero, no replacement occurs.

RMR1/RMR2/RMR3: RECEIVE MARK REGISTERS (Address=2D to 2F Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RMR1(2D)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RMR2(2E)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RMR3(2F)

SYMBOLS	POSITIONS	NAME AND DESCRIPTION
CH1 - 24	RMR1.0 - 3.7	**Receive Channel Mark Control Bits** 0 =do not affect the receive data associated with this channel 1 = replace the receive data associated with this channel with either the idle code or the digital milliwatt code (depends on the RCR2.7 bit)

11.2.2 Per–Channel Code Insertion

The second method involves using the Receive Channel Control Registers (RCC1/2/3) to determine which of the 24 T1 channels off of the T1 line and going to the backplane should be overwritten with the code placed in the Receive Channel Registers (RC1 to RC24). This method is more flexible than the first in that it allows a different 8–bit code to be placed into each of the 24 T1 channels.

RC1 TO RC24: RECEIVE CHANNEL REGISTERS

(Address=58 to 5F and 80 to 8F Hex)

(for brevity, only channel one is shown; see Table 4-1 for other register address)

(MSB)							(LSB)	
C7	C6	C5	C4	C3	C2	C1	C0	RC1 (80)

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	RC1.7	MSB of the Code (this bit is sent first to the backplane)
C0	RC1.0	LSB of the Code (this bit is sent last to the backplane)

RCC1/RCC2/RCC3: RECEIVE CHANNEL CONTROL REGISTER

(Address=1B to 1D Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCC1 (1B)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCC2 (1C)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCC3 (1D)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH1 - 24	RCC1.0 - 3.7	**Receive Code Insertion Control Bits** 0 = do not insert data from the RC register into the receive data stream 1 = insert data from the RC register into the receive data stream

12. DS0 SELECT CONTROL REGISTERS

The Receive Channel Blocking Registers (RCBR1/RCBR2/RCBR3) and the Transmit Channel Blocking Registers (TCBR1/TCBR2/TCBR3) control the internal RCHBLK and TCHBLK signals respectively. The internal RCHBLK and TCHBLK signals can be used to either control the Hardware Based Signaling attributes of the DS3120 or to decide to which channels the HDLC controller should be mapped.

RCBR1/RCBR2/RCBR3: RECEIVE CHANNEL BLOCKING REGISTERS
(Address=6C to 6E Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCBR1 (6C)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCBR2 (6D)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCBR3 (6E)

SYMBOLS	POSITIONS	NAME AND DESCRIPTION
CH1 - 24	RCBR1.0 - 3.7	**Receive Channel Blocking Control Bits (Signaling Application).** 0 = allow the robbed-bit signaling position to be forced to one 1 = do not modify the value in the robbed-bit signaling position **Receive Channel Blocking Control Bits (HDLC Application).** 0 = do not route the DS0 channel to the HDLC controller 1 = route the DS0 channel to the HDLC controller

TCBR1/TCBR2/TCBR3: TRANSMIT CHANNEL BLOCKING REGISTERS
(Address=32 to 34 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCBR1 (32)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCBR2 (33)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCBR3 (34)

SYMBOLS	POSITIONS	NAME AND DESCRIPTION
CH1 - 24	TCBR1.0 - 3.7	**Transmit Channel Blocking Control Bits (Signaling Application).** 0 = allow robbed-bit signaling information to be inserted 1 = do not allow robbed-bit signaling information to be inserted **Transmit Channel Blocking Control Bits (HDLC Application).** 0 = do not source the DS0 channel from the HDLC controller 1 = source the DS0 channel from the HDLC controller

12.1 RCHBLK & TCHBLK USED FOR SIGNALING CONTROL

On the Receive Side, when Hardware Based Signaling is used, the DS3120 has the ability to force the extracted robbed-bit signaling bit positions to a one. This operation is enabled via the CCR4.5 control bit. When this mode is enabled, the RCHBLK registers can be used to select which DS0 channels should have their robbed-bit signaling bit positions force to one. For the RCHBLK registers to be enabled, the CCR4.6 control bit must be set to one.

On the Transmit Side, when Hardware Based Signaling is used, the DS3120 will insert signaling from the TSIG input into the data stream input at TSER. This operation is enabled via the CCR4.2 control bit. When this mode is enabled, the TCHBLK registers can be used to select which DS0 channels should have robbed-bit signaling information inserted and which should not. For the TCHBLK registers to be enabled, the CCR4.1 control bit must be set to one.

12.2 RCHBLK & TCHBLK USED FOR HDLC CONTROL

The RCHBLK and TCHBLK signals can also be used to determine which DS0 channels should be mapped to/from the internal HDLC controller. This function is covered in Section 14.

13. ELASTIC STORE OPERATION

Each framer in the DS3120 contains dual two–frame (386 bits) elastic stores, one for the receive direction, and one for the transmit direction. These elastic stores are only used when the Interleave Bus Operation Modes (IBO) are enabled (i.e., Modes 9 & 10). When the DS3120 is operated in either of the IBO modes, then the elastic stores must be enabled which means that both the CCR1.7 and CCR1.2 control bits must be set to one. Both elastic stores contain full controlled slip capability and both elastic stores within the framer are fully independent. See Section 18 for a detailed description of the IBO function.

Controlled slips in the receive elastic store are reported in the SR1.4 bit and the direction of the slip is reported in the RIR1.3 and RIR1.4 bits. Controlled slips in the transmit elastic store are reported in the RIR2.3 bit and the direction of the slip is reported in the RIR2.5 and RIR2.4 bits. If the receive and transmit clocks of the framers are frequency locked to the 8MCLKI signal, then the elastic stores will never fill or empty and controlled slips will not occur.

Two mechanisms are available to the user for resetting the elastic stores. The Elastic Store Reset (TX - CCR7.4 & RX - CCR7.5) function forces the elastic stores to a depth of one frame unconditionally. Data is lost during the reset. The second method, the Elastic Store Align (TX - CCR6.5 & RX - CCR6.6) forces the elastic store depth to a minimum depth of half a frame only if the current pointer separation is already less then half a frame. If a realignment occurs data is lost. In both mechanisms, independent resets are provided for both the receive and transmit elastic stores. In most applications, the elastic stores do not need to be reset.

14. HDLC CONTROLLER

The DS3120 contains an onboard HDLC controller with 64-byte buffers that can be assigned to either the Facilities Data Link (FDL) or to one or more DS0 channels. If the HDLC controller is assigned to DS0 channels, then it can assigned to any DS0 channel or multiple DS0 channels as well as any specific bits within the DS0 channels. Table 14-1 details how the DS3120 should be configured to select whether the HDLC controller should be assigned to the FDL or to DS0 channels. See Figure 20-5 for details on where the HDLC is placed in the transmit side data flow.

HDLC Assignment Configuration Table 14-1

HDLC Assignment	TBOC.6	RDC1.7 / TDC1.7	TCR1.2
DS0(s)	0	1	1 or 0
FDL	1	0	1
Disable	0	0	1 or 0

Note that TBOC.6 = 1 and TDC1.7 = 1 cannot exist without corrupting the data in the FDL
(if TCR1.2=1).

14.1 GENERAL OVERVIEW

The DS3120 contains a complete HDLC controller with 64–byte buffers in both the transmit and receive directions as well as separate dedicated hardware for Bit Oriented Codes (BOC). The HDLC controller performs all the necessary overhead for generating and receiving Performance Report Messages (PRM) as described in ANSI T1.403 and the messages as described in AT&T TR54016. The HDLC controller automatically generates and detects flags, generates and checks the CRC check sum, generates and detects abort sequences, stuffs and destuffs zeros (for transparency), and byte aligns to the HDLC data stream. The 64–byte buffers in the HDLC controller are large enough to allow a full PRM to be received or transmitted without host intervention. The BOC controller will automatically detect incoming BOC sequences and alert the host. When the BOC ceases, the DS3120 will also alert the host. The user can set the device up to send any of the possible 6–bit BOC codes.

There are thirteen registers that the host will use to operate and control the operation of the HDLC and BOC controllers. A brief description of the registers is shown in Table 14–2.

HDLC/BOC CONTROLLER REGISTER LIST Table 14-2

NAME	FUNCTION
HDLC Control Register (HCR)	general control over the HDLC and BOC controllers
HDLC Status Register (HSR)	key status information for both transmit and receive directions
HDLC Interrupt Mask Register (HIMR)	allows/stops status bits to/from causing an interrupt
Receive HDLC Information Register (RHIR)	status information on receive HDLC controller
Receive BOC Register (RBOC)	status information on receive BOC controller
Receive HDLC FIFO Register (RHFR)	access to 64–byte HDLC FIFO in receive direction
Receive HDLC DS0 Control Register 1 (RDC1) Receive HDLC DS0 Control Register 2 (RDC2)	controls the HDLC function when used on DS0 channels
Transmit HDLC Information Register (THIR)	status information on transmit HDLC controller
Transmit BOC Register (TBOC)	enables/disables transmission of BOC codes
Transmit HDLC FIFO Register (THFR)	access to 64–byte HDLC FIFO in transmit direction
Transmit HDLC DS0 Control Register 1 (TDC1) Transmit HDLC DS0 Control Register 2 (TDC2)	controls the HDLC function when used on DS0 channels

14.2 STATUS REGISTER FOR THE HDLC

Four of the HDLC/BOC controller registers (HSR, RHIR, RBOC, and THIR) provide status information. When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers will be set to a one. Some of the bits in these four HDLC status registers are latched and some are real time bits that are not latched. Section 14.4 contains register descriptions that list which bits are latched and which are not. With the latched bits, when an event occurs and a bit is set to a one, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again. The real time bits report the current instantaneous conditions that are occurring and the history of these bits is not latched.

Like the other status registers in the DS3120, the user will always proceed a read of any of the four registers with a write. The byte written to the register will inform the DS3120 which of the latched bits the user wishes to read and have cleared (the real time bits are not affected by writing to the status register). The user will write a byte to one of these registers, with a one in the bit positions he or she wishes to read and a zero in the bit positions he or she does not wish to obtain the latest information on. When a one is written to a bit location, the read register will be updated with current value and it will be cleared. When a zero is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This write–read–write (for polled driven access) or write–read (for interrupt driven access) scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS3120 with higher–order software languages.

Like the SR1 and SR2 status registers, the HSR register has the unique ability to initiate a hardware interrupt via the INT* output pin. Each of the events in the HSR can be either masked or unmasked from the interrupt pin via the HDLC Interrupt Mask Register (HIMR). Interrupts will force the INT* pin low when the event occurs. The INT* pin will be allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

14.3 BASIC OPERATION DETAILS

To allow the framer to properly source/receive data from/to the HDLC and BOC controller the legacy FDL circuitry (which is described in Section 15) should be disabled and the following bits should be programmed as shown:

TCR1.2 = 1 (source FDL data from the HDLC and BOC controller)
TBOC.6 = 1 (enable HDLC and BOC controller)
CCR2.5 = 0 (disable SLC–96 and D4 Fs–bit insertion)
CCR2.4 = 0 (disable legacy FDL zero stuffer)
CCR2.1 = 0 (disable SLC–96 reception)
CCR2.0 = 0 (disable legacy FDL zero stuffer)
IMR2.4 = 0 (disable legacy receive FDL buffer full interrupt)
IMR2.3 = 0 (disable legacy transmit FDL buffer empty interrupt)
IMR2.2 = 0 (disable legacy FDL match interrupt)
IMR2.1 = 0 (disable legacy FDL abort interrupt).

As a basic guideline for interpreting and sending both HDLC messages and BOC messages, the following sequences can be applied:

Receive a HDLC Message or a BOC

1. Enable RBOC and RPS interrupts
2. Wait for interrupt to occur
3. If RBOC=1, then follow steps 5 and 6
4. If RPS=1, then follow steps 7 through 12
5. If LBD=1, a BOC is present, then read the code from the RBOC register and take action as needed
6. If BD=0, a BOC has ceased, take action as needed and then return to step 1
7. Disable RPS interrupt and enable either RPE, RNE, or RHALF interrupt
8. Read RHIR to obtain REMPTY status a. if REMPTY=0, then record OBYTE, CBYTE, and POK bits and then read the FIFO a1. if CBYTE=0 then skip to step 9 a2. if CBYTE=1 then skip to step 11 b. if REMPTY=1, then skip to step 10
9. Repeat step 8
10. Wait for interrupt, skip to step 8
11. If POK=0, then discard whole packet, if POK=1, accept the packet 12. disable RPE, RNE, or RHALF interrupt, enable RPS interrupt and return to step 1.

Transmit a HDLC Message

1. Make sure HDLC controller is done sending any previous messages and is current sending flags by checking that the FIFO is empty by reading the TEMPTY status bit in the THIR register
2. Enable either the THALF or TNF interrupt
3. Read THIR to obtain TFULL status a. if TFULL=0, then write a byte into the FIFO and skip to next step (special case occurs when the last byte is to be written, in this case set TEOM=1 before writing the byte and then skip to step 6) b. if TFULL=1, then skip to step 5
4. Repeat step 3
5. Wait for interrupt, skip to step 3
6. Disable THALF or TNF interrupt and enable TMEND interrupt
7. Wait for an interrupt, then read TUDR status bit to make sure packet was transmitted correctly.

Transmit a BOC

1. Write 6–bit code into TBOC
2. Set SBOC bit in TBOC=1

14.4 HDLC/BOC REGISTER DESCRIPTION

HCR: HDLC CONTROL REGISTER (Address = 00 Hex)

(MSB) … **(LSB)**

RBR	RHR	TFS	THR	TABT	TEOM	TZSD	TCRCD

SYMBOL	POSITION	NAME AND DESCRIPTION
RBR	HCR.7	**Receive BOC Reset.** A 0 to 1 transition will reset the BOC circuitry. Must be cleared and set again for a subsequent reset.
RHR	HCR.6	**Receive HDLC Reset.** A 0 to 1 transition will reset the HDLC controller. Must be cleared and set again for a subsequent reset.
TFS	HCR.5	**Transmit Flag/Idle Select.** 0 = 7Eh 1 = FFh
THR	HCR.4	**Transmit HDLC/BOC Reset.** A 0 to 1 transition will reset both the HDLC controller and the transmit BOC circuitry. Must be cleared and set again for a subsequent reset.
TABT	HCR.3	**Transmit Abort.** A 0 to 1 transition will cause the FIFO contents to be dumped and one FEh abort to be sent followed by 7Eh or FFh flags/idle until a new packet is initiated by writing new data into the FIFO. Must be cleared and set again for a subsequent abort to be sent.
TEOM	HCR.2	**Transmit End of Message.** Should be set to a one just before the last data byte of a HDLC packet is written into the transmit FIFO at THFR. The HDLC controller will clear this bit when the last byte has been transmitted.
TZSD	HCR.1	**Transmit Zero Stuffer Defeat.** Overrides internal enable. 0 = enable the zero stuffer (normal operation) 1 = disable the zero stuffer

SYMBOL	POSITION	NAME AND DESCRIPTION
TCRCD	HCR.0	**Transmit CRC Defeat.** 0 = enable CRC generation (normal operation) 1 = disable CRC generation

HSR: HDLC STATUS REGISTER (Address = 01 Hex)

(MSB)							(LSB)
RBOC	RPE	RPS	RHALF	RNE	THALF	TNF	TMEND

SYMBOL	POSITION	NAME AND DESCRIPTION
RBOC	HSR.7	**Receive BOC Detector Change of State.** Set whenever the BOC detector sees a change of state from a BOC Detected to a No Valid Code seen or vice versa. The setting of this bit prompt the user to read the RBOC register for details.
RPE	HSR.6	**Receive Packet End.** Set when the HDLC controller detects either the finish of a valid message (i.e., CRC check complete) or when the controller has experienced a message fault such as a CRC checking error, or an overrun condition, or an abort has been seen. The setting of this bit prompts the user to read the RHIR register for details.
RPS	HSR.5	**Receive Packet Start**. Set when the HDLC controller detects an opening byte. The setting of this bit prompts the user to read the RHIR register for details.
RHALF	HSR.4	**Receive FIFO Half Full.** Set when the receive 64–byte FIFO fills beyond the half way point. The setting of this bit prompts the user to read the RHIR register for details.
RNE	HSR.3	**Receive FIFO Not Empty.** Set when the receive 64–byte FIFO has at least 1 byte available for a read. The setting of this bit prompts the user to read the RHIR register for details.
THALF	HSR.2	**Transmit FIFO Half Empty.** Set when the transmit 64–byte FIFO empties beyond the half way point. The setting of this bit prompts the user to read the THIR register for details.
TNF	HSR.1	**Transmit FIFO Not Full.** Set when the transmit 64–byte FIFO has at least 1 byte available. The setting of this bit prompts the user to read the THIR register for details.
TMEND	HSR.0	**Transmit Message End.** Set when the transmit HDLC controller has finished sending a message. The setting of this bit prompts the user to read the THIR register for details.

NOTE:

The RBOC, RPE, RPS, and TMEND bits are latched and will be cleared when read.

HIMR: HDLC INTERRUPT MASK REGISTER (Address = 02 Hex)

(MSB) **(LSB)**

RBOC	RPE	RPS	RHALF	RNE	THALF	TNF	TMEND

SYMBOL	POSITION	NAME AND DESCRIPTION
RBOC	HIMR.7	**Receive BOC Detector Change of State.** 0 = interrupt masked 1 = interrupt enabled
RPE	HIMR.6	**Receive Packet End.** 0 = interrupt masked 1 = interrupt enabled
RPS	HIMR.5	**Receive Packet Start.** 0 = interrupt masked 1 = interrupt enabled
RHALF	HIMR.4	**Receive FIFO Half Full.** 0 = interrupt masked 1 = interrupt enabled
RNE	HIMR.3	**Receive FIFO Not Empty.** 0 = interrupt masked 1 = interrupt enabled
THALF	HIMR.2	**Transmit FIFO Half Empty.** 0 = interrupt masked 1 = interrupt enabled
TNF	HIMR.1	**Transmit FIFO Not Full.** 0 = interrupt masked 1 = interrupt enabled
TMEND	HIMR.0	**Transmit Message End.** 0 = interrupt masked 1 = interrupt enabled

RHIR: RECEIVE HDLC INFORMATION REGISTER (Address = 03 Hex)

(MSB) **(LSB)**

RABT	RCRCE	ROVR	RVM	REMPTY	POK	CBYTE	OBYTE

SYMBOL	POSITION	NAME AND DESCRIPTION
RABT	RHIR.7	**Abort Sequence Detected.** Set whenever the HDLC controller sees 7 or more ones in a row.
RCRCE	RHIR.6	**CRC Error.** Set when the CRC checksum is in error.
ROVR	RHIR.5	**Overrun.** Set when the HDLC controller has attempted to write a byte into an already full receive FIFO.
RVM	RHIR.4	**Valid Message.** Set when the HDLC controller has detected and checked a complete HDLC packet.
REMPTY	RHIR.3	**Empty.** A real–time bit that is set high when the receive FIFO is empty.
POK	RHIR.2	**Packet OK.** Set when the byte available for reading in the receive FIFO at RHFR is the last byte of a valid message (and hence no abort was seen, no overrun occurred, and the CRC was correct).
CBYTE	RHIR.1	**Closing Byte.** Set when the byte available for reading in the receive FIFO at RHFR is the last byte of a message (whether the message was valid or not).
OBYTE	RHIR.0	**Opening Byte.** Set when the byte available for reading in the receive FIFO at RHFR is the first byte of a message.

NOTE:

The RABT, RCRCE, ROVR, and RVM bits are latched and will be cleared when read.

RBOC: RECEIVE BIT ORIENTED CODE REGISTER (Address = 04 Hex)

(MSB) **(LSB)**

LBD	BD	BOC5	BOC4	BOC3	BOC2	BOC1	BOC0

SYMBOL	POSITION	NAME AND DESCRIPTION
LBD	RBOC.7	**Latched BOC Detected.** A latched version of the BD status bit (RBOC.6). Will be cleared when read.
BD	RBOC.6	**BOC Detected.** A real–time bit that is set high when the BOC detector is presently seeing a valid sequence and set low when no BOC is currently being detected.
BOC5	RBOC.5	**BOC Bit 5.** Last bit received of the 6–bit code word.
BOC4	RBOC.4	**BOC Bit 4.**
BOC3	RBOC.3	**BOC Bit 3.**
BOC2	RBOC.2	**BOC Bit 2.**
BOC1	RBOC.1	**BOC Bit 1.**
BOC0	RBOC.0	**BOC Bit 0.** First bit received of the 6–bit code word.

NOTE:
1. The LBD bit is latched and will be cleared when read.
2. The RBOC0 to RBOC5 bits display the last valid BOC code verified; these bits will be set to all ones on reset.

RHFR: RECEIVE HDLC FIFO (Address = 05 Hex)

(MSB) **(LSB)**

HDLC7	HDLC6	HDLC5	HDLC4	HDLC3	HDLC2	HDLC1	HDLC0

SYMBOL	POSITION	NAME AND DESCRIPTION
HDLC7	RHFR.7	**HDLC Data Bit 7**. MSB of a HDLC packet data byte.
HDLC6	RHFR.6	**HDLC Data Bit 6.**
HDLC5	RHFR.5	**HDLC Data Bit 5.**
HDLC4	RHFR.4	**HDLC Data Bit 4.**
HDLC3	RHFR.3	**HDLC Data Bit 3.**
HDLC2	RHFR.2	**HDLC Data Bit 2.**
HDLC1	RHFR.1	**HDLC Data Bit 1.**
HDLC0	RHFR.0	**HDLC Data Bit 0.** LSB of a HDLC packet data byte.

THIR: TRANSMIT HDLC INFORMATION (Address = 06 Hex)

(MSB) **(LSB)**

–	–	–	–	–	TEMPTY	TFULL	UDR

SYMBOL	POSITION	NAME AND DESCRIPTION
–	THIR.7	**Not Assigned.** Could be any value when read.
–	THIR.6	**Not Assigned.** Could be any value when read.
–	THIR.5	**Not Assigned.** Could be any value when read.
–	THIR.4	**Not Assigned.** Could be any value when read.
–	THIR.3	**Not Assigned.** Could be any value when read.
TEMPTY	THIR.2	**Transmit FIFO Empty.** A real–time bit that is set high when the FIFO is empty.
TFULL	THIR.1	**Transmit FIFO Full.** A real–time bit that is set high when the FIFO is full.
UDR	THIR.0	**Underrun.** Set when the transmit FIFO unwantedly empties out and an abort is automatically sent.

NOTE:
The UDR bit is latched and will be cleared when read.

TBOC: TRANSMIT BIT ORIENTED CODE (Address = 07 Hex)

(MSB) **(LSB)**

SBOC	HBEN	BOC5	BOC4	BOC3	BOC2	BOC1	BOC0

SYMBOL	POSITION	NAME AND DESCRIPTION
SBOC	TBOC.7	**Send BOC.** Rising edge triggered. Must be transitioned from a 0 to a 1 transmit the BOC code placed in the BOC0 to BOC5 bits instead of data from the HDLC controller.
HBEN	TBOC.6	**Transmit HDLC & BOC Controller Enable.** 0 = source FDL data from the TLINK pin 1 = source FDL data from the onboard HDLC and BOC controller
BOC5	TBOC.5	**BOC Bit 5.** Last bit transmitted of the 6–bit code word.
BOC4	TBOC.4	**BOC Bit 4.**
BOC3	TBOC.3	**BOC Bit 3.**
BOC2	TBOC.2	**BOC Bit 2.**
BOC1	TBOC.1	**BOC Bit 1.**
BOC0	TBOC.0	**BOC Bit 0.** First bit transmitted of the 6–bit code word.

THFR: TRANSMIT HDLC FIFO (Address = 08 Hex)

(MSB) **(LSB)**

HDLC7	HDLC6	HDLC5	HDLC4	HDLC3	HDLC2	HDLC1	HDLC0

SYMBOL	POSITION	NAME AND DESCRIPTION
HDLC7	THFR.7	**HDLC Data Bit 7.** MSB of a HDLC packet data byte.
HDLC6	THFR.6	**HDLC Data Bit 6.**
HDLC5	THFR.5	**HDLC Data Bit 5.**
HDLC4	THFR.4	**HDLC Data Bit 4.**
HDLC3	THFR.3	**HDLC Data Bit 3.**
HDLC2	THFR.2	**HDLC Data Bit 2.**
HDLC1	THFR.1	**HDLC Data Bit 1.**
HDLC0	THFR.0	**HDLC Data Bit 0.** LSB of a HDLC packet data byte.

RDC1: RECEIVE HDLC DS0 CONTROL REGISTER 1 (Address = 90 Hex)

(MSB) **(LSB)**

RDS0E	-	RDS0M	RD4	RD3	RD2	RD1	RD0

SYMBOL	POSITION	NAME AND DESCRIPTION
RDS0E	RDC1.7	**HDLC DS0 Enable.** 0 = use receive HDLC controller for the FDL. 1 = use receive HDLC controller for one or more DS0 channels.
-	RDC1.6	**Not Assigned.** Should be set to 0.
RDS0M	RDC1.5	**DS0 Selection Mode.** 0 = utilize the RD0 to RD4 bits to select which single DS0 channel to use. 1 = utilize the RCHBLK control registers to select which DS0 channels to use. See Section 12.
RD4	RDC1.4	**DS0 Channel Select Bit 4.** MSB of the DS0 channel select.
RD3	RDC1.3	**DS0 Channel Select Bit 3.**
RD2	RDC1.2	**DS0 Channel Select Bit 2.**
RD1	RDC1.1	**DS0 Channel Select Bit 1.**
RD0	RDC1.0	**DS0 Channel Select Bit 0.** LSB of the DS0 channel select.

RDC2: RECEIVE HDLC DS0 CONTROL REGISTER 2 (Address = 91 Hex)

(MSB) **(LSB)**

RDB8	RDB7	RDB6	RDB5	RDB4	RDB3	RDB2	RDB1

SYMBOL	POSITION	NAME AND DESCRIPTION
RDB8	RDC2.7	**DS0 Bit 8 Suppress Enable.** MSB of the DS0. Set to one to stop this bit from being used.
RDB7	RDC2.6	**DS0 Bit 7 Suppress Enable.** Set to one to stop this bit from being used.
RDB6	RDC2.5	**DS0 Bit 6 Suppress Enable.** Set to one to stop this bit from being used.
RDB5	RDC2.4	**DS0 Bit 5 Suppress Enable.** Set to one to stop this bit from being used.
RDB4	RDC2.3	**DS0 Bit 4 Suppress Enable.** Set to one to stop this bit from being used.
RDB3	RDC2.2	**DS0 Bit 3 Suppress Enable.** Set to one to stop this bit from being used.
RDB2	RDC2.1	**DS0 Bit 2 Suppress Enable.** Set to one to stop this bit from being used.
RDB1	RDC2.0	**DS0 Bit 1 Suppress Enable.** LSB of the DS0. Set to one to stop this bit from being used.

TDC1: TRANSMIT HDLC DS0 CONTROL REGISTER 1 (Address = 92 Hex)

(MSB) **(LSB)**

TDS0E	-	TDS0M	TD4	TD3	TD2	TD1	TD0

SYMBOL	POSITION	NAME AND DESCRIPTION
TDS0E	TDC1.7	**HDLC DS0 Enable.** 0 = use transmit HDLC controller for the FDL. 1 = use transmit HDLC controller for one or more DS0 channels.
-	TDC1.6	**Not Assigned.** Should be set to 0.
TDS0M	TDC1.5	**DS0 Selection Mode.** 0 = utilize the TD0 to TD4 bits to select which single DS0 channel to use. 1 = utilize the TCHBLK control registers to select which DS0 channels to use. See Section 12.
TD4	TDC1.4	**DS0 Channel Select Bit 4.** MSB of the DS0 channel select.
TD3	TDC1.3	**DS0 Channel Select Bit 3.**
TD2	TDC1.2	**DS0 Channel Select Bit 2.**
TD1	TDC1.1	**DS0 Channel Select Bit 1.**
TD0	TDC1.0	**DS0 Channel Select Bit 0.** LSB of the DS0 channel select.

TDC2: TRANSMIT HDLC DS0 CONTROL REGISTER 2 (Address = 93 Hex)

(MSB) **(LSB)**

TDB8	TDB7	TDB6	TDB5	TDB4	TDB3	TDB2	TDB1

SYMBOL	POSITION	NAME AND DESCRIPTION
TDB8	TDC2.7	**DS0 Bit 8 Suppress Enable.** MSB of the DS0. Set to one to stop this bit from being used.
TDB7	TDC2.6	**DS0 Bit 7 Suppress Enable.** Set to one to stop this bit from being used.
TDB6	TDC2.5	**DS0 Bit 6 Suppress Enable.** Set to one to stop this bit from being used.
TDB5	TDC2.4	**DS0 Bit 5 Suppress Enable.** Set to one to stop this bit from being used.
TDB4	TDC2.3	**DS0 Bit 4 Suppress Enable.** Set to one to stop this bit from being used.
TDB3	TDC2.2	**DS0 Bit 3 Suppress Enable.** Set to one to stop this bit from being used.
TDB2	TDC2.1	**DS0 Bit 2 Suppress Enable.** Set to one to stop this bit from being used.
TDB1	TDC2.0	**DS0 Bit 1 Suppress Enable.** LSB of the DS0. Set to one to stop this bit from being used.

15. LEGACY FDL SUPPORT & D4/SLC-96 SUPPORT

15.1 OVERVIEW

The DS3120 maintains the circuitry that existed in previous generations of Dallas Semiconductor's framers. Sections 15.2 & 15.3 cover the circuitry and operation of this legacy functionality. In new applications, it is recommended that the HDLC controller and BOC controller described in Section 14 be used. It is possible to have both the new HDLC/BOC controller and the legacy hardware working at the same time.

15.2 RECEIVE SECTION

In the receive section, the recovered FDL bits or Fs bits are shifted bit–by–bit into the Receive FDL register (RFDL). Since the RFDL is 8 bits in length, it will fill up every 2 ms (8 times 250 us). The framer will signal an external microcontroller that the buffer has filled via the SR2.4 bit. If enabled via IMR2.4, the INT* pin will toggle low indicating that the buffer has filled and needs to be read. The user has 2 ms to read this data before it is lost. If the byte in the RFDL matches either of the bytes programmed into the RMTCH1 or RMTCH2 registers, then the SR2.2 bit will be set to a one and the INT* pin will toggled low if enabled via IMR2.2. This feature allows an external microcontroller to ignore the FDL or Fs pattern until an important event occurs.

The framer also contains a zero destuffer, which is controlled via the CCR2.0 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol states that no more than 5 ones should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via CCR2.0, the DS3120 will automatically look for 5 ones in a row, followed by a zero. If it finds such a pattern, it will automatically remove the zero. If the zero destuffer sees six or more ones in a row followed by a zero, the zero is not removed. The CCR2.0 bit should always be set to a one when the DS3120 is extracting the FDL.

RFDL: RECEIVE FDL REGISTER (Address = 28 Hex)

(MSB)							(LSB)
RFDL7	RFDL6	RFDL5	RFDL4	RFDL3	RFDL2	RFDL1	RFDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
RFDL7	RFDL.7	MSB of the Received FDL Code
RFDL0	RFDL.0	LSB of the Received FDL Code

The Receive FDL Register (RFDL) reports the incoming Facility Data Link (FDL) or the incoming Fs bits. The LSB is received first.

RMTCH1: RECEIVE FDL MATCH REGISTER 1 (Address = 29 Hex)
RMTCH2: RECEIVE FDL MATCH REGISTER 2 (Address = 2A Hex)

(MSB)							(LSB)
RMFDL7	RMFDL6	RMFDL5	RMFDL4	RMFDL3	RMFDL2	RMFDL1	RMFDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
RMFDL7	RMTCH1.7 RMTCH2.7	MSB of the FDL Match Code
RMFDL0	RMTCH1.0 RMTCH2.0	LSB of the FDL Match Code

When the byte in the Receive FDL Register matches either of the two Receive FDL Match Registers (RMTCH1/RMTCH2), SR2.2 will be set to a one and the INT* will go active if enabled via IMR2.2.

15.3 TRANSMIT SECTION

The transmit section will shift out into the T1 data stream, either the FDL (in the ESF framing mode) or the Fs bits (in the D4 framing mode) contained in the Transmit FDL register (TFDL). When a new value is written to the TFDL, it will be multiplexed serially (LSB first) into the proper position in the outgoing T1 data stream. After the full 8 bits has been shifted out, the framer will signal the host microcontroller that the buffer is empty and that more data is needed by setting the SR2.3 bit to a one. The INT* will also toggle low if enabled via IMR2.3. The user has 2 ms to update the TFDL with a new value. If the TFDL is not updated, the old value in the TFDL will be transmitted once again. The framer also contains a zero stuffer, which is controlled via the CCR2.4 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol states that no more than 5 ones should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via CCR2.4, the framer will automatically look for 5 ones in a row. If it finds such a pattern, it will automatically insert a zero after the five ones. The CCR2.0 bit should always be set to a one when the framer is inserting the FDL.

TFDL: TRANSMIT FDL REGISTER (Address = 7E Hex)

[Also used to insert Fs framing pattern in D4 framing mode; see Section 15.4]

(MSB)							(LSB)
TFDL7	TFDL6	TFDL5	TFDL4	TFDL3	TFDL2	TFDL1	TFDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
TFDL7	TFDL.7	MSB of the FDL code to be transmitted
TFDL0	TFDL.0	LSB of the FDL code to be transmitted

The Transmit FDL Register (TFDL) contains the Facility Data Link (FDL) information that is to be inserted on a byte basis into the outgoing T1 data stream. The LSB is transmitted first.

15.4 D4/SLC–96 OPERATION

In the D4 framing mode, the framer uses the **TFDL register to insert the Fs framing pattern.** To allow the device to properly insert the Fs framing pattern, the TFDL register at address 7Eh must be programmed to 1Ch and the following bits must be programmed as shown:

TCR1.2=0 (source Fs data from the TFDL register)
CCR2.5=1 (allow the TFDL register to load on multiframe boundaries).

Since the SLC–96 message fields share the Fs–bit position, the user can access the these message fields via the TFDL and RFDL registers.

16. PROGRAMMABLE IN–BAND CODE GENERATION AND DETECTION

Each framer in the DS3120 has the ability to generate and detect a repeating bit pattern that is from one to 8 bits in length. To transmit a pattern, the user will load the pattern to be sent into the Transmit Code Definition (TCD) register and select the proper length of the pattern by setting the TC0 and TC1 bits in the In–Band Code Control (IBCC) register. Once this is accomplished, the pattern will be transmitted as long as the TLOOP control bit (CCR3.1) is enabled. Normally (unless the transmit formatter is programmed to not insert the F–bit position) the framer will overwrite the repeating pattern once every 193 bits to allow the F–bit position to be sent. See Figure 20-5 for more details. As an example, if the user wished to transmit the standard “loop up” code for Channel Service Units which is a repeating pattern of ...10000100001... then 80h would be loaded into TDR and the length would set to 5 bits.

Each framer can detect two separate repeating patterns to allow for both a “loop up” code and a “loop down” code to be detected. The user will program the codes to be detected in the Receive Up Code Definition (RUPCD) register and the Receive Down Code Definition (RDNCD) register and the length of each pattern will be selected via the IBCC register. The framer will detect repeating pattern codes in both framed and unframed circumstances with bit error rates as high as 10**–2. The code detector has a nominal integration period of 48 ms. Hence, after about 48 ms of receiving either code, the proper status bit (LUP at SR1.7 and LDN at SR1.6) will be set to a one. Normally codes are sent for a period of 5 seconds. It is recommend that the software poll the framer every 100 ms to 1000 ms until 5 seconds has elapsed to insure that the code is continuously present.

IBCC: IN–BAND CODE CONTROL REGISTER (Address=12 Hex)

(MSB)							(LSB)
TC1	TC0	RUP2	RUP1	RUP0	RDN2	RDN1	RDN0

SYMBOL	POSITION	NAME AND DESCRIPTION
TC1	IBCC.7	**Transmit Code Length Definition Bit 1.** See Table 16–1
TC0	IBCC.6	**Transmit Code Length Definition Bit 0.** See Table 16–1
RUP2	IBCC.5	**Receive Up Code Length Definition Bit 2.** See Table 16–2
RUP1	IBCC.4	**Receive Up Code Length Definition Bit 1.** See Table 16–2
RUP0	IBCC.3	**Receive Up Code Length Definition Bit 0.** See Table 16–2
RDN2	IBCC.2	**Receive Down Code Length Definition Bit 2.** See Table 16–2
RDN1	IBCC.1	**Receive Down Code Length Definition Bit 1.** See Table 16–2
RDN0	IBCC.0	**Receive Down Code Length Definition Bit 0.** See Table 16–2

TRANSMIT CODE LENGTH Table 16-1

TC1	TC0	LENGTH SELECTED
0	0	5 bits
0	1	6 bits / 3 bits
1	0	7 bits
1	1	8 bits / 4 bits / 2 bits / 1 bits

RECEIVE CODE LENGTH Table 16-2

RUP2/ RDN2	RUP1/ RDN1	RUP0/ RDN0	LENGTH SELECTED
0	0	0	1 bits
0	0	1	2 bits
0	1	0	3 bits
0	1	1	4 bits
1	0	0	5 bits
1	0	1	6 bits
1	1	0	7 bits
1	1	1	8 bits

TCD: TRANSMIT CODE DEFINITION REGISTER (Address=13 Hex)

(MSB)							(LSB)
C7	C6	C5	C4	C3	C2	C1	C0

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	TCD.7	**Transmit Code Definition Bit 7.** First bit of the repeating pattern.
C6	TCD.6	**Transmit Code Definition Bit 6.**
C5	TCD.5	**Transmit Code Definition Bit 5.**
C4	TCD.4	**Transmit Code Definition Bit 4.**
C3	TCD.3	**Transmit Code Definition Bit 3.**
C2	TCD.2	**Transmit Code Definition Bit 2.** A Don’t Care if a 5 bit length is selected.
C1	TCD.1	**Transmit Code Definition Bit 1.** A Don’t Care if a 5 or 6 bit length is selected.
C0	TCD.0	**Transmit Code Definition Bit 0.** A Don’t Care if a 5, 6 or 7 bit length is selected.

RUPCD: RECEIVE UP CODE DEFINITION REGISTER (Address=14 Hex)

(MSB) **(LSB)**

C7	C6	C5	C4	C3	C2	C1	C0

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	RUPCD.7	**Receive Up Code Definition Bit 7.** First bit of the repeating pattern.
C6	RUPCD.6	**Receive Up Code Definition Bit 6.** A Don't Care if a 1 bit length is selected.
C5	RUPCD.5	**Receive Up Code Definition Bit 5.** A Don't Care if a 1 or 2 bit length is selected.
C4	RUPCD.4	**Receive Up Code Definition Bit 4.** A Don't Care if a 1 to 3 bit length is selected.
C3	RUPCD.3	**Receive Up Code Definition Bit 3.** A Don't Care if a 1 to 4 bit length is selected.
C2	RUPCD.2	**Receive Up Code Definition Bit 2.** A Don't Care if a 1 to 5 bit length is selected.
C1	RUPCD.1	**Receive Up Code Definition Bit 1.** A Don't Care if a 1 to 6 bit length is selected.
C0	RUPCD.0	**Receive Up Code Definition Bit 0.** A Don't Care if a 1 to 7 bit length is selected.

RDNCD: RECEIVE DOWN CODE DEFINITION REGISTER (Address=15 Hex)

(MSB) **(LSB)**

C7	C6	C5	C4	C3	C2	C1	C0

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	RDNCD.7	**Receive Down Code Definition Bit 7.** First bit of the repeating pattern.
C6	RDNCD.6	**Receive Down Code Definition Bit 6.** A Don't Care if a 1 bit length is selected.
C5	RDNCD.5	**Receive Down Code Definition Bit 5.** A Don't Care if a 1 or 2 bit length is selected.
C4	RDNCD.4	**Receive Down Code Definition Bit 4.** A Don't Care if a 1 to 3 bit length is selected.
C3	RDNCD.3	**Receive Down Code Definition Bit 3.** A Don't Care if a 1 to 4 bit length is selected.
C2	RDNCD.2	**Receive Down Code Definition Bit 2.** A Don't Care if a 1 to 5 bit length is selected.
C1	RDNCD.1	**Receive Down Code Definition Bit 1.** A Don't Care if a 1 to 6 bit length is selected.
C0	RDNCD.0	**Receive Down Code Definition Bit 0.** A Don't Care if a 1 to 7 bit length is selected.

17. TRANSMIT TRANSPARENCY

Each of the 24 T1 channels in the transmit direction of the framer can be either forced to be transparent or in other words, can be forced to stop Bit 7 Stuffing and/or Processor Based Robbed Signaling from overwriting the data in the channels. Transparency can be invoked on a channel by channel basis by properly setting the TTR1, TTR2, and TTR3 registers.

TTR1/TTR2/TTR3: TRANSMIT TRANSPARENCY REGISTER

(Address=39 to 3B Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TTR1 (39)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TTR2 (3A)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TTR3 (3B)

SYMBOLS	POSITIONS	NAME AND DESCRIPTION
CH1-24	TTR1.0-3.7	**Transmit Transparency Registers.** 0 = this DS0 channel is not transparent 1 = this DS0 channel is transparent

Each of the bit position in the Transmit Transparency Registers (TTR1/TTR2/TTR3) represent a DS0 channel in the outgoing frame. When these bits are set to a one, the corresponding channel is transparent (or clear). If a DS0 is programmed to be clear, no robbed bit signaling will be inserted nor will the channel have Bit 7 stuffing performed. However, in the D4 framing mode, Bit 2 will be overwritten by a zero when a Yellow Alarm is transmitted. Also the user has the option to prevent the TTR registers from determining which channels are to have Bit 7 stuffing performed. If the TCR2.0 and TCR1.3 bits are set to one, then all 24 T1 channels will have Bit 7 stuffing performed on them regardless of how the TTR registers are programmed. In this manner, the TTR registers are only affecting which channels are to have robbed bit signaling inserted into them. See Figure 20-5 for more details.

18. 8 MHZ INTERLEAVED BUS OPERATION (IBO)

The DS3120 has the ability to aggregate four T1 datastreams into a single 8.192 MHz datastream. This functionality is called Interleaved Bus Operation (IBO) and it is available in Modes 9 & 10. See Section 3 for a discussion of the various modes within the device. The DS3120 can also support the aggregation of just two T1 datastreams into a single 4.096 MHz datastream but this functionality is not covered in this data sheet. Please contact the factory for support on 4.096 MHz applications.

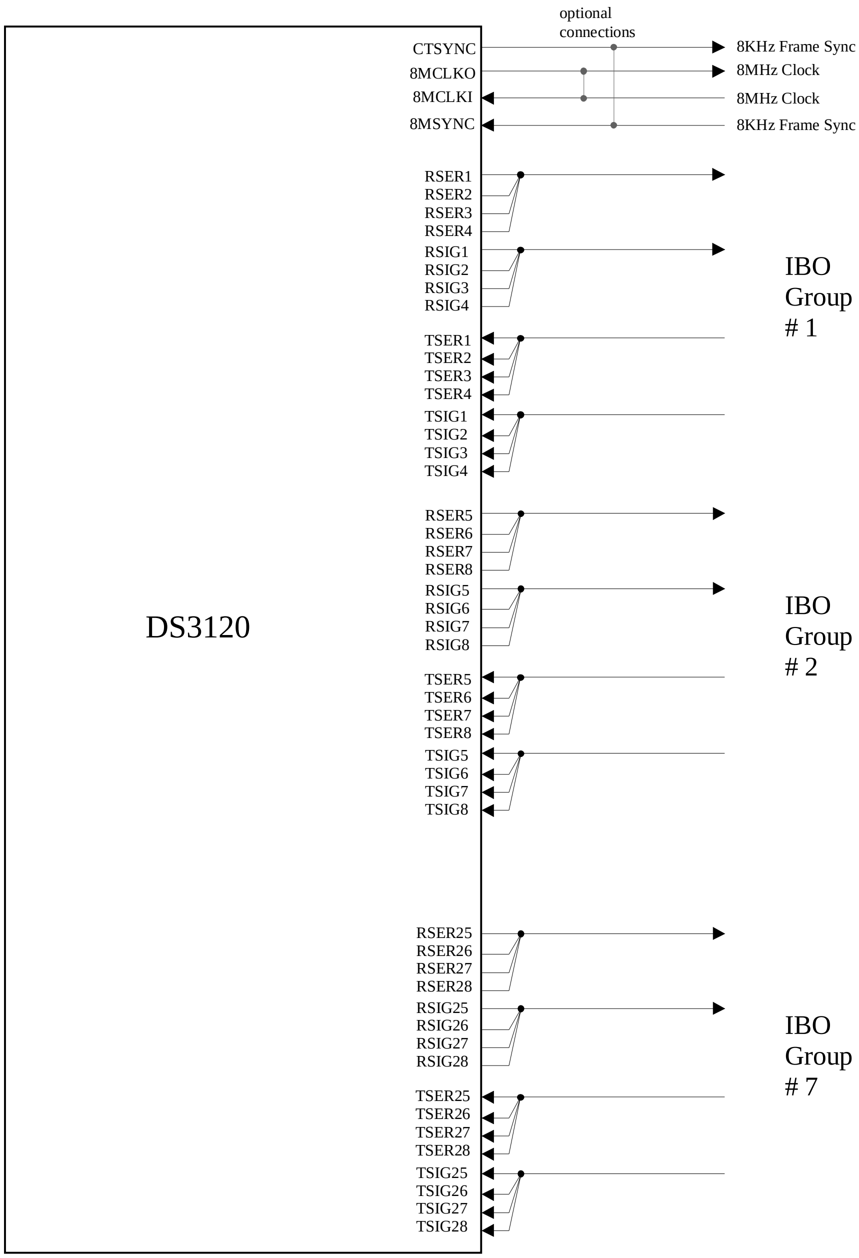
In IBO operation, the device must be supplied a 8 MHz clock and frame sync via the 8MCLKI and 8MSYNC inputs respectively and the elastic stores must be enabled via the TESE and RESE control bits in the CCR1 register (see Section 6). The clock and sync signals might be independently generated or they might be sourced from the 8MCLKO and CTSYNC outputs. The 28 T1 framers within the DS3120 are combined into seven groups of four framers each as shown below in Table 18-1 and in Figure 18-1. Within each IBO group, the four T1 datastreams can be either frame interleaved or byte interleaved. This selection is made via the INTSEL control bit in the IBO register. It is acceptable to have some IBO groups using frame interleaving and the others using byte interleaving. If the application requires frame interleaving, then the 8MCLKI clock must be frequency locked to RCLK (i.e., frame slips cannot occur). This restriction does not apply to byte interleaved applications (i.e., frame slips can occur).

IBO Group Assignment Table 18-1

IBO Group Number	Framers in the Group
1	1 / 2 / 3 / 4
2	5 / 6 / 7 / 8
3	9 / 10 / 11 / 12
4	13 / 14 / 15 / 16
5	17 / 18 / 19 / 20
6	21 / 22 / 23 / 24
7	25 / 26 / 27 / 28

The 8 MHz IBO bus contains 128 DS0 channels. Depending on whether the application is running byte interleaved or frame interleaved, the DS3120 will map the 24 channels of each of the four T1 frames into the 128 DS0 channels as shown in Table 18-2. The fourth channel from each framer will be forced to one. The F-bit will be passed through the device in the MSB of the first channel out of the device. Via TCR1.6, the MSB of the first channel can be sampled as the F-bit.

8 MHz INTERLEAVED BUS OPERATION EXTERNAL PIN CONNECTION
Figure 18-1



8 MHz IBO CHANNEL ASSIGNMENT Table 18-2

IBO Channel Number	Byte Interleaved Channel Assignment (only IBO Group #1 is listed)	Frame Interleaved Channel Assignment (only IBO Group #1 is listed)
1	Blank Channel (MSB contains the F Bit)	Blank Channel (MSB contains the F Bit)
2	Blank Channel (MSB contains the F Bit)	Framer 1 / T1 Channel 1
3	Blank Channel (MSB contains the F Bit)	Framer 1 / T1 Channel 2
4	Blank Channel (MSB contains the F Bit)	Framer 1 / T1 Channel 3
5	Framer 1 / T1 Channel 1	Blank Channel
6	Framer 2 / T1 Channel 1	Framer 1 / T1 Channel 4
7	Framer 3 / T1 Channel 1	Framer 1 / T1 Channel 5
8	Framer 4 / T1 Channel 1	Framer 1 / T1 Channel 6
9	Framer 1 / T1 Channel 2	Blank Channel
10	Framer 2 / T1 Channel 2	Framer 1 / T1 Channel 7
11	Framer 3 / T1 Channel 2	Framer 1 / T1 Channel 8
12	Framer 4 / T1 Channel 2	Framer 1 / T1 Channel 9
13	Framer 1 / T1 Channel 3	Blank Channel
14	Framer 2 / T1 Channel 3	Framer 1 / T1 Channel 10
15	Framer 3 / T1 Channel 3	Framer 1 / T1 Channel 11
16	Framer 4 / T1 Channel 3	Framer 1 / T1 Channel 12
17	Blank Channel	Blank Channel
18	Blank Channel	Framer 1 / T1 Channel 13
19	Blank Channel	Framer 1 / T1 Channel 14
20	Blank Channel	Framer 1 / T1 Channel 15
21	Framer 1 / T1 Channel 4	Blank Channel
22	Framer 2 / T1 Channel 4	Framer 1 / T1 Channel 16
23	Framer 3 / T1 Channel 4	Framer 1 / T1 Channel 17
24	Framer 4 / T1 Channel 4	Framer 1 / T1 Channel 18
25	Framer 1 / T1 Channel 5	Blank Channel
26	Framer 2 / T1 Channel 5	Framer 1 / T1 Channel 19
27	Framer 3 / T1 Channel 5	Framer 1 / T1 Channel 20
28	Framer 4 / T1 Channel 5	Framer 1 / T1 Channel 21
29	Framer 1 / T1 Channel 6	Blank Channel
30	Framer 2 / T1 Channel 6	Framer 1 / T1 Channel 22
31	Framer 3 / T1 Channel 6	Framer 1 / T1 Channel 23
32	Framer 4 / T1 Channel 6	Framer 1 / T1 Channel 24
33	Blank Channel	Blank Channel (MSB contains the F Bit)
34	Blank Channel	Framer 2 / T1 Channel 1
35	Blank Channel	Framer 2 / T1 Channel 2
36	Blank Channel	Framer 2 / T1 Channel 3
37	Framer 1 / T1 Channel 7	Blank Channel
38	Framer 2 / T1 Channel 7	Framer 2 / T1 Channel 4

IBO Channel Number	Byte Interleaved Channel Assignment (only IBO Group #1 is listed)	Frame Interleaved Channel Assignment (only IBO Group #1 is listed)
123	Framer 3 / T1 Channel 23	Framer 4 / T1 Channel 20
124	Framer 4 / T1 Channel 23	Framer 4 / T1 Channel 21
125	Framer 1 / T1 Channel 24	Blank Channel
126	Framer 2 / T1 Channel 24	Framer 4 / T1 Channel 22
127	Framer 3 / T1 Channel 24	Framer 4 / T1 Channel 23
128	Framer 4 / T1 Channel 24	Framer 4 / T1 Channel 24

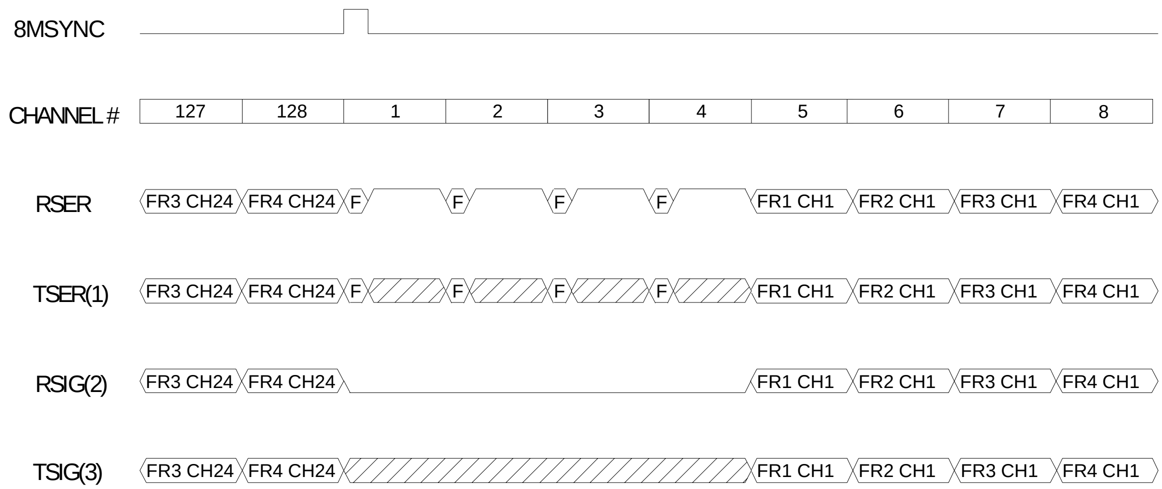
IBO: INTERLEAVE BUS OPERATION REGISTER (Address = 94 Hex)

(MSB)							(LSB)
-	-	-	-	IBOEN	INTSEL	MSEL0	MSEL1

SYMBOL	POSITION	NAME AND DESCRIPTION
-	IBO.6	**Not Assigned.** Should be set to 0.
-	IBO.6	**Not Assigned.** Should be set to 0.
-	IBO.5	**Not Assigned.** Should be set to 0.
-	IBO.4	**Not Assigned.** Should be set to 0.
IBOEN	IBO.3	**Interleave Bus Operation Enable.** This bit should be set to one in Modes 9 & 10. Set to zero in all other Modes. 0 = Interleave Bus Operation disabled. 1 = Interleave Bus Operation enabled.
INTSEL	IBO.2	**Interleave Type Select.** 0 = Byte interleave. 1 = Frame interleave.
MSEL0	IBO.1	**Master Device Bus Select Bit 0.** Should be set to zero.
MSEL1	IBO.0	**Master Device Bus Select Bit 1.** Should be set to zero on framers 2 / 3 / 4 / 6 / 7 / 8 / 10 / 11 / 12 / 14 / 15 / 16 / 18 / 19 / 20 / 22 / 23 / 24 / 26 / 27 / 28. Should be set to one on framers 1 / 5 / 9 / 13 / 17 / 21 / 25.

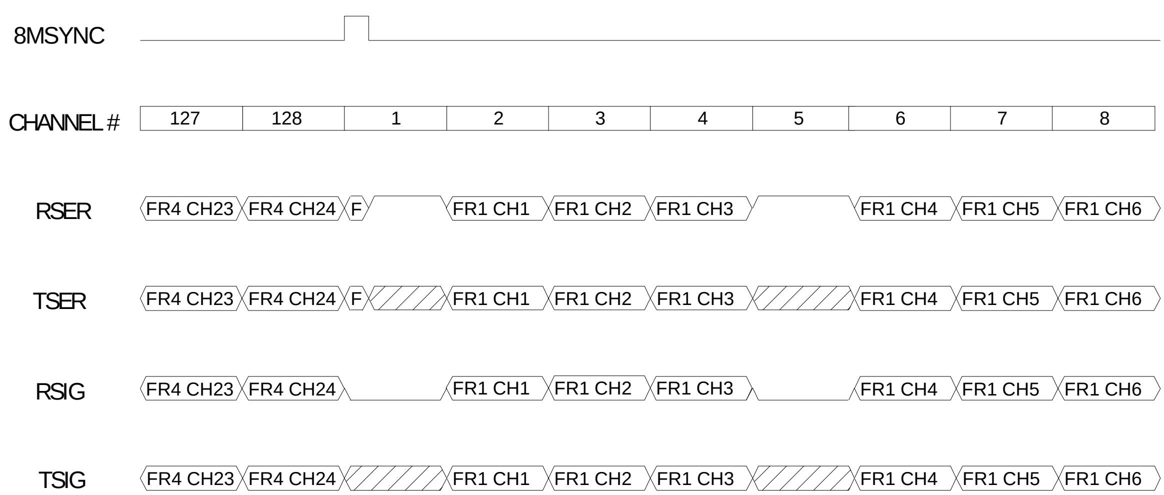
8 MHz INTERLEAVED BUS OPERATION TIMING (BYTE INTERLEAVING)
Figure 18-2

(only IBO Group #1 is shown; other IBO Groups operate in a similar fashion)



8 MHz INTERLEAVED BUS OPERATION TIMING (FRAME INTERLEAVING)
Figure 18-3

(only IBO Group #1 is shown; other IBO Groups operate in a similar fashion)



19. JTAG-BOUNDARY SCAN ARCHITECTURE AND TEST ACCESS PORT

19.1 DESCRIPTION

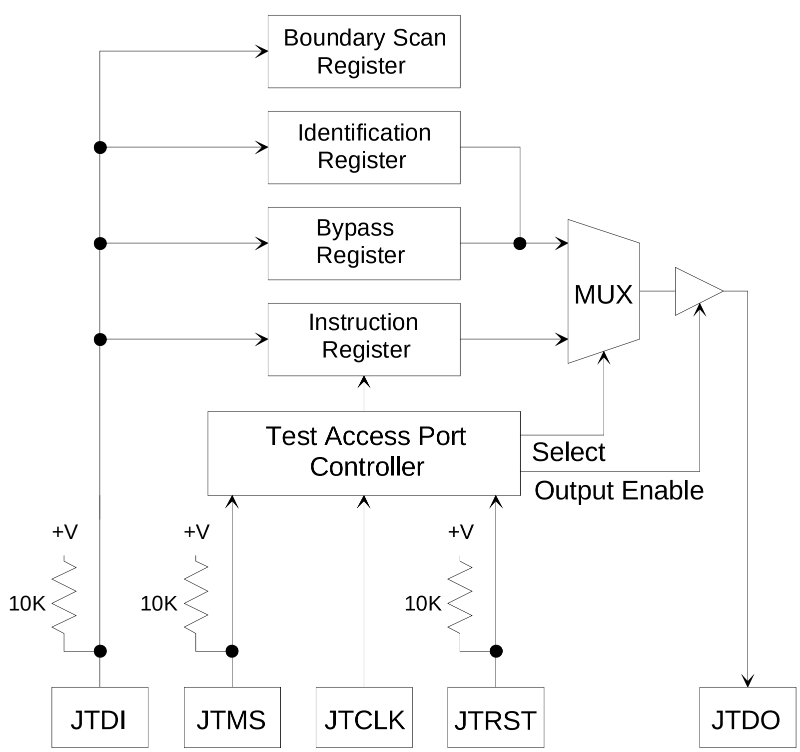
The DS3120 IEEE 1149.1 design supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included with this design are HIGHZ, CLAMP, and IDCODE. See Figure 19-1 for a block diagram. The DS3120 contains the following items, which meet the requirements, set by the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture.

Test Access Port (TAP)
TAP Controller
Instruction Register
Bypass Register
Boundary Scan Register
Device Identification Register

Details on Boundary Scan Architecture and the Test Access Port can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

The Test Access Port has the necessary interface pins; JTRST*, JTCLK, JTMS, JTDI, and JTDO. See the signal descriptions for details.

BOUNDARY SCAN ARCHITECTURE Figure 19-1



19.2 TAP CONTROLLER STATE MACHINE

This section covers the details on the operation of the Test Access Port (TAP) Controller State Machine. Please see Figure 19.2 for details on each of the states described below.

TAP Controller

The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK.

Test-Logic-Reset

Upon power up of the DS3120, the TAP Controller will be in the Test-Logic-Reset state. The Instruction register will contain the IDCODE instruction. All system logic of the DS3120 will operate normally.

Run-Test-Idle

The Run-Test-Idle is used between scan operations or during specific tests. The Instruction register and Test registers will remain idle.

Select-DR-Scan

All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and will initiate a scan sequence. JTMS HIGH during a rising edge on JTCLK moves the controller to the Select-IR

Capture-DR

Data may be parallel-loaded into the Test Data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the Test register will remain at its current value. On the rising edge of JTCLK, the controller will go to the Shift-DR state if JTMS is low or it will go to the Exit1-DR state if JTMS is high.

Shift-DR

The Test Data register selected by the current instruction will be connected between JTDI and JTDO and will shift data one stage towards its serial output on each rising edge of JTCLK. If a Test Register selected by the current instruction is not placed in the serial path, it will maintain its previous state.

Exit1-DR

While in this state, a rising edge on JTCLK with JTMS high will put the controller in the Update-DR state, and terminate the scanning process. A rising edge on JTCLK with JTMS low will put the controller in the Pause-DR state.

Pause-DR

Shifting of the test registers is halted while in this state. All Test registers selected by the current instruction will retain their previous state. The controller will remain in this state while JTMS is low. A rising edge on JTCLK with JTMS high will put the controller in the Exit2-DR state.

Exit2-DR

While in this state, a rising edge on JTCLK with JTMS high will put the controller in the Update-DR state and terminate the scanning process. A rising edge on JTCLK with JTMS low will enter the Shift-DR state.

Update-DR

A falling edge on JTCLK while in the Update-DR state will latch the data from the shift register path of the Test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register. A rising edge on JTCLK with JTMS low, will put the controller in the Run-Test-Idle state. With JTMS high, the controller will enter the Select-DR-Scan state.

Select-IR-Scan

All test registers retain their previous state. The instruction register will remain unchanged during this state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-IR state and will initiate a scan sequence for the Instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR

The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller will enter the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller will enter the Shift-IR state.

Shift-IR

In this state, the shift register in the instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK towards the serial output. The parallel registers, as well as all Test registers remain at their previous states. A rising edge on JTCLK with JTMS high will move the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low will keep the controller in the Shift-IR state while moving data one stage thorough the instruction shift register.

Exit1-IR

A rising edge on JTCLK with JTMS low will put the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller will enter the Update-IR state and terminate the scanning process.

Pause-IR

Shifting of the instruction shift register is halted temporarily. With JTMS high, a rising edge on JTCLK will put the controller in the Exit2-IR state. The controller will remain in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

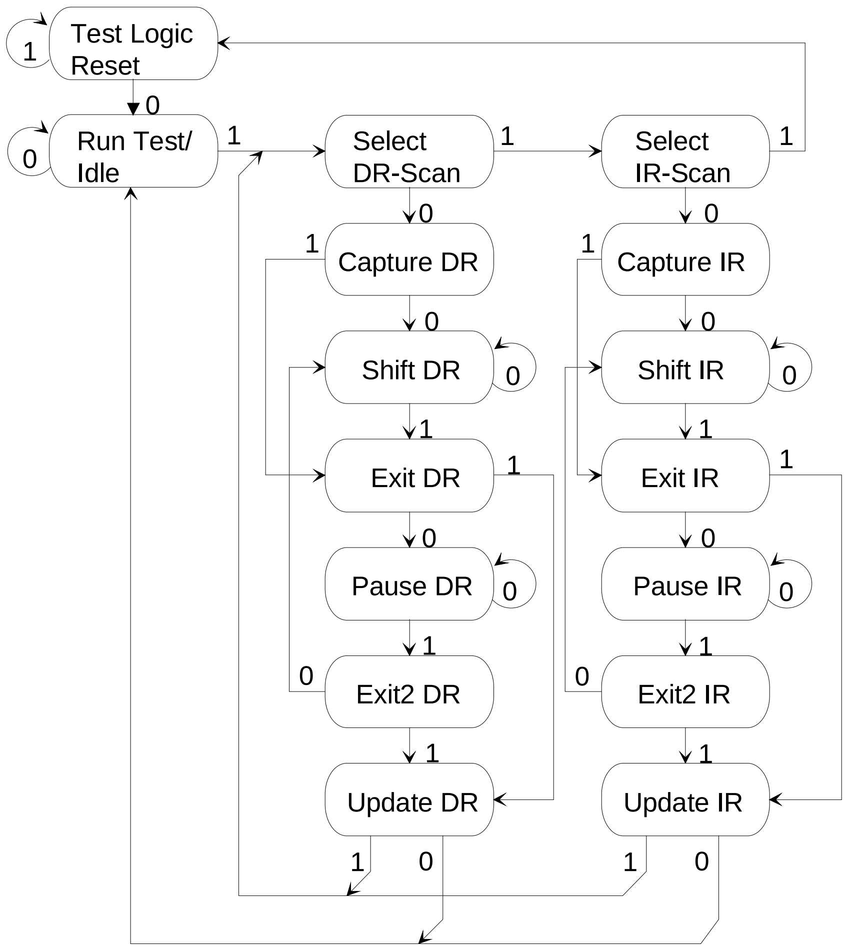
Exit2-IR

A rising edge on JTCLK with JTMS low will put the controller in the Update-IR state. The controller will loop back to Shift-IR if JTMS is high during a rising edge of JTCLK in this state.

Update-IR

The instruction code shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS low, will put the controller in the Run-Test-Idle state. With JTMS high, the controller will enter the Select-DR-Scan state.

TAP Controller State Machine Figure 19-2



19.3 INSTRUCTION REGISTER AND INSTRUCTIONS

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register will be connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low will shift the data one stage towards the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high will move the controller to the Update-IR state. The falling edge of that same JTCLK will latch the data in the instruction shift register to the instruction parallel output. Instructions supported by the DS3120 with their respective operational binary codes are shown in Table 19-1.

Instruction Codes Table 19-1

Instruction	Selected Register	Instruction Codes
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Boundary Scan	011
HIGHZ	Boundary Scan	100
IDCODE	Device Identification	001

SAMPLE/PRELOAD

A mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. The digital I/Os of the DS3120 can be sampled at the boundary scan register without interfering with the normal operation of the device by using the Capture-DR state. SAMPLE/PRELOAD also allows the DS3120 to shift data into the boundary scan register via JTDI using the Shift-DR state.

EXTEST

EXTEST allows testing of all interconnections to the DS3120. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled via the Update-IR state, the parallel outputs of all digital output pins will be driven. The boundary scan register will be connected between JTDI and JTDO. The Capture-DR will sample all digital inputs into the boundary scan register.

BYPASS

When the BYPASS instruction is latched into the parallel instruction register, JTDI connects to JTDO through the 1-bit bypass test register. This allows data to pass from JTDI to JTDO not affecting the device’s normal operation.

IDCODE

When the IDCODE instruction is latched into the parallel instruction register, the Identification Test register is selected. The device identification code will be loaded into the Identification register on the rising edge of JTCLK following entry into the Capture-DR state. Shift-DR can be used to shift the identification code out serially via JTDO. During Test-Logic-Reset, the identification code is forced into the instruction register’s parallel output. The ID code will always have a ‘1’ in the LSB position. The next 11 bits identify the manufacturer’s JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version. The device ID code for the DS3120 is **0000C143h**.

HIGHZ
All digital outputs of the DS3120 will be placed in a high impedance state. The BYPASS register will be connected between JTDI and JTDO.

CLAMP
All digital outputs of the DS3120 will output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs will not change during the CLAMP instruction.

19.4 TEST REGISTERS
IEEE 1149.1 requires a minimum of two test registers; the bypass register and the boundary scan register. An optional test register has been included with the DS3120 design. This test register is the identification register and is used in conjunction with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

Boundary Scan Register
This register contains both a shift register path and a latched parallel output for all control cells and digital I/O cells and is 321 bits in length. Table 19-2 shows all of the cell bit locations and definitions.

Bypass Register
This is a single 1-bit shift register used in conjunction with the BYPASS, CLAMP, and HIGHZ instructions, which provides a short path between JTDI and JTDO.

Identification Register
The identification register contains a 32-bit shift register and a 32-bit latched parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state.

BOUNDARY SCAN REGISTER DESCRIPTION Table 19-2

Bit	Symbol	Lead	I/O or Control Bit Description
1	MODE0	C2	I
2	MODE1	E4	I
3	MODE2	E3	I
4	MODE3	D2	I
5	RNRZ28	C1	I
6	RCLK28	F3	I
7	TNRZ28	F4	O
8	RNRZ27	E2	I
9	RCLK27	D1	I
10	TNRZ27	F2	O
11	RNRZ26	G5	I
12	RCLK26	G4	I
13	TNRZ26	G3	O
14	RNRZ25	E1	I
15	RCLK25	F1	I
16	TNRZ25	G2	O
17	RNRZ24	H4	I
18	RCLK24	H5	I
19	TNRZ24	H3	O
20	RNRZ23	G1	I
21	RCLK23	H2	I
22	TNRZ23	J3	O
23	RNRZ22	J4	I
24	RCLK22	J5	I
25	TNRZ22	J2	O
26	RNRZ21	J1	I
27	RCLK21	K1	I
28	TNRZ21	K3	O
29	RNRZ20	K4	I
30	RCLK20	K5	I
31	TNRZ20	K2	O
32	RNRZ19	L1	I
33	RCLK19	M1	I
34	TNRZ19	L2	O
35	RNRZ18	L3	I
36	RCLK18	L4	I
37	TNRZ18	L5	O
38	RNRZ17	M2	I
39	RCLK17	N1	I
40	TNRZ17	M3	O
41	RNRZ16	N2	I
42	RCLK16	M5	I
43	TNRZ16	M4	O
44	RNRZ15	P1	I

Bit	Symbol	Lead	I/O or Control Bit Description
45	RCLK15	N3	I
46	TNRZ15	R1	O
47	RNRZ14	P2	I
48	RCLK14	N5	I
49	TNRZ14	N4	O
50	RNRZ13	T1	I
51	RCLK13	P3	I
52	TNRZ13	R2	O
53	RNRZ12	P5	I
54	RCLK12	P4	I
55	TNRZ12	T2	O
56	RNRZ11	R3	I
57	RCLK11	V1	I
58	TNRZ11	W1	O
59	RNRZ10	Y1	I
60	RCLK10	R4	I
61	TNRZ10	U2	O
62	RNRZ9	T3	I
63	RCLK9	V2	I
64	TNRZ9	W2	O
65	RNRZ8	T4	I
66	RCLK8	U3	I
67	TNRZ8	V3	O
68	RNRZ7	U5	I
69	RCLK7	V5	I
70	TNRZ7	W4	O
71	RNRZ6	Y2	I
72	RCLK6	Y3	I
73	TNRZ6	U6	O
74	RNRZ5	T7	I
75	RCLK5	V6	I
76	TNRZ5	W5	O
77	RNRZ4	Y4	I
78	RCLK4	U7	I
79	TNRZ4	W6	O
80	RNRZ3	V7	I
81	RCLK3	Y5	I
82	TNRZ3	W7	O
83	RNRZ2	U8	I
84	RCLK2	T8	I
85	TNRZ2	Y6	O
86	RNRZ1	V8	I
87	RCLK1	Y7	I
88	TNRZ1	W8	O
89	RSYNC28	U9	O
90	RSER28	T9	O

Bit	Symbol	Lead	I/O or Control Bit Description
91	TCLK28/RSIG28.cntl	-	0 = TCLK28/RSIG28 is an input 1 = TCLK28/RSIG28 is an output
92	TCLK28/RSIG28	V9	I/O
93	TSER28	W9	I
94	TSYNC28/TSIG28.cntl	-	0 = TSYNC28/TSIG28 is an input 1 = TSYNC28/TSIG28 is an output
95	TSYNC28/TSIG28	Y9	I/O
96	RSYNC27	V10	O
97	RSER27	U10	O
98	TCLK27/RSIG27.cntl	-	0 = TCLK27/RSIG27 is an input 1 = TCLK27/RSIG27 is an output
99	TCLK27/RSIG27	T10	I/O
100	TSER27	W10	I
101	TSYNC27/TSIG27.cntl	-	0 = TSYNC27/TSIG27 is an input 1 = TSYNC27/TSIG27 is an output
102	TSYNC27/TSIG27	Y10	I/O
103	RSYNC26	Y11	O
104	RSER26	W11	O
105	TCLK26/RSIG26.cntl	-	0 = TCLK26/RSIG26 is an input 1 = TCLK26/RSIG26 is an output
106	TCLK26/RSIG26	V11	I/O
107	TSER26	U11	I
108	TSYNC26/TSIG26.cntl	-	0 = TSYNC26/TSIG26 is an input 1 = TSYNC26/TSIG26 is an output
109	TSYNC26/TSIG26	Y12	I/O
110	RSYNC25	W12	O
111	RSER25	Y13	O
112	TCLK25/RSIG25.cntl	-	0 = TCLK25/RSIG25 is an input 1 = TCLK25/RSIG25 is an output
113	TCLK25/RSIG25	V12	I/O
114	TSER25	T11	I
115	TSYNC25/TSIG25.cntl	-	0 = TSYNC25/TSIG25 is an input 1 = TSYNC25/TSIG25 is an output
116	TSYNC25/TSIG25	T12	I/O
117	RSYNC24	U12	O
118	RSER24	W13	O
119	TCLK24/RSIG24.cntl	-	0 = TCLK24/RSIG24 is an input 1 = TCLK24/RSIG24 is an output
120	TCLK24/RSIG24	Y14	I/O
121	TSER24	Y15	I

Bit	Symbol	Lead	I/O or Control Bit Description
122	TSYNC24/TSIG24.cntl	-	0 = TSYNC24/TSIG24 is an input 1 = TSYNC24/TSIG24 is an output
123	TSYNC24/TSIG24	V13	I/O
124	RSYNC23	T13	O
125	RSER23	U13	O
126	TCLK23/RSIG23.cntl	-	0 = TCLK23/RSIG23 is an input 1 = TCLK23/RSIG23 is an output
127	TCLK23/RSIG23	W14	I/O
128	TSER23	Y16	I
129	TSYNC23/TSIG23.cntl	-	0 = TSYNC23/TSIG23 is an input 1 = TSYNC23/TSIG23 is an output
130	TSYNC23/TSIG23	W15	I/O
131	RSYNC22	V14	O
132	RSER22	T14	O
133	TCLK22/RSIG22.cntl	-	0 = TCLK22/RSIG22 is an input 1 = TCLK22/RSIG22 is an output
134	TCLK22/RSIG22	U14	I/O
135	TSER22	W16	I
136	TSYNC22/TSIG22.cntl	-	0 = TSYNC22/TSIG22 is an input 1 = TSYNC22/TSIG22 is an output
137	TSYNC22/TSIG22	V15	I/O
138	RSYNC21	Y18	O
139	RSER21	Y19	O
140	TCLK21/RSIG21.cntl	-	0 = TCLK21/RSIG21 is an input 1 = TCLK21/RSIG21 is an output
141	TCLK21/RSIG21	U15	I/O
142	TSER21	Y20	I
143	TSYNC21/TSIG21.cntl	-	0 = TSYNC21/TSIG21 is an input 1 = TSYNC21/TSIG21 is an output
144	TSYNC21/TSIG21	W17	I/O
145	RSYNC20	V16	O
146	RSER20	W18	O
147	TCLK20/RSIG20.cntl	-	0 = TCLK20/RSIG20 is an input 1 = TCLK20/RSIG20 is an output
148	TCLK20/RSIG20	V17	I/O
149	TSER20	U16	I
150	TSYNC20/TSIG20.cntl	-	0 = TSYNC20/TSIG20 is an input 1 = TSYNC20/TSIG20 is an output
151	TSYNC20/TSIG20	U17	I/O
152	RSYNC19	T16	O
153	RSER19	V18	O
154	TCLK19/RSIG19.cntl	-	0 = TCLK19/RSIG19 is an input 1 = TCLK19/RSIG19 is an output
155	TCLK19/RSIG19	W19	I/O
156	TSER19	U18	I

Bit	Symbol	Lead	I/O or Control Bit Description
157	TSYNC19/TSIG19.cntl	-	0 = TSYNC19/TSIG19 is an input 1 = TSYNC19/TSIG19 is an output
158	TSYNC19/TSIG19	V19	I/O
159	RSYNC18	T17	O
160	RSER18	T18	O
161	TCLK18/RSIG18.cntl	-	0 = TCLK18/RSIG18 is an input 1 = TCLK18/RSIG18 is an output
162	TCLK18/RSIG18	U19	I/O
163	TSER18	W20	I
164	TSYNC18/TSIG18.cntl	-	0 = TSYNC18/TSIG18 is an input 1 = TSYNC18/TSIG18 is an output
165	TSYNC18/TSIG18	V20	I/O
166	RSYNC17	R17	O
167	RSER17	P16	O
168	TCLK17/RSIG17.cntl	-	0 = TCLK17/RSIG17 is an input 1 = TCLK17/RSIG17 is an output
169	TCLK17/RSIG17	R18	I/O
170	TSER17	T19	I
171	TSYNC17/TSIG17.cntl	-	0 = TSYNC17/TSIG17 is an input 1 = TSYNC17/TSIG17 is an output
172	TSYNC17/TSIG17	U20	I/O
173	RSYNC16	P17	O
174	RSER16	R19	O
175	TCLK16/RSIG16.cntl	-	0 = TCLK16/RSIG16 is an input 1 = TCLK16/RSIG16 is an output
176	TCLK16/RSIG16	P18	I/O
177	TSER16	T20	I
178	TSYNC16/TSIG16.cntl	-	0 = TSYNC16/TSIG16 is an input 1 = TSYNC16/TSIG16 is an output
179	TSYNC16/TSIG16	P19	I/O
180	RSYNC15	N17	O
181	RSER15	N16	O
182	TCLK15/RSIG15.cntl	-	0 = TCLK15/RSIG15 is an input 1 = TCLK15/RSIG15 is an output
183	TCLK15/RSIG15	N18	I/O
184	TSER15	P20	I
185	TSYNC15/TSIG15.cntl	-	0 = TSYNC15/TSIG15 is an input 1 = TSYNC15/TSIG15 is an output
186	TSYNC15/TSIG15	N19	I/O
187	RSYNC14	N20	O
188	RSER14	M17	O
189	TCLK14/RSIG14.cntl	-	0 = TCLK14/RSIG14 is an input 1 = TCLK14/RSIG14 is an output
190	TCLK14/RSIG14	M16	I/O
191	TSER14	M18	I

Bit	Symbol	Lead	I/O or Control Bit Description
192	TSYNC14/TSIG14.cntl	-	0 = TSYNC14/TSIG14 is an input 1 = TSYNC14/TSIG14 is an output
193	TSYNC14/TSIG14	M19	I/O
194	RSYNC13	M20	O
195	RSER13	L17	O
196	TCLK13/RSIG13.cntl	-	0 = TCLK13/RSIG13 is an input 1 = TCLK13/RSIG13 is an output
197	TCLK13/RSIG13	L16	I/O
198	TSER13	L18	I
199	TSYNC13/TSIG13.cntl	-	0 = TSYNC13/TSIG13 is an input 1 = TSYNC13/TSIG13 is an output
200	TSYNC13/TSIG13	L19	I/O
201	RSYNC12	L20	O
202	RSER12	K20	O
203	TCLK12/RSIG12.cntl	-	0 = TCLK12/RSIG12 is an input 1 = TCLK12/RSIG12 is an output
204	TCLK12/RSIG12	K19	I/O
205	TSER12	K17	I
206	TSYNC12/TSIG12.cntl	-	0 = TSYNC12/TSIG12 is an input 1 = TSYNC12/TSIG12 is an output
207	TSYNC12/TSIG12	K18	I/O
208	RSYNC11	J20	O
209	RSER11	J19	O
210	TCLK11/RSIG11.cntl	-	0 = TCLK11/RSIG11 is an input 1 = TCLK11/RSIG11 is an output
211	TCLK11/RSIG11	J18	I/O
212	TSER11	K16	I
213	TSYNC11/TSIG11.cntl	-	0 = TSYNC11/TSIG11 is an input 1 = TSYNC11/TSIG11 is an output
214	TSYNC11/TSIG11	J16	I/O
215	RSYNC10	J17	O
216	RSER10	H20	O
217	TCLK10/RSIG10.cntl	-	0 = TCLK10/RSIG10 is an input 1 = TCLK10/RSIG10 is an output
218	TCLK10/RSIG10	H19	I/O
219	TSER10	G20	I
220	TSYNC10/TSIG10.cntl	-	0 = TSYNC10/TSIG10 is an input 1 = TSYNC10/TSIG10 is an output
221	TSYNC10/TSIG10	H18	I/O
222	RSYNC9	H16	O
223	RSER9	H17	O
224	TCLK9/RSIG9.cntl	-	0 = TCLK9/RSIG9 is an input 1 = TCLK9/RSIG9 is an output
225	TCLK9/RSIG9	F20	I/O
226	TSER9	G19	I

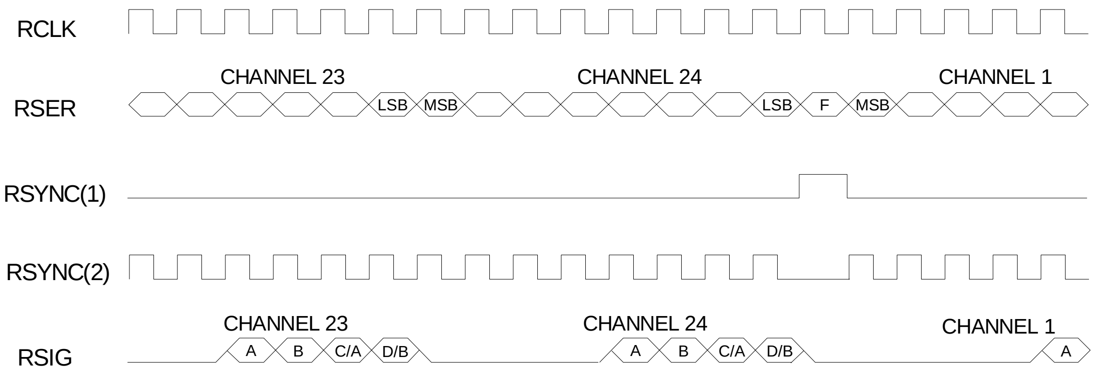
Bit	Symbol	Lead	I/O or Control Bit Description
227	TSYNC9/TSIG9.cntl	-	0 = TSYNC9/TSIG9 is an input 1 = TSYNC9/TSIG9 is an output
228	TSYNC9/TSIG9	G18	I/O
229	RSYNC8	G16	O
230	RSER8	G17	O
231	TCLK8/RSIG8.cntl	-	0 = TCLK8/RSIG8 is an input 1 = TCLK8/RSIG8 is an output
232	TCLK8/RSIG8	F19	I/O
233	TSER8	D20	I
234	TSYNC8/TSIG8.cntl	-	0 = TSYNC8/TSIG8 is an input 1 = TSYNC8/TSIG8 is an output
235	TSYNC8/TSIG8	E19	I/O
236	RSYNC7	F18	O
237	RSER7	C20	O
238	TCLK7/RSIG7.cntl	-	0 = TCLK7/RSIG7 is an input 1 = TCLK7/RSIG7 is an output
239	TCLK7/RSIG7	F17	I/O
240	TSER7	B20	I
241	TSYNC7/TSIG7.cntl	-	0 = TSYNC7/TSIG7 is an input 1 = TSYNC7/TSIG7 is an output
242	TSYNC7/TSIG7	D19	I/O
243	RSYNC6	E18	O
244	RSER6	E17	O
245	TCLK6/RSIG6.cntl	-	0 = TCLK6/RSIG6 is an input 1 = TCLK6/RSIG6 is an output
246	TCLK6/RSIG6	C19	I/O
247	TSER6	C17	I
248	TSYNC6/TSIG6.cntl	-	0 = TSYNC6/TSIG6 is an input 1 = TSYNC6/TSIG6 is an output
249	TSYNC6/TSIG6	B19	I/O
250	RSYNC5	B18	O
251	RSER5	D16	O
252	TCLK5/RSIG5.cntl	-	0 = TCLK5/RSIG5 is an input 1 = TCLK5/RSIG5 is an output
253	TCLK5/RSIG5	C16	I/O
254	TSER5	B17	I
255	TSYNC5/TSIG5.cntl	-	0 = TSYNC5/TSIG5 is an input 1 = TSYNC5/TSIG5 is an output
256	TSYNC5/TSIG5	A20	I/O
257	RSYNC4	A19	O
258	RSER4	E14	O
259	TCLK4/RSIG4.cntl	-	0 = TCLK4/RSIG4 is an input 1 = TCLK4/RSIG4 is an output
260	TCLK4/RSIG4	D15	I/O
261	TSER4	A18	I

Bit	Symbol	Lead	I/O or Control Bit Description
262	TSYNC4/TSIG4.cntl	-	0 = TSYNC4/TSIG4 is an input 1 = TSYNC4/TSIG4 is an output
263	TSYNC4/TSIG4	C15	I/O
264	RSYNC3	B16	O
265	RSER3	D14	O
266	TCLK3/RSIG3.cntl	-	0 = TCLK3/RSIG3 is an input 1 = TCLK3/RSIG3 is an output
267	TCLK3/RSIG3	A17	I/O
268	TSER3	B15	I
269	TSYNC3/TSIG3.cntl	-	0 = TSYNC3/TSIG3 is an input 1 = TSYNC3/TSIG3 is an output
270	TSYNC3/TSIG3	C14	I/O
271	RSYNC2	A16	O
272	RSER2	D13	O
273	TCLK2/RSIG2.cntl	-	0 = TCLK2/RSIG2 is an input 1 = TCLK2/RSIG2 is an output
274	TCLK2/RSIG2	E13	I/O
275	TSER2	B14	I
276	TSYNC2/TSIG2.cntl	-	0 = TSYNC2/TSIG2 is an input 1 = TSYNC2/TSIG2 is an output
277	TSYNC2/TSIG2	C13	I/O
278	RSYNC1	A14	O
279	RSER1	B13	O
280	TCLK1/RSIG1.cntl	-	0 = TCLK1/RSIG1 is an input 1 = TCLK1/RSIG1 is an output
281	TCLK1/RSIG1	D12	I/O
282	TSER1	E12	I
283	TSYNC1/TSIG1.cntl	-	0 = TSYNC1/TSIG1 is an input 1 = TSYNC1/TSIG1 is an output
284	TSYNC1/TSIG1	A13	I/O
285	8MCLKO	C12	O
286	CLKSI	B12	I
287	CTCLK	A12	I
288	CTSYNC	D11	O
289	8MSYNC	E11	I
290	8MCLKI	C11	I
291	BTS	B11	I
292	WR*/(R/W*)	A11	I
293	RD*/(DS*)	A10	I
294	INT.cntl	-	0 = INT* is a zero (“0”) 1 = INT* is 3-state (“z”)
295	INT*	B10	O
296	BUS.cntl	-	0 = D0 to D7 or AD0 to AD7 is an input 1 = D0 to D7 or AD0 to AD7 is an output

Bit	Symbol	Lead	I/O or Control Bit Description
297	D0 or AD0	D10	I/O
298	D1 or AD1	C10	I/O
299	D2 or AD2	A9	I/O
300	D3 or AD3	B9	I/O
301	D4 or AD4	C9	I/O
302	D5 or AD5	E10	I/O
303	D6 or AD6	E9	I/O
304	D7 or AD7	D9	I/O
305	A0	A8	I
306	A1	B8	I
307	A2	A7	I
308	A3	C8	I
309	A4	E8	I
310	A5	D8	I
311	A6/ALE (AS)	A6	I
312	A7	B7	I
313	FS0	C7	I
314	FS1	E7	I
315	FS2	D7	I
316	FS3	B6	I
317	FS4	A4	I
318	CS*	B5	I
319	MUX	C6	I
320	FIACT*	A3	I
321	TEST	D6	I

20. TIMING DIAGRAMS

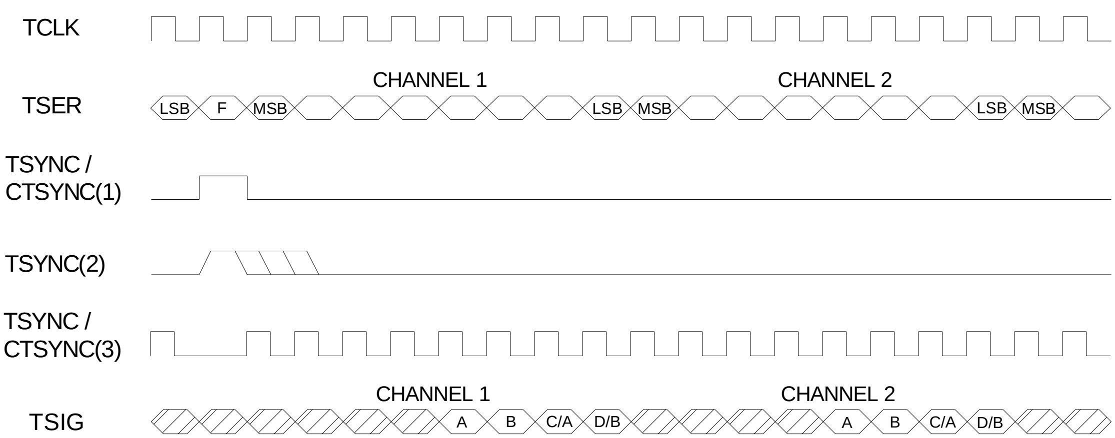
RECEIVE SIDE BOUNDARY TIMING Figure 20-1



Notes:

1. RSYNC outputting an 8 kHz frame pulse (Modes 1, 3, 5, 7, 9, 10, and 12).
2. RSYNC outputting a “Gapped Clock” (Modes 2, 4, 6, 8, and 13).

TRANSMIT SIDE BOUNDARY TIMING Figure 20-2

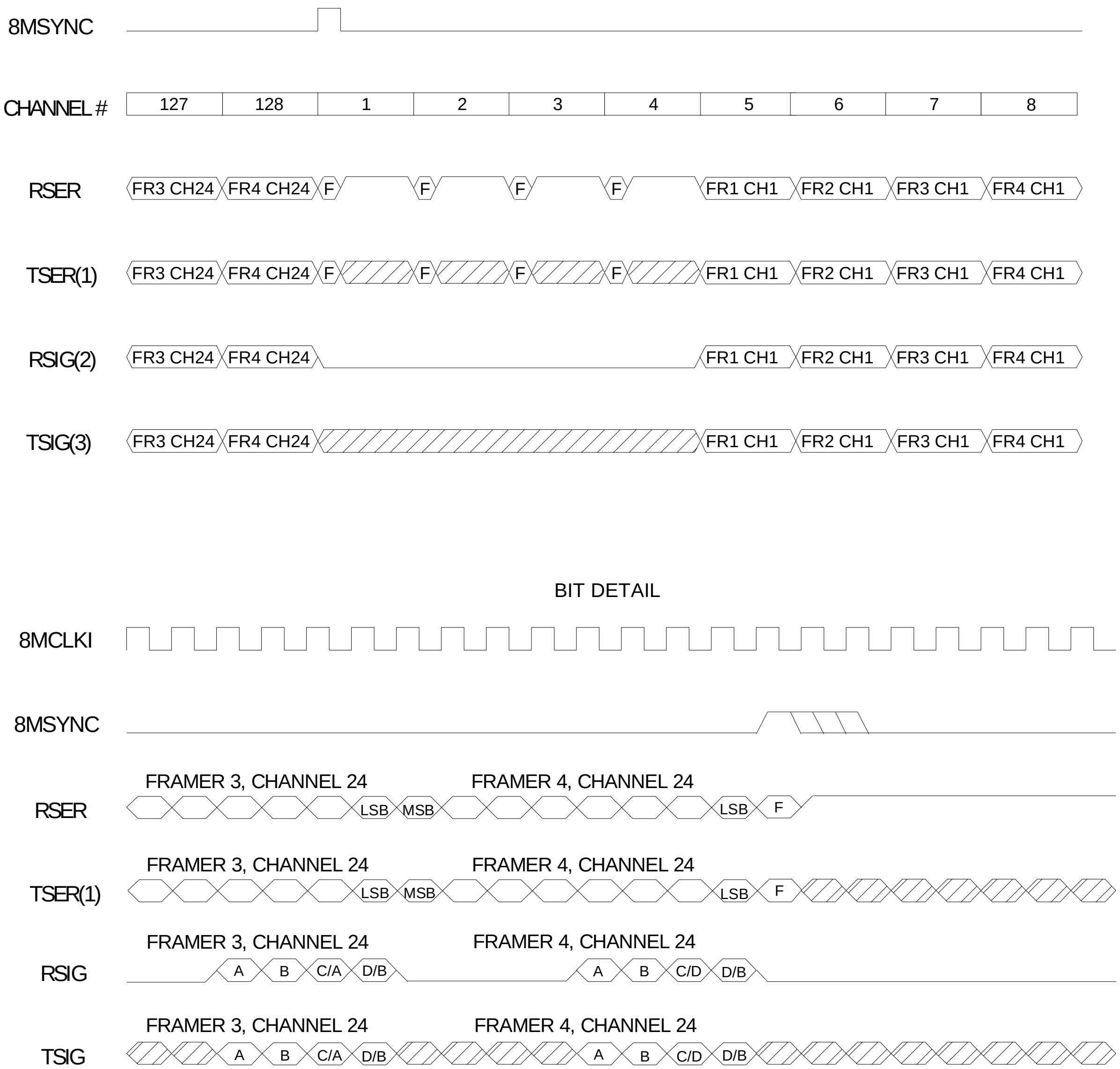


Notes:

1. TSYNC/CTSYNC is an 8 kHz frame boundary output (Modes 1, 3, 7, 9, 10, and 12).
2. TSYNC is an 8 kHZ frame boundary input (Mode 11).
3. TSYNC/CTSYNC is a “Gapped Clock” output (Modes 2, 4, 8, and 13).

8 MHZ INTERLEAVED BUS OPERATION (IBO) BYTE MODE TIMING

Figure 20-3

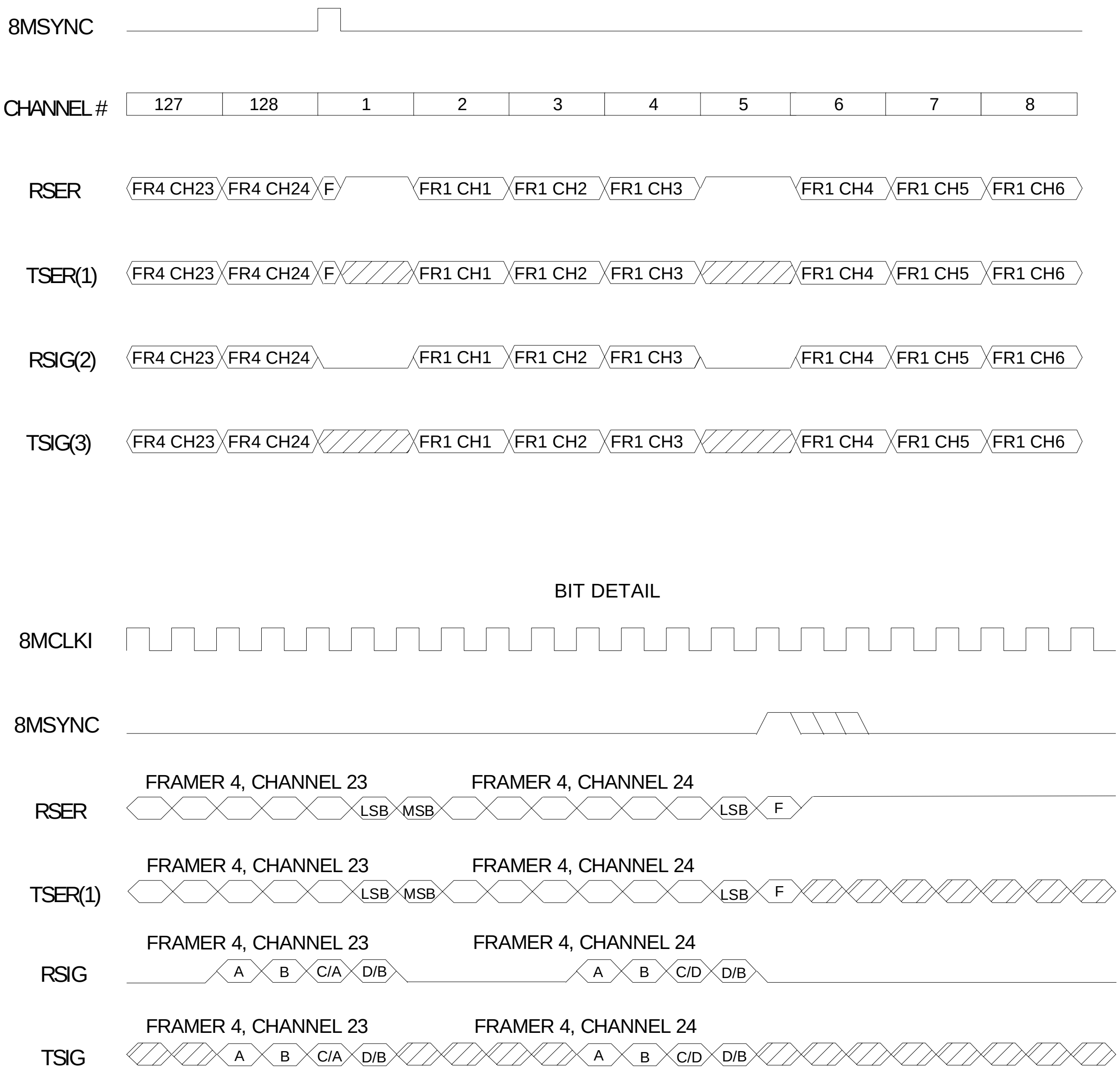


Notes:

1. TSER will only sample the F bit position when the transmit formatter is in "transparent" mode.
2. RSIG contains robbed bit signaling data in the least significant nibble.
3. TSIG samples robbed bit signaling data in the least significant nibble.

8 MHZ INTERLEAVED BUS OPERATION (IBO) FRAME MODE TIMING

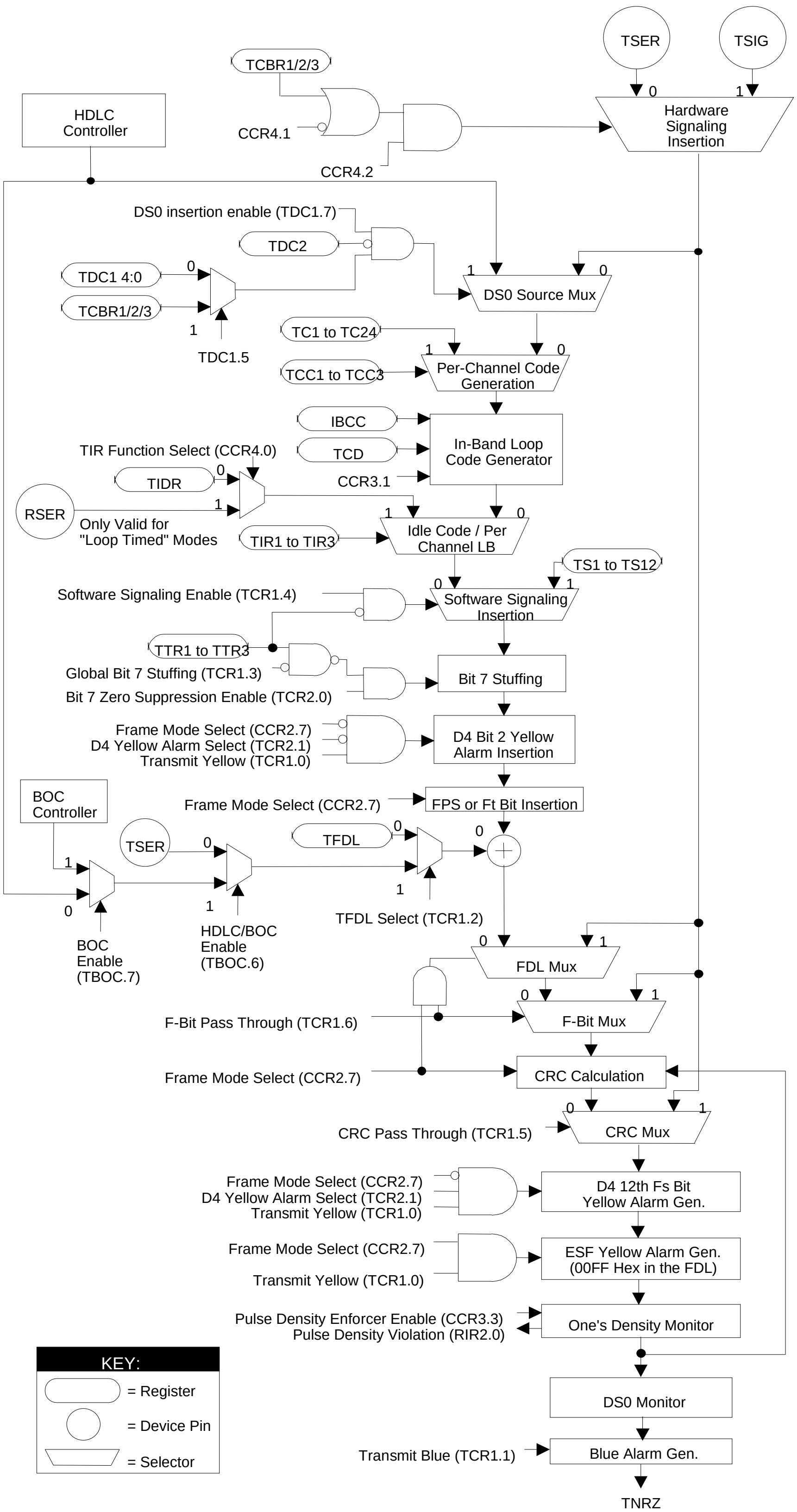
Figure 20-4



Notes:

1. TSER will only sample the F bit position when the transmit formatter is in “transparent” mode.
2. RSIG contains robbed bit signaling data in the least significant nibble.
3. TSIG samples robbed bit signaling data in the least significant nibble.

DS3120 TRANSMIT DATA FLOW Figure 20-5



21. OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Non-Supply Pin Relative to Ground	–1.0V to +5.5V
Core Supply Voltage (VDD_CORE)	-0.3V to +1.98V
I/O Supply Voltage (VDD_IO)	-0.3V to +3.63V
Operating Temperature for DS3120	0°C to 70°C
Operating Temperature for DS3120N	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	See J-STD-020A

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C for DS3120; 0°C to +85°C for DS3120N)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		5.5	V	
Logic 0	V_{IL}	–0.3		+0.8	V	
Supply for the Core	V_{DD_CORE}	1.71		1.89	V	
Supply for the IO Buffers	V_{DD_IO}	2.97		3.63	V	

CAPACITANCE

(t_A =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS

0°C to 70°C; V_{DD_CORE} = 1.71 to 1.89V &
V_{DD_IO} = 2.97 to 3.63V for DS3120 /
-40°C to +85°C; V_{DD_CORE} = 1.71 to 1.89V &
V_{DD_IO} = 2.97 to 3.63V for DS3120N

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current for VDD_CORE = 1.8V	I_{DDCORE}		50		mA	1
Supply Current for VDD_IO = 3.3V	I_{DDIO}		300		mA	1
Input Leakage	I_{IL}	–1.0		+1.0	µA	2
Output Leakage	I_{LO}			1.0	µA	3
Output Current (2.4V)	I_{OH}	–1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. CTCLK = CLKSI = RCLK = 1.544 MHz operating in Mode 1; inputs tied low, outputs open circuited.
2. 0.0V < VIN < V_{DD_IO}.
3. Applies to INT* / RSER / RSIG when 3–stated.

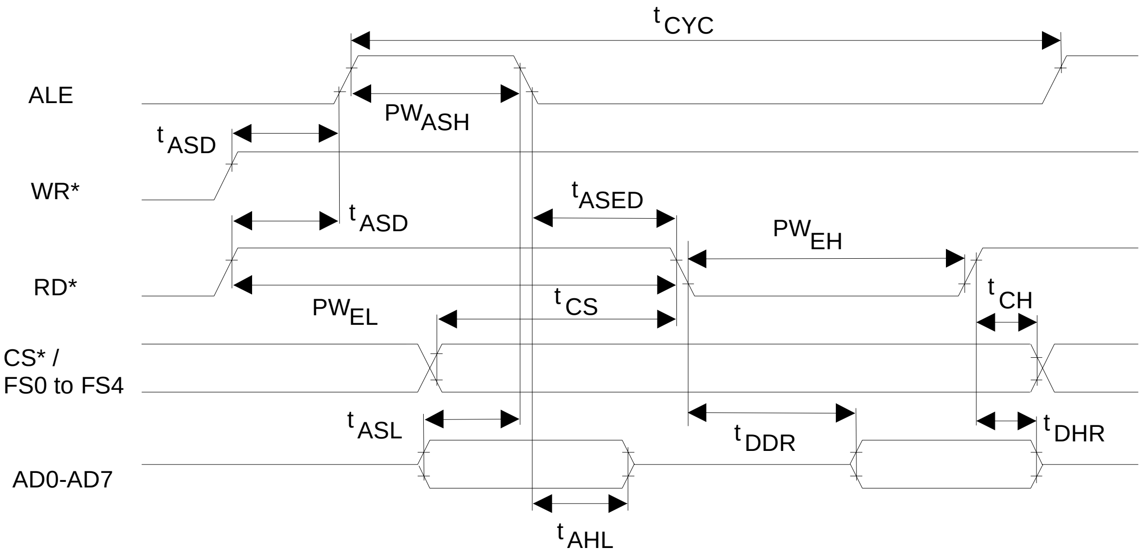
AC CHARACTERISTICS – MULTIPLEXED PARALLEL PORT (MUX = 1)

0°C to 70°C; V_{DD_CORE} = 1.71 to 1.89V & V_{DD_IO} = 2.97 to 3.63V for DS3120 /
-40°C to +85°C; V_{DD_CORE} = 1.71 to 1.89V & V_{DD_IO} = 2.97 to 3.63V for DS3120N

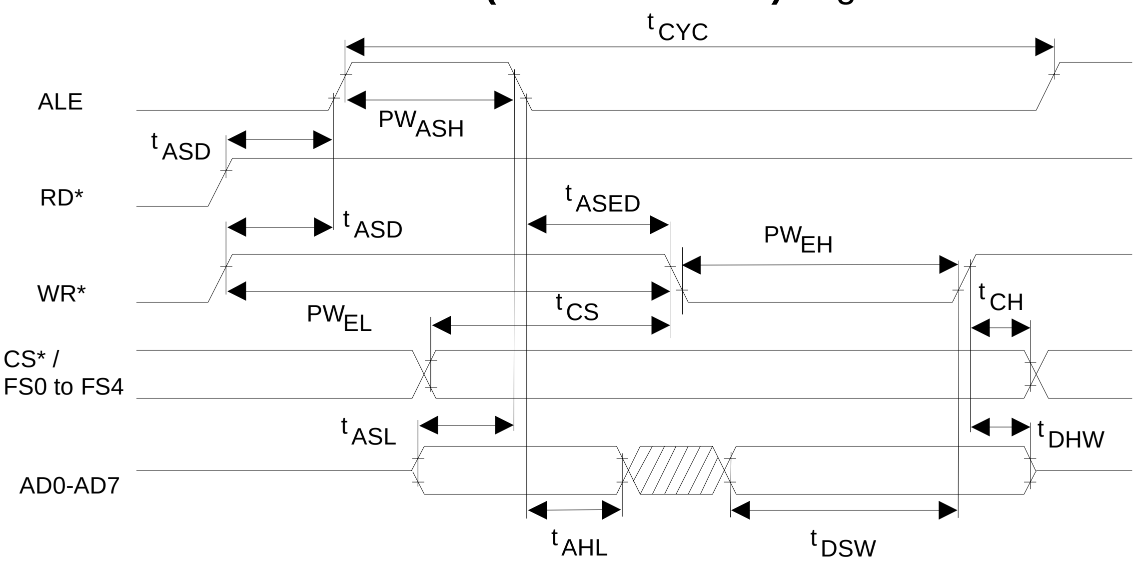
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	200			ns	
Pulse Width, DS low or RD* high	PW_{EL}	100			ns	
Pulse Width, DS high or RD* low	PW_{EH}	100			ns	
Input Rise/Fall times	t_R , t_F		20		ns	
R/W* Hold Time	t_{RWH}	10			ns	
R/W* Set Up time before DS high	t_{RWS}	50			ns	
CS*, FS0 to FS4 Set Up time before DS, WR* or RD* active	t_{CS}	20			ns	
CS*, FS0 to FS4 Hold time	t_{CH}	0			ns	
Read Data Hold time	t_{DHR}	10	50		ns	
Write Data Hold time	t_{DHW}	0			ns	
Muxed Address valid to AS or ALE fall	t_{ASL}	15			ns	
Muxed Address Hold time	t_{AHL}	10			ns	
Delay time DS, WR* or RD* to AS or ALE rise	t_{ASD}	20			ns	
Pulse Width AS or ALE high	PW_{ASH}	30			ns	
Delay time, AS or ALE to DS, WR* or RD*	t_{ASED}	10			ns	
Output Data Delay time from DS or RD*	t_{DDR}	20		80	ns	
Data Set Up time	t_{DSW}	50			ns	

(see Figures 21-1 to 21-3 for details)

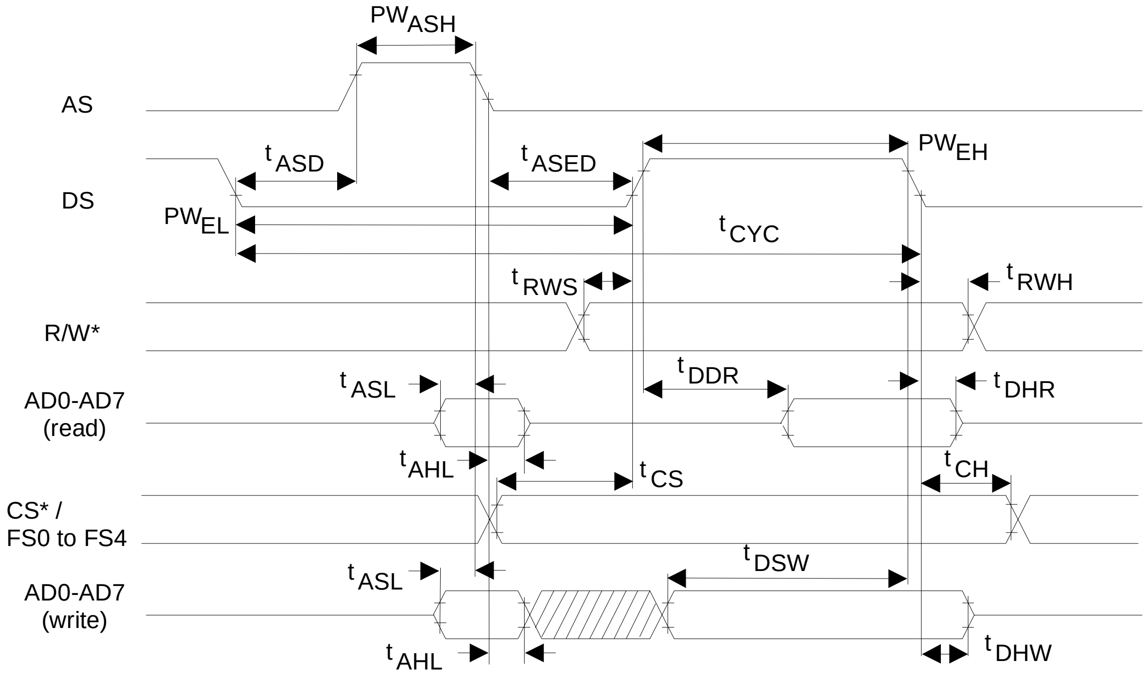
INTEL BUS READ AC TIMING (BTS=0 / MUX = 1) Figure 21-1



INTEL BUS WRITE TIMING (BTS=0 / MUX=1) Figure 21-2



MOTOROLA BUS AC TIMING (BTS = 1 / MUX = 1) Figure 21-3



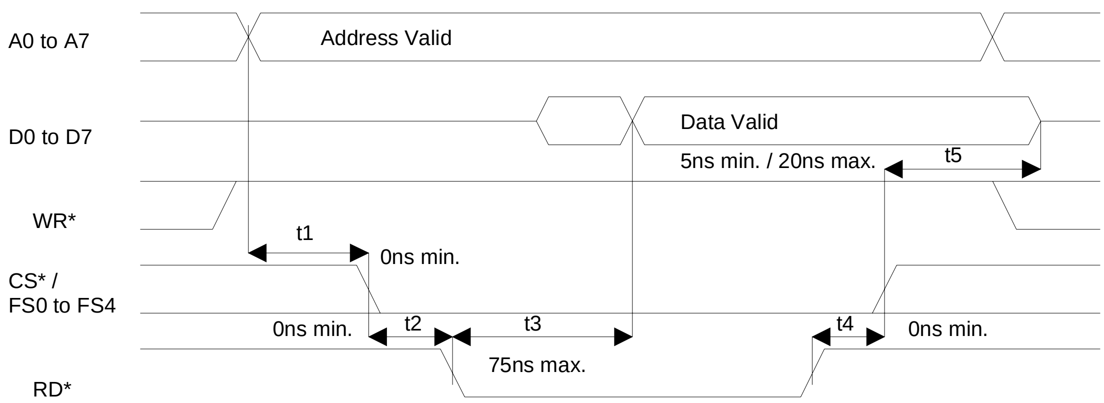
AC CHARACTERISTICS – NON-MULTIPLEXED PARALLEL PORT (MUX = 0)

0°C to 70°C; V_{DD_CORE} = 1.71 to 1.89V &
V_{DD_IO} = 2.97 to 3.63V for DS3120 /
-40°C to +85°C; V_{DD_CORE} = 1.71 to 1.89V &
V_{DD_IO} = 2.97 to 3.63V for DS3120N

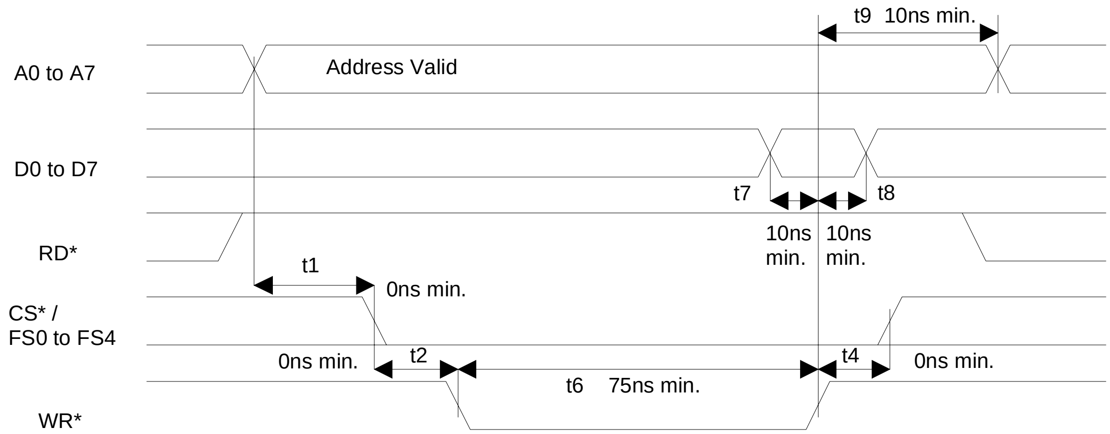
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Set Up Time for A0 to A7, FS0 to FS4 Valid to CS* Active	t_1	0			ns	
Set Up Time for CS* Active to either RD*, WR*, or DS* Active	t_2	0			ns	
Delay Time from either RD* or DS* Active to Data Valid	t_3			75	ns	
Hold Time from either RD*, WR*, or DS* Inactive to CS* Inactive	t_4	0			ns	
Hold Time from CS* Inactive to Data Bus 3–state	t_5	5		20	ns	
Wait Time from either WR* or DS* Active to Latch Data	t_6	75			ns	
Data Set Up Time to either WR* or DS* Inactive	t_7	10			ns	
Data Hold Time from either WR* or DS* Inactive	t_8	10			ns	
Address Hold from either WR* or DS* inactive	t_9	10			ns	

See Figures 21–4 to 21–7 for details.

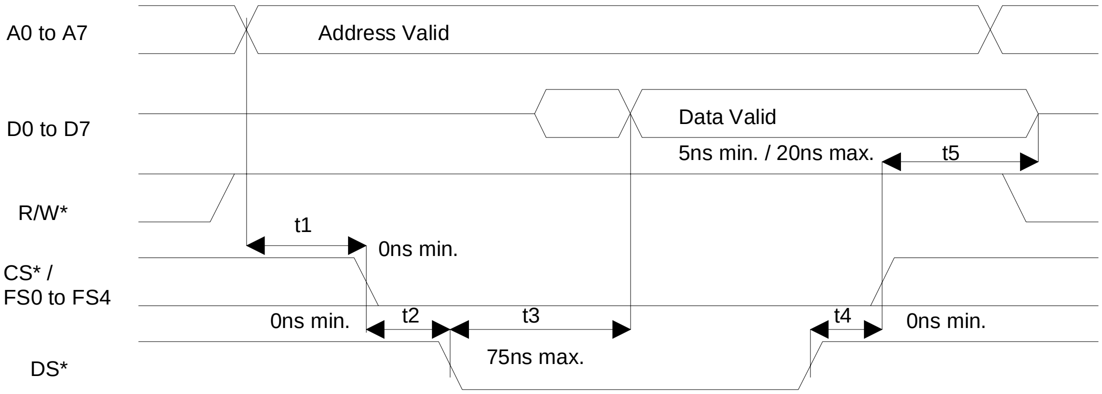
INTEL BUS READ AC TIMING (BTS=0 / MUX=0) Figure 21-4



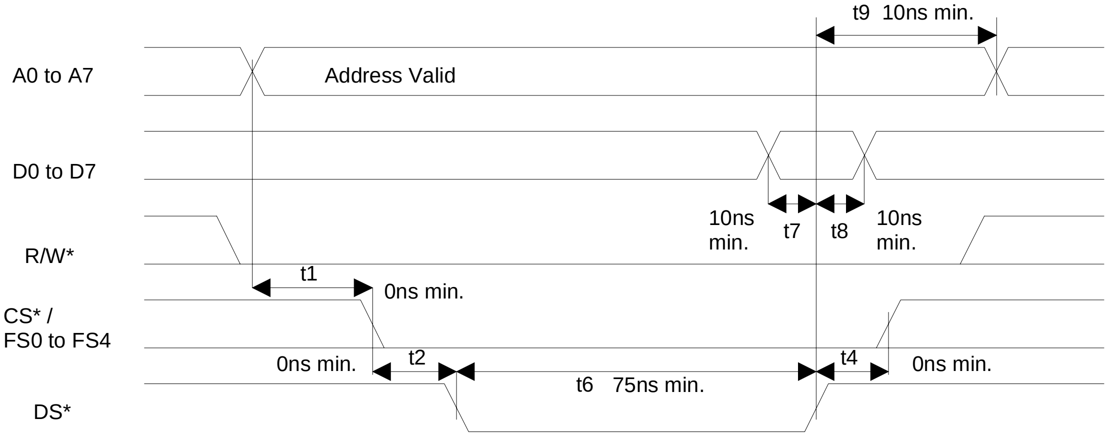
INTEL BUS WRITE AC TIMING (BTS=0 / MUX=0) Figure 21-5



MOTOROLA BUS READ AC TIMING (BTS=1 / MUX=0) Figure 21-6



MOTOROLA BUS WRITE AC TIMING (BTS=1 / MUX=0) Figure 21-7



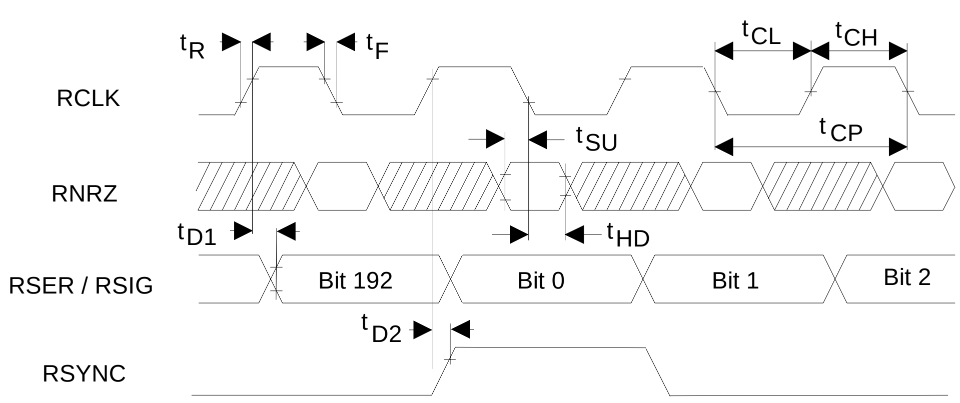
AC CHARACTERISTICS – RECEIVE SIDE

0°C to 70°C; V_{DD_CORE} = 1.71 to 1.89V &
V_{DD_IO} = 2.97 to 3.63V for DS3120 /
-40°C to +85°C; V_{DD_CORE} = 1.71 to 1.89V &
V_{DD_IO} = 2.97 to 3.63V for DS3120N

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{CP}		648		ns	
RCLK Pulse Width	t_{CH} t_{CL}	75 75			ns ns	
RNRZ Set Up to RCLK Falling	t_{SU}	20			ns	
RNRZ Hold From RCLK Falling	t_{HD}	20			ns	
RCLK Rise and Fall Times	t_R , t_F			25	ns	
Delay RCLK to RSER or RSIG Valid	t_{D1}			50	ns	
Delay RCLK to RSYNC	t_{D2}			50	ns	

See Figure 21-8 for details.

RECEIVE SIDE AC TIMING Figure 21-8



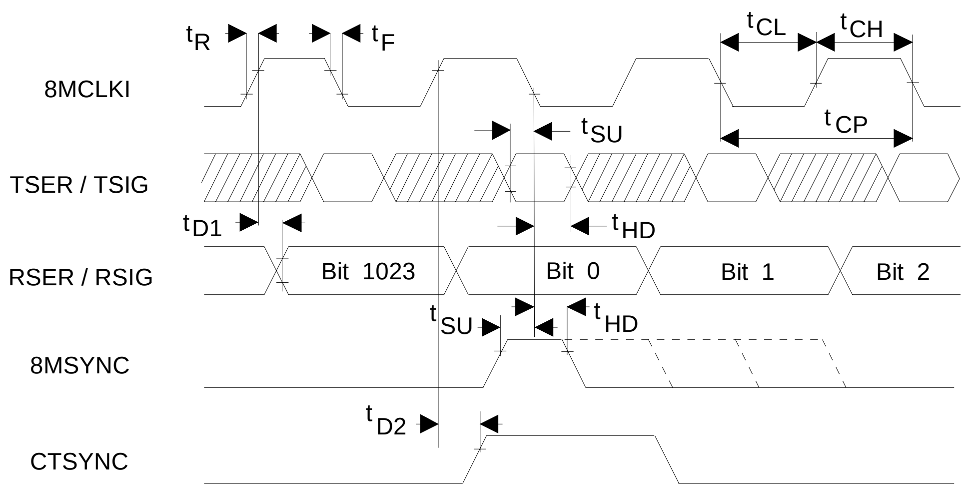
AC CHARACTERISTICS – 8 MHZ INTERLEAVED BUS OPERATION (IBO)

0°C to 70°C; V_{DD_CORE} = 1.71 to 1.89V & V_{DD_IO} = 2.97 to 3.63V for DS3120 /
-40°C to +85°C; V_{DD_CORE} = 1.71 to 1.89V & V_{DD_IO} = 2.97 to 3.63V for DS3120N

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
8MCLKI Period	t_{CP}		122		ns	
RCLK Pulse Width	t_{CH} t_{CL}	50 50			ns ns	
8MSYNC Set Up to 8MCLKI Falling	t_{SU}	20		t_{CH}–5	ns	
8MSYNC Hold from 8MCLKI Falling	t_{HD}	20		infinite	ns	
TSER / TSIG Set Up to RCLK Falling	t_{SU}	20			ns	
TSER / TSIG Hold From RCLK Falling	t_{HD}	20			ns	
8MCLKI Rise and Fall Times	t_R , t_F			10	ns	
Delay 8MCLKI to RSER or RSIG Valid	t_{D1}			50	ns	
Delay 8MCLKI to CTSYNC	t_{D2}			50	ns	

See Figure 21-9 for details.

8 MHZ IBO AC TIMING Figure 21-9



AC CHARACTERISTICS – TRANSMIT SIDE

0°C to 70°C; V_{DD_CORE} = 1.71 to 1.89V &
V_{DD_IO} = 2.97 to 3.63V for DS3120 /
-40°C to +85°C; V_{DD_CORE} = 1.71 to 1.89V &
V_{DD_IO} = 2.97 to 3.63V for DS3120N

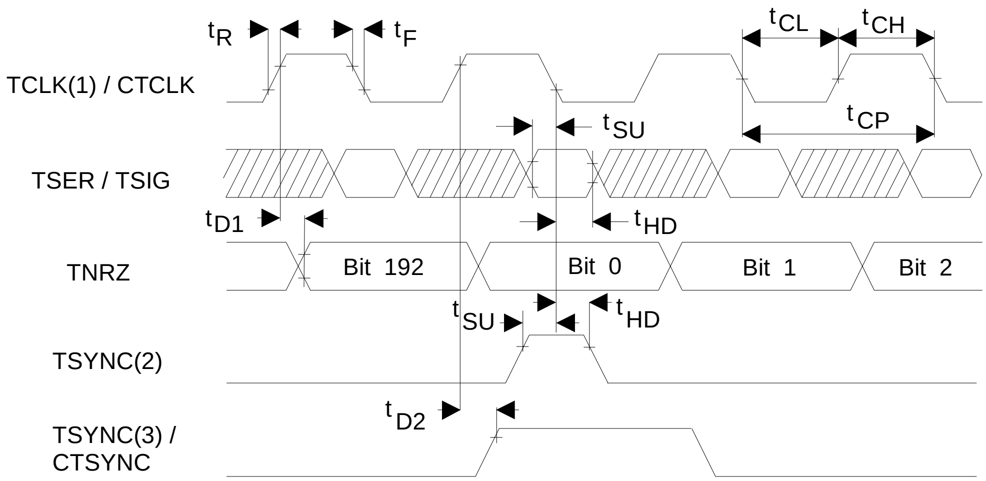
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_{CP}		648		ns	1
TCLK Pulse Width	t_{CH} t_{CL}	75 75			ns ns	1
TSYNC Set Up to TCLK Falling	t_{SU}	20		t_{CH} –5	ns	1, 2
TSYNC Hold from TCLK Falling	t_{HD}	20		infinite	ns	1, 2
TSER / TSIG Set Up to TCLK or CTCLK Falling	t_{SU}	20			ns	
TSER / TSIG Hold from TCLK or CTCLK Falling	t_{HD}	20			ns	
TCLK Rise and Fall Times	t_R , t_F			25	ns	1
Delay TCLK/CTCLK to TNRZ Valid	t_{D1}			50	ns	
Delay TCLK/CTCLK to TSYNC or CTSYNC	t_{D2}			50	ns	3

See Figure 21–10 for details.

NOTES:

1. TCLK is an input (Modes 11, 12, or 13).
2. TSYNC is an input (Mode 11 only).
3. TSYNC is an output (Modes 1 to 4 or 12 or 13).

TRANSMIT SIDE AC TIMING Figure 21-10



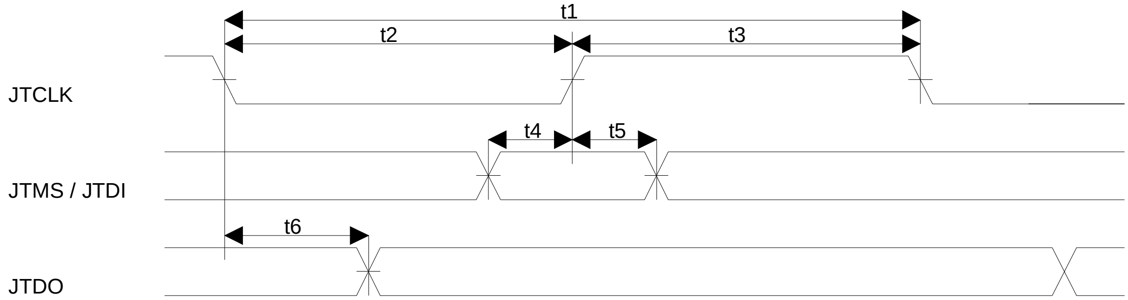
AC CHARACTERISTICS – JTAG TEST PORT INTERFACE

0°C to 70°C; V_{DD_CORE} = 1.71 to 1.89V &
V_{DD_IO} = 2.97 to 3.63V for DS3120 /
-40°C to +85°C; V_{DD_CORE} = 1.71 to 1.89V &
V_{DD_IO} = 2.97 to 3.63V for DS3120N

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
JTCLK Period	t_1	1000			ns	
JTCLK Clock Low Time	t_2	400			ns	
JTCLK Clock High Time	t_3	400			ns	
JTMS / JTDI Set Up Time to JTCLK Rising	t_4	50			ns	
JTMS / JTDI Hold Time from JTCLK Rising	t_5	50			ns	
Delay Time from JTCLK Falling to JTDO Valid	t_6	2		50	ns	

See Figure 21–11 for details.

JTAG TEST PORT AC TIMING Figure 21-11



22. MECHANICAL PACKAGE SPECIFICATIONS