FEATURES

- Sixteen (16) or Twelve (12) Completely Independent T1 or E1 Framers in One Small 27mm x 27mm Package
- Each Multi-Chip Module (MCM) Contains Either Four (FF) or Three (FT) Die of:
  DS21Q42 (DS21FF42 & DS21FT42)
  DS21Q44 (DS21FF44 & DS21FT44)
- Selection Guide:

	# Framers	Device
T1	16 (4 Quads)	DS21FF42
T1	12 (3 Quads)	DS21FT42
E1	16 (4 Quads)	DS21FF44
E1	12 (3 Quads)	DS21FT44

- See the Specific DS21Q42 and DS21Q44 Data Sheets for Details on their Feature Set and Operation
- Each Quad Framer Can be Concatenated into a Single 8.192MHz Backplane Data Stream
- IEEE 1149.1 JTAG-Boundary Scan Architecture
- DS21FF42 and DS21FF44 are Pin Compatible to Allow the Same Footprint to Support T1 and E1 Applications
- 300–pin MCM BGA package (27mm X 27mm)
- Low Power 3.3V CMOS with 5V Tolerant Input & Outputs

DESCRIPTION

The Four x Four and Four x Three MCMs offer a high density packaging arrangement for the DS21Q42 T1 Enhanced Quad Framer and the DS21Q44 E1 Enhanced Quad Framer. Either three (DS21FT42 and DS21FT44) or four (DS21FF42 and DS21FF44) silicon die of these devices is packaged in a Multi-Chip Module (MCM) with the electrical connections as shown in Figure 1.

All of the functions available on the DS21Q42 and DS21Q44 are also available in the MCM packaged version however in order to minimize package size, some signals have been deleted or combined. These differences are detailed in Table 1. In the Four x Three (FT) version, the fourth quad framer is not populated and hence all of the signals to and from this fourth framer are absent and should be treated as No Connects (NC). Table 2 lists all of the signals on the MCM and it also lists the absent signals for the Four x Three.

The availability of both a twelve and a sixteen channel version allow the maximum framer density with the lowest cost. For example, in a T3 application, two devices (one DS21FF42 and one DS21FT42) provide a total of 28 framers without the additional cost and power consumption of any unused framers that appear in an octal approach.

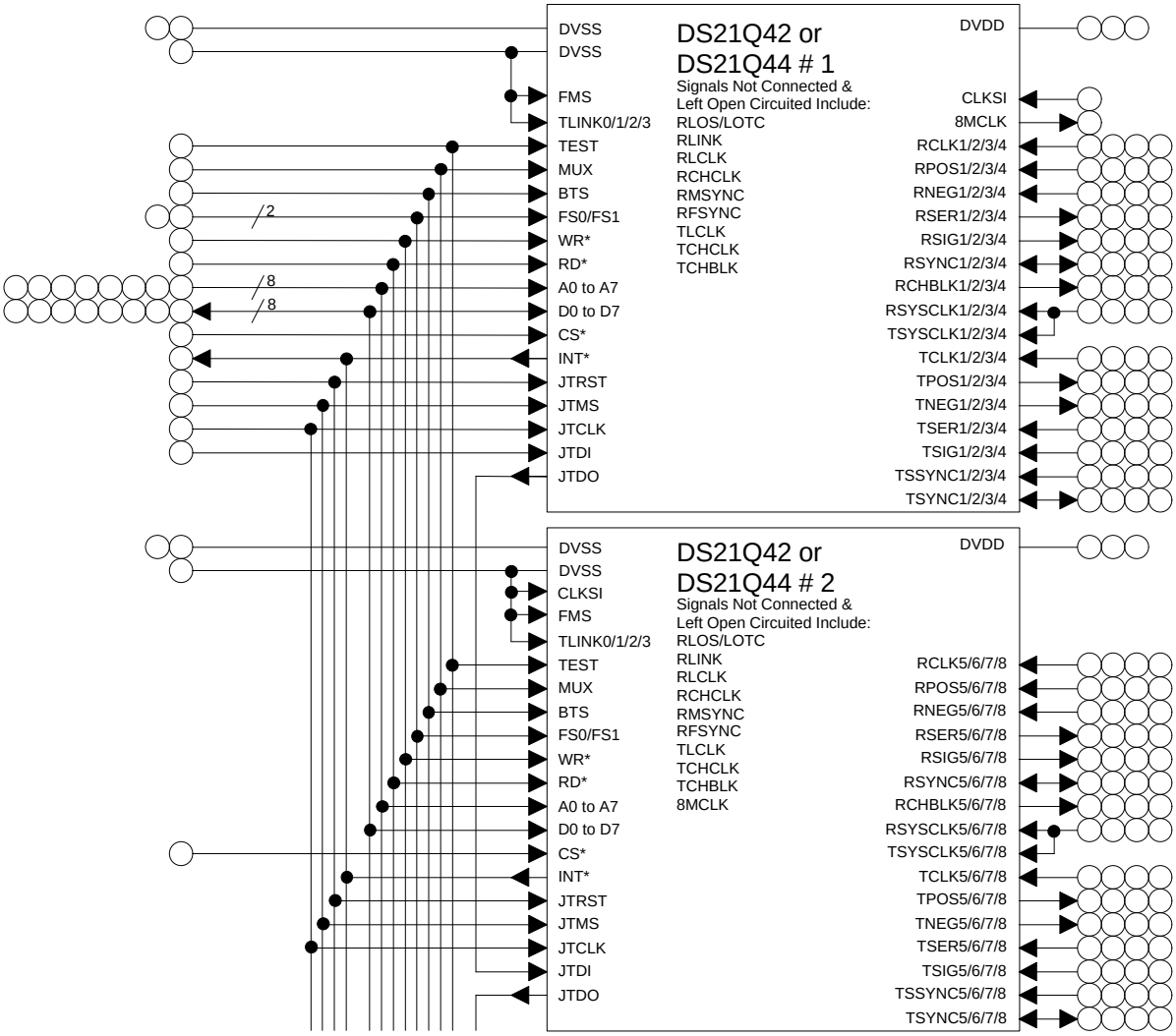
Changes Made From the August 7, 1998 Version of the Data Sheet:

Two new signals (TEST & MUX) were added at the previous No Connect (NC) leads.

Changes from Normal DS21Q42 and DS21Q44 Configuration Table 1

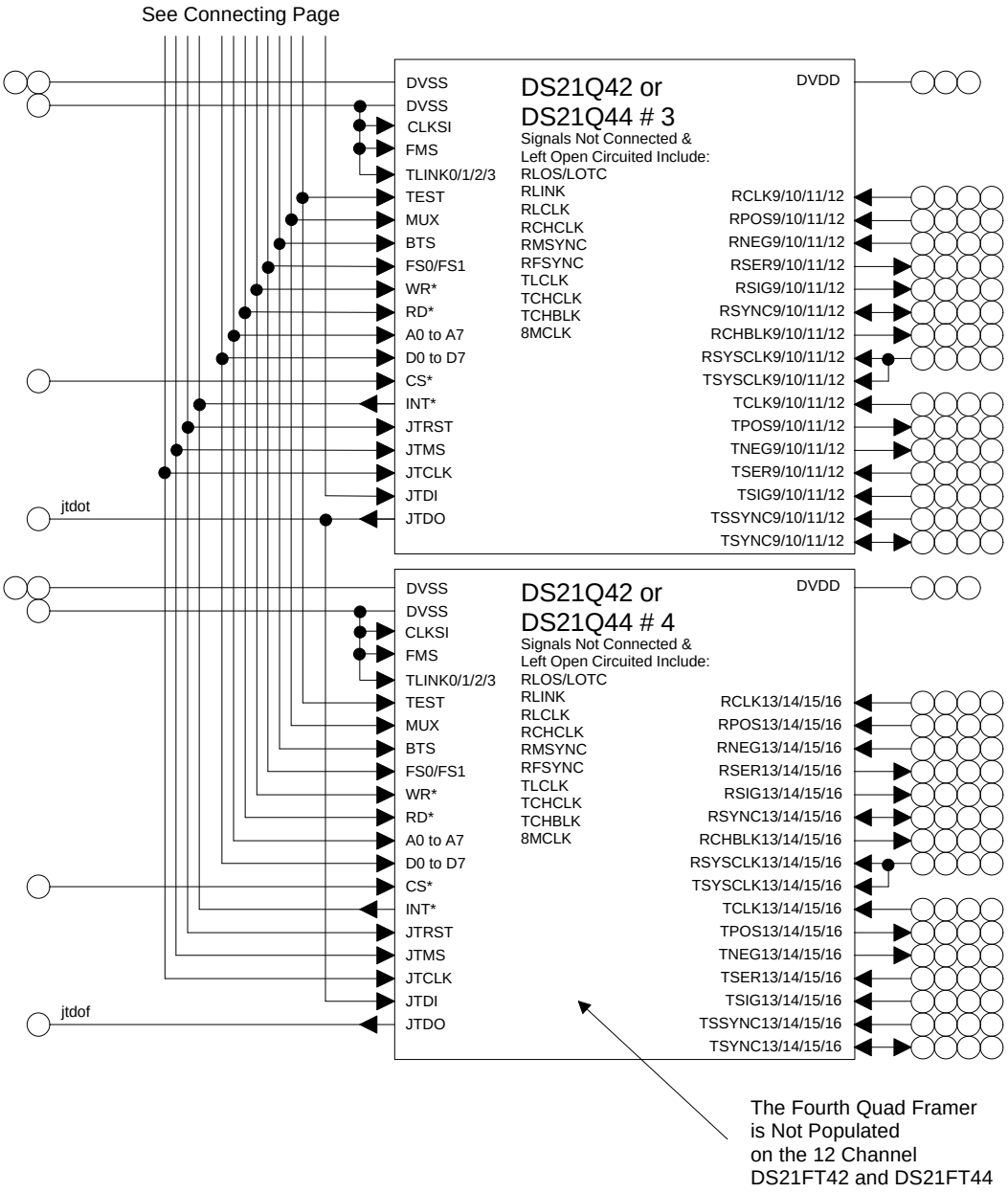
1. TSYSCLK and RSYSCLK are tied together.
2. The following signals are not available:
   RFSYNC / RLCLK / RLINK / RCHCLK / RMSYNC / RLOS/LOTC / TCHBLK / TLCLK / TLINK / TCHCLK

DS21FF42 / DS21FT42 / DS21FT44 / DS21FF44 Schematic Figure 1



See Connecting Page

DS21FF42 / DS21FT42 / DS21FF44 / DS21FT44 Schematic Figure 1 (continued)



Lead Description Sorted by Symbol Table 2

Lead	Symbol	I/O	Description
B7	8MCLK	O	8.192 MHz Clock Based on CLKSI.
G20	A0	I	Address Bus Bit 0 (lsb).
H20	A1	I	Address Bus Bit 1.
G19	A2	I	Address Bus Bit 2.
H19	A3	I	Address Bus Bit 3.
G18	A4	I	Address Bus Bit 4.
H18	A5	I	Address Bus Bit 5.
G17	A6	I	Address Bus Bit 6.
H17	A7	I	Address Bus Bit 7 (msb).
W15	BTS	I	Bus Timing Select. 0 = Intel / 1 = Motorola.
B6	CLKSI	I	Reference clock for the 8.192MHz clock synthesizer.
T8	CS1*	I	Chip Select for Quad Framer 1.
Y4	CS2*	I	Chip Select for Quad Framer 2.
Y15	CS3*	I	Chip Select for Quad Framer 3.
E19	CS4*/NC	I	Chip Select for Quad Framer 4. NC on Four x Three.
L20	D0	I/O	Data Bus Bit 0 (lsb).
M20	D1	I/O	Data Bus Bit 1.
L19	D2	I/O	Data Bus Bit 2.
M19	D3	I/O	Data Bus Bit 3.
L18	D4	I/O	Data Bus Bit 4.
M18	D5	I/O	Data Bus Bit 5.
L17	D6	I/O	Data Bus Bit 6.
M17	D7	I/O	Data Bus Bit 7 (msb).
C7	DVDD1	–	Digital Positive Supply for Framer 1.
E4	DVDD1	–	Digital Positive Supply for Framer 1.
D2	DVDD1	–	Digital Positive Supply for Framer 1.
K3	DVDD2	–	Digital Positive Supply for Framer 2.
U7	DVDD2	–	Digital Positive Supply for Framer 2.
P2	DVDD2	–	Digital Positive Supply for Framer 2.
V19	DVDD3	–	Digital Positive Supply for Framer 3.
T12	DVDD3	–	Digital Positive Supply for Framer 3.
L16	DVDD3	–	Digital Positive Supply for Framer 3.
D17	DVDD4/NC	–	Digital Positive Supply for Framer 4. NC on Four x Three.
F16	DVDD4/NC	–	Digital Positive Supply for Framer 4. NC on Four x Three.
B11	DVDD4/NC	–	Digital Positive Supply for Framer 4. NC on Four x Three.
E9	DVSS1	–	Digital Signal Ground for Framer 1.
A6	DVSS1	–	Digital Signal Ground for Framer 1.
D5	DVSS1	–	Digital Signal Ground for Framer 1.
U3	DVSS2	–	Digital Signal Ground for Framer 2.
K4	DVSS2	–	Digital Signal Ground for Framer 2.
U8	DVSS2	–	Digital Signal Ground for Framer 2.
U4	DVSS3	–	Digital Signal Ground for Framer 3.
R16	DVSS3	–	Digital Signal Ground for Framer 3.
Y20	DVSS3	–	Digital Signal Ground for Framer 3.
J20	DVSS4/NC	–	Digital Signal Ground for Framer 4. NC on Four x Three.
A11	DVSS4/NC	–	Digital Signal Ground for Framer 4. NC on Four x Three.
D19	DVSS4/NC	–	Digital Signal Ground for Framer 4. NC on Four x Three.
Y14	FS0	I	Framer Select 0 for the Parallel Control Port.
W14	FS1	I	Framer Select 1 for the Parallel Control Port.
G16	INT*	O	Interrupt for all four Quad Framers.
V14	JTCLK	I	JTAG Clock.
E10	JTDI	I	JTAG Data Input.
A19	JTDOF/NC	O	JTAG Data Output for Four x Four Version. NC on Four x Three.
T17	JTDOT	O	JTAG Data Output for Four x Three Version.

H16	JTMS	I	JTAG Test Mode Select.
K17	JTRST*	I	JTAG Reset.
A13	TEST	I	Tri-State. 0 = do not tri-state / 1 = tri-state all outputs & I/O signals
P17	MUX	I	Bus Operation Select. 0 = non-multiplexed bus / 1 = multiplexed bus
C2	RCHBLK1	O	Receive Channel Blocking Clock.
G3	RCHBLK2	O	Receive Channel Blocking Clock.
E6	RCHBLK3	O	Receive Channel Blocking Clock.
A8	RCHBLK4	O	Receive Channel Blocking Clock.
N1	RCHBLK5	O	Receive Channel Blocking Clock.
Y1	RCHBLK6	O	Receive Channel Blocking Clock.
U6	RCHBLK7	O	Receive Channel Blocking Clock.
N5	RCHBLK8	O	Receive Channel Blocking Clock.
Y8	RCHBLK9	O	Receive Channel Blocking Clock.
W12	RCHBLK10	O	Receive Channel Blocking Clock.
V17	RCHBLK11	O	Receive Channel Blocking Clock.
U17	RCHBLK12	O	Receive Channel Blocking Clock.
D16	RCHBLK13/NC	O	Receive Channel Blocking Clock. NC on Four x Three.
K20	RCHBLK14/NC	O	Receive Channel Blocking Clock. NC on Four x Three.
B18	RCHBLK15/NC	O	Receive Channel Blocking Clock. NC on Four x Three.
B16	RCHBLK16/NC	O	Receive Channel Blocking Clock. NC on Four x Three.
A2	RCLK1	I	Receive Clock for Framer 1
K1	RCLK2	I	Receive Clock for Framer 2.
D10	RCLK3	I	Receive Clock for Framer 3.
B9	RCLK4	I	Receive Clock for Framer 4.
M3	RCLK5	I	Receive Clock for Framer 5.
V1	RCLK6	I	Receive Clock for Framer 6.
W6	RCLK7	I	Receive Clock for Framer 7.
J3	RCLK8	I	Receive Clock for Framer 8.
T9	RCLK9	I	Receive Clock for Framer 9.
W10	RCLK10	I	Receive Clock for Framer 10.
Y18	RCLK11	I	Receive Clock for Framer 11.
N17	RCLK12	I	Receive Clock for Framer 12.
D14	RCLK13/NC	I	Receive Clock for Framer 13. NC on Four x Three.
P20	RCLK14/NC	I	Receive Clock for Framer 14. NC on Four x Three.
C18	RCLK15/NC	I	Receive Clock for Framer 15. NC on Four x Three.
C12	RCLK16/NC	I	Receive Clock for Framer 16. NC on Four x Three.
E18	RD*	I	Read Input.
B2	RNEG1	I	Receive Negative Data for Framer 1.
H2	RNEG2	I	Receive Negative Data for Framer 2.
D9	RNEG3	I	Receive Negative Data for Framer 3.
A9	RNEG4	I	Receive Negative Data for Framer 4.
M2	RNEG5	I	Receive Negative Data for Framer 5.
V3	RNEG6	I	Receive Negative Data for Framer 6.
V7	RNEG7	I	Receive Negative Data for Framer 7.
P3	RNEG8	I	Receive Negative Data for Framer 8.
U9	RNEG9	I	Receive Negative Data for Framer 9.
W11	RNEG10	I	Receive Negative Data for Framer 10.
W17	RNEG11	I	Receive Negative Data for Framer 11.
T20	RNEG12	I	Receive Negative Data for Framer 12.
E14	RNEG13/NC	I	Receive Negative Data for Framer 13. NC on Four x Three.
N20	RNEG14/NC	I	Receive Negative Data for Framer 14. NC on Four x Three.
C20	RNEG15/NC	I	Receive Negative Data for Framer 15. NC on Four x Three.
B13	RNEG16/NC	I	Receive Negative Data for Framer 16. NC on Four x Three.
A1	RPOS1	I	Receive Positive Data for Framer 1.
H1	RPOS2	I	Receive Positive Data for Framer 2.
H4	RPOS3	I	Receive Positive Data for Framer 3.
C9	RPOS4	I	Receive Positive Data for Framer 4.

M1	RPOS5	I	Receive Positive Data for Framer 5.
W2	RPOS6	I	Receive Positive Data for Framer 6.
V5	RPOS7	I	Receive Positive Data for Framer 7.
P4	RPOS8	I	Receive Positive Data for Framer 8.
T10	RPOS9	I	Receive Positive Data for Framer 9.
V11	RPOS10	I	Receive Positive Data for Framer 10.
Y19	RPOS11	I	Receive Positive Data for Framer 11.
R19	RPOS12	I	Receive Positive Data for Framer 12.
D15	RPOS13/NC	I	Receive Positive Data for Framer 13. NC on Four x Three.
J18	RPOS14/NC	I	Receive Positive Data for Framer 14. NC on Four x Three.
A20	RPOS15/NC	I	Receive Positive Data for Framer 15. NC on Four x Three.
A14	RPOS16/NC	I	Receive Positive Data for Framer 16. NC on Four x Three.
C1	RSER1	O	Receive Serial Data from Framer 1.
H3	RSER2	O	Receive Serial Data from Framer 2.
C6	RSER3	O	Receive Serial Data from Framer 3.
C8	RSER4	O	Receive Serial Data from Framer 4.
P1	RSER5	O	Receive Serial Data from Framer 5.
W4	RSER6	O	Receive Serial Data from Framer 6.
T7	RSER7	O	Receive Serial Data from Framer 7.
N4	RSER8	O	Receive Serial Data from Framer 8.
U11	RSER9	O	Receive Serial Data from Framer 9.
Y12	RSER10	O	Receive Serial Data from Framer 10.
V16	RSER11	O	Receive Serial Data from Framer 11.
T16	RSER12	O	Receive Serial Data from Framer 12.
E16	RSER13/NC	O	Receive Serial Data from Framer 13. NC on Four x Three.
F20	RSER14/NC	O	Receive Serial Data from Framer 14. NC on Four x Three.
C16	RSER15/NC	O	Receive Serial Data from Framer 15. NC on Four x Three.
A12	RSER16/NC	O	Receive Serial Data from Framer 16. NC on Four x Three.
D3	RSIG1	O	Receive Signaling Output from Framer 1.
G2	RSIG2	O	Receive Signaling Output from Framer 2.
D4	RSIG3	O	Receive Signaling Output from Framer 3.
D8	RSIG4	O	Receive Signaling Output from Framer 4.
N2	RSIG5	O	Receive Signaling Output from Framer 5.
V4	RSIG6	O	Receive Signaling Output from Framer 6.
V6	RSIG7	O	Receive Signaling Output from Framer 7.
K5	RSIG8	O	Receive Signaling Output from Framer 8.
U10	RSIG9	O	Receive Signaling Output from Framer 9.
Y11	RSIG10	O	Receive Signaling Output from Framer 10.
W19	RSIG11	O	Receive Signaling Output from Framer 11.
U20	RSIG12	O	Receive Signaling Output from Framer 12.
E15	RSIG13/NC	O	Receive Signaling Output from Framer 13. NC on Four x Three.
K19	RSIG14/NC	O	Receive Signaling Output from Framer 14. NC on Four x Three.
C17	RSIG15/NC	O	Receive Signaling Output from Framer 15. NC on Four x Three.
A15	RSIG16/NC	O	Receive Signaling Output from Framer 16. NC on Four x Three.
B1	RSYNC1	I/O	Receive Frame/Multiframe Sync for Framer 1.
G1	RSYNC2	I/O	Receive Frame/Multiframe Sync for Framer 2.
D6	RSYNC3	I/O	Receive Frame/Multiframe Sync for Framer 3.
A7	RSYNC4	I/O	Receive Frame/Multiframe Sync for Framer 4.
N3	RSYNC5	I/O	Receive Frame/Multiframe Sync for Framer 5.
Y2	RSYNC6	I/O	Receive Frame/Multiframe Sync for Framer 6.
U5	RSYNC7	I/O	Receive Frame/Multiframe Sync for Framer 7.
J4	RSYNC8	I/O	Receive Frame/Multiframe Sync for Framer 8.
T11	RSYNC9	I/O	Receive Frame/Multiframe Sync for Framer 9.
V13	RSYNC10	I/O	Receive Frame/Multiframe Sync for Framer 10.
V15	RSYNC11	I/O	Receive Frame/Multiframe Sync for Framer 11.
P18	RSYNC12	I/O	Receive Frame/Multiframe Sync for Framer 12.
J17	RSYNC13/NC	I/O	Receive Frame/Multiframe Sync for Framer 13. NC on Four x Three.

J19	RSYNC14/NC	I/O	Receive Frame/Multiframe Sync for Framer 14. NC on Four x Three.
B17	RSYNC15/NC	I/O	Receive Frame/Multiframe Sync for Framer 15. NC on Four x Three.
B12	RSYNC16/NC	I/O	Receive Frame/Multiframe Sync for Framer 16. NC on Four x Three.
B5	SYSCLK1	I	System Clock for Framer 1.
E2	SYSCLK2	I	System Clock for Framer 2.
E5	SYSCLK3	I	System Clock for Framer 3.
B8	SYSCLK4	I	System Clock for Framer 4.
M4	SYSCLK5	I	System Clock for Framer 5.
T2	SYSCLK6	I	System Clock for Framer 6.
Y5	SYSCLK7	I	System Clock for Framer 7.
W3	SYSCLK8	I	System Clock for Framer 8.
T4	SYSCLK9	I	System Clock for Framer 9.
Y9	SYSCLK10	I	System Clock for Framer 10.
U12	SYSCLK11	I	System Clock for Framer 11.
R17	SYSCLK12	I	System Clock for Framer 12.
E13	SYSCLK13/NC	I	System Clock for Framer 13. NC on Four x Three.
N18	SYSCLK14/NC	I	System Clock for Framer 14. NC on Four x Three.
E20	SYSCLK15/NC	I	System Clock for Framer 15. NC on Four x Three.
C14	SYSCLK16/NC	I	System Clock for Framer 16. NC on Four x Three.
D1	TCLK1	I	Transmit Clock for Framer 1.
H5	TCLK2	I	Transmit Clock for Framer 2.
C5	TCLK3	I	Transmit Clock for Framer 3.
A5	TCLK4	I	Transmit Clock for Framer 4.
R1	TCLK5	I	Transmit Clock for Framer 5.
Y3	TCLK6	I	Transmit Clock for Framer 6.
T6	TCLK7	I	Transmit Clock for Framer 7.
K2	TCLK8	I	Transmit Clock for Framer 8.
U13	TCLK9	I	Transmit Clock for Framer 9.
Y13	TCLK10	I	Transmit Clock for Framer 10.
T18	TCLK11	I	Transmit Clock for Framer 11.
P16	TCLK12	I	Transmit Clock for Framer 12.
K16	TCLK13/NC	I	Transmit Clock for Framer 13. NC on Four x Three.
F19	TCLK14/NC	I	Transmit Clock for Framer 14. NC on Four x Three.
E17	TCLK15/NC	I	Transmit Clock for Framer 15. NC on Four x Three.
C11	TCLK16/NC	I	Transmit Clock for Framer 16. NC on Four x Three.
C3	TNEG1	O	Transmit Negative Data from Framer 1.
J1	TNEG2	O	Transmit Negative Data from Framer 2.
F5	TNEG3	O	Transmit Negative Data from Framer 3.
A10	TNEG4	O	Transmit Negative Data from Framer 4.
L1	TNEG5	O	Transmit Negative Data from Framer 5.
V2	TNEG6	O	Transmit Negative Data from Framer 6.
V8	TNEG7	O	Transmit Negative Data from Framer 7.
P5	TNEG8	O	Transmit Negative Data from Framer 8.
U14	TNEG9	O	Transmit Negative Data from Framer 9.
V12	TNEG10	O	Transmit Negative Data from Framer 10.
W18	TNEG11	O	Transmit Negative Data from Framer 11.
T19	TNEG12	O	Transmit Negative Data from Framer 12.
D11	TNEG13/NC	O	Transmit Negative Data from Framer 13. NC on Four x Three.
K18	TNEG14/NC	O	Transmit Negative Data from Framer 14. NC on Four x Three.
C19	TNEG15/NC	O	Transmit Negative Data from Framer 15. NC on Four x Three.
B15	TNEG16/NC	O	Transmit Negative Data from Framer 16. NC on Four x Three.
B3	TPOS1	O	Transmit Positive Data from Framer 1.
J2	TPOS2	O	Transmit Positive Data from Framer 2.
J5	TPOS3	O	Transmit Positive Data from Framer 3.
B10	TPOS4	O	Transmit Positive Data from Framer 4.
L2	TPOS5	O	Transmit Positive Data from Framer 5.
W1	TPOS6	O	Transmit Positive Data from Framer 6.

W7	TPOS7	O	Transmit Positive Data from Framer 7.
R3	TPOS8	O	Transmit Positive Data from Framer 8.
T14	TPOS9	O	Transmit Positive Data from Framer 9.
Y10	TPOS10	O	Transmit Positive Data from Framer 10.
V18	TPOS11	O	Transmit Positive Data from Framer 11.
V20	TPOS12	O	Transmit Positive Data from Framer 12.
E12	TPOS13/NC	O	Transmit Positive Data from Framer 13. NC on Four x Three.
N19	TPOS14/NC	O	Transmit Positive Data from Framer 14. NC on Four x Three.
B19	TPOS15/NC	O	Transmit Positive Data from Framer 15. NC on Four x Three.
B14	TPOS16/NC	O	Transmit Positive Data from Framer 16. NC on Four x Three.
B4	TSER1	I	Transmit Serial Data for Framer 1.
E1	TSER2	I	Transmit Serial Data for Framer 2.
F3	TSER3	I	Transmit Serial Data for Framer 3.
D7	TSER4	I	Transmit Serial Data for Framer 4.
L5	TSER5	I	Transmit Serial Data for Framer 5.
T1	TSER6	I	Transmit Serial Data for Framer 6.
Y6	TSER7	I	Transmit Serial Data for Framer 7.
T3	TSER8	I	Transmit Serial Data for Framer 8.
M16	TSER9	I	Transmit Serial Data for Framer 9.
W9	TSER10	I	Transmit Serial Data for Framer 10.
W16	TSER11	I	Transmit Serial Data for Framer 11.
W20	TSER12	I	Transmit Serial Data for Framer 12.
D13	TSER13/NC	I	Transmit Serial Data for Framer 13. NC on Four x Three.
F17	TSER14/NC	I	Transmit Serial Data for Framer 14. NC on Four x Three.
D18	TSER15/NC	I	Transmit Serial Data for Framer 15. NC on Four x Three.
A18	TSER16/NC	I	Transmit Serial Data for Framer 16. NC on Four x Three.
C4	TSIG1	I	Transmit Signaling Input for Framer 1.
F1	TSIG2	I	Transmit Signaling Input for Framer 2.
G4	TSIG3	I	Transmit Signaling Input for Framer 3.
C10	TSIG4	I	Transmit Signaling Input for Framer 4.
L3	TSIG5	I	Transmit Signaling Input for Framer 5.
U2	TSIG6	I	Transmit Signaling Input for Framer 6.
V9	TSIG7	I	Transmit Signaling Input for Framer 7.
R5	TSIG8	I	Transmit Signaling Input for Framer 8.
U15	TSIG9	I	Transmit Signaling Input for Framer 9.
V10	TSIG10	I	Transmit Signaling Input for Framer 10.
U18	TSIG11	I	Transmit Signaling Input for Framer 11.
R18	TSIG12	I	Transmit Signaling Input for Framer 12.
E11	TSIG13/NC	I	Transmit Signaling Input for Framer 13. NC on Four x Three.
P19	TSIG14/NC	I	Transmit Signaling Input for Framer 14. NC on Four x Three.
B20	TSIG15/NC	I	Transmit Signaling Input for Framer 15. NC on Four x Three.
A16	TSIG16/NC	I	Transmit Signaling Input for Framer 16. NC on Four x Three.
A3	TSSYNC1	I	Transmit System Sync for Framer 1.
F2	TSSYNC2	I	Transmit System Sync for Framer 2.
G5	TSSYNC3	I	Transmit System Sync for Framer 3.
E8	TSSYNC4	I	Transmit System Sync for Framer 4.
L4	TSSYNC5	I	Transmit System Sync for Framer 5.
U1	TSSYNC6	I	Transmit System Sync for Framer 6.
Y7	TSSYNC7	I	Transmit System Sync for Framer 7.
R4	TSSYNC8	I	Transmit System Sync for Framer 8.
T15	TSSYNC9	I	Transmit System Sync for Framer 9.
W8	TSSYNC10	I	Transmit System Sync for Framer 10.
Y17	TSSYNC11	I	Transmit System Sync for Framer 11.
U19	TSSYNC12	I	Transmit System Sync for Framer 12.
C13	TSSYNC13/NC	I	Transmit System Sync for Framer 13. NC on Four x Three.
R20	TSSYNC14/NC	I	Transmit System Sync for Framer 14. NC on Four x Three.
D20	TSSYNC15/NC	I	Transmit System Sync for Framer 15. NC on Four x Three.

A17	TSSYNC16/NC	I	Transmit System Sync for Framer 16. NC on Four x Three.
E3	TSYNC1	I/O	Transmit Sync for Framer 1.
F4	TSYNC2	I/O	Transmit Sync for Framer 2.
E7	TSYNC3	I/O	Transmit Sync for Framer 3.
A4	TSYNC4	I/O	Transmit Sync for Framer 4.
R2	TSYNC5	I/O	Transmit Sync for Framer 5.
W5	TSYNC6	I/O	Transmit Sync for Framer 6.
T5	TSYNC7	I/O	Transmit Sync for Framer 7.
M5	TSYNC8	I/O	Transmit Sync for Framer 8.
T13	TSYNC9	I/O	Transmit Sync for Framer 9.
W13	TSYNC10	I/O	Transmit Sync for Framer 10.
U16	TSYNC11	I/O	Transmit Sync for Framer 11.
N16	TSYNC12	I/O	Transmit Sync for Framer 12.
J16	TSYNC13/NC	I/O	Transmit Sync for Framer 13. NC on Four x Three.
F18	TSYNC14/NC	I/O	Transmit Sync for Framer 14. NC on Four x Three.
C15	TSYNC15/NC	I/O	Transmit Sync for Framer 15. NC on Four x Three.
D12	TSYNC16/NC	I/O	Transmit Sync for Framer 16. NC on Four x Three.
Y16	WR*	I	Write Input.

DS21FF42 / DS21FF44 (Four x Four) PCB Land Pattern Figure 2

The diagram shown below is the lead pattern that will be placed on the target PCB. This is the same pattern that would be seen as viewed through the MCM from the top.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	rpos 1	rclk 1	ts sync 1	tsync 4	tclk 4	dvss 1	rsync 4	rch blk 4	rneg 4	tneg 4	dvss 4	rser 16	test	rpos 16	rsig 16	tsig 16	ts sync 16	tser 16	jtdof	rpos 15
B	rsync 1	rneg 1	tpos 1	tser 1	sys clk 1	clksi	8 mclk	sys clk 4	rclk 4	tpos 4	dvdd 4	rsync 16	rneg 16	tpos 16	tneg 16	rch blk 16	rsync 15	rch blk 15	tpos 15	tsig 15
C	rser 1	rch blk 1	tneg 1	tsig 1	tclk 3	rser 3	dvdd 1	rser4	rpos 4	tsig 4	tclk 16	rclk 16	ts sync 13	sys clk 16	tsync 15	rser 15	rsig 15	rclk 15	tneg 15	rneg 15
D	tclk 1	dvdd 1	rsig 1	rsig 3	dvss 1	rsync 3	tser 4	rsig4	rneg 3	rclk 3	tneg 13	tsync 16	tser 13	rclk 13	rpos 13	rch blk 13	dvdd 4	tser 15	dvss 4	ts sync 15
E	tser 2	sys clk 2	tsync 1	dvdd 1	sys clk 3	rch blk 3	tsync 3	ts sync 4	dvss 1	jtdi	tsig 13	tpos 13	sys clk 13	rneg 13	rsig 13	rser 13	tclk 15	rd*	cs4*	sys clk 15
F	tsig 2	ts sync 2	tser 3	tsync 2	tneg 3											dvdd 4	tser 14	tsync 14	tclk 14	rser 14
G	rsync 2	rsig 2	rch blk 2	tsig 3	ts sync 3											int*	A6	A4	A2	A0
H	rpos 2	rneg 2	rser 2	rpos 3	tclk 2											jtms	A7	A5	A3	A1
J	tneg 2	tpos 2	rclk 8	rsync 8	tpos 3											tsync 13	rsync 13	rpos 14	rsync 14	dvss 4
K	rclk 2	tclk 8	dvdd 2	dvss 2	rsig 8											tclk 13	jtrst*	tneg 14	rsig 14	rch blk 14
L	tneg 5	tpos 5	tsig 5	ts sync 5	tser 5											dvdd 3	D6	D4	D2	D0
M	rpos 5	rneg 5	rclk 5	sys clk 5	tsync 8											tser 9	D7	D5	D3	D1
N	rch blk 5	rsig 5	rsync 5	rser 8	rch blk 8											tsync 12	rclk 12	sys clk 14	tpos 14	rneg 14
P	rser 5	dvdd 2	rneg 8	rpos 8	tneg 8											tclk 12	mux	rsync 12	tsig 14	rclk 14
R	tclk 5	tsync 5	tpos 8	ts sync 8	tsig 8											dvss 3	sys clk 12	tsig 12	rpos 12	ts sync 14
T	tser 6	sys clk 6	tser 8	sys clk 9	tsync 7	tclk 7	rser 7	cs1*	rclk 9	rpos 9	rsync 9	dvdd 3	tsync 9	tpos 9	ts sync 9	rser 12	jtdot	tclk 11	tneg 12	rneg 12
U	ts sync 6	tsig 6	dvss 2	dvss 3	rsync 7	rch blk 7	dvdd 2	dvss 2	rneg 9	rsig 9	rser 9	sys clk 11	tclk 9	tneg 9	tsig 9	tsync 11	rch blk 12	tsig 11	tssync 12	rsig 12
V	rclk 6	tneg 6	rneg 6	rsig 6	rpos 7	rsig 7	rneg 7	tneg 7	tsig 7	tsig 10	rpos 10	tneg 10	rsync 10	jtclk	rsync 11	rser 11	rch blk 11	tpos 11	dvdd 3	tpos 12
W	tpos 6	rpos 6	sys clk 8	rser 6	tsync 6	rclk 7	tpos 7	ts sync 10	tser 10	rclk 10	rneg 10	rch blk 10	tsync 10	fs1	bts	tser 11	rneg 11	tneg 11	rsig 11	tser 12
Y	rch blk 6	rsync 6	tclk 6	cs2*	sys clk 7	tser 7	ts sync 7	rch blk 9	sys clk 10	tpos 10	rsig 10	rser 10	tclk 10	fs0	cs3*	wr*	ts sync 11	rclk 11	rpos 11	dvss 3

DS21FT42 / DS21FT44 (Four x Three) PCB Land Pattern Figure 3

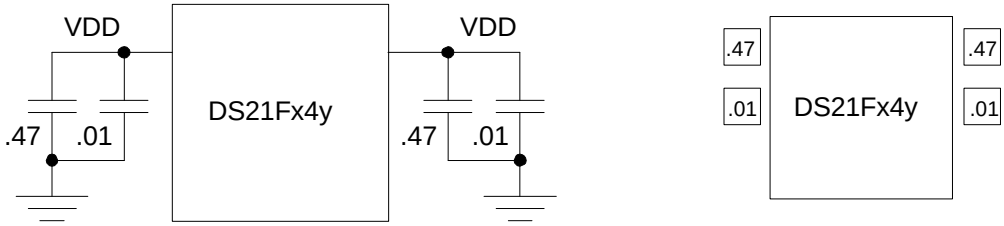
The diagram shown below is the lead pattern that will be placed on the target PCB. This is the same pattern that would be seen as viewed through the MCM from the top.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	rpos 1	rclk 1	ts sync 1	tsync 4	tclk 4	dvss 1	rsync 4	rch blk 4	rneg 4	tneg 4	nc	nc	test	ns	ns	nc	nc	nc	nc	nc
B	rsync 1	rneg 1	tpos 1	tser 1	sys clk 1	clksi	8 mclk	sys clk 4	rclk 4	tpos 4	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
C	rser 1	rch blk 1	tneg 1	tsig 1	tclk 3	rser 3	dvdd 1	rser4	rpos 4	tsig 4	nc	nc	nc	nc	ns	nc	nc	nc	nc	nc
D	tclk 1	dvdd 1	rsig 1	rsig 3	dvss 1	rsync 3	tser 4	rsig4	rneg 3	rclk 3	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
E	tser 2	sys clk 2	tsync 1	dvdd 1	sys clk 3	rch blk 3	tsync 3	ts sync 4	dvss 1	jtdi	nc	nc	nc	nc	nc	nc	nc	rd*	nc	nc
F	tsig 2	ts sync 2	tser 3	tsync 2	tneg 3											nc	nc	nc	nc	nc
G	rsync 2	rsig 2	rch blk 2	tsig 3	ts sync 3											int*	A6	A4	A2	A0
H	rpos 2	rneg 2	rser 2	rpos 3	tclk 2											jtms	A7	A5	A3	A1
J	tneg 2	tpos 2	rclk 8	rsync 8	tpos 3											nc	nc	nc	nc	nc
K	rclk 2	tclk 8	dvdd 2	dvss 2	rsig 8											nc	jtrst*	nc	nc	nc
L	tneg 5	tpos 5	tsig 5	ts sync 5	tser 5											dvdd 3	D6	D4	D2	D0
M	rpos 5	rneg 5	rclk 5	sys clk 5	tsync 8											tser 9	D7	D5	D3	D1
N	rch blk 5	rsig 5	rsync 5	rser 8	rch blk 8											tsync 12	rclk 12	nc	nc	nc
P	rser 5	dvdd 2	rneg 8	rpos 8	tneg 8											tclk 12	mux	rsync 12	nc	nc
R	tclk 5	tsync 5	tpos 8	ts sync 8	tsig 8											dvss 3	sys clk 12	tsig 12	rpos 12	nc
T	tser 6	sys clk 6	tser 8	sys clk 9	tsync 7	tclk 7	rser 7	cs1*	rclk 9	rpos 9	rsync 9	dvdd 3	tsync 9	tpos 9	ts sync 9	rser 12	jtdot	tclk 11	tneg 12	rneg 12
U	ts sync 6	tsig 6	dvss 2	dvss 3	rsync 7	rch blk 7	dvdd 2	dvss 2	rneg 9	rsig 9	rser 9	sys clk 11	tclk 9	tneg 9	tsig 9	tsync 11	rch blk 12	tsig 11	tssync 12	rsig 12
V	rclk 6	tneg 6	rneg 6	rsig 6	rpos 7	rsig 7	rneg 7	tneg 7	tsig 7	tsig 10	rpos 10	tneg 10	rsync 10	jtclk	rsync 11	rser 11	rch blk 11	tpos 11	dvdd 3	tpos 12
W	tpos 6	rpos 6	sys clk 8	rser 6	tsync 6	rclk 7	tpos 7	ts sync 10	tser 10	rclk 10	rneg 10	rch blk 10	tsync 10	fs1	bts	tser 11	rneg 11	tneg 11	rsig 11	tser 12
Y	rch blk 6	rsync 6	tclk 6	cs2*	sys clk 7	tser 7	ts sync 7	rch blk 9	sys clk 10	tpos 10	rsig 10	rser 10	tclk 10	fs0	cs3*	wr*	ts sync 11	rclk 11	rpos 11	dvss 3

POWER SUPPLY DE-COUPLING

In a typical PCB layout for the MCM, all of the VDD pins will connect to a common power plane and all the VSS lines will connect to a common ground plane. The recommended method for de-coupling is shown below in both schematic and pictorial form. As shown in the pictorial, the capacitors should be symmetrically located about the device. Figure 4 uses standard capacitors, two .47 uf ceramics and two .01uf ceramics. Since VDD and VSS signals will typically pass vertically to the power and ground planes of a PCB, the de-coupling caps must be placed as close to the DS21Fx4y as possible and routed vertically to power and ground planes.

De-coupling scheme using standard tantalum caps. Figure 4



DS21FF42 / DS21FT42 / DS21FF44 / DS21FT44 Mechanical Dimensions