

**DALLAS**  
SEMICONDUCTOR

## DS1689/DS1693

### 3 Volt/5 Volt Serialized Real Time Clock with NV RAM Control

#### FEATURES

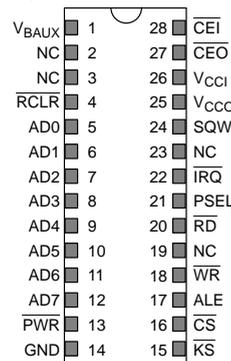
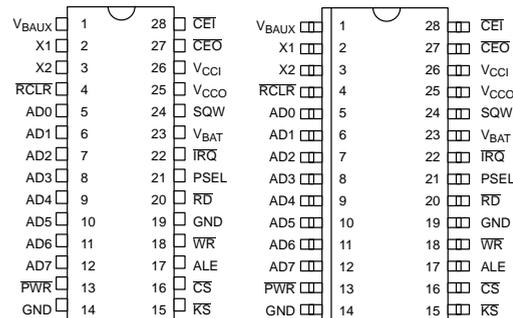
Incorporates industry standard DS1287 PC clock plus enhanced features:

- +3 or +5 volt operation
- 64-bit Silicon serial number
- 64-bit customer specific ROM or additional serial number available
- Power control circuitry supports system power on from date/time alarm or key closure
- Automatic battery backup and write protection to external SRAM
- Crystal select bit allows RTC to operate with 6 pF or 12.5 pF crystal
- 114 bytes user NVRAM
- Auxiliary battery input
- RAM clear input
- Century register
- 32 KHz output for power management
- 32-bit  $V_{CC}$  powered elapsed time counter
- 32-bit  $V_{BAT}$  powered elapsed time counter
- 16-bit power cycle counter
- Compatible with existing BIOS for original DS1287 functions
- Available as chip (DS1689) or standalone module with embedded battery and crystal (DS1693)
- Chips are available in industrial temperature version
- Timekeeping algorithm includes leap year compensation valid up to 2100

#### ORDERING INFORMATION

PART #	DESCRIPTION
DS1689	RTC Chip, 28-pin DIP
DS1689S	RTC Chip, 28-pin SOIC
DS1693	RTC Module; 28-pin DIP

#### PIN ASSIGNMENT



#### PIN DESCRIPTION

X1	– Crystal Input
X2	– Crystal Output
$\overline{RCLR}$	– RAM Clear Input
AD0-AD7	– Mux'ed Address/Data Bus
PWR	– Power-on Interrupt Output (open drain)
$\overline{KS}$	– Kickstart Input
$\overline{CS}$	– RTC Chip Select Input
ALE	– RTC Address Strobe
$\overline{WR}$	– RTC Write Data Strobe
$\overline{RD}$	– RTC Read Data Strobe
$V_{CCO}$	– RAM Power Supply Output

$\overline{\text{IRQ}}$	– Interrupt Request Output (open drain)
SQW	– Square Wave Output
$V_{\text{CCI}}$	– +3 or +5 Volt Main Supply
GND	– Ground
$V_{\text{BAT}}$	– Battery + Supply
$V_{\text{BAUX}}$	– Auxiliary Battery Supply
PSEL	– +3 or +5 Volt Power Select
$\overline{\text{CEI}}$	– RAM Chip Enable In
$\overline{\text{CEO}}$	– RAM Chip Enable Out

## DESCRIPTION

The DS1689/DS1693 is a real time clock (RTC) designed as a successor to the industry standard DS1285, DS1385, DS1485, and DS1585 PC real time clocks. This device provides the industry standard DS1285 clock function with the new feature of either +3.0 or +5.0 volt operation and automatic backup and write protection to an external SRAM. The DS1689 also incorporates a number of enhanced features including a silicon serial number, power on/off control circuitry, 114 bytes of user NVSRAM, power on elapsed timer, and power cycle counter.

Each DS1689/DS1693 is individually manufactured with a unique 64-bit serial number as well as an additional 64-bit customer specific ROM or serial number. The serial number is programmed and tested at Dallas to insure that no two devices are alike. The serial number can be used to electronically identify a system for purposes such as establishment of a network node address or for maintenance tracking. Blocks of available numbers from Dallas Semiconductor can be reserved by the customer.

The serialized RTC's also incorporate power control circuitry which allows the system to be powered on via an external stimulus, such as a keyboard or by a time and date (wake up) alarm. The  $\overline{\text{PWR}}$  output pin can be triggered by one or either of these events, and can be used to turn on an external power supply. The  $\overline{\text{PWR}}$  pin is under software control, so that when a task is complete, the system power can then be shut down.

The DS1689/DS1693 incorporates a power on elapsed time counter, a power on cycle counter, and a battery powered continuous counter. These three counters provide valuable information for maintenance and warranty requirements.

Automatic backup and write protection for an external SRAM is provided through the  $V_{\text{CCO}}$  and  $\overline{\text{CEO}}$  pins. The

lithium energy source used to permanently power the real time clock is also used to retain RAM data in the absence of  $V_{\text{CC}}$  power through the  $V_{\text{CCO}}$  pin. The chip enable output to RAM ( $\overline{\text{CEO}}$ ) is controlled during power transients to prevent data corruption.

The DS1689 is a clock/calendar chip with the features described above. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. The DS1693 incorporates the DS1689 chip, a 32.768 KHz crystal, and a lithium battery in a complete, self-contained timekeeping module. The entire unit is fully tested at Dallas Semiconductor such that a minimum of 10 years of timekeeping and data retention in the absence of  $V_{\text{CC}}$  is guaranteed.

## OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1689/DS1693. The following paragraphs describe the function of each pin.

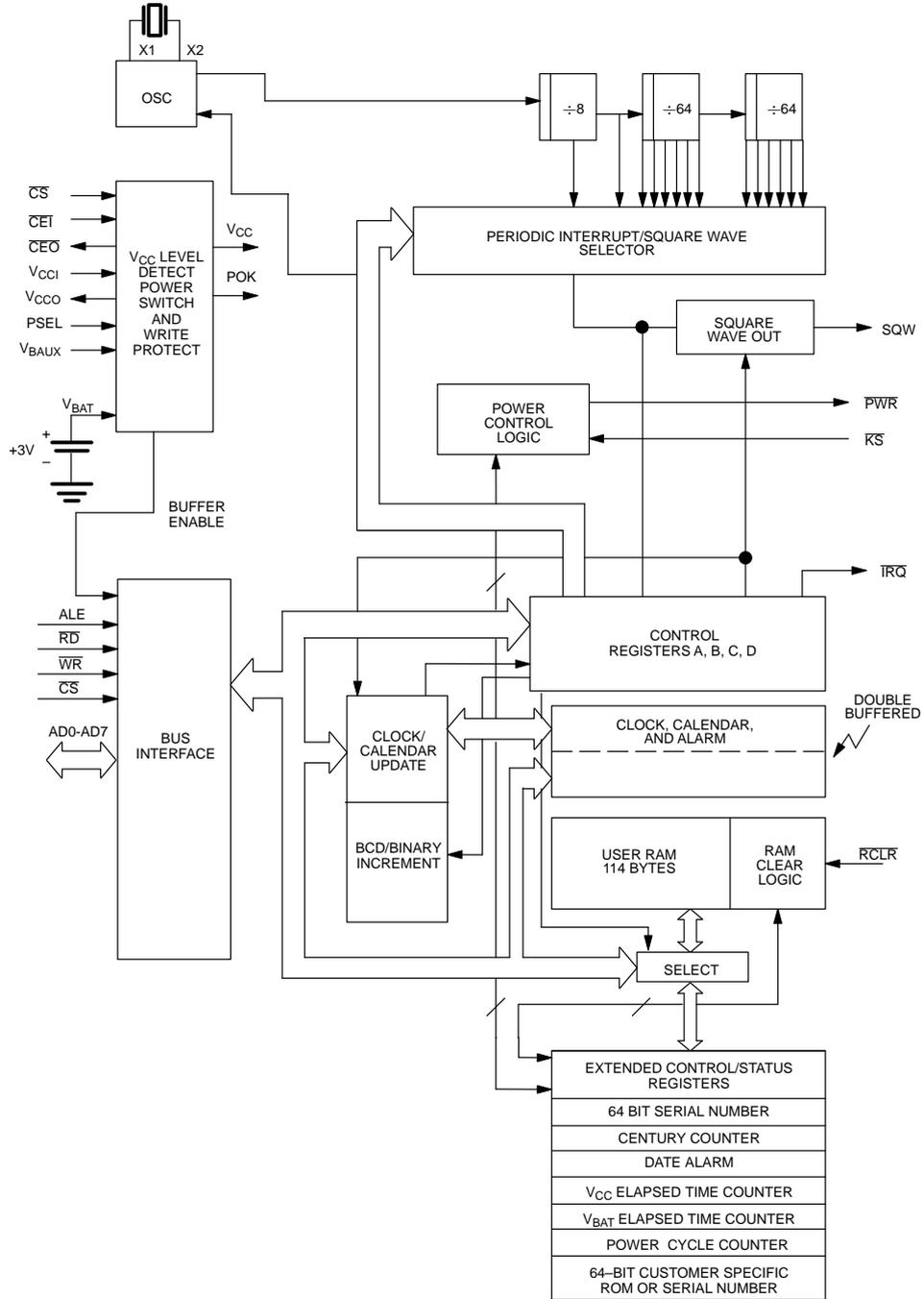
## SIGNAL DESCRIPTIONS

**GND,  $V_{\text{CCI}}$**  - DC power is provided to the device on these pins.  $V_{\text{CCI}}$  is the +3 volt or +5 volt input. Five volt operation is selected when the PSEL pin is at a logic 1. If PSEL is floated or at a logic 0, the device will be in auto-sense mode and will determine the correct operating voltage based on the  $V_{\text{CCI}}$  voltage level.

**PSEL (Power Select Input)** – This pin selects whether 3 volt operation or 5 volt operation will be used. When PSEL is a logic 1, 5 volt operation is selected. When PSEL is a logic 0 or is floated, the device will be in auto-sense mode and will determine the correct mode of operation based on the voltage on  $V_{\text{CCI}}$ .

**$V_{\text{CCO}}$  (External SRAM Power Supply Output)** – This pin will be internally connected to  $V_{\text{CCI}}$  when  $V_{\text{CCI}}$  is within nominal limits. However, during power fail,  $V_{\text{CCO}}$  will be internally connected to the  $V_{\text{BAT}}$  or  $V_{\text{BAUX}}$  (whichever is larger). For 5 volt operation, switch over from  $V_{\text{CCI}}$  to the backup supply occurs when  $V_{\text{CCI}}$  drops below the larger of  $V_{\text{BAT}}$  and  $V_{\text{BAUX}}$ . For 3 volt operation, switch over from  $V_{\text{CCI}}$  to the backup supply occurs at  $V_{\text{PF}}$  if  $V_{\text{PF}}$  is less than  $V_{\text{BAT}}$  and  $V_{\text{BAUX}}$ . If  $V_{\text{PF}}$  is greater than  $V_{\text{BAT}}$  and  $V_{\text{BAUX}}$ , the switch from  $V_{\text{CCI}}$  to the backup supply occurs when  $V_{\text{CCI}}$  drops below the larger of  $V_{\text{BAT}}$  and  $V_{\text{BAUX}}$ .

DS1689/DS1693 BLOCK DIAGRAM Figure 1



**SQW (Square Wave Output)** – The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in Register B. A 32 KHz SQW signal is output when SQWE=1, the Enable 32 KHz (E32K) bit in extended register 04BH is a logic one, and  $V_{CC}$  is above  $V_{PF}$ . A 32 KHz square wave is also available when  $V_{CC}$  is less than  $V_{PF}$  if E32K=1, ABE=1, and voltage is applied to  $V_{BAUX}$ .

**AD0–AD7 (Multiplexed Bidirectional Address/Data Bus)** – Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1689 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, at which time the DS1689/DS1693 latches the address. Valid write data must be present and held stable during the latter portion of the  $\overline{WR}$  pulse. In a read cycle the DS1689/DS1693 outputs 8 bits of data during the latter portion of the  $\overline{RD}$  pulse. The read cycle is terminated and the bus returns to a high impedance state as  $\overline{RD}$  transitions high. The address/data bus also serves as a bidirectional data path for the external extended RAM.

**ALE (RTC Address Strobe Input; active high)** – A pulse on the address strobe pin serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS1689/DS1693.

**$\overline{RD}$  (RTC Read Input; active low)** –  $\overline{RD}$  identifies the time period when the DS1689/DS1693 drives the bus with RTC read data. The  $\overline{RD}$  signal is an enable signal for the output buffers of the clock.

**$\overline{WR}$  (RTC Write Input; active low)** – The  $\overline{WR}$  signal is an active low signal. The  $\overline{WR}$  signal defines the time period during which data is written to the addressed register.

**$\overline{CS}$  (RTC Chip Select Input; active low)** – The Chip Select signal must be asserted low during a bus cycle for the RTC portion of the DS1689/DS1693 to be accessed.  $\overline{CS}$  must be kept in the active state during  $\overline{RD}$  and  $\overline{WR}$  timing. Bus cycles which take place with ALE

asserted but without asserting  $\overline{CS}$  will latch addresses. However, no data transfer will occur.

**$\overline{IRQ}$  (Interrupt Request Output; open drain, active low)** – The  $\overline{IRQ}$  pin is an active low output of the DS1689/DS1693 that can be tied to the interrupt input of a processor. The  $\overline{IRQ}$  output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the  $\overline{IRQ}$  pin, the application software must clear all enabled flag bits contributing to  $\overline{IRQ}$ 's active state.

When no interrupt conditions are present, the  $\overline{IRQ}$  level is in the high impedance state. Multiple interrupting devices can be connected to an  $\overline{IRQ}$  bus. The  $\overline{IRQ}$  pin is an open drain output and requires an external pull-up resistor.

**$\overline{CEI}$  (RAM Chip Enable Input; active low)** –  $\overline{CEI}$  should be driven low to enable the external RAM.

**$\overline{CEO}$  (RAM Chip Enable Output; active low)** – When power is valid,  $\overline{CEO}$  will equal  $\overline{CEI}$ . When power is not valid,  $\overline{CEO}$  will be driven high regardless of  $\overline{CEI}$ .

**$\overline{PWR}$  (Power On Output; open drain, active low)** – The  $\overline{PWR}$  pin is intended for use as an on/off control for the system power. With  $V_{CC}$  voltage removed from the DS1689/DS1693,  $\overline{PWR}$  may be automatically activated from a Kickstart input via the  $\overline{KS}$  pin or from a Wake Up interrupt. Once the system is powered on, the state of  $\overline{PWR}$  can be controlled via bits in the Dallas registers.

**$\overline{KS}$  (Kickstart Input; active low)** – When  $V_{CC}$  is removed from the DS1689/DS1693, the system can be powered on in response to an active low transition on the  $\overline{KS}$  pin, as might be generated from a key closure.  $V_{BAUX}$  must be present and Auxiliary Battery Enable bit (ABE) must be set to 1 if the kickstart function is used, and the  $\overline{KS}$  pin must be pulled up to the  $V_{BAUX}$  supply. While  $V_{CC}$  is applied, the  $\overline{KS}$  pin can be used as an interrupt input.

**$\overline{RCLR}$  (RAM Clear Input; active low)** – If enabled by software, taking  $\overline{RCLR}$  low will result in the clearing of the 114 bytes of user RAM. When enabled,  $\overline{RCLR}$  can be activated whether or not  $V_{CC}$  is present.

**$V_{BAUX}$**  – Auxiliary battery input required for kickstart and wake up features. This input also supports clock/calendar and External NVRAM if  $V_{BAT}$  is at lower voltage or is not present. A standard +3 volt lithium cell or

other energy source can be used. Battery voltage must be held between +2.5 and +3.7 volts for proper operation. If  $V_{BAUX}$  is not going to be used it should be grounded and auxiliary battery enable bit bank 1, register 4BH, should=0.

#### DS1689 ONLY

**X1, X2** – Connections for a standard 32.768 KHz quartz crystal. For greatest accuracy, the DS1689 must be used with a crystal that has a specified load capacitance of either 6 pF or 12.5 pF. The Crystal Select (CS) bit in Extended Control Register 4B is used to select operation with a 6 pF or 12.5 pF crystal. The crystal is attached directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard-ringed with ground and that high frequency signals be kept away from the crystal area.

For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks". The DS1689 can also be driven by an external 32.768 KHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

**V<sub>BAT</sub>** – Battery input for any standard 3 Volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation.

#### POWER-DOWN/POWER-UP CONSIDERATIONS

The real-time clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the  $V_{CCI}$  input. When  $V_{CCI}$  is applied to the DS1689/DS1693 and reaches a level of greater than  $V_{PF}$  (power fail trip point), the device becomes accessible after  $t_{REC}$ , provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied.

When PSEL is floating or logic 0, the DS1689 is in auto-sense mode and 3 volt or 5 volt operation is determined

based on the voltage on  $V_{CCI}$ . Selection of 5 volt operation is automatically invoked when  $V_{CCI}$  rises above 4.5 volts for a minimum of  $t_{REC}$ . However, 3 volt operation is automatically selected if  $V_{CCI}$  does not rise above the level of 4.25 volts. Selection of the power supply input levels requires 150 ms of input stability before operation can commence.

When 5 volt operation is selected, the device is fully accessible and data can be written and read only when  $V_{CCI}$  is greater than 4.5 volts. When  $V_{CCI}$  is below 4.5 volts, read and writes are inhibited. However, the time-keeping function continues unaffected by the lower input voltage. As  $V_{CC}$  falls below the greater of  $V_{BAT}$  and  $V_{BAUX}$ , the RAM and timekeeper are switched over to a lithium battery connected either to the  $V_{BAT}$  pin or  $V_{BAUX}$  pin.

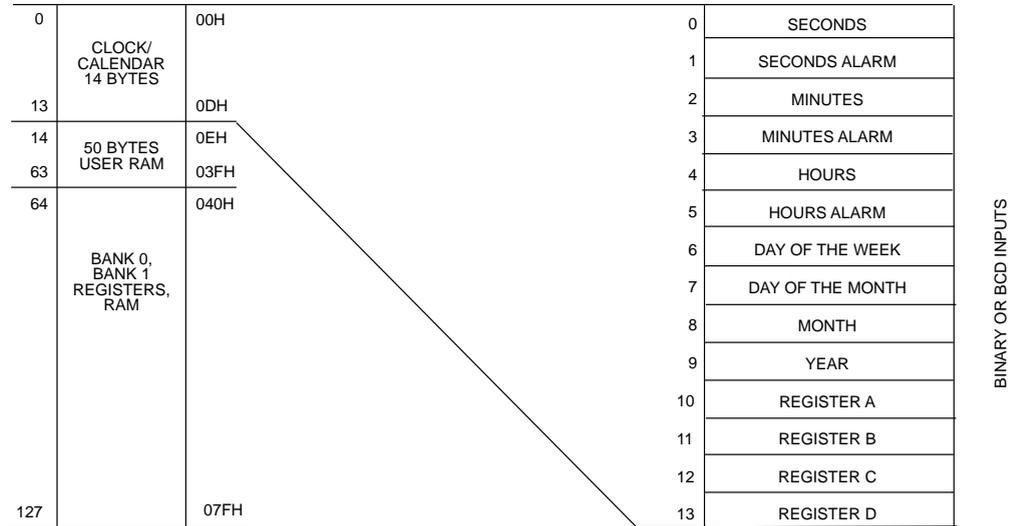
When 3 volt operation is selected and applied within normal limits, the device is fully accessible and data can be written or read. When  $V_{CCI}$  falls below  $V_{PF}$ , access to the device is inhibited. If  $V_{PF}$  is less than  $V_{BAT}$  and  $V_{BAUX}$ , the power supply is switched from  $V_{CCI}$  to the backup supply (the greater of  $V_{BAT}$  and  $V_{BAUX}$ ) when  $V_{CCI}$  drops below  $V_{PF}$ . If  $V_{PF}$  is greater than  $V_{BAT}$  and  $V_{BAUX}$ , the power supply is switched from  $V_{CCI}$  to the backup supply when  $V_{CCI}$  drops below the larger of  $V_{BAT}$  and  $V_{BAUX}$ .

When  $V_{CC}$  falls below  $V_{PF}$ , the chip is write-protected. With the possible exception of the KS,  $\overline{PWR}$ , and SQW pins, all inputs are ignored and all outputs are in a high impedance state.

#### RTC ADDRESS MAP

The address map for the RTC registers of the DS1689/DS1693 is shown in Figure 2. The address map consists of the 14 clock/calendar registers. Ten registers contain the time, calendar, and alarm data, and four bytes are used for control and status. All registers can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit 7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

**DS1689 REAL TIME CLOCK ADDRESS MAP** Figure 2**TIME, CALENDAR AND ALARM LOCATIONS**

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations that reside in both bank 0 and in bank 1, plus the two extended registers that reside in bank 1 only (bank 0 and bank 1 switching will be explained later in this text).

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a log-

ic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The four alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a "don't care" state in one or more of the four alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second. The three alarm bytes may be used in conjunction with the date alarm as described in the Wakeup/Kickstart section. The century counter will be discussed later in this text.

**TIME, CALENDAR AND ALARM DATA MODES** Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
00H	Seconds	0–59	00–3B	00–59
01H	Seconds Alarm	0–59	00–3B	00–59
02H	Minutes	0–59	00–3B	00–59
03H	Minutes Alarm	0–59	00–3B	00–59
04H	Hours 12–hr. Mode	1–12	01–0C AM, 81–8C PM	01–12 AM, 81–92 PM
	Hours 24–Hour Mode	0–23	00–17	00–23
05H	Hours Alarm 12–hr. Mode	1–12	01–0C AM, 81–8C PM	01–12AM, 81–92 PM
	Hours Alarm 24–hr. Mode	0–23	00–17	00–23
06H	Day of Week Sunday=1	1–7	01–07	01–07
07H	Date of Month	1–31	01–1F	01–31
08H	Month	1–12	01–0C	01–12
09H	Year	0–99	00–63	00–99
BANK 1, 48H	Century	0–99	00–63	00–99
BANK 1, 49H	Date Alarm	1–31	01–1F	01–31

**CONTROL REGISTERS**

The four control registers; A, B, C, and D reside in both bank 0 and bank 1. These registers are accessible at all times, even during the update cycle.

**NONVOLATILE RAM – RTC**

The 114 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS1689/DS1693. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible when bank 0 is selected.

**INTERRUPT CONTROL**

The DS1689/DS1693 includes six separate, fully automatic sources of interrupt for a processor:

1. Alarm interrupt
2. Periodic interrupt
3. Update-ended interrupt
4. Wake up interrupt
5. Kickstart interrupt
6. RAM clear interrupt

The conditions which generate each of these independent interrupt conditions are described in greater detail

elsewhere in this data sheet. This section describes the overall control of the interrupts.

The application software can select which interrupts, if any, are to be used. There are a total of six bits including three bits in Register B and three bits in Extended Register B which enable the interrupts. The extended register locations are described later. Writing a logic 1 to an interrupt enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in the interrupt enable bit prohibits the  $\overline{\text{IRQ}}$  pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled,  $\overline{\text{IRQ}}$  will immediately be set at an active level, even though the event initiating the interrupt condition may have occurred much earlier. As a result, there are cases where the software should clear these earlier generated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to a logic 1 in Register C or in Extended Register A. These flag bits are set regardless of the setting of the corresponding enable bit located either in Register B or in Extended Register B. The flag bits can be used in a polling mode without enabling the corresponding enable bits.

However, care should be taken when using the flag bits of Register C as they are automatically cleared to 0 immediately after they are read. Double latching is implemented on these bits so that bits which are set remain stable throughout the read cycle. All bits which were set are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The flag bits in Extended Register A are not automatically cleared following a read. Instead, each flag bit can be cleared to 0 only by writing 0 to that bit.

When using the flag bits with fully enabled interrupts, the  $\overline{\text{IRQ}}$  line will be driven low when an interrupt flag bit is set and its corresponding enable bit is also set.  $\overline{\text{IRQ}}$  will be held low as long as at least one of the six possible interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a 1 whenever the  $\overline{\text{IRQ}}$  pin is being driven low as a result of one of the six possible active sources. Therefore, determination that the DS1689/DS1693 initiated an interrupt is accomplished by reading Register C and finding IRQF=1. IRQF will remain set until all enabled interrupt flag bits are cleared to 0.

### SQUARE WAVE OUTPUT SELECTION

The SQW pin can be programmed to output a variety of frequencies divided down from the 32.768 KHz crystal tied to X1 and X2. The square wave output is enabled and disabled via the SQWE bit in Register B. If the square wave is enabled (SQWE=1), then the output frequency will be determined by the settings of the E32K bit in Extended Register B and by the RS3-0 bits in Register A. If the E32K = 1, then a 32.768 KHz square wave will be output on the SQW pin regardless of the settings of RS3-0.

If E32K = 0, then the square wave output frequency is determined by the RS3-0 bits. These bits control a 1-of-15 decoder which selects one of thirteen taps that divide the 32.768 KHz frequency. The RS3-0 bits establish the SQW output frequency as shown in Table 2. In addition, RS3-0 bits control the periodic interrupt selection as described below.

If SQWE1, E32K=1, and the Auxiliary Battery Enable bit (ABE, bank 1; register 04BH) is enabled, and voltage is applied to  $V_{\text{BAUX}}$  then the 32 KHz square wave output

signal will be output on the SQW pin in the absence of  $V_{\text{CC}}$ . This facility is provided to clock external power management circuitry. If any of the above requirements are not met, no square wave output signal will be generated on the SQW pin in the absence of  $V_{\text{CC}}$ .

A pattern of 01X in the DV2, DV1, and DV0, bits respectively, will turn the oscillator on and enable the countdown chain. Note that this is different than the DS1287, which required a pattern of 010 in these bits. DV0 is now a “don’t care” because it is used for selection between register banks 0 and 1.

A pattern of 11X will turn the oscillator on, but the oscillator’s countdown chain will be held in reset, as it was in the DS1287. Any other bit combination for DV2 and DV1 will keep the oscillator off.

### PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the  $\overline{\text{IRQ}}$  pin to go to an active state from once every 500 ms to once every 122  $\mu\text{s}$ . This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same RS3-0 bits in Register A which select the square wave frequency (see Table 2). Changing the bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

### UPDATE CYCLE

The Serialized RTC executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, alarm and elapsed time byte is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows the time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a “don’t care” code is present in all three positions.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244  $\mu$ s later. If a low is read on the UIP bit, the user has at least 244  $\mu$ s before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244  $\mu$ s.

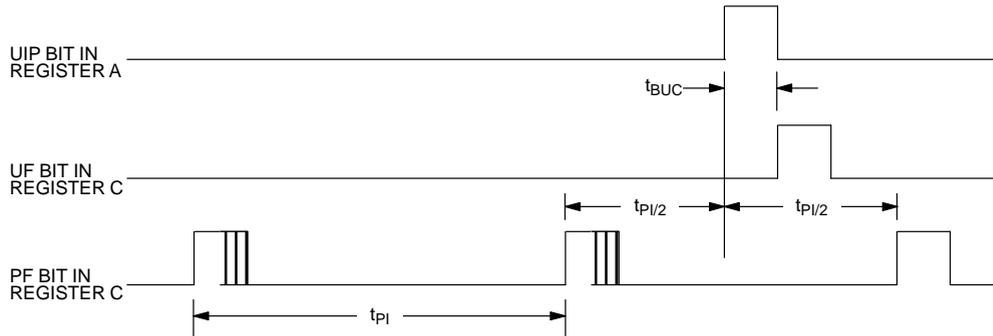
**PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY** Table 2

EXT. REG. B	SELECT BITS REGISTER A				$t_{PI}$ PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
	E32K	RS3	RS2	RS1		
0	0	0	0	0	None	None
0	0	0	0	1	3.90625 ms	256 Hz
0	0	0	1	0	7.8125 ms	128 Hz
0	0	0	1	1	122.070 $\mu$ s	8.192 KHz
0	0	1	0	0	244.141 $\mu$ s	4.096 KHz
0	0	1	0	1	488.281 $\mu$ s	2.048 KHz
0	0	1	1	0	976.5625 $\mu$ s	1.024 KHz
0	0	1	1	1	1.953125 ms	512 Hz
0	1	0	0	0	3.90625 ms	256 Hz
0	1	0	0	1	7.8125 ms	128 Hz
0	1	0	1	0	15.625 ms	64 Hz
0	1	0	1	1	31.25 ms	32 Hz
0	1	1	0	0	62.5 ms	16 Hz
0	1	1	0	1	125 ms	8 Hz
0	1	1	1	0	250 ms	4 Hz
0	1	1	1	1	500 ms	2 Hz
1	X	X	X	X	*	32.768 KHz

\*RS3-RS0 determine periodic interrupt rates as listed for E32K=0.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than  $t_{BUC}$  allow valid time and date informa-

tion to be reached at each occurrence of the periodic interrupt. The reads should be complete within  $(t_{PI} / 2 + t_{BUC})$  to ensure that data is not read during the update cycle.

**UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP** Figure 3

$t_{PI}$  = PERIODIC INTERRUPT TIME INTERNAL PER TABLE 1  
 $t_{BUC}$  = DELAY TIME BEFORE UPDATE CYCLE = 244  $\mu$ s

**REGISTER A**

MSB				LSB			
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

**UIP** – The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244  $\mu$ s. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

**DV0, DV1, DV2** – These bits are defined as follows:

- DV2 = Countdown Chain  
 1 – resets countdown chain only if DV1=1  
 0 – countdown chain enabled
- DV1 = Oscillator Enable  
 0 – oscillator off  
 1 – oscillator on
- DV0 = Bank Select  
 0 – original bank  
 1 – extended registers

A pattern of 01X is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 01X is written to DV2, DV1, and DV0.

**RS3, RS2, RS1, RS0** – These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

Enable the interrupt with the PIE bit;

Enable the SQW output pin with the SQWE bit;

Enable both at the same time and the same rate; or

Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

**REGISTER B**

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

**SET** – When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1689/DS1693.

**PIE** – The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the  $\overline{\text{IRQ}}$  pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the  $\overline{\text{IRQ}}$  pin low at a rate specified by the RS3–RS0 bits of Register A. A zero in the PIE bit blocks the  $\overline{\text{IRQ}}$  output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1689/DS1693 functions.

**AIE** – The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert  $\overline{\text{IRQ}}$ . An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the  $\overline{\text{IRQ}}$  signal. The internal functions of the DS1689/DS1693 do not affect the AIE bit.

**UIE** – The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert  $\overline{\text{IRQ}}$ . The SET bit going high clears the UIE bit.

**SQWE** – When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 and the E32K bit is driven out on the SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit.

**DM** – The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data

while a zero in DM specifies Binary Coded Decimal (BCD) data.

**24/12** – The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write.

**DSE** – The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 am to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

**REGISTER C**

MSB						LSB	
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

**IRQF** – The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

$$\begin{aligned} \text{PF} = \text{PIE} = 1 & & \text{WF} = \text{WIE} = 1 \\ \text{AF} = \text{AIE} = 1 & & \text{KF} = \text{KSE} = 1 \\ \text{UF} = \text{UIE} = 1 & & \text{RF} = \text{RIE} = 1 \end{aligned}$$

$$\text{i.e., IRQF} = (\text{PF} \bullet \text{PIE}) + (\text{AF} \bullet \text{AIE}) + (\text{UF} \bullet \text{UIE}) + (\text{WF} \bullet \text{WIE}) + (\text{KF} \bullet \text{KSE}) + (\text{RF} \bullet \text{RIE})$$

Any time the IRQF bit is a one, the  $\overline{\text{IRQ}}$  pin is driven low. Flag bits PF, AF, and UF are cleared after Register C is read by the program.

**PF** – The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the  $\overline{\text{IRQ}}$  signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

**AF** – A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the  $\overline{\text{IRQ}}$  pin will go low and a one will appear in the IRQF bit. A read of Register C will clear AF.

**UF** – The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the  $\overline{\text{IRQ}}$  pin. UF is cleared by reading Register C.

**BIT 0 THROUGH BIT 3** – These are unused bits of the status Register C. These bits always read zero and cannot be written.

## REGISTER D

MSB				LSB			
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

**VRT** – The Valid RAM and Time (VRT) bit indicates the condition of the battery connected to the  $V_{\text{BAT}}$  pin or the battery connected to  $V_{\text{BAUX}}$ , whichever is at a higher voltage. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

**BIT 6 THROUGH BIT 0** – The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

## EXTENDED FUNCTIONS

The extended functions provided by the DS1689/DS1693 that are new to the RAMified RTC family are accessed via a software controlled bank switching scheme, as illustrated in Figure 4. In bank 0, the clock/calendar registers and 50 bytes of user RAM are in the same locations as for the DS1287. As a result, existing routines implemented within BIOS, DOS, or application software packages can gain access to the

DS1689/DS1693 clock registers with no changes. Also in bank 0, an extra 64 bytes of RAM are provided at addresses just above the original locations for a total of 114 directly addressable bytes of user RAM.

When bank 1 is selected, the clock/calendar registers and the original 50 bytes of user RAM still appear as bank 0. However, the Dallas registers which provide control and status for the extended functions will be accessed in place of the additional 64 bytes of user RAM. The major extended functions controlled by the Dallas registers are listed below:

1. Silicon Revision byte
2. Serial Number
3. Eight Byte Customer Specific ROM or Serial Number
4. Century counter
5. Auxiliary Battery Control/Status
6. Wake Up
7. Kickstart
8. RAM Clear Control/Status
9.  $V_{\text{CC}}$  Powered Elapsed Time Counter
10.  $V_{\text{BAT}}$  Powered Elapsed Time Counter
11. Power On Cycle Counter

The bank selection is controlled by the state of the DV0 bit in register A. To access bank 0 the DV0 bit should be written to a 0. To access bank 1, DV0 should be written to a 1. Register locations designated as reserved in the bank 1 map are reserved for future use by Dallas Semiconductor. Bits in these locations cannot be written and will return a 0 if read.

DS1689/DS1693 EXTENDED REGISTER BANK DEFINITION Figure 4

BANK 0 DV0 = 0		BANK 1 DV0 = 1	
MSB	LSB	MSB	LSB
00		00	
TIMEKEEPING AND CONTROL		TIMEKEEPING AND CONTROL	
0D		0D	
0E		0E	
50 BYTES–USER RAM		50 BYTES–USER RAM	
3F		3F	
64 BYTES–USER RAM		40	MODEL BYTE
		41	1ST BYTE SERIAL #
		42	2ND BYTE SERIAL #
		43	3RD BYTE SERIAL #
		44	4TH BYTE SERIAL #
		45	5TH BYTE SERIAL #
		46	6TH BYTE SERIAL #
		47	CRC BYTE
		48	CENTURY BYTE
		49	DATE ALARM
		4A	EXTENDED CONTROL REG 4A
		4B	EXTENDED CONTROL REG 4B
		4C	RESERVED
		4D	RESERVED
		4E	RESERVED
		4F	RESERVED
		50	RESERVED
		51	RESERVED
		52	RESERVED
		53	RESERVED
		54	V <sub>CC</sub> ELAPSED TIME COUNTER
		55	V <sub>CC</sub> ELAPSED TIME COUNTER
		56	V <sub>CC</sub> ELAPSED TIME COUNTER
		57	V <sub>CC</sub> ELAPSED TIME COUNTER
		58	V <sub>BAT</sub> ELAPSED TIME COUNTER
		59	V <sub>BAT</sub> ELAPSED TIME COUNTER
		5A	V <sub>BAT</sub> ELAPSED TIME COUNTER
		5B	V <sub>BAT</sub> ELAPSED TIME COUNTER
		5C	POWER CYCLE COUNTER
		5D	POWER CYCLE COUNTER
		5E	RESERVED
		5F	RESERVED
60	8–BYTE CUSTOMER SPECIFIC ROM OR SERIAL NUMBER		
67	RESERVED		
7F		7F	

### SILICON SERIAL NUMBER/CUSTOMER SPECIFIC ROM

A total of 128 bits are available for use as serial number/ROM. These bits may be used as a 128-bit serial number or as a unique 64-bit serial number and 64-bit customer specific serial number or ROM. The unique 64-bit serial number is located in bank 1 registers 40H–47H. This serial number is divided into three parts. The first byte in register 40H contains a model number to identify the device type and revision of the DS1689/DS1693. Registers 41H–46H contain a unique binary number. Register 47H contains a CRC byte used to validate the data in registers 40H–46H. The method used to create the CRC byte is proprietary to Dallas Semiconductor, but can be made available if required. Typical applications should consider this byte simply as part of the overall unique serial number. All 8 bytes of the serial number are read only registers.

The DS1689/DS1693 is manufactured such that no two devices will contain an identical number in locations 41H–47H. Blocks of numbers for these locations can be reserved by the customer. Contact Dallas Semiconductor for special ordering information for DS1689/DS1693 with reserved blocks of serial numbers.

As already mentioned, another 64 bits are available for use as an additional serial number or customer specific ROM. These 64 bits are located in bank 1 registers 60H–67H.

### CENTURY COUNTER

A register has been added in bank 1, location 48H, to keep track of centuries. The value is read in either binary or BCD according to the setting of the DM bit.

### AUXILIARY BATTERY

The  $V_{BAUX}$  input is provided to supply power from an auxiliary battery for the DS1689/DS1693 kickstart, wake up, and SQW output features in the absence of  $V_{CC}$ . This power source must be available in order to use these auxiliary features when no  $V_{CC}$  is applied to the device.

The Auxiliary Battery Enable (ABE; bank 1, register 04BH) bit in extended control register B is used to turn on and off the auxiliary battery for the above functions in the absence of  $V_{CC}$ . When set to a 1,  $V_{BAUX}$  battery power is enabled, and when cleared to 0,  $V_{BAUX}$  battery power is disabled to these functions.

In the DS1689/DS1693, this auxiliary battery may be used as the primary backup power source for maintaining the clock/calendar, user RAM, and extended external RAM functions. This occurs if the  $V_{BAT}$  pin is at a lower voltage than  $V_{BAUX}$ . If the DS1689 is to be backed-up using a single battery with the auxiliary features enabled, then  $V_{BAUX}$  should be used and connected to  $V_{BAT}$ . If  $V_{BAUX}$  is not to be used, it should be grounded and ABE should be cleared to 0.

### WAKE UP/KICKSTART

The DS1689/DS1693 incorporates a wake up feature which can power the system on at a pre-determined date through activation of the  $\overline{PWR}$  output pin. In addition, the kickstart feature can allow the system to be powered up in response to a low going transition on the KS pin, without operating voltage applied to the  $V_{CC}$  pin. As a result, system power may be applied upon such events as a key closure, or modem ring detect signal. In order to use either the wake up or the kickstart features, the DS1689/DS1693 must have an auxiliary battery connected to the  $V_{BAUX}$  pin and the oscillator must be running and the countdown chain must not be in reset (Register A DV2, DV1, DV0 = 01X). If DV2, DV1, and DV0 are not in this required state, the  $\overline{PWR}$  pin will not be driven low in response to a kickstart or wakeup condition, while in battery-backed mode.

The wake up feature is controlled through the Wake up Interrupt Enable bit in extended control register B (WIE, bank 1, 04BH). Setting WIE to 1 enables the wake up feature, clearing WIE to 0 disables it. Similarly, the kickstart feature is controlled through the Kickstart Interrupt Enable bit in extended control register B (KSE, bank 1, 04BH).

A wake up sequence will occur as follows: When wake up is enabled via  $WIE = 1$  while the system is powered down (no  $V_{CC}$  voltage), the clock/calendar will monitor the current date for a match condition with the date alarm register (bank 1, register 049H). In conjunction with the date alarm register, the hours, minutes, and seconds alarm bytes in the clock/calendar register map (bank 0, registers 05H, 03H, and 01H) are also monitored. As a result, a wake up will occur at the date and time specified by the date, hours, minutes, and seconds alarm register values. This additional alarm will occur regardless of the programming of the AIE bit (bank 0, register B, 0BH). When the match condition occurs, the  $\overline{PWR}$  pin will automatically be driven low. This output can be used to turn on the main system power supply

which provides  $V_{CC}$  voltage to the DS1689/DS1693 as well as the other major components in the system. Also at this time, the Wake Up flag (WF, bank 1, register 04AH) will be set, indicating that a wake up condition has occurred.

A kickstart sequence will occur when kickstarting is enabled via  $KSE = 1$ . While the system is powered down, the  $\overline{KS}$  input pin will be monitored for a low going transition of minimum pulse width  $t_{KSPW}$ . When such a transition is detected, the  $\overline{PWR}$  line will be pulled low, as it is for a wake up condition. Also at this time, the Kickstart Flag (KF, bank 1, register 04AH) will be set, indicating that a kickstart condition has occurred.

The timing associated with both the wake up and kickstarting sequences is illustrated in the Wake Up / Kickstart Timing Diagram in the Electrical Specifications section of this data sheet. The timing associated with these functions is divided into 5 intervals, labeled 1-5 on the diagram.

The occurrence of either a kickstart or wake up condition will cause the  $\overline{PWR}$  pin to be driven low, as described above. During interval 1, if the supply voltage on the DS1689/DS1693  $V_{CC}$  pin rises above the 3 volt power fail level before the power on timeout period ( $t_{POTO}$ ) expires, then  $\overline{PWR}$  will remain at the active low level. If  $V_{CC}$  does not rise above the 3 volt power fail voltage in this time, then the  $\overline{PWR}$  output pin will be turned off and will return to its high impedance level. In this event, the  $\overline{IRQ}$  pin will also remain tri-stated. The interrupt flag bit (either WF or KF) associated with the attempted power on sequence will remain set until cleared by software during a subsequent system power on.

If  $V_{CC}$  is applied within the timeout period, then the system power on sequence will continue as shown in intervals 2–5 in the timing diagram. During interval 2,  $\overline{PWR}$  will remain active and  $\overline{IRQ}$  will be driven to its active low level, indicating that either WF or KF was set in initiating the power on. In the diagram  $\overline{KS}$  is assumed to be pulled up to the  $V_{BAUX}$  supply. Also at this time, the PAB bit will be automatically cleared to 0 in response to a successful power on. The  $\overline{PWR}$  line will remain active as long as the PAB remains cleared to 0.

At the beginning of interval 3, the system processor has begun code execution and clears the interrupt condition of WF and/or KF by writing zeroes to both of these control bits. As long as no other interrupt within the DS1689/DS1693 is pending, the  $\overline{IRQ}$  line will be taken inactive once these bits are reset. Execution of the application software may proceed. During this time, both the wake up and kickstart functions may be used to generate status and interrupts. WF will be set in response to a date, hours, and minutes match condition. KF will be set in response to a low going transition on  $\overline{KS}$ . If the associated interrupt enable bit is set (WIE and/or KSE) then the  $\overline{IRQ}$  line will driven active low in response to enabled event. In addition, the other possible interrupt sources within the DS1689/DS1693 may cause  $\overline{IRQ}$  to be driven low. While system power is applied, the on chip logic will always attempt to drive the  $\overline{PWR}$  pin active in response to the enabled kickstart or wake up condition. This is true even if  $\overline{PWR}$  was previously inactive as the result of power being applied by some means other than wake up or kickstart.

The system may be powered down under software control by setting the PAB bit to a logic 1. This causes the open-drain  $\overline{PWR}$  pin to be placed in a high impedance state, as shown at the beginning of interval 4 in the timing diagram. As  $V_{CC}$  voltage decays, the  $\overline{IRQ}$  output pin will be placed in a high impedance state when  $V_{CC}$  goes below  $V_{PF}$ . If the system is to be again powered on in response to a wake up or kickstart, then the both the WF and KF flags should be cleared and WIE and/or KSE should be enabled prior to setting the PAB bit.

During interval 5, the system is fully powered down. Battery backup of the clock calendar and nonvolatile RAM is in effect,  $\overline{PWR}$  and  $\overline{IRQ}$  are tri-stated, and monitoring of wake up and kickstart takes place.

#### RAM CLEAR

The DS1689/DS1693 provides a RAM clear function for the 114 bytes of user RAM. When enabled, this function can be performed regardless of the condition of the  $V_{CC}$  pin.

The RAM clear function is enabled or disabled via the RAM Clear Enable bit (RCE; bank 1, register 04BH). When this bit is set to a logic 1, the 114 bytes of user RAM will be cleared (all bits set to 1) when an active low transition is sensed on the  $\overline{\text{RCLR}}$  pin. This action will have no effect on either the clock/calendar settings or upon the contents of the external extended RAM. The RAM clear Flag (RF, bank 1, register 04BH) will be set when the RAM clear operation has been completed. If  $V_{\text{CC}}$  is present at the time of the RAM clear and  $\text{RIE}=1$ , the  $\overline{\text{IRQ}}$  line will also be driven low upon completion. The interrupt condition can be cleared by writing a zero to the RF bit. The  $\overline{\text{IRQ}}$  line will then return to its inactive high level provided there are no other pending interrupts. Once the  $\overline{\text{RCLR}}$  pin is activated, all read/write accesses are locked out for a minimum recover time, specified as  $t_{\text{REC}}$  in the Electrical Characteristics section.

When RCE is cleared to zero, the RAM clear function is disabled. The state of the  $\overline{\text{RCLR}}$  pin will have no effect on the contents of the user RAM, and transitions on the  $\overline{\text{RCLR}}$  pin have no effect on RF.

### EXTENDED CONTROL REGISTERS

Two extended control registers are provided to supply controls and status information for the extended features offered by the DS1689/DS1693. These are designated as extended control registers A and B and are located in register bank 1, locations 04AH and 04BH, respectively. The functions of the bits within these registers are described as follows.

#### EXTENDED CONTROL REGISTER 4A

MSB				LSB			
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT2	INCR	*	*	PAB	RF	WF	KF

**VRT2** – This status bit gives the condition of the auxiliary battery. It is set to a logic 1 condition when the external lithium battery is connected to the  $V_{\text{BAUX}}$ . If this bit is read as a logic 0, the external battery should be replaced.

**INCR** – Increment in Progress status bit. This bit is set to a 1 when an increment to the time/date registers is in progress and the alarm checks are being made. INCR will be set to a 1 at 122  $\mu\text{s}$  before the update cycle starts and will be cleared to 0 at the end of each update cycle.

**PAB** – Power Active Bar control bit. When this bit is 0, the  $\overline{\text{PWR}}$  pin is in the active low state. This bit can be written to a logic 1 or 0 by the user. If either  $\text{WF AND WIE} = 1$  OR  $\text{KF AND KSE} = 1$ , the PAB bit will be cleared to 0.

**RF** – Ram Clear Flag. This bit will be set to a logic 1 when a high to low transition occurs on the  $\overline{\text{RCLR}}$  input if  $\text{RCE}=1$ . The RF bit is cleared by writing it to a logic 0. This bit can also be written to a logic 1 to force an interrupt condition.

**WF** – Wake up Alarm Flag – This bit is set to 1 when a wake up alarm condition occurs or when the user writes it to a 1. WF is cleared by writing it to a 0.

**KF** – Kickstart Flag – This bit is set to a 1 when a kickstart condition occurs or when the user writes it to a 1. This bit is cleared by writing it to a logic 0.

#### EXTENDED CONTROL REGISTER 4B

MSB				LSB			
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ABE	E32K	CS	RCE	PRS	RIE	WIE	KSE

**ABE** – Auxiliary Battery Enable. This bit when written to a logic 1 will enable the  $V_{\text{BAUX}}$  pin for extended functions.

**E32K** – Enable 32,768 output. This bit when written to a logic 1 will enable the 32,768 Hz oscillator frequency to be output on the SQW pin provided  $\text{SQWE}=1$ .

**CS** – Crystal Select Bit. When CS is set to a 0, the oscillator is configured for operation with a crystal that has a 6 pF specified load capacitance. When  $\text{CS}=1$ , the oscillator is configured for a 12.5 pF crystal.

**RCE** – RAM Clear Enable bit. When set to a 1, this bit enables a low level on pin 4 ( $\overline{\text{RCLR}}$ ) to clear all 114 bytes of user RAM. When  $\text{RCE} = 0$ , the RAM clear function is disabled.

**PRS** – PAB Reset Select Bit. When set to a 0 the  $\overline{\text{PWR}}$  pin will be set hi-Z when the DS1689 goes into power fail. When set to a 1, the  $\overline{\text{PWR}}$  pin will remain active upon entering power fail.

**RIE** – Ram Clear Interrupt Enable. When RIE is set to a 1, the  $\overline{\text{IRQ}}$  pin will be driven low when a RAM clear function is completed.

**WIE** – Wake Up Alarm Interrupt Enable. When  $V_{\text{CC}}$  voltage is absent and WIE is set to a 1, the  $\overline{\text{PWR}}$  pin will be driven active low when a wake up condition occurs, causing the WF bit to be set to 1. When  $V_{\text{CC}}$  is then applied, the  $\overline{\text{IRQ}}$  pin will also be driven low. If WIE is set while system power is applied, both  $\overline{\text{IRQ}}$  and  $\overline{\text{PWR}}$  will be driven low in response to WF being set to 1. When WIE is cleared to a 0, the WF bit will have no effect on the  $\overline{\text{PWR}}$  or  $\overline{\text{IRQ}}$  pins.

**KSE** – Kickstart Interrupt Enable. When  $V_{\text{CC}}$  voltage is absent and KSE is set to a 1, the  $\overline{\text{PWR}}$  pin will be driven active low when a kickstart condition occurs ( $\overline{\text{KS}}$  pulsed low), causing the KF bit to be set to 1. When  $V_{\text{CC}}$  is then applied, the  $\overline{\text{IRQ}}$  pin will also be driven low. If KSE is set to 1 while system power is applied, both  $\overline{\text{IRQ}}$  and  $\overline{\text{PWR}}$  will be driven low in response to KF being set to 1. When KSE is cleared to a 0, the KF bit will have no effect on the  $\overline{\text{PWR}}$  or  $\overline{\text{IRQ}}$  pins.

\* Reserved bits. These bits are reserved for future use by Dallas Semiconductor. They can be read and written, but have no effect on operation.

### ELAPSED TIME COUNTERS

The DS1689/DS1693 has two 32 bit elapsed time counters, which reside in bank 1 of the RTC registers. To access these counters the DV0 bit in register A must first be set to a logical 1.

The  $V_{\text{CC}}$  powered elapsed time counter resides in register 54H through 57H. The LSB of this counter resides in register 54 and the MSB is in 57H. The  $V_{\text{CC}}$  powered

elapsed time counter runs only while the  $V_{\text{CCI}}$  input is within nominal limits. The elapsed time counter is a binary counter that records the number of seconds that have elapsed. The counter can be read or written at the users discretion. The  $V_{\text{BAT}}$  powered elapsed time counter resides in register 58H through 5BH. The LSB of this counter resides in register 58 and the MSB is in 5BH.

The  $V_{\text{BAT}}$  powered elapsed time counter runs continually as long as the  $V_{\text{BAT}}$  or  $V_{\text{BAUX}}$  pin is within nominal limits regardless of the condition of  $V_{\text{CCI}}$ . The number of seconds that have elapsed are recorded in a binary counter and the counter may be read or written at the user's discretion.

In a typical application the  $V_{\text{BAT}}$  powered elapsed time counter can be used to record the length of time that has elapsed from which the equipment which contains the device was first put into service. The  $V_{\text{CC}}$  powered counter can then be used to record the length of time that  $V_{\text{CC}}$  power is applied. These functions can be particularly useful for warranty and maintenance information. In addition, battery life can be predicted based on known loading factors. However, it is worth noting that a properly selected battery should power the DS1689/DS1693 and external RAM for the useful life of most equipment.

### POWER CYCLE COUNTER

The DS1689/DS1693 has a 16 bit power cycle counter that resides in register 5C and 5D of bank 1. The LSB of this counter resides in 5C and the MSB is in 5D. This binary counter is incremented by 1 count each time  $V_{\text{CCI}}$  power is applied within nominal limits. This counter can be read or written at the user's discretion.

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature DS1689 and DS1689S	-40°C to +85°C
Operating Temperature DS1693	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds (See Note 18)

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage 5 Volt Operation	V <sub>CCI</sub>	4.5	5.0	5.5	V	1
Power Supply Voltage 3 Volt Operation	V <sub>CCI</sub>	2.7	3.0	4.0	V	1
Input Logic 1	V <sub>IH</sub>	2.2		V <sub>CC</sub> +0.3	V	1
Input Logic 0	V <sub>IL</sub>	-0.3		0.6	V	1
Battery Voltage	V <sub>BAT</sub>	2.5		3.7	V	1
Auxiliary Battery Voltage	V <sub>BAUX</sub>	2.5		3.7	V	1

**DC ELECTRICAL CHARACTERISTICS**(0°C to 70°C; V<sub>CC</sub>=4.5V to 5.5 V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V <sub>CC</sub> Power Supply Current	I <sub>CC1</sub>		7	15	mA	2, 3
CMOS Standby Current (CS=V <sub>CC</sub> -0.2V)	I <sub>CC2</sub>		1	3	mA	2, 3
Input Leakage Current (any input)	I <sub>IL</sub>	-1		+1	μA	
CE <sub>I</sub> Input Leakage	I <sub>CEI</sub>	-200		+1	μA	15
PSEL Input Leakage	I <sub>PSEL</sub>	-1		+200	μA	16
Output Leakage Current	I <sub>OL</sub>	-1		+1	μA	8
Output Logic 1 Voltage (I <sub>OUT</sub> = -1.0 mA)	V <sub>OH</sub>	2.4			V	
Output Logic 0 Voltage (I <sub>OUT</sub> = +2.1 mA)	V <sub>OL</sub>			0.4	V	
Output Voltage	V <sub>CCO1</sub>	V <sub>CC</sub> -0.3			V	4
Output Current	I <sub>CCO1</sub>			85	mA	4
Power Fail Trip Point	V <sub>PF</sub>	4.25	4.37	4.5	V	5
Battery Switch Voltage	V <sub>SW</sub>		V <sub>BAT</sub> , V <sub>BAUX</sub>		V	
Output Voltage	V <sub>CCO2</sub>	V <sub>BAT</sub> -0.3			V	6

**DC ELECTRICAL CHARACTERISTICS (cont'd)** (0°C to 70°C;  $V_{CC}=4.5V$  to 5.5 V)

Output Current	$I_{CCO2}$			100	$\mu A$	6
Battery Leakage OSC ON	$I_{BAT1}$		500	1000	nA	
Battery Leakage OSC OFF	$I_{BAT2}$		50	150	nA	17
I/O Leakage	$I_{LO}$	-1		+1	$\mu A$	7
PWR Output @ 0.4V	$I_{OLPWR}$			10.0	mA	1
$\overline{CEI}$ to $\overline{CEO}$ Impedance	$Z_{CE}$			60	$\Omega$	12

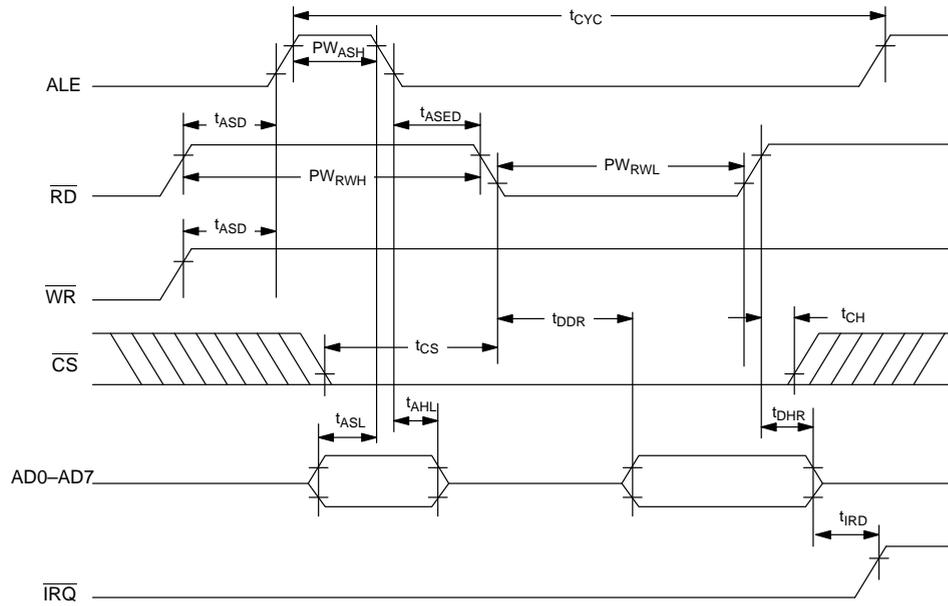
**DC ELECTRICAL CHARACTERISTICS** (0°C to 70°C;  $V_{CC}=2.7V$  to 4.0 V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average $V_{CC}$ Power Supply Current	$I_{CC1}$		5	10	mA	2, 3
CMOS Standby Current ( $\overline{CS}=V_{CC}-0.2V$ )	$I_{CC2}$		0.5	2	mA	2, 3
Input Leakage Current (any input)	$I_{IL}$	-1		+1	$\mu A$	
$\overline{CEI}$ Input Leakage	$\overline{I_{CEI}}$	-160		+1	$\mu A$	15
PSEL Input Leakage	$I_{PSEL}$	+1		-160	$\mu A$	16
Output Leakage Current	$I_{OL}$	+160		-1	$\mu A$	8
Output Logic 1 Voltage @ 0.4 mA	$V_{OH}$	2.4			V	
Output Logic 0 Voltage @ 0.8 mA	$V_{OL}$			0.4	V	
Output Voltage	$V_{CCO1}$	$V_{CC}-0.3$			V	4
Output Current	$I_{CCO1}$			50	mA	4
Power Fail Trip Point	$V_{PF}$	2.5	2.6	2.7	V	5
Output Voltage	$V_{CCO2}$	$V_{BAT}-0.3$			V	6
Output Current	$I_{CCO2}$			100	$\mu A$	6
Battery Leakage OSC ON	$I_{BAT1}$		500	1000	nA	
Battery Leakage OSC OFF	$I_{BAT2}$		50	150	nA	17
I/O Leakage	$I_{LO}$	-1		+1	$\mu A$	7
PWR Output @ 0.4V	$I_{OLPWR}$			4	mA	1
$\overline{CEI}$ to $\overline{CEO}$ Impedance	$Z_{CE}$			120	$\Omega$	12

**RTC AC TIMING CHARACTERISTICS**(0°C to 70°C;  $V_{CC} = 2.7V$  to 4.0V)

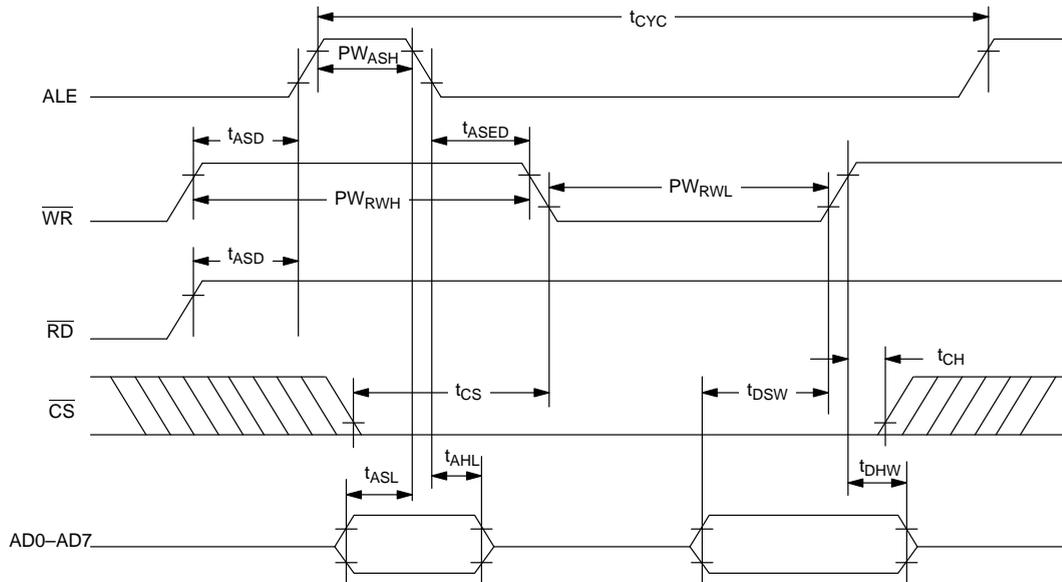
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	$t_{CYC}$	915		DC	ns	
Pulse Width, $\overline{RD}/\overline{WR}$ Low	$PW_{RWL}$	375			ns	
Pulse Width, $\overline{RD}/\overline{WR}$ High	$PW_{RWH}$	450			ns	
Input Rise and Fall Time	$t_R, t_F$			30	ns	
Chip Select Setup Time Before $\overline{WR}$ , or $\overline{RD}$	$t_{CS}$	75			ns	
Chip Select Hold Time	$t_{CH}$	0			ns	
Read Data Hold Time	$t_{DHR}$	10		120	ns	
Write Data Hold Time	$t_{DHW}$	0			ns	
Muxed Address Valid Time to ALE Fall	$t_{ASL}$	90			ns	
Muxed Address Hold Time from ALE fall	$t_{AHL}$	30			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	$t_{ASD}$	30			ns	
Pulse Width ALE High	$PW_{ASH}$	180			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	$t_{ASED}$	120			ns	
Output Data Delay Time from $\overline{RD}$	$t_{DDR}$	20		370	ns	9
Data Setup Time	$t_{DSW}$	180			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	$t_{IRD}$			2	$\mu s$	
$\overline{CEI}$ to $\overline{CEO}$ Delay	$t_{CED}$			20	ns	

## DS1689/DS1693 BUS TIMING FOR READ CYCLE TO RTC

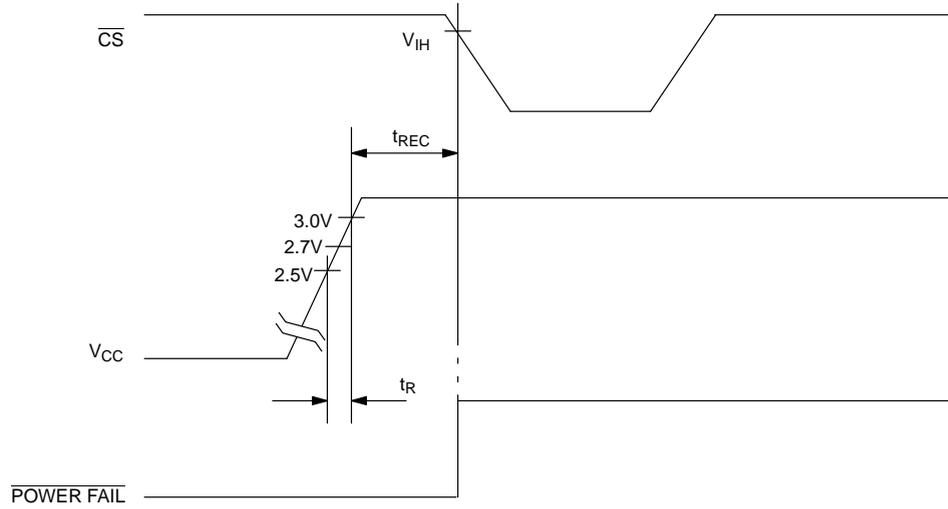


**RTC AC TIMING CHARACTERISTICS**(0°C to 70°C;  $V_{CC} = 5.0V \pm 10\%$ )

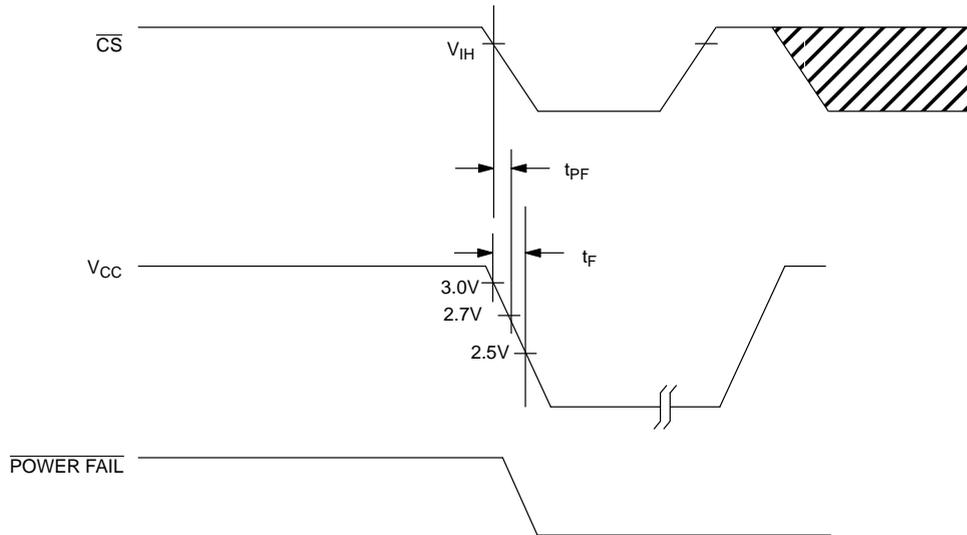
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	$t_{CYC}$	305		DC	ns	
Pulse Width, $\overline{RD}/\overline{WR}$ Low	$PW_{RWL}$	125			ns	
Pulse Width, $\overline{RD}/\overline{WR}$ High	$PW_{RWH}$	150			ns	
Input Rise and Fall Time	$t_R, t_F$			30	ns	
Chip Select Setup Time Before $\overline{WR}$ , or $\overline{RD}$	$t_{CS}$	20			ns	
Chip Select Hold Time	$t_{CH}$	0			ns	
Read Data Hold Time	$t_{DHR}$	10		80	ns	
Write Data Hold Time	$t_{DHW}$	0			ns	
Muxed Address Valid Time to ALE Fall	$t_{ASL}$	30			ns	
Muxed Address Hold Time from ALE fall	$t_{AHL}$	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	$t_{ASD}$	25			ns	
Pulse Width ALE High	$PW_{ASH}$	60			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	$t_{ASED}$	40			ns	
Output Data Delay Time from $\overline{RD}$	$t_{DDR}$	20		120	ns	9
Data Setup Time	$t_{DSW}$	100			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	$t_{IRD}$			2	$\mu s$	
CEI to CEO Delay	$t_{CED}$			10	ns	

**DS1689/DS1693 BUS TIMING FOR WRITE CYCLE TO RTC AND RTC REGISTERS**

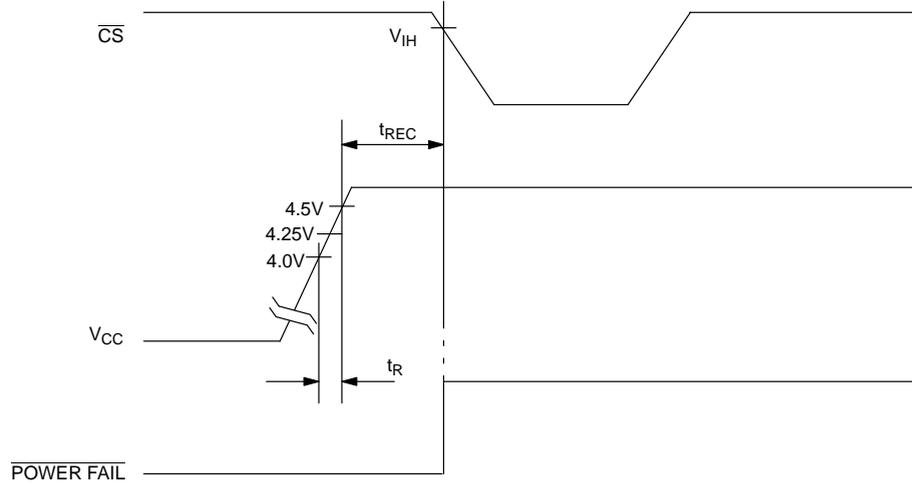
**POWER-UP CONDITION 3 VOLT OPERATION**



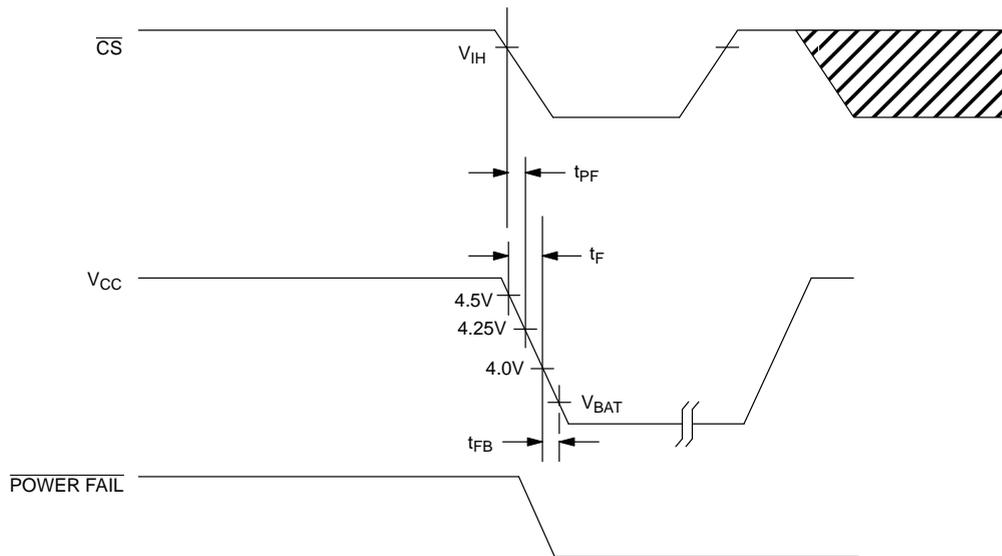
**POWER-DOWN CONDITION 3 VOLT OPERATION**



**POWER-UP CONDITION 5.0 VOLT OPERATION**



**POWER-DOWN CONDITION 5.0 VOLT OPERATION**



**POWER-UP POWER-DOWN TIMING 5 VOLT OPERATION** $(t_A = 25^\circ\text{C})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{\text{CS}}$ High to Power Fail	$t_{\text{PF}}$			0	ns	
Recovery at Power Up	$t_{\text{REC}}$		150		ms	
$V_{\text{CC}}$ Slew Rate Power-down	$t_{\text{F}}$ $4.0 \leq V_{\text{CC}} \leq 4.5\text{V}$	300			$\mu\text{s}$	
$V_{\text{CC}}$ Slew Rate Power-down	$t_{\text{FB}}$ $3.0 \leq V_{\text{CC}} \leq 4.0\text{V}$	10			$\mu\text{s}$	
$V_{\text{CC}}$ Slew Rate Power-up	$t_{\text{R}}$ $4.5\text{V} \geq V_{\text{CC}} \geq 4.0\text{V}$	0			$\mu\text{s}$	
Expected Data Retention	$t_{\text{DR}}$	10			years	13, 14

**POWER-UP POWER-DOWN TIMING 3 VOLT OPERATION** $(t_A = 25^\circ\text{C})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{\text{CS}}$ High to Power Fail	$t_{\text{PF}}$			0	ns	
Recovery at Power-up	$t_{\text{REC}}$		150		ms	
$V_{\text{CC}}$ Slew Rate Power-down	$t_{\text{F}}$ $2.5 \leq V_{\text{CC}} \leq 3.0\text{V}$	300			$\mu\text{s}$	
$V_{\text{CC}}$ Slew Rate Power-up	$t_{\text{R}}$ $3.0\text{V} \geq V_{\text{CC}} \geq 2.5\text{V}$	0			$\mu\text{s}$	
Expected Data Retention	$t_{\text{DR}}$	10			years	13, 14

**WARNING:**

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

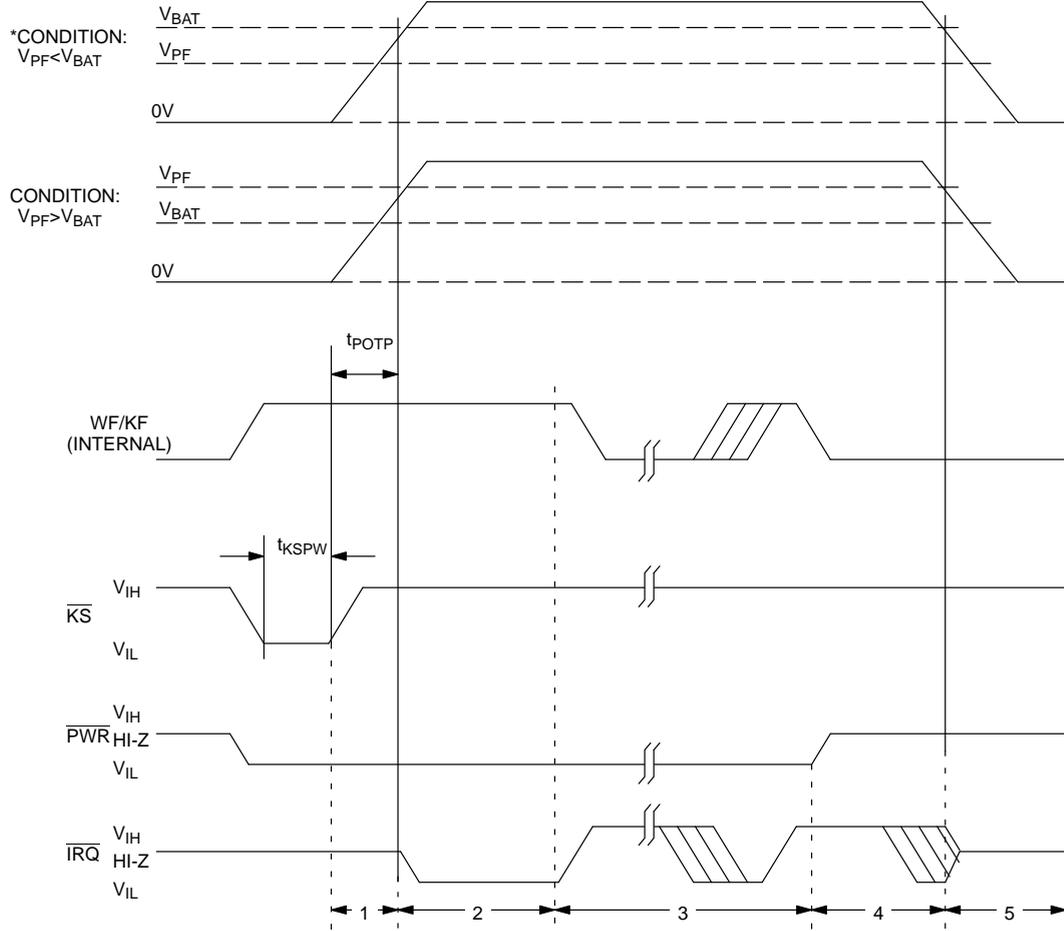
**CAPACITANCE** $(t_A = 25^\circ\text{C})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	$C_{\text{IN}}$			12	pF	
Output Capacitance	$C_{\text{OUT}}$			12	pF	

**WAKE UP/KICKSTART TIMING** $(t_A = 25^\circ\text{C})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Kickstart Input Pulse Width	$t_{\text{KSPW}}$	2			$\mu\text{s}$	
Wake up/Kickstart Power On Timeout	$t_{\text{POTO}}$	2			seconds	10

**WAKE UP/KICKSTART TIMING**



**NOTE:**

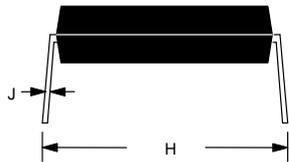
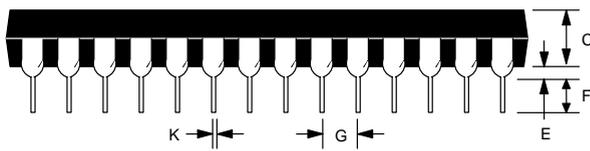
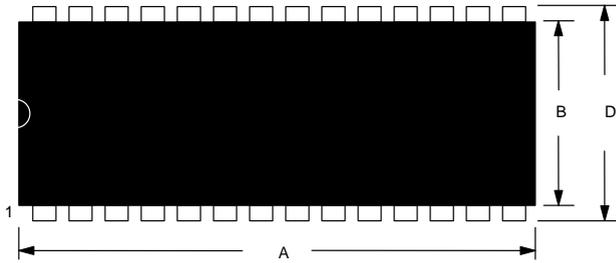
Time intervals shown above are referenced in Wake up/Kickstart section.

\* This condition can occur when the device is operated in 3 volt mode.

**NOTES:**

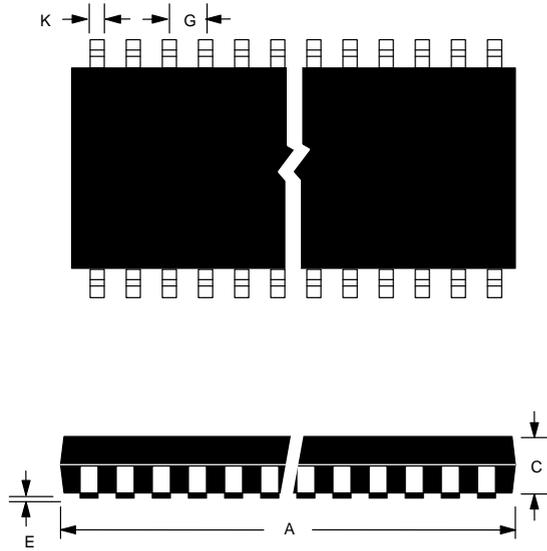
1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Value for voltage and currents is from the  $V_{CCI}$  input pin to the  $V_{CCO}$  pin.
5. Write protection trip point occurs during power fail prior to switchover from  $V_{CC}$  to  $V_{BAT}$ .
6. Value for voltage and currents is from the  $V_{BAT}$  input pin to the  $V_{CCO}$  pin.
7. Applies to the AD0–AD7 pins, and the SQW pin when each is in a high impedance state.
8. The  $\overline{IRQ}$  pin is open drain.
9. Measured with a load of 50 pF + 1 TTL gate.
10. Wakeup kickstart timeout generated only when the oscillator is enabled and the countdown chain is not reset.
11.  $V_{SW}$  is determined by the larger of  $V_{BAT}$  and  $V_{BAUX}$ .
12.  $Z_{CE}$  is an average input to output impedance as the input is swept from GND to  $V_{CCI}$  and less than 4 mA is forced through  $Z_{CE}$ .
13. The DS1693 will keep time to an accuracy of  $\pm 1$  minute per month during data retention time for the period of  $t_{DR}$ .
14.  $t_{DR}$  is the amount of time that the internal battery can power the internal oscillator and internal registers of the DS1693. As such,  $t_{DR}$  is specified with  $V_{CCO}$  floating. If  $V_{CCO}$  is powering an external SRAM, an auxiliary battery must be connected to the  $V_{BAUX}$  pin. The auxiliary battery should be sized such that it can power the external SRAM for the  $t_{DR}$  period.
15. The  $\overline{CEI}$  pin has an internal pull-up of 60 K $\Omega$ .
16. The PSEL pin has an internal pull-down of 60 K $\Omega$ .
17. For industrial grade parts,  $I_{BAT}$  (with OSC off) limit increases to 250 nA.
18. Real-Time Clock Modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used.

**DS1689 28-PIN DIP**



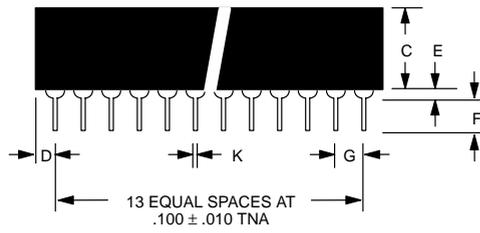
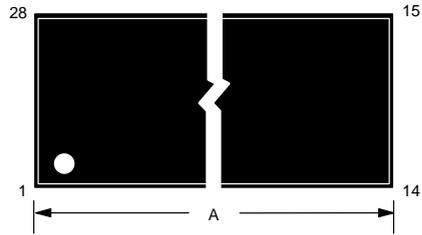
PKG	28-PIN	
	MIN	MAX
A IN.	1.445	1.470
MM	36.70	37.34
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.56

**DS1689S 28-PIN SOIC**

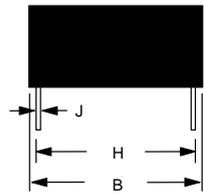


PKG	28-PIN	
DIM	MIN	MAX
A IN.	0.706	0.728
MM	17.93	18.49
B IN.	0.338	0.350
MM	8.58	8.89
C IN.	0.086	0.110
MM	2.18	2.79
D IN.	0.020	0.050
MM	0.58	1.27
E IN.	0.002	0.014
MM	0.05	0.36
F IN.	0.090	0.124
MM	2.29	3.15
G IN.	0.050	BSC
MM	1.27	
H IN.	0.460	0.480
MM	11.68	12.19
J IN.	0.006	0.013
MM	0.15	0.33
K IN.	0.014	0.020
MM	0.36	0.51

**DS1693 28-PIN 740 MIL MODULE**



PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.740
MM	17.65	18.80
C IN.	0.350	0.375
MM	8.89	9.52
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53



NOTE: PINS 2, 3, 19 AND 23 ARE MISSING BY DESIGN.