Variable Delay Motherboard Clock Buffer

Features

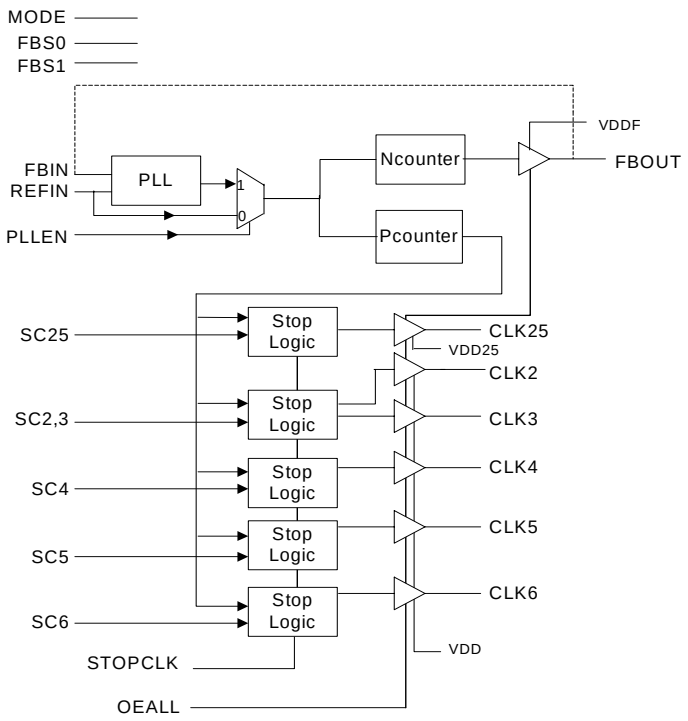
- **Output phase relationship is precisely controllable with respect to input clock via a dedicated external feedback path**
- **Two-kV ESD protected**
- **Six low-skew clocks generated**
- **One 2.5V output clock**
- **Outputs are individually enabled**
- **Output frequencies from 30 to 120 MHz**
- **3.3V power supply**
- **Synchronous output enable and disable control**
- **45–55% output duty cycle**
- **±100 ps cycle-to-cycle jitter**
- **32-lead TQFP package**
- **Pin-compatible with MPC932P**

Table 1. Feedback Scale Select Codes

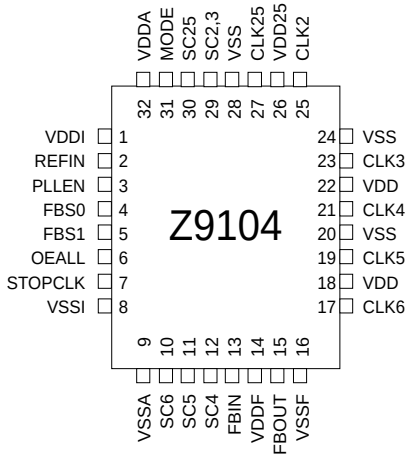
Mode	FBS1	FBS0	Pcounter	Ncounter	MF[1]
0	0	0	³ 4	³ 8	2.0
0	0	1	³ 4	³ 10	2.5
0	1	0	³ 4	³ 12	3.0
0	1	1	³ 8	³ 12	1.5
1	0	0	³ 4	³ 4	1.0
1	0	1	³ 4	³ 5	1.25
1	1	0	³ 4	³ 6	1.5
1	1	1	³ 8	³ 8	1.0

Note:
1. Multiplication Factor – The multiplication factor for these configurations is the output frequency with respect to REFIN (FOUT = FIN × multiplication factor).

Block Diagram



Pin Configuration



Pin Description

Pin	Name	PWR	I/O[2]	Description
2	REFIN	VDDI	I	External reference clock input pin.
3	PLLEN	VDD	I PU	When LOW, Ref input bypass PLL. It is intended for static testing at the part's internal logic.
4, 5	FBS(0:1)	VDD	I PU	Feedback selection pins. These input pins control the internal routing of the feedback output clock that produce the multiplier values listed in the "Feedback Scale Select Code" table on page 1.
31	MODE	VDD	I PD	Combined with the FBS pins, this pin determines the output clocks frequency with respect to the REFIN pin. See table on page 1 for functionality.
6	OEALL	VDD	I PU	Output Enable for all CLK output clocks. When at a logic LOW level, all outputs are driven to a three-state.
7	STOPCLK	VDD	I PU	Stop Clock for all CLK output clocks. When at a logic LOW CLK (2:6) and CLK25 are driven to a logic LOW level synchronously with their next occurring HIGH to LOW transition. This signal does NOT effect the FBOUT clock.
15	FBOUT	VDDF	O	Clock source that is used in the device's external feedback loop. This pin is connected to the device's FBIN pin either directly or through an external delay circuit.
27	CLK25	VDD25	O	2.5V output clock copy of CLK(2:6).
25, 23, 21, 19, 17	CLK(2:6)	VDD	O	These output clocks are the synthesized product of the REFIN clock and the selections programmed on the FB0, FB1 and MODE pins.
20, 24, 28	VSS		P	Ground pins for the device.
18, 22	VDD		P	3.3V power supply pins for clock buffer circuit.
14	VDDF		P	3.3V power supply pins for the FBOUT clock output buffers.
30	SC25	VDD	I PU	Synchronous output enable control pin for CLK25.[3]
29	SC2:3	VDD	I PU	Synchronous output enable control pin for CLK2 and CLK3 pins.[3]
12	SC4	VDD	I PU	Synchronous output enable control pin for CLK4 pins.[3]
11	SC5	VDD	I PU	Synchronous output enable control pin for CLK5 pins.[3]
10	SC6	VDD	I PU	Synchronous output enable control pin for CLK6 pins.[3]
26	VDD25		P	2.5V power supply pin for the CLK25 clock output buffers.
32	VDDA		P	Analog power. See recommended circuitry later in this data sheet.
16	VSSF		P	Ground supply for pin 15 (FBOUT) buffer.
9	VSSA		P	Ground power connection for analog circuitry.
8	VSSI		P	Ground power connection for input clock circuitry.
1	VDDI		P	3.3V power connection for input clock circuitry.

Notes:

2. Pins with "PU" or "PD" listed in the Type column indicate that these pins have internal pull-up or pull down resistors. These resistors ensure that the device will sense a logic 1 (HIGH) or logic 0 (LOW) condition respectively when the device is powered up and no electrical connection is made to these pins.
3. All synchronous output enables, when driven to a logic LOW level, will cause their associated output clocks to transition to a logic LOW level and remain there. Likewise, they will cause their associated output clocks to begin running when driven to a logic HIGH level. This enabling and disabling action will produce no runt (short or long) clock output cycles.

Output Clock Disable and Enable Timing

When each clock enable pin (SC25 through SC6) is brought to a logic low level, its related output clock (CLK25 through CLK6) will be forced to a logic low level after one complete cycle. The enable pins are synchronized to the internal clock such that upon assertion, these signals will hold the clocks low until the beginning of a new clock period and thus avoid a runt pulse generation on the outputs.

Figure 2 shows the recommended power supply decoupling circuitry to obtain minimum device clock noise (jitter). Designs shown implements this decoupling scheme in noisy V_{DD} environments to protect the device's internal analog circuitry from digital noise generated on the main 3.3V supply. A range of 2.2 to 15 Ohms is recommended for Rs. Rs should be adjusted to the minimum value required to produce acceptable performances from the device. The ultimate limitation on the Rs maximum value is the device's minimum V_{DD} spec.

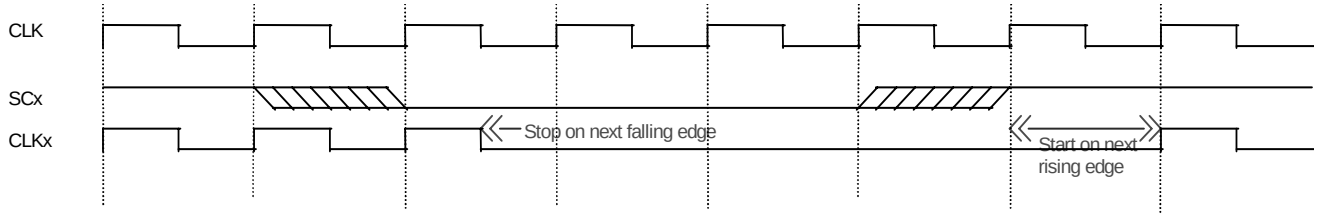


Figure 1.

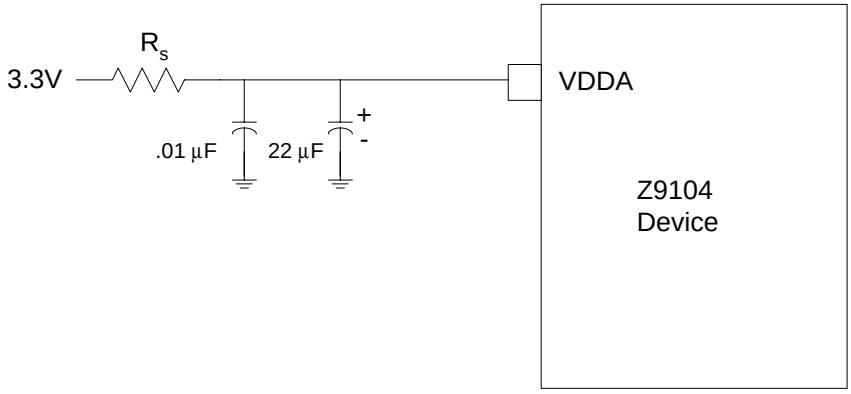


Figure 2.

Applications Examples

Table 2. Z9104 Input Reference Frequency Ranges

Mode	FBS1	FBS0	REFIN Frequency Min. (MHz)	REFIN Frequency Max. (MHz)	CLK(25:6), Output Frequency (MHz)	Example
1	0	0	50	120	1 x REFIN	REFIN = 66.7 MHz CLK* = 66.7 MHz
1	0	1	40	96	1.25 x REFIN	REFIN = 66.7 MHz CLK* = 83.3 MHz
1	1	0	33.3	80	1.5 x REFIN	REFIN = 66.7 MHz CLK* = 100 MHz
1	1	1	25	60	1 x REFIN	REFIN = 33.3 MHz CLK* = 33.3 MHz
0	0	0	25	60	2 x REFIN	REFIN = 33.3 MHz CLK* = 66.7 MHz
0	0	1	20	48	2.5 x REFIN	REFIN = 33.3 MHz CLK* = 83.3 MHz
0	1	0	16.7	40	3 X REFIN	REFIN = 33.3 MHz CLK* = 100 MHz
0	1	1	16.7	40	1.5 X REFIN	REFIN = 33.3 MHz CLK* = 50 MHz

Maximum Ratings

Voltage Relative to V_{SS}:.....–0.3V
Voltage Relative to V_{DD}: 0.3V
Storage Temperature: .....–65°C to + 150°C
Operating Temperature: .....–40°C to +85°C
Maximum Power Supply: 7V
Maximum ESD protection 2KV

This device contains circuitry to protect the inputs against damage due to up to 2,000 volt static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters: $V_{DD} = V_{DDF} = 3.3V \pm 5\%$, $V_{DD25} = 2.5V \pm 5\%$, $T_A = –40°C$ to $+85°C$

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage		V_{SS}		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
I_{IL}	Input Low Current[5]	$V_{IN} = V_{SS}$			–100	mA
I_{IH}	Input High Current[5]	$V_{IN} = V_{DD}$			+100	mA
V_{OH}	Output Voltage High for CLK(2:6)[4]	$@I_{OH}$ = –20 mA	2.4			V
VOH_{C25}	Output Voltage for High CLK25[4,6]	$@I_{OH}$ = –13 mA	1.8			V
VOL	Output Low Voltage for CLK(2:6)[4]	$@I_{OL}$ = 20mA			0.5	V
VOL_{C25}	Output Low Voltage for CLK25[4,6]	$@I_{OL}$ = 13 mA			0.5	V
I_{oz}	Three-State Leakage Current				10	mA
Cpd	Power Dissipation Capacitance	Per Output		20		pF
I_{CCQ}	Quiescent Supply Current				15	mA
I_{CC}	Maximum Core Supply Current				130	mA
I_{CCPLL}	Maximum PLL Supply Current				20	mA

Notes:
4. Z9104D outputs can drive series or parallel terminated 50W (or 50W to $V_{DD}/2$) transmission lines.
5. Inputs have pull-up and pull-down resistors, which affect the input current
6. Varies 1:1 with V_{DD25}.

AC Parameters[7]: $V_{DD} = V_{DDF} = 3.3V \pm 5\%$, $V_{DD25} = 2.5V \pm 5\%$, $T_A = -40°C$ to $+85°C$

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T_r, T_f	REFIN Rise/Fall Time	0.4 to 2.4 Volts			3.0	ns
F_{VCO}	VCO lock range		200		480	MHz
F_{max}	Maximum output frequency	Pcounter = 4			120	MHz
REFIN	Input Reference Frequency	See *Table 2*	Controlled by VCO lock range			MHz
F_{refDC}	Reference Input Duty Cycle	Measured @ 1.5V	25		75	%
T_{SkewO}	Output to Output clock skew (CLK(2:6))[8]	Measured at 1.5 Volts			300	ps
$T_{SkewO25}$	Output to Output clock skew (CLK25 to Q(2:6))[8]	Measured at 1.5 V on CLK(2:6) and at 1.25V on CLK25			600	ps
T_{pd}	REFIN to FBIN Average Delay[9,10]	F_{in} = 66.6 MHz	–150	0	+150	ps
DC	Output Duty Cycle	Measured at 1.5 V on CLK(2:6) and at 1.25V on CLK25	45	50	55	%
T_r, T_f	Output Rise/Fall Time	Measured from 0.8V to 2.0V on CLK(2:6) and from 0.8V to 1.8V on CLK25	0.1		1.2	ns
T_{en}	Output Enable Time		2.0		10	ns
T_{dis}	Output Disable Time		2.0		8.0	ns
T_{jitter}	Cycle-to-cycle jitter	Short term jitter (adjacent cycle) Select Code 100 50 MHz in/out		$\pm$100		ps
T_{lock}	Maximum PLL Lock Time				10	ms
T_{pr}	Power Up Ramp Time	Measured between 0.3V and 3.0V	250		20 ms	ns

Notes:

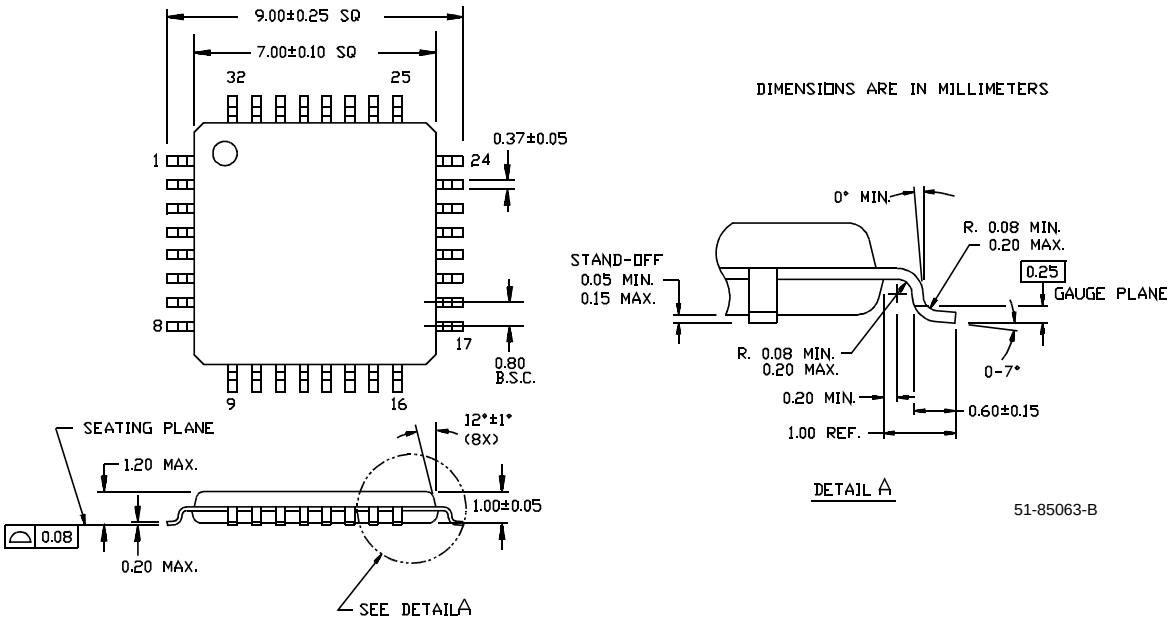
7. Parameters are guaranteed by design and characterization. Not 100% tested in production.
8. Outputs are loaded with 33 pF each.
9. REFIN rise time = FBIN rise time.
10. T_{pd} measurement uses the averaging feature of the scope to filter out the jitter component.

Ordering Information

Part Number	Package Type	Production Flow
IMIZ9104DAB	32-lead TQFP	Industrial, –40°C to +85°C
IMIZ9104DABT	32-lead TQFP–Tape and Reel	Industrial, –40°C to +85°C

Package Drawing and Dimension

32-lead Thin Plastic Quad Flatpack 7 × 7 × 1.0 mm A32



Document Title: Z9104 Variable Delay Motherboard Clock Buffer Document Number: 38-07083				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107119	06/05/01	IKA	Convert from IMI to Cypress
*A	108351	6/29/01	NDP	Change Production flow from “Commercial” to “Industrial.” Change Part Number Revision from “C” to “D.”
*B	109808	02/01/02	DSG	Convert from Word Doc to Adobe Framemaker Cypress Format Changed the Output Frequency (30 to 10 MHz) to (30 to 120 MHz)
*C	113686	05/13/02	CTK	Corrected ordering information to indicate “Industrial” range