



CYPRESS

PRELIMINARY

W219B

Frequency Generator for Integrated Core Logic with 133-MHz FSB

Features

- Maximized EMI suppression using Cypress's Spread Spectrum technology
- Low jitter and tightly controlled clock skew
- Highly integrated device providing clocks required for CPU, core logic, and SDRAM
- Two copies of CPU clock
- Nine copies of SDRAM clock
- Seven copies of PCI clock
- One copy of synchronous APIC clock
- Three copies of 66-MHz outputs
- Two copies of 48-MHz outputs
- One copy of selectable 24- or 48-MHz clock
- One copy of double strength 14.31818-MHz reference clock
- Power-down control
- SMBus interface for turning off unused clocks

Key Specifications

CPU, SDRAM Outputs Cycle-to-Cycle Jitter: 250 ps

APIC, 48-MHz, 3V66, PCI Outputs
Cycle-to-Cycle Jitter: 500 ps

CPU, 3V66 Output Skew: 175 ps

SDRAM, APIC, 48-MHz Output Skew: 250 ps

PCI Output Skew: 500 ps

CPU to SDRAM Skew (@ 133 MHz) ± 0.5 ns

CPU to SDRAM Skew (@ 100 MHz) 4.5 to 5.5 ns

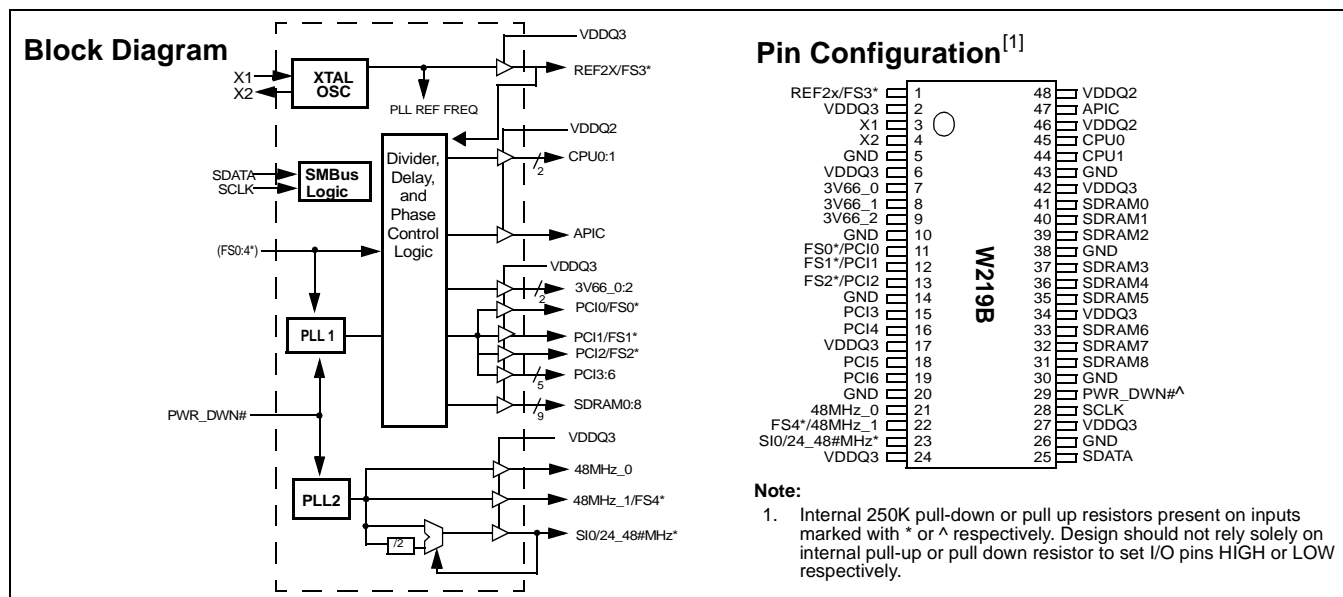
CPU to 3V66 Skew (@ 66 MHz) 7.0 to 8.0 ns

3V66 to PCI Skew (3V66 lead) 1.5 to 3.5 ns

PCI to APIC Skew ± 0.5 ns

Table 1. Frequency Selections

| FS4 | FS3 | FS2 | FS1 | FS0 | CPU | SDRAM | 3V66 | PCI | APIC | SS |
|-----|-----|-----|-----|-----|-------|-------|------|------|------|--------------|
| 0 | 0 | 0 | 0 | 0 | 75.3 | 113.0 | 75.3 | 37.6 | 18.8 | OFF |
| 0 | 0 | 0 | 0 | 1 | 95.0 | 95.0 | 63.3 | 31.6 | 15.8 | -0.6% |
| 0 | 0 | 0 | 1 | 0 | 129.0 | 129.0 | 86.0 | 43.0 | 21.5 | OFF |
| 0 | 0 | 0 | 1 | 1 | 150.0 | 113.0 | 75.3 | 37.6 | 18.8 | OFF |
| 0 | 0 | 1 | 0 | 0 | 150.0 | 150.0 | 75.0 | 37.5 | 18.7 | OFF |
| 0 | 0 | 1 | 0 | 1 | 110.0 | 110.0 | 73.0 | 36.6 | 18.3 | OFF |
| 0 | 0 | 1 | 1 | 0 | 140.0 | 140.0 | 70.0 | 35.0 | 17.5 | OFF |
| 0 | 0 | 1 | 1 | 1 | 144.0 | 108.0 | 72.0 | 36.0 | 18.0 | OFF |
| 0 | 1 | 0 | 0 | 0 | 68.3 | 102.5 | 68.3 | 34.1 | 17.0 | OFF |
| 0 | 1 | 0 | 0 | 1 | 105.0 | 105.0 | 70.0 | 35.0 | 17.5 | OFF |
| 0 | 1 | 0 | 1 | 0 | 138.0 | 138.0 | 69.0 | 34.5 | 17.0 | OFF |
| 0 | 1 | 0 | 1 | 1 | 140.0 | 105.0 | 70.0 | 35.0 | 17.5 | OFF |
| 0 | 1 | 1 | 0 | 0 | 66.8 | 100.2 | 66.8 | 33.4 | 16.7 | $\pm 0.45\%$ |
| 0 | 1 | 1 | 0 | 1 | 100.2 | 100.2 | 66.8 | 33.4 | 16.7 | $\pm 0.45\%$ |
| 0 | 1 | 1 | 1 | 0 | 133.6 | 133.6 | 66.8 | 33.4 | 16.7 | $\pm 0.45\%$ |
| 0 | 1 | 1 | 1 | 1 | 133.6 | 100.2 | 66.8 | 33.4 | 16.7 | $\pm 0.45\%$ |
| 1 | 0 | 0 | 0 | 0 | 157.3 | 118.0 | 78.6 | 39.3 | 19.6 | OFF |
| 1 | 0 | 0 | 0 | 1 | 160.0 | 120.0 | 80.0 | 40.0 | 20.0 | OFF |
| 1 | 0 | 0 | 1 | 0 | 146.6 | 110.0 | 73.3 | 36.6 | 18.3 | OFF |
| 1 | 0 | 0 | 1 | 1 | 122.0 | 91.5 | 61.0 | 30.5 | 15.2 | -0.6% |
| 1 | 0 | 1 | 0 | 0 | 127.0 | 127.0 | 84.6 | 42.3 | 21.1 | OFF |
| 1 | 0 | 1 | 0 | 1 | 122.0 | 122.0 | 81.3 | 40.6 | 20.3 | -0.6% |
| 1 | 0 | 1 | 1 | 0 | 117.0 | 117.0 | 78.0 | 39.0 | 19.5 | OFF |
| 1 | 0 | 1 | 1 | 1 | 114.0 | 114.0 | 76.0 | 38.0 | 19.0 | OFF |
| 1 | 1 | 0 | 0 | 0 | 80.0 | 120.0 | 80.0 | 40.0 | 20.0 | OFF |
| 1 | 1 | 0 | 0 | 1 | 78.0 | 117.0 | 78.0 | 39.0 | 19.5 | OFF |
| 1 | 1 | 0 | 1 | 0 | 166.0 | 124.5 | 83.0 | 41.5 | 20.7 | OFF |
| 1 | 1 | 0 | 1 | 1 | 133.6 | 133.6 | 89.0 | 44.5 | 22.2 | OFF |
| 1 | 1 | 1 | 0 | 0 | 66.6 | 100.0 | 66.6 | 33.3 | 16.6 | -0.6% |
| 1 | 1 | 1 | 0 | 1 | 100.0 | 100.0 | 66.6 | 33.3 | 16.6 | -0.6% |
| 1 | 1 | 1 | 1 | 0 | 133.3 | 133.3 | 66.6 | 33.3 | 16.6 | -0.6% |
| 1 | 1 | 1 | 1 | 1 | 133.3 | 100.0 | 66.6 | 33.3 | 16.6 | -0.6% |



Pin Definitions

| Pin Name | Pin No. | Pin Type | Pin Description |
|-------------------|--|----------|--|
| REF2x/FS3 | 1 | I/O | Reference Clock with 2x Drive/Frequency Select 3: 3.3V 14.318-MHz clock output. This pin also serves as the select strap to determine device operating frequency as described in <i>Table 1</i> . |
| X1 | 3 | I | Crystal Input: This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input. |
| X2 | 4 | I | Crystal Output: An input connection for an external 14.318-MHz crystal connection. If using an external reference, this pin must be left unconnected. |
| PCI0/FS0 | 11 | I/O | PCI Clock 0/Frequency Selection 0: 3.3V 33-MHz PCI clock outputs. This pin also serves as the select strap to determine device operating frequency as described in <i>Table 1</i> . |
| PCI1/FS1 | 12 | I/O | PCI Clock 1/Frequency Selection 1: 3.3V 33-MHz PCI clock outputs. This pin also serves as the select strap to determine device operating frequency as described in <i>Table 1</i> . |
| PCI2/FS2 | 13 | I/O | PCI Clock 2/Frequency Selection 2: 3.3V 33-MHz PCI clock outputs. This pin also serves as the select strap to determine device operating frequency as described in <i>Table 1</i> . |
| PCI3:6 | 15, 16, 18, 19 | O | PCI Clock 3 through 6: 3.3V 33-MHz PCI clock outputs. PCI0:6 can be individually turned off via SMBus interface. |
| 3V66_0:2 | 7, 8, 9 | O | 66-MHz Clock Output: 3.3V output clocks. The operating frequency is controlled by FS0:4 (see <i>Table 1</i>). |
| 48MHz_0 | 21 | O | 48-MHz Clock Output: 3.3V fixed 48-MHz, non-spread spectrum clock output. |
| 48MHz_1/ FS4 | 22 | I/O | 48-MHz Clock Output/Frequency Selection 4: 3.3V fixed 48-MHz, non-spread spectrum clock output. This pin also serves as the select strap to determine device operating frequency as described in <i>Table 1</i> . |
| SIO/ 24_48#MHz | 23 | I/O | Clock Output for Super I/O: This is the input clock for a Super I/O (SIO) device. During power-up, it also serves as a selection strap. If it is sampled HIGH, the output frequency for SIO is 24 MHz. If the input is sampled LOW, the output is 48 MHz. |
| PWR_DWN# | 29 | I | Power Down Control: LVTTTL-compatible input that places the device in power-down mode when held LOW. |
| CPU0:1 | 45, 44 | O | CPU Clock Outputs: Clock outputs for the host bus interface. Output frequencies depending on the configuration of FS0:4. Voltage swing is set by VDDQ2. |
| SDRAM0:8 | 41, 40, 39, 37, 36, 35, 33, 32, 31 | O | SDRAM Clock Outputs: 3.3V outputs for SDRAM. The operating frequency is controlled by FS0:4 (see <i>Table 1</i>). |
| APIC | 47 | O | Synchronous APIC Clock Outputs: Clock outputs running synchronous with the PCI clock outputs. Voltage swing set by VDDQ2. |
| SDATA | 25 | I/O | Data pin for SMBus circuitry. |
| SCLK | 28 | I | Clock pin for SMBus circuitry. |
| VDDQ3 | 2, 6, 17, 24, 27, 34, 42 | P | 3.3V Power Connection: Power supply for SDRAM output buffers, PCI output buffers, reference output buffers and 48-MHz output buffers. Connect to 3.3V. |
| VDDQ2 | 46, 48 | P | 2.5V Power Connection: Power supply for IOAPIC and CPU output buffers. Connect to 2.5V or 3.3V. |
| GND | 5, 10, 14, 20, 26, 30, 38, 43, | G | Ground Connections: Connect all ground pins to the common system ground plane. |

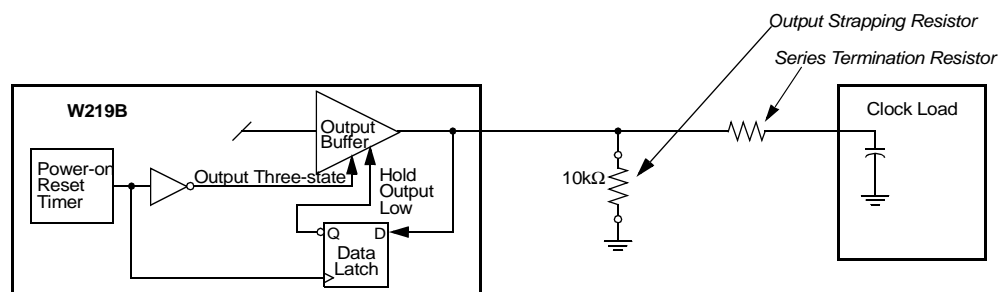


Figure 1. Input Logic Selection Through Resistor Load Option

Overview

The W219B is a highly integrated frequency timing generator, supplying all the required clock sources for an Intel® architecture platform using graphics integrated core logic.

Functional Description

I/O Pin Operation

Pin # 1, 11, 12, 13, 22, and 23 are dual-purpose I/O pins. Upon power-up the pin acts as a logic input. An external 10-kΩ strapping resistor should be used. *Figure 1* shows a suggested method for strapping resistor connections.

After 2 ms, the pin becomes an output. Assuming the power supply has stabilized by then, the specified output frequency

is delivered on the pins. If the power supply has not yet reached full value, output frequency initially may be below target but will increase to target once supply voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

Offsets Among Clock Signal Groups

Figure 2 and *Figure 3* represent the phase relationship among the different groups of clock outputs from W219B when it is providing a 66-MHz CPU clock and a 100-MHz CPU clock, respectively. It should be noted that when CPU clock is operating at 100 MHz, CPU clock output is 180 degrees out of phase with SDRAM clock outputs.

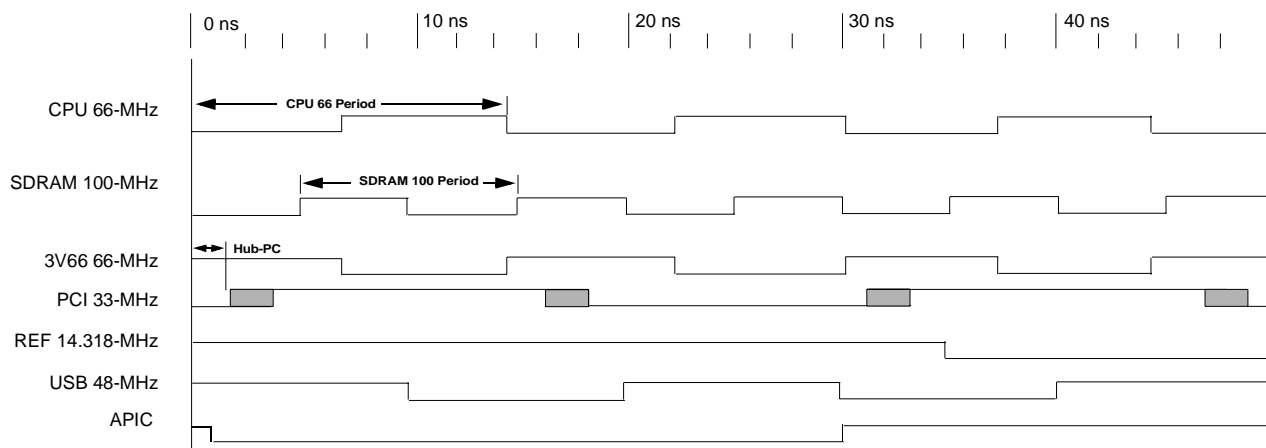


Figure 2. Group Offset Waveforms (66.8 CPU Clock, 100.2 SDRAM Clock)

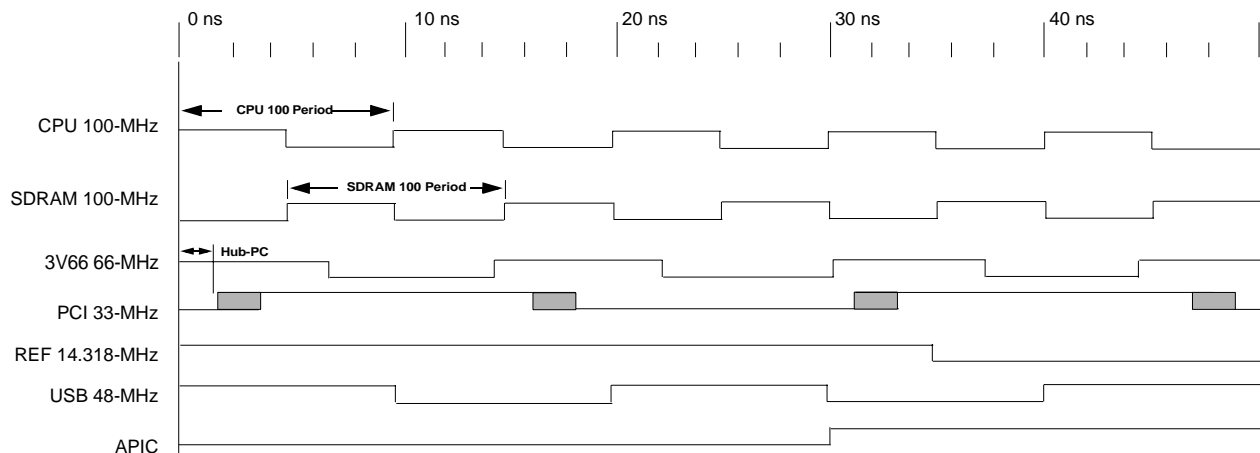


Figure 3. Group Offset Waveforms (100.2 CPU Clock, 100.2 SDRAM Clock)

Power-Down Control

W219B provides one PWRDWN# signal to place the device in low-power mode. In low-power mode, the PLLs are turned off and all clock outputs are driven LOW.

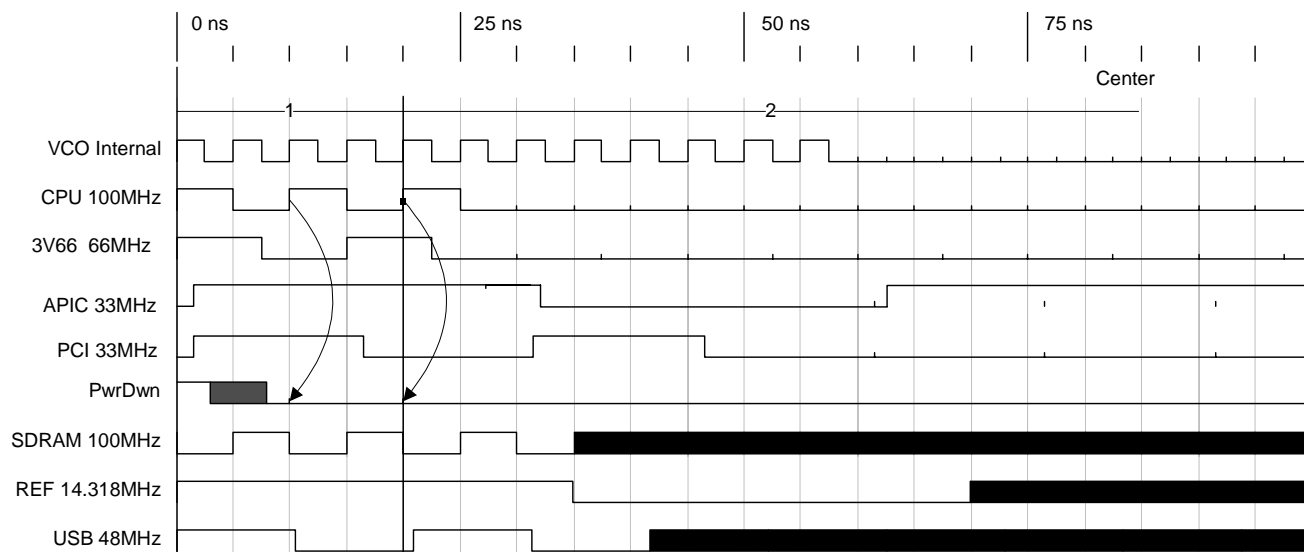


Figure 4. PWRDWN# Timing Diagram^[2, 3, 4, 5]

Notes:

2. Once the PWRDWN# signal is sampled LOW for two consecutive rising edges of CPU, clocks of interest will be held LOW on the next HIGH-to-LOW transition.
3. PWRDWN# is an asynchronous input and metastable conditions could exist. This signal is synchronized inside W219B.
4. The shaded sections on the SDRAM, REF, and USB clocks indicate "Don't Care" states.
5. Diagrams shown with respect to 100 MHz. Similar operation when CPU is 66 MHz.

Spread Spectrum Frequency Timing Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 5*.

As shown in *Figure 5*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is:

$$dB = 6.5 + 9 \log_{10}(P) + 9 \log_{10}(F)$$

Where P is the percentage of deviation and F is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 6*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is $\pm 0.45\%$ or -0.6% of the selected frequency. *Figure 6* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

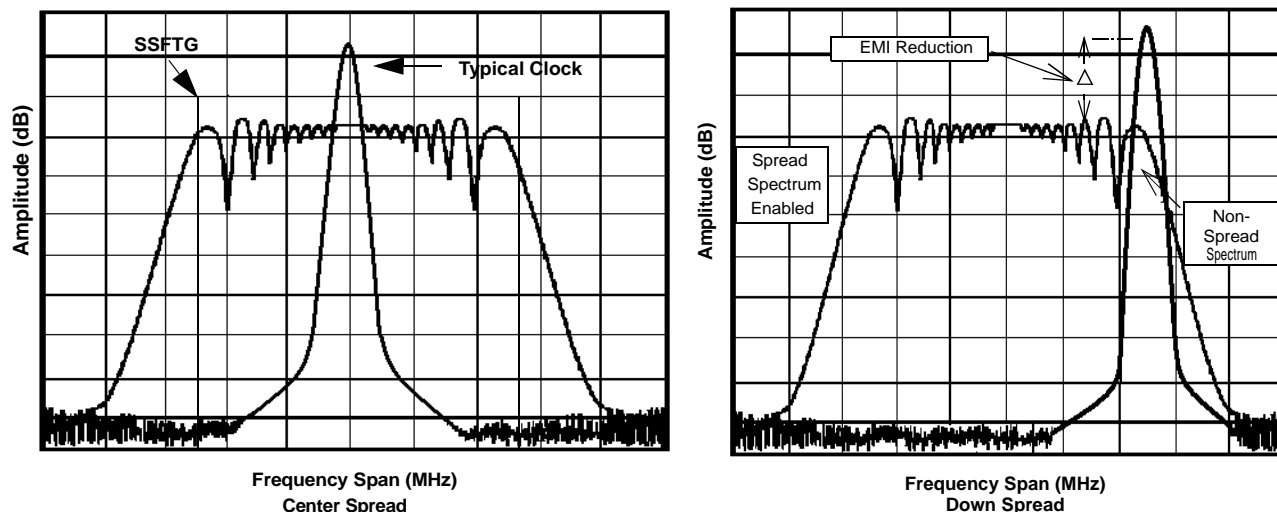


Figure 5. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

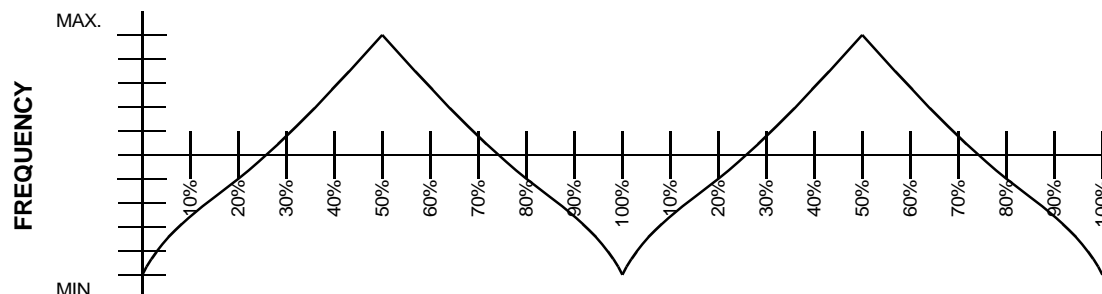


Figure 6. Typical Modulation Profile

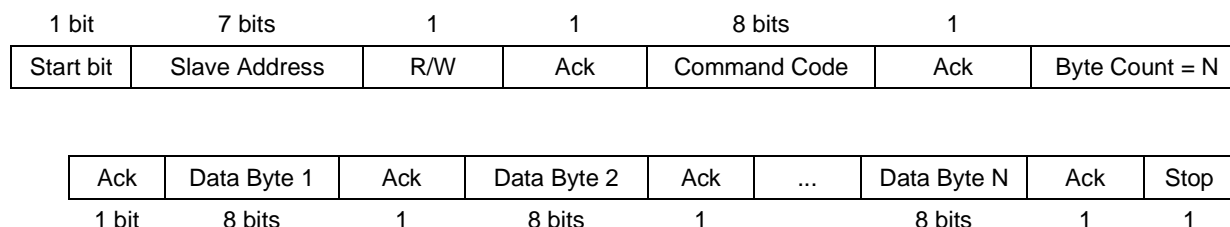


Figure 7. An Example of a Block Write^[6]

Serial Data Interface

The W219B features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions.

Data Protocol

The clock driver serial protocol accepts only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. Indexed bytes are not allowed.

A block write begins with a slave address and a write condition. After the command code the core logic issues a byte count which describes how many more bytes will follow in the message. If the host had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be 0. A block write command is allowed to trans-

fer a maximum of 32 data bytes. The slave receiver address for W219B is 11010010. *Figure 7* shows an example of a block write.

The command code and the byte count bytes are required as the first two bytes of any transfer. W219B expects a command code of 0000 0000. The byte count byte is the number of additional bytes required for the transfer, not counting the command code and byte count bytes. Additionally, the byte count byte is required to be a minimum of 1 byte and a maximum of 32 bytes to satisfy the above requirement. *Table 2* shows an example of a possible byte count value.

A transfer is considered valid after the acknowledge bit corresponding to the byte count is read by the controller. The command code and byte count bytes are ignored by the W219B. However, these bytes must be included in the data write sequence to maintain proper byte allocation.

Table 2. Example of Possible Byte Count Value

| Byte Count Byte | | Notes |
|-----------------|------|--|
| MSB | LSB | |
| 0000 | 0000 | Not allowed. Must have at least one byte. |
| 0000 | 0001 | Data for functional and frequency select register (currently byte 0 in spec) |
| 0000 | 0010 | Reads first two bytes of data. (byte 0 then byte 1) |
| 0000 | 0011 | Reads first three bytes (byte 0, 1, 2 in order) |
| 0000 | 0100 | Reads first four bytes (byte 0, 1, 2, 3 in order) |
| 0000 | 0101 | Reads first five bytes (byte 0, 1, 2, 3, 4 in order) ^[7] |
| 0000 | 0110 | Reads first six bytes (byte 0, 1, 2, 3, 4, 5 in order) ^[7] |
| 0000 | 0111 | Reads first seven bytes (byte 0, 1, 2, 3, 4, 5, 6 in order) |
| 0010 | 0000 | Max. byte count supported = 32 |

Table 3. Serial Data Interface Control Functions Summary

| Control Function | Description | Common Application |
|------------------|---|---|
| Output Disable | Any individual clock output(s) can be disabled. Disabled outputs are actively held LOW. | Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots. |
| (Reserved) | Reserved function for future device revision or production device testing. | No user application. Register bit must be written as 0. |

Notes:

6. The acknowledgment bit is returned by the slave/receiver (W219B).
7. Bytes 6 and 7 are not defined for W219B.

Serial Configuration Map

1. The serial bits will be read by the clock driver in the following order:

Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

2. All unused register bits (reserved and N/A) should be written to a "0" level.

3. All register bits labeled "Initialize to 0" must be written to zero during initialization. Failure to do so may result in higher than normal operating current. The controller will read back the written value.

Byte 0: Control Register (1 = Enable, 0 = Disable)^[8]

| Bit | Pin# | Name | Default | Pin Function |
|-------|--------|-----------|---------|-------------------|
| Bit 7 | - | Reserved | 0 | Reserved |
| Bit 6 | - | Reserved | 0 | Reserved |
| Bit 5 | - | Reserved | 0 | Reserved |
| Bit 4 | - | Reserved | 0 | Reserved |
| Bit 3 | - | Reserved | 0 | Reserved |
| Bit 2 | 23 | 24/48 MHz | 1 | (Active/Inactive) |
| Bit 1 | 21, 22 | 48 MHz | 1 | (Active/Inactive) |
| Bit 0 | - | Reserved | 0 | Reserved |

Byte 1: Control Register (1 = Enable, 0 = Disable)^[8]

| Bit | Pin# | Name | Default | Pin Description |
|-------|------|--------|---------|-------------------|
| Bit 7 | 32 | SDRAM7 | 1 | (Active/Inactive) |
| Bit 6 | 33 | SDRAM6 | 1 | (Active/Inactive) |
| Bit 5 | 35 | SDRAM5 | 1 | (Active/Inactive) |
| Bit 4 | 36 | SDRAM4 | 1 | (Active/Inactive) |
| Bit 3 | 37 | SDRAM3 | 1 | (Active/Inactive) |
| Bit 2 | 39 | SDRAM2 | 1 | (Active/Inactive) |
| Bit 1 | 40 | SDRAM1 | 1 | (Active/Inactive) |
| Bit 0 | 41 | SDRAM0 | 1 | (Active/Inactive) |

Byte 2: Control Register (1 = Enable, 0 = Disable)^[8]

| Bit | Pin# | Name | Default | Pin Description |
|-------|------|----------|---------|-------------------|
| Bit 7 | -- | Reserved | 0 | Reserved |
| Bit 6 | 19 | PCI6 | 1 | (Active/Inactive) |
| Bit 5 | 18 | PCI5 | 1 | (Active/Inactive) |
| Bit 4 | 16 | PCI4 | 1 | (Active/Inactive) |
| Bit 3 | 15 | PCI3 | 1 | (Active/Inactive) |
| Bit 2 | 13 | PCI2 | 1 | (Active/Inactive) |
| Bit 1 | 12 | PCI1 | 1 | (Active/Inactive) |
| Bit 0 | 11 | PCI0 | 1 | (Active/Inactive) |

Note:

8. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

Byte 3: Reserved Register (1 = Enable, 0 = Disable)

| Bit | Pin# | Name | Default | Pin Description |
|-------|------|----------|---------|-------------------|
| Bit 7 | 31 | SDRAM8 | 1 | (Active/Inactive) |
| Bit 6 | - | Reserved | 0 | Reserved |
| Bit 5 | - | Reserved | 0 | Reserved |
| Bit 4 | - | Reserved | 0 | Reserved |
| Bit 3 | 47 | APIC | 1 | (Active/Inactive) |
| Bit 2 | - | Reserved | 0 | Reserved |
| Bit 1 | - | Reserved | 1 | Reserved |
| Bit 0 | - | Reserved | 0 | Reserved |

Byte 4: Reserved Register (1 = Enable, 0 = Disable)

| Bit | Pin# | Name | Default | Pin Function |
|-------|------|------------------|---------|--|
| Bit 7 | - | SEL3 | 0 | See Table 4 |
| Bit 6 | - | SEL2 | 0 | See Table 4 |
| Bit 5 | - | SEL1 | 0 | See Table 4 |
| Bit 4 | - | SEL0 | 0 | See Table 4 |
| Bit 3 | - | FS(0:4) Override | 0 | 0 = Select operating frequency by FS(0:4) strapping 1 = Select operating frequency by SEL(0:4) bit settings |
| Bit 2 | - | SEL4 | 0 | See Table 4 |
| Bit 1 | - | Reserved | 0 | Reserved |
| Bit 0 | - | Test Mode | 0 | 0 = All output enable 1 = All output three-stated |

Byte 5: Reserved Register (1 = Enable, 0 = Disable)

| Bit | Pin# | Name | Default | Pin Description |
|-------|------|----------|---------|-----------------|
| Bit 7 | - | Reserved | 0 | Reserved |
| Bit 6 | - | Reserved | 0 | Reserved |
| Bit 5 | - | Reserved | 0 | Reserved |
| Bit 4 | - | Reserved | 0 | Reserved |
| Bit 3 | - | Reserved | 0 | Reserved |
| Bit 2 | - | Reserved | 0 | Reserved |
| Bit 1 | - | Reserved | 0 | Reserved |
| Bit 0 | - | Reserved | 0 | Reserved |

Byte 6: Reserved Register (1 = Enable, 0 = Disable)

| Bit | Pin# | Name | Default | Pin Description |
|-------|------|----------|---------|-----------------|
| Bit 7 | - | Reserved | 0 | Reserved |
| Bit 6 | - | Reserved | 0 | Reserved |
| Bit 5 | - | Reserved | 0 | Reserved |
| Bit 4 | - | Reserved | 0 | Reserved |
| Bit 3 | - | Reserved | 0 | Reserved |
| Bit 2 | - | Reserved | 1 | Reserved |
| Bit 1 | - | Reserved | 1 | Reserved |
| Bit 0 | - | Reserved | 0 | Reserved |

Table 4. Additional Frequency Selections through Serial Data Interface Data Bytes

| Input Conditions | | | | | Output Frequency | | | | | |
|------------------------|----------------|----------------|----------------|----------------|------------------|-------|------|------|------|-----------------|
| Data Byte 4, Bit 3 = 1 | | | | | CPU | SDRAM | 3V66 | PCI | APIC | Spread Spectrum |
| Bit 2 SEL_4 | Bit 7 SEL_3 | Bit 6 SEL_2 | Bit 5 SEL_1 | Bit 4 SEL_0 | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 75.3 | 113.0 | 75.3 | 37.6 | 18.8 | OFF |
| 0 | 0 | 0 | 0 | 1 | 95.0 | 95.0 | 63.3 | 31.6 | 15.8 | −0.6% |
| 0 | 0 | 0 | 1 | 0 | 129.0 | 129.0 | 86.0 | 43.0 | 21.5 | OFF |
| 0 | 0 | 0 | 1 | 1 | 150.0 | 113.0 | 75.3 | 37.6 | 18.8 | OFF |
| 0 | 0 | 1 | 0 | 0 | 150.0 | 150.0 | 75.0 | 37.5 | 18.7 | OFF |
| 0 | 0 | 1 | 0 | 1 | 110.0 | 110.0 | 73.0 | 36.6 | 18.3 | OFF |
| 0 | 0 | 1 | 1 | 0 | 140.0 | 140.0 | 70.0 | 35.0 | 17.5 | OFF |
| 0 | 0 | 1 | 1 | 1 | 144.0 | 108.0 | 72.0 | 36.0 | 18.0 | OFF |
| 0 | 1 | 0 | 0 | 0 | 68.3 | 102.5 | 68.3 | 34.1 | 17.0 | OFF |
| 0 | 1 | 0 | 0 | 1 | 105.0 | 105.0 | 70.0 | 35.0 | 17.5 | OFF |
| 0 | 1 | 0 | 1 | 0 | 138.0 | 138.0 | 69.0 | 34.5 | 17.0 | OFF |
| 0 | 1 | 0 | 1 | 1 | 140.0 | 105.0 | 70.0 | 35.0 | 17.5 | OFF |
| 0 | 1 | 1 | 0 | 0 | 66.8 | 100.2 | 66.8 | 33.4 | 16.7 | ±0.45% |
| 0 | 1 | 1 | 0 | 1 | 100.2 | 100.2 | 66.8 | 33.4 | 16.7 | ±0.45% |
| 0 | 1 | 1 | 1 | 0 | 133.6 | 133.6 | 66.8 | 33.4 | 16.7 | ±0.45% |
| 0 | 1 | 1 | 1 | 1 | 133.6 | 100.2 | 66.8 | 33.4 | 16.7 | ±0.45% |
| 1 | 0 | 0 | 0 | 0 | 157.3 | 118.0 | 78.6 | 39.3 | 19.6 | OFF |
| 1 | 0 | 0 | 0 | 1 | 160.0 | 120.0 | 80.0 | 40.0 | 20.0 | OFF |
| 1 | 0 | 0 | 1 | 0 | 146.6 | 110.0 | 73.3 | 36.6 | 18.3 | OFF |
| 1 | 0 | 0 | 1 | 1 | 122.0 | 91.5 | 61.0 | 30.5 | 15.2 | −0.6% |
| 1 | 0 | 1 | 0 | 0 | 127.0 | 127.0 | 84.6 | 42.3 | 21.1 | OFF |
| 1 | 0 | 1 | 0 | 1 | 122.0 | 122.0 | 81.3 | 40.6 | 20.3 | −0.6% |
| 1 | 0 | 1 | 1 | 0 | 117.0 | 117.0 | 78.0 | 39.0 | 19.5 | OFF |
| 1 | 0 | 1 | 1 | 1 | 114.0 | 114.0 | 76.0 | 38.0 | 19.0 | OFF |
| 1 | 1 | 0 | 0 | 0 | 80.0 | 120.0 | 80.0 | 40.0 | 20.0 | OFF |
| 1 | 1 | 0 | 0 | 1 | 78.0 | 117.0 | 78.0 | 39.0 | 19.5 | OFF |
| 1 | 1 | 0 | 1 | 0 | 166.0 | 124.5 | 83.0 | 41.5 | 20.7 | OFF |
| 1 | 1 | 0 | 1 | 1 | 133.6 | 133.6 | 89.0 | 44.5 | 22.2 | OFF |
| 1 | 1 | 1 | 0 | 0 | 66.6 | 100.0 | 66.6 | 33.3 | 16.6 | −0.6% |
| 1 | 1 | 1 | 0 | 1 | 100.0 | 100.0 | 66.6 | 33.3 | 16.6 | −0.6% |
| 1 | 1 | 1 | 1 | 0 | 133.3 | 133.3 | 66.6 | 33.3 | 16.6 | −0.6% |
| 1 | 1 | 1 | 1 | 1 | 133.3 | 100.0 | 66.6 | 33.3 | 16.6 | −0.6% |

DC Electrical Characteristics

DC parameters must be sustainable under steady state (DC) conditions.

Absolute Maximum DC Power Supply

| Parameter | Description | Min. | Max. | Unit |
|------------|--------------------------|------|------|------|
| V_{DDQ3} | 3.3V Core Supply Voltage | -0.5 | 4.6 | V |
| V_{DDQ2} | 2.5V I/O Supply Voltage | -0.5 | 3.6 | V |
| T_S | Storage Temperature | -65 | 150 | °C |

Absolute Maximum DC I/O

| Parameter | Description | Min. | Max. | Unit |
|------------|--------------------------|------|------|------|
| $V_{i/o3}$ | 3.3V Core Supply Voltage | -0.5 | 4.6 | V |
| $V_{i/o3}$ | 2.5V I/O Supply Voltage | -0.5 | 3.6 | V |
| ESD prot. | Input ESD Protection | 2000 | | V |

DC Operating Requirements

| Parameter | Description | Condition | Min. | Max. | Unit |
|---------------------------|--------------------------------------|----------------------------|-----------|----------------|------|
| V_{DD3} | 3.3V Core Supply Voltage | $3.3V \pm 5\%$ | 3.135 | 3.465 | V |
| V_{DDQ3} | 3.3V I/O Supply Voltage | $3.3V \pm 5\%$ | 3.135 | 3.465 | V |
| V_{DDQ2} | 2.5V I/O Supply Voltage | $2.5V \pm 5\%$ | 2.375 | 2.625 | V |
| $V_{DD3} = 3.3V \pm 5\%$ | | | | | |
| V_{ih3} | 3.3V Input High Voltage | V_{DD3} | 2.0 | $V_{DD} + 0.3$ | V |
| V_{il3} | 3.3V Input Low Voltage | | GND - 0.3 | 0.8 | V |
| I_{il} | Input Leakage Current ^[9] | $0 < V_{in} < V_{DDQ3}$ | -5 | +5 | μA |
| $V_{DDQ2} = 2.5V \pm 5\%$ | | | | | |
| V_{oh2} | 2.5V Output High Voltage | $I_{oh} = (-1 \text{ mA})$ | 2.0 | | V |
| V_{ol2} | 2.5V Output Low Voltage | $I_{ol} = (1 \text{ mA})$ | | 0.4 | V |
| $V_{DDQ3} = 3.3V \pm 5\%$ | | | | | |
| V_{oh3} | 3.3V Output High Voltage | $I_{oh} = (-1 \text{ mA})$ | 2.4 | | V |
| V_{ol3} | 3.3V Output Low Voltage | $I_{ol} = (1 \text{ mA})$ | | 0.4 | V |
| $V_{DDQ3} = 3.3V \pm 5\%$ | | | | | |
| V_{poh3} | PCI Bus Output High Voltage | $I_{oh} = (-1 \text{ mA})$ | 2.4 | | V |
| V_{pol3} | PCI Bus Output Low Voltage | $I_{ol} = (1 \text{ mA})$ | | 0.55 | V |
| | | | | | |
| C_{in} | Input Pin Capacitance | | | 5 | pF |
| C_{xtal} | Xtal Pin Capacitance | | 13.5 | 22.5 | pF |
| C_{out} | Output Pin Capacitance | | | 6 | pF |
| L_{pin} | Pin Inductance | | 0 | 7 | nH |
| T_a | Ambient Temperature | No Airflow | 0 | 70 | °C |

Note:

9. Input Leakage Current does not include inputs with pull-up or pull-down resistors.

AC Electrical Characteristics

$T_A = 0^\circ\text{C to } +70^\circ\text{C}$, $V_{DDQ3} = 3.3\text{V} \pm 5\%$, $V_{DDQ2} = 2.5\text{V} \pm 5\%$
 $f_{XTL} = 14.31818 \text{ MHz}$

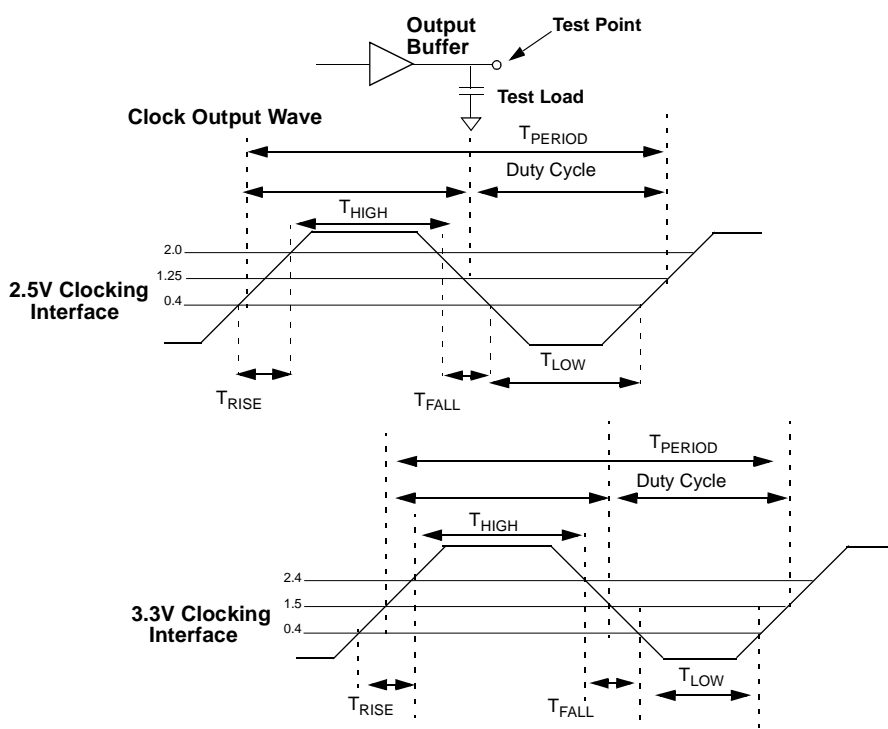
| Parameter | Description | 66.6-MHz Host | | 100-MHz Host | | 133-MHz Host | | Unit | Notes |
|----------------------------------|---------------------------------------|---------------|------|--------------|------|--------------|------|------|--------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| T_{Period} | Host/CPUCCLK Period | 15.0 | 15.5 | 10.0 | 10.5 | 7.5 | 8.0 | ns | 10 |
| T_{HIGH} | Host/CPUCCLK High Time | 5.2 | N/A | 3.0 | N/A | 1.87 | N/A | ns | 13 |
| T_{LOW} | Host/CPUCCLK Low Time | 5.0 | N/A | 2.8 | N/A | 1.67 | N/A | ns | |
| T_{RISE} | Host/CPUCCLK Rise Time | 0.4 | 1.6 | 0.4 | 1.6 | 0.4 | 1.6 | ns | 14 |
| T_{FALL} | Host/CPUCCLK Fall Time | 0.4 | 1.6 | 0.4 | 1.6 | 0.4 | 1.6 | ns | 14 |
| T_{Period} | SDRAM CLK Period | 10.0 | 10.5 | 10.0 | 10.5 | 10.0 | 10.5 | ns | 10 |
| T_{HIGH} | SDRAM CLK High Time | 3.0 | N/A | 3.0 | N/A | 3.0 | N/A | ns | 13 |
| T_{LOW} | SDRAM CLK Low Time | 2.8 | N/A | 2.8 | N/A | 2.8 | N/A | ns | |
| T_{RISE} | SDRAM CLK Rise Time | 0.4 | 1.6 | 0.4 | 1.6 | 0.4 | 1.6 | ns | 14 |
| T_{FALL} | SDRAM CLK Fall Time | 0.4 | 1.6 | 0.4 | 1.6 | 0.4 | 1.6 | ns | 14 |
| T_{Period} | APIC CLK Period | 60.0 | 64.0 | 60.0 | N/A | 60.0 | 64.0 | ns | 10 |
| T_{HIGH} | APIC CLK High Time | 25.5 | N/A | 25.5 | N/A | 25.5 | N/A | ns | 13 |
| T_{LOW} | APIC CLK Low Time | 25.3 | N/A | 25.30 | N/A | 25.30 | N/A | ns | |
| T_{RISE} | APIC CLK Rise Time | 0.4 | 1.6 | 0.4 | 1.6 | 0.4 | 1.6 | ns | 14 |
| T_{FALL} | APIC CLK Fall Time | 0.4 | 1.6 | 0.4 | 1.6 | 0.4 | 1.6 | ns | 14 |
| T_{Period} | 3V66 CLK Period | 30.0 | N/A | 30.0 | N/A | 30.0 | N/A | ns | 10, 12 |
| T_{HIGH} | 3V66 CLK High Time | 12.0 | N/A | 12.0 | N/A | 12.0 | N/A | ns | 13 |
| T_{LOW} | 3V66 CLK Low Time | 12.0 | N/A | 12.0 | N/A | 12.0 | N/A | ns | |
| T_{RISE} | 3V66 CLK Rise Time | 0.4 | 1.6 | 0.4 | 1.6 | 0.4 | 1.6 | ns | 14 |
| T_{FALL} | 3V66 CLK Fall Time | 0.4 | 1.6 | 0.4 | 1.6 | 0.4 | 1.6 | ns | 14 |
| T_{Period} | PCI CLK Period | 15.0 | 16.0 | 15.0 | 16.0 | 15.0 | 16.0 | ns | 10, 11 |
| T_{HIGH} | PCI CLK High Time | 5.25 | N/A | 5.25 | N/A | 5.25 | N/A | ns | 13 |
| T_{LOW} | PCI CLK Low Time | 5.05 | N/A | 5.05 | N/A | 5.05 | N/A | ns | |
| T_{RISE} | PCI CLK Rise Time | 0.5 | 2.0 | 0.5 | 2.0 | 0.5 | 2.0 | ns | 14 |
| T_{FALL} | PCI CLK Fall Time | 0.5 | 2.0 | 0.5 | 2.0 | 0.5 | 2.0 | ns | 14 |
| $t_{\text{pZL}}, t_{\text{pZH}}$ | Output Enable Delay (All outputs) | 30.0 | N/A | 30.0 | N/A | 30.0 | N/A | ns | |
| $t_{\text{pLZ}}, t_{\text{pZH}}$ | Output Disable Delay (All outputs) | 12.0 | N/A | 12.0 | N/A | 12.0 | N/A | ns | 14 |
| t_{stable} | All Clock Stabilization from Power-Up | 12.0 | N/A | 12.0 | N/A | 12.0 | N/A | ms | 14 |

Notes:

- Period, jitter, offset, and skew measured on rising edge at 1.25 for 2.5V clocks and at 1.5V for 3.3V clocks.
- T_{HIGH} is measured at 2.0V for 2.5V outputs, 2.4V for 3.3V outputs.
- T_{LOW} is measured at 0.4V for all outputs.
- The time specified is measured from when V_{DDQ3} achieves its nominal operating level (typical condition $V_{DDQ3} = 3.3\text{V}$) until the frequency output is stable and operating within specification.
- T_{RISE} and T_{FALL} are measured as a transition through the threshold region $V_{\text{ol}} = 0.4\text{V}$ and $V_{\text{oh}} = 2.0\text{V}$ (1 mA) JEDEC specification for 2.5V outputs, and $V_{\text{ol}} = 0.4\text{V}$ and $V_{\text{oh}} = 2.4\text{V}$ for 3.3V.

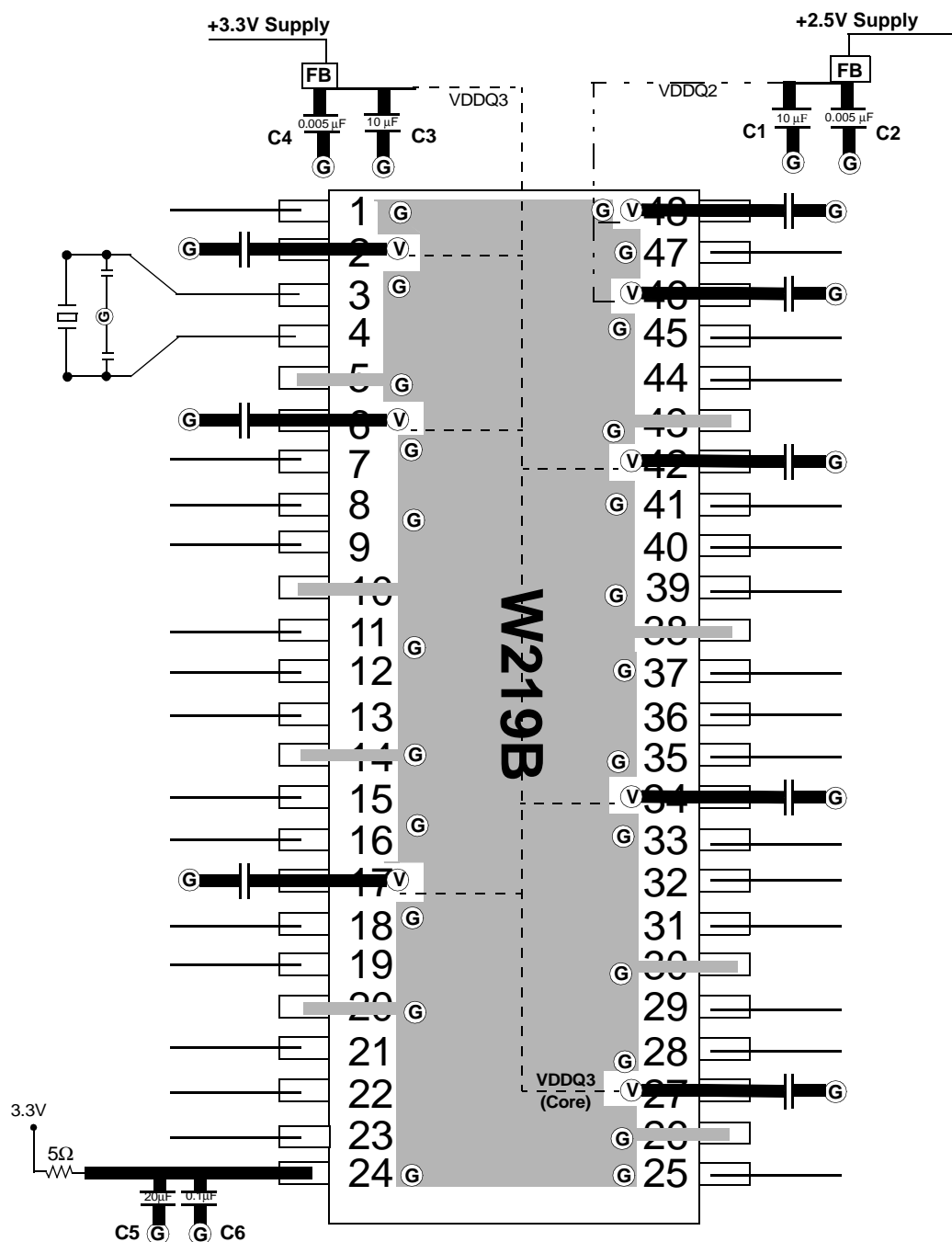
Group Skew and Jitter Limits

| Output Group | Pin-Pin Skew Max. | Cycle-Cycle Jitter | Duty Cycle | Nom Vdd | Skew, Jitter Measure Point |
|--------------|-------------------|--------------------|------------|---------|----------------------------|
| CPU | 175 ps | 250 ps | 45/55 | 2.5V | 1.25V |
| SDRAM | 250 ps | 250 ps | 45/55 | 3.3V | 1.5V |
| APIC | 250 ps | 500 ps | 45/55 | 2.5V | 1.25V |
| 48MHz | 250 ps | 500 ps | 45/55 | 3.3V | 1.5V |
| 3V66 | 175 ps | 500 ps | 45/55 | 3.3V | 1.5V |
| PCI | 500 ps | 500 ps | 45/55 | 3.3V | 1.5V |
| REF | N/A | 1000 ps | 45/55 | 3.3V | 1.5V |


Figure 8. Output Buffer
Ordering Information

| Ordering Code | Package Name | Package Type |
|---------------|--------------|------------------------|
| W219B | H | 48-pin SSOP (300 mils) |

Intel is a registered trademark of Intel Corporation.

Layout Example


FB = Dale ILB1206 - 300 (300 Ω @ 100 MHz) or TDK ACB2012L-120

Ceramic Caps C1 & C3, C5 = 10 – 22 μ F C2 & C4 = 0.005 μ F C6 = 0.1 μ F

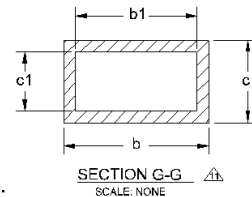
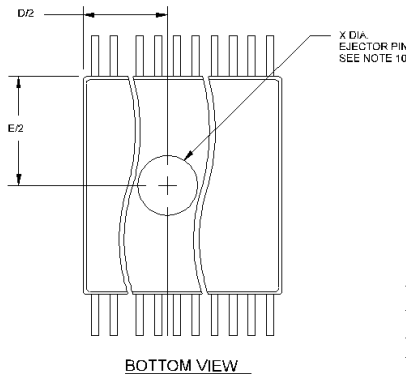
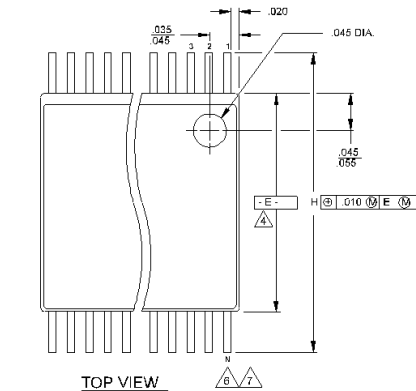
ⓐ = VIA to GND plane layer ⓑ = VIA to respective supply plane trace

Note: Each supply plane or strip should have a ferrite bead and capacitors

All VDD by pass capacitors = 0.1 μ F

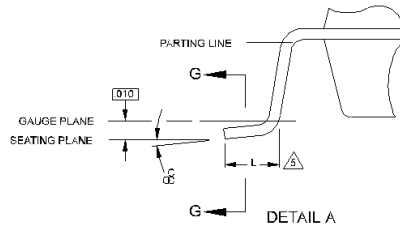
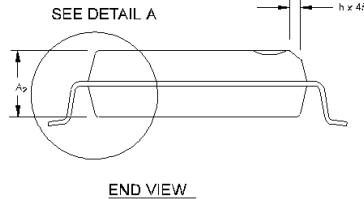
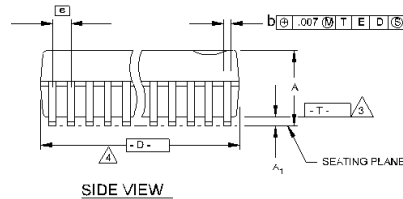
Package Diagram

48-Pin Shrink Small Outline Package (SSOP, 300 mils)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .005 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015/.025".



| SYMBOL | COMMON DIMENSIONS | | | NOTE VARIATIONS | 4 D | | | 6 N |
|----------------|-------------------|------|-------|-----------------|------|------|------|-----|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. | |
| A | .095 | .102 | .110 | AA | .620 | .625 | .630 | 48 |
| A ₁ | .008 | .012 | .016 | AB | .720 | .725 | .730 | 56 |
| A ₂ | .008 | .090 | .092 | | | | | |
| b | .008 | .010 | .0135 | | | | | |
| b ₁ | .008 | .010 | .012 | | | | | |
| c | .005 | - | .010 | | | | | |
| c ₁ | .005 | .006 | .0085 | | | | | |
| D | SEE VARIATIONS | | | 4 | | | | |
| E | .292 | .296 | .299 | | | | | |
| e | .025 BSC | | | | | | | |
| H | .400 | .406 | .410 | | | | | |
| h | .010 | .013 | .016 | | | | | |
| L | .024 | .032 | .040 | | | | | |
| N | SEE VARIATIONS | | | 6 | | | | |
| X | .085 | .093 | .100 | 10 | | | | |
| α | 0° | 5° | 8° | | | | | |

THIS TABLE IN INCHES

| SYMBOL | COMMON DIMENSIONS | | | NOTE VARIATIONS | 4 D | | | 6 N |
|----------------|-------------------|-------|-------|-----------------|-------|-------|-------|-----|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. | |
| A | 2.41 | 2.59 | 2.79 | AA | 15.75 | 15.88 | 16.00 | 48 |
| A ₁ | 0.20 | 0.31 | 0.41 | AB | 18.29 | 18.42 | 18.54 | 56 |
| A ₂ | 2.24 | 2.29 | 2.34 | | | | | |
| b | 0.203 | 0.254 | 0.343 | | | | | |
| b ₁ | 0.203 | 0.254 | 0.305 | | | | | |
| c | 0.127 | - | 0.254 | | | | | |
| c ₁ | 0.127 | 0.152 | 0.216 | | | | | |
| D | SEE VARIATIONS | | | 4 | | | | |
| E | 7.42 | 7.52 | 7.59 | | | | | |
| e | 0.635 BSC | | | | | | | |
| H | 10.16 | 10.31 | 10.41 | | | | | |
| h | 0.25 | 0.33 | 0.41 | | | | | |
| L | 0.61 | 0.81 | 1.02 | | | | | |
| N | SEE VARIATIONS | | | 6 | | | | |
| X | 2.16 | 2.36 | 2.54 | 10 | | | | |
| α | 0° | 5° | 8° | | | | | |

THIS TABLE IN MILLIMETERS



| Document Title: W219B Frequency Generator for Integrated Core Logic with 133-MHz FSB Document Number: 38-07220 | | | | |
|---|----------------|-------------------|------------------------|---|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 110485 | 10/21/01 | SZV | Change from Spec number: 38-00884 to 38-07220 |