Spread Spectrum FTG for 440BX and VIA Apollo Pro-133

Features

- **Maximized EMI suppression using Cypress's spread spectrum technology**
- **Optimized system frequency synthesizer for 440BX and VIA Apollo Pro-133**
- **Four copies of CPU output**
- **Eight copies of PCI clock (synchronous w/CPU output)**
- **Two copies of 14.318-MHz IOAPIC output and three buffered copies of 14.318-MHz reference input**
- **One copy of 48-MHz USB output**
- **Selectable 24-/48-MHz clock-through-resistor strapping**
- **Power management control input pins**
- **Programmable clock outputs up to 155 MHz via SMBus interface (32 selectable frequencies)**

Key Specifications

Supply Voltages: ..... VDDQ3 = 3.3V±5%
VDDQ2 = 2.5V±5%

CPU Cycle to Cycle Jitter: ..... 250 ps

CPU0:3 Output Skew: ..... 175 ps

PCI_F, PCI1:7 Output Skew: ..... 500 ps

CPU to PCI Output Skew: ..... 1.0–4.0 ns (CPU Leads)

REF0/SEL48#, SCLK,SDATA: ..... 250K pull-up

FS1: ..... 250K pull-down

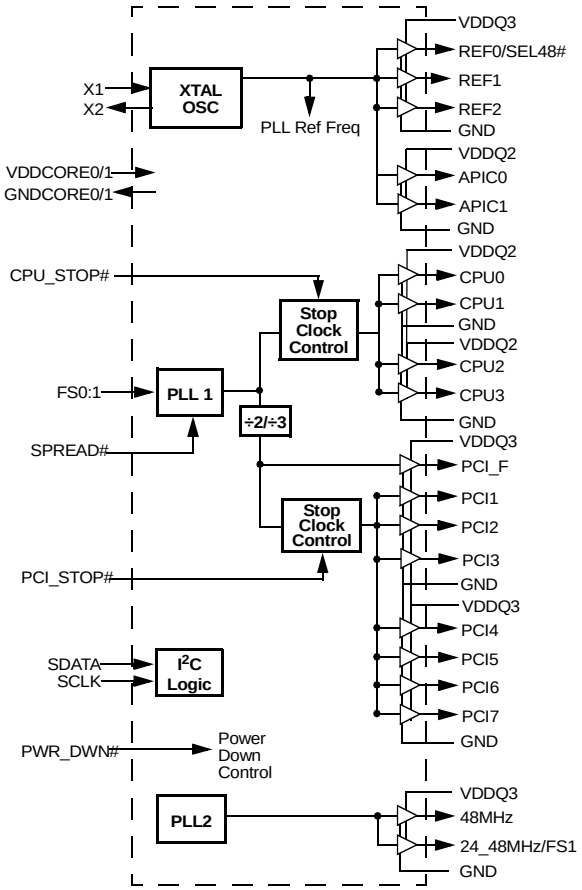
FS0: ..... No pull-up or pull-down

Test mode and output three-state through SMBus interface

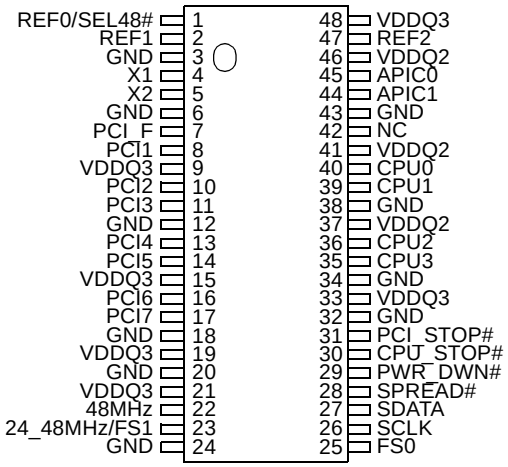
Table 1. Pin Selectable Frequency

FS1	FS0	CPU(0:3)	PCI
1	1	133.3 MHz	33.3 MHz
1	0	105 MHz	35 MHz
0	1	100 MHz	33.3 MHz
0	0	66.8 MHz	33.3 MHz

Block Diagram



Pin Configuration[1]



Note:

1. Internal pull-up resistors should not be relied upon for setting I/O pins HIGH.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:3	40, 39, 36, 35	O	***CPU Clock Outputs 0 through 3:*** These four CPU clock outputs are controlled by the CPU_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ2.
PCI1:7	8, 10, 11, 13, 14, 16, 17	O	***PCI Bus Clock Outputs 1 through 7:*** These seven PCI clock outputs are controlled by the PCI_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ3.
PCI_F	7	O	***Fixed PCI Clock Output:*** Unlike PCI1:7 outputs, this output is not controlled by the PCI_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ3.
CPU_STOP#	30	I	***CPU_STOP# Input:*** When brought LOW, clock outputs CPU0:3 are stopped LOW after completing a full clock cycle (2-3 CPU clock latency). When brought HIGH, clock outputs CPU0:3 start beginning with a full clock cycle (2-3 CPU clock latency).
PCI_STOP#	31	I	***PCI_STOP# Input:*** The PCI_STOP# input enables the PCI 1:7 outputs when HIGH and causes them to remain at logic 0 when LOW. The PCI_STOP signal is latched on the rising edge of PCI_F. Its effect takes place on the next PCI_F clock cycle.
SPREAD#	28	I	***SPREAD# Input:*** When brought low this pin activates Spread Spectrum clocking.
APIC0:1	45, 44	O	***I/O APIC Clock Outputs:*** Provides 14.318-MHz fixed frequency. The output voltage swing is controlled by VDDQ2.
48MHz	22	O	***48-MHz Output:*** Fixed clock outputs at 48 MHz. Output voltage swing is controlled by voltage applied to VDDQ3.
24_48MHz/FS1	23	O	***24-MHz or 48-MHz Output/Frequency Select 1:*** 24 MHz output when pin 1 is strapped through 10-KΩ resistor to VDDQ3. 48-MHz output when pin 1 is strapped through 10-KΩ resistor to GND. This pin also serves as the select strap to determine device operating frequency as described in *Table 1*.
REF0/SEL48#	1	I/O	***I/O Dual-Function REF0 and SEL48# pin:*** During power-on, SEL48# input will be latched which will set pin 23 to output 24 MHz or 48 MHz. It then reverts to REF0 fixed output.
REF1:2	2, 47	O	***Fixed 14.318-MHz Outputs 1 through 2:*** Used for various system applications. Output voltage swing is controlled by voltage applied to VDDQ3.
FS0	25	I	***Frequency Selection 0:*** Selects power-up default CPU clock frequency as shown in *Table 1*.
SCLK	26	I	Clock pin for SMBus circuitry.
SDATA	27	I/O	Data pin for SMBus circuitry.
X1	4	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	5	I	***Crystal Connection:*** An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
PWR_DWN#	29	I	***Power-Down Control:*** When this input is LOW, device goes into a low-power stand-by condition. All outputs are actively held LOW while in power-down. CPU and PCI clock outputs are stopped LOW after completing a full clock cycle (2–3 CPU clock cycle latency). When brought high, CPU, SDRAM and PCI outputs start with a full clock cycle at full operating frequency (3 ms maximum latency).
VDDQ3	9, 15, 19, 21, 33, 48	P	***Power Connection:*** Connect to 3.3V supply.
VDDQ2	46, 41, 37	P	***Power Connection:*** Power supply for APIC0:1 and CPU0:3 output buffers. Connect to 2.5V.
GND	3, 6, 12, 18, 20, 24, 32, 34, 38, 43	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

Overview

The W204, a motherboard clock synthesizer, can provide either a 2.5V or 3.3V CPU clock swing making it suitable for a variety of CPU options. A fixed 48-MHz clock is provided for other system functions. The device W204 supports spread spectrum clocking for reduced EMI.

Functional Description

I/O Pin Operation

Pins 1 and 23 are dual-purpose I/O pins. Upon power-up these pins act as a logic input, allowing the determination of assigned device functions. A short time after power-up, the logic state of the pin is latched and the pin becomes a clock output. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10-KΩ "strapping" resistor is connected between the I/O pin and ground or V_{DD}. Connection to ground sets a latch to "0", connection to V_{DD} sets a latch to "1". *Figure 1* and *Figure 2* show two suggested methods for strapping resistor connections.

Upon W204 power-up, the first 2 ms of operation is used for input logic selection. During this period, pins 1 and 23 are three-stated, allowing the output strapping resistor on the I/O pin to pull the pin and its associated capacitive clock load to either a logic HIGH or LOW state. At the end of the 2-ms period, the established logic "0" or "1" condition of the I/O pin is then latched. Next the output buffer is enabled which converts the I/O pin into an operating clock output. The 2-ms timer is started when V_{DD} reaches 2.0V. The input bits can only be reset by turning V_{DD} off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of clock output is 40Ω (nominal) which is minimally affected by the 10-KΩ strap to ground or V_{DD}. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or V_{DD} should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

When the clock outputs are enabled following the 2-ms input period, the associated output frequencies are delivered on the pins, assuming that V_{DD} has stabilized. If V_{DD} has not yet reached full value, output frequency initially may be below target but will increase to target once V_{DD} voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

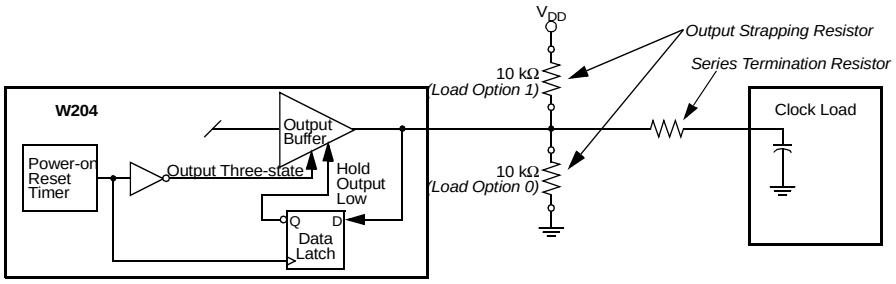


Figure 1. Input Logic Selection Through Resistor Load Option

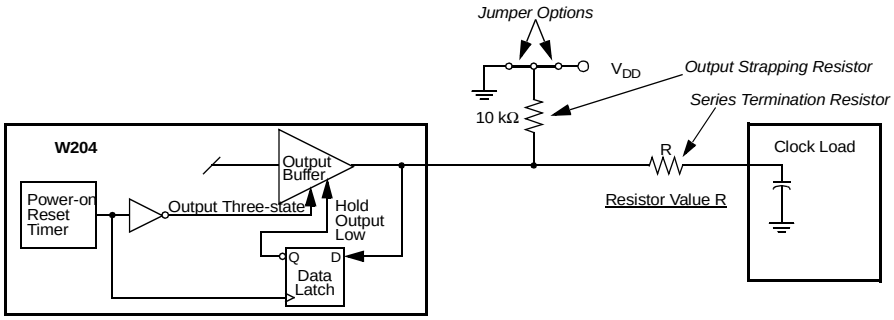


Figure 2. Input Logic Selection Through Jumper Option

Spread Spectrum Feature

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 3*.

As shown in *Figure 3*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is:

$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 4*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is ± 0.5% of the center frequency. *Figure 4* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

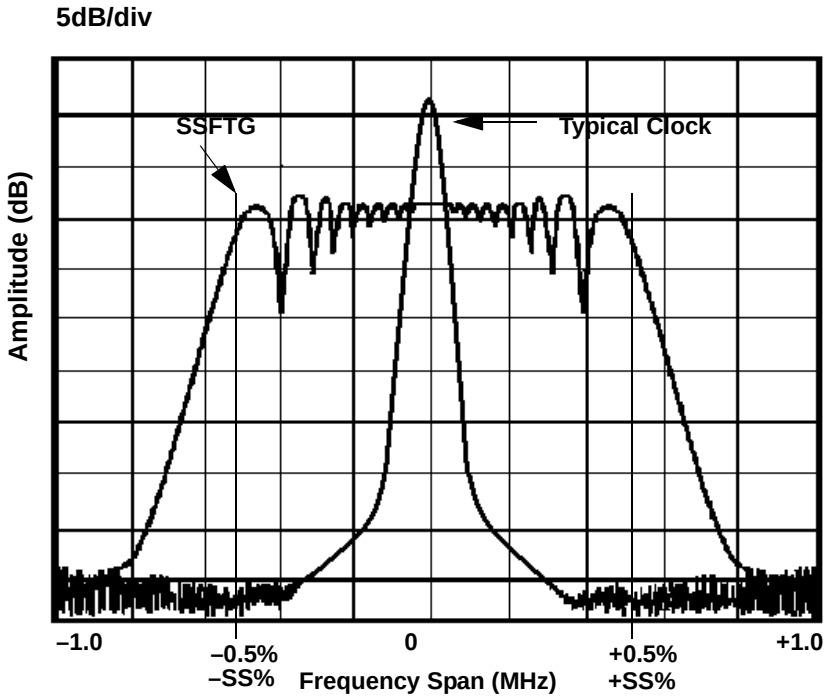


Figure 3. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

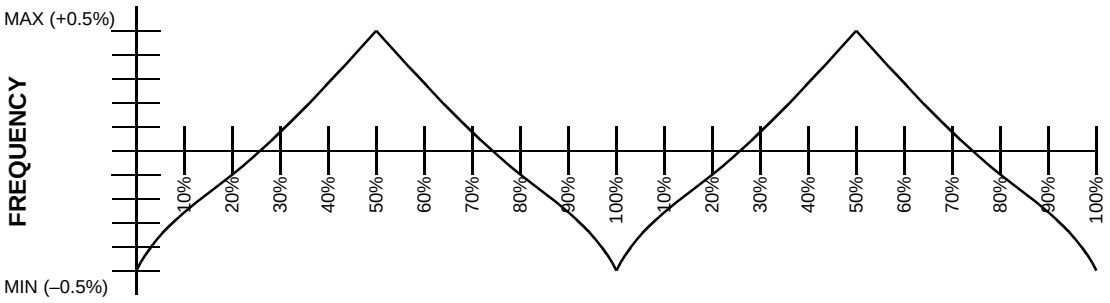


Figure 4. Typical Modulation Profile

Serial Data Interface

The W204 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the W204 initializes with default register settings. Therefore, the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if required. The interface can also be used during system operation for power management functions. *Table 2* summarizes the control functions of the serial data interface.

Operation

Data is written to the W204 in ten bytes of eight bits each. Bytes are written in the order shown in *Table 3*.

Table 2. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held LOW.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections beyond the 100- and 66.66-MHz selections that are provided by the FS0:1 pins. Frequency is changed in a smooth and controlled fashion.	For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Output Three-state	Puts all clock outputs into a high impedance state.	Production PCB testing.
Test Mode	All clock outputs toggle in relation to X1 input, internal PLL is bypassed. Refer to *Table 4*.	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Table 3. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the W204 to accept the bits in Data Bytes 3–6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W204 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the W204, therefore bit values are ignored ("Don't Care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the W204, therefore bit values are ignored ("Don't Care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Don't Care	Refer to Cypress SDRAM drivers.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3	Refer to *Table 4*	The data bits in these bytes set internal W204 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to *Table 4*, Data Byte Serial Configuration Map.
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Writing Data Bytes

Each bit in the data bytes control a particular device function except for the “reserved” bits which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. *Table 4* gives the bit formats for registers located in Data Bytes 3–6.

Table 5 details additional frequency selections that are available through the serial data interface.

Table 6 details the select functions for Byte 3, bits 1 and 0.

Table 4. Data Bytes 3–6 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 3						
7	--	--	SEL_3	Refer to *Table 5*		0
6	--	--	SEL_2	Refer to *Table 5*		0
5	--	--	SEL_1	Refer to *Table 5*		0
4	--	--	SEL_0	Refer to *Table 5*		0
3	--	--	BYT3_FS#	Frequency Controlled by external FS0:1 pins	Frequency Controlled by BYT3 SEL_(3:0)	0
2	--	--	(Reserved)	--	--	0
1–0	--	--	Bit 1 Bit 0 Function (See *Table 6* for function details) 0 0 Spread Spectrum OFF 0 1 Test Mode 1 0 Spread Spectrum ON (default) 1 1 All Outputs Three-stated			10
Data Byte 4						
7	--	--	(Reserved)	--	--	0
6	23	24_48MHz	Clock Output Disable	Low	Active	1
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	35	CPU3	Clock Output Disable	Low	Active	1
2	36	CPU2	Clock Output Disable	Low	Active	1
1	39	CPU1	Clock Output Disable	Low	Active	1
0	40	CPU0	Clock Output Disable	Low	Active	1
Data Byte 5						
7	7	PCI_F	Clock Output Disable	Low	Active	1
6	17	PCI7	Clock Output Disable	Low	Active	1
5	16	PCI6	Clock Output Disable	Low	Active	1
4	14	PCI5	Clock Output Disable	Low	Active	1
3	13	PCI4	Clock Output Disable	Low	Active	1
2	11	PCI3	Clock Output Disable	Low	Active	1
1	10	PCI2	Clock Output Disable	Low	Active	1
0	8	PCI1	Clock Output Disable	Low	Active	1
Data Byte 6						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	44	APIC1	Clock Output Disable	Low	Active	1
4	45	APIC0	Clock Output Disable	Low	Active	1
3	--	--	(Reserved)	--	--	0
2	47	REF2	Clock Output Disable	Low	Active	1
1	2	REF1	Clock Output Disable	Low	Active	1
0	1	REF0	Clock Output Disable	Low	Active	1

Table 5. Additional Frequency Selections through Serial Data Interface Data Bytes

Input Conditions Data Byte 3, Bit [7:4, 1:0]					Output Frequency		If Spread Is On
Bit [1:0]	Bit 7 SEL_3	Bit 6 SEL_2	Bit 5 SEL_1	Bit 4 SEL_0	CPU, SDRAM Clocks (MHz)	PCI Clocks (MHz)	Spread Percentage
00	0	0	0	0	78	39	OFF
00	0	0	0	1	81	40.5	OFF
00	0	0	1	0	113.5	37.8	OFF
00	0	0	1	1	66.8	33.4	OFF
00	0	1	0	0	117	39	OFF
00	0	1	0	1	118.5	39.5	OFF
00	0	1	1	0	122	37.3	OFF
00	0	1	1	1	100	33.3	OFF
00	1	0	0	0	126	31.5	OFF
00	1	0	0	1	135	33.75	OFF
00	1	0	1	0	137	34.25	OFF
00	1	0	1	1	138.5	34.62	OFF
00	1	1	0	0	142	35.5	OFF
00	1	1	0	1	144	36	OFF
00	1	1	1	0	155	38.75	OFF
00	1	1	1	1	133.3	33.3	OFF
10	0	0	0	0	124	41.3	±0.5% Center
10	0	0	0	1	75	37.5	±0.5% Center
10	0	0	1	0	83.3	41.65	±0.5% Center
10	0	0	1	1	66.8	33.4	±0.5% Center
10	0	1	0	0	90	30	±0.5% Center
10	0	1	0	1	112	37.3	±0.5% Center
10	0	1	1	0	95	31.67	±0.5% Center
10	0	1	1	1	100	33.3	±0.5% Center
10	1	0	0	0	120	40	±0.5% Center
10	1	0	0	1	115	38.3	±0.5% Center
10	1	0	1	0	110	36.67	±0.5% Center
10	1	0	1	1	105	35	±0.5% Center
10	1	1	0	0	140	35	±0.5% Center
10	1	1	0	1	150	37.5	±0.5% Center
10	1	1	1	0	124	31	±0.5% Center
10	1	1	1	1	133.3	33.3	±0.5% Center

Table 6. Select Function for Data Byte 3, Bits 0:1

Function	Input Conditions Data Byte 3		Output Conditions				
	Bit 1	Bit 0	CPU0:3	PCI_F, PCI1:7	REF0:2, IOAPIC0:1	48MHZ	24MHZ
Spread Spectrum OFF	0	0	Note 2	Note 2	14.318 MHz	48 MHz	24 MHz
Test Mode	0	1	X1/2	CPU/2 or 3	X1	X1/2	X1/4
Spread Spectrum ON (default)	1	0	Note 2 SS%=±0.5	Note 2 SS%=±0.5	14.318 MHz	48 MHz	24 MHz
Three-state	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Note:

2. CPU and PCI frequency selections are listed in *Table 1* and *Table 5*.

How To Use the Serial Data Interface

Electrical Requirements

Figure 5 illustrates electrical characteristics for the serial interface bus used with the W204. Devices send data over the bus with an open drain logic output that can (a) pull the bus line low, or (b) let the bus default to logic 1. The pull-up resistors on the bus (both clock and data lines) establish a default logic 1. All bus devices generally have logic inputs to receive data.

Although the W204 is a receive-only device (no data write-back capability), it does transmit an “acknowledge” data pulse after each byte is received. Thus, the SDATA line can both transmit and receive data.

The pull-up resistor should be sized to meet the rise and fall times specified in AC parameters, taking into consideration total bus line capacitance.

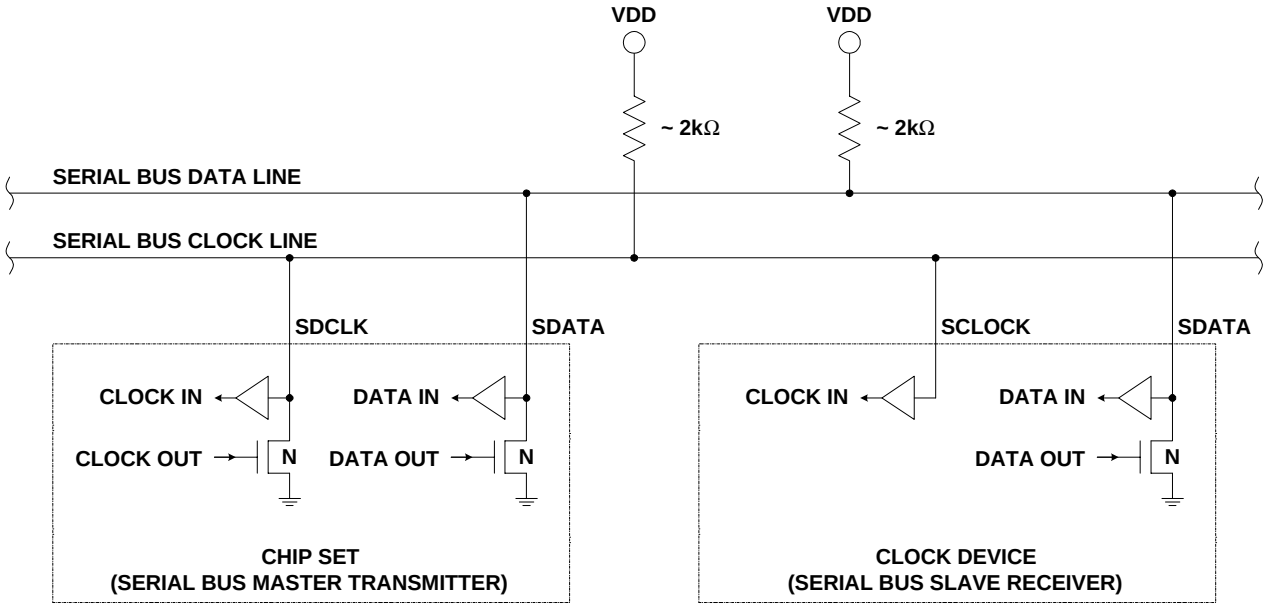


Figure 5. Serial Interface Bus Electrical Characteristics

Signaling Requirements

As shown in *Figure 6*, valid data bits are defined as stable logic 0 or 1 condition on the data line during a clock HIGH (logic 1) pulse. A transitioning data line during a clock HIGH pulse may be interpreted as a start or stop pulse (it will be interpreted as a start or stop pulse if the start/stop timing parameters are met).

A write sequence is initiated by a “start bit” as shown in *Figure 7*. A “stop bit” signifies that a transmission has ended.

As stated previously, the W204 sends an “acknowledge” pulse after receiving eight data bits in each byte as shown in *Figure 8*.

Sending Data to the W204

The device accepts data once it has detected a valid start bit and address byte sequence. Device functionality is changed upon the receipt of each data bit (registers are not double buffered). Partial transmission is allowed meaning that a transmission can be truncated as soon as the desired data bits are transmitted (remaining registers will be unmodified). Transmission is truncated with either a stop bit or new start bit (restart condition).

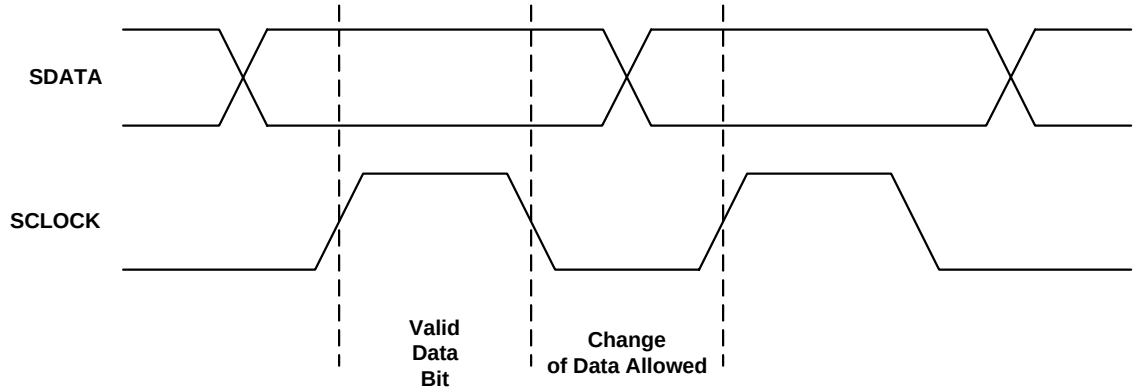


Figure 6. Serial Data Bus Valid Data Bit

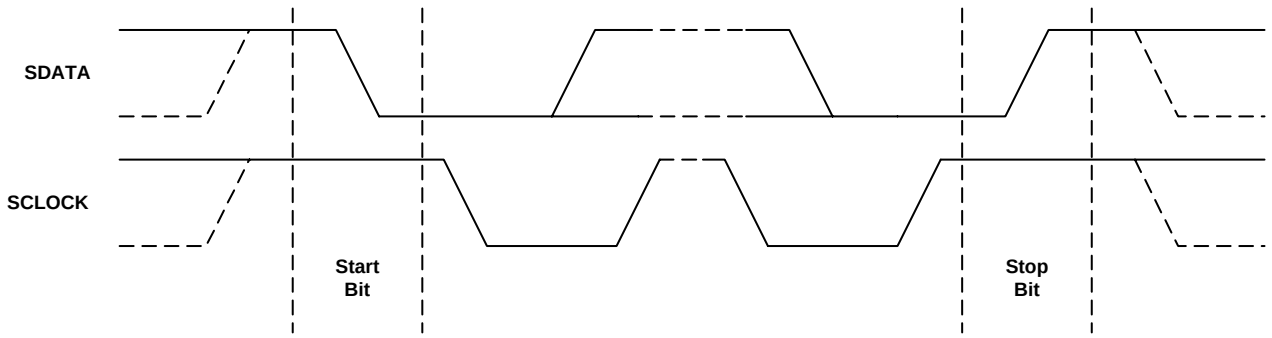


Figure 7. Serial Data Bus Start and Stop Bit

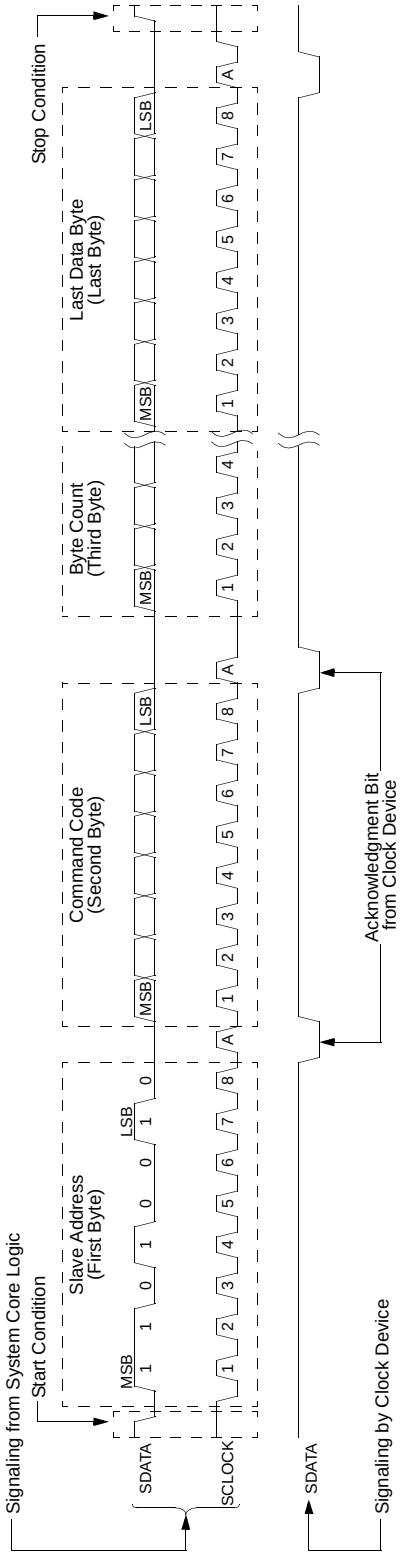


Figure 8. Serial Data Bus Write Sequence

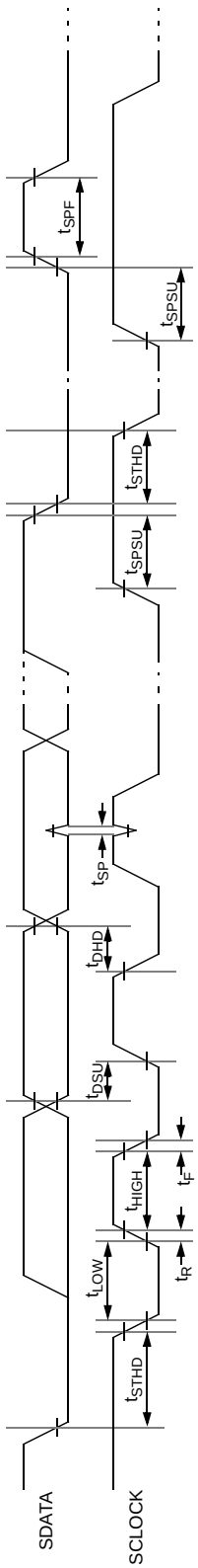


Figure 9. Serial Data Bus Timing Diagram

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
ESD_{PROT}	Input ESD Protection	2 (min.)	kV

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V±5%

Parameter	Description		Test Condition	Min.	Typ.	Max.	Unit
Supply Current							
I_{DDQ3}	3.3V Supply Current		CPU0:3 =100 MHz Outputs Loaded[3]			120	mA
I_{DDQ2}	2.5V Supply Current					60	mA
Logic Inputs							
V_{IL}	Input Low Voltage			GND – 0.3		0.8	V
V_{IH}	Input High Voltage			2.0		V_{DD} + 0.3	V
I_{IL}	Input Low Current[4]					–25	µA
I_{IH}	Input High Current[4]					10	µA
	Input Low Current (FS0)					–5	µA
	Input High Current (FS0)					+5	µA
Clock Outputs							
V_{OL}	Output Low Voltage		I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage		I_{OH} = –1 mA	3.1			V
V_{OH}	Output High Voltage (CPU, APIC)		I_{OH} = –1 mA	2.2			V
I_{OL}	Output Low Current	CPU0:3	V_{OL} = 1.25V	27	57	97	mA
		PCI_F, PCI1:7	V_{OL} = 1.5V	20.5	53	139	mA
		APIC0:1	V_{OL} = 1.25V	40	85	140	mA
		REF0:2	V_{OL} = 1.5V	25	37	76	mA
		48MHz 0:1	V_{OL} = 1.5V	25	37	76	mA
I_{OH}	Output High Current	CPU0:3	V_{OL} = 1.25V	25	55	97	mA
		PCI_F, PCI1:7	V_{OL} = 1.5V	31	55	189	mA
		APIC0:1	V_{OL} = 1.25V	40	87	155	mA
		REF0:2	V_{OL} = 1.5V	27	44	94	mA
		48MHz 0:1	V_{OL} = 1.5V	27	44	94	mA
Crystal Oscillator							
V_{TH}	X1 Input Threshold Voltage[5]		V_{DDQ3} = 3.3V		1.65		V
C_{LOAD}	Load Capacitance, as seen by External Crystal[6]				14		pF
$C_{IN,X1}$	X1 Input Capacitance[7]		Pin X2 unconnected		28		pF

Notes:

3. All clock outputs loaded with 6" 60Ω transmission lines with 20-pF capacitors.
4. W204 logic inputs have internal pull-up resistors, except FS0 (pull-ups not full CMOS level).
5. X1 input threshold voltage (typical) is $V_{DD}/2$.
6. The W204 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14 pF; this includes typical stray capacitance of short PCB traces to crystal.
7. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V±5% (continued)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%,V_{DDQ2} = 2.5V± 5%, f_{XTL} = 14.31818 MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum clocking is disabled.

CPU Clock Outputs, CPU0:3 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.8 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25V	15		15.5	10		10.5	ns
t_H	High Time	Duration of clock cycle above 2.0V	5.2			3.0			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5.0			2.8			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			200			200	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V			250			250	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20		Ω

PCI Clock Outputs, PCI1:7 and PCI_F (Lump Capacitance Test Load = 30 pF

Parameter	Description	Test Condition/Comments	CPU = 66.8/100 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	30			ns
t_H	High Time	Duration of clock cycle above 2.4V	12			ns
t_L	Low Time	Duration of clock cycle below 0.4V	12			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			500	ps
t_O	CPU to PCI Clock Skew	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.	1		4	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		30		Ω

APIC0:1 Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.8/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator	14.31818			MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		Ω

REF0:2 Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.8/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator	14.318			MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

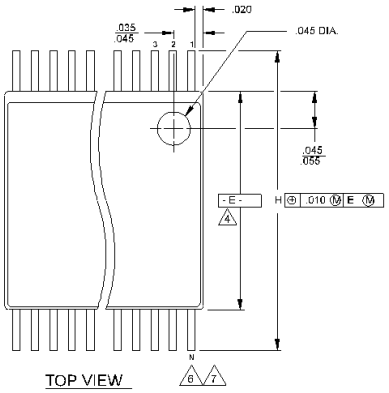
48-MHz0:1 Clock Output (Lump Capacitance Test Load = 20 pF = 66.6/100 MHz)

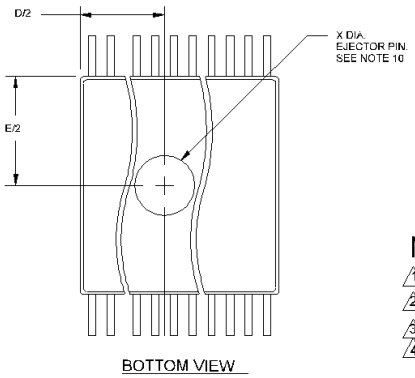
Parameter	Description	Test Condition/Comments	CPU = 66.8/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)		48.008		MHz
f_D	Deviation from 48 MHz	(48.008 – 48)/48		+167		ppm
m/n	PLL Ratio	(14.31818 MHz x 57/17 = 48.008 MHz)		57/17		
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

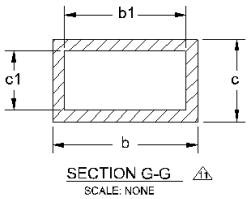
Ordering Information

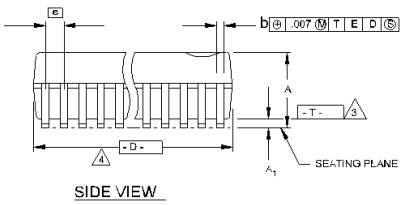
Ordering Code	Package Name	Package Type
W204	H	48-pin SSOP (300 mils)

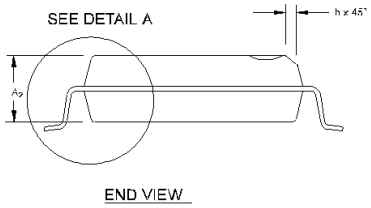
Package Diagram

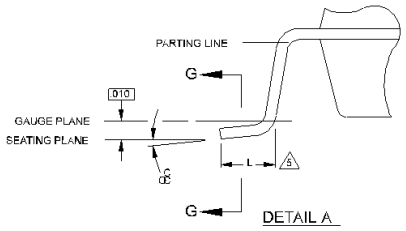












NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	.095	.102	.110		AA	.620	.625	.630	48
A_1	.008	.012	.016		AB	.720	.725	.730	56
A_2	.088	.090	.092						
b	.008	.010	.0135						
b_1	.008	.010	.012						
c	.005	-	.010						
c_1	.005	.006	.0085						
D	SEE VARIATIONS			4					
E	.292	.296	.299						
e	.025 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			6					
X	.085	.093	.100	10					
α	0°	5°	8°						

THIS TABLE IN INCHES

Summary of nominal dimensions in inches:

Body Width: 0.296
Lead Pitch: 0.025
Body Length: 0.625
Body Height: 0.102

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	2.41	2.59	2.79		AA	15.75	15.88	16.00	48
A_1	0.20	0.31	0.41		AB	18.29	18.42	18.54	56
A_2	2.24	2.29	2.34						
b	0.203	0.254	0.343						
b_1	0.203	0.254	0.305						
c	0.127	-	0.254						
c_1	0.127	0.152	0.216						
D	SEE VARIATIONS			4					
E	7.42	7.52	7.59						
e	0.635 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			6					
X	2.16	2.36	2.54	10					
α	0°	5°	8°						

THIS TABLE IN MILLIMETERS

Document Title: W204 Spread Spectrum FTG for 440BX and VIA Apollo Pro-133 Document Number: 38-07264				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110529	01/31/02	SZV	Change from Spec number: 38-01103 to 38-07264