Spread Spectrum FTG for SiS530 and 620 Chip Sets

Features

- **Maximized EMI suppression using Cypress's Spread Spectrum technology**
- **Single-chip system frequency synthesizer for SiS530 and SiS620 core logic chip sets**
- **Three copies of CPU output**
- **Six copies of PCI output**
- **One 48-MHz output for USB**
- **One 24/48 MHz selectable output for SIO**
- **Three buffered reference outputs**
- **One IOAPIC output**
- **Thirteen SDRAM outputs provide support for 3 DIMMs**
- **SMBus interface for programming allows jumperless frequency selection**

Key Specifications

CPU Cycle-to-Cycle Jitter: ..... 250 ps

CPU to CPU Output Skew: ..... 175 ps

PCI to PCI Output Skew: ..... 250 ps

CPU to PCI Output Skew (Synch. mode): ..... 1–4 ns

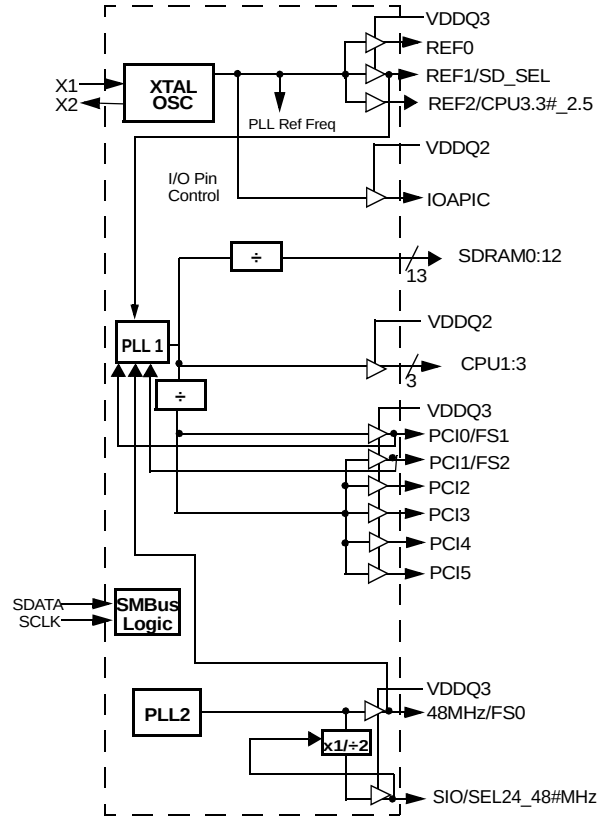
V_{DDQ3} ..... 3.3V ± 5%

V_{DDQ2} .....3.3V ± 5% or 2.5V ± 5%

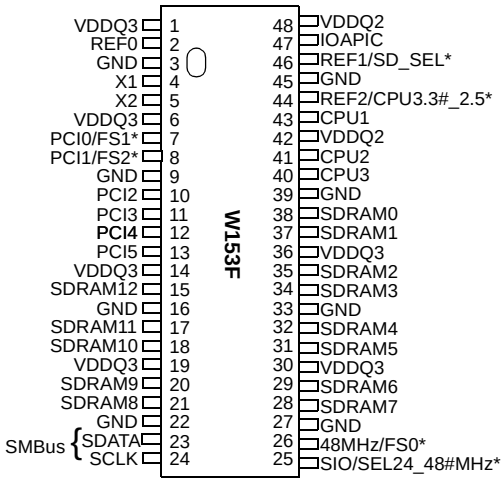
Table 1. Pin Selectable Frequency

SD_SEL	FS2	FS1	FS0	CPU1:3 (MHz)	SDRAM (MHz)	PCI
0	0	0	0	90	90	CPU/3
0	0	0	1	83.3	55.53	CPU/2.5
0	0	1	0	95.25	63.5	CPU/3
0	0	1	1	66.8	100	CPU/2
0	1	0	0	105	105	CPU/3
0	1	0	1	112	74.67	CPU/3
0	1	1	0	Reserved		
0	1	1	1	Reserved		
1	0	0	0	66.8	66.8	CPU/2
1	0	0	1	75	75	CPU/2.5
1	0	1	0	83.3	83.3	CPU/2.5
1	0	1	1	95.25	95.25	CPU/3
1	1	0	0	100.2	100.2	CPU/3
1	1	0	1	112	112	CPU/3
1	1	1	0	Reserved		
1	1	1	1	Reserved		

Block Diagram



Pin Configuration[1]



Note:

1. Internal 250kΩ pull-up resistors present on inputs marked with *. Design should not rely solely on internal pull-up resistors to set I/O pins HIGH.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU1:3	43, 41, 40	O	***CPU Clock Outputs:*** See *Table 1* and *Table 5* for detailed frequency information. Output voltage swing is controlled by voltage applied to VDDQ2.
PCI0/FS1	7	I/O	***PCI Clock Outputs 0/Frequency Selection 1:*** PCI clock outputs. Output voltage swing is controlled by voltage applied to VDDQ3. Shortly after initial power-up the pin is sampled as an input to determine CPU, SDRAM, and PCI operating frequencies.
PCI1/FS2	8	I/O	***PCI Clock Outputs 1/Frequency Selection 2:*** PCI clock outputs. Output voltage swing is controlled by voltage applied to VDDQ3. Shortly after initial power-up the pin is sampled as an input to determine CPU, SDRAM, and PCI operating frequencies.
PCI2:5	10, 11, 12, 13	O	***PCI Clock Outputs 2 through 5:*** PCI clock outputs. Output voltage swing is controlled by voltage applied to VDDQ3.
IOAPIC	47	O	***IOAPIC Clock Output:*** Provides 14.318 MHz fixed frequency. The output voltage swing is controlled by VDDQ2.
48MHz/FS0	26	I/O	***48-MHz Output/Frequency Select 0:*** 48 MHz is provided in normal operation. In standard systems, this output can be used as the reference for the Universal Serial Bus. Upon power-up FS0 input will be latched, which will set clock frequencies as described in *Table 1*. This output does not have Spread Spectrum modulation.
SIO/ SEL24_48#MHz	25	I/O	***Super I/O Output / Super I/O Frequency Select:*** This output is used for the clock input for a Super I/O chip. Upon power-up its input will be latched. If the input is a logic 1 state, SIO will be set to 24 MHz. Otherwise, the output will be set to 48 MHz.
REF1/ SD_SEL	46	I/O	***I/O Dual Function REF1/ Synchronous DRAM Interface Mode Selection:*** Upon power-up, the input will be latched, which will set clock frequencies as described in *Table 1*. When used as an output, this pin provides a fixed frequency signal determined by the reference signal provided at X1/X2 pins.
REF2/ CPU3.3#_2.5	44	I/O	***I/O Dual Function REF2/CPU Voltage Select:*** Upon power-up, the input will be latched. If the input is a logic 1 state, CPU1:3 will be configured for 2.5V operations, otherwise they are configured for 3.3V. When used as an output, this pin provides a fixed frequency signal determined by the reference signal provided at X1/X2 pins.
REF0	2	I/O	***Fixed 14.318-MHz Output 0:*** This pin provides a fixed clock signal equal in frequency to the reference signal provided at the X1/X2 pins.
SDRAM0:12	38, 37, 35, 34, 32, 31, 29, 28, 21, 20, 18, 17, 15	O	**Buffered Outputs:** These thirteen dedicated outputs provide copies of the signal provided at the SDRAMIN input. The swing is set by VDDQ3.
SCLK	24	I	Clock pin for SMBus circuitry.
SDATA	23	I/O	Data pin for SMBus circuitry.
X1	4	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	5	I	***Crystal Connection:*** An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
VDDQ3	1, 6, 14, 19, 30, 36	P	***Power Connection:*** Power supply for core logic, PLL circuitry, SDRAM outputs, PCI outputs, reference outputs, 48-MHz output, and 24-MHz output. Connect to 3.3V supply.
VDDQ2	42, 48	P	***Power Connection:*** Power supply for IOAPIC and CPU0:1 output buffers. Connect to 2.5V, or 3.3V.
GND	3, 9, 16, 22, 27, 33, 39, 45	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

Overview

The W153F is a spread spectrum system timing generator designed to support SiS530 and 620 core logic chip sets. It is a highly integrated device, providing clock outputs for CPU, core logic, super I/O, PCI, and up to three SDRAM DIMMs.

Functional Description

I/O Pin Operation

Pins 7, 8, 25, 26, 44, and 46 are dual-purpose I/O pins.

Upon power-up, each I/O pin acts as a logic input, allowing the determination of assigned device functions. A short time after power-up, the logic state of each pin is latched and each pin then becomes a clock output. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10-kΩ "strapping" resistor is connected between each I/O pin and ground or V_{DDQ3}. Connection to ground sets a "0" bit, connection to V_{DDQ3} sets a "1" bit. *Figure 1* and *Figure 2* show two suggested methods for strapping resistor connection.

Upon W153F power-up, the first 2 ms of operation is used for input logic selection. During this period, each clock output buffer is three-stated, allowing the output strapping resistor on each I/O pin to pull the pin and its associated capacitive clock load to either a logic high or low state. At the end of the 2-ms period, the established logic 0 or 1 condition of each I/O pin is then latched. Next the output buffer is enabled converting all I/O pins into operating clock outputs. The 2 ms timer starts when V_{DDQ3} reaches 2.0V. The input bits can only be reset by turning V_{DDQ3} off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of the clock outputs is <40Ω (nominal) which is minimally affected by the 10-kohm strap to ground or V_{DDQ3}. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or V_{DDQ3} should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

When each clock output is enabled following the 2-ms input period, target (normal) output frequency is delivered assuming that V_{DDQ3} has stabilized. If V_{DDQ3} has not yet reached full value, output frequency initially may be below target but will increase to target once V_{DDQ3} voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

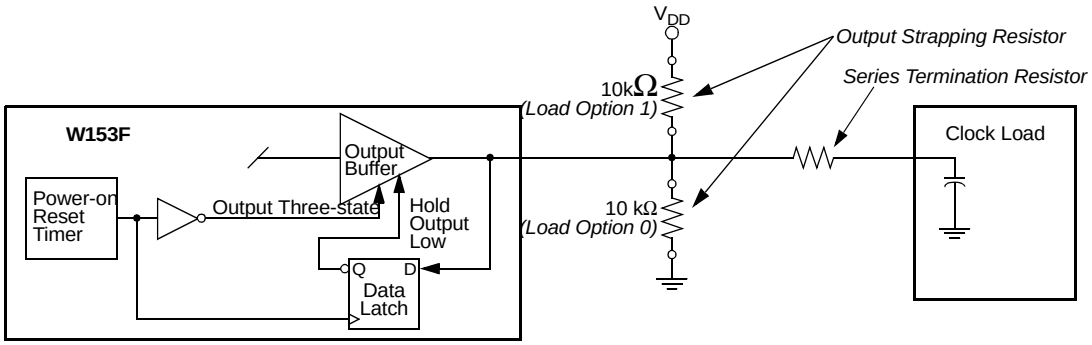


Figure 1. Selection Through Resistor Load Option.

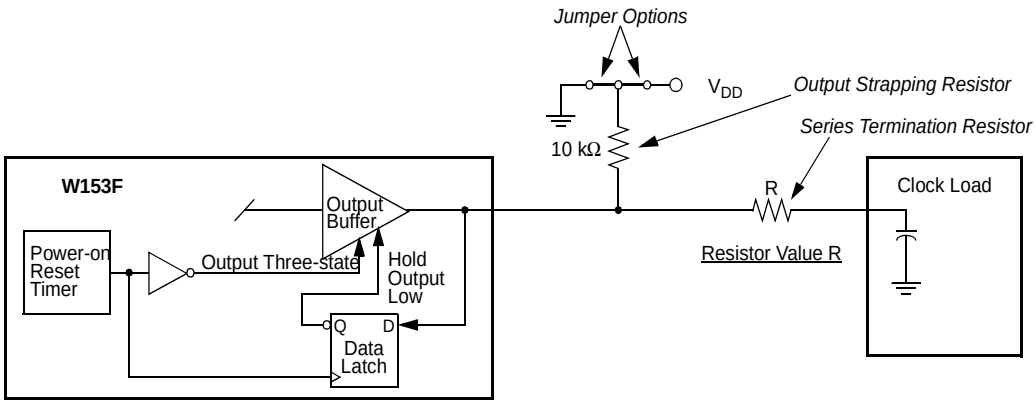


Figure 2. Input Selection Through Jumper Option.

CPU/PCI Frequency Selection

CPU frequency is selected with I/O pins 46, 26, 7, and 8 (REF1/SD_SEL, 48MHz/FS0, PCI0/FS1, and PCI1/FS2, respectively). Refer to *Table 1* for CPU/PCI frequency programming information. Alternatively, frequency selections are available through the serial data interface. Refer to *Table 3*.

Output Buffer Configuration

Clock Outputs

All clock outputs are designed to drive serial terminated clock lines. The device outputs are CMOS-type, which provide rail-to-rail output swing. To accommodate the limited voltage swing required by some processors, the output buffers of CPU0:3 use a special V_{DDQ2} power supply pin that can be tied to 2.5V nominal.

Crystal Oscillator

The device requires one input reference clock to synthesize all output frequencies. The reference clock can be either an externally generated clock signal or the clock generated by the internal crystal oscillator. When using an external clock signal, pin X1 is used as the clock input and pin X2 is left open. The input threshold voltage of pin X1 is $(V_{DDQ3})/2$.

The internal crystal oscillator is used in conjunction with a quartz crystal connected to device pins X1 and X2. This forms a parallel-resonant crystal oscillator circuit. The device incorporates the necessary feedback resistor and crystal load capacitors. Including typical stray circuit capacitance, the total load presented to the crystal is approximately 18 pF. For optimum frequency accuracy without the addition of external capacitors, a parallel-resonant mode crystal specifying a load of 18 pF should be used. This will typically yield reference frequency accuracies within ±100 ppm. To achieve similar accuracies with a crystal calling for a greater load, external capacitors must be added such that the total load (internal, external, and parasitic capacitors) equals that called for by the crystal.

Dual Supply Voltage Operation

The device is designed for dual power supply operation. Supply pin VDDQ3 is connected to a 3.3V supply and supply power to the internal core circuit and to the clock output buffers, except for outputs CPU0:3 and IOAPIC. Supply pins VDDQ2 may be connected to either a 2.5V or 3.3V supply, although device specifications may not be provided for both configurations.

Spread Spectrum Clocking

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 3*.

As shown in *Figure 3*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 4*. This waveform, as discussed in “Spread Spectrum Clock Generation for the Reduction of Radiated Emissions” by Bush, Fessler, and Hardin, produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is specified in*Table 6*. *Figure 4* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking is activated or deactivated by selecting the appropriate values for bits 1–0 in data byte 0 of the SMBus data stream. Refer to *Table 4* for more details.

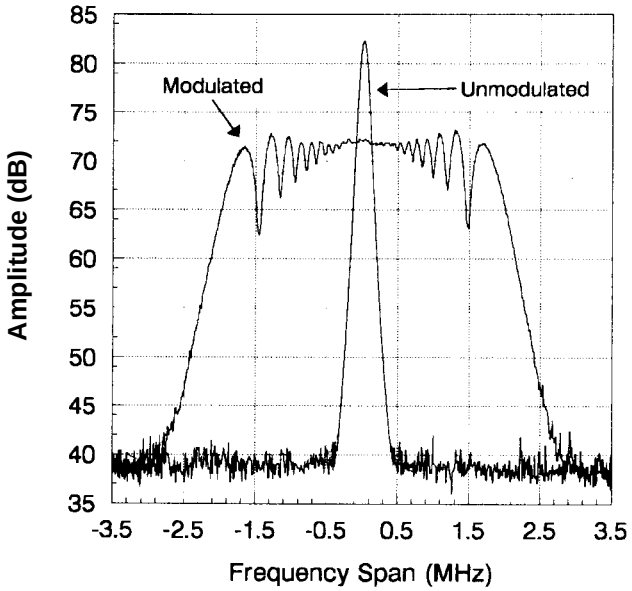


Figure 3. Clock Harmonic with an without SSCG Modulation Frequency Domain Representation.

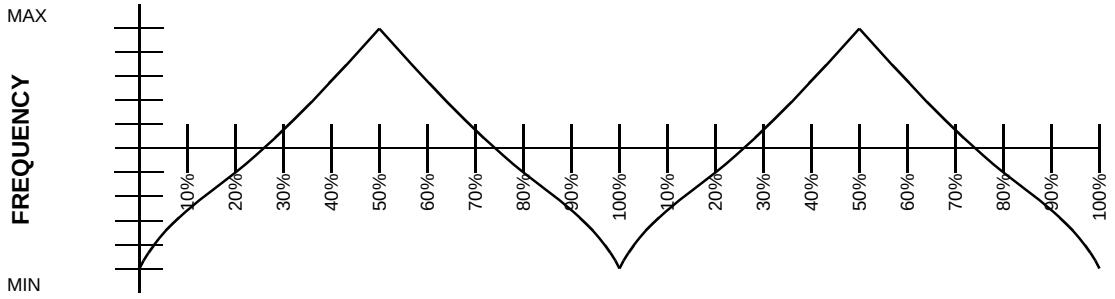


Figure 4. Typical Modulation Profile.

Serial Data Interface

The device features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the W153F initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. summarizes the control functions of the serial data interface.

Operation

Data is written to the device in ten bytes of eight bits each. Bytes are written in the order shown in *Table 3*.

Table 2. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held LOW.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused SDRAM DIMM socket or PCI slot.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections beyond the options that are provided by the frequency selection pin power-on default selection. Frequency is changed in a smooth and controlled fashion.	For alternate CPU devices, and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Output Three-state	Puts all clock outputs into a high impedance state.	Production PCB testing.
Test Mode	All clock outputs toggle in relation with X1 input, internal PLL is bypassed. Refer to *Table 4*.	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Table 3. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the device to accept the bits in Data Bytes 0–6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the device is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the device, therefore bit values are ignored (Don't Care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the device, therefore bit values are ignored (Don't Care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to *Table 4*	The data bits in these bytes set internal W153F registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to *Table 4*.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Writing Data Bytes

Each bit in the data bytes controls a particular device function except for the “reserved” bits which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7.

Table 4 gives the bit formats for registers located in Data Bytes 0–6. *Table 1* details additional frequency selections that are available through the serial data interface.

Table 2 details the select functions for Byte 0, bits 1 and 0.

Table 4. Data Bytes 0–6 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 0						
7	--	--	(Reserved)	--	--	0
6	--	--	BYTE0 _SEL2	Refer to *Table 1*		0
5	--	--	BYTE0 _SEL1	Refer to *Table 1*		0
4	--	--	BYTE0 _SEL0	Refer to *Table 1*		0
3	--	--	BYTE0 _FS#	Frequency Controlled by FS (2:0) and SD_SEL	Frequency Controlled by BYT0_SEL (3:0)	0
2	--	--	BYTE0_SEL3	Refer to *Table 5*		0
1-0	--	--	Bit 1 Bit 0 0 0 0 1 1 0 1 1	Function (See *Table 6* for function details) Normal Operation Normal Operation Spread Spectrum On All Outputs Three-stated		00
Data Byte 1						
7	--	--	(Reserved)			0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	40	CPU3	Clock Output Disable	Low	Active	1
2	41	CPU2	Clock Output Disable	Low	Active	1
1	43	CPU1	Clock Output Disable	Low	Active	1
0	--	--	(Reserved)	--	--	0
Data Byte 2						
7	--	--	(Reserved)	--	--	0
6	7	PCI0	Clock Output Disable	Low	Active	1
5	15	SDRAM12	Clock Output Disable	Low	Active	1
4	13	PCI5	Clock Output Disable	Low	Active	1
3	12	PCI4	Clock Output Disable	Low	Active	1
2	11	PCI3	Clock Output Disable	Low	Active	1
1	10	PCI2	Clock Output Disable	Low	Active	1
0	8	PCI1	Clock Output Disable	Low	Active	1

Table 4. Data Bytes 0–6 Serial Configuration Map (continued)

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 3						
7	28	SDRAM7	Clock Output Disable	Low	Active	1
6	29	SDRAM6	Clock Output Disable	Low	Active	1
5	31	SDRAM5	Clock Output Disable	Low	Active	1
4	32	SDRAM4	Clock Output Disable	Low	Active	1
3	34	SDRAM3	Clock Output Disable	Low	Active	1
2	35	SDRAM2	Clock Output Disable	Low	Active	1
1	37	SDRAM1	Clock Output Disable	Low	Active	1
0	38	SDRAM0	Clock Output Disable	Low	Active	1
Data Byte 4						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	17	SDRAM11	Clock Output Disable	Low	Active	1
2	18	SDRAM10	Clock Output Disable	Low	Active	1
1	20	SDRAM9	Clock Output Disable	Low	Active	1
0	21	SDRAM8	Clock Output Disable	Low	Active	1
Data Byte 5						
7	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	47	IOAPIC	Clock Output Disable	Low	Active	1
3	--	--	(Reserved)	--	--	0
2	44	REF2	Clock Output Disable	Low	Active	1
1	46	REF1	Clock Output Disable	Low	Active	1
0	2	REF0	Clock Output Disable	Low	Active	1
Data Byte 6						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	--	--	(Reserved)	--	--	0

Table 5. Additional Frequency Selections through Serial Data Interface Data Bytes

Input Conditions				Output Frequency		
Bit 2 BYTE0_SEL3	**Bit 6 BYTE0_SEL2**	**Bit 5 BYTE0_SEL1**	**Bit 4 BYTE0_SEL0**	**CPU (MHz)**	**SDRAM (MHz)**	**PCI Clocks (MHz)**
0	0	0	0	90	90	CPU/3
0	0	0	1	83.3	55.53	CPU/2.5
0	0	1	0	95.25	63.5	CPU/3
0	0	1	1	66.8	100	CPU/2
0	1	0	0	105	105	CPU/3
0	1	0	1	112	74.67	CPU/3
0	1	1	0	Reserved		
0	1	1	1	Reserved		
1	0	0	0	66.8	66.8	CPU/2
1	0	0	1	75	75	CPU/2.5
1	0	1	0	83.3	83.3	CPU/2.5
1	0	1	1	95.25	95.25	CPU/3
1	1	0	0	100.2	100.2	CPU/3
1	1	0	1	112	112	CPU/3
1	1	1	0	Reserved		
1	1	1	1	Reserved		

Table 6. Select Function for Data Byte 0, Bits 0:1

	Input Conditions		Output Conditions			
	Data Byte 0					
Function	**Bit 1**	**Bit 0**	**CPU0:3, SDRAM0:11**	**PCI_F, PCI0:5**	**REF0:1, IOAPIC**	**48/24MHZ**
Normal Operation	0	0	Note 2	Note 2	14.318 MHz	48/24 MHz
Normal Operation	0	1	Note 2	Note 2	14.318 MHz	48/24 MHz
Spread Spectrum On	1	0	Note 2 ±0.5% spread	Note 2 ±0.5% spread	14.318 MHz	48/24 MHz
Three-state	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Notes:

2. CPU, SDRAM and PCI frequency selections are listed in *Table 4*.
3. In Test Mode, the 48/24MHz clock outputs are:
   - X1/2 for 48-MHz output
   - X1/4 for 24-MHz output

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on Any Pin with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
ESD_{PROT}	Input ESD Protection	2 (min)	kV

3.3V DC Electrical Characteristics: (CPU3.3#_2.5 Input = 0)

T_A = 0°C to +70°C, V_{DDQ3} = V_{DDQ2} = 3.3V±5% (3.135–3.465V)

Parameter	Description		Test Condition	Min.	Typ.	Max.	Unit
Supply Current							
I_{DD}	Combined 3.3V Supply Current		CPU0:3 = 66.8 MHz Outputs Loaded[4]			365	mA
Logic Inputs							
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{IL}	Input Low Current[5]					10	µA
I_{IH}	Input High Current[5]					10	µA
Clock Outputs							
V_{OL}	Output Low Voltage		I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage		I_{OH} = –1 mA	3.1			V
I_{OL}	Output Low Current:	CPU1:3	V_{OL} = 1.5V	55	75	105	mA
		SDRAM0:11		80	110	155	
		PCI_F, PCI0:5		55	75	105	
		IOAPIC		100	135	190	
		REF0		60	75	90	
		REF1		45	60	75	
		48/24MHZ		55	75	105	
I_{OH}	Output High Current:	CPU1:3	V_{OH} = 1.5V	55	85	125	mA
		SDRAM0:11		80	120	175	
		PCI_F, PCI0:5		55	85	125	
		IOAPIC		100	150	220	
		REF0		60	85	110	
		REF1		45	65	90	
		48/24MHZ		55	85	125	

Notes:

4. All clock outputs loaded with 6" 60Ω traces with 22 pF capacitors.
5. W153F logic inputs have internal pull-up devices (pull-ups not full CMOS level).

3.3V DC Electrical Characteristics: (CPU3.3#_2.5 Input = 0) (continued)

T_A = 0°C to +70°C, V_{DDQ3} = V_{DDQ2} = 3.3V±5% (3.135–3.465V)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Crystal Oscillator						
V_{TH}	X1 Input threshold Voltage[6]			1.65		V
C_{LOAD}	Load Capacitance, Imposed on External Crystal[7]			18		pF
$C_{IN,X1}$	X1 Input Capacitance[8]	Pin X2 unconnected		28		pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH
Serial Input Port						
V_{IL}	Input Low Voltage				$0.3V_{DD}$	V
V_{IH}	Input High Voltage		$0.7V_{DD}$			V
I_{IL}	Input Low Current	No internal pull-up/down on SCLOCK			10	µA
I_{IH}	Input High Current	No internal pull-up/down on SCLOCK			10	µA
I_{OL}	Sink Current into SDATA Open Drain N-Channel Device On	$I_{OL} = 0.3V_{DD}$	6			mA
C_{IN}	Input Capacitance of SDATA and SCLOCK				10	pF
C_{SDATA}	Total Capacitance of SDATA Bus				400	pF
C_{SCLOCK}	Total Capacitance of SCLOCK Bus				400	pF

Notes:

6. X1 input threshold voltage (typical) is (V_{DDQ3})/2.
7. The W153F contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 18 pF; this includes typical stray capacitance of short PCB traces to crystal.
8. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

2.5V DC Electrical Characteristics (CPU3.3#_2.5 Input = 1)

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5% (3.135–3.456V), V_{DDQ2} = 2.5V±5% (2.375–2.625V)

Parameter	Description		Test Condition	Min.	Typ.	Max.	Unit
Supply Current							
$I_{DD-3.3V}$	Combined 3.3V Supply Current		CPU0:3 = 66.8MHz Outputs Loaded[4]			300	mA
$I_{DD-2.5}$	Combined 2.5V Supply Current		CPU0:3= 66.8MHz Outputs Loaded[4]			50	mA
Logic Inputs							
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{IL}	Input Low Current[5]					10	µA
I_{IH}	Input High Current[5]					10	µA
Clock Outputs							
V_{OL}	Output Low Voltage		I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage		I_{OH} = –1 mA	2.2			V
I_{OL}	Output Low Current:	CPU1:3	V_{OL} = 1.25V	45	70	105	mA
		SDRAM0:11	V_{OL} = 1.5V	80	110	155	
		PCI_F, PCI0:5	V_{OL} = 1.5V	55	75	105	
		IOAPIC	V_{OL} = 1.25V	55	85	130	
		REF0	V_{OL} = 1.5V	60	75	90	
		REF1	V_{OL} = 1.5V	45	60	75	
		48/24MHZ	V_{OL} = 1.5V	55	75	105	
I_{OH}	Output High Current:	CPU1:3	V_{OH} = 1.25V	40	65	95	mA
		SDRAM0:11	V_{OH} = 1.5V	80	120	175	
		PCI_F, PCI0:5	V_{OH} = 1.5V	55	85	125	
		IOAPIC	V_{OH} = 1.25V	50	80	120	
		REF0	V_{OH} = 1.5V	60	85	110	
		REF1	V_{OH} = 1.5V	45	65	90	
		48/24MHZ	V_{OH} = 1.5V	55	85	125	

3.3V AC Electrical Characteristics (CPU3.3#_2.5 Input = 0)

T_A = 0°C to +70°C, V_{DDQ3} = V_{DDQ2} = 3.3V±5% (3.135–3.465V), f_{XTL} = 14.31818 MHz
Spread Spectrum function turned off

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

CPU Clock Outputs, (Lump Capacitance Test Load = 20 pF

Parameter	Description	Test Condition/Comments	CPU = 66.8 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	15				10	10.5	ns
f	Frequency, Actual	Determined by PLL divider ratio		66.8			100.2		MHz
t_H	High Time	Duration of clock cycle above 2.4V	5.2			3.0			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5			2.8			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55			55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			175			175	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	15	20	30		13.5		Ω

SDRAM Clock Outputs, (Lump Capacitance Test Load = 30 pF)

Parameter	Description	SDRAM = 66.8 MHz			SDRAM = 100 MHz			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	15				10		ns
f	Frequency, Actual		66.8			100.2		MHz
t_R	Output Rise Edge Rate	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	1		4	1		4	V/ns
t_D	Duty Cycle	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle			250			250	ps
t_{SK}	Output Skew		100			100		ps
t_{SK}	CPU to SDRAM Clock Skew			500			500	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)			3			3	ms
Z_o	AC Output Impedance	10	15	20	10	15	20	Ω

PCI Clock Outputs, PCI_F and PCI0:5 (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	PCI = 33.4 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	30			ns
f	Frequency, Actual	Determined by PLL divider ratio		33.4		MHz
t_H	High Time	Duration of clock cycle above 2.4V	12			ns
t_L	Low Time	Duration of clock cycle below 0.4V	12			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			250	ps
t_O	CPU to PCI Clock Skew	Covers all CPU/SDRAM outputs. Measured on rising edge at 1.5V	1		4	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	15	20	30	ohm

IOAPIC Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Frequency generated by crystal oscillator		14.31818		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	8	12	15	ohm

REF0 Clock Output (Lump Capacitance Test Load = 45 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Frequency generated by crystal oscillator		14.31818		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	17	20	25	ohm

REF1 Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Frequency generated by crystal oscillator		14.31818		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	20	25	35	ohm

48/24MHZ Clock Outputs (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)		48.008/24.004		MHz
f_D	Deviation from 48 MHz	(48.008 – 48)/48		+167		ppm
m/n	PLL Ratio	(14.31818 MHz x 57/17 = 48.008 MHz)		57/17, 57/34		
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	15	20	30	ohm

Serial Input Port

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
f_{SCLOCK}	SCLOCK Frequency	Normal Mode	0		100	kHz
t_{STHD}	Start Hold Time		4.0			µs
t_{LOW}	SCLOCK Low Time		4.7			µs
t_{HIGH}	SCLOCK High Time		4.0			µs
t_{DSU}	Data Set-up Time		250			ns
t_{DHD}	Data Hold Time	Transmitter should provide a 300-ns hold time to ensure proper timing at the receiver	0			ns
t_R	Rise Time, SDATA and SCLOCK	From $0.3V_{DD}$ to $0.7V_{DD}$			1000	ns
t_F	Fall Time, SDATA and SCLOCK	From $0.7V_{DD}$ to $0.3V_{DD}$			300	ns
t_{STSU}	Stop Set-up Time		4.0			µs
t_{SPF}	Bus Free Time between Stop and Start Condition		4.7			µs
t_{SP}	Allowable Noise Spike Pulse Width				50	ns

2.5V AC Electrical Characteristics (CPU3.3#_2.5 Input = 1)[9]

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5% (3.135–3.465V), V_{DDQ2} = 2.5V±5% (2.375–2.625V), f_{XTL} = 14.31818 MHz

CPU Clock Outputs, (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.8 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25V	15			10		10.5	ns
f	Frequency, Actual	Determined by PLL divider ratio		66.8			100.2		MHz
t_H	High Time	Duration of clock cycle above 2.0V	5.2			3			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5			2.8		4	ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	0.8		3	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	0.8		3	15		45	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V			175			175	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	15	20	30	15	20	30	Ω

IOAPIC Clock Output (Lump Capacitance Test Load = 20pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Frequency generated by crystal oscillator		14.31818		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	10	15	25	ohm

Ordering Information

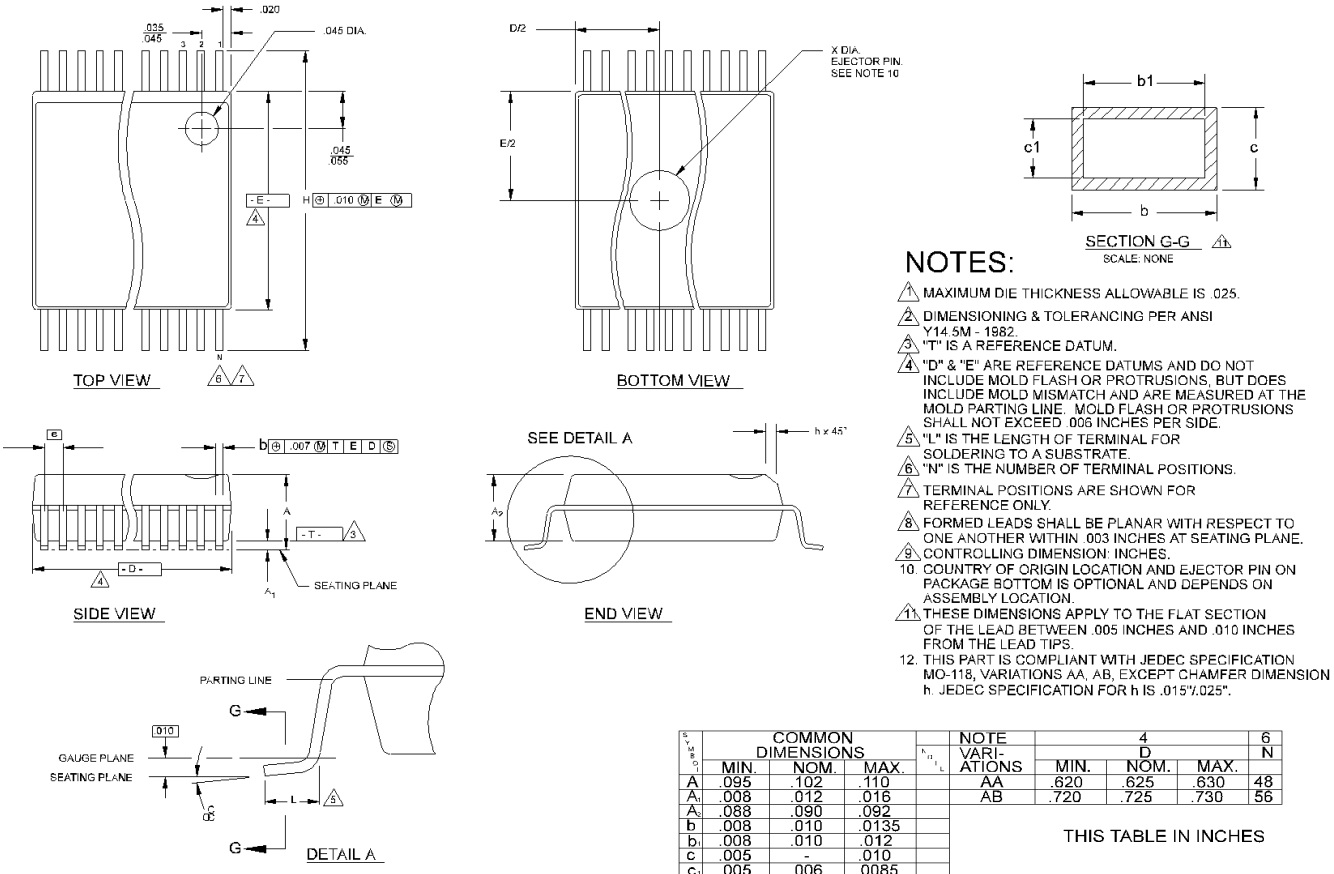
Part Number	Package
W153F	H = SSOP (300 mils)

Note:

9. AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

Mechanical Package Outline

48-Pin Shrink Small Outline Package (SSOP, 300 mils)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	.095	.102	.110	
A_1	.008	.012	.016	
A_2	.088	.090	.092	
b	.008	.010	.0135	
b_1	.008	.010	.012	
c	.005	-	.010	
c_1	.005	.006	.0085	
D	SEE VARIATIONS			4
E	.292	.296	.299	
e	.025 BSC			
H	.400	.406	.410	
h	.010	.013	.016	
L	.024	.032	.040	
N	SEE VARIATIONS			6
X	.085	.093	.100	10
α	0°	5°	8°	

VARI-ATIONS	4 D MIN.	NOM.	MAX.	6 N
AA	.620	.625	.630	48
AB	.720	.725	.730	56

THIS TABLE IN INCHES

Summary of nominal dimensions in inches:

Body Width: 0.296
Lead Pitch: 0.025
Body Length: 0.625
Body Height: 0.102

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	2.41	2.59	2.79	
A_1	0.20	0.31	0.41	
A_2	2.24	2.29	2.34	
b	0.203	0.254	0.343	
b_1	0.203	0.254	0.305	
c	0.127	-	0.254	
c_1	0.127	0.152	0.216	
D	SEE VARIATIONS			4
E	7.42	7.52	7.59	
e	0.635 BSC			
H	10.16	10.31	10.41	
h	0.25	0.33	0.41	
L	0.61	0.81	1.02	
N	SEE VARIATIONS			6
X	2.16	2.36	2.54	10
α	0°	5°	8°	

VARI-ATIONS	4 D MIN.	NOM.	MAX.	6 N
AA	15.75	15.88	16.00	48
AB	18.29	18.42	18.54	56

THIS TABLE IN MILLIMETERS

Document Title: W153F Spread Spectrum FTG for SiS530 and 620 Chip Sets Document Number: 38-07003				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111610	03/06/02	IKA	New data sheet