Spread Spectrum Clock Generator

Features

- 54- to 200-MHz operating frequency range
- Wide (9) range of spread selections
- Accepts clock and crystal inputs
- Low power dissipation
- 3.3V = 165 mw. (Fin = 200 MHz)
- Frequency spread disable function
- Center spread modulation
- Low cycle-to cycle jitter
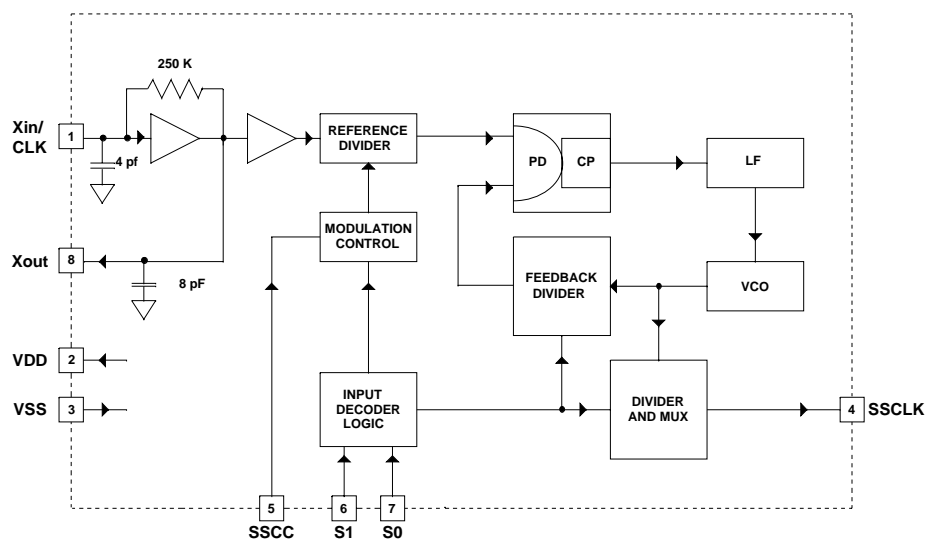- 8-pin SOIC package

Applications

- High-resolution VGA controllers
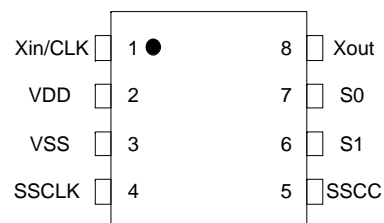- LCD panels and monitors
- Workstations and servers

Benefits

- Peak electromagnetic interference (EMI) reduction by 8 to 16 dB
- Fast time to market
- Cost reduction

Block Diagram

Pin Configuration

Pin Description

Pin Number	Pin Name	Type	Pin Description
1	Xin/CLK	I	**Clock or Crystal connection input**. Refer to *Table 1* for input frequency range selection.
2	VDD	P	**Positive power supply**.
3	GND	P	**Power supply ground**.
4	SSCLK	O	**SSCG Modulated clock output**.
5	SSCC	I	**Spread Spectrum Clock Control (Enable/Disable) function**. SSCG function is enabled when input is high and disabled when input is low. This pin is pulled high internally.
6	S1	I	**Tri-Level Logic input control pin used to select Frequency and Bandwidth**. See *Figure 1* for programming details. This pin does not have an internal pull-up or pull-down resistor.
7	S0	I	**Tri-Level Logic input control pin used to select Frequency and Bandwidth**. See *Figure 1* for programming details. This pin does not have an internal pull-up or pull-down resistor.
8	Xout	O	**Oscillator output pin connected to crystal**. Leave this pin unconnected when Xin/CLK is driven by an external clock source.

General Description

The CYPRESS SM562 is a Spread Spectrum Clock Generator (SSCG) IC used for the purpose of reducing EMI found in today's high-speed digital electronic systems.

The SM562 uses a Cypress proprietary phase-locked loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and frequency modulate the input frequency of the reference clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies of clock (SSCLK) is greatly reduced.

This reduction in radiated energy can significantly reduce the cost of complying with regulatory requirements and time to market without degrading system performance.

The SM562 is a very simple and versatile device to use. The frequency and spread% range is selected by programming S0 and S1 digital inputs. These inputs use three (3) logic states including High (H), Low (L), and Middle (M) logic levels to

select one of the nine available Frequency Modulation and Spread% ranges. Refer to *Table 1* for programming details.

The SM562 is intended for applications with a reference frequency in the range of 54 to 200 MHz.

A wide range of digitally selectable spread percentages is made possible by using Three-Level (High, Low and Middle) logic at the S0 and S1 digital control inputs.

The output spread (frequency modulation) is symmetrically centered on the input frequency.

Spread Spectrum Clock Control (SSCC) function enables or disables the frequency spread and is provided for easy comparison of system performance during EMI testing.

The SM562 is available in an eight-pin SOIC package with a 0° to 70°C operating temperature range.

Refer to SM561 for applications with lower drive requirements and the SM560 with lower drive and frequency requirements.

Table 1. Frequency and Spread% Selection (Center Spread)

54– 108 MHz (Low Range)

Input Frequency (MHz)	S1=M S0=M	S1=M S0=0	S1=1 S0=0	S1=0 S0=0	S1=0 S0=M	
54– 60	3.6	3.1	2.6	2.1	1.8	Select the Frequency and Spread % desired and then set S1, S0 as indicated.
60 – 70	3.5	3.0	2.5	2.0	1.7	
70 – 80	3.3	2.8	2.4	1.9	1.6	
80 - 100	3.0	2.5	2.1	1.7	1.4	
100 - 108	2.6	2.3	1.9	1.5	1.3	

108 – 200 MHz (High Range)

Input Frequency (MHz)	S1=1 S0=M	S1=0 S0=1	S1=1 S0=1	S1=M S0=1	
108 – 120	2.3	1.7	1.1	0.9	Select the Frequency and Spread % desired and then set S1, S0 as indicated.
120 – 130	2.3	1.7	1.1	0.9	
130 – 140	2.3	1.7	1.1	0.9	
140 – 150	2.2	1.6	1.1	0.9	
150 - 160	2.1	1.5	1.0	0.8	
160 – 170	2.0	1.5	0.9	0.8	
170 - 180	1.9	1.4	0.9	0.7	
180 – 190	1.8	1.3	0.8	0.7	
190 - 200	1.7	1.2	0.7	0.6	

Tri-Level Logic

With binary logic, four states can be programmed with two control lines whereas Tri-Level Logic can program nine logic states using two control lines. Tri-Level Logic in the SM561 is implemented by defining a third logic state in addition to the standard logic "1" and "0." Pins 6 and 7 of the SM561 recognize a logic state by the voltage applied to the respective pin. These states are defined as "0" (Low), "M" (Middle), and "1" (One). Each of these states has a defined voltage range that is interpreted by the SM561 as a "0," an "M," or a "1" logic state. Refer to *Table 1* for each logic state. By using two equal value resistors (typically 20K), the "M" state can easily be programmed. Pins 6 or 7 can be tied directly to ground or V_{DD} for logic "0" or "1," respectively.
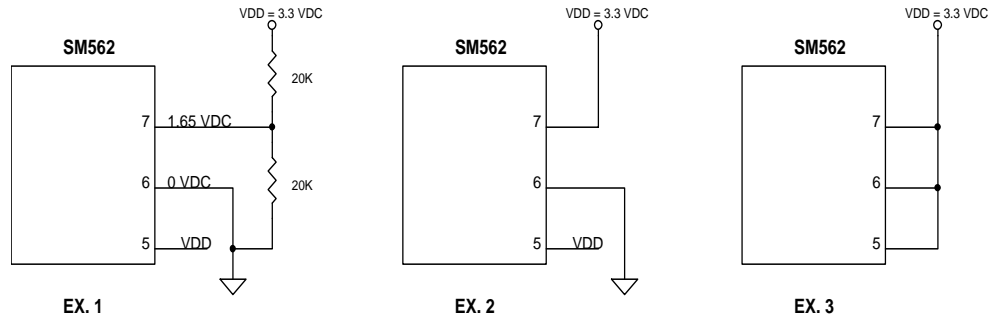

Figure 1.

Absolute Maximum Ratings[1]

Supply Voltage (AV_{DD} or DV_{DD}:.....................................+ 6V

AV_{DD}–DV_{DD}: ....± 300mV

AGND–DGND ....± 300mV

Junction Temperature: ....0°C to +70°C

Storage Temperature (10 sec. soldering): .... + 300°C

Operating Temperature:..................................... 0°C to 70°C

Storage Temperature................................. -65°C to +150°C

DC Electrical Characteristics V_{DD} = 3.3V, Temp. = 25°C and C_L (pin 4) = 15 pF, unless otherwise noted

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VDD	Power Supply Range	± 10%	2.97	3.3	3.63	V
VINH	Input High Voltage	S0 and S1 only	$0.85V_{DD}$	V_{DD}	V_{DD}	V
VINM	Input Middle Voltage	S0 and S1 only	$0.40V_{DD}$	$0.50V_{DD}$	$0.60V_{DD}$	V
VINL	Input Low Voltage	S0 and S1 only	0.0	0.0	$0.15V_{DD}$	V
VOH1	Output High Voltage	IOH = 6 ma	2.4			V
VOH2	Output High Voltage	IOH = 20 ma	2.0			V
VOL1	Output Low Voltage	IOH = 6 ma			0.4	V
VOL2	Output Low Voltage	IOH = 20 ma			1.2	V
Cin1	Input Capacitance	Xin/CLK (pin 1)	3	4	5	pF
Cin2	Input Capacitance	Xout (pin 8)	6	8	10	pF
Cin2	Input Capacitance	S0, S1, SSCC (pins 7,6,5)	3	4	5	pF
IDD1	Power Supply Current	FIN = 65 MHz, C_L = 15 pF		35	45	mA
IDD2	Power Supply Current	FIN = 200 MHz, C_L = 33 pF		50	56	mA
IDD3	Power Supply Current	FIN = 200 MHz, No Load		48	54	

Electrical Timing Characteristics V_{DD} = 3.3V, T = 25°C and C_L = 15 pF, unless otherwise noted.
Rise/Fall@ 0.4 – 2.4V, Duty@ 1.5V

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
ICLKFR	Input Clock Frequency Range	Peak-Peak = 3.0V	54		200	MHz
t_R	Clock Rise Time (pin 4)	SSCLK1, CL = 15 pF, 200 MHz	0.70	0.75	0.80	ns
t_F	Clock Fall Time (pin 4)	SSCLK1, CL = 15 pF, 200 MHz	0.70	0.75	0.80	ns
t_R	Clock Rise Time (pin 4)	SSCLK1, CL = 33 pF, 200 MHz	1.40	1.50	1.60	ns
t_F	Clock Fall Time (pin 4)	SSCLK1, CL = 33 pF, 200 MHz	1.65	1.75	1.85	ns
DTYin	Input Clock Duty Cycle	XIN/CLK (pin 1)	20	50	80	%
DTYout	Output Clock Duty Cycle	SSCLK1 (pin 4)	45	50	55	%
FM1	Frequency Modulation	Fin = 70 MHz	29.5	30.0	30.5	kHz
FM2	Frequency Modulation	Fin = 200 MHz	85.0	85.4	86.0	kHz
JCC1	Cycle-to-Cycle Jitter	Fin = 54 MHz, Mod ON		150	175	ps
JCC2	Cycle-to-Cycle Jitter	Fin =120 MHz, Mod ON		175	200	ps
JCC3	Cycle-to-Cycle Jitter	Fin = 200 MHz, Mod ON		250	300	ps

Note:
1. Operation at any Absolute Maximum Rating is not Implied.

SSCG Theory of Operation

The SM562 is a PLL-type clock generator using a proprietary Cypress design to modulate the reference clock. By precisely controlling the bandwidth of the output clock, the SM562 becomes a low-EMI clock generator. The theory and detailed operation of the SM562 will be discussed in the following sections.

EMI

All digital clocks generate unwanted energy in their harmonics. Conventional digital clocks are square waves with a duty cycle that is very close to 50%. Because of this 50/50-duty cycle, digital clocks generate most of their harmonic energy in the odd harmonics, i.e., third, fifth, seventh, etc. It is possible to reduce the amount of energy contained in the fundamental and odd harmonics by increasing the bandwidth of the fundamental clock frequency. Conventional digital clocks have a very high Q factor, which means that all of the energy at that frequency is concentrated in a very narrow bandwidth, consequently, higher energy peaks. Regulatory agencies test electronic equipment by the amount of peak energy radiated from the equipment. By reducing the peak energy at the fundamental and harmonic frequencies, the equipment under test is able to satisfy agency requirements for EMI. Conventional methods of reducing EMI have been to use shielding, filtering, multilayer PCBs etc. The SM562 reduces the peak energy in the clock by increasing the clock bandwidth, thus, lowering the Q.

SSCG

SSCG uses a patented technology of modulating the clock over a very narrow bandwidth and controlled rate of change, both peak and cycle to cycle. The SM562 takes a narrow band digital reference clock in the range of 54–200 MHz and produces a clock that sweeps between a controlled start (F1) and stop (F2) frequency at a precise rate of change. To understand what happens to a clock when SSCG is applied, consider a 200-MHz clock with a 50% duty cycle. From a 200-MHz clock we know the following.

50 % **50 %**

Tc = 5.0 ns
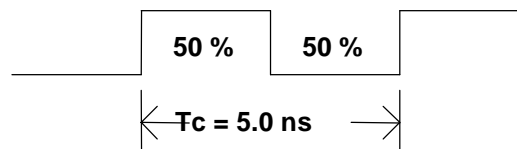
Clock Frequency = fc = 200MHz
Clock Period = Tc =1/200 MHz = 5.0 ns

If this clock is applied to the Xin/CLK pin of the SM562, the output clock at pin 4 (SSCLK) will be sweeping back and forth between two frequencies. These two frequencies, F1 and F2, are used to calculate to total amount of spread or bandwidth applied to the reference clock at pin 1. As the clock is making the transition, sweep, from F1 to F2, the amount of time and sweep waveform become a very important factor in the amount of EMI reduction realized from an SSCG clock.

The modulation domain analyzer is used to visualize the sweep waveform and sweep period. *Figure 2* shows the modulation profile of a 200-MHz SSCG clock. Notice that the actual sweep waveform is not a simple sine or sawtooth waveform. *Figure 2* also shows a scan of the same SSCG clock using a spectrum analyzer. The spectrum analyzer scan in *Figure 2* shows a 10-dB reduction in the peak RF energy when using the SM562 SSCG clock.

Modulation Rate

Spectrum Spread Clock Generators utilize frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (Fmax) and minimum frequency of the clock (Fmin) determine this band of frequencies. The time required to transition from Fmin to Fmax and back to Fmin is the period of the Modulation Rate, Tmr. Modulation Rates of SSCG clocks are generally referred to in terms of frequency or Fmod = 1/Tmod.

The input clock frequency, Fin, and the internal divider count, Cdiv, determine the Modulation Rate. In some SSCG clock generators, the selected range determines the internal divider count. In other SSCG clocks, the internal divider count is fixed over the operating range of the part. The SM562 has a fixed divider count of 2332.
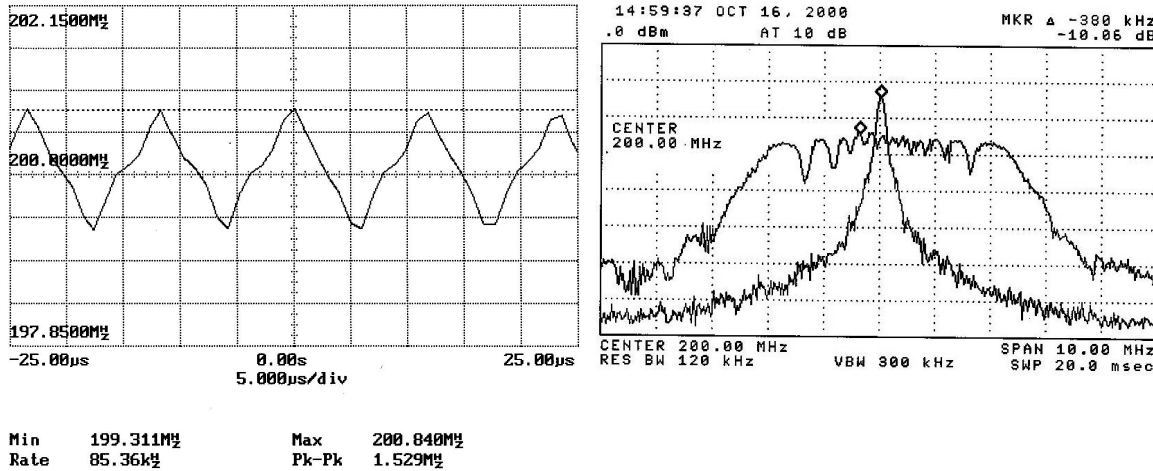
Device	Cdiv	
SM562	2332	(All Ranges)

Example:

Device	=	SM562
Fin	=	200 MHz
Range	=	S1 = 1, S0 = 1

Then;

Modulation Rate = Fmod = 200 MHz/2332 = 85.7 kHz.

Min 199.311MHz	Max 200.840MHz
Rate 85.36kHz	Pk-Pk 1.529MHz

Modulation Profile   **Spectrum Analyzer**

Figure 2. SSCG Clock, SM562, Fin = 200 MHz
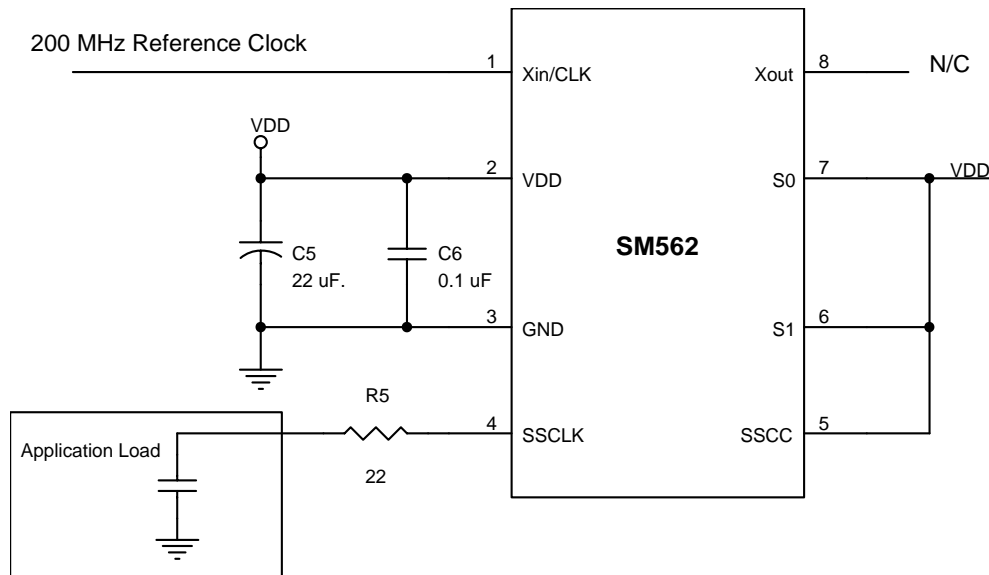
SM562 Application Schematic

Figure 3. Application Schematic

The schematic in *Figure 3* above demonstrates how the SM562 is configured in a typical application. This application is using a 200-MHz reference clock connected to pin 1. Because an external reference clock is used, pin 8 (Xout) is left unconnected.
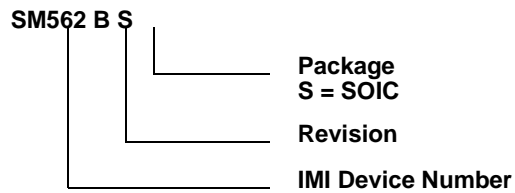
This configuration depicts the profile and spectrum scans shown in figure 3. Note that S0 = S1 = 1, for a spread of approximately 0.7%.
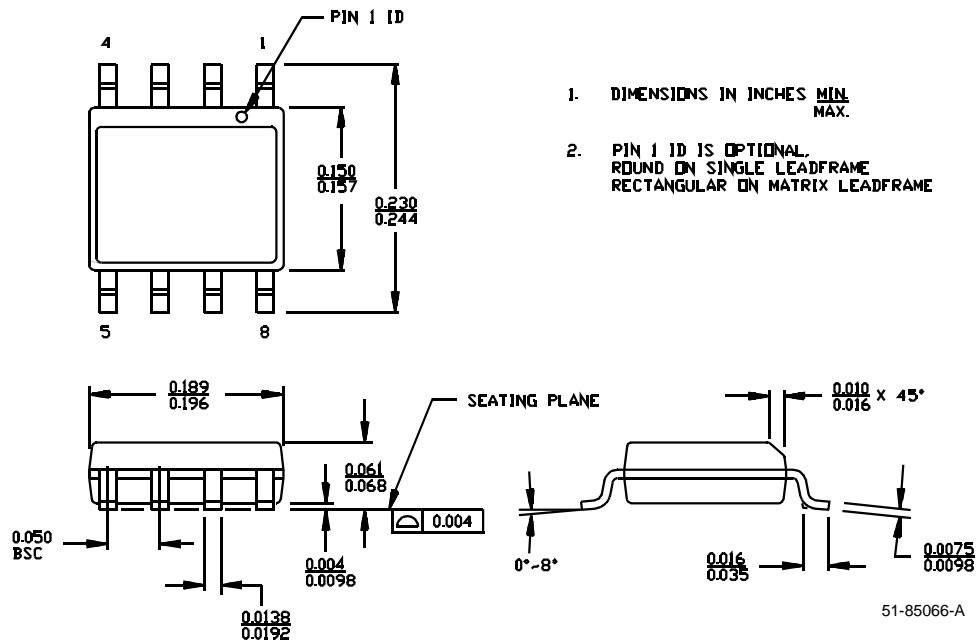
Ordering Information[2]

Part Number	Package Type	Product Flow
IMISM562BZ	8-pin SOIC	Commercial, 0° to 70°C
IMISM562BZT	8-pin SOIC–Tape and Reel	Commercial, 0° to 70°C

Marking: Example:

**IMI
SM562BS
Date Code, Lot#**

SM562 B S

Package
S = SOIC

Revision

IMI Device Number

Package Drawing and Dimensions

8-lead (150-Mil) SOIC S8

1. DIMENSIONS IN INCHES $\frac{MIN.}{MAX.}$

2. PIN 1 ID IS OPTIONAL.
ROUND ON SINGLE LEADFRAME
RECTANGULAR ON MATRIX LEADFRAME

51-85066-A

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Note:
2. The ordering part number differs from the marking on the actual device.

Document Title:SM562 Spread Spectrum Clock Generator
Document Number: 38-07022

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	106950	06/06/01	IKA	Convert from IMI to Cypress
*A	113522	05/08/02	DMG	Change the marking suffix